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Effectiveness of Using MyFPGA Platform for Teaching Digital Logic

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Effectiveness of Using MyFPGA Platform for Teaching Digital Logic

Abstract

Accompanying electric circuits and computer programming, digital logic is deemed one of the most essential parts of any Electrical and Computer Engineering curriculum, so student success in the course is critical. Furthermore, research shows that the academic performance of students is heavily dependent upon student engagement, which is believed to increase with classroom strategies such as flipped-classrooms, cooperative learning, project-based learning, and virtual labs. The University of Texas Rio Grande Valley (UTRGV) is a Hispanic serving institution with distributive campuses, where many of the students work part-time. With consideration of the special needs of our students and the latest developments in engineering education, this study focuses on our recent experience of teaching digital logical using MyFPGA, online FPGA platform.

We first introduce the MyFPGA platform in this paper. Developed by one of the authors of this paper, this web-based design features I/O interfacing circuits with an Intel FPGA hardware board as well as API web services with the Intel Quartus II design software. The platform provides 24/7 real-time hardware design experience at students' fingertips, requiring only a web browser and internet access. It exposes the students to a complete engineering design cycle that includes problem specification, block diagram design, HDL source code design, simulation and hardware verification, trouble shooting and evaluation, and reporting. We consider different cases of the platform usage in two digital logic courses. To evaluate the effectiveness of the student learning experience, data is collected using outcome assessments, student feedback and self-evaluations, instructor observations, and comparative studies. Preliminary results confirmed the effectiveness of the online digital design platform. We have also identified a few pitfalls, such as instructors' initial reluctance in adopting the platform and students' first perception of the platform as a pure simulation tool. Based on the studies, recommendations are made to identify the best practices in the utilization of the platform to better serve Electrical and Computer Engineering majors and secondary school students interested in the general STEM fields.

1. Introduction

A typical course in Digital Logic has both lecture and lab components. These two are designed to complement each other in such a way that lectures focus on fundamental concepts, theories and principles, while labs focus on hands-on experience and practical skills. This arrangement is mainly due to the convenience of having information delivered in a classroom environment, while making use of the lab resources to apply and experiment with the newly gathered information. However, keeping these two separate is neither ideal nor representative of the workplace, where engineering is a coherent and iterative process. In fact, problems often arise when the lecture and lab components are not fully coordinated. In attempt to progress engineering education, the MyFPGA platform is developed.

Building a remote laboratory such as MyFPGA has been an active research area since MIT started the iCampus research project [1], aiming at creating an online laboratory for various engineering experiments. Initiated in 1999, the iCampus project is a research collaboration program between Microsoft Research and MIT whose goal is to create and demonstrate technologies with the potential for revolutionary change throughout the university curriculum [2]. As a result of the program, five projects have been institutionalized with a great success. One of them is iLab where students can use web browsers to design experiments and collect data from distant laboratory equipment. Another example is "eDiViDe: European Digital Virtual Design Lab" [2] [3], a 3-year project funded by the Education, Audiovisual and Culture Executive Agency (EACEA) of the European Commission under the Erasmus program within the Lifelong Learning Program (LLP). The eDiViDe is a distributed digital lab platform across several institutes: KU Leuven - KHLim (Belgium), H-BRS (Germany), TUKE (Slovakia) and UiO (Norway). Each institute provides a different experiment setup. Users around the world can login to the same website and conduct experiments without the need to know the physical location of the lab. Thus, it is easily expandable. Other research activities on FPGA remote labs in Europe and Japan can be found in [4] [5] [6] [7].

Specifically, the MyFPGA platform was created with two goals. First, the platform should provide real-time hardware lab experience outside a physical lab. This allows for students to see their designs in action straight from their computers. Students will gain access to lab outside scheduled lab time 24/7 from anywhere with a computer and internet. This increased accessibility is one of the biggest benefits of the platform. Second, the online FPGA platform should provide an integrative design flow consisting of the problem statement, block diagram design, source coding, compilation, simulation, debugging, hardware verification, and reporting. With the FPGA platform, students taking a lab course will be able to verify the pre-lab work with the fast prototyping technique. They will also be able to see the lab work in the framework of a whole engineering design cycle.

In our traditional physical lab setting, a typical FPGA platform consists of a computer installed with the Intel / Altera Quartus II software and a DE-2 FPGA board. A student can then use the computer for Verilog programing and interact with the board for design verification. Creating an online FPGA platform requires three main parts: 1) board I/O interface to enable control and status data access from a computer; 2) frontend user interface to create the digital design process within

a web browser; 3) backend server to process transactions associated with Quartus II, the board and other services such as user registration.

Started in 2016, the platform has gone through some major changes and is still evolving. It was originally based on proprietary software LabView and MATLAB and used as a teaching demo tool in one course with Virtual Network Computing (VNC) remote access. The main problem was that the program had a single instance, i.e., all remote users work on the same interface. It was later implemented in 2018 with the open source Python programming language, and a desktop application with web interface was developed to allow multiple independent instances. However, such configuration would still need the installation of the software locally, so it was not portable. The current web-based platform was initially developed in 2019 using JavaScript and CSS in the frontend and python in the backend.

In the next sections, we will describe the related courses in which MyFPGA platform has been used. We will then present student surveys and usage data collected in these courses and discuss the effectiveness of the platform.

2. Related Courses

In the Electrical and Computer Engineering Department at our university, we offer ABET-accredited BS degrees in both Electrical Engineering and Computer Engineering on two campuses. In the digital area, we have two required courses: Digital Engineering I and Digital Engineering II. How the platform has been used in these two courses as follows.

2.1 Digital II

This junior or senior course teaches digital design using a hardware description language (HDL) such as Verilog. In the lab section of the course, students use the Intel/Altera Quartus II software and the DE2 FPGA hardware board. The MyFPGA platform meets the needs for this class perfectly as it provides both the Verilog source programming interface and the basic DE2 board functions.

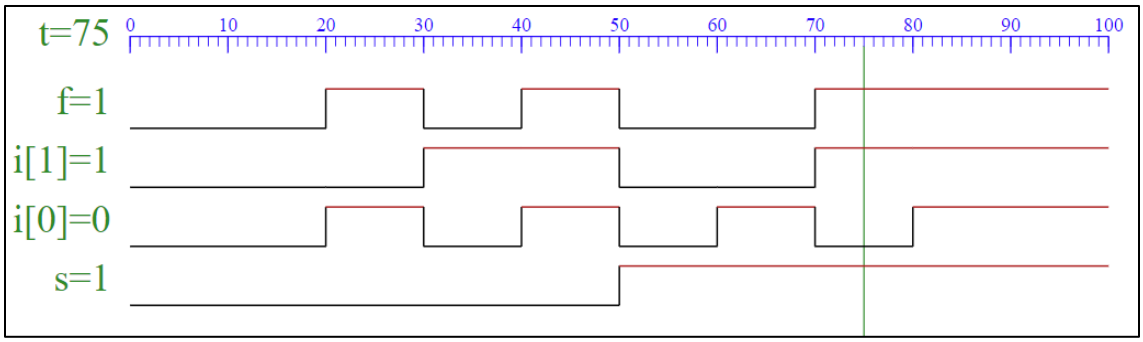
Some features of the platform are shown in Figure 1. Fig. 1a shows that the first error in the source is highlighted after compilation error occurs. This will help students fix the compilation errors one at a time. Fig. 1b shows the simulation results where s=1, f=i[1]=1. This is important for students to identify logical errors as the simulation is fast and doesn't need the hardware board. Fig. 1c shows the DE2 board interface. Eighteen switches and four key presses are used as inputs controlled by mouse clicks on a computer. Eighteen led red lights, eight led green lights and, eight 7-segment displays are used as outputs. Anyone can access the board as a viewer. When there are multiple users using the board as controllers, since there is only one hardware board there is a waitlist. The active controller is set to have a 20 second timeout limit.

```
1  module mux2(s,i,f);
2      input s;
3      input [1:0] i;
4      output f;
5      always @(*)
6          if (s)
7              f=i[1];
8          else
9              f=i[0];
10 endmodule
11
12
```

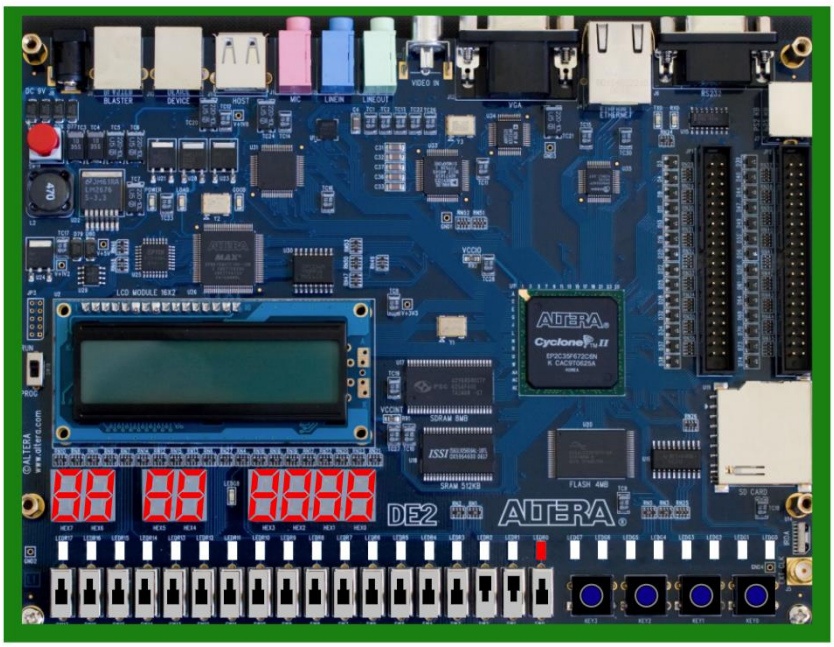
```
53 Info: Found 1 design units, including 1 entities, in source file mux2.v
54     Info: Found entity 1: mux2
55 Error (10137): Verilog HDL Procedural Assignment error at mux2.v(7): object "f" on left-hand side of assignment must have a variable data type
56 Error (10137): Verilog HDL Procedural Assignment error at mux2.v(9): object "f" on left-hand side of assignment must have a variable data type
```

☐ Info off ☐ Warnings off ☑ 1st error highlighted

(a)



(b)



(c)

Fig. 1 Example platform interfaces of a 2:1 mux design (a) source debugging (b) simulation (c) hardware verification

2.2 Digital I and Digital I Lab

This freshman or sophomore courses teach the fundamental concepts of digital logic circuits, including combinational and sequential logic. The accompanying lab requires students to use 74 series IC chips and breadboard prototyping.

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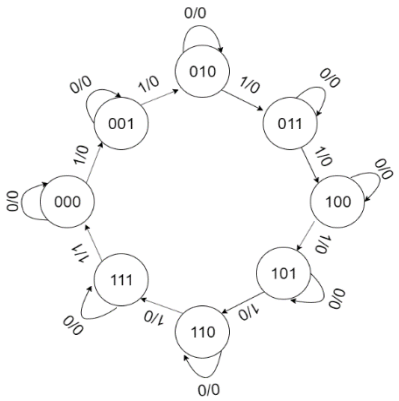


(a)

e Q2 \ Q1 Q0	00	01	11	10
00	0	0	0	0
01	x	x	x	x
11	x	x	x	x
10	0	0	1	0

J= e*Q1*Q0

e Q2 \ Q1 Q0	00	01	11	10
00	x	x	x	x
01	0	0	0	0
11	0	0	1	0
10	x	x	x	x

K= e*Q1*Q0

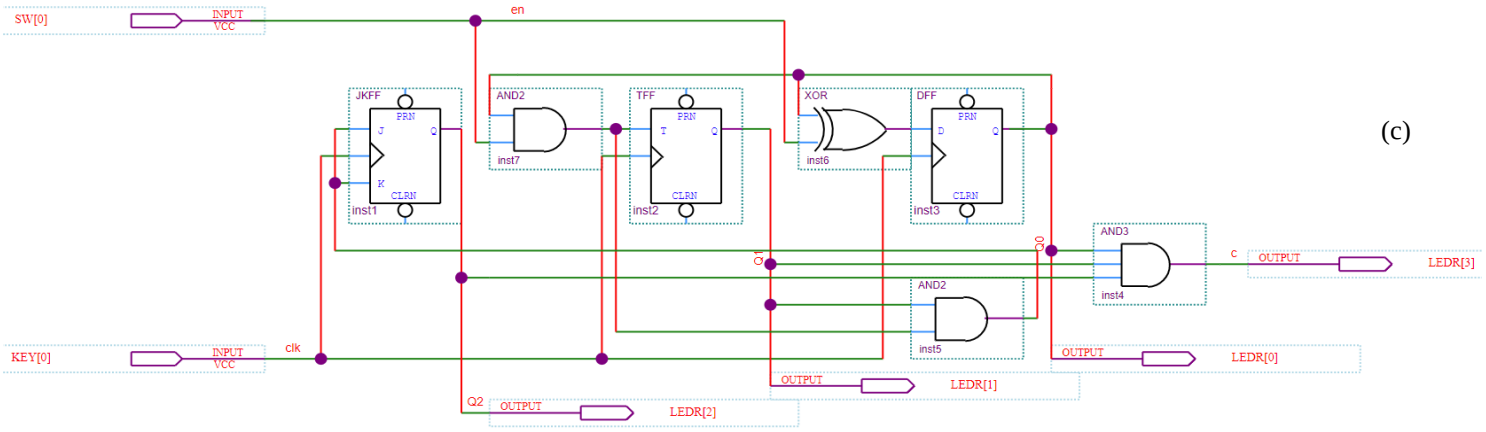
e Q2 \ Q1 Q0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	1	0
10	0	1	1	0

T= e*Q0

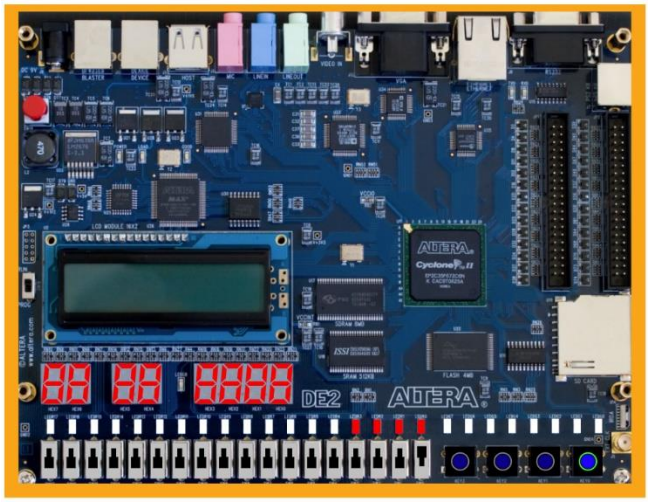
e Q2 \ Q1 Q0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	1	0	0	1
10	1	0	0	1

D= e'*Q0+e*Q0'

(b)



(c)



(d)

Fig. 2 A guided lab on design of a counter (a) state diagram (b) excitation design (c) circuit block diagram (d) board verification

MyFPGA is introduced for both the lecture and lab courses because it provides a much faster prototyping scheme than the traditional PCB prototyping. It also requires the students to focus on an important skill of block diagram-based design

An example lab on the design of a 3-bit counter using the platform is shown in Figure 2. Students will be able to not only complete the pre-lab work on the truth tables, K-maps, and logic expressions online but also check their work by clicking a button for instant feedback and a scoring report automatically generated by MyFPGA. Only after the students score 100% on the prelab work, will the circuit diagram be generated, and the students can then work on the hardware verification on the DE2 board from the web.

The challenge is that students in the introductory digital logic courses are not yet taught with the EDA design software and the FPGA technology. Therefore, it may take some time for the students to learn how to use the platform at ease.

3. Data Collection

To evaluate the effectiveness of MyFPGA for teaching digital logic, we collected and analyzed data from anonymous surveys. We also examined the platform usage data from the server.

3.1 Digital I and Digital II Survey

The students from both lecture courses taught by one instructor were asked to rate their experience with the platform regarding each of the 15 statements in the table as follows on a linear scale from 1 to 5.

Table 1. List of question for student ratings of platform effectiveness

strongly disagree (1) ----- disagree (2) ------ don't know (3) ------ agree (4) ------ strongly agree (5)

#	Statement
Q1	MyFPGA class demos by the instructor have been helpful for my learning.
Q2	MyFPGA lab exercises have been useful.
Q3	MyFPGA interface is intuitive.
Q4	I cannot relate the MyFPGA to real life.
Q5	MyFPGA interface is confusing
Q6	MyFPGA provides real-time hardware lab experience of my design.
Q7	MyFPGA shall be used next year for future students.
Q8	I want to see MyFPGA to be used more in the Digital 2 class.
Q9	I enjoy the quick results from the designed circuits using MyFPGA.
Q10	MyFPGA has no relevance to the coursework.
Q11	Using MyFPGA has made me understand things better. I would not have been able to achieve that from just lectures or the textbook.
Q12	MyFPGA was not intellectually stimulating.
Q13	I would recommend other professors adopt MyFPGA in their classes.
Q14	MyFPGA is slow.
Q15	MyFPGA is readily available from home or computer labs on campus.
Q16*	What is the most important aspect you like the MyFPGA platform?
Q17*	In which area(s) do you like the platform to be improved?

**Students were also asked to provide free written responses to these two additional questions.*

3.2 Digital I Laboratory Survey

After participating in an online lab exercise on the MyFPGA platform, Digital I Lab students taught by another instructor were given the following survey to evaluate how helpful the exercise was in their understanding the multiplexer circuits.

Q1L	Does MyFPGA help you understand the lab procedure?
Q2L	Does MyFPGA help you understand the digital theory?
Q3L	Is MyFPGA easy to use compared to a physical breadboard?
Q4L	Do you prefer to use breadboard only, combination of breadboard and MyFPGA, or MyFPGA only?

3.3 Usage data

Design files including the block diagrams, Verilog source codes, simulation results, Quartus II software generated files and lab exercise scoring report are kept on the server. Some of the files are also stored on the client side as local storage. This ensures that when a user reopens the web browser, the user may continue with previous design without starting from scratch. It will also allow the web design files to be interfaced with stand-alone programs running on a local computer.

A closer look at these files can reveal the specific type of projects a student is working on, the progress, and other information regarding the platform usage.

4. Results

4.1 Student ratings

56 responses from the survey were collected, including 36 from the Digital II class and 20 from the Digital I class. The student rating in percentages for each category on the 15 questions for both courses are summarized in Table 2 below.

Table 2. Categorized student ratings on survey questions for Digital I and II

strongly disagree (1) ----- disagree (2) ------ don't know (3) ------ agree (4) ------ strongly agree (5)

#	Digital I						Digital II					
	R1	R2	R3	R4	R5	R	R1	R2	R3	R4	R5	R
Q1	0	0	0	55%	45%	100%	0	0	0	19%	81%	100%
Q2	0	0	15%	55%	30%	85%	0	0	0	22%	78%	100%
Q3	0	10%	35%	50%	5%	50%	0	6%	11%	42%	42%	78%
Q4	10%	35%	30%	20%	5%	20%	17%	31%	44%	6%	0	42%
Q5	5%	35%	30%	30%	0	10%	17%	56%	17%	6%	6%	61%
Q6	0	0	5%	65%	30%	95%	0	0	6%	19%	75%	94%
Q7	0	0	20%	30%	50%	80%	0	0	11%	25%	64%	89%
Q8	0	0	15%	30%	55%	85%	0	0	6%	44%	50%	94%
Q9	0	0	10%	40%	50%	90%	0	0	3%	25%	72%	97%
Q10	30%	40%	20%	10%	0	60%	69%	19%	6%	3%	3%	82%
Q11	0	5%	20%	65%	10%	75%	0	3%	11%	33%	53%	83%
Q12	10%	40%	35%	15%	0	35%	44%	31%	17%	6%	3%	66%
Q13	0	5%	10%	55%	30%	85%	0	3%	3%	31%	64%	92%
Q14	30%	30%	20%	20%	0	40%	25%	44%	19%	6%	6%	57%
Q15	0	25%	30%	30%	15%	20%	3%	25%	11%	33%	28%	33%

The overall rating for survey collected from each course is calculated using

$$R = R3 + R4 - R1 - R2 \text{ for questions 4-5 ,10,12,14}$$

or

$$R = R1 + R2 - R3 - R4 \text{ for other questions.}$$

This places the ideal favorable rating at 100% for all the questions. The plot's R values for the two surveys with the 15 questions can be seen in Figure 3.

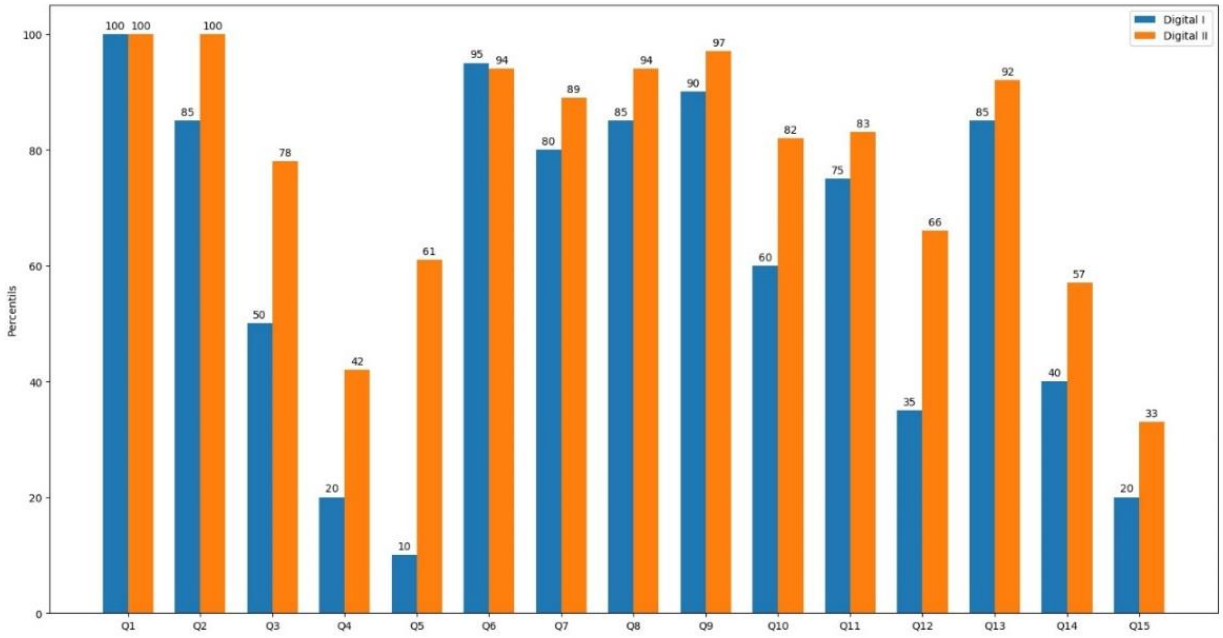


Fig. 3 Rating percentiles by questions and courses

It is observed that students have 75% or above ratings in both courses for Q1-2, Q6-9, Q11, Q13 which are related to their overall positive experience with the platform. The results confirm that the platform is perceived by majority of the students as being helpful with their learning; it is an effective tool providing real-time results from their designs, and it is recommended for future classes.

On the other hand, student ratings are below 50% in both courses for Q4 and Q15, meaning that the students had a hard time relating the FPGA to real-life and the main complaint is the limited availability of the platform.

It is also noted that ratings from the two courses follow a surprisingly similar pattern. The normalized correlation coefficient is calculated to be 0.86. The high correlation of the two sets of ratings validate the usefulness of collected data. There is a notable difference between Digital I and Digital II results: ratings from the Digital II class are convincingly higher, meaning students in the Digital II class tend to favor MyFPGA platform more. We think this is because digital design using Verilog and Quartus II is only covered in Digital II and that feature is an import part of the platform.

MyFPGA is also introduced for the Digital I Laboratory taught by another instructor. Tables 3 and 4 show the survey results from 19 students. Table 3 Q1L and Q2L are compared to the Table 2 Q1 and Q2 which are very similar in survey. Also, Table 3 Q3L is compared to the Table 2 Q3. We then see there are similar results between Digital I and Digital I Laboratory.

Table 3. Categorized student ratings on survey questions for laboratory

#	Strongly Agree	Agree	Disagree	Strongly Disagree	Overall Rating
Q1L	37 %	53 %	5 %	5 %	80%

Q2L	26 %	63 %	5 %	5 %	79%
Q3L	32 %	63 %	1 %	0 %	94%

Table 4 shows student preference on the laboratory methods to be conducted. It shows a clear preference to the use of the traditional hardware with breadboard combined with MyFPGA.

Table 4. Student preference on survey questions for laboratory

#	Breadboard Only	Breadboard + MyFPGA	MyFPGA Only
Q4L	16 %	68 %	16 %

The breadboard combined with the learning method involves the block diagram design and simulation using and prototyping on a breadboard in a traditional lab. This method may require a significantly longer laboratory period compared to the traditional laboratory method based solely on the breadboard; however, the combined method requires only slightly more time as shown in Table 5.

Table 5. Time spent on the laboratory

Method	1 hour	1 hour 20 min	1 hour 40 min	2 hours
Breadboard only	25 %	50 %	25 %	
Breadboard + MyFPGA		40 %	40 %	20 %

4.2 Most liked features

Based on the free responses from Q16, students like the fact that they can practice the designs without going to a physical lab. The word could plot in Figure 4 shows the word frequencies of the answers, showing ‘board’ as the most used word. Some of the example responses are as follows:

- “That it can be accessed in a personal computer without having to find a DE2 board.”
- “One of the best aspects I liked about MyFPGA is that it allowed me to access a DE2 board without having to go to a lab. MyFPGA allows for the ability to check if my code functions properly.”
- “I think it is nice that we can use MyFPGA from places outside of lab. It is also convenient to not be needing to ask for permission to borrow a physical board, and I like opening it up in a browser rather than setting up a bunch of wires.”
- “Being able to have a quick design right there and then.”

Fig. 4 Word clouds plot of free responses to Q16 on most liked aspect

Besides accessibility, other features liked most by the students include functionality, easiness, convenience, and quickness associated with the design. Interface was also mentioned. For example:

- "The interface is very similar to the actual Quartus program and the board interface is exactly to the real board"

Fig. 5 Word clouds plot of free responses to Q17 on areas needing improvement

4.3 Areas to be improved

We have also collected students' written responses on the platform's areas of improvement. The word clouds are shown in Figure 5. The plot shows interface as the feature that needs to be improved most. It is mentioned in 12 responses. Other features needing improvement includes accessibility (11 responses), and multiple user waitlist (9 responses). Some of the comments are listed below.

- "Being able to handle more users; A more friendly user-interface."
- "The only issue that I have with MyFPGA was that not all computers could have outright access to MyFPGA. Having to manually input the IP address in order to gain access to the platform is the only drawback for me."
- "The only improvements would be to the user interface to make it more visually appealing. There were no real problems with the functions as accurate results were obtained. The only potential thing to add would be a way to simulate multiple button presses at once."
- "The interface slightly if anything."
- "Accessible from more computers, more boards available, quick tutorial menu."
- "don't have to wait for other users stop using it"
- "I cannot think of any improvement, maybe more intuitive tutorials in the introduction of MyFPGA."

Interestingly, several features are both the most liked feature and a feature to be improved. These hold different meanings in the different contexts.

User interface: Students like that the board interface resembles that of an actual board and that the design process is similar to that of the Quartus II flow; however, students have a lot of complaints about the interface being not user friendly, meaning much work still needs to be done on the GUI design. The platform is especially challenging to the Digital I class students as they have never been introduced to concepts such as the FPGA technology and HDL programming. Q5 ratings data from Table 2 regarding the statement "the user interface is confusing" receives 40% disagreement, 30% agreement from the Digital I class and 73% disagreement and 12% agreement form the Digital II class. Students would also like the platform to have a help menu and tutorial materials available.

Availability: While students like the platform for providing access to a DE2 hardware board from a web browser, they would like more readily access to the web service. Currently, a computer needs to have its public IP whitelisted for it to have access to the platform. 15 computers in a computer lab were given access. If students want to gain access from home, they must find their computer public IP address first and then request the IP to be whitelisted.

Speed: One of the most liked features of the platform is its quickness to provide the users with the real-time results of the design. On the other hand, students don't like that they have to wait for others to finish when there are multiple users and some say they don't have enough time to finish the test before the 20s timeout. Students also complained about the wait-time for the Quartus 2 software to compile the design, which is limited by the computational power of the server.

4.4 Usage

We wanted to know when the students used the platform most frequently. We identified there to be 696 unique Verilog design files over the Fall 2019 semester kept on the server. Considering there are about 60 students in the Digital II class, the overall usage data is limited. We examined the creation time of the files and plotted the number of design files as functions of time-of-the-day

and day-of-the-week as in Figure 6a and 6b respectively. It seems that the platform is accessed mostly during the daytime of the weekdays.

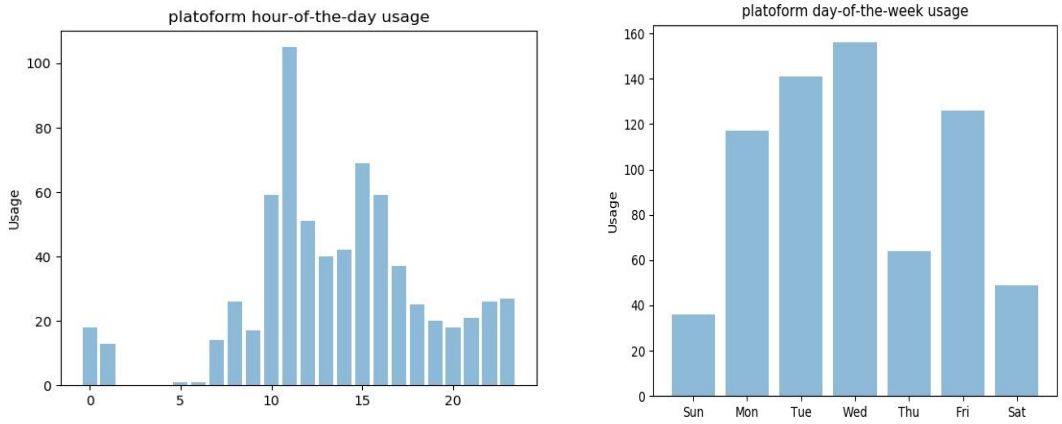


Figure 6. Platform usage (a) hour-of-the-day usage (b) day-of-the-week usage

5. Conclusions

Based on our limited experience of adopting the MyFPGA platform and the preliminary results from students' ratings and written responses, we conclude that the platform can be an effective tool for teaching Digital Logic courses.

Started as a side-project by the corresponding author, the platform is still in its early stage of development. Recommendations based on student responses to improve the platform include

- Improve user interface
- Implement a user registration and login system without IP restrictions for easier access
- Implement an online reservation system for exclusive board access for a user
- Add more boards at the server to reduce multiple user wait time
- Upgrade server and provide an option for local compilation to reduce online Quartus II software compilation time
- Add online help documentation and tutorial materials

In summary, MyFPGA platform is a useful tool to learn digital design as it provides real-time hardware prototyping capability for students from anywhere, anytime with an internet browser. Improvement in some of the platform's practical issues such as easier access to the web service, more user-friendly interfaces, reduced wait time of compilation and multi-user board access, and online help system will enhance the platform usage for greater impact on student learning.