Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: BI-WEEKLY REPORT, PART I, DECEMBER 26, 1948

To: 6345 Engineers

From: Jay W. Forrester

Date: January 2, 1948

1.0 WHIRLWIND I COMPUTER ELEMENTS

1.1 Listed by Block Diagram Number

(H. Fahnestock) Sylvania circuit schematics discussed with Stevens, Brown, Taylor, Watt. In view of present Sylvania drafting facilities, decided M.I.T. would complete revision of circuit schematics on Program Counter, Program Register, A-register, accumulator, B-register, check Register. Promised dates below.

100 Operators' Console

(H. Kenosian) A different type of push-button pulse control is being devised for the operator's console to save tubes and space. The type of push-button switches needed are being investigated in the catalogues. The switches will be tested when and if they can be obtained.

101 Master Clock

(H. Kenosian) Further conferences have been held on requirements of Master Clock and Time Pulse Distributor control circuits. The final block diagrams have been discussed, but the final model will not be constructed until the associated circuits have been developed further.

102 Program Counter

(D.R.Brown) Circuit schematic for the prototype has been started in the drafting room.- due January 5.

103 Program Register

(D.R. Brown) Circuit Schematic for the prototype has been started in the drafting room - due January 9.

104 Control Switch

(H. Fahnestock) The control switch is being worked on at Sylvania, see their report of December 19.

106 Time Pulse Distributor

(D. R. Brown) A new block diagram of the time-pulse-distributor control, D-31387, supersedes B-37076-1.

203 Flip-flop Storage

(D. R. Brown) Circuit schematics for the prototype have been started in the drafting room - due January 16.

300 Arithmetic Control

(G. C. Sumner) The arithmetic control block schematic will be issued within the next few days. Block schematics of individual panels are underway in the drafting room. Much of the past two weeks has been spent in time studies with special regard for the inclusion of flexible components in arithmetic control. Delay lines will be included to permit easy change in time phase after the computer is built by merely changing the length of delay lines. Also it was decided to make the divide time distributor a four way distributor which could be changed easily to a three way or a two way distributor. The use of these flexible components was felt advisable because of the difficulty in predicting system delays in some cases. For example, the high speed carry under certain conditions must pass through 16 serial gates.

301 A-Register

(C. W. Watt)

A. Work is continuing toward obtaining a final layout of of the A-Register.
B. The Schematic has been finished. It is No.D-31276.
C. The proposed layout will be revised to agree with the schematic.
D. The delays now consist of
   1. Bus driver decisions.
   2. Time to do the work.

302 Accumulator

A. Layout work on the accumulator was begun again.
B. Decisions on the accumulator were made that will enable the layout to continue. The main one was the decisipn to use the whiffle tree gate chain for shift and carry.
C. Layout will progress during the next two weeks.

302 Whiffle Tree Switch for Shift and Carry

(N. Taylor) The Whiffle Tree circuit has been tested sufficiently to make a decision as to its use in WWI Accumulator Design. This circuit will replace the four position crystal matrix and eliminate trouble we have experienced due to plate current unbalance in F.F. Buffer Tubes.

Circuit changes in the "Accumulator" will be of a very minor nature from now on, so construction of a proto type will commence as soon as schematics and video layout work can be processed in the drafting room to accomodate the above "Whiffle Tree" change.

Whiffle Tree Switch for Shift and Carry in the Accummulator

(J.J. O'Brien)

A. A bread-board model has been installed in the Demonstration Multiplier
B. The Switch works satisfactorily.
C. Some slight design changes may be necessary and more measurements for the records.

Flip-flop Buffers to Drive the Accummulator shift and Carry Matrix.

A. This has been dropped because of the acceptance of the Whiffle Tree Switch to replace the Matrix.
B. --
C. --
D. --
E. Some information on the subject will appear in a report on the Whiffle Tree Switch.

303 B-Register

(C.W. Watt)

A. A schematic of the B-Register was nearly completed in our drafting department.
B. --
C. The Schematic will be completed and preliminary layouts based upon them will be redone by Sylvania.

500 Input and Output Register

(D.R. Brown) The input-output register, also used as the trouble-location register, will consist of a number register, and a complement register. Block diagrams of these two registers are being prepared and will be issued with a forthcoming report. Panel space for these two registers will not exceed 28" as given in M-198.

601 Check Register

(D.R. Brown) Circuit schematic for the prototype has been started in the drafting room - due January 9.

1.22 Power Cabling
(C. W. Watt)
No new work was done on this phase of the project at M.I.T.

1.23 Video Cabling

(C.W. Watt) Samples of fixed tee connectors were received from Industrial Products Co. while a great improvement over previous fixed tee connectors, the decision to use removable tees still seems well taken.

1.3 Auxiliary Equipment

1.32 Air Conditioning

(W. C. Bohn) The complete estimate for an air conditioning system capable of removing the heat from 60 K.W., has now been received from the Carrier Corporation.

1.33 Cabinets

(J.A. O'Brien) A survey was made to determine the cabinet requirements for storage and control in WWI. The result of the survey will appear in a memorandum. These and others appear in M-197, 198, 199.

1.4 Unclassified

Standard Circuits
(J.A. O'Brien) Progress is being made on compiling the specifications for the standard circuit. Requests have been sent to all engineers concerned to submit a list of the specifications of the circuits in their charge. A few specifications have been received, but it is expected that it will be a few weeks before all required information is assembled and can be printed.

No work has been done yet on compiling standard layouts for these circuits.

Mechanical and Wiring Specifications for WWI
(C.W. Watt)

A. Work continued toward standardizing specifications for WWI.
B. Criticisms of E-79 were obtained, worked over, and a revised set of specifications is ready for discussion.
C. It is hoped decision can be reached on form, content, and scope of the specifications, and that they may be issued soon.

2.0 WHIRLWIND I RESEARCH

2.1 Circuits

2.11 Flop-flop Design and Stability

A. Nature of Present Work: (A.B. Horton)
A carefully constructed model of the ac flip-flop has been set into operation in the laboratory. Mathematical analysis of the behavior of the circuit has essentially been completed and correlation of the theoretical and experimental results is being made. A study is being made of the results to determine those parameters and characteristics of the circuit which are most influential on its behavior, and a design procedure is being devised.
B. Results of Greatest Interest
Analytical and experimental results check well, taking into consideration the difference between the design and actual values of the circuit parameters. The parameters used in the flip-flop model were selected at random from stock.
C. Future Plans
The writing of the thesis report to be submitted to M.I.T. will be started immediately.
D. -
E. More Detailed Write-ups
Thesis Progress Report #3

(J.J.O'Brien) The design of a new dc coupled circuit has been generally completed and is being tested.
The replacement of the cathode resistor by an inductance works very satisfactorily.

(N.Daggett) A study has been made of flip-flop sticking. Results indicate that it is due chiefly to a decrease of tube emission. Lowering the screen voltage of first one tube and then the other with the flip-flop triggered at a relatively low PRF seems to offer a satisfactory method of anticipating sticking.

2.15 Restorer Operation Without Trigger Tube

(J.J. O'Brien)
A. Memoranda 138 and 192 have been issued on the testing of this method
B. -
C. The Flip-flop Life Test Rack will begin a new run in Barta Building as soon as the motor generator installation is completed. It will continue to operate without trigger tubes.
One or more digit panels of the multiplier will have their trigger tubes removed and tests will be made.

2.16 Gate Generator

(J.A. O'Brien) A gate generator using a blocking oscillator made up of a 6SN7 was constructed and tested. The output was very satisfactory, the oscillator produced an output pulse ½ microseconds long, of 24 volts amplitude into 100 ohms. This condition was attained by producing extrememly high peak current, in the order of ½ amperes, in the 6SN7. The resolution time of the circuit was made as low as 2.5 microseconds.

The principle difficulties seem too be excessively high tube current. A large tube was tried in the circuit, but it was then found that the transformer was not of the proper impedance and satisfactory output could not be obtained. Further tests will have to await different type transformers.

2.23 SR-1030 Tests and Specifications

(D.R. Brown) The RMA number for the SR-1030 Sylvania gate tube is 7AK7. Specifications are now being written at Emporium and will be forwarded to us as soon as they are complete. All preaging will prbbably be done in Boston rather than Emporium. Emporium, however, will make the usual life tests before they release any 7AK7's for us.

2.24 Tube Testing

(R.L. Ellis) Retests have been made on eight 6AG7 flip-flop tubes from the multiplier. New tests, A and B, were used which simulate actual working conditions. These tests have also now been made on six new 6AG7 tubes taken from stock. Tests are being planned for the gate tube, 7AK7 as well as on 6V6, 6L6, 6Y6 tubes.

It would simplify testing if personnel desiring it would write out the test desired. This should be done on inter-office correspondence paper. Results of possible general interest should be written up as E-Series memorandums.

2.4 High-Conductivity Crystals

(D.R. Brown) On December 24, we received 35 high-conductivity crystal rectifiers. The Sylvania type number is D-344.

(R.L. Best) Work is progressing on the large panel which will simulate the horizontal driving problem; it should be ready for tests in a few weeks.

3.0 SPECIAL CIRCUITS

3.1 Five-digit Multiplier

(N. Taylor) The first major step in several weeks in improving "Multiplier" techniques has been achieved in the last few days. Multiplication is being programmed repetitively at 1000 microsecond intervals using the "Multiplier Periodic Program Control" test panel. This provides a powerful method of measuring computer performance quantitatively and will aid materially in the writing of test specifications for future testings. The "flip-flop" sticking problem is becoming more common as the tubes in the Multiplier grow older. Considerable effort is being expended to develop test methods to detect this "sticking" before it causes errors in computation. A unique feature of this problem is the time necessary to detect the failure. Repetitive testing will not uncover the sticking. It will take some flip-flops as long as a second to return erronously from a preset condition.

(H. L. Ziegler) In addition to continuous operation, the multiplier is now operating under control of the multiplier periodic program control. This equipment supplies clear, read in and multiply pulses in that order with provisions for varying the time interval between the individual pulses. By using the trigger output of a Model 5 Synchroscope as input for the control, the entire sequence of pulses can be shifted in time or phase with respect to the restorer pulses which are used to synchronize the scope.

A whiffle-tree gate tube switch has been substituted for the original crystal-matrix switch in digit #1. This was done for purposes of comparison of the relative merits of the two switches. The whiffle-tree switch which uses the new SR1030 gate tubes appears to have several advantages over the crystal-matrix switch besides its very satisfactory operation. Chief among these are less sensitivity to unbalance in the tubes used to drive it and less distortion of the transmitted shift and carry pulses.

Though the periodic program control has been in operation only a short time, it shows promise of being very valuable for study of the various multiplier circuits under actual operating conditions. At present, the cyclic multiplication operations are being carried out at a 1 kc rate.

(E. W. Sard) The "Periodic Program Control for Multiplier" has been in operation with the five digit multiplier since December 22. The set-up is able to perform a problem periodically at a rate as high as 10KC and as low as single operations.

Life Data of the Demonstration Multiplier
(J. J. O'Brien)
A. In this period life testing has been interrupted by the installation of new devices in the multiplier, and their testing. The life data immediately desired is on sticking flip-flops. The principal figure desired is the minimum plate current in a

a 6AG7 tube necessary to operate a flip-flop, and whether these tubes which are failing have had abnormally short lives.
B. --
C. Separate supplies will be installed for the screens of the flip-flop tubes. Whether this will give a test of marginal failures will be determined from life data.

3.21 Standard Test Equipment
(John O. Ely)

A. Nature of present work
1. Conferences and discussions concerning proposal on standard test equipment.
2. Revision of tentative proposal.
3. Continued investigation of pulse shaping and delay circuits suitable for use in test equipment.

B. Results
1. Discussions to date have resulted in clarification of objectives and needs for this program.
2. A delay multivibrator having range of delay from 0.3 to 5000 microseconds with recovery time of less than 8 microseconds and with features which reduce dependence of delay on tube characteristics was built and tested. Performance is not satisfactory because the delay depends on supply voltages to an extent which makes very close regulation necessary.
3. A blocking oscillator capable of producing 0.1 microseconds pulses was built. Pulse shape and amplitude were not satisfactory.

C. Future Plans
1. Revised proposal will be issued early next week.
2. Will continue work on circuits.

D. Difficulties and Delays
1. Work could be expedited if more block diagrams and timing diagrams were available to illustrate the type of timing problems which may be encountered.

3.22 Special Test Equipment

Variable Delay Pulse and Gate Generator
(H. Kenosian) The prototype with 3 channels has been completed and is undergoing final tests. As soon as the unit is complete, it will be delivered to Sylvania for their use, and one or more may be constructed for the laboratory.

Low Frequency Five-Stage Binary Counter with Trigger Phase Control

The breadboard model has been completed and tested. The schematics have been submitted to Sylvania and work is proceeding there to build them for their own use. The unit seems to be much more reliable than the GE counter for triggering synchroscopes. One of these units will be built into the variable frequency clock-restorer pulse distributor and the 2 m.c. crystal controlled clock for

the 5 Digit Multiplier.

Variable Frequency Clock-Restorer Pulse Distributor
The frequency divider section has been drawn and is being constructed. The distributor section block diagram has been completed except for the push-button circuit. This unit will be used to test the effects of P.R.F. variation on the 5 Digit Multiplier and WWI.

(R.L. Best) The pulse amplitude monitor has been completed by the electronics laboratory, and is now undergoing test. The frequency divider, which has an output near 4KC regardless of input pulse repitition frequency, will soon be turned over to the electronics laboratory to have a more finished model built.

(R.L. Massard) Present works consists of eliminating phase shift between the two push pull sides of the amplifier. This shift caused the frequency-gain characteristic to be bad in shape, as certain frequencies lagged more in one side of the output than others. The compensating circuit can be adjusted after this difference in phase shift is removed.(Reference M-125)

(R.L. Ellis) I have completed the constuction of the variable delay pulse and gate generator. Two changes have been made since. A 150 ohm resistor has been put in series with each delay control potentiometer. The 12AU7 tubes were replaced by 2C51 tubes necessitating changes in wiring.

4.0 BLOCK DIAGRAMS

(R.R. Everett)
The changes to be made in the block diagrams of R-127 have been largely decided on. A set of prints will be marked and delivered to the drafting room in the near future.

4.1 Timing Studies

(E.I. Blumenthal) A series of conferences has been held within the past two weeks onprobable changes in the block diagrams suggested by R-133 (Timing of Whirlwind I). These conferences have been attended by R. Everett, N. Taylor, D. Brown, J.A. O'Brien, C. Watt, G. Hoberg; G. Summer and myself.
Multiply and divide have been found to be marginal at 2 and 1 m.c. respectively; while the Transfer Check may or may not stop the clock in time to block the next time pulse, in event of an alarm.
The possiblilties have been suggested of:

1. Rearranging the bus-C.R. corrections to cut 0.2 microseconds off the transfer check.
2. Redesigning the Step Counter End-Carry system for faster operation (difficulties with Push Button operation may be met)
3. Redesigning the Divide Time Distributor as a 4-way switch.

Any changes will be discussed in the forthcoming revisions to the block diagrams.

(J.A. O'Brien) I participated in the several meetings concerning timing studies. A few parts of the system were found to need modification, and such modifications were proposed and discussed. Further details are contained in the Bi-Weekly Reports of E. Blumenthal, and R. Everett.

(G.G. Hoberg) A study of trouble-location methods was begun with the object of developing a logical procedure for isolating faults and predicting incipient failures of components in a computer such as WWI. This subject has been chosen as a thesis topic.