Digital Computer Laboratory
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SUBJECT: READOUT AND DIGIT-PLANE DRIVING SYSTEMS - P.B. No. 62

To: Norman H. Taylor

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Abstract: This note contains a survey of the existing readout and digit-plane driving systems as well as a survey of some of the more promising new systems that are proposed. Preliminary block diagrams with weak and strong points of each system are also included.

Introduction

In order to make an evaluation of readout and digit-plane driving systems, certain basic assumptions have been made to establish a starting point of this investigation. They are:

1. Storage Medium - it is assumed that small ferrite rings approximately 0.090 inches O.D., 0.060 inches I.D., and 0.030 inches thick will be used as the storage medium.

2. Selection System - it is assumed that the memory will be of the coincident-current single-turn type using digit-plane winding currents for inhibition of write-current pulses, and using 2:1 current ratios.

3. Readout System - it is assumed that the readout system will be destructive. Cores holding a ONE will induce a voltage pulse in a sense winding, threaded through cores in each memory plane, when interrogated by a read current pulse of essentially the same shape and amplitude as the write pulses.

READOUT SYSTEMS

Proposed Readout Schemes

1. Single Sensing Winding (Fig. 1-A)

This scheme is the present system of read-write using one sensing winding and one sensing amplifier per plane. The output of the sensing amplifier is to be a positive-going pulse applied to the negatively-biased suppressor grid of a gate tube. A strobing pulse will determine the point of sampling.

The present MTC sensing amplifier consists of 5 tubes: 3 stages of amplification, a phase inverter, and a cathode follower. The amplifier gain is from 250 to 1000. Rise time is approximately 0.3 μsecond and bandwidth is 2 mcps.

If specially-designed pulse transformers were available, the sensing amplifier design might be reduced to two stages of amplification and a cathode follower.

2. Multiple Sensing Windings (Fig. 1-B)

This is the same scheme as (1) except that the sensing winding is divided into N number of sections with one sensing amplifier for each section. This requires N times as many sensing amplifiers and tubes as scheme 1. Considering equal size planes, the delta noise per sensing amplifier would be reduced over that in scheme 1 by a factor of 1 over the square root of the number of sections.

3. Post-Write Disturb (Fig. 2-A)

This consists of scheme 1 or 2 with an added post-write disturb pulse. The post-write pulse can be generated by the digit-plane driver or by a separate driver. The duration of the post-write pulse is from 1/2 to 2/3 of the switching time. This results in a much-improved signal ratio.

If the digit-plane driver is used for post-writing, no added tubes or components in the memory system are required. The addition of the extra pulse, of course, increases the overall memory cycle time by that amount.

4. Staggered Read (Fig. 2-B)

The start of the read pulse is staggered, i.e., the read pulse on one coordinate line is delayed. This will result in having the half-selected core outputs along one coordinate line reach a maximum and decay to a small magnitude well before the point of sensing. Effectively, this reduces the delta noise to one-half that of scheme 1.

A negligible amount of additional tubes or components are required in the memory system. The memory cycle time will be increased by approximately one-half the switching time of the core and the information readout time will be increased by a factor of 2.

5. Same-Polarity Double-Read and Compare (Fig. 3-A)

This method requires a double read pulse. The first readout is delayed and then compared with a second readout in a difference amplifier. If the same noise is read out both times, they should cancel, leaving only a ONE for a core holding ONE or nothing for a core holding ZERO. A post-write disturb pulse is necessary to assure that each core produces the same half-selected output during both readouts. This results in an increased memory cycle time of over 1.6 times that of scheme 1 while the information readout time is increased at least 4 times.

6. Opposite-Polarity Double-Read and Compare (Fig. 3-B)

This method is similar to scheme 5 except that the second read pulse is opposite in polarity to the first. This allows the use of a magnetic-matrix switch or transformer driver. The first read is delayed, inverted and compared with the second read in the same manner as described in scheme 5. The rewrite may be as in scheme 1 unless magnetic-core drivers are used, in which case another pair of opposite-polarity pulses must be used. The memory cycle time is thus increased over scheme 1 by a factor of at least 1.5 for vacuum-tube drivers, or 2 for magnetic-core drivers. The information readout time is increased by a factor of at least 4.

In order to have the delta noise equal during first and second read pulses, it will be necessary to half-select all cores in a write direction prior to the readout. This further increases the overall operation time.

With the addition of integration in this sensing scheme it becomes essentially that being used at R.C.A. Laboratories. Using the integral of the outputs means that all "closed-path" noises will be cancelled out.

7. Single Read with Delay (Fig. 4-A)

If the rise and fall time of the read current pulse are equal, the $d\Phi/dt$ producing both delta noise and air-flux noise will be almost equal in magnitude and opposite in polarity at the start and finish of the read pulse. This noise can be cancelled by proper delay and comparison in a difference amplifier. A post-write pulse is necessary so that the core's history will assure more complete noise cancellation. The overall time added to the present read-write-post-write disturb system is approximately 1/3 the duration of the read gate while the information readout time may be about 3 times larger.

8. Combination of Scheme 3 with Others (Fig. 4-B)

The post-write pulse has the pronounced effect of reducing the delta noise in the sensing winding and may be incorporated with other methods in reducing the overall delta-noise outputs. Schemes 3 and 4 would be a good delta noise-reducing combination. A disadvantage, though, would be the increase in memory-cycle time. The post-write pulse is also necessary with schemes 5 and 7 in order to assure better noise cancellation.

DIGIT PLANE DRIVERS

The Problem

The insertion of binary information into the memory registers of WWI necessitates the use of inhibition pulses supplied to a digit-plane winding of each plane in the memory where a ZERO is to be written. These pulses are approximately the same amplitude and shape as the x and y selection-plane currents. They are applied during the application of x and y write current pulses and nullify the effect of these pulses on the core at the x-y intersection. MTC experience has indicated the usefulness of a post-write disturb pulse, that is a pulse applied to the digit-plane winding of every memory plane, of the same amplitude and approximately the same shape as the inhibition pulse. A convenient

time to apply this pulse is immediately after the memory write time. The post-write disturb pulse is effective in reducing the "delta" noise in large arrays when certain configurations of ONES and ZEROS are stored.

Theoretical studies of noise in large arrays predict that a reduction in noise can also be accomplished by using the post-write disturb pulse only on those planes into which a ONE has been written. This reduction of noise is of the same order as that which is obtained by using a post-write disturb pulse at the end of each memory read-write cycle irrespective of whether a ONE or a ZERO is written. The use of post-write disturb pulses only in those planes into which a ONE has been written lends itself nicely to some of the digit-plane driving schemes to be mentioned in this report since it would be difficult (in these cases) to supply a post-write disturb pulse immediately after an inhibition pulse. The problem as to whether or not a post-write disturb pulse is to be used or whether a "partial" post-write disturb or a "full" post-write disturb system is to be used is largely dependent on the nature of the memory cores and the sensing scheme to be used, therefore the relative merits of each system will not be discussed further.

Drawing once more from MTC experience we can list the tentative specifications for a WWII digit plane driver:

I_m	300 - 500 ma
Rise Time	0.3 - 0.6 μsecond
Current Regulation	$\pm$ 5%
Overshoot or Ripple on Top of Pulse	$\pm$ 5%
Inhibit Pulse Duration	approx. 2 μseconds
Post-Write Disturb Pulse Duration	approx. 1.5 μsecond
Interval between Inhibit and Post-Write Disturb Pulses	may be as small as 0 μsecond
Memory Cycle Time	5 - 10 μseconds

It may be possible to allow digit-plane currents to vary much more than $\pm$ 5% as stated above. In MTC while a "complemented checkerboard pattern" (so called worst possible pattern) was being interrogated, the digit-plane driver currents could be varied in any one of 3 digits (these were the only ones tried) + 30% from the normal operating current without causing an error. While this test was by no means conclusive it indicates that the above specification on current regulation may be too strict. Further study will be needed in this matter.

The problem at hand is to outline digit-plane driving schemes which will meet the above specifications and to list the advantages and disadvantages of each.

The Proposed Systems

To supply memory plane inhibition and possible post-write disturb pulses in WWII, four schemes are hereforth proposed:

A. Utilizing digit-plane drivers of the type currently used in MTC. Inhibition and post-write pulse currents would flow through a digit-plane winding in the plane directly coupled to the plate circuit of the output driver stage. This requires that the driver output tubes pass peak currents of approximately 0.5 ampere. A schematic diagram of such a driver which meets the tentative specifications above is shown in Fig. 6. A block diagram of such a system is given in Fig. 7. Advantages and disadvantages of this scheme are given in Fig. 11.

B. Utilizing a digit-plane driver of the same type used in part A with the exception that the plate circuit of the output stage is transformer coupled to the digit-plane winding of the memory plane. Since better transfer of energy to the digit-plane winding is attained, a saving of one of the output tubes in the circuit of figure 1 can be realized. Advantages and disadvantages of this system are given in Fig. 11.

C. Essentially the scheme described in part B with diodes in transformer secondary. An objection to the scheme proposed in part B is that the negative overshoot on the secondary of the pulse transformer is objectionable when applied to a driving line of a memory. Also if an attempt is made to keep the amplitude of this overshoot small by adjusting transformer parameters a long time is taken for the overshoot to disappear completely and the transformer is PRF sensitive. A means of overcoming either of these two faults might be to place a diode either in series or parallel with the transformer secondary. Advantages and disadvantages of this system are given in Fig. 11.

D. Utilizing switch cores. No experience has been gained with this type system, therefore a more detailed explanation will be given. Switch cores of the type now under investigation for use in x and y selection-plane driver systems could be used here. A block diagram is shown in Fig. 8 and a timing diagram in Fig. 9 while a schematic diagram of the system is shown in Fig. 10. The operation of the system is as follows: Control Pulses are (see Fig. 9) applied from a current source. The first pulse which occurs during the memory write time causes the switching of unbiased cores and a resulting inhibition pulse is applied to each digit plane where a ZERO is to be written. A removal of bias on all cores during the Post-Write Disturb time allows a second positive pulse in the control winding to switch cores not previously switched and thus a post-write disturb pulse is applied to those digit planes into which a ONE was just written. A negative pulse applied to the control winding resets all switch cores to their original state. A junction diode in the output line

FIGURE 11

	A Direct-Coupled Drivers	B Transformer-Coupled Drivers	C Transformer-Coupled Drivers with Diodes in Secondary	D Switch-Core Drivers
Experience with the system	Much experience with this system	None	None	None
Experience with components	Same as above	Fair: A little work has been gained on transformers. More work is needed. Driving circuits appear to be conventional	Fair: Same as B. Almost no work has been done with junction diodes	Fair: Experience has been gained from research on switch cores for x and y plane drivers. Almost no work done on junction diodes.
Output pulse shape	Good-can be controlled	Good	Same as B.	Can be made good by doctoring Control Pulse shape
Overshoot	Same as above	Unknown-depends on design of transformer	Same as B.	Good
Current regulation	Same as above	Appears might be good	Same as B.	Same as B
Line to line regulation	Same as above	Same as A	Same as A	Fair: may have to be controlled by selecting cores
Recovery time	Good	Poor-core must be given long time in which to recover if overshoot is to be kept small	Unknown-hoped that transformer parameters can be adjusted to give fast recovery	Good
PRF Sensitivity	Good	Subject to above	Subject to above	Good-except cores may need forced cooling to dissipate heat caused by core losses
Signal to noise ratio	∞	∞	∞	Unknown
Effect of load	Minimized by circuitry	Same as A	Same as A	Unknown
Sensing schemes not compatible with	None	No. 3 (questionable)	Same as B	None
No. of tubes per digit	5-6	4-5	4-5 plus 1 junction diode	1-2 plus 1 junction diode
No. tubes in control circuit	0	0	0	5-7
Difficulty of fabrication	Requires 32 subchasses for Z-plane drivers	Same as A	Same as A	Cores may be mounted on single frame Less components, faster assembly time

FIGURE 11 (CONTINUED)

	A Direct Coupled Drivers	B Transformer-Coupled Drivers	C Transformer-Coupled Drivers with Diodes in Secondary	D Switch-Core Drivers
Availability of tubes	Investigation of tube types for this use is now going on	Same as A	Same as A	Unknown
Availability of other components	Good	Good-except transformers unknown	Good-except transformers and junction diodes unknown	Good-switch cores in small quantities appear to be available. Junction diodes unknown.
Type of Post-Write Disturb System-compatible with	Any	Partial Post-Write Disturb No Post-Write Disturb	No Post-Write Disturb. Partial Post-Write Disturb. Probably. Full Post-Write Disturb	Same as B

of each core prevents the reset pulse of each core from being applied to the digit-plane winding of the memory planes. Advantages and disadvantages of this system are listed in Fig. 11.

Signed W. J. Canty
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S. Fine
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Approved
W. N. Papian

WJC/SF:jrt

Drawings Attached:

SA 37479	SA 54918-2
SA 37480	SA 55146
SA 37481	SA 55147
SA 37482	SA 55148
SA 37483	Figure 11
SA 37484	

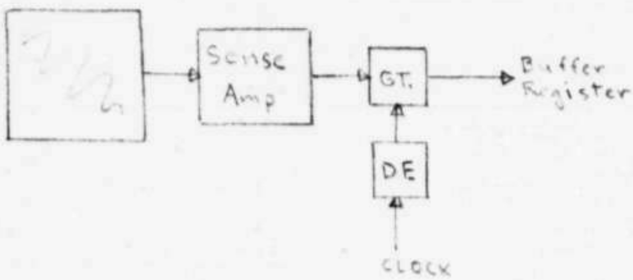
Distribution List:

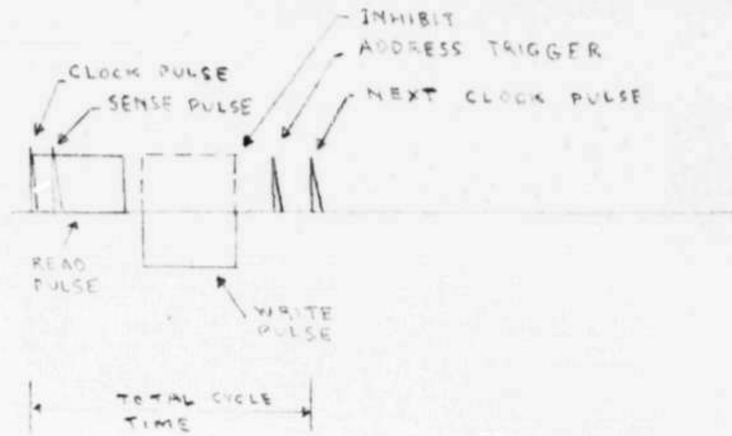
D. R. Brown
N. Edwards
C. A. Laspina
J. H. McCusker
R. A. Nelson
D. Shansky
Magnetic Memory Section

SA-03779

Scheme 1

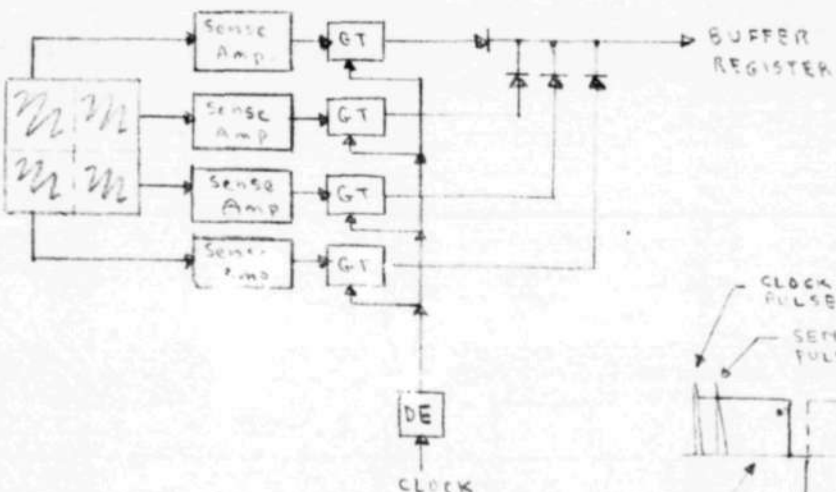
FIGURE 1-A

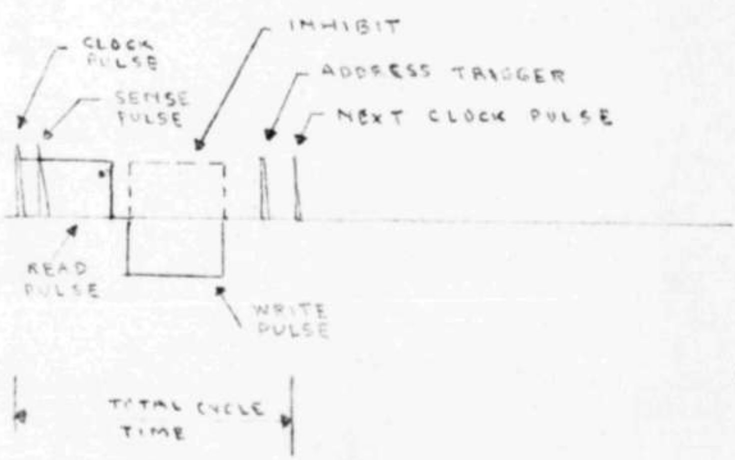




Scheme 2

FIGURE 1-B





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SA 37480

FIGURE 2-B

Scheme 4

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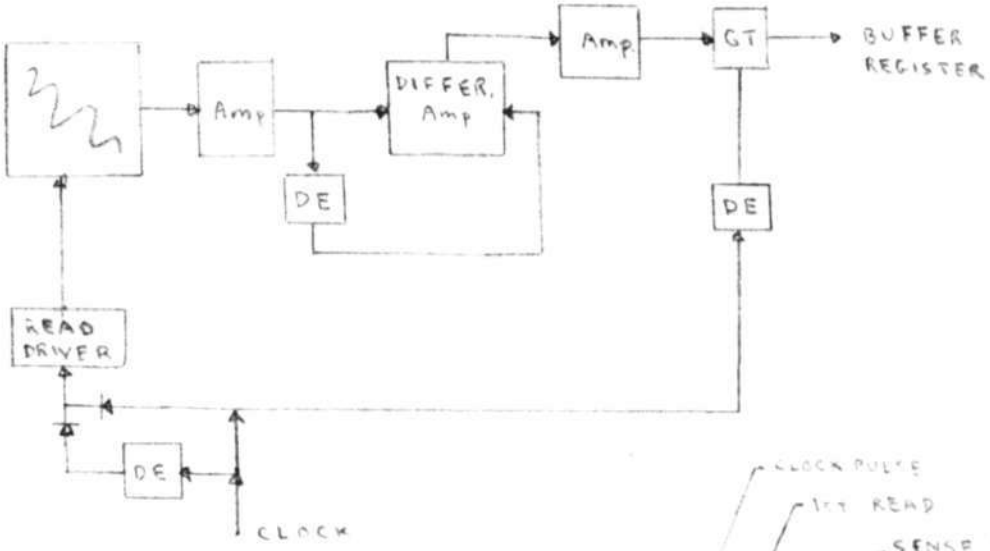
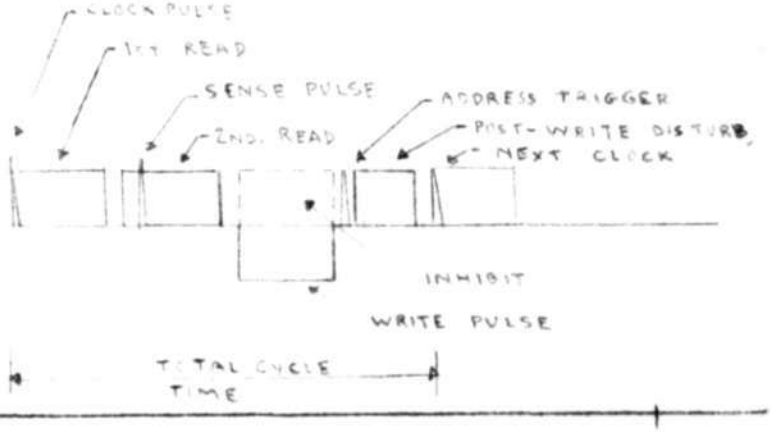
FIGURE 2-A

Scheme 3

FIGURE 3-A

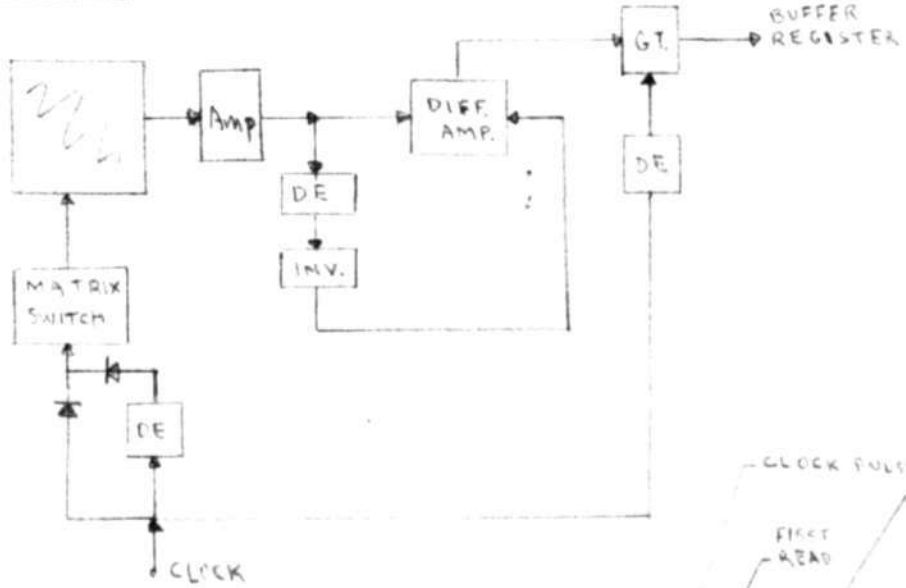
Scheme 5

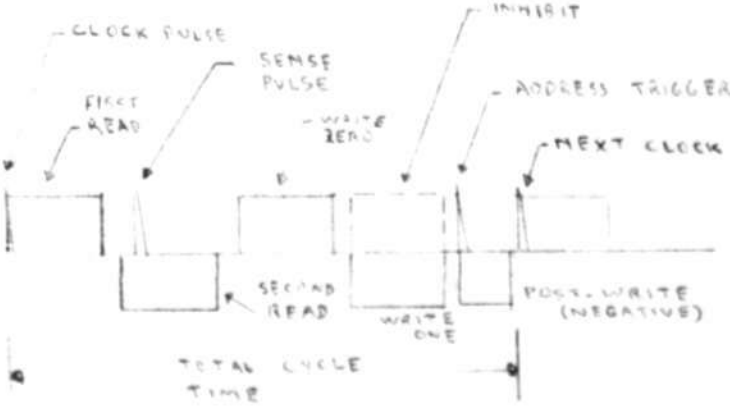




Scheme 6

FIGURE 3-B





Scheme 7

FIGURE 4-A

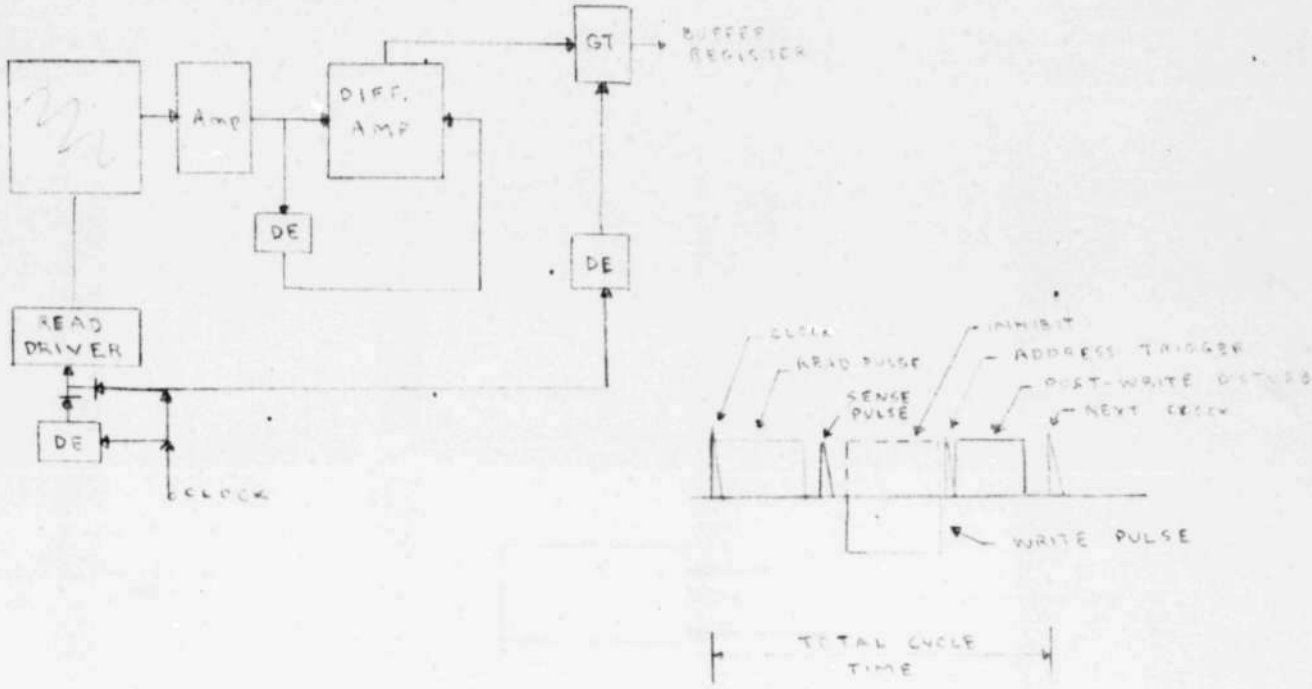
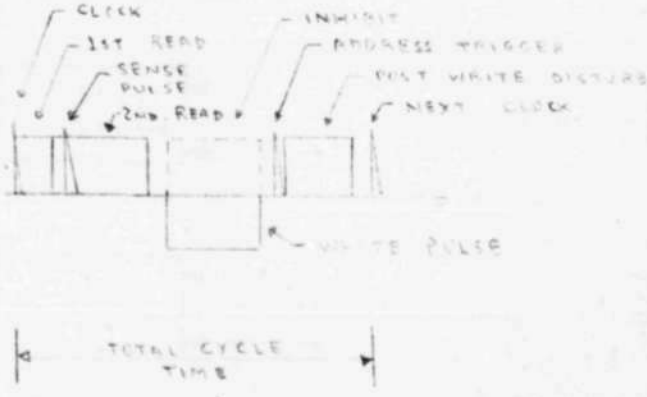


FIGURE 4-B

Scheme 8

SAME AS SCHEMES 3 AND 4.



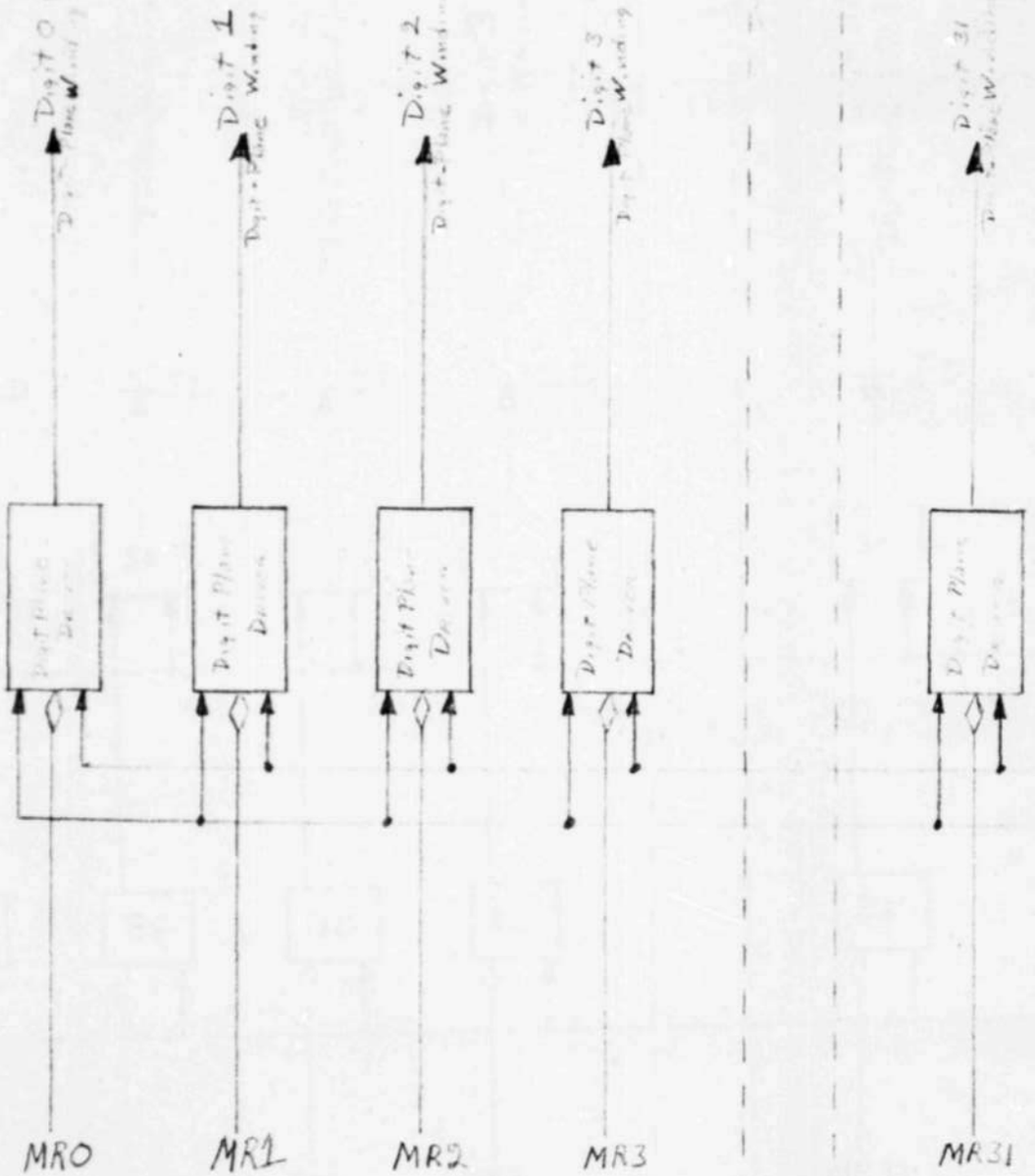


Fig. 7 .
Block Diagram: Digit-Plane Driving Scheme A, B & C.

SA 3 7+84

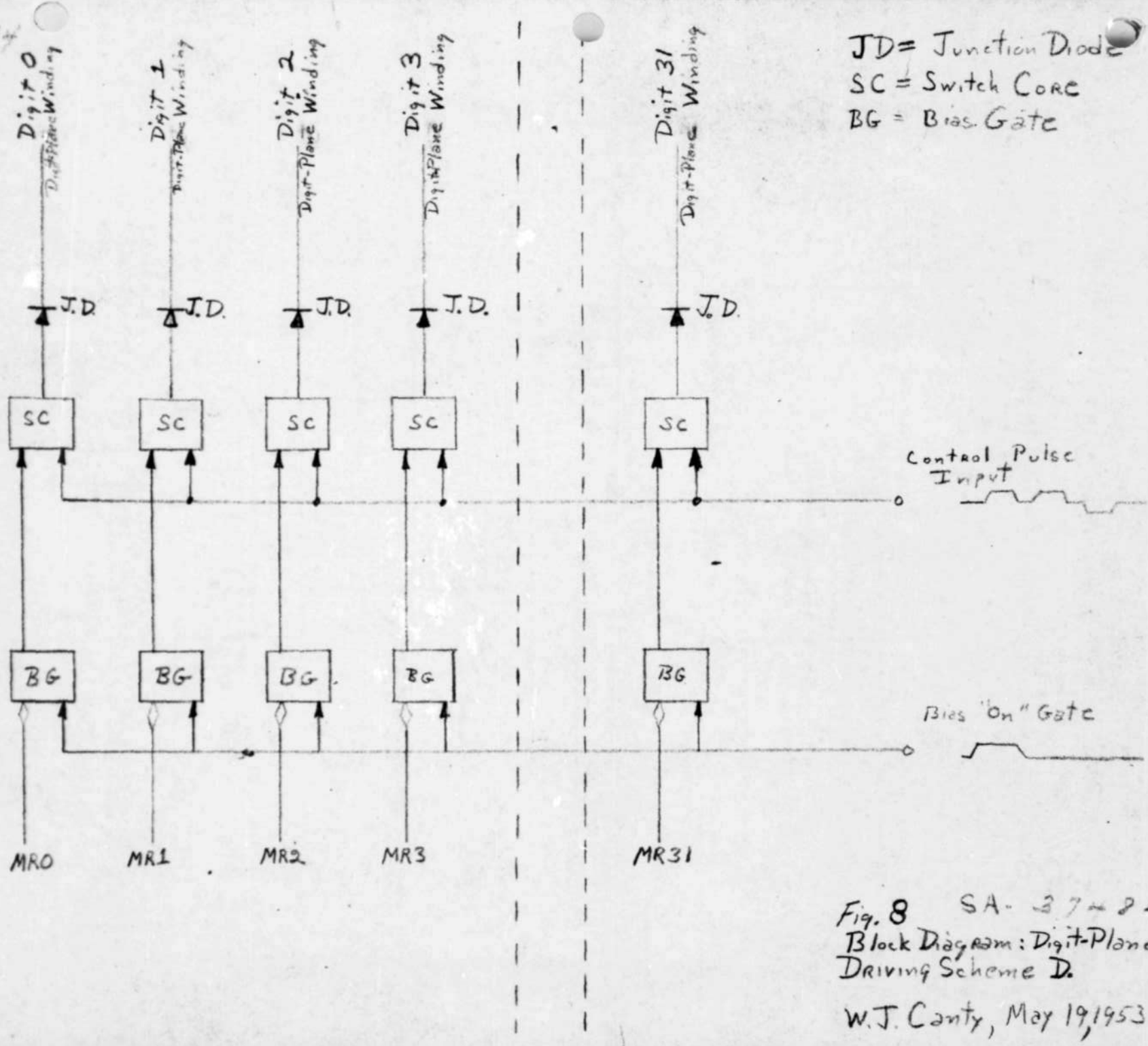


Fig. 8 SA- 3 7 + 8 4
Block Diagram: Digit-Plane Driving Scheme D.

W.J. Canty, May 19, 1953

Z (digit)-plane driver

SA-54918-2

D. Shansky

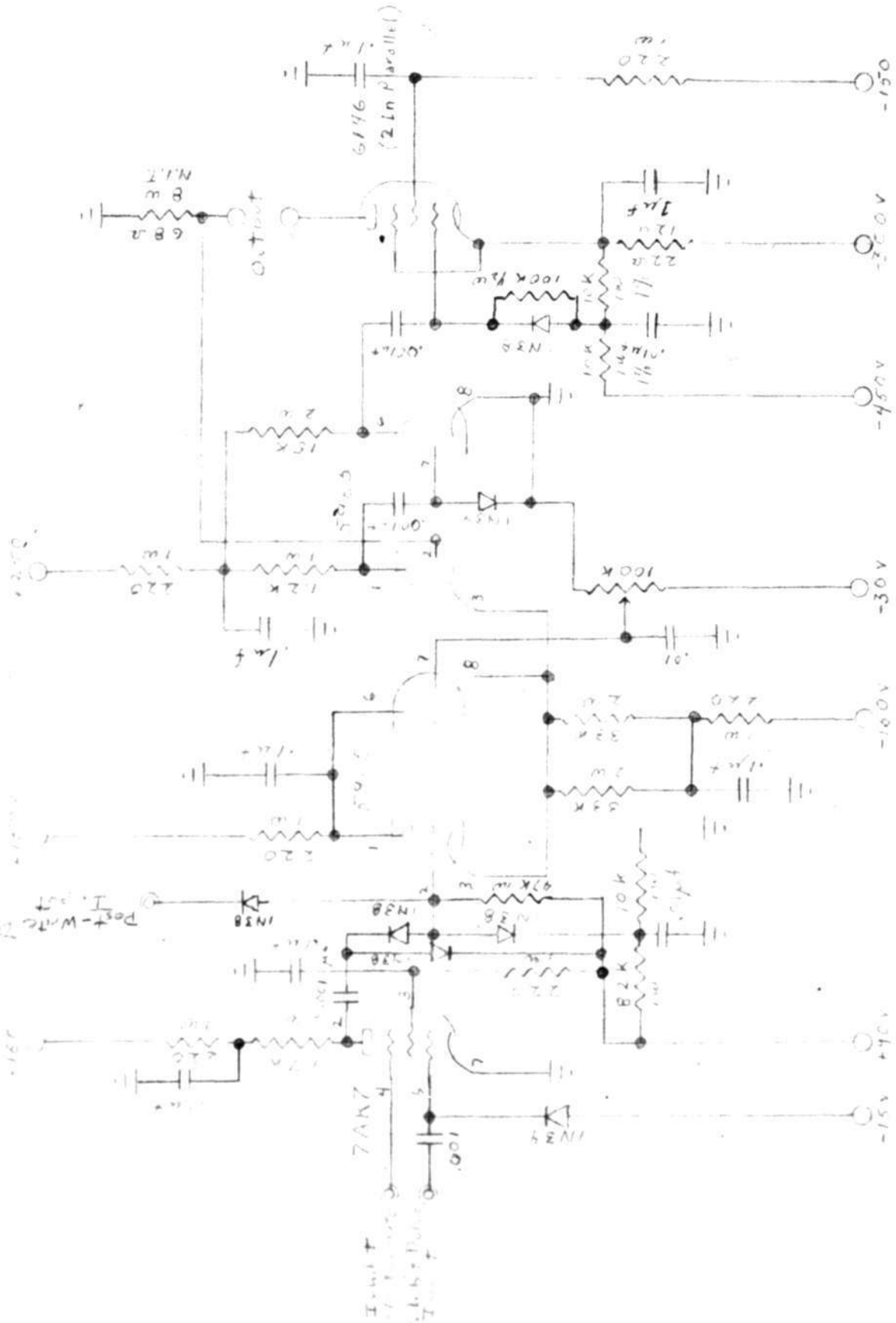


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FIGURE 5

	SCHEME 1 READ-WRITE	SCHEME 2 MULTIPLE WINDINGS	SCHEME 3 POST-WRITE	SCHEME 4 DELAYED READ	SCHEME 5 READ-READ WRITE	SCHEME 6 DOUBLE READ-WRITE	SCHEME 7 READ-DELAY WRITE	SCHEME 8 COMBINATION 3 AND 4
TOTAL CYCLE TIME	2/3 OF SCHEME 3	SAME AS 1	SPECS. REQUIRE < 6 MSEC.	SAME AS 3	4/3 TIMES SCHEME 3	3/2 to 2 TIME SCHEME 3	7/6 TIMES SCHEME 3	SAME AS 7
DELTA-NOISE REDUCTION	NONE	$\frac{2}{N}$ SECTIONS THAT OF 1	CONSIDERABLE	1/2 THAT OF 1	NEARLY COMPLETE	NEARLY COMPLETE	NEARLY COMPLETE	MORE THAN 2 OR 3
AIR-FLUX NOISE REDUCTION	NONE	SAME AS ABOVE	NONE	SAME AS ABOVE	COMPLETE	COMPLETE	COMPLETE	SAME AS 4
DRIVERS TO BE USED	ANY TYPE	ANY TYPE	ANY TYPE	ANY TYPE	VACUUM TUBE ONLY	ANY TYPE	ANY TYPE	ANY TYPE
EXPERIENCE	EXTENSIVE	NONE	EXTENSIVE	SOME	SOME	NONE	SOME	SOME
EFFECTIVE CORE UNIFORMITY	CRITICAL FACTOR	SAME AS 1	LESS THAN 1	SAME AS 1	NOT AS CRITICAL AS OTHERS	SAME AS 5	SAME AS 5	SAME AS 3
POST-WRITE DISTURB NEEDED	NO	NO	YES	NO	YES	YES (No 4)	YES	YES
NUMBER OF TUBES REQUIRED	32 TIMES NUMBER IN ONE AMP. (160)	N TIMES SCHEME 1	SAME AS 1	SAME AS 1	SCHEME 1 PLUS $\geq$ 64 (224)	SAME AS 5	SAME AS 5	SAME AS 1
ADDED LOGIC (COMPARED TO SCHEME 3)	LESS	LESS		YES	YES	YES	YES	YES
ADDED COMPONENTS (COMPARED TO SCHEME 3)	NO	N-TIMES MORE		NO	YES	YES	YES	YES
INFORMATION READOUT TIME (COMPARED TO SCHEME 3)	SAME AS SCHEME 3	SAME AS SCHEME 3		TWICE THAT OF SCHEME 3	4 TIMES THAT OF SCHEME 3	4 TIMES THAT OF SCHEME 3	3 TIMES THAT OF SCHEME 3	SAME AS SCHEME 4

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Timing Diagram: Digit-Plane Driving Scheme D.

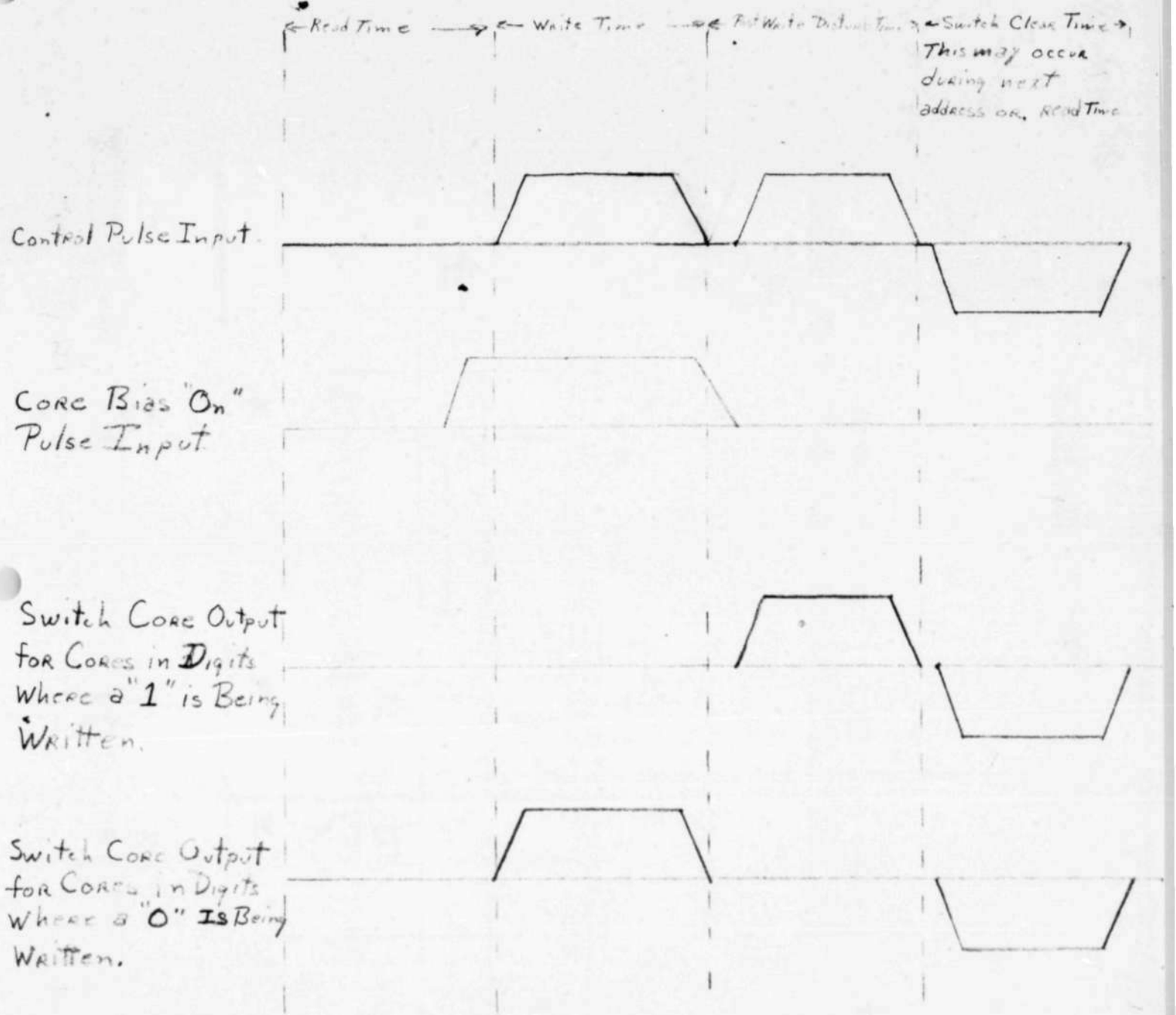
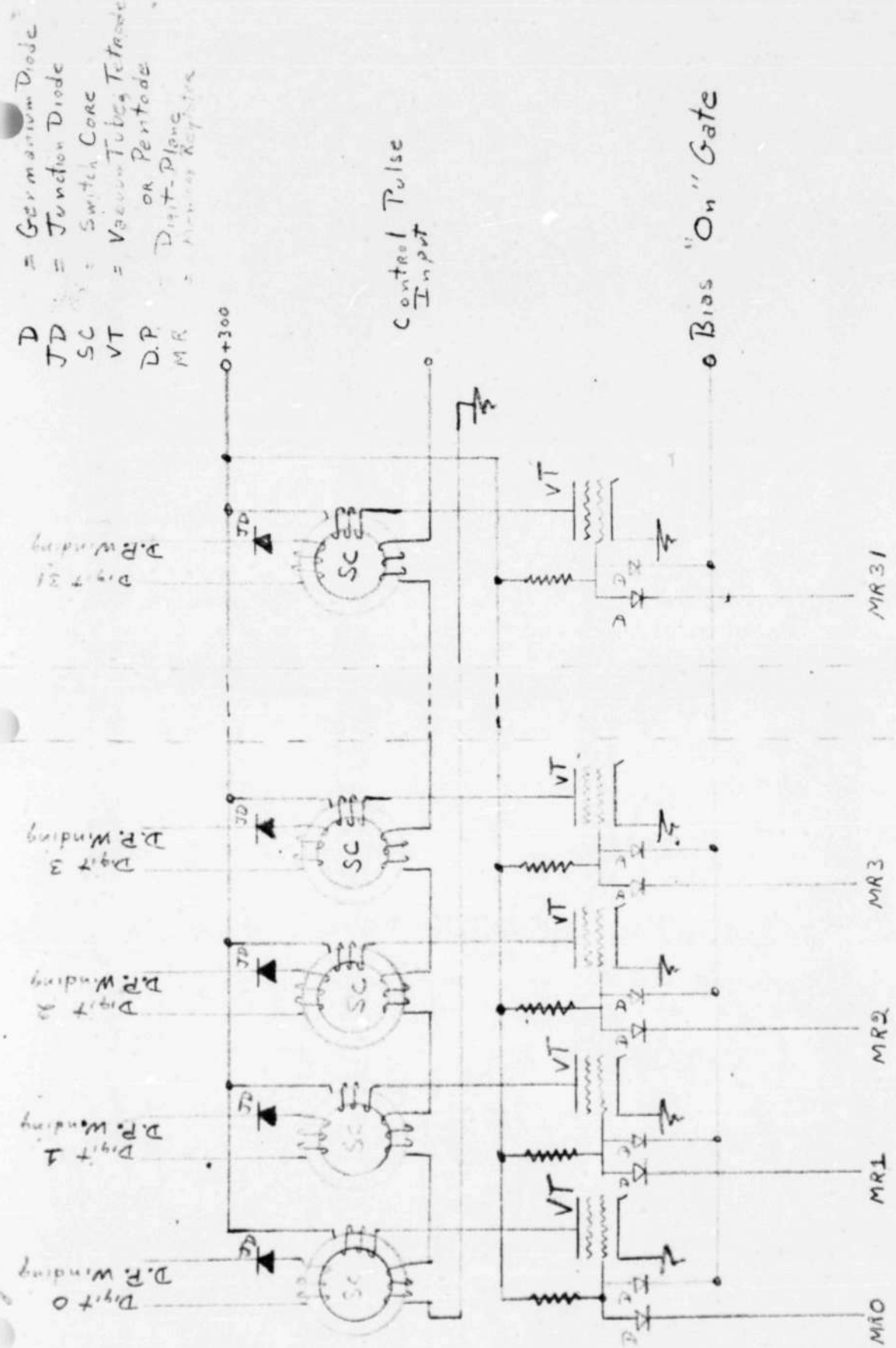


Fig. 9

SA-55-1

W. J. Canty May 19, 1953



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