Digital Computer Laboratory
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SUBJECT: WWII BLOCK DIAGRAMS MEETING OF APRIL 22, 1952

To: WWII Planning Group

From: R. P. Mayer

Date: April 30, 1952

Abstract: This report summarizes the discussion of the meeting for the benefit of those who may want to trace the development of thought on this subject.

Present: G. Briggs, D. Brown, S. Dodd, R. Everett, J. Forrester, H. Grosch, R. Mayer, I. Reed, N. Taylor

The first part of this meeting was devoted to a brief discussion of methods of designing a stepping register type of control. This control is to be used with the single-register computer that has been under investigation. In particular, a previously suggested method of operating the shift instruction was discussed. At the end of program timing the electronic register contains the number which specifies the number of shifts, so the electronic register is used as a counter until an overflow occurs, and then the number from AC is transferred to the electronic register and shifted the proper number of times. In this system the shift takes a constant number of steps. The count-number is used to specify how many of these steps should NOT shift, so that by the time the stepping is completed, the desired number of shifts will be performed. Another proposal was sketched on the board showing how a selection matrix would be used to start the chain of shift-command cores at the proper place to provide the correct number of shifts. Some other methods of controlling the shift were mentioned briefly.

It was then suggested that these details concerning how the shift should operate are not important at this time. Several ideas were expressed as to where the project of designing a new computer should begin and how it should progress. Some thought that the problems to be handled by the computer should be analyzed first, others felt that the components to be used should be discussed first, and still others felt that the logical design of the computer should be

analyzed first. The system under which we have been operating up to now, and under which we will probably continue to operate, is based on the premise that we should start with the absolute minimum number of components possible in a working computer and then add new components to it in a step-by-step fashion, getting concrete figures as to how much complexity is added at each step and how much time is gained at each step, as well as concrete figures on the number of components, reliability, etc., if these are obtainable. Following this procedure, we should eventually end up with a computer suitable for the task at hand and yet containing components which we know are being used to their maximum efficiency.

It is possible that this technique will require too much time in order to do all the required careful analysis at each step. An alternate approach is to review very roughly the speed requirements and start the program with a more or less realistic design of a complete computer. Then the additional time can be spent in analyzing and refining this design. Following this method, R. Everett has come up with some ideas which he explained to us as follows: Using some figures for the probable frequency of use of various instructions in programs for which the computer is designed and using some rough designs of simple computers, it can be shown that the average operation in a one-register computer will have 9 storage access times (AT) and 9 pulse times (TP). A two-register computer will have 5 AT and 9 TP. A three-register computer will have $3\frac{1}{2}$ AT and 9 TP. A computer with three registers plus a program counter will have $2\frac{1}{4}$ AT and 8 TP.

From this analysis, it looks as though at least three registers should be used, and probably three registers plus a program counter. If the latter is used, it is interesting to notice that most of the time is spent in high-speed carry during a multiply operation. High-speed carry for other operations is usually masked by access to storage. It would be desirable to speed up the high-speed carry, and if it cannot be done by simply speeding-up the electronic circuitry, then it may be necessary to use the carry flip-flops with the shift-and-carry technique used in WWI. If a matrix adder increases the speed, it should be considered also.

It was mentioned that the CADAC computer uses crystal matrices and is "very reliable". It was suggested that S. Dodd should investigate the CADAC computer to find out how reliable it is in terms of WWI reliability and WWII desired reliability.

It would be nice to have a B-box type of order, but this would seem to require a great deal of equipment. (Perhaps some equipment can be saved if the B-box indication is programmed on the instruction previous to that on which it should be used.)

Since it may be desirable to have at least two memory systems in the computer, it may be worthwhile to consider using one memory exclusively for operations and the other exclusively for numbers, so that a program counter would control one and a selection register the other. A computer designed in that way could probably be made to operate rather rapidly, since each re-write into storage can be done while the other storage is being used.

There are several possible ways of modifying the operations in such a split memory. One of the storages could have odd addresses, and the other could have even addresses. A B-box technique could be used for modifying any instructions. The operation memory could be arranged so that it could be changed only by large block transfers from the drum. Perhaps the best system is to have a transfer-digits order (and other special orders) arranged to actually modify a register in the operation memory.

We should be careful not to make such a system too complicated, but it is possible that the instructions in this computer could be fast enough (4 or 5 microseconds) so that it would not need to have special built-in instructions. This could mean that the very complicated central control is replaced by a somewhat less complicated method of operating the dual-storage system.

We have heard a number of times about a deadline sometime in June. J. Forrester was asked to clarify just what is required by this deadline.

By sometime in June, probably the end of June, we should know the kinds of physical components we need. For example: we should know whether we are going to use the three-dimensional memory, the step register control, and the electronic arithmetic element. After this, nine months can be spent in deciding the number of components required and how they should be interconnected. In this calendar year, we should develop the components and settle the block diagrams. In the following year, we should produce the full design from the complete block diagrams.

This means that by the end of June the materials groups should be able to tell us what techniques will be available for us to use and which techniques are not worth further investigation. It is necessary, however, for the block diagrams group to point out what kinds of components are desirable, so that the materials groups can investigate such components and see if they are worth considering further.

It was suggested that at the next meeting, on Thursday, Reed and Jeffrey should present Reed's simple computer to the group, showing both the equations and the block diagrams. The object will be to show how the method of Boolean algebra can be applied to the design of a computer. It is planned that some literature on Boolean algebra and on Reed's computer will be available before Thursday's meeting.

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