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SUBJECT: MAGNETIC CORE MATRIX SWITCH ADDER

To: N.H. Taylor, Memory Section, and Arithmetic Element Section

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Abstract: The principle of operation of the three input-two output matrix adder is based upon the saturable transformer characteristics of the magnetic cores. The control and driving windings are matrix connected. This presents a selection scheme which produces an almost instantaneous addition or subtraction of two binary numbers. The carry propagate time is about 0.07 μsec per digit for a pulse length of 0.5 μsec at a PRF of 1 mc.

Principles of Operation

The application of the magnetic core in the matrix switch depends upon the utilization of its non-linear properties. The core as a non-linear device has two states, a low impedance and a high impedance state, and the more pronounced the non-linearity the more satisfactory is the unit as a two-state element. Figure 1 shows the flux-current characteristics of a magnetic core. The points "X" and "Y" represent two residual magnetic flux conditions. The nearly horizontal parts of the curve (flux saturation portions) represent the low impedance state, and the high slope portions of the curve represent the high impedance state of the core.

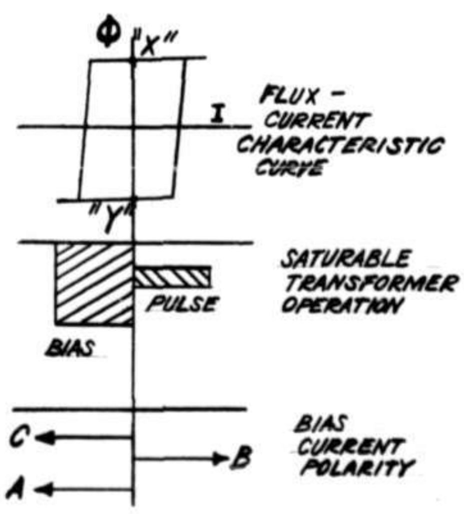


Figure 1

The core operates in the matrix as a saturable transformer. The saturable transformer must have windings which will perform three essential functions: (1) apply an input signal, (2) control the output, and (3) sense the output. The input signal appears as a current pulse. The control function appears as a bias current which must be opposite in polarity from the input signal and equal to or greater than it in amplitude. The output appears as a voltage pulse.

The magnetic flux change in the core will be small if a signal is applied when a bias current exists. If the pulse is applied when the core does not have a bias, the flux change will be a maximum if the residual flux condition of the core is such that the pulse will cause it to switch to the other of the two conditions (i.e., from the "X" to the "Y" condition if the core originally held "X", or from the "Y" to the "X" condition if the core originally held "Y"). The flux change will induce a voltage in any sensing winding on the core. The induced voltage is proportional to the product of tne number of turns of wire and the time rate of change of the flux.

The utilization of the saturable transformer characteristics of magnetic cores as the basic building block in the matrix selection scheme has been presented in an M.I.T. Thesis by K. Olsen. This material is now available in Report R-211 (A Magnetic Matrix Switch and Its Incorporation into a Coincident-Current Memory).

Figure 2 shows one digit of the magnetic core matrix switch adder as it is presently being operated. The table of binary numbers lists all the combinations of three variables (input) and the corresponding sum (S) and carry (CR) outputs from the addition of each of the combinations. The binary numbers are realized in the matrix by the circuits labeled "1" and "0", each of which has windings on four of the eight cores. The "A", "B", and "C" inputs are represented by bias currents of the polarity shown in Figure 1, except that the "C" bias current is reduced to zero during the interval of the input pulse. The "S" and "CR" outputs are represented by the pulse which occurs at either the "1" or "0" circuit terminals.

INPUT			OUTPUT	
A	B	C	S	CR
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

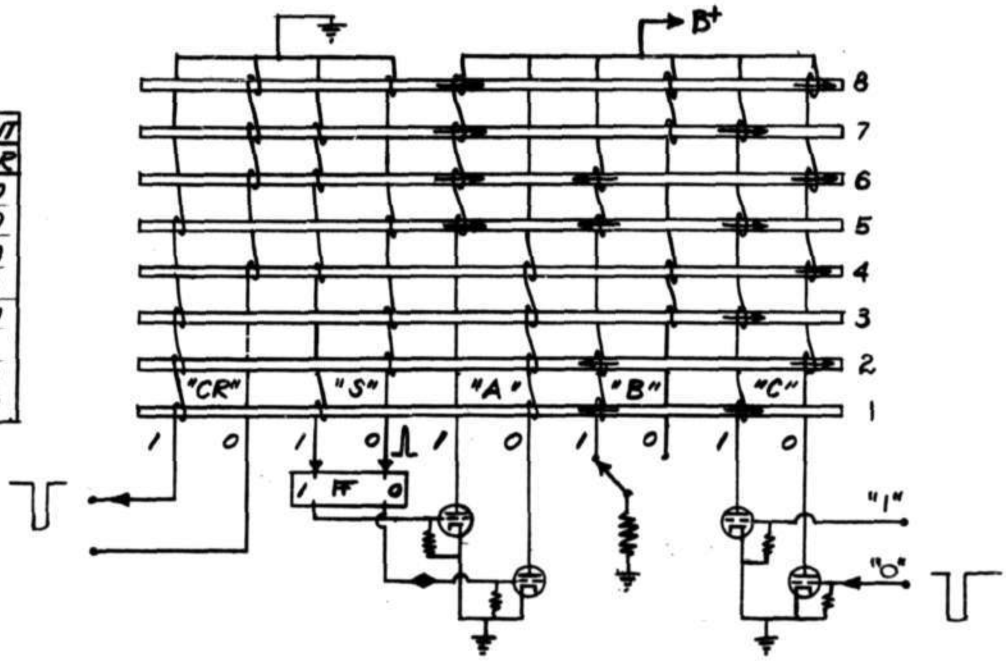


Figure 2

The magnetic flux direction is shown by the **arrows on the** cores and the pulse waveforms are shown at the input and outputs of the matrix for the addition: A = 1, B = 1, C = 0 ⟶ S = 0, CR = 1.

The C_0 and C_1 windings of the matrix are connected in the plate circuits of the 6Y6 tubes. All eight cores are biased by the current in the C windings with approximately 5.5 amp-turns of the polarity shown in Figure 1. This bias is changed only during the pulse, at which time its value is zero for the four cores affected by the C winding that is pulsed.

The A and B windings introduce the two binary numbers to be added or subtracted in the matrix by biasing certain of the cores with the polarity shown in Figure 1. The magnitudes of the A and B bias currents are approximately equal to 4 amp-turns. The C bias is sufficiently large to assure that any core that may have been switched will have its magnetic flux returned to the same orientation that existed before the arithmetic operation. This clears all cores for the subsequent switching operation. The resultant bias from the combination of C and B bias amp-turns is about 1.5 amp-turn. This value is somewhat greater than the coercive force of the core material.

Suppose that the addition (A and B) is to be performed when A = 1 and B = 1. The A_1 windings will supply bias to cores 5, 6, 7 and 8. This bias adds to that already being furnished by the C_1 and C_0 windings. The B_1 winding supplies bias to cores 1, 2, 5 and 6, but of opposite polarity from the "A" and "C" bias currents. The application of the negative pulse to the grid of the tube connected to the C_0 winding will remove the C_0 bias during the pulse and this will cause a change in the resultant bias on cores 2, 4, 6 and 8. The bias currents and their resultants for these four cores are shown in Figure 3.

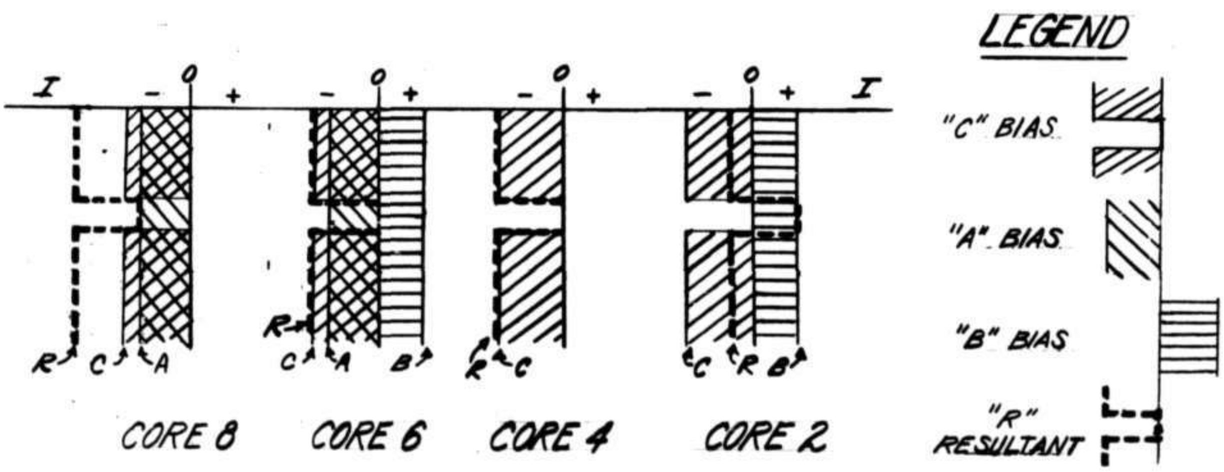


Figure 3

This indicates that core #2 is the only core in the matrix that is switched for this addition. The sum and carry outputs will be supplied by the sensing windings on this core.

If the subtraction (A-B) is to be performed, the B number to be operated on in the matrix must be the complement of the B number involved in the chosen subtractive operation. Therefore, if it is desired to subtract B = 0 from A = 1, the numbers to be placed in the matrix will be A = 1, B = 1 and the C_1 winding will be pulsed. Cores 1, 3, 5 and 7 will be affected just as cores 4, 2, 8 and 6 respectively were changed for the case of addition. Core #3 will be switched and will supply the appropriate sum and carry outputs.

The testing equipment arrangement is shown in Figure 2. The "B" binary number is selected by a manually operated two-position switch. The "A" binary number is selected by the output of the flip-flop which gets its input from the sum output winding of the matrix. This method of operation produces a circulating "A" number which will:

1. Repeat when:

a) B = 0, during addition	A = 0 B = 0 S = 0	A = 1 B = 0 S = 1	A and S are the same, therefore,
b) B = 1, during subtraction	A = 0 -B = 1 S = 0	A = 1 -B = 1 S = 1	A does not change after each operation

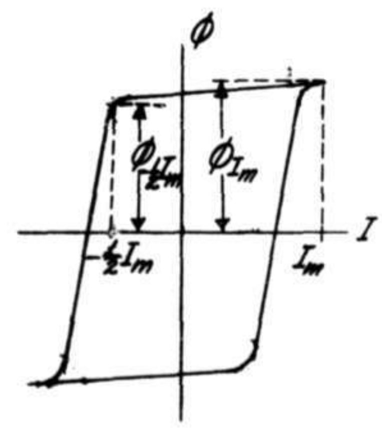
2. Alternate when:

a) B = 1, during addition	A = 0 B = 1 S = 1	A = 1 B = 1 S = 0	A and S differ - therefore A changes
b) B = 0, during subtraction	A = 0 -B = 0 S = 1	A = 1 -B = 0 S = 0	after each operation

This pattern of operation permits oscilloscope observation of high-speed addition or subtraction for any of four combinations of two binary numbers.

<u>Materials</u>

The cores used in the matrix switch are of Mo-Permalloy 216 (20 wraps of 1/4 mil tape, 1/8 in. wide on a 1/8 in. diameter bobbin). They have an average squareness ratio of 0.9. The squareness ratio is defined as the ratio of the flux at minus one-half the maximum current ($-1/2\ I_m$) required for saturation, to the flux at saturation (I_m). These cores are of the most rectangular type available in the lab at the present time.



The vacuum tubes that furnish bias current are 6Y6's. They operate with 150 volts on the plate and furnish about 200 ma. The bias ampere-turns for satisfactory operation are as follows:

A = (.200 amp) (20 turns) = 4.0 AT.

B = (.200 amp) (20 turns) = 4.0 AT.

C = (.185 amp) (30 turns) = 5.5 AT.

The cores are wound with AWG #36 Formex Magnet wire, enamel insulated.

Results

The matrix has been operated from a signal source which produces a 0.5 μsec pulse of 20 volts amplitude. It is to be expected that in order to couple two or more digits of the matrix switch adder it will be necessary that the output of the next lowest order digit be of the same magnitude as provided by the signal source. There is some distortion of the input waveshape through the matrix and therefore a pulse reshaper may be necessary between digits.

The optimum signal to noise ratio obtainable within a fairly narrow range of bias currents is 8 or greater.

The carry propagate time is approximately 0.07 μsec per digit.

The present maximum operating frequency of one digit of the adder with its associated equipment is approximately 1 mc. Operation at higher frequencies will necessitate an investigation of: (1) the effect of heating due to power dissipation in the core, and (2) the effect of the speed of operation of the associated flip-flop register which furnishes bias voltage to the "A" vacuum tubes, and hence controls the bias current.

A more significant evaluation of the operation of this device with respect to its usefulness as a component in an arithmetic element will be forthcoming upon completion of tests involving the integrated operation of two or three of these digits.

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