Variable VAR compensator circuits

C. Marouchos, M.K. Darwish and M. El-Habrouk

Abstract: A family of two reactive-power compensator circuit is presented. A general model of some basic linear elements and switching function blocks is developed first. Then the two proposed compensator circuits are derived from the generalised model. The proposed circuits are capable of supplying leading as well as lagging reactive currents in stepless variation without using an inverter configuration. The switching frequency is in the range of 2.5 kHz and the largest capacitor utilised does not exceed 60 μF. The generated reactive current, in either the leading or lagging modes, contains less than 2% total harmonic distortion.

1 Introduction

The need for smooth, harmonic-free reactive power compensators has been addressed by many publications and has attracted a great deal of interest [1, 2]. The main reason for such interest is the nature of recent loads and applications where a wide range of stepless reactive power supplies is required. The stepwise control and basic stepless control are provided by some of the conventional methods [3–6], such as some types of thyristor control reactors (TCR) and thyristor switched capacitors (TSC). These have the disadvantages of the large number of parallel capacitors required as well as the generation of current harmonics. Also conventional methods are slow to respond to sudden changes of reactive power [7, 8]. The control of the conventional techniques is based on phase control of thyristor circuits. The operating frequency in this case is the supply frequency (50/60 Hz) and the amount of harmonics generated is very large [7].

Modified systems using inverter configurations have been proposed in the past, as reviewed in [7–10]. These techniques overcome the basic stepless control of the TSC and TCR circuits but fall short in the fact that they require high switching frequencies (in excess of 15–20 kHz) and a large value of DC link capacitor (~4700 μF) [7]. The inverter configuration reactive compensator is normally used as a current-shaping circuit in order to inject/draw currents into/from the supply with predetermined waveforms [7–9]. This compensator current is computed from the undesired current components (usually combining active filtering and reactive power compensation applications) [7], in addition to the necessary charging/discharging current to compensate for the voltage fluctuations across the DC-link capacitor. This control method is generally called the 'constant capacitor voltage technique' [7–9]. Moreover, for single-phase applications, the inverter requires four power semiconductor switches of the same rating as the load.

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The work presented in this paper is an investigation of a new general model circuit, which can be used for stepless reactive-power compensation at a switching frequency in the range of 2.5 kHz without the presence of large values of DC-link capacitors. It requires only a maximum of 60 μF. The main idea behind the small capacitance used in switched-capacitor circuits is that the capacitor is not used to smooth the voltage across its terminals to its DC value as is the case for inverter configurations. Instead, it is used to smooth the voltage across its terminals to a fundamental 50 Hz voltage waveshape. The action of the switches in switched-capacitor circuits is to allow both the fundamental component of current as well as harmonics of the order of 2.5 kHz through the capacitors. The main role of the capacitor in this case is to attenuate only the high-frequency (2.5 kHz) harmonic voltages across its terminals but not the fundamental (50 Hz). In the case of inverter circuits [11], the action of the switches is to allow a strong low-frequency (100 Hz) current through the DC-link capacitor. The main role of the capacitor in this case is to attenuate any harmonic voltage ripple across its terminals down to the order of the 50 Hz fundamental frequency. Obviously, the capacitor (~4700 μF) required to smooth the inverter DC-link voltage to a pure DC value is much higher than the case of switched capacitor circuits where the capacitor (60 μF) is only smoothing much higher harmonics (2.5 kHz).

From the proposed general model two specific circuits are developed; class A and class B. The two circuits are capable of generating smoothly varied leading and lagging reactivepower with minimum total harmonic distortion (THD) (less than 2%).

The paper presents merely the concept of the switched capacitor circuits as applied to reactive power control. The demonstrated results concern only the capabilities of the circuit in the open loop. Further work for addressing the control problem is required and is outside the scope of the paper (using online/offline optimisation techniques as well as non-uniform and statistical PWM techniques).

2 General model for reactive-power compensator circuit

In this general model, a capacitor with a series semiconductor switch is the basic building block. As shown in Fig. 1*a*, a number of these basic building blocks are placed in parallel and connected to the mains via an inductor *L*. It is assumed that there are neither overlapping nor dead

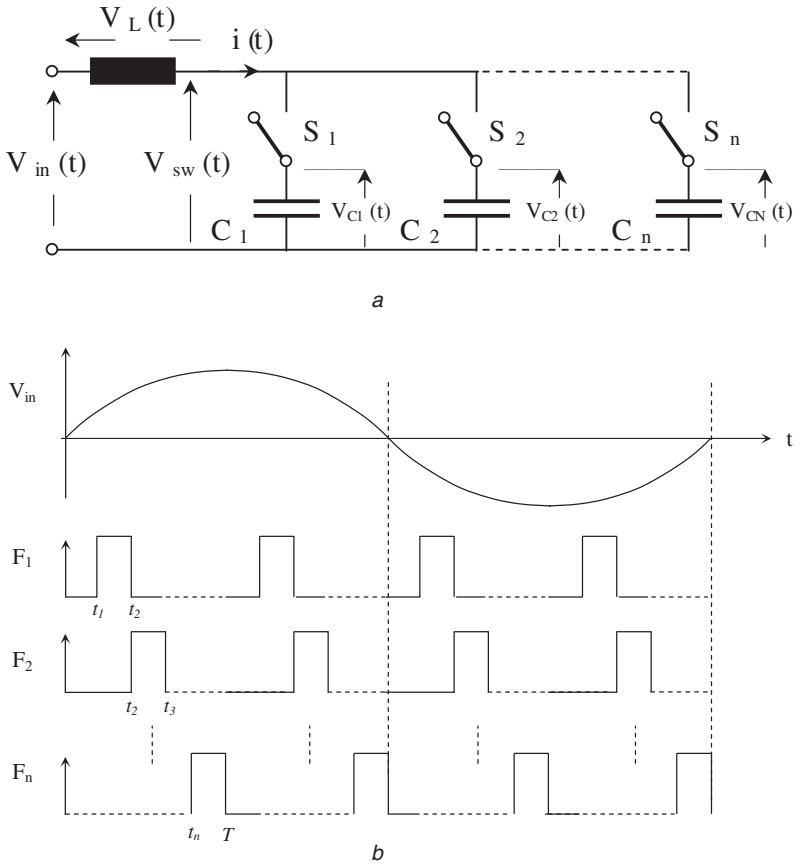

Fig. 1 *General model of proposed VAR circuit and its switching functions*
a Circuit diagram
b Switching functions

periods between the switching functions of the switches (i.e. only one switch may be active at any one instant of time) as shown in Fig. 1*b*, ensuring always a continuous and single path for the inductor current. Therefore the loop equation can be expressed as:

$$V_{in}(t) = V_L(t) + V_{sw}(t) \tag{1}$$

It is obvious that $V_{sw}(t)$ equals the voltage across the capacitor C_1, $V_{C1}(t)$, when S_1 is closed; i.e. the switching function for S_1 equals 1 ($F_1 = 1$), while $F_i = 0$ for $i = 2, 3, 4, \ldots N$, where N is the number of parallel branches. Similarly, $V_{sw}(t)$ equals $V_{C2}(t)$ when S_2 is closed, i.e. the switching function for S_2 equals 1 ($F_2 = 1$) etc…

In general:

$$V_{sw}(t) = F_1(t)\frac{1}{C_1}\int_{t_1}^{t_2} F_1(t)i(t)dt + F_2(t)\frac{1}{C_2}\int_{t_2}^{t_3} F_2(t)i(t)dt + \ldots + F_N(t)\frac{1}{C_N}\int_{t_N}^{t_{N+1}} F_N(t)i(t)dt \tag{2}$$

Note that the function F_i inside the integral is mandatory, as when a capacitor is not connected to the circuit (one terminal is opened with the switch), it will not accumulate any charge and hence its voltage will not change. This is guaranteed by the presence of F_i inside the integral. On the other hand, the presence of F_i outside the integral ensures that only one capacitor voltage is added to the sum (since only one switch is connected at any one instant of time).

Equations (1) and (2) are used to deduce a mathematical 'block diagram' model for the operation of the general circuit in Fig. 1*a*. This mathematical 'block diagram' is illustrated in Fig. 2, and is modelled in the following way:

- The line current $i(t)$ is diverted from one branch to another multiplied by $F_1(t)$, $F_2(t)$, …, $F_N(t)$ and converted to $i_{c1}(t)$, $i_{c2}(t)$, …, $i_{cN}(t)$. This operation is represented by modulators M_{11}, M_{21}, …, M_{N1}.
- Integrators G_{c1}, G_{c2}, …, G_{cN}, convert $i_{c1}(t)$, $i_{c2}(t)$, …, $i_{cN}(t)$ to $V_{c1}(t)$, $V_{c2}(t)$, …, $V_{cN}(t)$.
- Every voltage $V_{c1}(t)$, $V_{c2}(t)$, …, or V_{cN} (t) is multiplied by the appropriate $F_1(t)$, $F_2(t)$, …, or $F_N(t)$ to develop $V_{sw}(t)$. This is carried out through one of the modulator M_{12}, M_{22}, …, or M_{N2} and then through the adder 'A_1'.
- The voltage across the inductor $V_L(t)$ is then evaluated by subtracting $V_{sw}(t)$ from $V_{in}(t)$, through the adder 'A_2'.
- Finally, the integrator G_L converts $V_L(t)$ back to $i(t)$ and the whole sequence is repeated.

A unified expression for $V_{sw}(t)$ in (2) can be given as:

$$V_{sw}(t) = \sum_{r=1}^{N} \frac{F_r(t)}{C_r}\int_0^{t_{r+1}} i(t)F_r(t)dt \tag{3}$$

The switching function F_r (t) in (3) is a pulse function and can be expressed by the sum of sinusoids, according to the Fourier series, as [11]:

$$F_r(t) = K_{0r} + \Phi_r(t) \tag{4}$$

where K_{0r} = duty cycle of the switch 'r'; $K_{nr} = \sin n\delta_r / n\pi$; $\Phi_r(t) = 2\sum_{n=1}^{\infty} K_{nr}\cos(n\omega_s t - n\theta)$; $\delta_r =$ half the 'on' period of the switch; ω_s = switching angular frequency, $2\pi f_s$; and θ = the phase angle of the switching function with respect to $V_{in}(t)$.

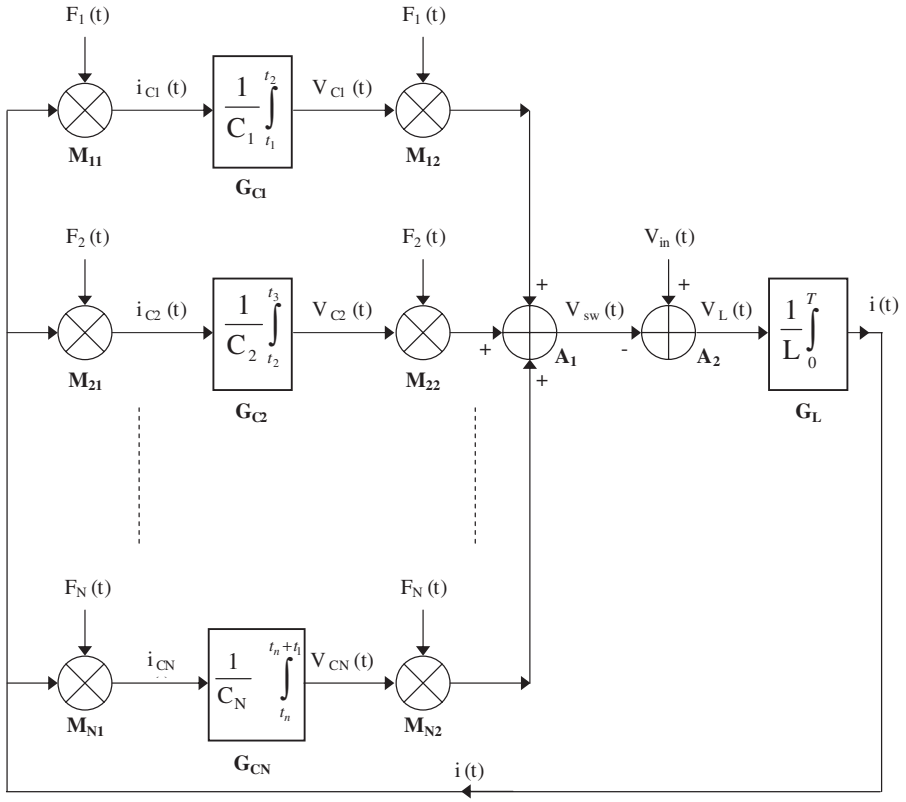

Fig. 2 *Mathematical model of circuit in Fig. 1*

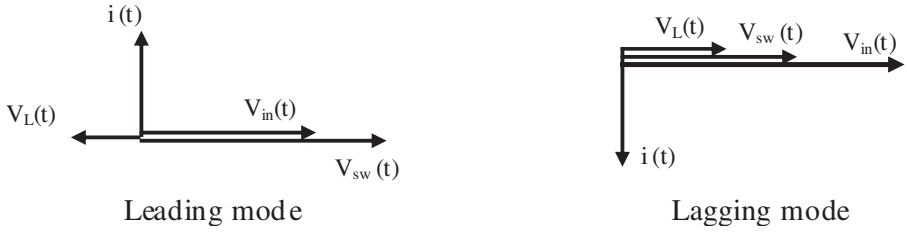

Fig. 3 *Ideal phasor relationships between $V_{in}(t)$, $V_L(t)$, $V_{sw}(t)$, and $i(t)$ in general model of proposed VAR circuit*

The switching functions $F_1(t)$, $F_2(t)$, …, $F_N(t)$ have no overlap or dead periods (as mentioned earlier), therefore

$$\sum_{r=1}^{N} F_r(t) = 1 \tag{5}$$

For reactive power generation the switched part of the circuit must develop a voltage $V_{sw}(t)$ at the power frequency with a larger magnitude than $V_{in}(t)$ for a leading inductor current or a smaller magnitude than $V_{in}(t)$ for a lagging inductor current, as shown in Fig. 3, depending on the switching pattern and the values of the capacitors. The two extreme cases are shown in Fig. 3 for lossless systems.

The switching function $F_r(t)$ should be chosen so that $V_{sw}(t)$ (the voltage across the switched part of the circuit) has very few or no harmonics. This can be achieved if $F_r(t)$ occurs at high frequency [11]. For a switching frequency 'm' times the fundamental frequency (50 Hz or 60 Hz), the lowest harmonics in the line current (above the fundamental) are of order '$m \pm 1$'. The current in each capacitor will contain in this case the same order harmonics after the first modulation (M_{11}, M_{21}, …, or M_{N1} in Fig. 2). These current harmonics will produce voltage harmonics across each capacitor. These voltage harmonics are heavily attenuated if the switching frequency is much higher than the fundamental frequency, i.e. '$m \gg 1$'. During the second modulation process (M_{12}, M_{22}, …, or M_{N2} in Fig. 2), the voltage across each capacitor is modulated by the corresponding switching function in order to produce $V_{sw}(t)$.

For reactive power generation the line current, $i(t)$, must be a pure sinusoid. Any presence of current harmonics adds to the degradation of the quality of the produced reactive power. In general the line current can be expressed as:

$$i(t) = I_1 \cos \omega t + \sum_{n=1}^{\infty} I_{nm\pm1}(\cos(nm \pm 1)\omega t - \theta_{nm\pm1}) \tag{6}$$

where $\omega =$ mains angular frequency, $2\pi f$.

The ripple part (or harmonic currents) in the above equation is:

$$i_{\text{ripple}}(t) = \sum_{n=1}^{\infty} I_{nm\pm1}(\cos(nm \pm 1)\omega t - \theta_{nm\pm1})$$

The phase delay of the line ripple current is set by both the phase delay θ of the switching function and the presence of losses in the circuit. The losses are very small in these circuits, as will be shown in the experimental results, and they are neglected in the analysis. The phase delay of the switching function is set to zero; it has no effect on the performance of the compensator as far as reactive power is concerned. Furthermore, the best control is achieved by setting the phase angle of the switching functions to zero,

$\theta = 0^\circ$ [11]. For the purpose of this analysis and for all practical purposes the ripple current is limited to the first two harmonics; they are cosine terms with no phase delay. By setting $\theta_{mn\pm1}$ to zero, the ripple current becomes:

$$i_{\text{ripple}}(t) = I_{m-1}\cos(m-1)\omega t + I_{m+1}\cos(m+1)\omega t \quad (7)$$

Substituting $F_r(t)$ (4), and $i(t)$ (6) into $V_{sw}(t)$ (3) and expanding:

$$V_{sw}(t) = \sum_{r=1}^{N}\left\{[K_{0r}+\Phi_r(t)]\frac{1}{C_r}\int_0^{\infty}[K_{0r}I_1\cos\omega t + \Phi_r(t)I_1\cos\omega t + \Phi_r(t)i_{\text{ripple}}(t) + K_{0r}i_{\text{ripple}}(t)]dt\right\} \quad (8)$$

The voltage across the rth capacitor in (8) is given by the result of the integral. It is observed that the first term, $K_{0r}I_1\cos\omega t$, is a fundamental component and the third term, $\Phi_r(t)i_{\text{ripple}}(t)$, contributes to the fundamental by a component $I_{1H}(t)$; the rest constitute high-frequency ripple components of the order $2mn\pm1$. These high-frequency terms will be attenuated by a harmonic impedance $(2mn\pm1)\omega C_r$; the harmonic impedance of each capacitor and for practical purposes can be neglected by virtue of the high switching frequency (ω_s) and the large value of the capacitance (C_r). Hence the capacitor voltage is approximated to the fundamental component and the rest of the voltage harmonics are neglected:

$$V_{sw}(t) = \sum_{r=1}^{N}\left\{[K_{0r}+\Phi_r(t)]\frac{1}{C_r}\int_0^{\infty}[K_{0r}I_1\cos\omega t + I_{1H}(t)]dt\right\} \quad (9)$$

The fundamental component of the switching function $\Phi_r(t)$ is the only component which contributes to the fundamental current and it can be expressed as:

$$\Phi_1(t) = 2K_{1r}\cos(m\omega t)$$

$I_{1H}(t)$ in (9) is the contribution of the harmonic line current to the capacitor fundamental current. It can be expressed from the 3rd term of (8) as:

$$I_{1H}(t) = [2K_{1r}\cos(m\omega t)]I_{m-1}\cos(m-1)\omega t + [2K_{1r}\cos(m\omega t)]I_{m+1}\cos(m+1)\omega t$$

By applying simple trigonometry and selecting the fundamental components only:

$$I_{1H}(t) = K_{1r}I_{m-1}\cos(\omega t) + K_{1r}I_{m+1}\cos(\omega t) \quad (10)$$

Replacing $I_{1H}(t)$ from (10) in (9) and integrating

$$V_{sw}(t) = \sum_{r=1}^{N}\left\{[K_{0r}+\Phi_r(t)]\left[\frac{1}{\omega C_r}K_{0r}I_1\sin\omega t + \frac{1}{\omega C_r}K_{1r}I_{m-1}\sin\omega t + \frac{1}{\omega C_r}K_{1r}I_{m+1}\sin\omega t\right]\right\} \quad (11)$$

The voltage across the rth capacitor is given by the integral of (9), and by considering $I_{1H}(t)$ in (10), $V_{Cr}(t)$ can be expressed as:

$$V_{Cr}(t) = X_{Cr}K_{0r}I_1\sin\omega t + X_{Cr}K_{1r}I_{m-1}\sin\omega t + X_{Cr}K_{1r}I_{m+1}\sin\omega t \quad (12)$$

where $1/\omega C_r$ is replaced by X_{Cr}.

The peak voltage across the rth capacitor in (12) is given by

$$V_{C\text{peak}} = X_{Cr}K_{0r}I_1 + X_{Cr}K_{1r}I_{m-1} + X_{Cr}K_{1r}I_{m+1} \quad (13)$$

Since the line current was limited to the fundamental and the first two harmonics, the voltage across the switched network, $V_{sw}(t)$, must contain only the fundamental and the first set of the two harmonics, $m\pm1$. Hence in expanding (11), only these components must be retained. The only component of $\Phi_r(t)$ that contributes to the two harmonics is K_{1r}. Hence $\Phi_r(t)$ is reduced to:

$$\Phi_1(t) = 2K_{1r}\cos(m\omega t)$$

Expanding (11), collecting terms, simplifying and replacing $1/\omega C_r$ by X_{Cr}

$$V_{sw}(t) = \sum_{r=1}^{N}\left\{\begin{array}{l} X_{Cr}[K_{0r}^2I_1 + K_{0r}K_{1r}I_{m-1} + K_{0r}K_{1r}I_{m+1}] \\ \times\sin\omega t + X_{Cr}[K_{0r}K_{1r}I_1 + K_{1r}^2I_{m-1} \\ + K_{1r}^2I_{m+1}]\sin((m\pm1)\omega t)\end{array}\right\} \quad (14)$$

The voltage across the inductor $V_L(t)$

$$V_L(t) = L\frac{dI(t)}{dt}$$

By considering only the first two line current harmonics in (7), $V_L(t)$ becomes:

$$V_L(t) = -I_1X_L\sin(\omega t) - (m-1)X_LI_{m-1}\times\sin((m-1)\omega t) - (m+1)X_LI_{m+1}\times\cos((m+1)\omega t) \quad (15)$$

3 Class A compensator

The Class A compensator consists of two branches and, in implementing this circuit, each bidirectional switch is realised by two unidirectional switches that are independently controlled to avoid the problems associated with the switching delays of semiconductor devices (dead times and overlaps). Therefore S_1 is implemented using IGBTs 'T_A' and 'T_B' while S_2 is implemented using IGBTs 'T_C' and 'T_D', as shown in Fig. 4*a*. The current in the Class A compensator is controlled independently in each direction so that IGBTs T_A and T_C conduct the current during the positive half-cycle and IGBTs T_B and T_D conduct the current during the negative half-cycle. By introducing overlaps in the driving signals of the IGBTs a secure continuous path of the inductor current is provided and short circuiting of the inductor is avoided, as illustrated Fig. 4*b*. The two switches (S_1 and S_2) are operating in anti-parallel, i.e.

$$F_1(t) = 1 - F_2(t) \quad (16)$$

Equation (16) implies that:

$$K_{02} = 1 - K_{01} \quad \text{and} \quad K_{12} = -K_{11}$$

By setting $N=2$ (two branches) in (14), $V_{sw}(t)$ can be expressed as:

$$\begin{aligned} V_{sw}(t) = {} & X_{c1}[K_{01}^2I_1 + K_{01}K_{11}I_{m-1} + K_{01}K_{11}I_{m+1}]\sin(\omega t) \\ & + X_{c1}[K_{11}K_{01}I_1 + K_{11}^2I_{m-1} + K_{11}^2I_{m+1}]\sin((m\pm1)\omega t) \\ & + X_{c2}[K_{02}^2I_1 + K_{02}K_{12}I_{m-1} + K_{02}K_{12}I_{m+1}]\sin(\omega t) \\ & + X_{c2}[K_{12}K_{02}I_1 + K_{12}^2I_{m-1} + K_{12}^2I_{m+1}]\sin((m\pm1)\omega t) \end{aligned}$$

Collecting terms,

$$\begin{aligned} V_{sw}(t) = {} & \{X_{c1}[K_{01}^2I_1 + K_{01}K_{11}I_{m-1} + K_{01}K_{11}I_{m+1}] \\ & + X_{c2}[K_{02}^2I_1 + K_{02}K_{12}I_{m-1} + K_{02}K_{12}I_{m+1}]\}\sin\omega t \\ & + \{X_{c1}[K_{11}K_{01}I_1 + K_{11}^2I_{m-1} + K_{11}^2I_{m+1}] \\ & + X_{c2}[K_{12}K_{02}I_1 + K_{12}^2I_{m-1} + K_{12}^2I_{m+1}]\}\sin(m\pm1)\omega t \end{aligned} \quad (17)$$

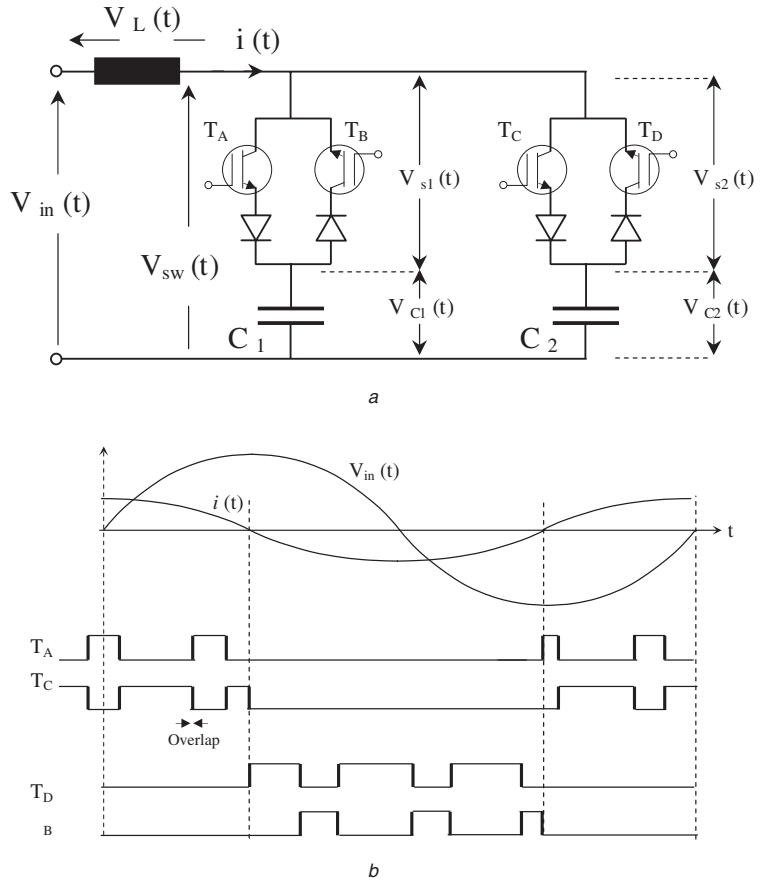

Fig. 4
a Class A compensator
b Driving signals for Class A compensator

Equation (1) can now be written for the Class A compensator in matrix form using (15) and (17).

$$\begin{pmatrix} V_P \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} X_{C1}K_{01}^2 + X_{C2}K_{02}^2 - X_L & X_{C1}K_{01}K_{11} + X_{C2}K_{02}K_{12} \\ X_{C1}K_{11}K_{01} + X_{C2}K_{12}K_{02} & X_{C1}K_{11}^2 + X_{C2}K_{12}^2 - (m-1)X_L \\ X_{C1}K_{11}K_{01} + X_{C2}K_{12}K_{02} & X_{C1}K_{11}^2 + X_{C2}K_{12}^2 \end{pmatrix} \begin{pmatrix} X_{C1}K_{01}K_{11} + X_{C2}K_{02}K_{12} \\ X_{C1}K_{11}^2 + X_{C2}K_{12}^2 \\ X_{C1}K_{11}^2 + X_{C2}K_{12}^2 - (m+1)X_L \end{pmatrix} \begin{pmatrix} I_1 \\ I_{m-1} \\ I_{m+1} \end{pmatrix} \quad (18)$$

Equation (18) can be simplified by introducing the following terms:

$$G = \frac{X_{C1}}{X_L}, \quad H = \frac{X_{C2}}{X_{C1}}, \quad P_{m-1} = \frac{I_{m-1}}{I_1}, \quad P_{m+1} = \frac{I_{m+1}}{I_1}$$

$$\begin{pmatrix} X_1/X_L \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} GK_{01}^2 + HGK_{02}^2 - 1 & GK_{01}K_{11} + GHK_{02}K_{12} \\ GK_{11}K_{01} + HGK_{12}K_{02} & GK_{11}^2 + GHK_{12}^2 - (m-1) \\ GK_{11}K_{01} + GHK_{12}K_{02} & GK_{11}^2 + GHK_{12}^2 \end{pmatrix} \begin{pmatrix} GK_{01}K_{11} + GHK_{02}K_{12} \\ GK_{11}^2 + GHK_{12}^2 \\ GK_{11}^2 + GHK_{12}^2 - (m+1) \end{pmatrix} \begin{pmatrix} 1 \\ P_{m-1} \\ P_{m+1} \end{pmatrix} \quad (19)$$

Equation (19) is solved by Cramer's rule [12] to give the per-unit impedance X_1/X_L (Fig. 5), and the level of current harmonics P_{m-1} and P_{m+1} (Fig. 6*a*) of the Class A compensator. The wide smooth variations of the capacitive impedance (hence the reactive power) of Class A compensators can be seen from Fig. 5. Figure 6*a* shows that the percentage of the maximum harmonics ($P_{m\pm1}$) will occur at 0.25 and 0.75 duty cycles with values not more than 1.4% of the fundamental component. By considering the two dominant line harmonics ($I_{m\pm1}$), the total harmonic distortion is $<2\%$.

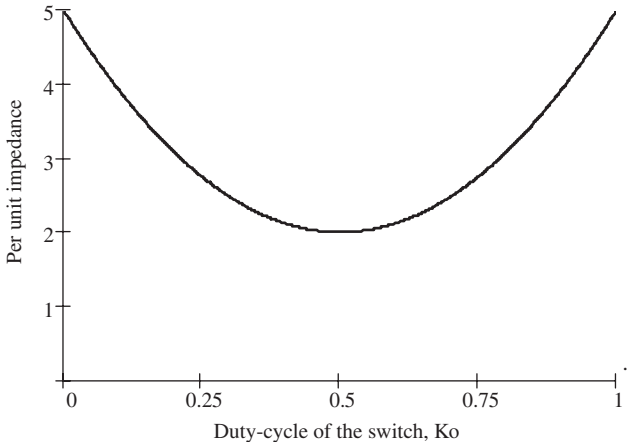

Fig. 5 *Per-unit impedance of Class A compensator*

The choice of capacitor and inductor values obviously influences the range of the generated reactive power. A good range of reactive power can be generated when X_{C1} is six times X_L. The harmonics generated from such range is less than 1.4% of the fundamental, as shown in Fig. 6*b*.

The overvoltage ratio (OVR) can be defined as the ratio of the peak voltage across the switch to the peak value of the mains voltage:

$$\text{OVR} = V_{s1\,(\text{peak})}/V_P \quad (20)$$

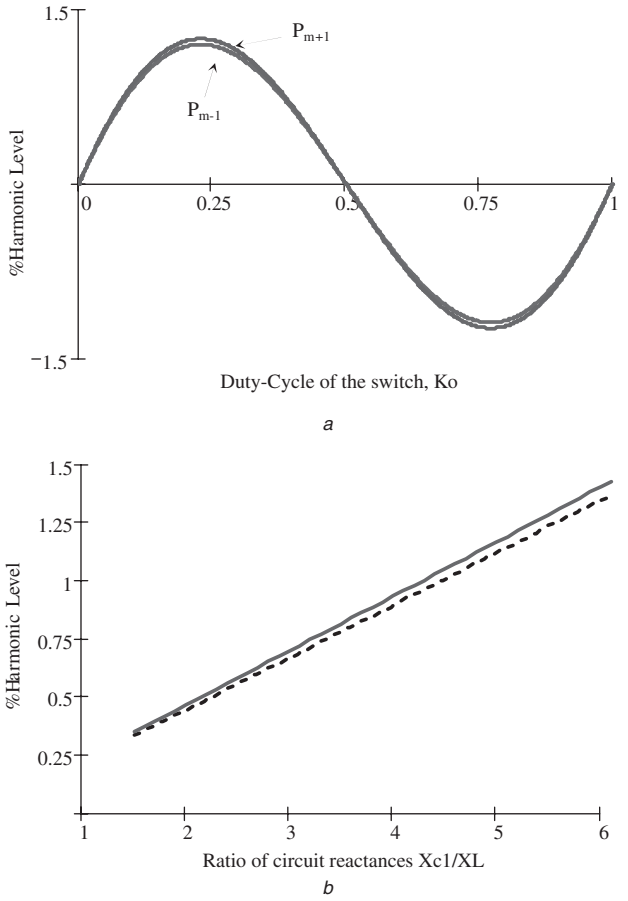

Fig. 6 *Harmonic level of Class A compensator*
a Harmonic level against K_0
b Harmonic level against X_{C1}/X_L

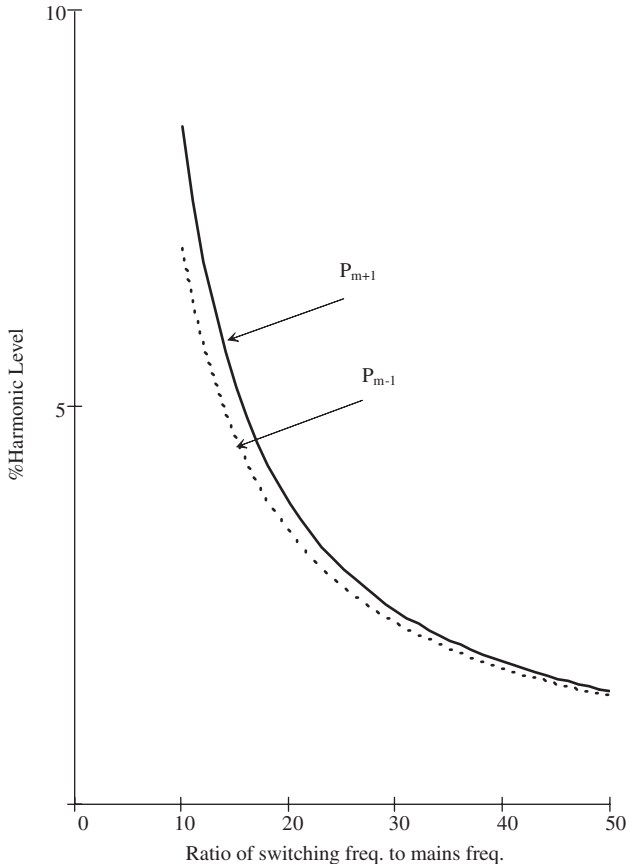

Fig. 7 *Harmonic level of Class A compensator against m*

where $V_{s1(\text{peak})}$ is the peak voltage across the switch S_1 and V_P is the peak mains voltage. For Class A compensators the voltage across any one of the two switches is the difference between the two capacitor voltages, $V_{C1}(t) - V_{C2}(t)$. It follows from (13) that the peak voltage across any of the two switches can be expressed as:

$$V_{s1(\text{peak})} = X_{C1}[K_{01}I_1 + K_{11}I_{m-1} + K_{11}I_{m+1}] - X_{C2}[K_{02}I_1 + K_{12}I_{m-1} + K_{12}I_{m+1}]$$

Substituting X_{C2} by $HX_{C1}(H = X_{C2}/X_{C1})$ in the above expression and dividing both sides by I_1, yields:

$$\frac{V_{s1(\text{peak})}}{I_1} = X_{C1}[K_{01} + K_{11}P_{m-1} + K_{11}P_{m+1}] - HX_{C1}[K_{02} + K_{12}P_{m-1} + K_{12}P_{m+1}]$$

Replacing I_1 with (V_P/X_1):

$$\text{OVR} = \frac{X_{C1}}{X_1}\{[K_{01} + K_{11}P_{m-1} + K_{11}P_{m+1}] - H[K_{02} + K_{12}P_{m-1} + K_{12}P_{m+1}]\} \quad (21)$$

From the matrix in (19), the terms P_{m+1} and P_{m-1} are calculated using Cramer's rule [12]. These terms are used in (21) to calculate the OVR. Table 1 shows that the OVR of the semiconductor switches can be only as high as 1.3 times the supply voltage; i.e. for 240 V RMS the voltage rating of the switch is about 440 V. Such voltage rating is not high and is very common in all different types of semiconductor switches. The operating frequency of the switches should be around 2.5 kHz (50 times the supply frequency). Below this frequency the harmonic levels will be increased, as shown in Fig. 7, and beyond this frequency, higher switching losses will be introduced.

Table 1: Ratio of voltage across switch to mains voltage (OVR) in Class A compensator

Duty cycle	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
OVR		−1.2	−1.3	−1.2	−1.0	−0.7	0.0	0.7	1.0	1.2	1.3	1.2

4 Class B compensator

In some applications a lagging reactive compensation is also required. As will be shown in this Section, a Class B compensator (Fig. 8) is capable of providing both leading and lagging reactive powers (at different values of duty cycle). The circuit consists of two branches, one with a switch and a capacitor and the other with just a switch. The whole circuit is connected to the mains via an inductor. The two bidirectional switches operate in anti-parallel (each bidirectional switch is replaced by two unidirectional switches, which are independently controlled in a similar

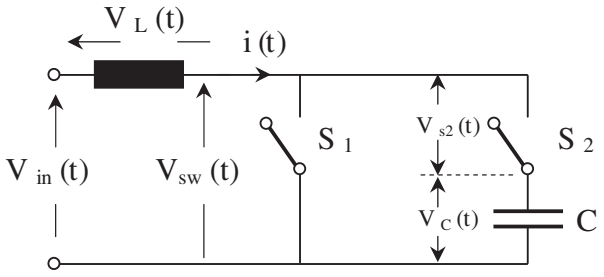

Fig. 8 *Class B compensator*

fashion as in the Class A compensator), i.e.

$$F_1(t) = 1 - F_2(t)$$

which implies that

$$K_{02} = 1 - K_{01} \quad \text{and} \quad K_{12} = -K_{11}$$

Since only one branch contains a capacitor, (14) in the general model can be altered to:

$$V_{sw}(t) = X_c[K_{02}^2 I_1 + K_{02}K_{12}I_{m-1} + K_{02}K_{12}I_{m+1}]\sin(\omega t) + X_c[K_{12}K_{02}I_1 + K_{12}^2 I_{m-1} + K_{12}^2 I_{m+1}]\sin((m \pm 1)\omega t) \quad (22)$$

Equation (1) can now be written for the Class B compensator in a matrix form using (15) and (22):

$$\begin{pmatrix} V_P \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} X_C K_{02}^2 - X_L & X_C K_{02}K_{12} & X_C K_{02}K_{12} \\ X_C K_{12}K_{02} & X_C K_{12}^2 - (m-1)X_L & X_C K_{12}^2 \\ X_C K_{12}K_{02} & X_C K_{12}^2 & X_C K_{12}^2 - (m+1)X_L \end{pmatrix} \begin{pmatrix} I \\ I_{m-1} \\ I_{m+1} \end{pmatrix} \quad (23)$$

The term G can be redefined so that: $G = X_C/X_L$. P_{m+1} and P_{m-1} are the same as in Class A compensators. Equation (23) can now be simplified to:

$$\begin{pmatrix} X_1/X_L \\ 0 \\ 0 \end{pmatrix} = \begin{pmatrix} GK_{02}^2 - 1 & GK_{02}K_{12} & GK_{02}K_{12} \\ GK_{12}K_{02} & GK_{12}^2 - (m-1) & GK_{12}^2 \\ GK_{12}K_{02} & GK_{12}^2 & GK_{12}^2 - (m+1) \end{pmatrix} \begin{pmatrix} 1 \\ P_{m-1} \\ P_{m+1} \end{pmatrix} \quad (24)$$

Equation (24) is solved by Cramer's rule [12] to give the per-unit impedance X_1/X_L (Fig. 9). From Fig. 9, it can be seen that the circuit is capable of producing a leading reactive power (0–0.3 duty cycle) and a lagging reactive power (0.3–1 duty cycle). Figure 10*a* shows that the percentage of the maximum harmonic level ($P_{m\pm1}$) is 0.75% occurring at 0.35 duty cycle. By considering the two dominant line harmonics ($I_{m\pm1}$), the total harmonic distortion is $<1\%$.

Again in Class B compensators, the choice of the capacitance and inductance obviously influences the range of the generated reactive power. A good range of leading and lagging reactive power can be generated when X_C is twice X_L. The harmonics generated from such a range are less than 0.75% of the fundamental, as shown in Fig. 10*b*.

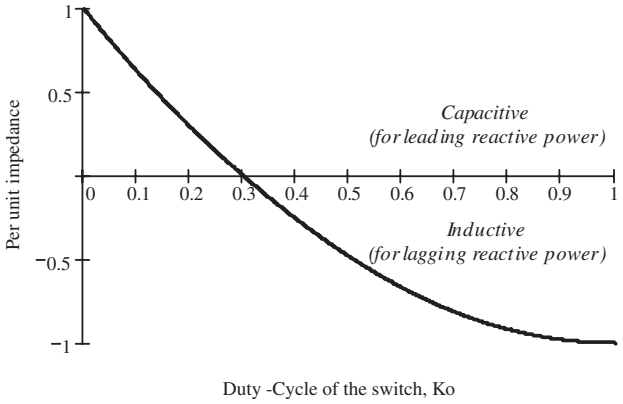

Fig. 9 *Per-unit impedance of Class B Compensator*

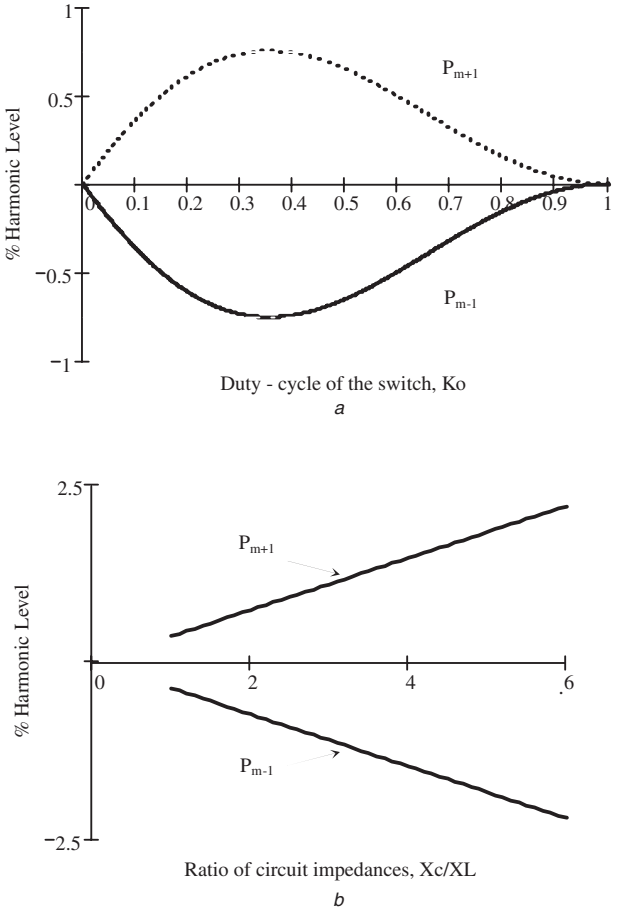

Fig. 10 *Harmonic level of Class B compensator*
a Harmonic level against K_0
b Harmonic level against X_C/X_L

For Class B compensators, the voltage across any one of the two switches (in the off state) is the capacitor voltage $V_C(t)$. It follows from (13) that the peak voltage across any of the two switches can be expressed as:

$$V_{s1(\text{peak})} = X_C[K_{01}I_1 + K_{11}I_{m-1} + K_{12}I_{m+1}]$$

Dividing both sides by I_1:

$$\frac{V_{s1(\text{peak})}}{I_1} = X_{C1}[K_{01} + K_{11}P_{m-1} + K_{11}P_{m+1}] - HX_{C1}[K_{02} + K_{12}P_{m-1} + K_{12}P_{m+1}]$$

Replacing I_1 with (V_P/X_1):

$$\text{OVR} = \frac{X_C}{X_1}[K_{01} + K_{11}P_{m-1} + K_{12}P_{m+1}] \quad (25)$$

The terms P_{m+1} and P_{m-1} from the matrix in (24) are calculated using Cramer's rule [12]. These terms are used in (25) to calculate the OVR. Table 2 shows that the OVR of the semiconductor switches can be limited to four times the supply voltage (assuming that the operation of this circuit is occurring at ≤ 0.26 or ≥ 0.37 duty cycles). It is obvious that the circuit will approach the resonance phenomenon

Table 2: Ratio of voltage across switch to mains voltage (OVR) in Class B compensator

Duty cycle	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
OVR	0	0.3	1.3	∞	3.3	2.1	1.9	1.8	1.8	1.9	2.1

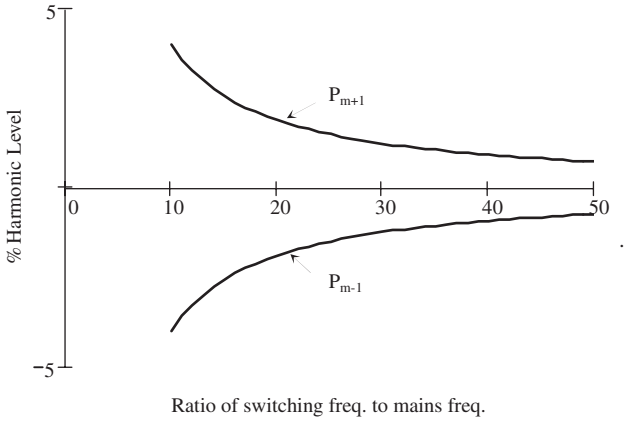

Fig. 11 *Harmonic level of Class B compensator against m*

between 0.26 and 0.37 duty cycles and such a range of duty cycle should be avoided.

The operating frequency of the switches in Class B compensators is similar to that in Class A (2.5 kHz). Again, below this frequency the harmonics levels will increase, as shown in Fig. 11, and beyond this frequency higher switching losses will be introduced.

5 Experimental results

The two circuits for Class A and Class B compensators were designed with the following values:

Class A: $L = 85.3\,\text{mH}$; $C_1 = C_2 = 19.8\,\mu\text{F}$; switching frequency = 2.5 kHz

Class B: $L = 85.3\,\text{mH}$; $C = 59.4\,\mu\text{F}$; switching frequency = 2.5 kHz.

Figure 12*a* shows the experimental results for the Class A compensator. The switching frequency was deliberately selected at 400 Hz so that the P_{m-1} and P_{m+1} harmonics (7th and 9th) can be clearly illustrated. Figure 12*b* shows similar results for the Class B compensator at 90% duty cycle so that the compensator current is inductive (see Fig. 9).

The effect of smoothing the capacitor voltage waveform is clear in the supply current waveforms with the reduced amount of harmonic content, as shown in the waveforms of Fig. 12*b*. Almost 90° phase shift is achieved for both leading and lagging power factors.

With respect to the transient response, the circuit is operating on a minimum switching frequency of 2.5 kHz. Hence the control command addressed to the circuit would be changed according to the control requirements (not discussed in this paper) within 400 µs. This is well within the required response times for power system components.

6 Conclusions

Two reactive power compensator circuits are introduced in this paper. A Class A compensator is capable of generating wide range of leading reactive power with very low total harmonic distortion (< 1.25%). A Class B compensator is capable of generating leading as well as lagging reactive powers and also with very low total harmonic distortion. The switching function technique is used in analysing the two compensator circuits. The main advantage of applying this technique is that the voltage across the semiconductor switches can easily be derived. This is important particularly in Class B compensators where care has to be taken in choosing the operating duty cycle in order to avoid the resonance phenomenon (Table 2). An experimental

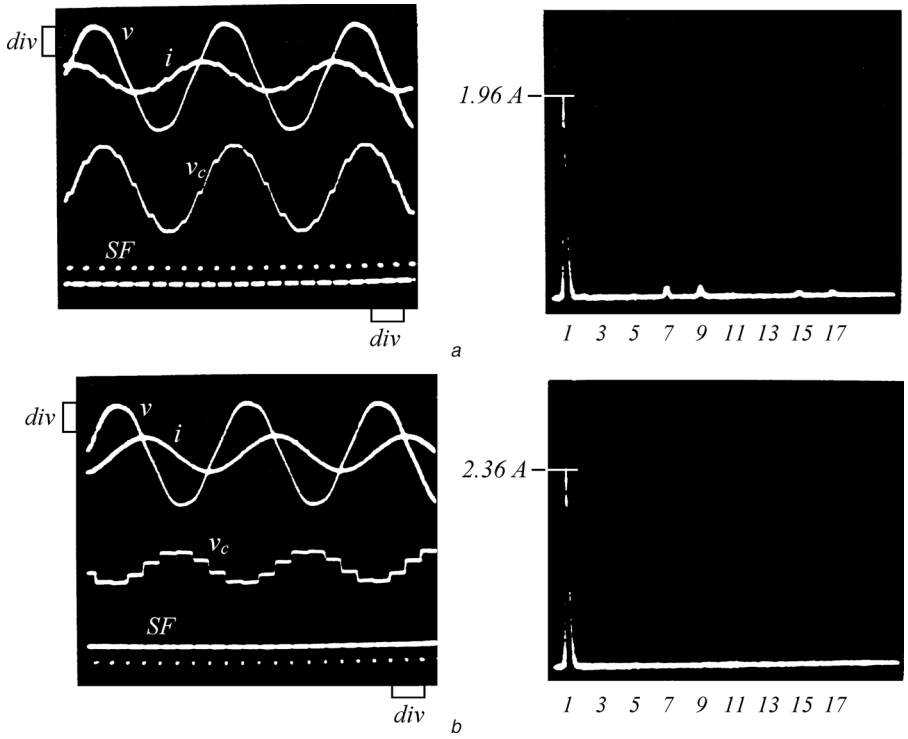

Fig. 12 *Experimental results for Class A and Class B Compensators*
a Class A compensator experimental results: supply voltage, reactive current, capacitor voltage (V_{C1}), switching function (S_1) and harmonic spectrum for reactive current (200 V/div., 4 A/div., 5 ms/div.)
b Class B compensator experimental results: supply voltage, reactive current (in inductive mode), capacitor voltage, switching function (S_1) and harmonic spectrum for the reactive current (200 V/div., 4 A/div., 5 ms/div.)

prototype was constructed for the two compensators. Close agreement between experimental and simulation results demonstrates that a variable leading and lagging reactive power can be generated with minimum total harmonic distortion.

The proposed circuits control reactive power in a stepless manner. They avoid the main problems with inverter-type circuits (DC-link capacitor, high switching frequency and number of active switches). The THD resulting from the operation of the circuit at its full range is well below 2%, which is power quality friendly.

The typical application for such circuits would be for large commercial office buildings (with air conditioning) and on factory interfaces where the reactive power change is not very fast. This is very important since the main characteristic of the circuit is the lower number of switches (as compared to inverter configurations, normally termed as stepless var compensators), which would be more economical for larger power applications. This way the circuit would not only be suitable for distributed small loads but also for larger combinations of load. These aspects render the proposed circuit much more economical than other configurations for such applications.

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