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Numerical and experimental validation with bifurcation diagrams for a controlled DC–DC converter with quasi-sliding control

Validación numérica y experimental mediante diagramas de bifurcaciones, para un convertidor DC–DC controlado con control cuasi-deslizante

Fredy E. Hoyos[1], John E. Candelo-Becerra[2], y Nicolás Toro[3]

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[1] Electrical Engineer, PhD in Engineering-Automation, Facultad de Ciencias, Escuela de Física, Grupo de Investigación en Tecnologías Aplicadas-GITA, Universidad Nacional de Colombia, Medellín-Colombia, fehoyosve@unal.edu.co

[2] Electrical Engineer, PhD in Engineering-Electrical Engineering, Department of Electrical Energy and Automation, Grupo de Investigación en Tecnologías Aplicadas – GITA, Universidad Nacional de Colombia, Medellín-Colombia, jecandelob@unal.edu.co

[3] Electrical Engineer, PhD. in Engineering-Automation, Department of Electrical, Electronic and Computer Engineering, Universidad Nacional de Colombia, Manizales-Colombia, ntoroga@unal.edu.co

Abstract

This paper presents a stability analysis of a buck converter using a Zero Average Dynamics (ZAD) controller and Fixed-Point Induction Control (FPIC) when the control parameter N, the reference voltage v_{ref}, and the source voltage E are changed. The study was based on a previous analysis in which the control parameter was adjusted to $N = 1$ and the parameter K_s was changed during the simulation, finding the stability zone and regions with chaotic behavior. Thus, this new study presents the transient and steady-state behaviors and robustness of the buck converter when the control parameter N changes. Moreover, numerical simulation results are compared with experimental observations. The results show that the system regulates the output voltage with low error when the voltage is changed in the source E. Besides, the voltage overshoot increases, and the settling time decreases when the control parameter N is augmented and the control parameter K_s is constant. Furthermore, the buck converter controlled by ZAD and FPIC techniques is effective in regulating the output voltage of the circuit even when there are two delay periods and voltage input disturbances.

Keywords

DC–DC buck converter, bifurcations in FPIC control parameter, sliding control, two-dimensional bifurcation, microgrid, electrical network.

Resumen

Este artículo presenta un análisis de estabilidad del convertidor buck usando la técnica de control de promediado cero (ZAD) y el control por inducción de punto fijo (FPIC), cuando se cambian el parámetro de control N, el voltaje de referencia v_{ref}, y el valor de la tensión de la fuente de alimentación E. El estudio se basó en un análisis previo en el cual se ajustó el parámetro de control en $N = 1$ y el parámetro K_s fue cambiado durante la simulación, encontrando la zona de estabilidad y regiones con comportamiento caótico. Así, este nuevo estudio determina los comportamientos transitorios y de estado estacionario y la robustez del convertidor buck cuando el parámetro de control N varía, comparando los resultados de la simulación y pruebas experimentales. Los resultados muestran que el sistema regula la tensión de salida con un error bajo cuando se cambia la tensión en la fuente E. Además, el sobre impulso del voltaje aumenta y el tiempo de estabilización disminuye cuando el parámetro de control N es aumentado y el parámetro de control K_s es constante. También, el convertidor buck controlado por las técnicas ZAD y FPIC es eficaz en la regulación de voltaje de salida del circuito, incluso cuando hay dos períodos de atraso.

Palabras clave

Convertidor reductor DC–DC, bifurcaciones en parámetro de control FPIC, control por modos deslizantes, bifurcaciones de codimensión dos, micro red, red eléctrica.

1. INTRODUCTION

Power converters are used in microgrids to transfer electrical energy from direct to direct current (DC–DC) or from alternating to direct current (AC–DC), as shown in Fig. 1. A buck converter (step-down converter) is a DC–DC power converter that can be modeled as a piecewise linear system with three topologies [1]. A complete introduction to power converters can be found in [2]. However, as different types of loads are normally connected to these converters [3], some significant voltage variations are presented in the network [4]. Two recent techniques applied to the network are the Zero Average Dynamics (ZAD) and Fixed-Point Induction Control (FPIC), which have shown good results for controlling the output voltage [5]–[7].

Therefore, the response of digitally controlled DC–DC converters was studied in [8] by considering non-uniform quantization. Besides, in [5], the steady-state limit cycles in DPWM-controlled converters were evaluated and, to avoid oscillations, some conditions were imposed on the control law and the quantization resolution. The FPIC control technique allows the stabilization of unstable orbits as presented in [9]. Furthermore, the parameter estimation techniques allow to calculate unknown varying parameters of converters [10], [11]. In [12], the minimum requirements for digital controller parameters, namely, sampling time and quantization resolution dimensions, are determined.

All these techniques demonstrate how to control some unstable events and show some advantages of using the parameters of adjustment. In [13], the estimation of the parameters of a buck converter with digital-PWM control and ZAD strategy is presented. A visualization approach has been applied in [14], where the output voltage of a buck power converter is controlled by means of a quasi-sliding scheme. Such authors introduced the load estimator by means of Least Mean Squares to make ZAD and FPIC control feasible in load variation conditions, and comparative results for the buck converter with different control strategies (including SMC, PID and ZAD-FPIC) were presented. However, the work [14] lacks a complete analysis and the comparison of different effects induced by variations of the control parameters, particularly the control parameter N of the FPIC control technique.

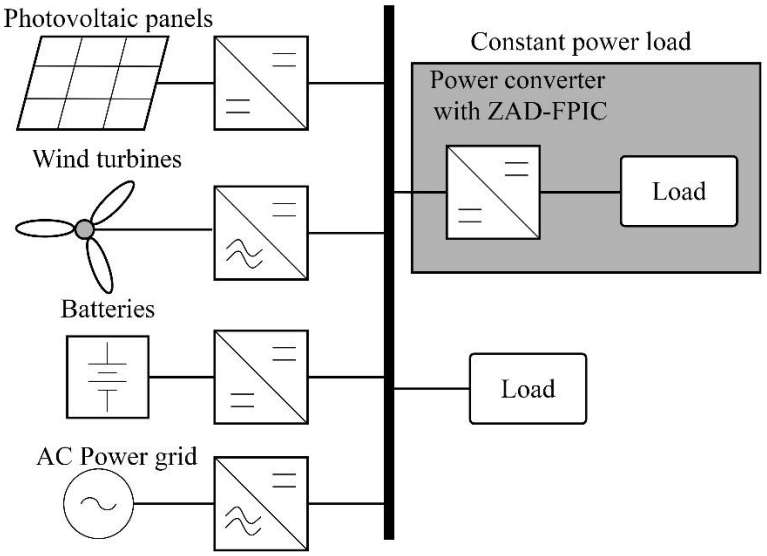


Fig. 1. Power converter with ZAD-FPIC used in a microgrid. Source: Authors.

According to the literature, the buck converter controlled by the ZAD and FPIC techniques has shown good output voltage regulation and tracking capabilities in both numerical simulation and experimental testing. Additionally, the quantization effects have been studied to evaluate the output signal response of the system. Although the stability behavior has been analyzed with only one parameter (in particular, the K_s parameter of the ZAD controller), other parameters have not been considered to evaluate the impact of the controller on the system's dynamics. For that reason, the goal of this paper is to present a transient and steady stability analysis of the buck converters controlled by the ZAD and FPIC techniques when the FPIC control parameter N is varied. Thus, the paper is organized as follows: Section 2 presents the materials and methods and the ZAD control strategy, Section 3 shows the FPIC control technique, Section 4 presents the results and analysis, and Section 5 concludes the paper.

2. MATERIALS AND METHODS

2.1 Buck converter controlled by ZAD-FPIC

Fig. 2 displays a diagram of the buck converter with an integrated control that uses the ZAD and FPIC techniques. The converter has a power source with voltage E, internal source resistor r_s, a metal-oxide semiconductor field-effect transistor (MOSFET) working as a switch S, an internal MOSFET resistance r_M, a diode D with forward voltage v_{fd}, a filter LC, an internal resistance of the inductor r_L, a resistance used to measure current r_{Med}, and a resistance R, which represents the load of the circuit.

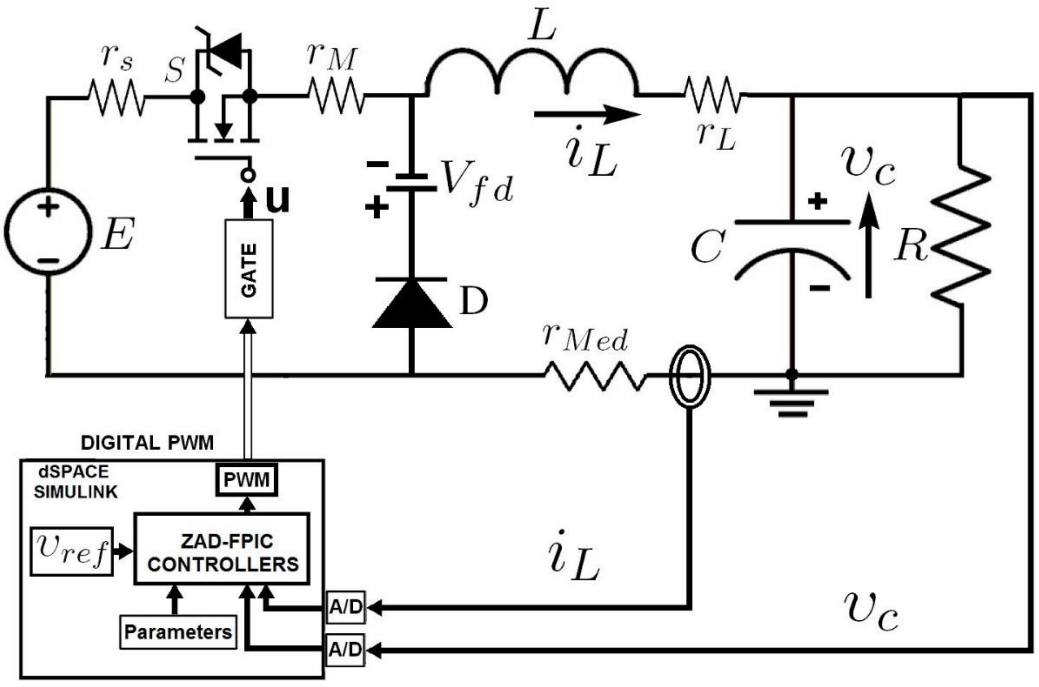


Fig. 2. Buck converter controlled by the ZAD-FPIC. Source: Authors.

Based on the circuit in Fig. 2, the output voltage v_C and the inductor current i_L are measured in discrete time at each sampling period T. These measures are the inputs for the ZAD-FPIC control law used to regulate the output signal v_C. The control requires adjusting the reference voltage x_{1ref} and the control parameters K_s and N. These parameters are responsible for the system dynamics and stability regions. In particular, x_{1ref} determines the maximum voltage that the DC–DC buck converter can reach, while the other two (K_s and N), besides imposing a particular system response, can induce bifurcations scenarios and chaotic behavior as well.

The output signal of the controller reaches the Centered Pulse Width Modulation (CPWM), which takes action on the switch S between ON (E) and OFF ($-v_{fd}$) states. This modulator consists of a circuit composed of a switch S and a DC power source which, in conjunction with the filter LC and the diode D, must supply to the load R an average voltage v_C during a switching period.

Fig. 3 shows the output signal of a CPWM, where d (duty cycle) is calculated for each period T, and E is the voltage magnitude.

When the output signal of the CPMW indicates the value u = 1, switch S is activated (ON). With this condition, the system is in continuous conduction mode (CCM) and the mathematical expression is as shown in (1):

$$\begin{bmatrix}\dot{v}_C\\ \dot{i}_L\end{bmatrix}=\begin{bmatrix}-\frac{1}{RC} & \frac{1}{C}\\ -\frac{1}{L} & \frac{-(r_s+r_M+r_{Med}+r_L)}{L}\end{bmatrix}\begin{bmatrix}v_C\\ i_L\end{bmatrix}+\begin{bmatrix}0\\ \frac{E}{L}\end{bmatrix} \quad (1)$$

This equation can be simplified as shown in (2), with the terms $a=-1/RC, h=1/C, m=-1/L$, and $p_2=-(r_s+r_M+r_{Med}+r_L)/L$. The term x_1 is the output voltage v_C, and x_2 is the current in the inductor i_L:

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix}=\begin{bmatrix}a & h\\ m & p_2\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\begin{bmatrix}0\\ \frac{E}{L}\end{bmatrix} \quad (2)$$

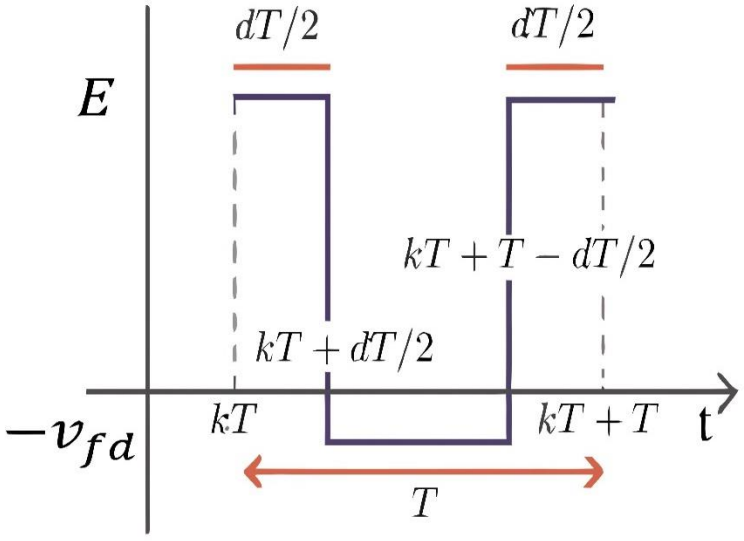


Fig. 3. Output signal of a CPWM. Source: Authors.

When the output signal of the PMWC indicates the value $u = 0$, the switch S is deactivated (OFF). With this condition, the system can be modeled by (3):

$$\begin{bmatrix}\dot{v}_C \\ \dot{i}_L\end{bmatrix} = \begin{bmatrix}-\frac{1}{RC} & \frac{1}{C} \\ -\frac{1}{L} & \frac{-(r_{Med}+r_L)}{L}\end{bmatrix}\begin{bmatrix}v_C \\ i_L\end{bmatrix} + \begin{bmatrix}0 \\ \frac{-v_{fd}}{L}\end{bmatrix} \quad (3)$$

This equation can be simplified as shown in (4), with the terms $a = -1/RC$, $h = 1/C$, $m = -1/L$, and $p_3 = -(r_{Med} + r_L)/L$. As previously defined, the term x_1 is the output voltage v_C, and x_2 is the current in the inductor i_L:

$$\begin{bmatrix}\dot{x}_1 \\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}a & h \\ m & p_3\end{bmatrix}\begin{bmatrix}x_1 \\ x_2\end{bmatrix} + \begin{bmatrix}0 \\ \frac{-v_{fd}}{L}\end{bmatrix} \quad (4)$$

Equations (2) and (4) have been simplified as shown in (5), where $x = [\dot{x}_1, \dot{x}_2]' = \left[\frac{dx_1}{dt}, \frac{dx_2}{dt}\right]'$. Matrices B_1 and B_2 contain information about the control inputs according to the scheme of the CPWM (Fig. 3):

$$\dot{x} = \begin{cases} A_1x + B_1 & \text{if } kT \le t \le dT/2 \\ A_2x + B_2 & \text{if } kT + \frac{dT}{2} \le t \le kT + T - dT/2 \\ A_1x + B_1 & \text{if } kT + T - \frac{dT}{2} \le t \le kT + T \end{cases} . \quad (5)$$

The output voltage must be regulated with the controller in a way that $x_1 = v_C$. The regulation must be performed in the predefined period T and then the switch must remain closed ($u = 1$) during the period of the duty cycle ($d \in [0, T]$).

2.2 ZAD control strategy

The technique proposed in [15] consists of defining a function and forcing an average value of zero at each sampling period [16]. Let us consider $s\big(x(kT)\big)$ as a piecewise linear function of the state value, described by (6) during a complete sampling period, and shown in Fig. 4. The slopes are calculated from the values of the state variables at the instant of sampling $t = kT$, as shown in (6) and (7). In [11], [13], [14], and [17], a comparison between numerical and experimental tests for the buck converter is presented.

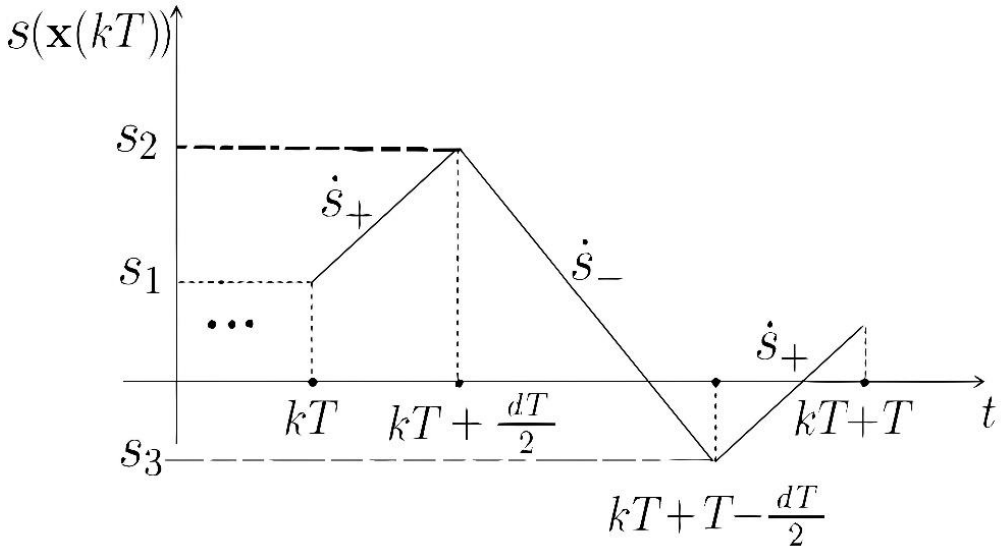


Fig. 4. Commutation expressed in sections. Source: Authors.

$$s\big(x(kT)\big) = \begin{cases} s_1 + (t-kT)\dot{s}_+ & \text{if } kT \le t \le kT + dT/2 \\ s_2 + (t-kT-dT/2)\dot{s}_- & \text{if } kT + \frac{dT}{2} \le t \le kT + T - dT/2 \\ s_3 + (t-kT-T+dT/2)\dot{s}_+ & \text{if } kT + T - \frac{dT}{2} \le t \le (k+1)T \end{cases} \quad (6)$$

where

$$\begin{aligned} \dot{s}_+ &= (\dot{x}_1 + k_s\ddot{x}_1)\big|_{x=x(kT),\ S=\text{ON}} \\ \dot{s}_- &= (\dot{x}_1 + k_s\ddot{x}_1)\big|_{x=x(kT),\ S=\text{OFF}} \\ s_1 &= (x_1 - x_{1ref} + k_s\dot{x}_1)\big|_{x=x(kT),S=\text{ON}} \\ s_2 &= \frac{d}{2}T\dot{s}_+ + s_1 \\ s_3 &= s_2 + (1-d)T\dot{s}_-. \end{aligned} \quad (7)$$

In this equation, $k_s = K_s\sqrt{LC}$, where K_s is a constant of the controller that will be considered as a parameter in the bifurcation analysis.

The mathematical description for the condition of zero average dynamics is given by (8). Herein, the first and third slopes in Fig. 4 have the same values, and to build the piecewise function $s\big(x(kT)\big)$ it is necessary to obtain information from the state values x_1 and x_2 at instant kT:

$$\int_{kT}^{(k+1)T} s\big(x(kT)\big)dt = 0. \quad (8)$$

Equation (8) is solved to obtain the duty cycle $d_{k(kT)}$ at each sampling time, which ensures the condition of zero average dynamics when applied to the system through switch S. The duty cycle was obtained in [9], [15] and can be expressed by Equation (9):

$$d_{k(kT)} = \frac{2s_1(kT) + T\dot{s}_-(kT)}{T(\dot{s}_-(kT) - \dot{s}_+(kT)}. \quad (9)$$

The authors would like to note that, in the experimental test, the state variables are measured to calculate the CPWM with a sampling frequency of 10 kHz and a one-period delay. Thus, the duty cycle used experimentally is given by (10), which means that the actual control law in the current period k is calculated with the values of state variables measured at the previous iteration (k-1):

$$d_{k(kT)} = \frac{2s_1((k-1)T) + T\dot{s}_-((k-1)T)}{T(\dot{s}_-((k-1)T) - \dot{s}_+((k-1)T)}. \quad (10)$$

3. FPIC TECHNIQUE

This control technique was proposed in [18], numerically tested in [19], and experimentally tested in [9]. Let's consider a system with a set of equations given by (11):

$$x(k+1) = f\big(x(k)\big) \quad (11)$$

Now, if a fixed point, namely x^*, exists and it is assumed to be unstable, then $x^* = f(x^*)$. Therefore, the space trajectory around it locally diverges if the Jacobian of the discrete system, denoted by $J = \partial f/\partial x$, presents at least one i, such that $|\lambda_i\ (J)| > 1$. Herein, the term λ_i represents the system eigenvalues. Moreover, let us assume there is a control parameter, namely N, in the Jacobian of the system; as a result, it is possible to ensure that $|\lambda_i\ (J, N)| < 1$ for all i. Hence, with control parameter N it is possible to guarantee the system's stabilization at a fixed point of (12) with real positive value:

$$x(k+1) = \frac{f\big(x(k)\big) + Nx^*}{N+1} \quad (12)$$

Changes in parameter N can be evaluated considering that the Jacobian of the new system (12) can be expressed as shown in (13), with J_c being the Jacobian of the controlled system and J being the Jacobian of the unstable system:

$$J_c = \frac{1}{N+1}J \quad (13)$$

Parameter N can be calculated directly through the Jury stability criterion; however, this work focuses on evaluating dif-

ferent values of parameter N to identify the behaviors of the output signal of the buck converter controlled by ZAD given in (10) and FPIC in (12). Then, the ZAD and FPIC techniques applied to the buck converter obtain a new duty cycle as expressed in (14):

$$d_{ZAD-FPIC}(kT) = \frac{d_k(kT) + Nd^*}{N+1}. \quad (14)$$

Herein, the term $d_k(kT)$ is obtained from (10) and d^* can be calculated at the beginning of each period as in (15):

$$d^* = d_k(kT)|_{steady\ state}\ . \quad (15)$$

Assuming a duty cycle greater than zero and less than 1, a saturation function given by (16) is applied.

$$d = \begin{cases} d_{ZAD-FPIC}(kT) & if\ 0 < d_{ZAD-FPIC}(kT) < 1 \\ 1 & if\ 1 < d_{ZAD-FPIC}(kT) \\ 0 & if\ d_{ZAD-FPIC}(kT) \leq 0 \end{cases}. \quad (16)$$

The duty cycle with the ZAD technique is calculated using (17) and (18) as presented by the authors of [14].

$$d_{k(kT)} = \frac{2s_1((k-1)T) + T\dot{s}_-((k-1)T)}{T(\dot{s}_-((k-1)T) - \dot{s}_+((k-1)T)} \quad (17)$$

Where

$$\begin{aligned} s_1((k-1)T) &= (1 + ak_s)x_1((k-1)T \\ &\quad + k_s h x_2\big((k-1)T\big) - x_{1ref} \\ \dot{s}_+((k-1)T) &= (a + a^2k_s + k_s hm)x_1((k-1)T \\ &\quad + (h + ak_s h \\ &\quad + k_s hp_2)x_2\big((k-1)T\big) \\ &\quad + k_s h(\frac{E}{L}) \\ \dot{s}_-((k-1)T) &= (a + a^2k_s + k_s hm)x_1((k-1)T \\ &\quad + (h + ak_s h \\ &\quad + k_s hp_3)x_2\big((k-1)T\big) \\ &\quad - k_s h(\frac{v_{fd}}{L}) \end{aligned} \quad (18)$$

When the FPIC control technique is used, (19) is obtained.

$$d^* = \left[\frac{x_{1ref}\left(1 + \frac{r_{Med} + r_L}{R}\right) + V_{fd}}{-x_{1ref}\left(\frac{r_s + r_M}{R}\right) + E_{sensado} + V_{fd}}\right]. \quad (19)$$

4. RESULTS AND ANALYSIS

This section presents a comparison between simulation and experimental tests of the buck converter controlled by ZAD-FPIC techniques with quantization effects.

4.1 Initial parameters

Table 1 shows all the parameters used for the simulation and experimental tests of the DC–DC power converter presented in Fig. 2. The parameters listed in Table 1, including voltages, resistances, inductance, capacitance, and commutation are assumed to be constant values to simulate the stability conditions, while control parameters K_s and N are modified. In particular, the tests consider changes in K_s from 0 to 5 and changes of N ranging from 1 to 20. Furthermore, the quantization effects for the tests are defined: 12 bits for analog inputs (v_C and i_L) and 10 bits for the duty cycle.

The proposed numerical model can be validated by using the frequency response of the circuit. Fig. 5(a) shows the Bode diagram with voltage v_C plotted in Matlab for the theoretical model, and Fig. 5(b) shows the Bode diagram with the voltage v_C plotted in LTSPICE with the same values of the elements used for the experimental test. As shown in these figures, the frequency response for both the magnitude and phase of the output voltage v_C are similar.

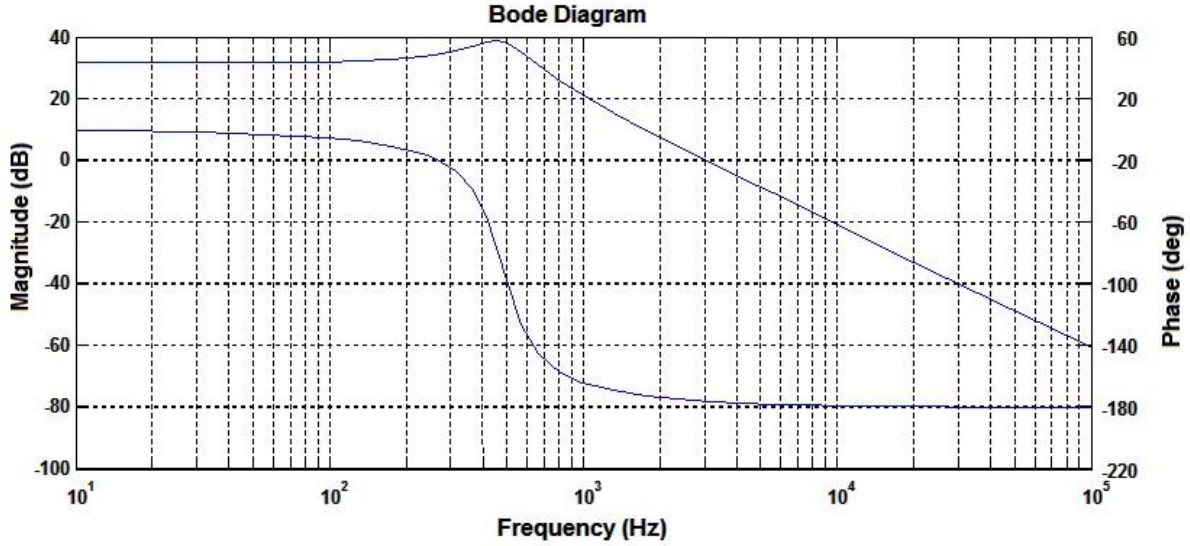
Table 1. Parameters for DC–DC power converter and ZAD-FPIC controller with 12 bits for ADC and 10 bits for duty cycle. Source: Authors.

Parameter	Description	Value
v_{ref}	**Reference Voltage**	32 V
E	Input voltage	40.086 V
R	Load resistance	39.3 Ω
C	Capacitance	46.27 μF
L	Inductance	2.473 mH
r_{Med}	Resistor to measure inductor i_L	1.007 Ω
r_L	Inductor Internal resistance	0.338 Ω
r_s	Internal resistance of the voltage source	0.3887 Ω
r_M	MOSFET resistance	0.3 Ω
v_{fd}	Forward voltage diode	1.1 V
N	FPIC Control parameter, (considered also as a Bifurcation parameter)	1–20
K_s	ZAD Control parameter	0–5
Fc	Commutation frequency	10 kHz
Fs	Sampling frequency	10 kHz
1T_p	Delay period	100 μs
bits ADC	Number of bits ADC	12 bits
bits d	Number of bits duty cycle	10 bits

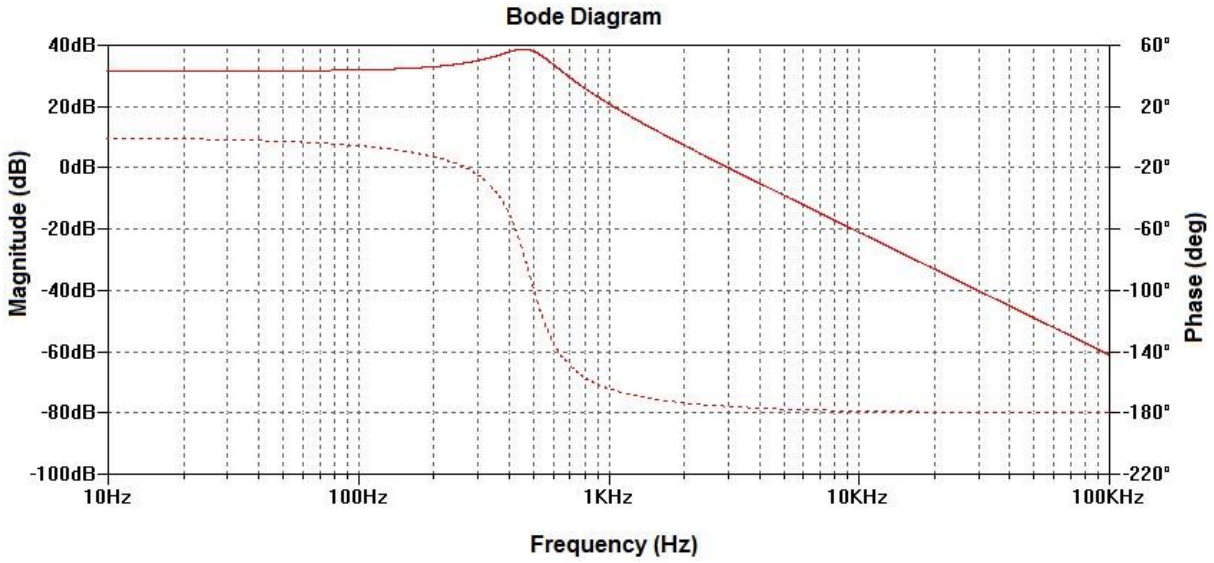
The comparison between numerical simulated and experimental bifurcation diagrams is shown in Fig. 6(a) and 6(b). In this case, the buck converter is controlled by ZAD-FPIC with N=1 and control parameter K_s (consider in Fig. 6 as a bifurcation parameter) is varied from 0 to 5. Fig. 6(a) shows the output capacitor voltage obtained via numerical simulations, while Fig. 6(b) shows the capacitor's output voltage of the buck controller with ZAD-FPIC measured by the experimental prototype.

The slight difference between numerical simulations and experimental results in Fig 6 is mainly due to parameters' uncertainties of electronic components in the DC–DC converter.

Both figures show that when bifurcation parameter K_s decreases, the system slowly loses its ability to regulate the voltage, passing through regions of chaotic behavior and periodic bands. The numerical simulation shows that the stability limit is approximately $K_s = 3.35$, whereas the stability limit in the experimental test was $K_s = 2.6$. This means that it is slightly shifted to the right, which is attributed to parameters' uncertainties that were neither modeled nor included in the controller, such as internal resistance, parasitic capacitances, and parasitic inductances in the elements of the circuit.

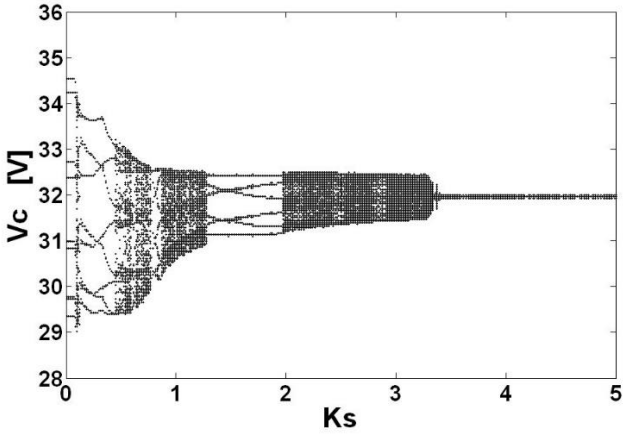


(a) Bode diagram computed with Matlab.

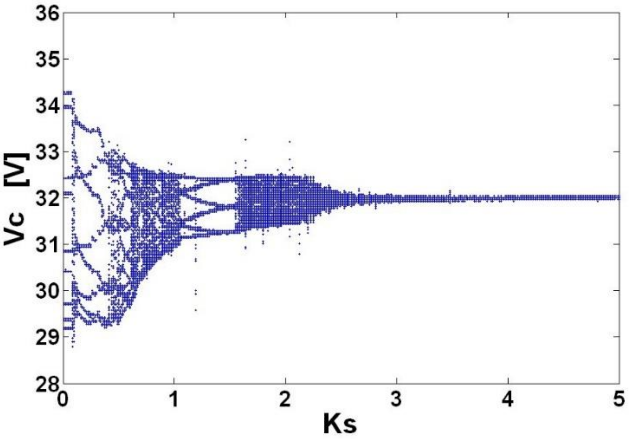


(b) Bode diagram computed with LTSPICE.

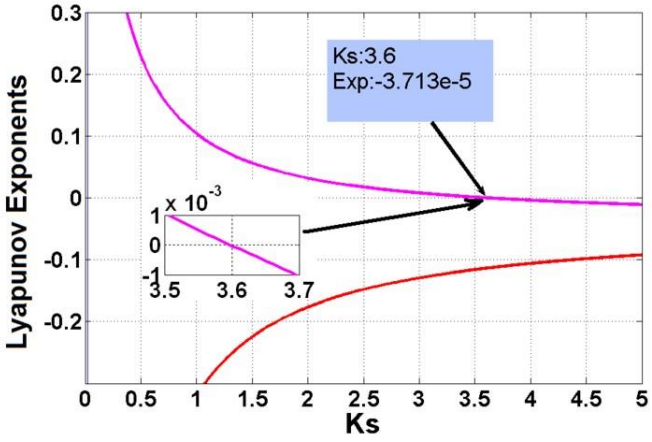
Fig. 5. Frequency-based validation using Bode diagrams. Source: Authors



(a) v_C vs. K_s for the numerical simulation test.



(b) v_C vs. K_s for the experimental test.



(c) Variation of Lyapunov exponents.

Fig. 6. Bifurcation diagrams when parameter K_s is changed. Source: Authors.

The figure of the experimental test shows a small cloud of electromagnetic noise due to commutation of switch S, which is in superposition to the noise of the electronic components and to the effects of quantization. However, this noise can be considered insignificant as the main band transitions and stability regions obtained numerically in simulations are well observed experimentally. In general, the numerical and experimental diagrams are similar, with minimum error in the experimental of 0.15% and in the simulation of 0.2%. Parameter K_s found in previous results is the starting point to consider other analyses of the buck converter controlled by ZAD-FPIC. In this case, it is necessary to evaluate the effects of changing control parameter N and reference voltage v_{ref}.

Now, the stability of the periodic orbit $1T$ [20] for the first model of the buck converter controlled by the ZAD and FPIC is determined with Lyapunov Exponents (LEs). LEs are directly calculated from the Poincare application given by (20).

Equation (20) can be simplified as (21):

$$\mathrm{x}(k+1) = \mathrm{F}(\mathrm{x}(k)). \tag{20}$$

Let $DF(x(k))$ be the Jacobian matrix of $F(\mathrm{x}(k))$ and the term $q_i(DF(x))$, the i-th eigenvalue of $DF(x(k))$. The LE (λ_i) of the respective eigenvalue is given by (22).

$$\lambda_i = \lim_{n\to\infty}\left\{\frac{1}{n}\sum_{k=0}^{n}\log|q_i(DF(x))|\right\} \tag{21}$$

Fig. 6(c) shows the evolution of the LEs computed with the mathematical solution. The results show that the LEs are negative for $K_s \geq 3.6$ in the theoretical analysis, which indicates the stability of the system. This is similar to the results obtained in the numerical simulation and coherent with the experimental observations. The stability limit in the experimental test is obtained when $K_s \geq 2.6$, whereas for the simulation test, it is $K_s \geq 3.35$.

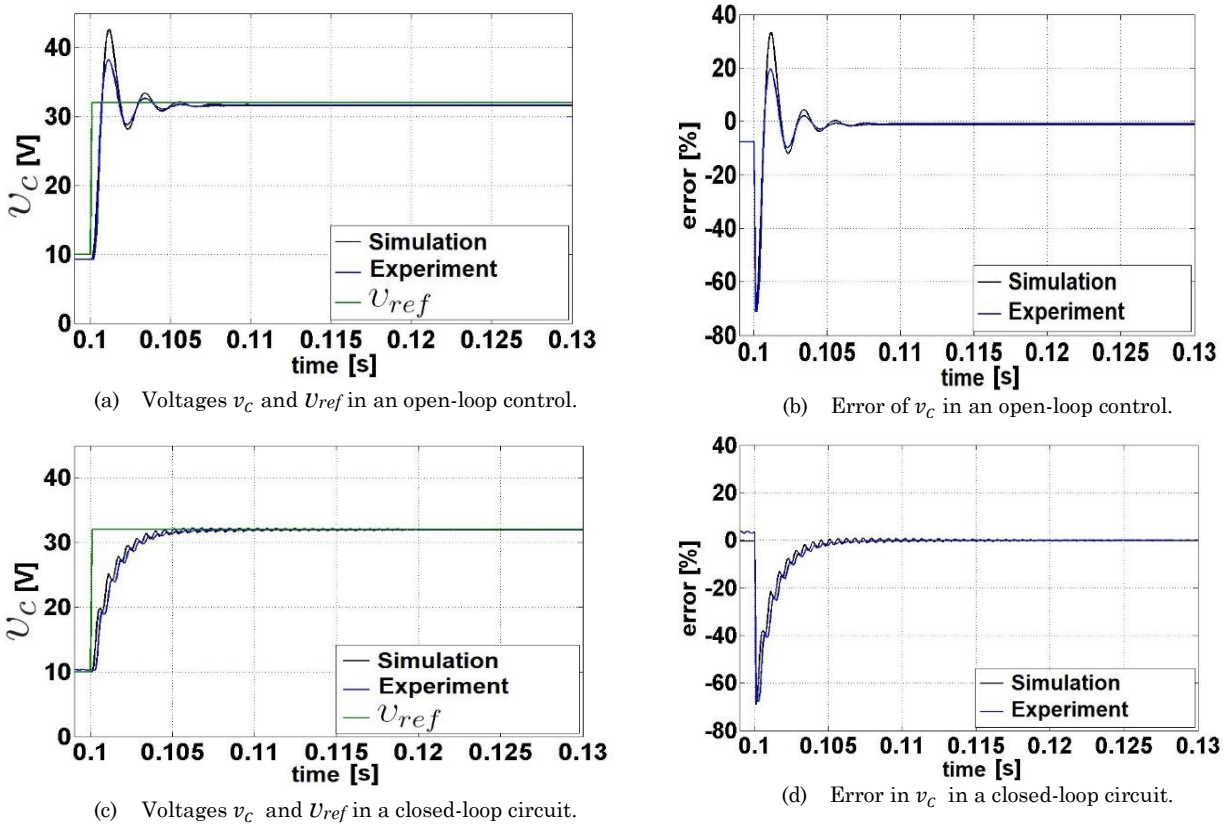
4.2 Buck converter with open- and closed-loop control

A voltage regulation analysis of the buck converter is performed when the controller works in open- and closed-loop circuit configurations. Both simulation and experimental tests are shown in Fig. 7(a) for the open loop case and in Fig. 7(c) for the closed loop with ZAD-FPIC controller. Here, the goal is to show how the ZAD-FPIC control technique regulates the output capacitor voltage of the DC–DC converter and the error of the response. Indeed, Fig. 7(c) shows that, in the closed-loop circuit configuration, the capacitor voltage does not exhibit voltage overshoot, which means no risk of voltage peaks for load R.

Thus, Fig. 7(a) and 7(b) show the output voltages and the errors of regulation for both the simulation and experimental tests when the buck converter works in an open loop. Those two figures show that the reference voltage is v_{ref} = 32 V. However, the voltage signals reach a high value with respect to the reference and start an oscillation that is further reduced.

Fig. 7(a) shows that, in the experimental test, the maximum voltage peak obtained is 38.3 V, which is equivalent to an overshoot of M_p = 19.6453%, whereas in the simulation test the maximum voltage peak is 42.6 V, which is equivalent to an overshoot of M_p = 33.2413%.

$$x((k+1)T) = e^{AT}x(kT) + [e^{AT} - e^{AT(1-\frac{d}{2})} + e^{AT\frac{d}{2}} - I]A^{-1}B. \tag{22}$$



(a) Voltages v_C and v_{ref} in an open-loop control.

(b) Error of v_C in an open-loop control.

(c) Voltages v_C and v_{ref} in a closed-loop circuit.

(d) Error in v_C in a closed-loop circuit.

Fig. 7. Numerical and experimental results for the buck converter with control in open- and closed-loop control. Source: Authors.

The settling time for the voltage signal v_C in the simulation is 4.7 ms, which is equivalent to 47 periods of commutation, whereas the voltage signal in the experiment is obtained as 4.4 ms, which is equivalent to 44 periods of commutation. The steady-state error for the simulation is −1.0443%, whereas in the experimental test it is −1.4%.

Fig. 7(c) and 7(d) show the output voltage and the regulation error in the time for both the simulation and experimental tests when the buck converter works with the control ZAD-FPIC in the closed-loop circuit. In this case, the reference voltage is adjusted to v_{ref} = 32 V. As observed in Fig. 7(c), the circuit has low overshoot for both simulation and experimental tests. The settling time for the regulated voltage signal v_C is t_s = 5.9 ms, which is equivalent to 59 commutation periods, whereas in the experimental test the time is t_s = 5.3 ms, which is equivalent to 53 commutation periods. The steady-state error for the simulation test is −0.0984%, whereas for the experimental test it is 0.0937%.

Table 2 shows the simulated and experimental results for the buck converter operating with control in open and closed loops. The term M_p is the overshoot, t_s is the time in seconds, and error corresponds to the percentage error between the reference voltage (v_{ref}) and the output voltages (v_C). The results for the closed loop in Fig. 6(b) and 6(c) show that the overshoots are not presented and the steady-state error is low; however, the settling time is augmented.

Table 2. Transient response indexes of the buck converter with control in open and closed loops.
Source: Authors.

Controller	Mp (%)	ts (ms)	Error (%)
Open-loop simulation	33.2413	4.7	-1.0443
Open-loop experimental	19.6453	4.4	-1.4000
Closed-loop simulation	0.8475	5.9	-0.0984
Closed-loop experimental	0.0197	5.3	0.0937

4.3 Transient stability analysis when changing control parameter *N*

Fig. 8 shows the transient response of the buck converter controlled by ZAD-FPIC in open and closed loops when $K_s = 4.5$, $v_{ref} = 32\ V$, and N changes from 1 to 20.

Both simulation and experimental tests show that the steady-state error is less than 1% for the different parameters of N. Both tests indicate that, when the value of N increases, the overshoot M_p (%) also increases. For smaller values of N and close to 1, M_p (%) tends to zero, but the settling time t_s increases.

Tables (3) and (4) summarize the results of Fig. 8. For values of N less than 5, the simulation and experimental tests are similar, but when N is greater than 7, some differences between the simulation and experimental tests are observed. Figs. 8(b) and 8(d) show that the duty cycle is not saturated in the steady state; therefore, there is a fixed switching frequency for all values of N shown in Table (4).

4.4 Consideration of parameter N

Fig. 9 shows the behavior of the system for a one-delay period when the parameter of the ZAD technique is fixed to a constant value of $K_s = 4.5$, while the FPIC control parameter N is varied to obtain the bifurcation diagrams.

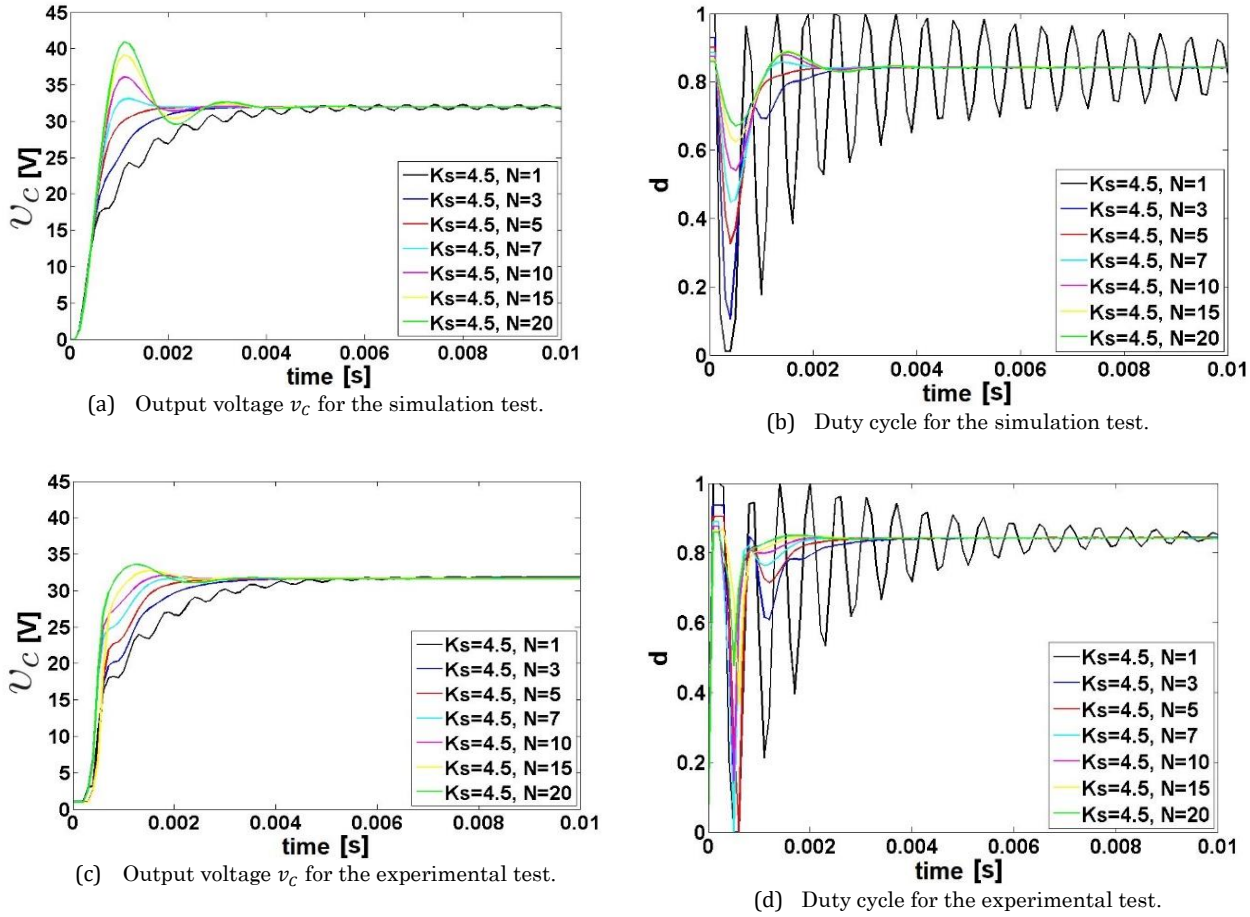
Table 3. Transient response indexes of the buck converter controlled with ZAD-FPIC for the simulation tests.
Source: Authors.

Operating Condition	Mp (%)	ts (ms)	Error (%)
$N = 1$	Overdamping	4	-1.04
$N = 3$	Overdamping	2	-0.0985
$N = 5$	Overdamping	2	-0.0985
$N = 7$	3.5501	2	-0.0985
$N = 10$	12.8993	2	-0.0985
$N = 15$	22.3667	3	-0.0985
N= 20	27.9291	3	-0.0985

Table 4. Transient response of the buck converter controlled with ZAD-FPIC for the experimental tests.
Source: Authors.

Operating Condition	Mp (%)	ts (ms)	Error (%)
$N = 1$	Overdamping	4.8	-0.2167
$N = 3$	Overdamping	2.8	-0.4532
$N = 5$	Overdamping	1.9	-0.5714
$N = 7$	Overdamping	1.4	-0.5714
$N = 10$	0.5943	1.2	-0.5714
$N = 15$	2.8535	1.5	-0.5714
$N = 20$	5.7209	2.3	-0.8079

The critical value for parameter N in the simulation test is $N_{cri} = 0.95$ and for the experimental test is $N_{cri} = 0.8525$. For values greater than N_{cri}, there is a change of stability and the regulated variable (v_C) tends to reach a fixed point, rendering the system stable. Therefore, with a value of $N \geq 1$ and $K_s = 4.5$, an acceptable voltage regulation is obtained.



(a) Output voltage v_C for the simulation test.

(b) Duty cycle for the simulation test.

(c) Output voltage v_C for the experimental test.

(d) Duty cycle for the experimental test.

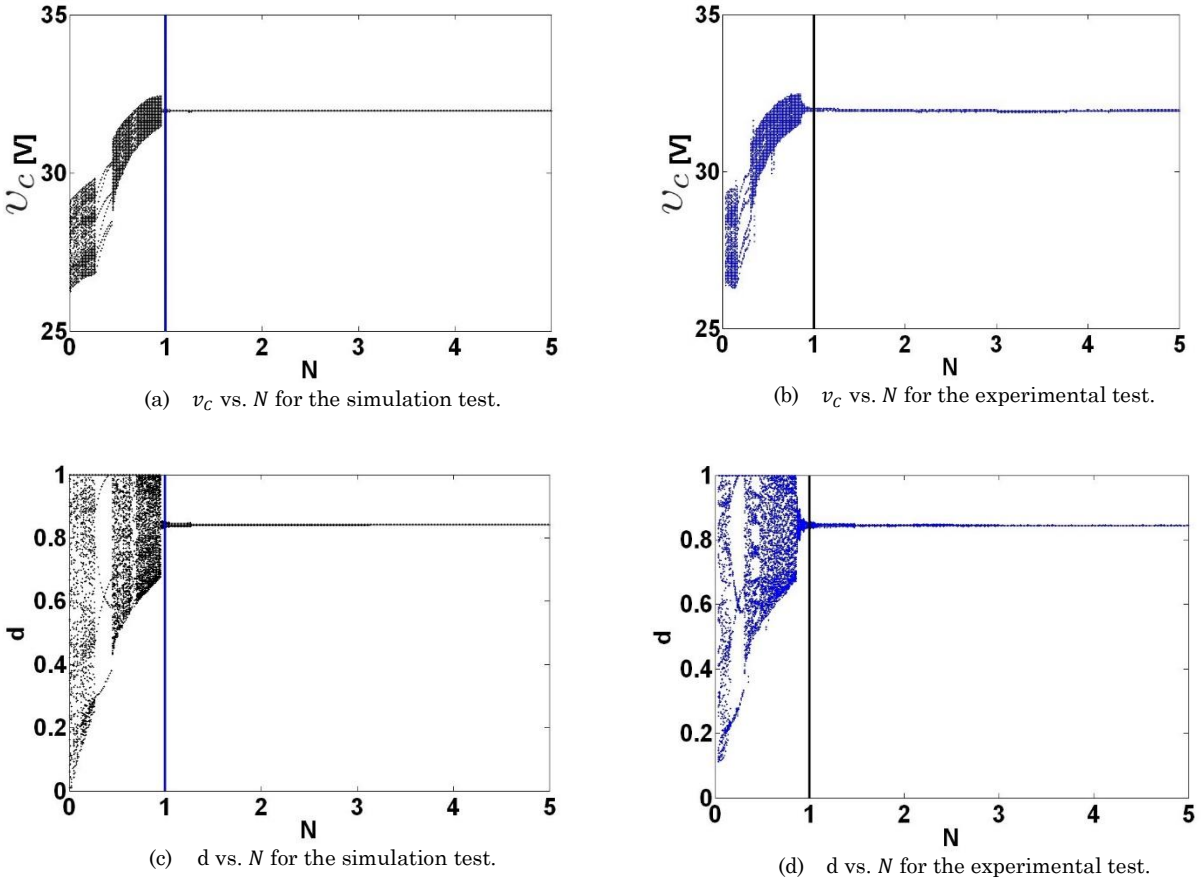
Fig. 8. Numerical simulations and experimental results to show the behavior of the buck converter when varying the ZAD-FPIC control parameters N with K_s = 4.5. Source: Authors.

In the simulation, chaos appears when values $0 \leq N \leq 0.2625$ and $0.45 \leq N \leq 0.95$, whereas in the experimental test the values are $0 \leq N \leq 0.1615$ and $0.3135 \leq N \leq 0.8525$. In the simulation, when the values are $0.2625 \leq N \leq 0.45$, there are regions with periodic bands, whereas in the experimental test those are presented in the range $0.1615 \leq N \leq 0.3135$. Furthermore, for the value of $N \geq 1.037$ in the simulation test and $N \geq 0.95$ in the experimental test, the errors are less than −0.1% and −0.335%, respectively.

In general, both numerical and experimental diagrams are qualitatively and quantitatively equivalent. Besides, the ZAD-FPIC control technique presents good performance when controlling the output capacitor's voltage v_C . Note from the results that the FPIC technique is effective in controlling the chaotic behavior.

Fig. 10 shows the results with $2T$ periods of delay when $K_s = 4.5$ and N changes in the range [0, 5]. The critical value of N for the simulation test is $N_{cri} = 2.47$ and for the experimental test is $N_{cri} = 3.24$.

Stable operation is experimentally ensured when the control parameter value is greater than the bifurcation point, that is, $N > N_{cri} = 3.24$, and the regulated state variable v_C tends to the desired value.



(a) v_C vs. N for the simulation test.

(b) v_C vs. N for the experimental test.

(c) d vs. N for the simulation test.

(d) d vs. N for the experimental test.

Fig. 9. Simulation and experimental tests with ZAD-FPIC control parameters K_s = 4.5 and N between 0 and 5 and a one-delay period. Source: Authors.

Therefore, with N = 3.5 and $K_s = 4.5$ there is good regulation. From the numerical bifurcation diagram in Fig 10, the regions with chaotic bands, fixed points, and periodic orbits are clearly observed. Although the experimental bifurcation diagram presents some noise due to measure interference, the main dynamic behaviors are captured, which results in a clear verification of numerically-predicted nonlinear phenomena.

In the simulation, chaos is present for values $0 \leq N \leq 0.2625$ and $0.45 \leq N \leq 0.95$, whereas in the experimental test the values are $0 \leq N \leq 0.1615$ and $0.3135 \leq N \leq 0.8525$. In the simulation, when the values are $0.2625 \leq N \leq 0.45$, there are regions with periodic bands, whereas in the experimental test those appear in the range $0.1615 \leq N \leq 0.3135$. Furthermore, for the value of $N \geq 1.037$ in the simulation test and ($N \geq 0.95$) in the experimental test, the errors are less than −0.1% and −0.335%, respectively.

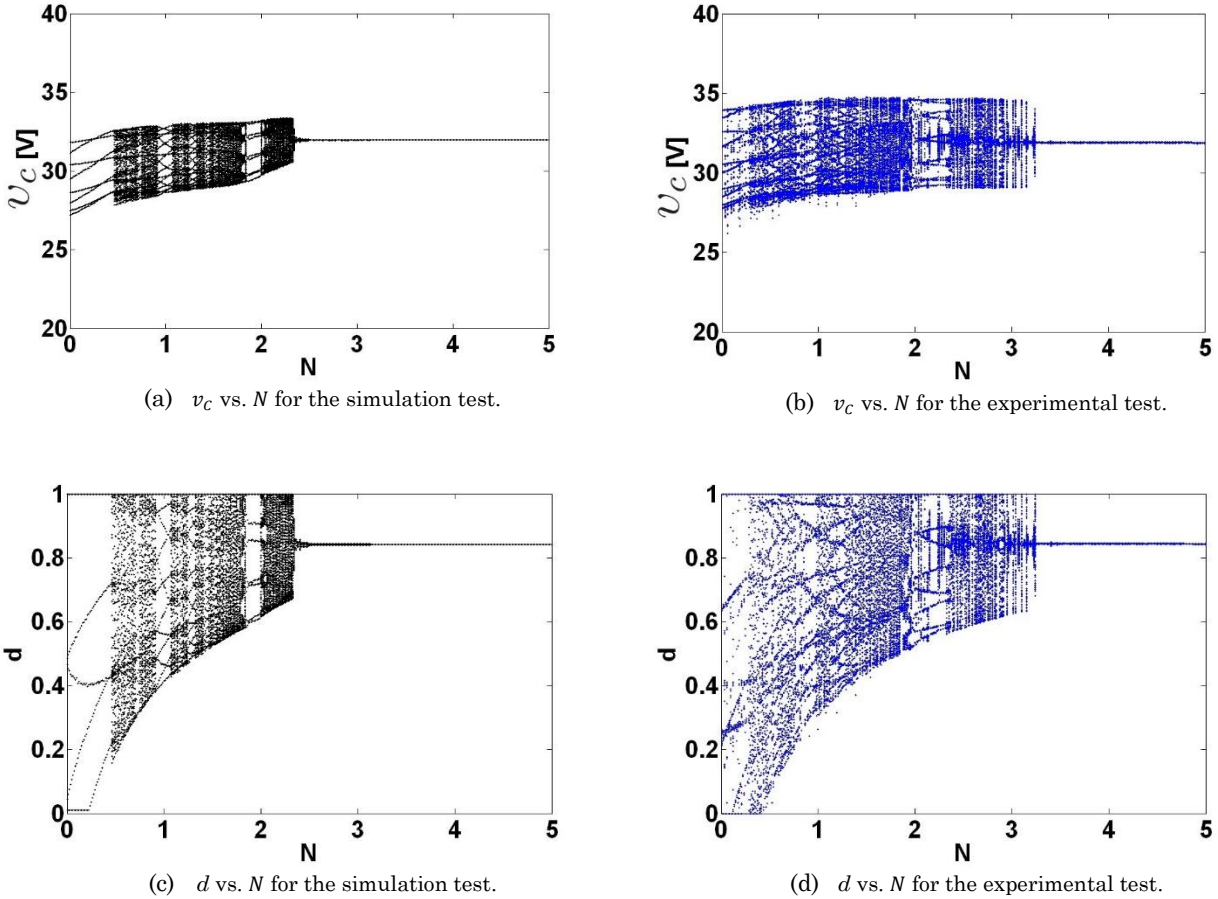
In general, both numerical and experimental diagrams are qualitatively and quantitatively equivalent. Besides, the ZAD-FPIC control technique presents good performance when controlling the output capacitor voltage v_C. Note from the results that the FPIC technique is effective to control the chaotic behavior

Fig. 10 shows the results with $2T$ periods of delay when $K_s = 4.5$ and N changes in the range [0, 5]. The critical value of N for the simulation test is N_{cri} = 2.47 and for the experimental test is N_{cri} = 3.24.

Stable operation is experimentally ensured when the control parameter value is greater than the bifurcation point, that is,

$N > N_{cri}$ =3.24, and the regulated state variable v_C tends to the desired value. Therefore, with N = 3.5 and K_s = 4.5 there is good regulation. From the numerical bifurcation diagram in Fig 10, the regions with chaotic bands, fixed points, and periodic orbits can be clearly observed. Although the experimental bifurcation diagram presents some noise due to measure interference, the main dynamic behaviors are captured, which results in a clear verification of numerically-predicted nonlinear phenomena.

In the stable region, a voltage regulation error lower than 0.1% was found in the simulation test, whereas in the experimental test this error is lower than 0.5%. In general, both the numerical and experimental diagrams represent the events in a similar manner. Despite the presence of two delay periods, the control technique ZAD-FPIC presents good performance in terms of tracking capabilities and voltage regulation when the control parameters are tuned in the range $N \geq 3.5$, with K_s = 4.5.



(a) v_C vs. N for the simulation test.

(b) v_C vs. N for the experimental test.

(c) d vs. N for the simulation test.

(d) d vs. N for the experimental test.

Fig. 10. Numerical simulation and experimental bifurcation diagrams with constant K_s = 4.5 , with 2T delay periods and N as bifurcation parameter varying from 0 and 5. Source: Authors.

Fig. 11 shows a two-dimensional numerical bifurcation diagram that considers control parameters N and K_s as bifurcation parameters. This figure shows that, for different values of control parameter K_s and considering a constant value of $N = 1$, the system is close to a very sensitive zone of instability. This situation occurs because any small disturbance in the system's parameters (temperature or load variations) can result in entering the unstable region.

Therefore, in this scenario, control parameter N should be increased to a greater value, so as to operate the closed loop buck converter in a more robust region and improve the robustness of the system. From the application viewpoint, the tuning of the ZAD-FPIC controller to operate the system in such a robust operating region is fundamental. In so doing, the controller can account for buck converter circuit parameter variations and scenarios where load R can also change.

4.5 Changes in source *E*

Fig. 12 shows the dynamic behavior of the buck converter when input voltage E of the buck converter controlled with ZAD-FPIC controller is changed. The goal of this study is to analyze the robustness properties of the controller with respect to input variations and, of course, to assess the impact on output voltage experienced by load R. From the application viewpoint, this assessment is very important since in microgrid technologies, e.g. photovoltaic panels (affected by variations of sun light intensity) and wind turbines (wind flow variations), power supply can exhibit voltage variations.

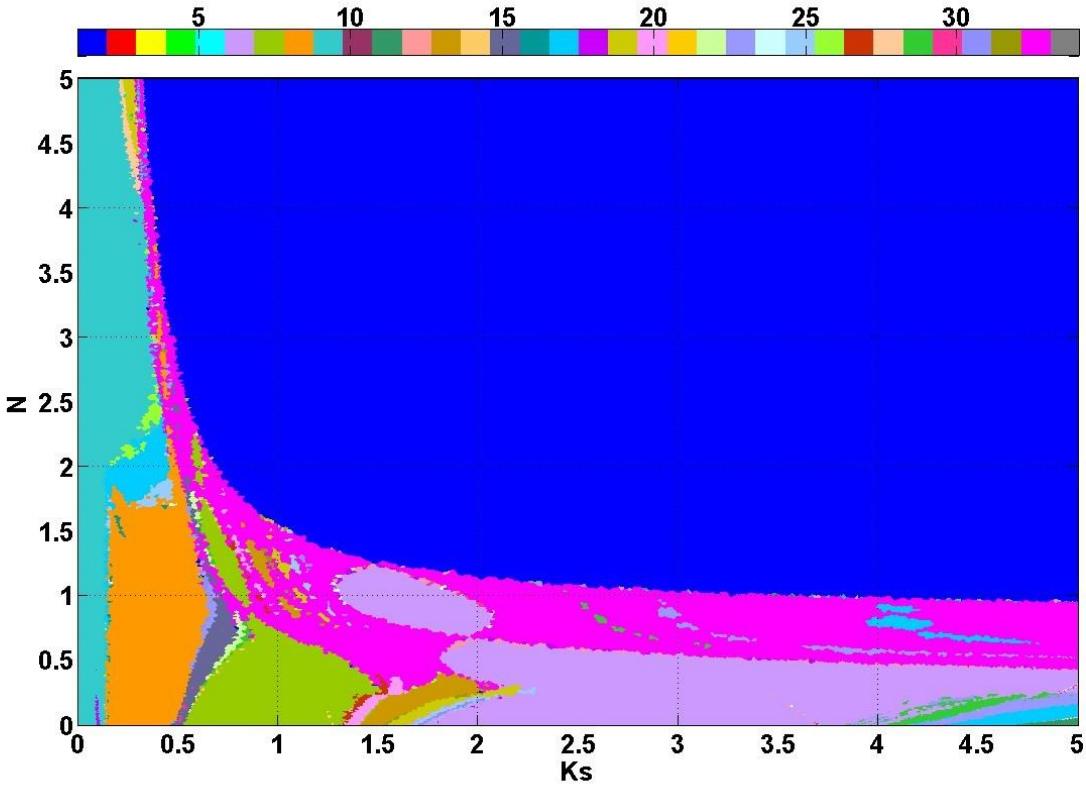
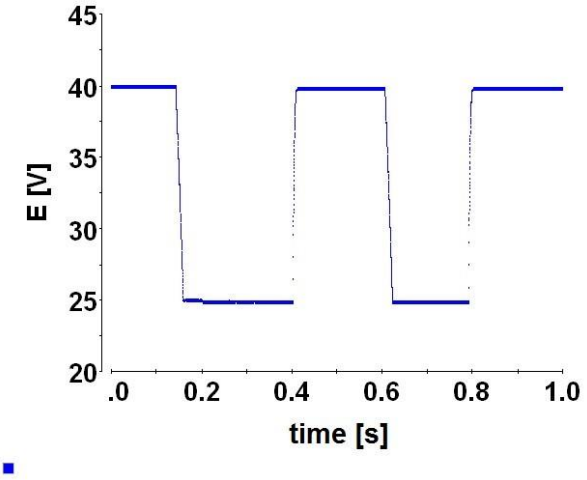


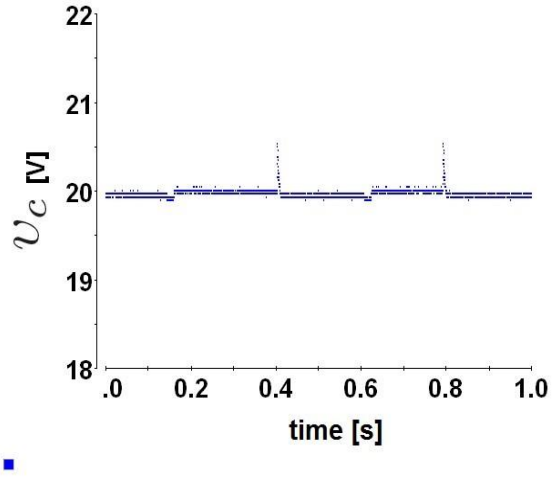
Fig. 11. N vs. K_s in the two-dimensional bifurcation diagram obtained in the simulation test. Source: Authors.

These experiments require measuring E with another 12-bit ADC channel, as well as state variables v_C and i_L. The measurement is synchronized with the PWMC and sampled at $Fs = 1/T = 10$ kHz. In this case, $K_s = 5$, $N = 1$. Fig. 12(a) shows the changes or disturbances produced in the voltage source with respect to the time. This input disturbance is used to evaluate the voltage regulation of the buck converter with the ZAD-FPIC controller.

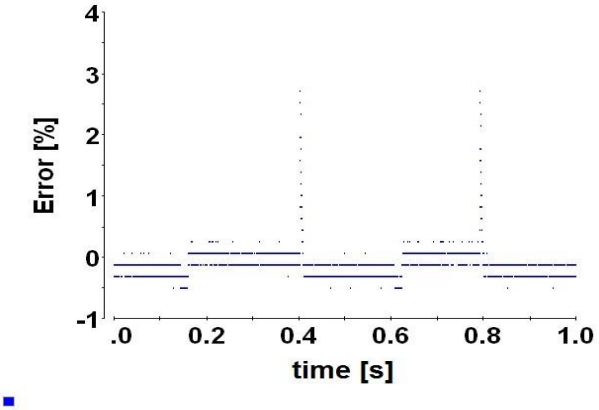
Fig. 12(b) shows the good regulation capability of the buck converter controlled by ZAD-FPIC, where v_{ref} =20V. Note that despite all the variations produced in the voltage source, the ZAD-FPIC controller ensures a regulated voltage of 20 V to load R. Of course, during the transients a small error takes place for all the input changes shown in Fig. 12(a). Such error never exceeds 1 V, as shown in Fig. 12(c), which means a robust response of the ZAD-FPIC controller. Fig. 12(d) shows the transient effect described by trajectory in the plane v_C vs. E. The main observation is that input variations do not impact the voltage on load R since the voltage is properly regulated with the robust ZAD-FPIC technique, which allows to protect the load from voltage peaks while ensuring a regulated output.



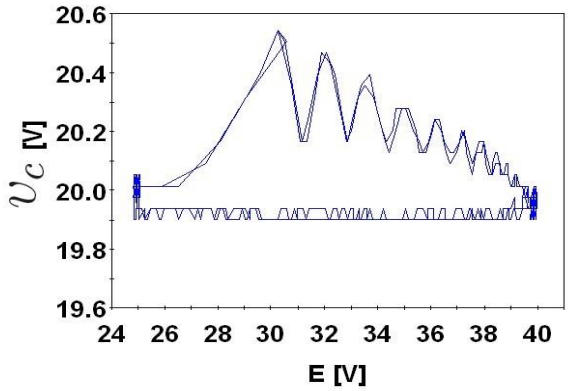
(a) Variation of *E*.



(b) Regulated output voltage v_C.



(c) Error in the controlled variable.



(d) Behavior of v_C vs. *E*.

Fig. 12. Experimental results of the buck converter to test the ZAD-FPIC control robustness with respect to instantaneous disturbances in input voltage E, ZAD-FPIC's control parameters are K_s = 5, and N = 1.
Source: Authors.

5. CONCLUSIONS

This paper has presented the steady-state and transient stability analysis of a buck converter controlled by ZAD-FPIC control technique. Numerical predictions via simulations have been validated using an experimental prototype of a buck converter controlled with ZAD-FPIC. The results have shown that the buck converter with ZAD-FPIC regulates the output voltage with low error values. The effect of control parameters on the regulated voltage has been studied in terms of capacitor voltage overshoot and settling time. Furthermore, the simulation and experimental tests have shown that strategy of controlling the buck converter with ZAD-FPIC enables to regulate the output voltage, even in the presence of two delay periods.

Numerical and experimental bifurcation diagrams have been obtained and compared for different operating conditions. The numerically-predicted regions (including periodic bands, chaotic bands and stable fixed-point) were successfully validated with experiments. The observed nonlinear dynamics reveal new open topics that can be the subject of future research to understand the observed bifurcations.

This paper has also presented a robustness analysis of the buck converter controlled with ZAD-FPIC with respect to disturbances in the power supply. Experimental results have shown that, for a large variation in the input voltage source, the ZAD-FPIC controller ensures a regulated voltage to load R.

Voltage can present high fluctuations in alternative energy systems due to the variability in energy sources. Therefore, this paper has shown how the ZAD-FPIC controller can regulate the output voltage in a buck converter even when strong changes in the input voltage take place, thereby demonstrating the robustness of the system in the presence of voltage variations.

In microgrids, there is a large number of variables to control and the processes require a large effort for signal processing and control. Time delays when sending control signals and global instability problems arise during real-time operation of the system. With the use of FPIC, the DC–DC system can be stabilized even with two delay periods, which represents a great advantage for the application to control systems with time delays.

6. ACKNOWLEDGMENTS

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