3-2020

Real-time Monitoring of the Semiconductor Wirebond Interconnection Process for Production Yield and Quality Improvement

Reymart Rio C. Haldos

Patricia Angela R. Abu

Carlos M. Oppus

Rosula SJ Reyes

Real-time Monitoring of the Semiconductor Wirebond Interconnection Process for Production Yield and Quality Improvement

Reymart Rio C. Haldos
Department of Electronics, Computer, and Communications Engineering
Ateneo de Manila University
Katipunan Ave., Loyola Hts., Quezon City, 1108 Philippines
reymart.haldos@obf.ateneo.edu

Patricia Angela R. Abu
Department of Information Systems and Computer Science
Ateneo de Manila University
Katipunan Ave., Loyola Hts., Quezon City, 1108 Philippines
pabu@ateneo.edu

Carlos M. Oppus
Department of Electronics, Computer, and Communications Engineering
Ateneo de Manila University
Katipunan Ave., Loyola Hts., Quezon City, 1108 Philippines
coppus@ateneo.edu

Rosula S.J. Reyes
Department of Electronics, Computer, and Communications Engineering
Ateneo de Manila University
Katipunan Ave., Loyola Hts., Quezon City, 1108 Philippines
rsjreyes@ateneo.edu

Abstract

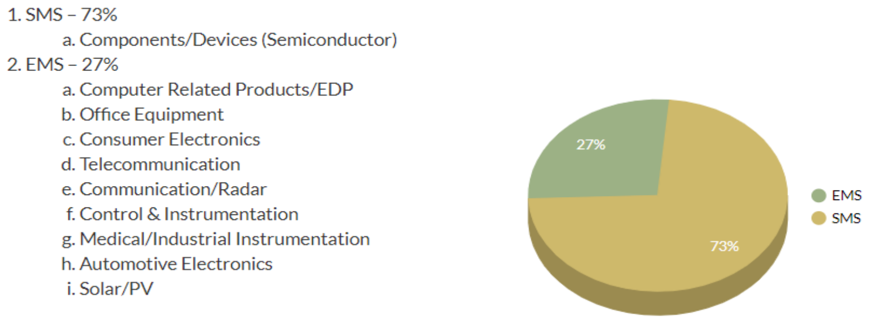
The electronics industry in the Philippine is the largest contributor to the manufacturing sector within the country. The Philippines is also considered the fastest growing economy in the region where its electronics products are among its top exports. The manufacturing of new electronics devices that comes with the emerging technologies translate to new processes that require new equipment that poses challenges to the industry. Thus, innovative solutions are developed by the engineers to improve and increase the production yield.

This study presents the development of a monitoring system that is interfaced to an existing wirebonding machine as a means of improving production yield. The system detects and records the bouncing of the "area under bond" which is identified as a major cause of product rejection. The Arduino-based microcontroller takes the U/SG (Ultrasonic Generator/Gain) signals from the machine. The Raspberry pi monitors the real-time signal provided by the microcontroller and compares the signal from the database module with trained signals. Tests run show that the system can detect the signals and present it in a ".csv" file format. Twenty (20) units of a specific electronic device were tested to identify between good and defective device.

Keywords
Wirebond, Production Yield, Quality Improvement, Device Under Test

1. Introduction

The world demand for electronics devices and equipment is continuously increasing. This growing trend in a socio-technological era boosts the Philippine economy since the electronics and semiconductor industry is the largest contributor to its manufacturing industry and still has the highest percentage impact on the Gross Domestic Product (GDP) of the county. The Philippine Electronics Industry is classified into two, the Semiconductor Manufacturing Services (SMS) and the Electronics Manufacturing Services (EMS) which comprises 73% and 27%, respectively, as illustrated in Figure 1. Most of the electronics businesses in the country operate in four key areas: Metro Manila, CALABARZON, Northern/Central Luzon and Cebu. Electronic companies in the country practice the best-known methods in manufacturing with capabilities ranging from IC packaging, PCB Assembly and Full Product Assembly. [1]



Source: NSO (2012)

Figure 1. Classification of Electronics Industry.

The SMS class with the largest percentage among the electronics and semiconductor industry, however, is faced with the challenges brought about by the complexity and technical requirement of these new electronics devices as they require new processes and procedures. New electronics devices come with new expensive machines that local-based companies find it too expensive to purchase. The use of old machines on the other hand, requires additional maintenance thus reducing the product yield. Upgrading machines and equipment entails additional costs and reduces manpower requirements.

Electronics devices and equipment consist of integrated circuits that are built with millions of semiconductor components. Manufacturing of semiconductor devices undergoes various manufacturing processes that include the following: wafer fabrication, wafer dicing, die attach, wire bond interconnection, encapsulation, and testing. This study will focus on the wirebond interconnection process since this poses the most challenging part of the manufacturing process.

Wirebonding is an electrical interconnection technique that uses a thin wire with a combination of heat, pressure and/or ultrasonic energy. Wirebonding is a solid phase welding process where the two metallic materials, wire and pad surface, are brought into firm contact. Once the surfaces are in firm contact, electron sharing or interdiffusion of atoms takes place resulting in the formation of a wirebond. In a wirebonding process, the bonding force can lead to material deformation, breaking up of the contamination layer, and smoothing out of the surface asperity, which can be enhanced through ultrasonic energy. Heat can accelerate Interatomic Diffusion, thus the wirebond formation. [2]

Basically, wirebonding is the process in which the pads are connected onto a die and leadframe (or substrate) using a very thin wire. The basic steps of wirebonding include the formation of the first bond (normally on the chip), the wire loop, and the second bond (normally on the substrate). The wire-bonding process sequence is illustrated in Figure 2.

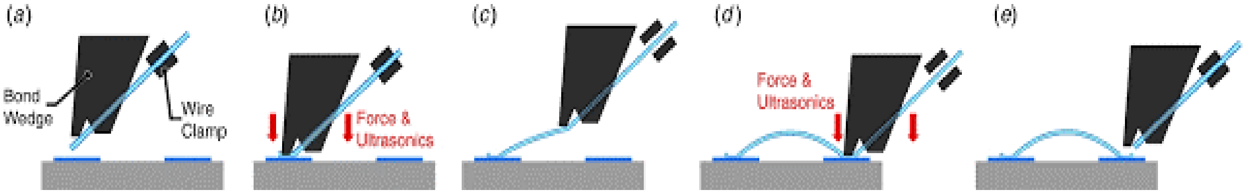


Figure 2. Wirebonding Process.

In Figure 2(a) the wirebonder head goes to the first bond area (normally on the chip). In Figure 2(b) the wirebonder head starts the wirebonding process by applying three main parameters: (1) ultrasonic power which is used to form the formation of wire, (2) the force which is used to press the formed wire towards the area under bond, and (3) the time which is used to induced these two parameters. The next step in the wirebonding process is shown in Figure 2(c) where the wirebonder head makes a loop towards the second bond area. This step is followed by the second wirebond process as show in Figure 2(d) which is just the same process as Figure 2(b). The wire bond process sequence ends with the release of the wire bond head as shown in Figure 2(e).

The wirebond process takes into account three important parameters, namely: (1) the power (ultrasonic), which is used for the formation, (2) the force, which is used to press the formed wire, and (3) the time, which is required to ensure that the wires are bonded.

2. Industry Yield Report

Figure 3 shows the assembly manufacturing pareto of reject encountered during the first two quarters of the year 2019. It lists the top five (5) sources of rejects: (1) Scratch, (2) Chip-out, (3) Wedge-off, (4) Bond-off, and (5) Tool Mark, measured in KPPM (thousand pulse per million) unit. It can be seen from the graph that the highest reject is wedge-off and if combined with bond-off will even increase the number of rejects. These two types of rejects occur in the wirebonding process. Based in the assembly manufacturing pareto of rejects, 60% of the rejects are induced by the wirebond assembly process.

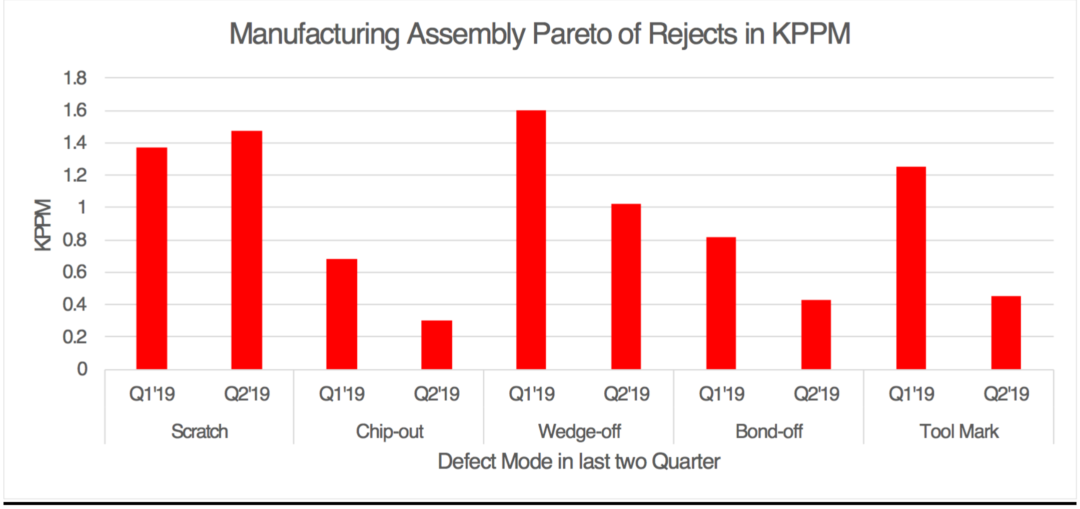


Figure 3. Assembly Manufacturing Pareto of Rejects.

Interventions in process control and manpower development are continually implemented but the improvement is minimal. Wirebonding machines have an operating life span that allows optimum yield. Preventive maintenance may extend the operational life of the machines but to a large extent, wear and tear still influence the operation of the machine.

This paper presents the development of a monitoring system that is interfaced to an existing wirebonding machine to improve the production yield. The system detects and differentiates between the good wirebond signal over the poor wirebond signal and makes the necessary action to stop the wirebonding operation when the signal is considered poor.

3. Methodology

Figure 4 illustrates the four phases towards the development of the monitoring system. It is composed of the following phases: (1) wire bond signal acquisition, (2) wire bond signal determination (3) definition of the wire bond signal window limit, and (4) definition of the reject criteria. The first phase is a hardware implementation of the system that involves the design of the sensor module, the controllers, and the computing device for real-time acquisition and monitoring of the wirebond signal. The second phase compares the acquired signal from a set of good and poor wire-bond signals. During this phase, detection of a good signal and a poor signal determines whether the unit is a good unit or a defective unit, respectively. The third phase involves defining the wirebond signal window that separates a good signal from a poor signal, and therefore differentiates a good unit from a defective unit. The range of the known good wirebond signal and its boundary in comparison to the known poor bond signal will be defined in this phase. In the fourth and last phase, Definition of Reject Criteria will be determined by doing wirebond pull test on taken samples from known good signal and known poor signal.

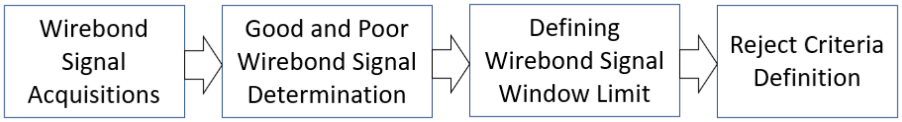
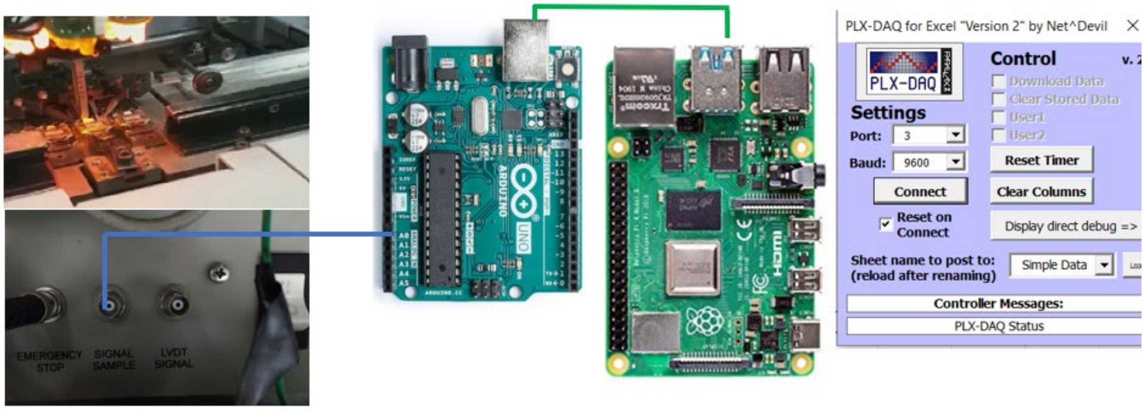


Figure 4. Methodology Phases.

4. Data and Results

4.1. Wirebond Signal Acquisition

The wirebond signal acquisition set-up is shown in Figure 5. The existing wirebond machine is equipped with an ultrasonic generator sample signal port. The generated analog sample signal (ultrasonic bond signal) from this output port is applied to the Arduino Uno Microcontroller using a BNC (Baby Neill Constant) coaxial cable. The Arduino Uno Microcontroller output signal is then applied to the Raspberry Pi Microprocessor unit. The acquired signal is presented and stored in ".csv" file for graph presentation and dataset information, also shown in Figure 5.



Port: 3
Baud: 9600
☑ Reset on Connect
Sheet name to post to: (reload after renaming) Simple Data
PLX-DAQ Status

Figure 5. Wirebond Signal Acquisition Set-up.

4.2. Good and Poor Wire Bond Signal Determination

An initial test run was conducted using Arduino and raspberry pi to gathered sample signals which are presented in ".csv" file. Graphical presentation of the acquired signal illustrates the difference of good signal (produced good unit) over the poor signal (produced defective unit).

Below are the steps conducted:

1. Set-up the Arduino on USG signal port of wirebond machine.

2. Wirebond 20 units of a specified device using the following conditions:
    2.1. wire bond 10 units with known stable and good clamping of units
    2.2. wire bond 10 units with no clamping at leadframe/unit post (worst case in production, simulated scenario that the clamp is not totally functioning)
3. Review the data gathered (.csv file)

Figure 6 shows the gathered bond signal for known good units and known reject units.

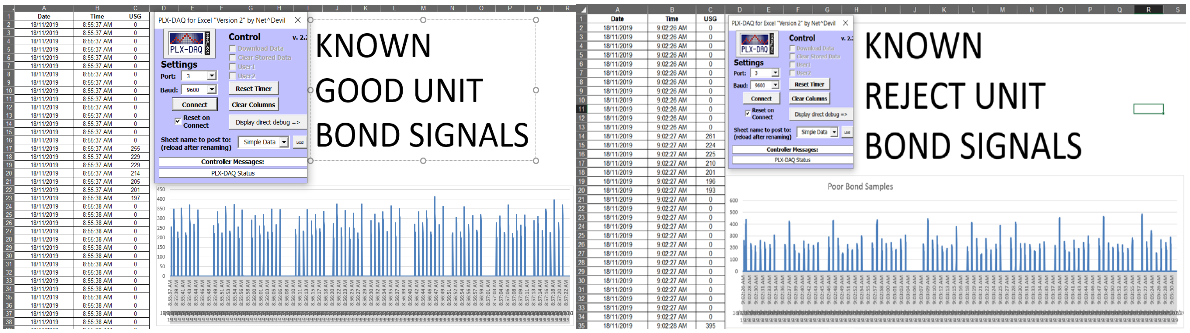


Figure 6. Acquired known good and reject units bond signals.

Vehicle Unit used was composed of 4 wirebonds, with each wirebond having two signals. The 1st wirebond is on the die and the 2nd wirebond is on leadframe lead post. It is expected to get an 8-graph profile for each unit.

To analyze the difference of known good wirebond signal compare to known poor wirebond signal, the gathered signal was split in two group (the 1st bond and 2nd bond) since two bonds are using different wirebond parameters. It is then presented in plot per point instead of time axis. Figure 7 shows the separated good bond signal for 1st bond and 2nd bond. Figure 8 shows the graphical presentation of separated poor bond signal for 1st bond and 2nd bond. Based on the gathered data, it clearly shows that poor bond signal was scattered and not stable compare to the good bond signals. With this result, it is possible to differentiate the good and poor bond signal. A wedge-off at 2nd bond on simulation bond with out wirebond clamp was also observed. Figure 8 .0 shows the separated poor bond signal for 1st bond and 2nd bond.

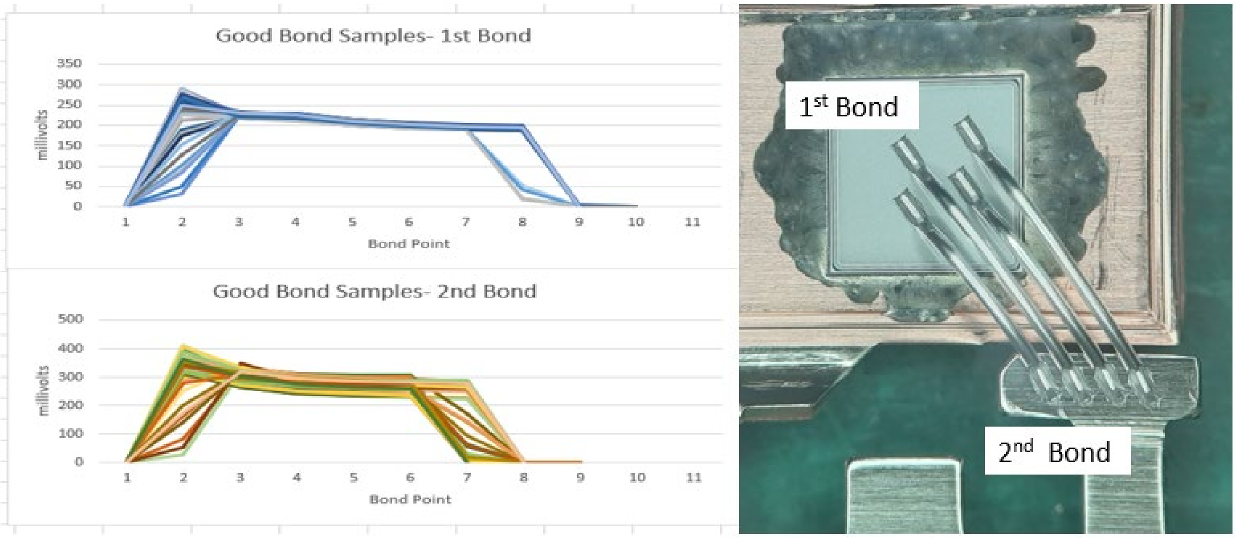


Figure 7. Graphical presentation of known good bond signal for 1st and 2nd bond.

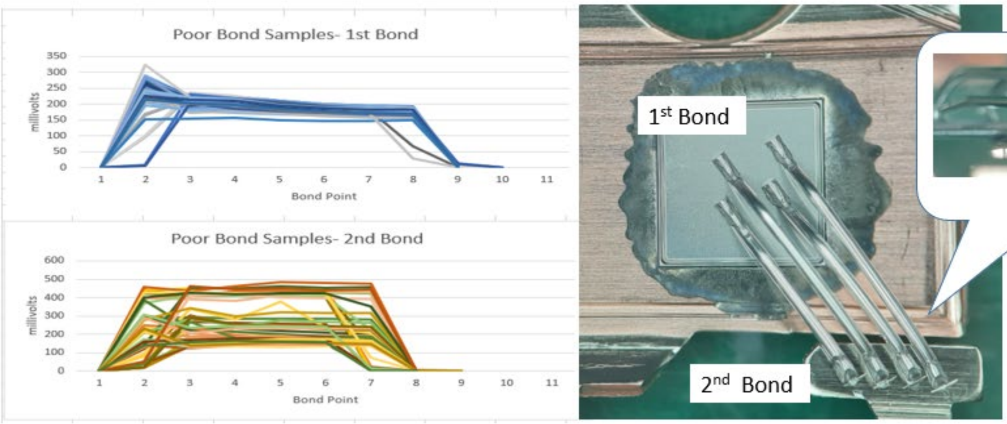


Figure 8. Graphical Presentation of known poor bond signal for 1st and 2nd bond.

4.3. Defining Wirebond Signal Window Limit

To define the wirebond signal window limit, the range of the gathered known good signal is calculated for every point. For conditions where good wirebond signal passes the wire pull test requirement, the minimum and maximum values of each point are used to determine the baseline of the window limit in reference to a specified tolerance requirement. Figure 9 shows a graphical presentation of good bond signal for the defined window limit of 1st and 2nd bond.

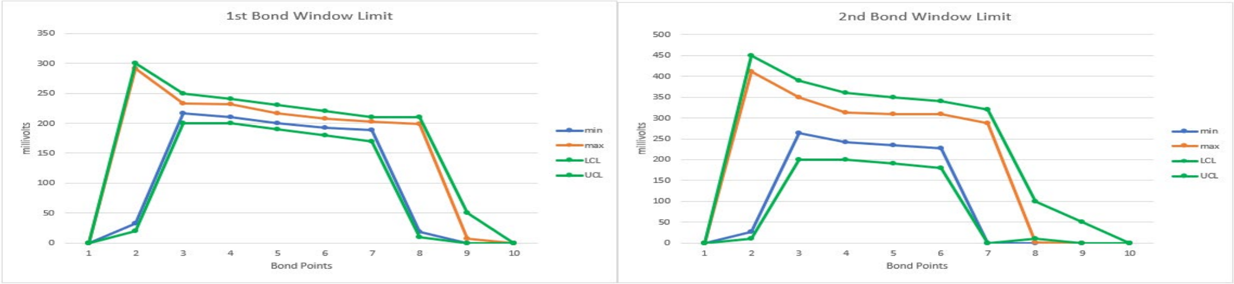


Figure 9. Graphical Presentation of good bond signal window limit for 1st and 2nd bond.

4.3.1.Simulation of Defined Wirebond Signal Window Limit

To simulate the effectiveness of the defined window limit, signals of identified good and poor wirebond signals are compared in the window limit graph. Shown in Figure 10 are graphical representations of good and poor bonds identified within the defined window limit. Based from these data, the graphical profile of good and poor wirebond signals of the identified good wirebond samples (1st and 2nd bond) are within the defined window limit, while it can be observed that the known poor wirebond signal samples profiles are outside the defined window limit.

4.3.2.Verification of Defined Window Wirebond Signal Limit

To verify the reliability of the defined window limit, wirebond pull test and visual inspection of every bond is performed. Table 1 shows the table of data for wire pull tests and break modes for all samples from good and poor wirebond signals.

Based on the result of the wire pull tests of all the samples, all test readings from known good bond signals ranges from 907 to 1000gram force. All readings are above the minimum requirement of 350-gram force. On the contrary, the wire pull test readings from the known poor bond signals ranges from 0- 895-gram force. And noticeably that all break modes are wedge-off.

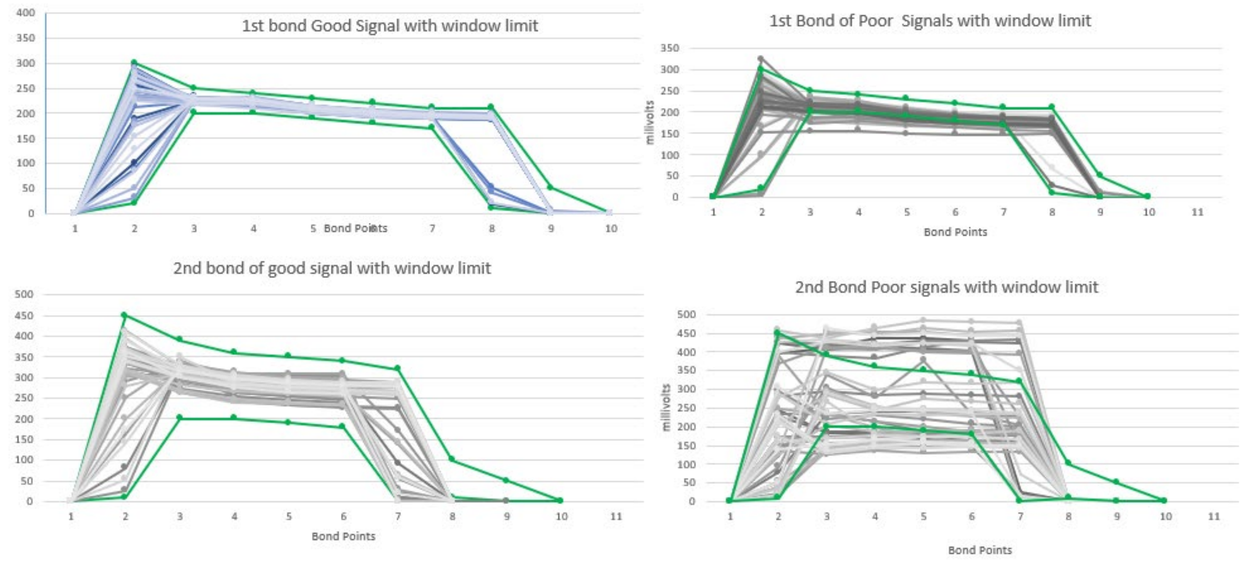


Figure 10. Graphical Presentation of good and poor bond signal with window limit for 1st and 2nd bond.

4.4. Reject Criteria Definition

Figure 11 shows a graphical presentation of the data taken for the pull tests and break mode readings for all the samples of known good and known poor wirebond signals. All signals above the UCL are wedge-off upon wirebond and all signals below the LCL, less than 500 grams force. Both these conditions exhibit wedge-off which are criteria for rejection. The graph shows that wirebond points 3, 4, 5 ,6 are determined as critical points, any signal point that falls outside the defined window per point are considered defective in wirebond quality. This will give a trigger signal to the wirebonder to stop processing.

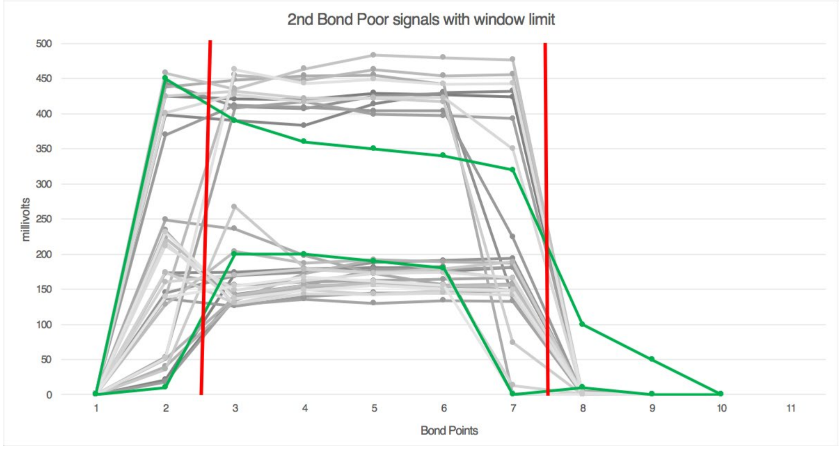


Figure 11. Wire pull test reading and break mode for all samples from good and poor bond signal.

5. Conclusion

Based on the result of evaluation, using the Arduino-based microcontroller and raspberry pi system can acquire signal from existing wirebond and monitor the ultrasonic generator signal on each wirebond. All signals acquired can be determined to be good or poor. The system can detect if the machine needs to stop operations before further wirebonds lead to more device rejection. It is recommended to validate the obtained system on 1000 wire bond unit for further study and analysis. It is also recommended to feed the acquired data in machine learning algorithm for prediction analysis.

Table 1. Wire pull test reading and break mode for all samples from good and poor bond signal.

Known Good Bond Signal Samples			
Minimum Wirepull Reading Requirement: 350 gram force			
Unit Sample	Wire Number	Wirepull Reading	Break Mode
1	1	958	Span Break
	2	964	Span Break
	3	996	Span Break
	4	921	Span Break
2	1	958	Span Break
	2	964	Span Break
	3	923	Span Break
	4	971	Span Break
3	1	933	Span Break
	2	983	Span Break
	3	931	Span Break
	4	909	Span Break
4	1	1000	Span Break
	2	970	Span Break
	3	940	Span Break
	4	991	Span Break
5	1	961	Span Break
	2	937	Span Break
	3	938	Span Break
	4	955	Span Break
6	1	932	Span Break
	2	922	Span Break
	3	914	Span Break
	4	978	Span Break
7	1	929	Span Break
	2	928	Span Break
	3	923	Span Break
	4	965	Span Break
8	1	941	Span Break
	2	987	Span Break
	3	923	Span Break
	4	944	Span Break
9	1	990	Span Break
	2	988	Span Break
	3	907	Span Break
	4	939	Span Break
10	1	911	Span Break
	2	958	Span Break
	3	945	Span Break
	4	914	Span Break
min		907	
max		1000	
average		948.15	
std dev		27.74159006	

Known Poor Bond Signal Samples			
Minimum Wirepull Reading Requirement: 350 gram force			
Unit Sample	Wire Number	Wirepull Reading	Break Mode
1	1	593	Wedge-off
	2	336	Wedge-off
	3	395	Wedge-off
	4	0	Wedge-off
2	1	473	Wedge-off
	2	484	Wedge-off
	3	485	Wedge-off
	4	839	Wedge-off
3	1	0	Wedge-off
	2	438	Wedge-off
	3	801	Wedge-off
	4	0	Wedge-off
4	1	0	Wedge-off
	2	0	Wedge-off
	3	0	Wedge-off
	4	0	Wedge-off
5	1	0	Wedge-off
	2	0	Wedge-off
	3	0	Wedge-off
	4	0	Wedge-off
6	1	437	Wedge-off
	2	820	Wedge-off
	3	441	Wedge-off
	4	895	Wedge-off
7	1	854	Wedge-off
	2	876	Wedge-off
	3	856	Wedge-off
	4	857	Wedge-off
8	1	854	Wedge-off
	2	876	Wedge-off
	3	856	Wedge-off
	4	857	Wedge-off
9	1	0	Wedge-off
	2	0	Wedge-off
	3	0	Wedge-off
	4	0	Wedge-off
10	1	0	Wedge-off
	2	412	Wedge-off
	3	0	Wedge-off
	4	0	Wedge-off
min		0	
max		895	
average		367.525	
std dev		383.6478162	

Acknowledgements

The authors would like to thank Fastech Synergy Philippines Inc and First Asia Institute of Technology and Humanities (FAITH) for their continuous support on this research.

References

Semiconductor and Electronics Industries in the Philippines, Inc., About the Industry Available: http://www.seipi.org.ph/profile/about-the-industry/

IVF, The Swedish Institute of Production Engineering Research, The Nordic Electronics Packaging Guidelines, Chapter A, Available : http://extra.ivf.se/ngl/

S.W. Or, et al (1996) Sensors for automatic process control of wirebonding, Hongkong Polytechnic University September 1996

Shuichi, Ishida et al (2016), Improvement of Sampling Inspection for Wirebonding Using Taming and Thin Film AE Sensor, Advanced Manufacturing Research Institute, National Institute of Advanced Industrial Science and Technology, Saga Japan, December 20, 2016

Koh, Jeremy et al (2009), "Closed Loop" Study for Wirebonding Process, SPT Asia Pte Ltd, February 12, 2009

Rogado, Alex., Wirebond Bond Process Control and Monitoring System, 8th International Conferecne on Electronic Materials and Packaging, December 13, 2006

Biographies

Reymart Rio Haldos is currently assigned as Sr. Package Development Engineer in Fastech Advanced Assembly Inc. one of the sub-con manufacturing assembly, test and tune, product development and drop shipment services for OEM semiconductor and RF / microwave manufacturers in Europe, US and Asia. With his more than 8 years of experience in Semiconductor company give him a lot of exposure in various manufacturing technology like Wafer Dicing, Die Attach, Wire bond interconnections, Encapsulation, up to Electrical and Reliability Testing. He has authored several technical papers and presented in annual Association of Semiconductor and Electronics Manufacturing Engineers of the Philippines (ASEMEP) National Technical Symposium. He has conducted his 5-year ECE studies at Polytechnic University of the Philippines- Sta. Rosa Campus. He is currently taking his Master Studies in Ateneo de Manila University.

Patricia Angela Reyes-Abu is an Assistant Professor at the Department of Information Systems and Computer Science at the Ateneo de Manila University. She has authored several ISI/SCOPUS/SCI-indexed publications with current research focus on image processing and computer vision with biomedical and agricultural applications, and IoT systems and applications. Dr. Abu received her M.S. degree in Electronics Engineering Major in Microelectronics from Chung Yuan Christian University, Chung-Li, Taiwan in 2009. She received both her Ph.D. in Computer Science and B.S. in Electronics and Communications Engineering degrees from the Ateneo de Manila University, Philippines in 2007 and 2012, respectively.

Carlos Matti Oppus is currently the Director of the Ateneo Innovation Center, Ateneo de Manila University. He is concurrently an Assistant Professor in Ateneo de Manila University. He is a member of various professional organizations like IEEE and Physics Association. He has authored several ISI/SCOPUS-indexed publications in the area of Machine Learning, FPGA, Robotics and Wireless Sensor Network. He has received several grants from the Department of Science and Technology as well as from Ateneo de Manila University. He has a Computer Engineering and Physics degrees allowing him to do research in a variety of fields. Since, 2009 to present, he is a recipient of the Ateneo de Manila University Loyola Schools Research/Publication Awards.

Rosula San Jose-Reyes is an Associate Professor at the Department of Electronics, Computer, and Communications Engineering, School of Science and Engineering, Ateneo de Manila University. She holds a Bachelor of Science degree in Electronics and Communications Engineering from the University of Santo Tomas, a Masters of Engineering Education major in Computer Engineering degree from the University of the Philippines, and a Doctor of Philosophy in Education degree from the University of Santo Tomas. She is a recipient of the Leaders in Innovation Fellow from the joint Royal Academy of Engineering in the United Kingdom and the Asian Institute of Management in the Philippines under of the Newton Program. Her research involvement in Biomedical Device Instrumentation and Robotics produced several ISI/SCOPUS-indexed publications. She has a long-time research collaborations with the International Centre for Theoretical Physics and Scuola Superiore Sant'Ana both in Italy, Chung Yuan Christian University in Taiwan, and Institut Catholique D"Arts et Metier in France. She is an ASEAN University assessor and three-time President of the Institute of Electronics Engineers of the Philippines. She is a recipient of several awards in the Engineering profession, and Science and Technology from various award-giving bodies.