# The Alternate Arm Converter (AAC) "Extended-Overlap" Mode: AC Faults

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*Abstract*—This paper presents AC fault ride-through strategies for the "extended-overlap" operating mode of the Alternate Arm Converter (AAC), which is a type of modular multilevel Voltage Source Converter (VSC) that has been proposed for HVDC transmission applications. The AAC offers several benefits over the Half-Bridge (HB) Modular Multilevel Converter (MMC), such as requiring fewer Sub-Modules (SMs) with a smaller capacitance and providing DC fault ride-through capability. Novel symmetrical and asymmetrical AC fault ride-through strategies are described and these strategies are experimentally validated by using a Small Scale Prototype (SSP).

*Index Terms*—HVDC converters, HVDC transmission, Multi-level systems, Power conversion.

## I. Introduction

THE Modular Multilevel Converter (MMC) [1] is presently the preferred VSC topology for commercial HVDC installations [2] due to the Half-Bridge (HB) Sub-Module (SM) variant having an efficiency of $\approx$ 99% [3]. Additionally, this converter generates high-fidelity AC side voltages, thereby easing filtering requirements [1], [4], [5]. In each converter arm, hundreds of SMs are series-connected to form a valve and the charged capacitors in each SM are switched into the circuit with positive polarity or are switched out of the circuit to generate a multilevel voltage. Each arm also comprises an inductor, which has the main purpose of limiting the fault current gradient and the corresponding current peak during DC side faults [6], before the relatively slow-acting AC side mechanical breaker is opened to disconnect the converter from the AC network, thereby breaking the fault current [7], [8]. Normally, these inductors do not cause voltage spikes during operation because the arm currents flow continuously [5].

The Full-Bridge (FB) SM variant of the MMC [9] can stay connected to the AC network and operate as a STATCOM during DC side faults because the valves can now generate positive and negative voltages, thereby allowing the AC side voltage to be opposed throughout a fundamental period so that uncontrolled diode conduction can be prevented. However, twice as many semiconductor devices are required [9] and the converter conduction losses double during normal operation

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[10]. In order to provide DC fault ride-through capability with fewer semiconductor devices, alternative SM arrangements, such as the "double-clamp" SM, have been proposed [11]. Alternatively, the "hybrid" MMC typically uses an equal number of FB and HB SMs so that DC fault ride-through is provided with 25% fewer semiconductor devices than the FB-MMC [12].

The Alternate Arm Converter (AAC) is another type of modular multilevel VSC that has been proposed for HVDC transmission applications [13], [14]. The AAC offers several benefits over the HB-MMC, such as comprising typically 30–40% fewer SMs [15], requiring approximately half the SM capacitance to yield a given SM capacitor voltage ripple [16], [17], and providing DC fault ride-through capability [18], [19]. In addition to each arm comprising a valve (formed by FB SMs) and an inductor, there is also a series-connection of self-commutated semiconductor devices with anti-parallel diodes, termed a Director Switch (DS). A strategy is required to balance the voltages across the series-connected devices within a DS [20]. The two DSs in each converter phase-leg alternate conduction of the AC side current so that this current is rectified on the DC side. There is a handover period, termed "overlap", twice per fundamental period, where a controlled circulating current flows to enable SM energy management [21], [22]. When an arm is conducting the AC side current because its DS is closed, the corresponding valve is generating the multilevel AC side voltage for this phase. The valve in the other arm of the corresponding phase-leg generates a voltage which aims to ensure the voltage across its DS remains positive so that the anti-parallel diodes remain reversed biased.

A comparison of the HB-MMC, FB-MMC and AAC attributes is shown in Table I [1], [9], [13]–[19]. The nominal SM capacitor voltage is equal for all converters. The number of SMs, SM capacitance and semiconductors are normalised to those required for a HB-MMC.

The original AAC operation mode is termed "short-overlap", where the nominal "overlap" angular duration is in the region of 15–18° [21], [23]. In this operation mode, the DC current contains a characteristic ripple at multiples of six times the fundamental frequency, which can be filtered by using a bulky passive low-pass filter [14], [21]. Alternatively, the electrical characteristics of the HVDC link along with DC link capacitance and additional damping resistance can provide the required filtering [23].

This paper concerns the more recently disclosed "extended-overlap" mode [24], [25], where the nominal "overlap" angular duration is 60° [12]. This operating mode causes the AC currents sum to zero at a point within the converter and makes

TABLE I
COMPARISON OF MODULAR MULTILEVEL VSCs

|  | HB-MMC | FB-MMC | AAC |
|---|---|---|---|
| SM type | HB | FB | FB |
| Normalised no. of SMs | 1 | 1 | 0.6–0.7 |
| Normalised SM capacitance | 1 | 1 | $\approx 0.5$ |
| DSs required | No | No | Yes |
| Normalised no. of semiconductors | 1 | 2 | $\approx 1.5$ |
| DC fault ride-through capability | No | Yes | Yes |

a conduction path for the DC current through a phase-leg always available and therefore a ripple free DC current can be obtained [12]; this attribute is termed "active filtering" [24], [26]. As the DC current no longer has a characteristic ripple, a bulky passive filter is not required and therefore the related drawbacks of the AAC described in [27] are resolved. Additionally, as the DC side current is no longer coupled to the rectified AC side currents and as the "overlap" duration is longer, the AAC can operate more easily away from the "sweet-spot", where there is a natural AC and DC side power balance [14], [21], without requiring unrealisable circulating currents [12]. When operating with only a fundamental phase-neutral converter voltage component, a longer "overlap" duration increases the required valve voltage rating. However, by operating in the "extended-overlap" mode with an additional Zero Phase Sequence (ZPS) converter voltage component, which cancels at the grid-side due to the transformer arrangement, the zero-crossing regions of the converter voltages can be "flattened" such that the required valve voltage rating is comparable to that for "short-overlap" operation, at the expense of increasing the required DS voltage rating by $\approx 60\%$ [15]. Nonetheless, a DS voltage rating increase does not increase the cost or volume of the converter as much as an equal increase in the valve voltage rating, mainly due to not requiring additional costly and bulky SM capacitors [13], [28].

By using the Small Scale Prototype (SSP) described in [29], AAC DC fault ride-through strategies described and validated by simulation in [18], [19], termed STATCOM mode 'A' (where the mean DC side current equals zero) and modes 'B1' and 'B2' (where the instantaneous DC side current equals zero), are experimentally validated for the "extended-overlap" mode in [29].

Converters in HVDC applications are required by regulations such as [30] to remain connected to the AC network during periods of depressed voltage at the Point of Common Coupling (PCC) caused by AC faults, which vary in typical duration between hundreds of milliseconds for severe faults to a few seconds for minor faults. Depending on operator requirements and fault severity, the converters may be required to exchange reactive power with the AC network to provide AC voltage support during faults and continue to transfer active power, albeit potentially at a reduced level due to converter limits. After the fault is removed, pre-fault active power should be restored. Voltage or current protection should not be triggered at any point throughout the entire sequence.

A consideration for modular multilevel VSCs during faults is to aim to ensure that the capacitor voltage of each SM still remains within normal operation limits so that the converter continues to operate properly and safely. MMC control strategies for SM capacitor voltage/energy management [31]–[34] and AC fault ride-through [35]–[37] are not directly applicable to the AAC because this topology is time-varying over a fundamental period due to the varying DS combinations [23], [38], unlike the MMC topology, which is time-invariant when the valves are approximated as controllable voltage sources [39]. AAC "short-overlap" mode control strategies for SM capacitor voltage management [22], [40], [41] and AC fault ride-through [42] cannot be directly applied to the "extended-overlap" mode due to the previously described operational differences between these two modes. Therefore, in this paper, novel AC fault ride-though strategies for the AAC "extended-overlap" mode are described and then experimentally validated by using the SSP.

The remainder of this paper is organised as follows. In Section II, the AAC "extended-overlap" mode is described in more detail. A symmetrical AC fault ride-through strategy is presented in Section III. In Section IV, considerations for operation during asymmetrical AC faults are introduced and ride-through strategies for single-phase and line-line faults are presented in Sections V and VI, respectively. In Section VII, the described ride-through strategies are experimentally validated by using the SSP. Finally, conclusions are drawn in Section VIII.

## II. CONVERTER TOPOLOGY AND OPERATION

The AAC is illustrated in Fig. 1, where: $x \in \{a, b, c\}$ is the phase identifier; $v_{LWx}$, $i_{LWx}$, $v_{VWx}$ and $i_{VWx}$ are the Line Winding (LW) and Valve Winding (VW) voltages and currents; $v_{VUx}$, $v_{VLx}$, $i_{VUx}$ and $i_{VLx}$ are the upper and lower valve voltages and currents; and $v_{DSUx}$ and $v_{DSLx}$ are the upper and lower DS voltages. Each arm comprises a FB SM valve, an inductor, and a DS, which is formed by series-connected IGBTs and anti-parallel diodes. The AC side is a three-phase three-wire system and the converter is interfaced to the AC network by using a star-delta transformer with a LW to VW turns ratio of $1 : N_{VW}$. This transformer winding arrangement is typical for HVDC-VSC schemes [43] and provides cancellation of the ZPS VW voltage on the LW side, during all conditions, so that distortion is not introduced to the AC side currents. Although other winding arrangements, which provide this cancellation, are also feasible. The positive and negative pole-ground DC voltages are denoted by $V_{DCp}$ and $V_{DCn}$, and the positive and negative pole DC currents by $I_{DCp}$ and $I_{DCn}$. All figures and values in this paper are approximate and not definite in nature.

The AAC "extended-overlap" mode is described in detail in [12]. The operating principle of this mode is illustrated in Figs. 2 and 3 by showing nominal ideal waveforms of the phase 'a' DS gate signals and system voltages (see Section II-A) and the three-phase system currents, for an example case where the VW voltage and current are in-phase ($\phi = 0$). The ideal waveforms shown in this paper (Figs. 2–3 and 5–29) are generated by MATLAB® from equations.
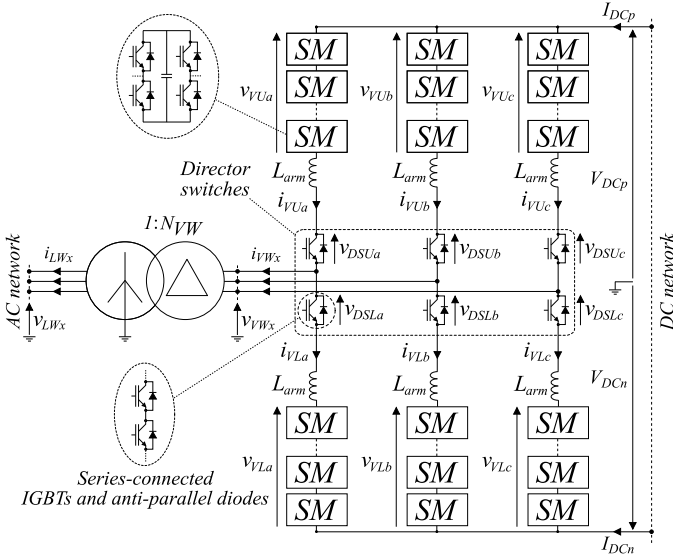
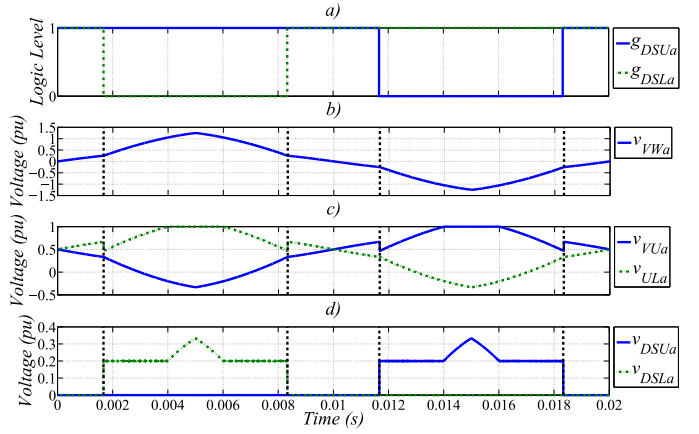Fig. 1.  Alternate Arm Converter (AAC) schematic



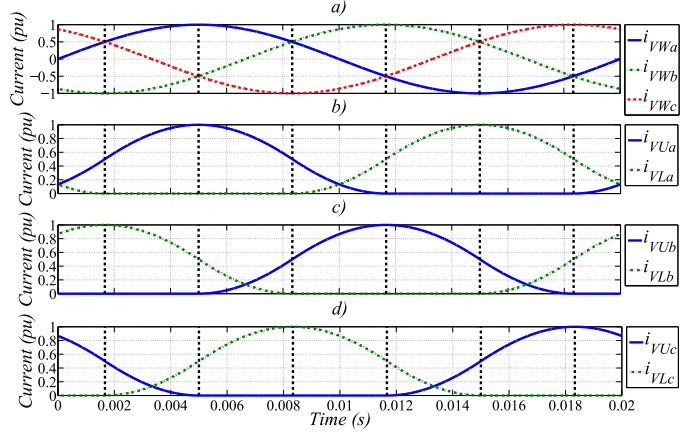Fig. 2.  Nominal phase 'a' a) DS gate signals, b) VW voltage, c) valve voltages, and d) DS voltages



Fig. 3.  Nominal a) three-phase VW currents, b) phase 'a' valve currents, c) phase 'b' valve currents, and d) phase 'c' valve currents

Taking phase-leg 'a' as an example, when only the upper arm DS is closed [intervals where $g_{DSUa} = 1$ and $g_{DSLa} = 0$ in Fig. 2a)], the upper valve is solely responsible for generating a positive VW voltage, as seen in Figs. 2b) and c), and the upper arm conducts the VW current, as seen in Figs. 3a) and b). The lower valve generates the voltage shown in Fig. 2c), which aims to ensure that the lower arm DS anti-parallel diodes remain reversed biased by having a positive voltage across this DS, as seen in Fig. 2d). Conversely, when only the lower arm DS is closed [intervals where $g_{DSUa} = 0$ and $g_{DSLa} = 1$ in Fig. 2a)], the lower valve is responsible for generating a negative VW voltage, as seen in Figs. 2b) and c), and the lower arm conducts the inverse of the VW current, as seen in Figs. 3a) and b). The upper valve now generates the voltage shown in Fig. 2c), which aims to ensure that the upper arm DS anti-parallel diodes remain reversed biased by having a positive voltage across this DS, as seen in Fig. 2d).

When the upper and lower arm DSs are both closed [intervals where $g_{DSUa} = 1$ and $g_{DSLa} = 1$ in Fig. 2a)], this is termed "overlap", which is a key terminology for the AAC. "Overlap" periods occur for a nominal angular duration of $60°$ and are centred around the zero-crossings of the VW voltage, as seen in Fig. 2b). In Figs. 2 and 3, the start and end of "overlap" periods for phase 'a' and for the three phases, respectively, are indicated by the vertical dashed lines. During "overlap", both valves are responsible for generating the VW voltage, as seen in Figs. 2b) and c). The upper arm conducts half the VW current and the lower arm conducts the inverse of half the VW current. Additionally, both arms conduct the current component relating to the DC side power and, although not shown in the valve currents of Fig. 3 for the sake of clarity, smaller current components relating to SM capacitor energy regulation denoted by $I_{circ_x}$ (see Section II-B). Furthermore, both arms conduct current components relating to "active filtering" so that an ideally ripple free DC current can be obtained [24], [26]. When a DS is required to open at the end of an "overlap" period, "zero-current" turn-off is achieved by actually opening the DS when its anti-parallel diodes are conducting [44] (not shown in the valve currents of Fig. 3 for the sake of clarity).

Taking as an example the $60°$ interval in Fig. 3 where phase-leg 'a' is in "overlap", phase-leg 'b' has only its upper DS closed and phase-leg 'c' has only its lower DS closed ($0.0083 \leq t < 0.0117$), the valve currents are defined by (1). Similar valve current expressions can be found for the remaining five $60°$ intervals of a fundamental period [12].

$$i_{VUa}(t) = \frac{1}{2}i_{VWa}(t) + I_{DC} +$$
$$I_{circ_a}(t) + \frac{1}{2}i_{VWa}(t) + i_{VWc}(t) \tag{1a}$$

$$i_{VUb}(t) = i_{VWb}(t) \tag{1b}$$

$$i_{VUc}(t) = 0 \tag{1c}$$

$$i_{VLa}(t) = -\frac{1}{2}i_{VWa}(t) + I_{DC} +$$
$$I_{circ_a}(t) - \left(\frac{1}{2}i_{VWa}(t) + i_{VWb}(t)\right) \tag{1d}$$

$$i_{VLb}(t) = 0 \tag{1e}$$

$$i_{VLc}(t) = -i_{VWc}(t) \tag{1f}$$

Throughout a fundamental period, the valve currents of the three phases plotted in Figs. 3b)–d) obtain the sinusoidal VW currents shown in Fig. 3a) and defined by (2), where $x \in \{a,b,c\} \equiv k \in \{0,1,2\}$. As the same circulating current is applied to both arms of the phase-leg that is in "overlap", the circulating currents do not appear in the VW currents. A ripple free DC current, defined by (3), is obtained due to the VW current components in the arms summing to zero in both DC pole currents and the circulating currents equalling zero in steady-state (see Section II-B).

$$i_{VWx}(t) = \hat{I}_{VWx} \sin (\omega t - 2k\pi/3 + \phi_x)$$
$$= i_{VUx}(t) - i_{VLx}(t) \qquad (2)$$
$$I_{DC} = I_{DCp} = i_{VUa}(t) + i_{VUb}(t) + i_{VUc}(t)$$
$$= -I_{DCn} = i_{VLa}(t) + i_{VLb}(t) + i_{VLc}(t) \qquad (3)$$

The AAC requires several controllers to regulate the active and reactive power components and each SM capacitor energy to their desired set-points. The control philosophy used in this paper is described in [45]–[48] and is applicable, not only to the MMC, but also to the AAC when modifications are made to the control strategies for SM capacitor energy regulation and AC fault ride-through as well as considering DS operation. This control philosophy is effective when the converter is connected to strong or weak AC systems during symmetrical or asymmetrical conditions, without requiring a Phase-Locked Loop (PLL).

Fig. 4 illustrates the overall control strategy for the AAC, which is summarised here and described further in the following sections. The measured LW voltages, referred to the transformer VW side, are transformed to positive and negative phase sequence components in the $\alpha\beta$ stationary reference frame. A unified power controller independently regulates the measured DC side power (or DC voltage) and the measured reactive power (or AC voltage) to their orders by using PI controllers. The power controller outputs a reference AC side active power, which is trimmed to consider losses (see Section II-B), a reference reactive power and a reference DC current. The reference AC side active and reactive powers along with the referred LW voltages are used to derive the reference VW currents. These references along with the reference DC current and the reference circulating currents related to SM energy management (see Section II-B) are used to derive the reference valve currents. Additionally, in order to facilitate DS "zero-current" turn-off, the corresponding reference valve current is made negative at the end of "overlap" [44]. A Linear Quadratic Regulator (LQR) controller is used to regulate the measured valve currents to their references by generating reference voltages for the valves. The reference valve voltages also include a ZPS component and are offset when the corresponding DS is open to aim to ensure the DS anti-parallel diodes remain reversed biased. The reference valve voltages are synthesised by the SMs by using a level-shifted multilevel modulation scheme [49] and a SM rotation algorithm [31] is applied to each valve as the modulation scheme generates unequal SM duties. The instants at which a DS is required to open or close are derived from the VW voltage angular displacement and the

"overlap" angle, but the IGBTs in the DS are only actually opened when the corresponding measured valve current is negative [44].

*A. Reference Valve Voltages*

Ideal reference valve voltages can be found from the VW voltages required for a given operating condition. The fundamental VW voltages are ideally sinusoidal waveforms and can be defined by (4). A ZPS component is introduced to "flatten" the VW voltage zero-crossing regions so that the valve voltage rating is reduced [15]. The ZPS component is nominally a triangular waveform with a period of a third of a fundamental period and is defined by (5) for $0 \le t < \frac{\Phi_{OVx}}{2\omega}$, where $\Phi_{OVx}$ is the "overlap" angle and $\omega$ is the fundamental angular frequency; similar expressions apply for the remainder of a fundamental period. The same ZPS component is always applied to each phase and therefore this component cancels at the LW due to the transformer arrangement. Given (4) and (5), the VW voltages are defined by (6). The nominal fundamental to ZPS component magnitude ratio is defined by (7) so that the required valve voltage rating is comparable to that of the "short-overlap" mode [15]. By using (4)–(7) with $\Phi_{OVx} = \pi/3$ rad and $\omega = 2\pi50$ rad/s, the phase 'a' VW voltages are plotted in Fig. 5a), when normalised to the nominal fundamental VW voltage magnitude.

$$v_{VWx}^{fund}(t) = \hat{V}_{VWx}^{fund} \sin(\omega t - 2k\pi/3) \qquad (4)$$

$$v_{VW}^{zero}(t) = -\frac{\hat{V}_{VW}^{zero}}{\Phi_{OVx}/2} \omega t, \quad \text{for } 0 \le t < \frac{\Phi_{OVx}}{2\omega} \qquad (5)$$

$$v_{VWx}^{ref}(t) = v_{VWx}^{fund}(t) + v_{VW}^{zero}(t) \qquad (6)$$

$$m_{ratio} = \frac{\hat{V}_{VW}^{zero}}{\hat{V}_{VWx}^{fund}} = \frac{1}{4} \qquad (7)$$

Ideal reference upper and lower valve voltages can be found by neglecting the relatively small arm inductor voltages and by assuming that $V_{DCp} = -V_{DCn} = V_{DC}/2$. When the upper or lower arm DSs are closed ($g_{DSUx} = 1$ or $g_{DSLx} = 1$), the reference valve voltages can be derived from $V_{DC}$ and $v_{VWx}^{ref}$. However, when the upper or lower arm DSs are open ($g_{DSUx} = 0$ or $g_{DSLx} = 0$), an offset of $V_V^{os}$ is also applied to the valve voltages to aim to ensure that the arm DS anti-parallel diodes remain reversed biased. Consequently, the reference upper and lower valve voltages can be defined by (8) and (9), respectively.

$$v_{VUx}^{ref}(t) = \begin{cases} \frac{V_{DC}}{2} - v_{VWx}^{ref}(t), & \text{for } g_{DSUx} = 1 \\ \frac{V_{DC}}{2} - v_{VWx}^{ref}(t) - V_V^{os}, & \text{for } g_{DSUx} = 0 \end{cases} \qquad (8)$$

$$v_{VLx}^{ref}(t) = \begin{cases} \frac{V_{DC}}{2} + v_{VWx}^{ref}(t), & \text{for } g_{DSLx} = 1 \\ \frac{V_{DC}}{2} + v_{VWx}^{ref}(t) - V_V^{os}, & \text{for } g_{DSLx} = 0 \end{cases} \qquad (9)$$

The reference valve voltages are plotted in Fig. 5b) for nominal operation, when normalised to the DC voltage. The offset valve voltage, $V_V^{os}$, is selected to equal $2V_{sm}^{nom}$, where $V_{sm}^{nom}$ is the nominal SM capacitor voltage and is equal to 0.2pu as its base is the DC voltage. The valve voltages are limited to 1pu as this is the SSP valve voltage rating,
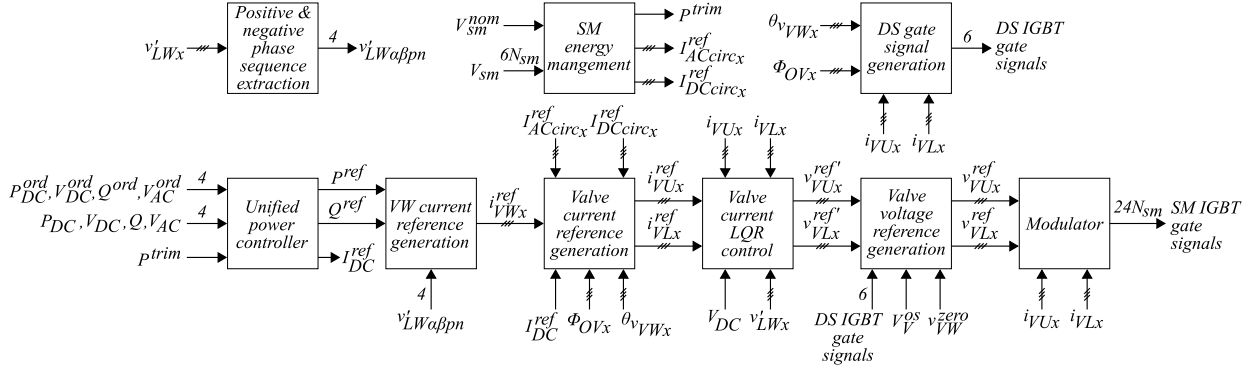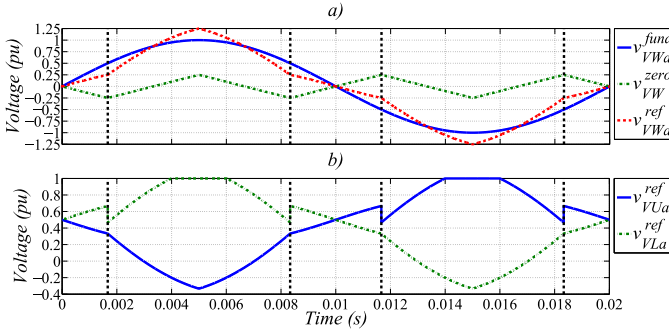
Fig. 4. Overall control strategy



Fig. 5. Nominal a) VW voltages, and b) reference upper and lower valve voltages

but at the end of "overlap", the arms stop conducting the corresponding VW current and therefore the corresponding valve stops generating the VW voltage (see Section IV-B). The valve voltages during "overlap" are of interest for SM capacitor energy management and are plotted in Fig. 6a).

### B. SM Capacitor Energy Management

The SM capacitor energies vary as they are charged or discharged by the valve currents. For sustained converter operation, the mean SM capacitor energies need to be regulated to the nominal value defined by (10), where $C_{sm}$ is the SM capacitance.

$$E_{sm}^{nom} = \frac{1}{2} C_{sm} V_{sm}^{nom2} \qquad (10)$$

The SM capacitor energy controller (SM energy management block in Fig. 4) is based on [45], [46], but has been adapted for the AAC "extended-overlap" mode. The AC side power is trimmed by using a PI controller to account for losses so that the mean of the total SM capacitor energy stored within the converter is regulated to $6N_{sm}E_{sm}^{nom}$, where $N_{sm}$ is the number of SMs per valve. As the converter is operated around the "sweet-spot" [12], the AC side power trim is minimised.

In each phase-leg, the mean of the summed upper and lower valve SM capacitor energies is regulated to $2N_{sm}E_{sm}^{nom}$ by using a PI controller, where the output of the PI controller is denoted by $I_{DCcirc_x}^{ref\prime}$. During steady-state symmetrical operation, these outputs are ideally zero due to the symmetry

between converter phase-legs. The PI controller outputs for the three phase-legs are combined to form the controller actuators, termed the reference DC circulating currents, $I_{DCcirc_x}^{ref}$. The reference DC circulating currents are derived by using (11) so that over half a fundamental period (the duration of three "overlap" periods) they sum to zero in both DC pole currents. In each phase-leg, the reference DC circulating current component interacts with the Voltage Time Area (VTA) of the summed valve voltages during "overlap" to cause a controlled net change in the summed upper and lower valve SM capacitor energy.

$$\begin{bmatrix} I_{DCcirc_a}^{ref}(t) \\ I_{DCcirc_b}^{ref}(t) \\ I_{DCcirc_c}^{ref}(t) \end{bmatrix} = \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} I_{DCcirc_a}^{ref\prime}(t) \\ I_{DCcirc_b}^{ref\prime}(t) \\ I_{DCcirc_c}^{ref\prime}(t) \end{bmatrix} \qquad (11)$$

In each phase-leg, the mean of the difference between the summed upper and summed lower valve SM capacitor energies is regulated to zero by using a PI controller, where the actuator is the reference AC circulating current, $I_{ACcirc_x}^{ref}$, and this component interacts with the VTA of the difference between the valve voltages during "overlap" to cause a controlled net change in the difference between the summed upper and summed lower valve SM capacitor energy. Ideally in steady-state, the reference AC circulating current for each of the three phase-legs is zero due to the converter upper and lower arm symmetry. During transients, the AC circulating current appears instantaneously in the DC pole currents, but for a phase-leg, sums to zero over an "overlap" period because the AC circulating current for the first half of "overlap" is set to the inverse of that for the second half of "overlap".

The reference DC and AC circulating current components form the reference circulating current, $I_{circ_x}^{ref}$, which is defined by (12) and is plotted in Fig. 6b) for an example case where $|I_{DCcirc_x}^{ref}|$ and $|I_{ACcirc_x}^{ref}|$ are both chosen to equal 0.1pu. These values for the reference DC and AC circulating currents are chosen to merely simplify the illustration and description of SM capacitor energy management, they are actually calculated by the SM energy management block shown in Fig. 4 and described in this section.

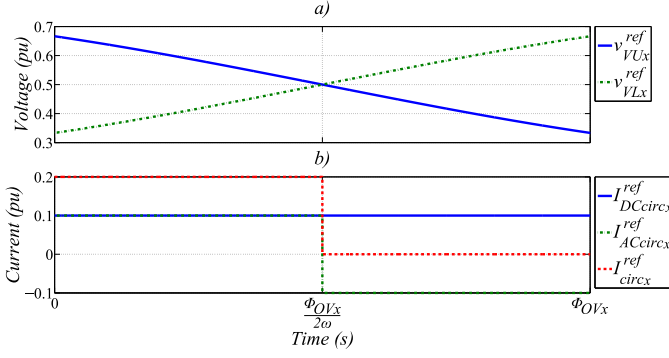$$I_{circ_x}^{ref}(t) = I_{DCcirc_x}^{ref}(t) + I_{ACcirc_x}^{ref}(t) \qquad (12)$$

Fig. 6. a) Reference upper and lower valve voltages, and b) reference DC and AC circulating currents
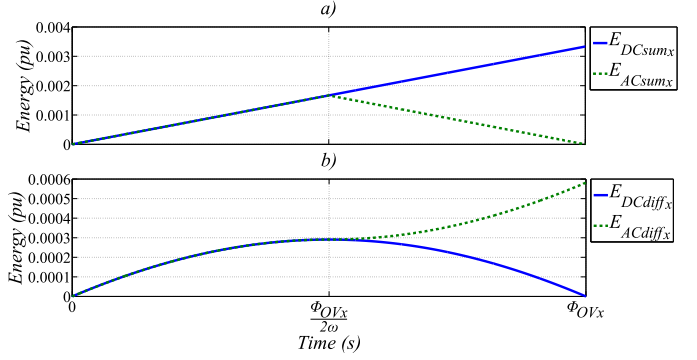


Fig. 7. a) Instantaneous energy of the summed upper and lower valve SM capacitors caused by the DC and AC circulating currents, and b) instantaneous energy of the difference between the summed upper and summed lower valve SM capacitors caused by the DC and AC circulating currents

During "overlap", the four instantaneous energies shown in (13) can be defined. For the voltages and currents shown in Fig. 6, these energies are plotted in Fig. 7, when $\Phi_{OVx} = \pi/3$ rad. The plots show that the DC component affects the net change in energy of the summed upper and lower valve SM capacitors ($\Delta E_{DCsum_x} > 0$) and that the AC component affects the net change in energy of the difference between the summed upper and summed lower valve SM capacitors ($\Delta E_{ACdiff_x} > 0$). Whereas, the AC component does not affect the net change in energy of the summed upper and lower valve SM capacitors ($\Delta E_{ACsum_x} = 0$) and the DC component does not affect the net change in energy of the difference between the summed upper and summed lower valve SM capacitors ($\Delta E_{DCdiff_x} = 0$). Additionally, for this example case, $\Delta E_{DCsum_x}$ can be made negative by using a negative DC circulating current and $\Delta E_{ACdiff_x}$ can be made negative by inverting the AC circulating current.

$$E_{DCsum_x}(t) = \int \overbrace{\left( v_{VUx}^{ref}(t) + v_{VLx}^{ref}(t) \right)}^{V_{DC}} I_{DCcirc_x}^{ref}(t) \, \mathrm{d}t \tag{13a}$$

$$E_{ACsum_x}(t) = \int \left( v_{VUx}^{ref}(t) + v_{VLx}^{ref}(t) \right) I_{ACcirc_x}^{ref}(t) \, \mathrm{d}t \tag{13b}$$

$$E_{DCdiff_x}(t) = \int \overbrace{\left( v_{VUx}^{ref}(t) - v_{VLx}^{ref}(t) \right)}^{-2v_{VWx}^{ref}(t)} I_{DCcirc_x}^{ref}(t) \, \mathrm{d}t \tag{13c}$$

$$E_{ACdiff_x}(t) = \int \left( v_{VUx}^{ref}(t) - v_{VLx}^{ref}(t) \right) I_{ACcirc_x}^{ref}(t) \, \mathrm{d}t \tag{13d}$$

## III. SYMMETRICAL AC FAULT RIDE-THROUGH STRATEGY

As the severity of a symmetrical AC fault increases, the fundamental VW voltage magnitude decreases towards zero. When using a constant fundamental to ZPS component voltage magnitude ratio, such as that defined by (7), the VTA during "overlap" of the difference between the reference upper and lower valve voltages decreases linearly towards zero. As this VTA decreases, the required AC circulating current magnitude has to increase to have the same affect as previously.

Furthermore, if the circulating current limit is reached, the means of the summed SM capacitor voltages in the upper arm and those in the lower arm of a phase-leg begin to diverge from each other during the fault. Therefore, a ride-through strategy for symmetrical AC faults is proposed to aim to ensure that this VTA remains constant, even when the fundamental VW voltage magnitude varies from its nominal value. This is achieved by modifying the calculated ZPS VW voltage, which is input to the valve voltage generation block in Fig. 4. The amount of energy exchanged between the capacitors in the upper arm and those in the lower arm is controlled by varying AC circulating current magnitude, which is calculated by the SM energy management block in Fig. 4 (see Section II-B).

Integrating the difference between the reference upper and lower valve voltages, over the first half of "overlap" ($0 \leq t < \frac{\Phi_{OVx}}{2\omega}$ in Fig. 6), yields the VTA defined by (14), where the phase identifier has been omitted due to symmetrical operation. As the converter has upper and lower arm symmetry, (15) can be written, where $VTA2$ is found when integrating over the second half of "overlap" ($\frac{\Phi_{OVx}}{2\omega} \leq t < \frac{\Phi_{OVx}}{\omega}$ in Fig. 6). If $m_{ratio}$ is kept constant as $\hat{V}_{VW}^{fund}$ reduces to zero, $VTA$ decreases linearly to zero, as shown in Fig. 8a).

$$VTA1 = \int_0^{\frac{\Phi_{OV}}{2\omega}} \left( v_{VU}^{ref}(t) - v_{VL}^{ref}(t) \right) \mathrm{d}t$$
$$= \frac{\hat{V}_{VW}^{fund}}{2\omega} \left( 8\sin^2(\Phi_{OV}/4) - \Phi_{OV} m_{ratio} \right) \tag{14}$$
$$VTA = VTA1 = |VTA2| \tag{15}$$

The dashed line in Fig. 8a) indicates the nominal case, where $VTA$ is defined by (16). By equating $VTA$ with $VTA_{nom}$ and then solving for $m_{ratio}$, yields (17). As $m_{ratio}$ is a function of $\hat{V}_{VW}^{fund}$ in (17), when $\hat{V}_{VW}^{fund}$ varies from its nominal value, $VTA$ can be maintained constant by compensating with $m_{ratio}$. During symmetrical AC faults, $m_{ratio}$ is flexible because all valves have sufficient available voltage during "overlap" due to a reduction in $\hat{V}_{VW}^{fund}$ on all phases. Equation (17) is plotted in Fig. 8b), where $m_{ratio} = -\infty$
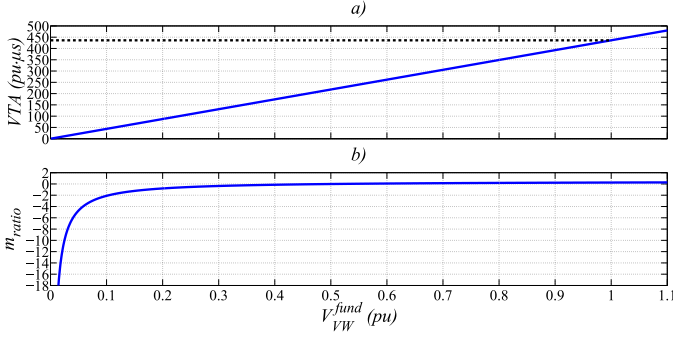
Fig. 8. a) $\hat{V}_{VW}^{fund}$ vs. $VTA$ when $m_{ratio} = 0.25$, and b) $\hat{V}_{VW}^{fund}$ vs. $m_{ratio}$ when $VTA = VTA_{nom}$

TABLE II
SYMMETRICAL AC FAULT CASES

| Fault Severity | $\hat{V}_{VW}^{fund}$ (pu) | $m_{ratio}$ |
|---|---|---|
| Minor | 0.8 | $\approx 0.18$ |
| Major | 0.5 | $\approx -0.01$ |
| Severe | 0.01 | $\approx -25.66$ |

when $\hat{V}_{VW}^{fund} = 0$.

$$VTA_{nom} = \frac{8\sin^2(\pi/12) - \pi/12}{200\pi} \approx 436.24 \text{ pu} \cdot \mu s \quad (16)$$

$$m_{ratio} = \frac{8\sin^2(\Phi_{OV}/4) - 2\omega VTA_{nom}/\hat{V}_{VW}^{fund}}{\Phi_{OV}} \quad (17)$$

Residual VW voltages of 0.8pu, 0.5pu and 0.01pu are used to illustrate representative minor, major and severe AC faults, respectively. These fault cases are given in Table II along with their $m_{ratio}$ values found from (17). The VW voltages for these fault cases are plotted in Figs. 9a), 10a) and 11a), and the corresponding reference valve voltages are plotted in Figs. 9b), 10b) and 11b), respectively.

Regardless of the chosen transformer winding arrangement, the three-phase VW voltages are always displaced by 120° during symmetrical AC faults (unlike asymmetrical AC faults described in Section IV). Therefore, this symmetrical AC fault ride-through strategy directly applies to other applicable winding arrangements.

Power losses when using the symmetrical AC fault ride-through strategy, and when using the ride-through strategies
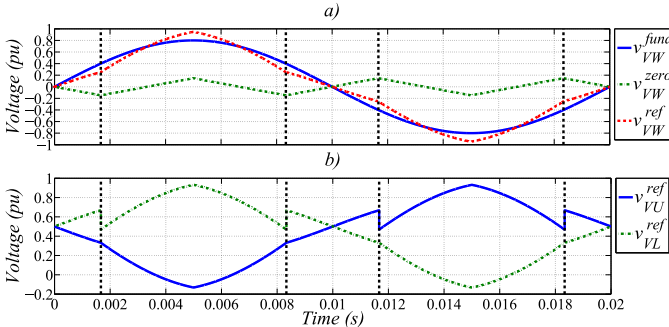


Fig. 9. a) VW voltages, and b) reference upper and lower valve voltages for a 0.8pu residual VW voltage
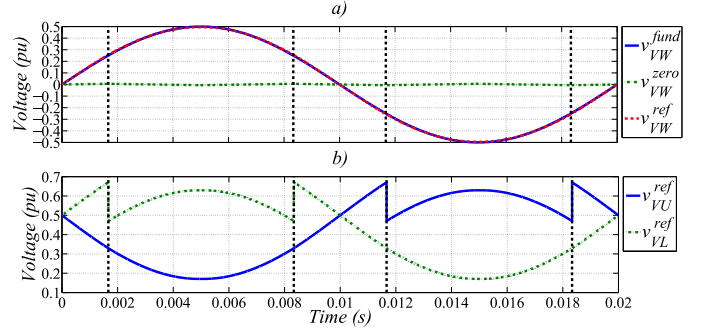


Fig. 10. a) VW voltages, and b) reference upper and lower valve voltages for a 0.5pu residual VW voltage
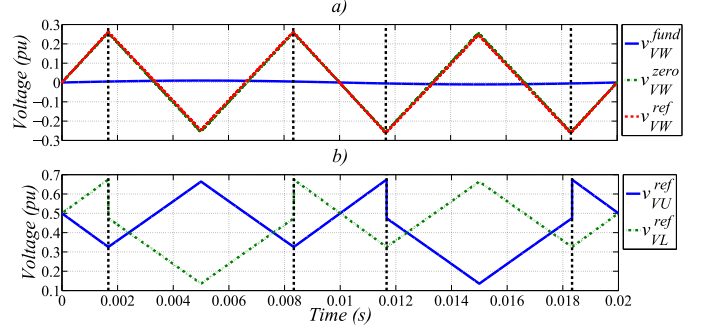


Fig. 11. a) VW voltages, and b) reference upper and lower valve voltages for a 0.01pu residual VW voltage

for single-phase and line-line AC faults described in Sections V and VI, respectively, are not considered in this paper. This is reasonable because losses for HVDC schemes are calculated for normal operation during steady-state [50], [51], not during AC faults, which only occur for between hundreds of milliseconds and a few seconds, depending on the fault severity, otherwise the converter is allowed to be disconnected from the AC network [30].

### A. Further Assessment Criteria

The range of symmetrical AC faults with residual voltages down to 0pu causes the largest change in the three-phase VW voltage vector magnitude, when compared to asymmetrical AC faults, and contains the worst-case fault (a three-phase to ground fault). Therefore, the symmetrical AC fault ride-through strategy is further assessed in terms of peak and RMS valve currents, and peak-peak valve energy deviation.

An exemplar active and reactive power operating envelope for VW voltages down to 0pu is derived. Given the VW voltage and current conventions of Fig. 1, positive active power indicates that the converter is inverting and positive reactive power indicates that current is lagging voltage to provide AC voltage support. The envelope is based on the following constraints: the maximum VW current magnitude occurs at rated active and reactive power ($P = 1$pu and $Q = 0.4$pu) with an VW voltage magnitude of 0.9pu; reactive power is prioritised over active power when the VW voltage magnitude is $< 0.9$pu; and active power is zero when the residual VW voltage magnitude is $\leq 0.5$pu [30], [52]. In Table III, the

TABLE III
EXEMPLAR ACTIVE AND REACTIVE POWER OPERATING ENVELOPE FOR
THE SYMMETRICAL AC FAULT RIDE-THROUGH STRATEGY

| $\hat{V}_{VW}^{fund}$ (pu) | $\hat{I}_{VW}$ (pu) | $\phi$ (°) | $P$ (pu) | $Q$ (pu) |
|---|---|---|---|---|
| 1 | 1 | −21.80 | 1 | 0.4 |
| 0.9 | 1.11 | −21.80 | 1 | 0.4 |
| 0.8 | 1.11 | −24.70 | 0.87 | 0.4 |
| 0.7 | 1.11 | −28.52 | 0.74 | 0.4 |
| 0.6 | 1.11 | −33.85 | 0.60 | 0.4 |
| 0.5 | 0.74 | −90 | 0 | 0.4 |
| 0.4 | 0.93 | −90 | 0 | 0.4 |
| 0.3 | 1.11 | −90 | 0 | 0.36 |
| 0.2 | 1.11 | −90 | 0 | 0.24 |
| 0.1 | 1.11 | −90 | 0 | 0.12 |
| 0 | 1.11 | −90 | 0 | 0 |

TABLE IV
ASSESSMENT CRITERIA OF THE SYMMETRICAL AC FAULT
RIDE-THROUGH STRATEGY

| $\hat{V}_{VW}^{fund}$ (pu) | $\hat{I}_{VU}$ (pu) | $\tilde{I}_{VU}$ (pu) | $\Delta E_{VUpk\text{-}pk}$ (pu) |
|---|---|---|---|
| 1 | 1 | 0.4952 | 0.000681 |
| 0.9 | 1.11 | 0.5422 | 0.000629 |
| 0.8 | 1.11 | 0.5387 | 0.000607 |
| 0.7 | 1.11 | 0.5403 | 0.000761 |
| 0.6 | 1.11 | 0.5446 | 0.001016 |
| 0.5 | 0.64 | 0.3284 | 0.000822 |
| 0.4 | 0.80 | 0.4105 | 0.001086 |
| 0.3 | 0.96 | 0.4913 | 0.001369 |
| 0.2 | 0.96 | 0.4913 | 0.001439 |
| 0.1 | 0.96 | 0.4913 | 0.001509 |
| 0 | 0.96 | 0.4913 | 0.001578 |
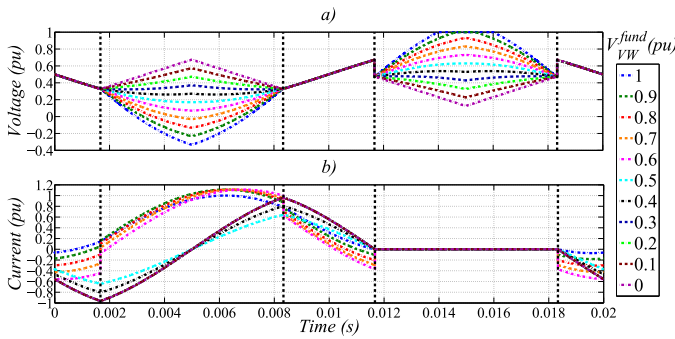


Fig. 12. Upper valve a) voltage and b) current for the VW voltage magnitude range
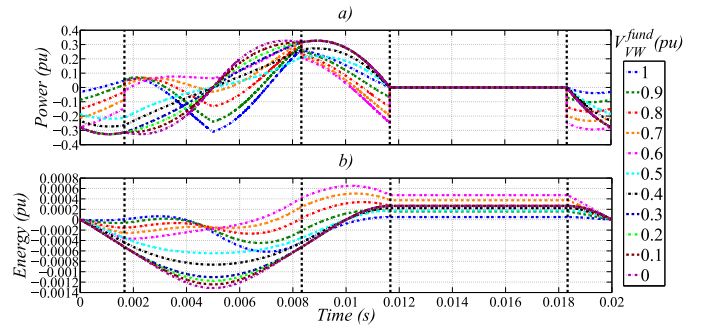


Fig. 13. Upper valve a) power and b) energy deviation for the VW voltage magnitude range

VW current magnitude, phase angle between VW current and voltage, active power and reactive power are shown for the VW voltage magnitude range.

Due the converter upper and lower arm symmetry, only the upper arm is considered in the following analysis. By using (4)–(6), (8) and (17), the upper valve voltages, across the VW voltage magnitude range, are plotted in Fig. 12a). By using (1a) (and similar expressions for the remaining five 60° intervals of a fundamental period), (2) and Table III, the upper valve currents are plotted in Fig. 12b). The peak and RMS valve currents are shown in Table IV. The largest peak and RMS valve currents occur with a VW voltage magnitude of 0.9pu because rated active and reactive power is maintained.

The upper valve power is found by multiplying together its voltage and current and is plotted in Fig. 13a). This power can be integrated to find the upper valve energy deviation, which is plotted in Fig. 13b). The peak-peak valve energy deviations are shown in Table IV. The largest peak-peak valve energy deviation occurs during the worst-case fault, where this value is 2.3 times that for nominal operation. However, the peak-peak valve energy deviation for a MMC with a residual AC side voltage magnitude of just 0.9pu is already three times that for an AAC [17].

## IV. ASYMMETRICAL AC FAULTS

Determining the propagation of asymmetrical AC faults at the LW through the wye-delta transformer and determining

the maximum valve voltage when an arm is conducting the VW current during nominal operation are both required for developing the asymmetrical AC fault ride-through strategies described in Sections V and VI.

### A. Propagation of Asymmetrical AC Faults through the Wye-Delta Transformer

In Appendix A, the phase-neutral Referred LW (RLW) voltages, which are the LW voltages referred to the transformer VW side, are defined in terms of the phase-neutral LW voltages in (23) so that the propagation through the wye-delta transformer of LW single-phase and line-line AC faults with residual voltages of 0.8pu, 0.5pu and 0pu can be determined, as shown in Tables V and VI. Equivalent results can be found for single-phase and line-line AC faults on the other phases.

If a different transformer winding arrangement is chosen, which does not introduce a phase shift between the LW and RLW voltages (unlike the star-delta arrangement), asymmetrical AC faults on the LW side would not affect the phase angles of the RLW voltages. Therefore, the AC fault ride-through strategies would only have to consider RLW voltages with depressed magnitudes, but with zero phase shift as a result of the fault.

### B. Maximum Valve Voltage during Nominal Operation

The maximum required valve voltage, when an arm is conducting the VW current, occurs at the start and end of

TABLE V
SINGLE-PHASE LW FAULT TRANSFORMER PROPAGATION

| Phase | Wye ($v_{LWx}$) | Delta ($v'_{LWx}$) |
|---|---|---|
| 'a' | $0.8\underline{/0°}$ | $0.902N_{VW}\underline{/-33.67°}$ |
| 'b' | $1\underline{/-120°}$ | $0.902N_{VW}\underline{/-146.33°}$ |
| 'c' | $1\underline{/+120°}$ | $N_{VW}\underline{/+90°}$ |
| 'a' | $0.5\underline{/0°}$ | $0.764N_{VW}\underline{/-40.9°}$ |
| 'b' | $1\underline{/-120°}$ | $0.764N_{VW}\underline{/-139.1°}$ |
| 'c' | $1\underline{/+120°}$ | $N_{VW}\underline{/+90°}$ |
| 'a' | $0\underline{/0°}$ | $N_{VW}/\sqrt{3}\underline{/-60°}$ |
| 'b' | $1\underline{/-120°}$ | $N_{VW}/\sqrt{3}\underline{/-120°}$ |
| 'c' | $1\underline{/+120°}$ | $N_{VW}/\sqrt{3}\underline{/+90°}$ |

TABLE VI
LINE-LINE LW FAULT TRANSFORMER PROPAGATION

| Phase | Wye ($v_{LWx}$) | Delta ($v'_{LWx}$) |
|---|---|---|
| 'a' | $0.8\underline{/0°}$ | $0.902N_{VW}\underline{/-33.67°}$ |
| 'b' | $0.8\underline{/-120°}$ | $0.8N_{VW}\underline{/-150°}$ |
| 'c' | $1\underline{/+120°}$ | $0.902N_{VW}\underline{/+93.67°}$ |
| 'a' | $0.5\underline{/0°}$ | $0.764N_{VW}\underline{/-40.89°}$ |
| 'b' | $0.5\underline{/-120°}$ | $0.5N_{VW}\underline{/-150°}$ |
| 'c' | $1\underline{/+120°}$ | $0.764N_{VW}\underline{/+100.89°}$ |
| 'a' | $0\underline{/0°}$ | $N_{VW}/\sqrt{3}\underline{/-60°}$ |
| 'b' | $0\underline{/-120°}$ | $0\underline{/-150°}$ |
| 'c' | $1\underline{/+120°}$ | $N_{VW}/\sqrt{3}\underline{/+120°}$ |

"overlap", as seen in Fig. 5b). By substituting (4)–(7) into (9) when $g_{DSLx} = 1$, with $\hat{V}_{VWx}^{fund} = 1$pu, $V_{DC} = 1$pu, $\omega t = \Phi_{OVx}/2$ rad and $\Phi_{OVx} = \pi/3$ rad, the maximum valve voltage during nominal operation can be found, as shown in (18). The $2/3$ factor appears in (18) due to the change of base for the fundamental VW voltage magnitude from the nominal fundamental VW voltage magnitude to the DC voltage. The ratio between these two base voltages is defined by "sweet-spot" operation [12].

$$V_{Vmax}^{nom} = \frac{1}{2} + \frac{2}{3}\frac{1}{4} = \frac{2}{3} \qquad (18)$$

## V. SINGLE-PHASE AC FAULT RIDE-THROUGH STRATEGY

The ride-through strategy for LW single-phase faults depends on one phase having a residual LW voltage of $< 0.75$pu or not; the reasoning for this is described in Section V-B. In order to illustrate the strategy, typical steady-state waveforms during phase 'a' residual LW voltages of 0.8pu, 0.5pu and 0pu are shown in Sections V-A, V-B and V-C, respectively. In order to illustrate the strategy, the reference DC circulating currents for phases 'a', 'b' and 'c' are chosen to equal +0.1pu, −0.1pu and 0pu, respectively (these currents sum to zero for the reason described in Section II-B), and the reference AC circulating current magnitudes for all phases are chosen to equal 0.2pu. These values for the reference DC and AC circulating currents are chosen to merely simplify the illustration and description of the strategy, they are actually calculated by the SM energy management block in Fig. 4, which is described in Section II-B. The reference circuiting current, which is the sum of
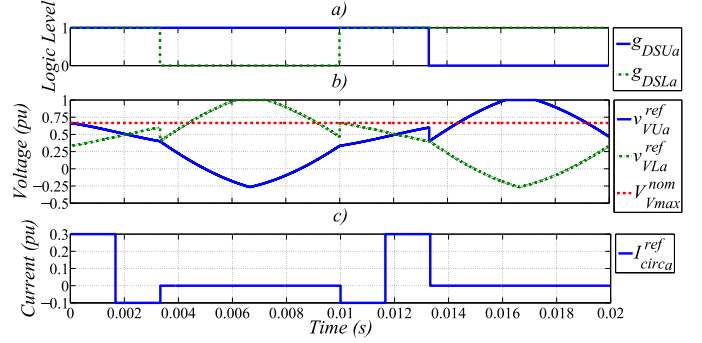
reference DC and AC circulating currents, is set to zero during non-"overlap" periods.

### A. 0.8pu Fault

Fig. 14 shows the phase 'a' DS IGBT gate signals, the reference valve voltages, and the reference circulating current for a phase 'a' 0.8pu residual LW voltage. The corresponding waveforms for phases 'b' and 'c' are shown in Figs. 15 and 16, respectively.

So that the fault does not cause the required valve voltage rating to increase, the phase with the largest (and unchanged) fundamental RLW voltage magnitude, which from Table V is phase 'c' for this case, is used to calculate the ZPS VW



Fig. 14. Phase 'a' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for a phase 'a' 0.8pu residual LW voltage
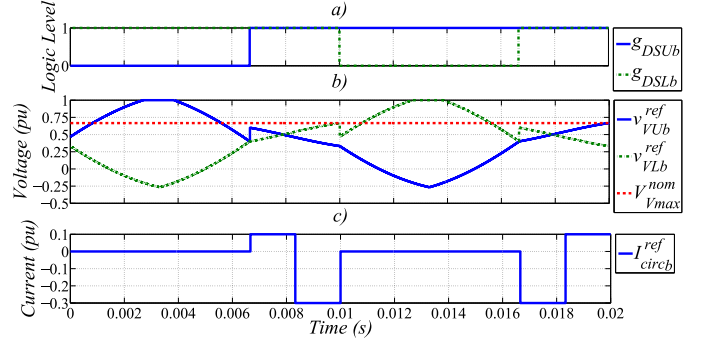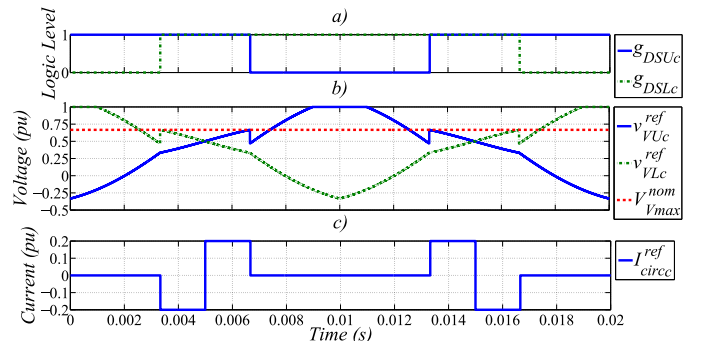


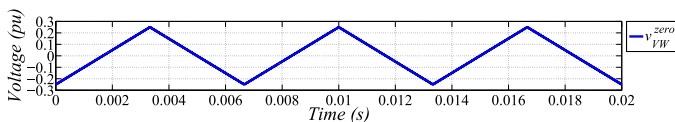Fig. 15. Phase 'b' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for a phase 'a' 0.8pu residual LW voltage



Fig. 16. Phase 'c' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for a phase 'a' 0.8pu residual LW voltage

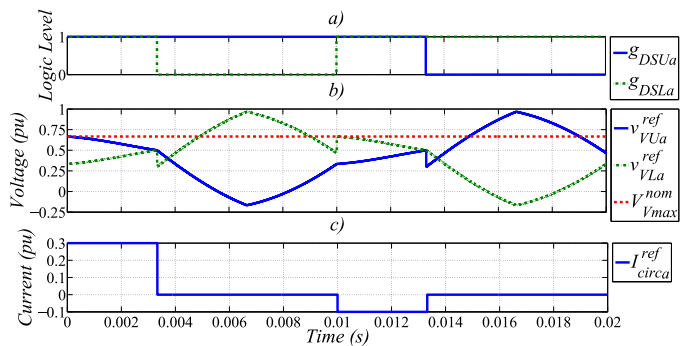Fig. 17. ZPS VW voltage for a phase 'a' 0.8pu residual LW voltage



Fig. 18. Phase 'a' a) DS gate signals, b) reference valve voltages, and c) circulating current for a phase 'a' 0.5pu residual LW voltage
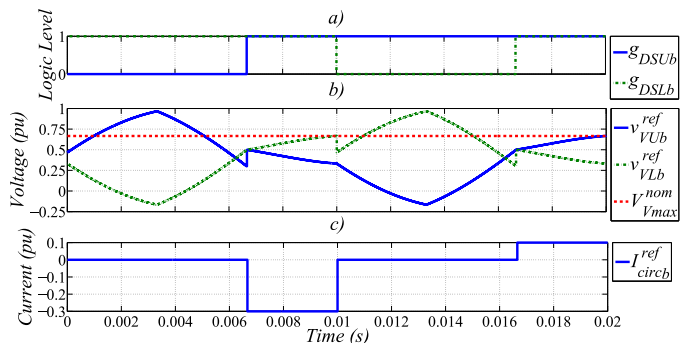


Fig. 19. Phase 'b' a) DS gate signals, b) reference valve voltages, and c) circulating current for a phase 'a' 0.5pu residual LW voltage

magnitude by using (17) and the phase of this component is aligned to the phase 'c' fundamental VW voltage, as shown in Fig. 17. Furthermore, "overlap" angular durations of $60°$ are used for all phases and these periods are aligned relative to the phase 'c' fundamental VW voltage zero-crossings. As for normal "extended-overlap" mode operation, "overlap" angular durations of $60°$ are maintained, and therefore a smooth current component relating to DC side power is obtained. The "overlap" period alignment is achieved by setting the VW voltage angular displacement input for the DS gate signal generation block in Fig. 4 to the phase 'c' VW voltage angular displacement.

The operation of phase 'c' is still the same as the symmetrical fault case described in Section III because the AC circulating current of this phase equals $+0.2$pu when $v_{VUc}^{ref}(t) > v_{VLc}^{ref}(t)$, whereas the AC circulating current equals $-0.2$pu when $v_{VUc}^{ref}(t) < v_{VLc}^{ref}(t)$, as shown in Fig. 16. However, as the successive VW voltage zero-crossings during "overlap" between phase 'a' and phase 'c' and between phase 'c' and phase 'b' are not displaced by $60°$ (see Table V), the AC circulating currents for phases 'a' and 'b' are not aligned with the corresponding reference valve voltage 0.5pu-crossings, as shown in Figs. 14 and 15. Yet, as the amount that the "overlap" periods are offset from the corresponding valve voltage 0.5pu-crossings is relatively small, applying the AC circulating currents during each "overlap" period on phases 'a' and 'b' as in the symmetrical fault case is still effective, although not optimal.

As the summed reference upper and lower valve voltages in each phase still equal 0.5pu during "overlap", the DC circulating currents are still as effective as the symmetrical fault case during this fault, as well as during all other AC faults.

### B. 0.5pu Fault

The phase 'a' and 'b' waveforms for a phase 'a' 0.5pu residual LW voltage are shown in Figs. 18 and 19, respectively. As the magnitude and phase of the phase 'c' RLW voltage is the same as that for a 0.8pu fault (see Table V), the phase 'c' waveforms are the same as those plotted in Fig. 16 and the the ZPS VW voltage is the same as that plotted in Fig. 17, due to the reasons stated in Section V-A.

"Overlap" angular durations of $60°$ are maintained for all phases. The phase 'c' AC circulating current is still aligned with the 0.5pu-crossings of its valve voltages. The 0.5pu-crossings of the phase 'a' and 'b' valve voltages during "overlap" now occur at the start or end of "overlap", as seen in Figs. 18 and 19. Consequently, applying the corresponding AC circulating current during each "overlap" is now ineffective. However, as the VTA during "overlap" of the difference

between the reference upper and lower arm valve voltages are equal in absolute value, but opposite in sign, for two successive "overlap" periods in phase 'a' or in phase 'b', the corresponding AC circulating current can be applied over two successive "overlaps" for phases 'a' and 'b', as seen in Figs. 18 and 19, to be effective. The functionality of the SM energy management block in Fig. 4 is expanded accordingly. During transients, the AC circulating current appears instantaneously in the DC pole currents (see Section II-B), but for phases 'a' and 'b', now sums to zero over two successive "overlap" periods in phase 'a' or in phase 'b', respectively, instead of over one "overlap" period, as previously.

The transition point between the normal AC circulating current operation mode, described in Section II-B and used in Section V-A, and the AC circulating current operation mode, used in this section, is selected to be when one phase has a LW voltage magnitude of 0.75pu. This point is halfway between all phases having a LW voltage magnitude of 1pu, where the VTA of the first and second halves of "overlap" are equal in absolute value but opposite in sign [see Fig. 6a)], and one phase having a LW voltage magnitude of 0.5pu, where the VTA for two successive "overlap" periods of this phase are equal in absolute value but opposite in sign [see Figs. 18b) or 19b)].

### C. 0pu Fault

The phase 'a' and 'b' waveforms for a phase 'a' 0pu residual LW voltage are shown in Figs. 20 and 21, respectively. Due
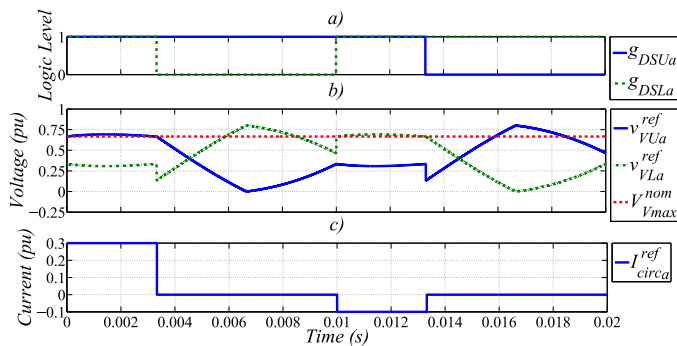
Fig. 20. Phase 'a' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for a phase 'a' 0pu residual LW voltage
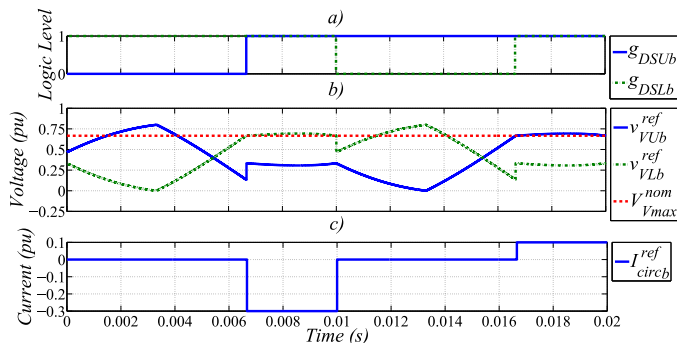


Fig. 21. Phase 'b' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for a phase 'a' 0pu residual LW voltage



Fig. 22. Phase 'a' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for phase 'a' and 'b' 0.8pu residual LW voltages



Fig. 23. Phase 'b' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for phase 'a' and 'b' 0.8pu residual LW voltages

to the reasons stated in Section V-A, the phase 'c' waveforms and the ZPS VW voltage are the same as those plotted in Figs. 16 and 17, respectively.

The ride-through strategy during this fault is same as that described in Section V-B because one phase has a LW voltage between 0.75pu and 0pu. However, during phase 'a' and 'b' "overlap" periods, $V_{Vmax}^{nom}$ (see Section IV-B) is slightly exceeded by the reference valve voltages, as seen in Figs. 20b) and 21b). Yet, the maximum valve voltage ($\approx 0.7$pu) only exceeds $V_{Vmax}^{nom}$ by 5%.

## VI. LINE-LINE AC FAULT RIDE-THROUGH STRATEGY

The ride-through strategy for LW line-line faults is described in this section. In order to simplify the illustration and description of the strategy, the typical waveforms have the same reference circulating currents as those given for single-phase faults in Section V.

### A. 0.8pu Fault

The phase 'a', 'b' and 'c' waveforms for phase 'a' and 'b' 0.8pu residual LW voltages are shown in Figs. 22, 23 and 24, respectively. So that the fault does not cause the required valve voltage rating to increase, the fundamental VW voltage magnitude of the phase which has most recently entered "overlap" is used to calculate the ZPS VW voltage magnitude by using (17) and the phase of this ZPS component is aligned to the corresponding fundamental VW voltage. As the phase 'b' fundamental VW voltage magnitude is the
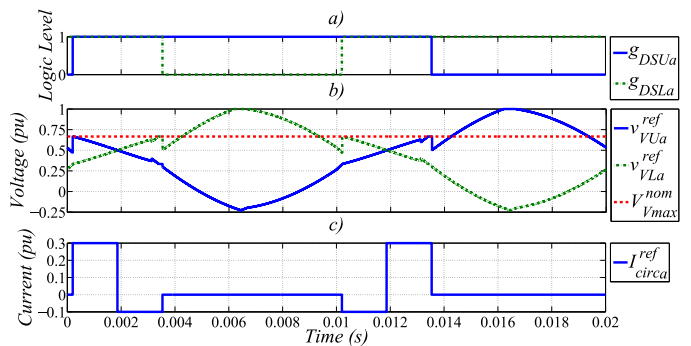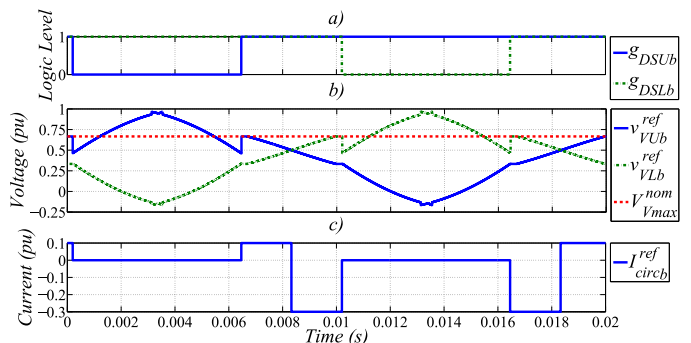
smallest in this case and as the phase of this component is unaffected by the fault (see Table VI), "overlap" periods of $60°$ are used by phases 'a' and 'c' and these periods are aligned to the 0.5pu-crossings of the corresponding reference valve voltages, as seen in Figs. 22 and 24. Whereas, phase 'b' has "overlap" periods during the remaining intervals of a fundamental period, as seen in Fig. 23. As the sum of the "overlap" periods across phases is maintained at $180°$, a smooth current component relating to DC side power is still obtained. The "overlap" period alignment is achieved by setting the VW voltage angular displacement input for the DS gate signal generation block in Fig. 4 to use the phase 'a' and 'c' VW voltage angular displacements for phases 'a' and 'c', respectively, with an "overlap" period input of $60°$, then the phase 'b' "overlap" periods are the remaining intervals. Any net DC circulating current component, caused by operating phase-leg 'b' with an unequal "overlap" period, is compensated for by the AC side power trimming controller (see Section II-B).

The ZPS VW voltage is shown in Fig. 25. If a reference valve voltage is going to exceed $V_{Vmax}^{nom}$ during "overlap", the ZPS VW voltage, which is input to the valve voltage generation block in Fig. 4, is modified so that the reference valve voltage is now limited to $V_{Vmax}^{nom}$.

The ride-through strategy described for this fault is also applicable to line-line AC faults with residual LW voltages all the way down to 0pu.
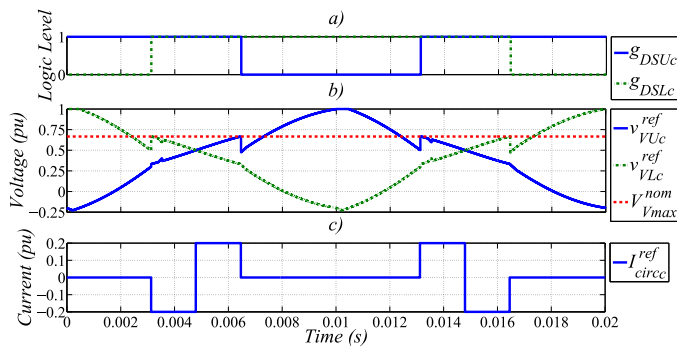
Fig. 24. Phase 'c' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for phase 'a' and 'b' 0.8pu residual LW voltages
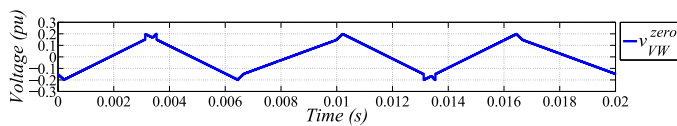


Fig. 25. ZPS VW voltage for phase 'a' and 'b' 0.8pu residual LW voltages

## B. 0pu Fault

The phase 'a', 'b' and 'c' waveforms for phase 'a' and 'b' 0pu residual LW voltages are shown in Figs. 26, 27 and 28, respectively, and the ZPS VW voltage is shown in Fig. 29. The ride-through strategy during this fault is the same as that of a 0.8pu fault. However, just before 0.002 s, for example, the phase 'a' reference upper valve voltage slightly exceeds $V_{Vmax}^{nom}$ during phase 'a' "overlap" (see Fig. 26) because the phase 'c' reference lower valve voltage is being limited to $V_{Vmax}^{nom}$ by the ZPS VW voltage during phase 'c' "overlap" occurring at the same time (see Fig. 28). Yet, the maximum valve voltage ($\approx 0.7$pu) only exceeds $V_{Vmax}^{nom}$ by 5%.

## VII. EXPERIMENTAL RESULTS

The AC fault ride-through strategies presented in Sections III, V and VI are experimentally validated by using the SSP, which is described in detail in [29]. In summary, the experimental setup comprises the SSP, a OPAL-RT Technologies rapid prototyping control platform, and programmable power supplies for the AC and DC sides. There are three cabinets
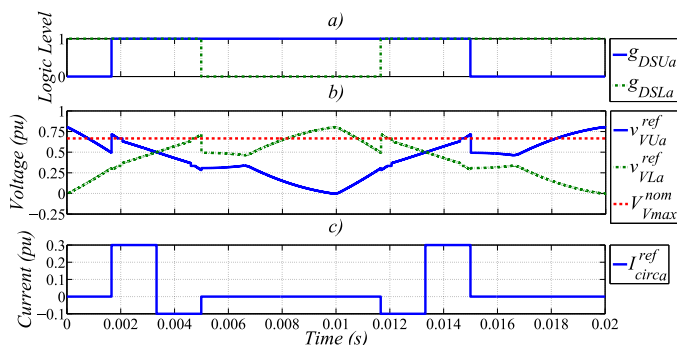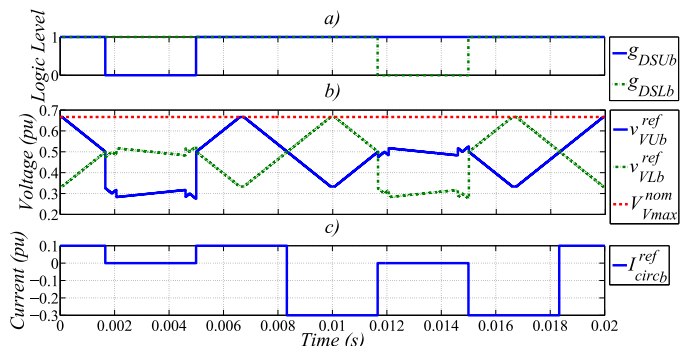


Fig. 26. Phase 'a' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for phase 'a' and 'b' 0pu residual LW voltages



Fig. 27. Phase 'b' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for phase 'a' and 'b' 0pu residual LW voltages
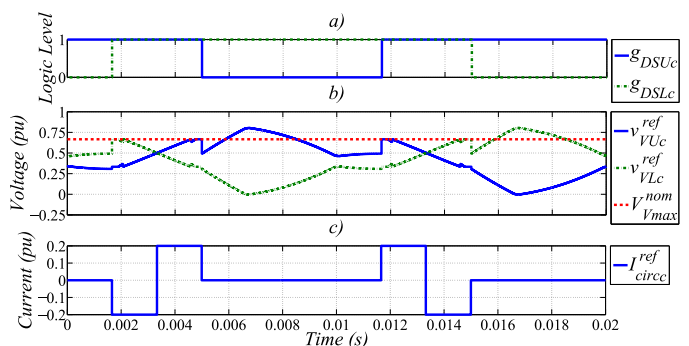


Fig. 28. Phase 'c' a) DS gate signals, b) reference valve voltages, and c) reference circulating current for phase 'a' and 'b' 0pu residual LW voltages

containing the SSP and control hardware, and these are pictured in Fig. 30. The main elements of the leftmost cabinet are three AC side single-phase transformers, six DSs, and six arm inductors. The middle cabinet contains 60 SMs (ten per arm). The rightmost cabinet houses the control hardware. Fig. 31a) pictures the back of the middle cabinet showing backplane PCBs, there are twelve in total (two per arm). Five SM PCBs are connected to each backplane PCB, by a plug and socket configuration, for ease of disconnection. Each SM PCB is connected to an IGBT module interface PCB, again by a plug and socket configuration. An unplugged SM PCB and its IGBT interface PCB are pictured in Fig. 31b).

Fig. 1 illustrates the SSP schematic and shows voltage and current conventions. Positive active power indicates that the converter is inverting and positive reactive power indicates that current is lagging voltage. When operating the SSP in AAC "extended-overlap" mode with a DC voltage of 1 kV, the main parameters are given in Table VII. Data for the experimental results is captured by the OPAL-RT control platform at a sampling period of 135 µs and is plotted by MATLAB®.
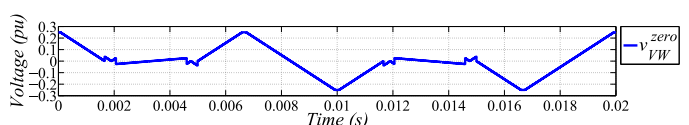


Fig. 29. ZPS VW voltage for phase 'a' and 'b' 0pu residual LW voltages

Fig. 30. Cabinets for components interfacing SMs with AC and DC sides (left), SMs (middle), and control hardware (right)
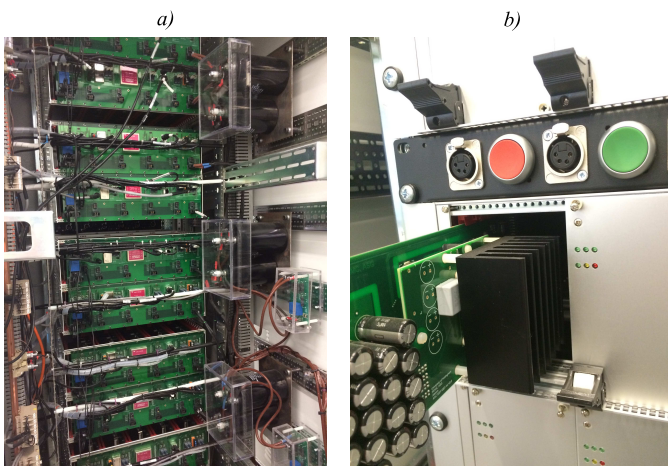


Fig. 31. SSP a) backplane PCBs, and b) SM and IGBT interface PCBs

TABLE VII
SSP PARAMETERS

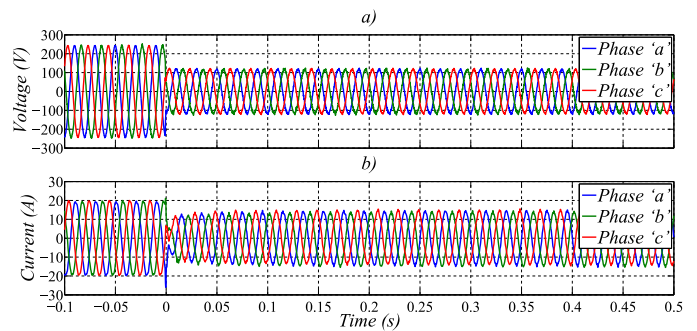| Parameter | Symbol | Value |
|---|---|---|
| Rated active power | $P^{rat}$ | 7.43 kW |
| Rated reactive power | $Q^{rat}$ | 2.45 kVAr |
| RMS line-line LW voltage | $V_{LW}$ | 292.16 V |
| RMS LW current | $I_{LW}$ | 15.46 A |
| Transformer turns ratio | $N_{VW}$ | $1.61\sqrt{3}$ |
| DC voltage | $V_{DC}$ | 1 kV |
| DC current | $I_{DC}$ | 7.43 A |
| Arm inductance | $L_{arm}$ | 0.75 mH |
| Number of SMs per valve | $N_{sm}$ | 10 |
| Nominal SM voltage | $V_{sm}^{nom}$ | 100 V |
| SM capacitance | $C_{sm}$ | 1.08 mF |



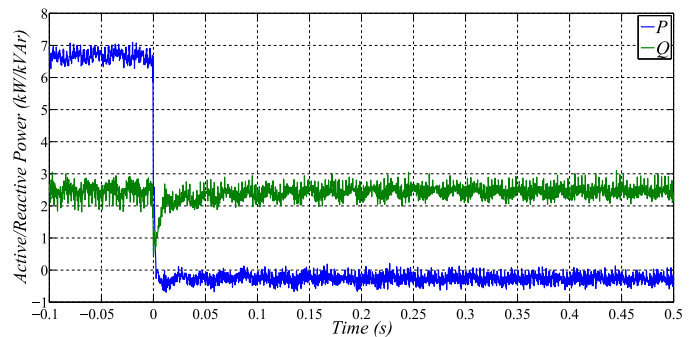Fig. 32. Experimental result of LW a) voltages and b) currents when applying a 0.5pu symmetrical AC fault



Fig. 33. Experimental result of LW a) active and b) reactive power when applying a 0.5pu symmetrical AC fault

### A. 0.5pu Symmetrical AC Fault

When applying a 0.5pu symmetrical fault to the AC supply voltages at rated power, the LW voltages and currents are shown in Fig. 32. The sudden depression in the voltages causes a spike in these currents, although protection limits are not exceeded. During the fault, the current magnitude is lower than prior to the fault due to the change in the selected active and reactive power operating point, as shown by the LW powers in Fig. 33. Active power transmission is suspended and pre-fault reactive power compensation is maintained during the fault as priority is given to reactive power to provide AC voltage support in this paper. However, the control strategy is fully adaptable to other combinations of active and reactive power priority. During the fault, as there is only a small LW active power (due to the power trim described in Section II-B to account for losses), but there is reactive power compensation, the LW voltages and currents are in quadrature.

Fig. 34 shows the DC side voltages and currents. The sudden decrease in the DC side currents causes a ripple in the DC side voltages, which decays within ≈ 0.5 s. This ripple is determined by the tuning of the DC voltage controller provided by the programmable power supply on the DC side, not by the converter, which is controlling active power. The additional harmonic content in the DC currents after applying fault is caused by the circulating currents required for SM energy management, as a result of the transient, not instantaneously cancelling on the DC side (see Section II-B). Although, these currents do decay within ≈ 0.5 s. Additionally, experimental considerations, such as measurement errors and component
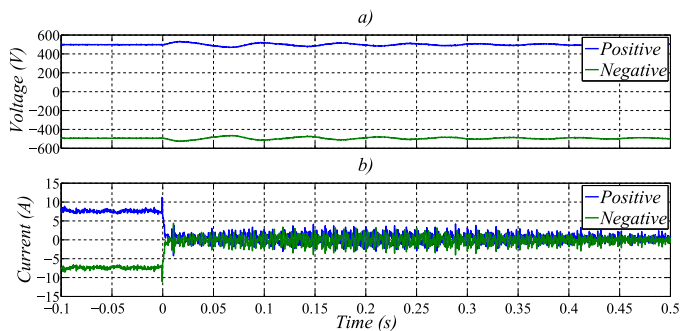
Fig. 34. Experimental result of DC side a) voltages and b) currents when applying a 0.5pu symmetrical AC fault
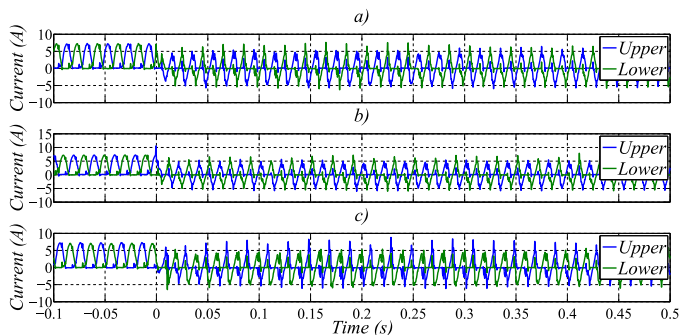


Fig. 35. Experimental result of valve currents for a) phase 'a', b) phase 'b' and c) phase 'c' when applying a 0.5pu symmetrical AC fault
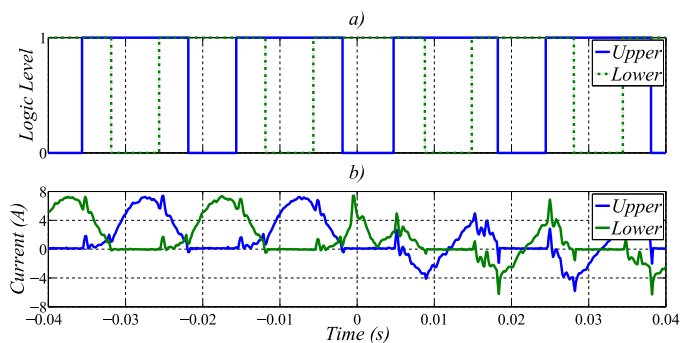


Fig. 36. Experimental result of zoomed a) valve currents and b) DS gate signals for phase 'a' when applying a 0.5pu symmetrical AC fault
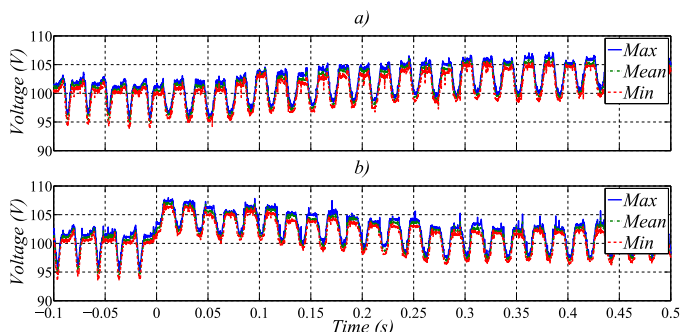


Fig. 37. Experimental result of phase 'a' maximum, mean and minimum SM capacitor voltages for the a) upper and b) lower arms when applying a 0.5pu symmetrical AC fault
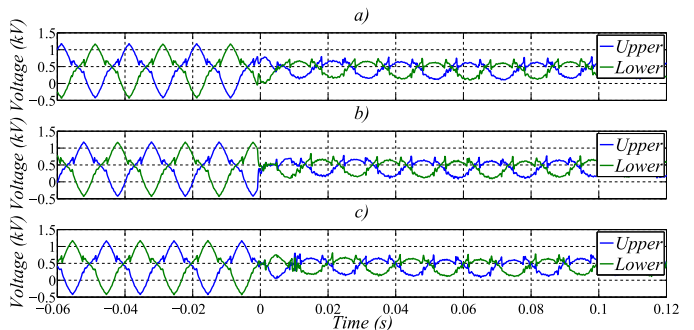


Fig. 38. Experimental result of zoomed reference valve voltages for a) phase 'a', b) phase 'b' and c) phase 'c' when applying a 0.5pu symmetrical AC fault
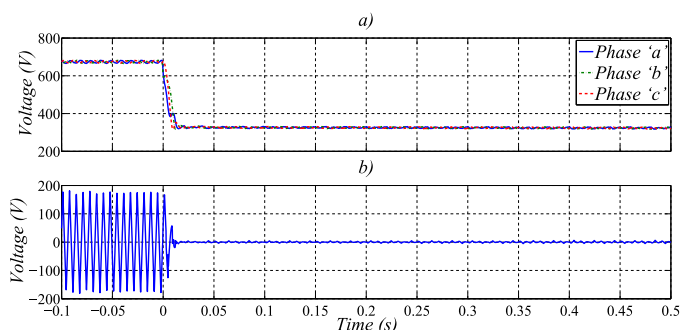


Fig. 39. Experimental result of VW a) fundamental voltage magnitudes and b) reference ZPS component when applying a 0.5pu symmetrical AC fault

tolerances, affect the cancellation. The harmonic content of the LW waveforms in Fig. 32 during faults is still however comparable to that during normal operation.

The valve currents are shown in Fig. 35. The fault causes a spike in these currents, although protection limits are not exceeded. As the LW voltages and currents are in quadrature during the fault, the VW voltages and currents are also, if the relatively small phase angle introduced by AC side impedance is neglected. As DS operation is coupled to the VW voltage, the valve currents are therefore both positive and negative during the fault [also see Fig. 12b)]. When a DS is required to open at the end of an "overlap" period, "zero-current" turn-off is achieved throughout by actually opening the DS when its valve current is negative, as illustrated by the zoomed phase 'a' DS gate signal and valve current waveforms in Fig. 36.

Fig. 37 shows the phase 'a' maximum, mean and minimum SM capacitor voltages. The fault causes the SM capacitor voltages to deviate from the set-point (100 V), but these voltages remain well within protection limits throughout. The phase 'b' and 'c' SM capacitor voltages also have a similar response.

Zoomed reference valve voltages are shown in Fig. 38 and the fundamental VW voltage magnitudes and reference ZPS component are shown in Fig. 39. During the fault, the reference ZPS component magnitude is ≈ 0 (see Table II). Consequently, the valve voltages are comparable to the ideal waveforms of Fig. 10b) in Section III.
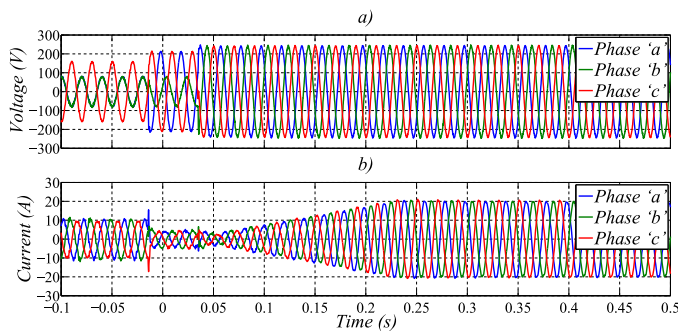
Fig. 40. Experimental result of LW a) voltages and b) currents when removing a 0pu line-line AC fault



Fig. 41. Experimental result of LW a) active and b) reactive power when removing a 0pu line-line AC fault



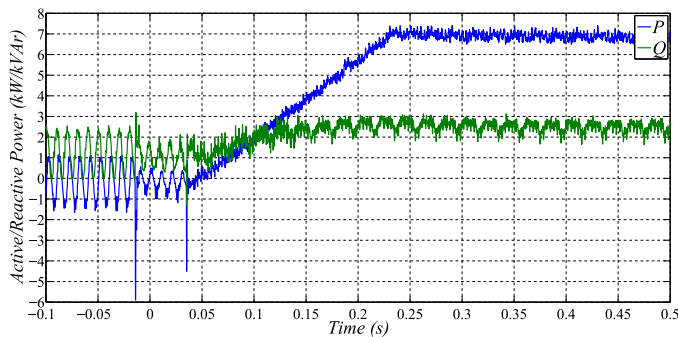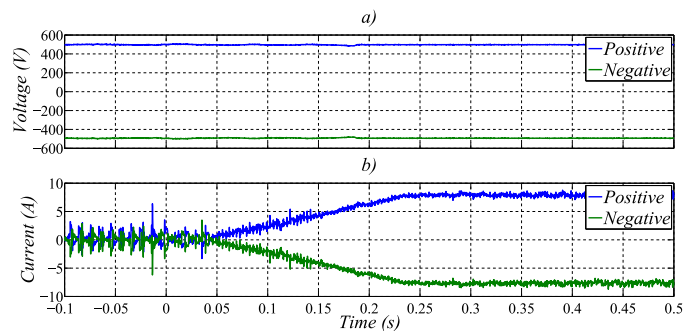Fig. 42. Experimental result of DC side a) voltages and b) currents when removing a 0pu line-line AC fault
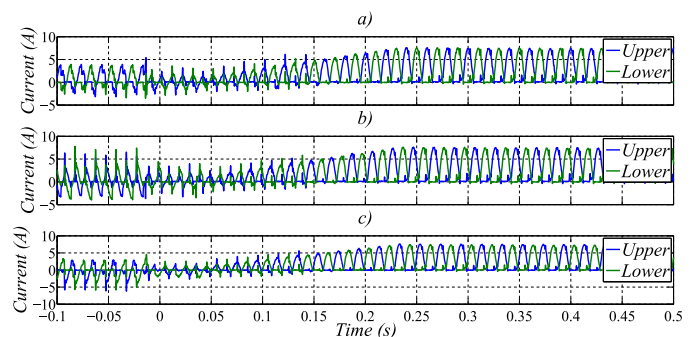


Fig. 43. Experimental result of valve currents for a) phase 'a', b) phase 'b' and c) phase 'c' when removing a 0pu line-line AC fault

## B. 0pu Single-Phase and Line-Line AC Faults

When demanding the AC power supply to remove a phase 'a' and phase 'b' 0pu fault, the LW voltages and currents are shown in Fig. 40. A limitation of the programmable AC power supply is that when demanding a three-phase voltage with Positive Phase Sequence (PPS), Negative Phase Sequence (NPS) and ZPS components, only the PPS and NPS components are actually realised. However, as the wye-delta transformer would block the ZPS component, the three-phase voltage seen by the converter on the VW is still as desired. Another limitation of the AC power supply is that only one (or all) of the voltage magnitudes can be changed simultaneously and therefore an interval of $\approx$ 50 ms between the two magnitude changes is observed. Consequently, a phase 'a' and 'b' 0pu fault is observed initially up to the first LW voltage transition, followed by a phase 'b' 0pu fault up to the second LW voltage transition, and then the fault is fully removed. After the fault is removed, the LW currents ramp back to their pre-fault values over $\approx$ 200 ms due to the programmed power ramp rate used in this paper.

The LW powers are shown in Fig. 41. During the fault, active power transmission is suspended, but reactive power compensation is continued to provide AC voltage support. As symmetrical LW currents are maintained, in the presence of an asymmetrical LW voltage, the LW powers both contain a twice fundamental frequency (100 Hz) ripple during the fault. After the fault has been removed, the pre-fault rated power is restored over $\approx$ 200 ms.

Fig. 42 shows the DC side voltages and currents. There is a slight dip in the DC side voltages as the DC side currents return to their pre-fault values. Figs. 43 and 44 show the valve currents and the phase 'a' SM capacitor voltages, respectively. The waveforms remain within protection limits throughout.

Zoomed reference valve voltages are shown in Fig. 45 and the fundamental VW voltages magnitudes and reference ZPS component are shown in Fig. 46. During the single-phase fault, these voltages are comparable to the corresponding waveforms presented in Section V-C and, during the line-line fault, are comparable to the corresponding waveforms presented in Section VI-B.
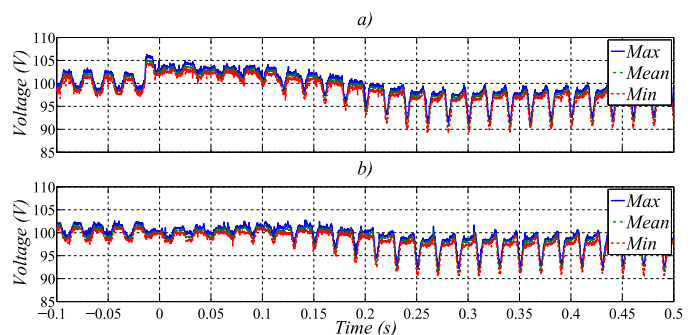


Fig. 44. Experimental result of phase 'a' maximum, mean and minimum SM capacitor voltages for the a) upper and b) lower arms when removing a 0pu line-line AC fault
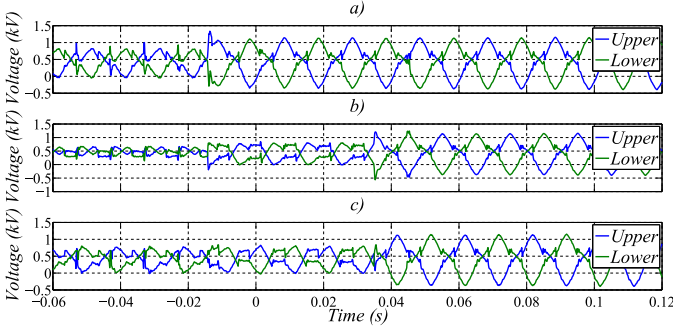
Fig. 45. Experimental result of zoomed reference valve voltages for a) phase 'a', b) phase 'b' and c) phase 'c' when removing a 0pu line-line AC fault
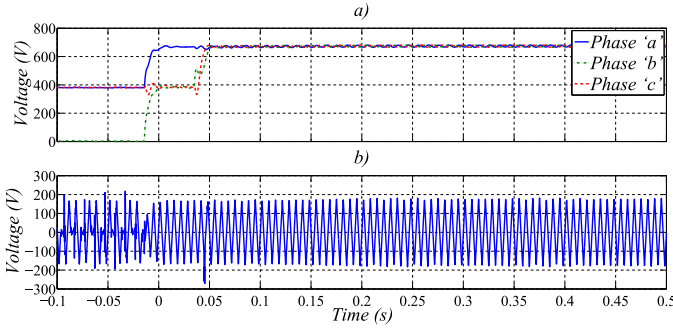


Fig. 46. Experimental result of VW a) fundamental voltage magnitudes and b) reference ZPS component when removing a 0pu line-line AC fault

## VIII. CONCLUSION

The AAC is a type of modular multilevel VSC that has been proposed for HVDC transmission applications. The AAC offers several benefits over the MMC, such as requiring typically 30–40% fewer SMs with half the capacitance and providing improved attributes for handling DC side faults. A major benefit of the AAC "extended-overlap" mode, over the "short-overlap" mode, is that a bulky DC side passive filter is not required. As HVDC converters are required by regulations to stay connected to AC networks during AC faults and, depending on operator requirements and fault severity, the converters may be required to exchange reactive power with the AC network to provide AC voltage support and continue to transfer active power. Furthermore, pre-fault active power should be restored after the fault is removed and voltage or current protection should not be triggered at any point throughout the entire fault sequence. An additional requirement for modular multilevel VSCs during faults is to aim to ensure that the capacitor voltage of each SM still remains within normal operation limits so that the converter continues to operate properly and safely. The novel ride-through strategies presented in this paper for symmetrical, single-phase and line-line AC faults allow the AAC "extended-overlap" mode to help meet these requirements under all anticipated AC fault conditions. The strategies have been successfully experimentally validated on a SSP and steady-state and transient results for representative AC faults have been presented.

## APPENDIX
### RELATIONSHIP BETWEEN LW AND RLW VOLTAGES

The phase-neutral LW voltages are related to the phase-neutral RLW voltages by (19). Given that LW voltages are defined by (20), the RLW voltages are then defined by (21).

$$\begin{bmatrix} v'_{LWa}(t) \\ v'_{LWb}(t) \\ v'_{LWc}(t) \end{bmatrix} = \frac{N_{VW}}{\sqrt{3}} \begin{bmatrix} v_{LWa}(t) - v_{LWc}(t) \\ v_{LWb}(t) - v_{LWa}(t) \\ v_{LWc}(t) - v_{LWb}(t) \end{bmatrix} \quad (19)$$

$$\begin{bmatrix} v_{LWa}(t) \\ v_{LWb}(t) \\ v_{LWc}(t) \end{bmatrix} = \begin{bmatrix} \hat{V}_{LWa}\sin(\omega t) \\ \hat{V}_{LWb}\sin(\omega t - 2\pi/3) \\ \hat{V}_{LWc}\sin(\omega t + 2\pi/3) \end{bmatrix} \quad (20)$$

$$\begin{bmatrix} v'_{LWa}(t) \\ v'_{LWb}(t) \\ v'_{LWc}(t) \end{bmatrix} = \frac{N_{VW}}{\sqrt{3}} \begin{bmatrix} \hat{V}_{LWa}\sin(\omega t) - \hat{V}_{LWc}\sin(\omega t + 2\pi/3) \\ \hat{V}_{LWb}\sin(\omega t - 2\pi/3) - \hat{V}_{LWa}\sin(\omega t) \\ \hat{V}_{LWc}\sin(\omega t + 2\pi/3) - \hat{V}_{LWb}\sin(\omega t - 2\pi/3) \end{bmatrix} \quad (21)$$

Each of the RLW voltages in (21) can be expressed as a single phasor, as shown in (22), so that the magnitudes and phases are known directly. By using trigonometry to superimpose sine waves, the relationship between (21) and (22) is given by (23), where inverse tangent is four-quadrant.

$$\begin{bmatrix} v'_{LWa}(t) \\ v'_{LWb}(t) \\ v'_{LWc}(t) \end{bmatrix} = \begin{bmatrix} \hat{V}'_{LWa}\sin(\omega t + \phi'_{LWa}) \\ \hat{V}'_{LWb}\sin(\omega t + \phi'_{LWb}) \\ \hat{V}'_{LWc}\sin(\omega t + \phi'_{LWc}) \end{bmatrix} \quad (22)$$

$$\hat{V}'_{LWa} = \frac{N_{VW}}{\sqrt{3}}\left(\hat{V}_{LWa}{}^2 + \hat{V}_{LWc}{}^2 - 2\hat{V}_{LWa}\hat{V}_{LWc}\cos(-2\pi/3)\right)^{1/2} \quad (23a)$$

$$\hat{V}'_{LWb} = \frac{N_{VW}}{\sqrt{3}}\left(\hat{V}_{LWb}{}^2 + \hat{V}_{LWa}{}^2 - 2\hat{V}_{LWb}\hat{V}_{LWa}\cos(-2\pi/3)\right)^{1/2} \quad (23b)$$

$$\hat{V}'_{LWc} = \frac{N_{VW}}{\sqrt{3}}\left(\hat{V}_{LWc}{}^2 + \hat{V}_{LWb}{}^2 - 2\hat{V}_{LWc}\hat{V}_{LWb}\cos(-2\pi/3)\right)^{1/2} \quad (23c)$$

$$\phi'_{LWa} = \tan^{-1}\left(\frac{-\hat{V}_{LWc}\sin(-2\pi/3)}{\hat{V}_{LWa} - \hat{V}_{LWc}\cos(-2\pi/3)}\right) \quad (23d)$$

$$\phi'_{LWb} = \tan^{-1}\left(\frac{\hat{V}_{LWb}\sin(-2\pi/3)}{\hat{V}_{LWb}\cos(-2\pi/3) - \hat{V}_{LWa}}\right) \quad (23e)$$

$$\phi'_{LWc} = \tan^{-1}\left(\frac{\hat{V}_{LWc}\sin(+2\pi/3) - \hat{V}_{LWb}\sin(-2\pi/3)}{\hat{V}_{LWc}\cos(+2\pi/3) - \hat{V}_{LWb}\cos(-2\pi/3)}\right) \quad (23f)$$

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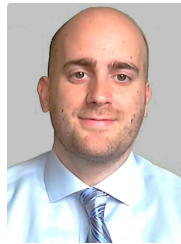
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