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A LIN Inspired Optical Bus for Signal Isolation in Multilevel or Modular Power Electronic Converters

Mark A. H. Broadmeadow and Geoffrey R. Walker
School of Electrical Engineering and Computer Science
Queensland University of Technology
Brisbane, Australia
Email: mark.broadmeadow@qut.edu.au

***Abstract*—Proposed in this paper is a low-cost, half-duplex optical communication bus for control signal isolation in modular or multilevel power electronic converters. The concept is inspired by the Local Interconnect Network (LIN) serial network protocol as used in the automotive industry. The proposed communications bus utilises readily available optical transceivers and is suitable for use with low-cost microcontrollers for distributed control of multilevel converters. As a signal isolation concept, the proposed optical bus enables very high cell count modular multilevel cascaded converters (MMCCs) for high-bandwidth, high-voltage and high-power applications. Prototype hardware is developed and the optical bus concept is validated experimentally in a 33-level MMCC converter operating at 120 Vrms and 60 Hz.**

I. Introduction

A. Local Interconnect Network

Local Interconnect Network (LIN) is an automotive serial network protocol originally developed as a low-cost, lower-speed alternative to Controller Area Network (CAN) for interfacing body sensors and components in vehicles [1]. The protocol utilises a single wire for the bus and can be implemented using standard UART peripherals, allowing inexpensive microcontrollers to be used as slave nodes [2].

Standard LIN operates at speeds up to 20 kb/s (constrained by a slew rate limitation imposed to meet EMC requirements) and allows up to sixteen slave nodes to be addressed by a single master [1]. Data on the bus is encoded by dominant (low) and recessive (high) states (wired OR). Bus arbitration is not required as the master node always initiates communication.

B. Proposed optical bus

We propose using the LIN concept as a basis for a low-cost bus for signal isolation in power electronic converters, where the physical layer is implemented using optical transceivers. In the optical version the one-wire transmission of logical voltage levels is replaced by the presence or absence of transmitted light. The presence of light is the dominant state on the optical bus, while the absence of light is recessive (analogous to wired OR). The interface to the microcontroller remains the same, via a UART peripheral.

With an appropriate physical configuration the transmission of light between the master and slaves can be achieved without any light guides. A typical implementation may involve the placement of all optical transceivers and hardware within a reflective enclosure.

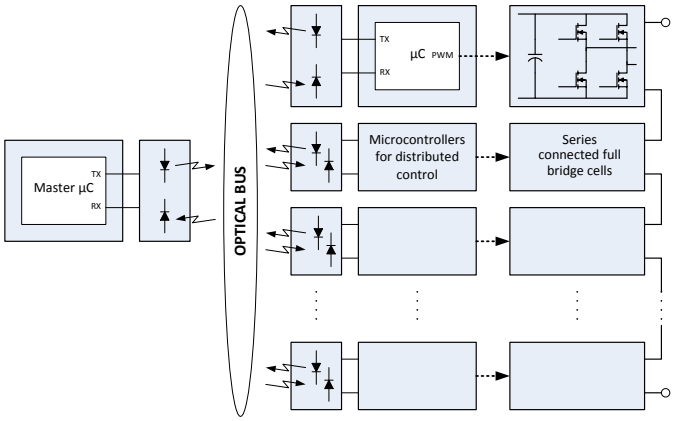

Fig. 1. Block diagram showing the proposed optical bus applied to a multilevel converter.

IrDA transceivers are proposed as an attractive solution for implementation of the optical bus. These transceivers are readily available, inexpensive, in a convenient form factor and optimised for low power consumption. It may also be attractive to operate these transceivers according to the IrDA specification, in which the LED is held on for only a portion of the pulse width. Many low cost microcontrollers include an IrDA extension to their UART peripheral which makes implementation of the pulse-shaping transparent from the perspective of the end user [2]. In the slowest mode, IrDA transceivers will operate up to 115.2 kb/s while in high-speed modes can operate up to 4 Mb/s, or higher depending on hardware and encoding.

C. Extension of the LIN concept

While LIN is the primary inspiration of the proposed optical bus, it may be both necessary and desirable to remove unnecessary features from the standard LIN protocol and to extend the protocol with modifications targeting the application to power electronic converters. For example, as EMI is not of concern for an optical bus, much higher bitrates can be targeted in order to support higher bandwidth converters. Similarly, it may be useful to dispense with some of the features of standard LIN, such as addressing and automatic baud rate detection in

order to reduce the overhead of the implemented protocol. Alternatively it may be useful to extend the address space beyond the standard sixteen nodes (the protocol supports up to 64 nodes [1]) for high-level-count MMCC converters with more than sixteen modules.

II. Features of the proposed optical bus

A. Auto-addressing

In many applications it may not be necessary to address slave nodes individually, however, in others applications it may be of interest to address individual modules, for the purpose of fault identification, for example. Addressing of nodes is inherent in the LIN protocol, and methods for auto-addressing of slaves already exist. Particularly the extra wire daisy chain method [1] would be suitable for application to the proposed optical bus.

In this configuration an additional input and output are required on each node. Each node is then daisy chained via an optocoupler. The order in which the nodes are connected then determines the address assigned to each node.

B. Modulation and synchronisation

The proposed application of the optical bus for signal isolation in power electronic converters is two-fold: firstly, synchronisation of the PWM carriers of the controllers of multiple independent switching modules, and secondly, broadcast of a common modulation reference to all controllers [3], [4], [5].

Synchronisation of the PWM carriers allows the switching of modules to be phase-offset, providing benefits in terms of effective switching frequency, filter requirements, and harmonics. Alternatively, if very-high-cell-count MMCCs are enabled by this isolation strategy, synchronisation of carriers may not be required, and it may be possible to rely on the diversity of the individual controller clock speeds alone [6].

C. Key benefits

- As light is used as the physical medium, the bus is not constrained by slew rate (EMI) considerations and is immune to electromagnetic interference from the switching converters.
- Optical isolation permits high-bandwidth converter operation at higher voltages than achievable with conventional isolation technologies. For example, direct connected converters at the 11 kV voltage level (~9 kV_{pk} L-N) could be realised utilising sixteen 1 kV modules in communication with a single master controller.
- The broadcast nature of the bus results in a flexible, scalable, extensible and modular solution for high-level-count MMCCs.

III. Experimental validation

An experimental prototype was developed to validate the proposed optical bus concept in hardware. Three primary goals were identified for this hardware:

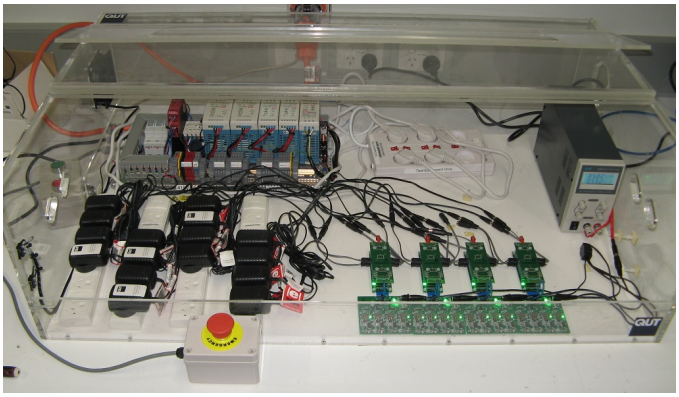

Fig. 2. Experimental setup of 33-level series connected MMCC with optical bus.

1) Demonstrate the optical bus concept at the physical layer utilising low-cost microcontrollers and IrDA transceivers.
2) Demonstrate broadcast of a common control signal to multiple slave controller nodes.
3) Demonstrate synchronisation of PWM carriers of slave nodes for the purpose of controlling PWM phase offsets between slave modules.

As the primary purpose of this initial prototype was to act as a proof-of-concept, functionality was limited to the three core priorities outlined above; possible improvements and enhancements are discussed in section VII below. Some specific boundaries and limitations of the implementation discussed in this paper are outlined below:

- Only unidirectional communication is implemented (master $\rightarrow$ slaves)
- Slaves are not individually addressable (broadcast only)
- PWM carrier phase offsets of slaves are hard-coded (unique firmware for each slave)
- The IrDA transceivers are operated in SIR mode (max. 115.2 kb/s).

IV. Experimental hardware

A. Multilevel converter platform

The optical bus prototype was targeted for application to a high-level-count modular multilevel cascaded converter (MMCC). A stackable modular multilevel prototype system had been previously developed [7] which was suitable for this purpose. This system was configured into a 33-level series-connected MMCC (sixteen full bridge modules) each with a 12 V DC bus (see fig. 2). This configuration provides working voltages up to 135 V_{RMS} with an achievable bandwidth in excess of 12 MHz. The modules have been previously demonstrated in a 9-level system driving ultrasonic transducers at fundamental frequencies up to 71 kHz and 34 V_{RMS} [8].

B. Optical bus transceiver module

A transceiver module was developed to implement an optical bus utilising low-cost microcontrollers and IrDA

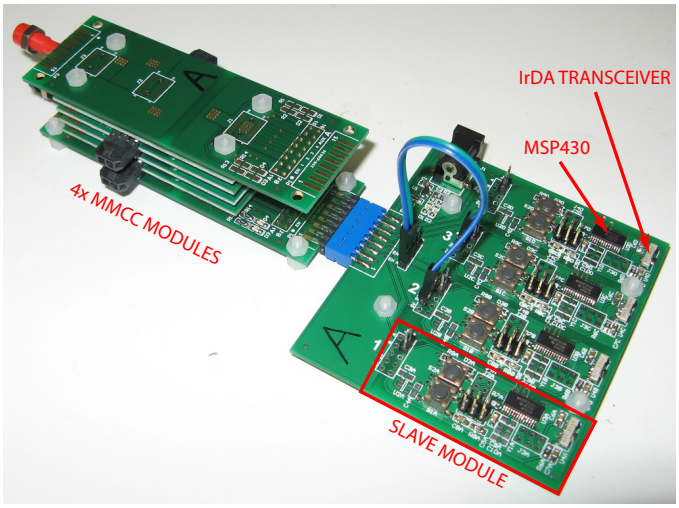

Fig. 3. Stackable MMCC module connected to four independent optical bus slave modules.

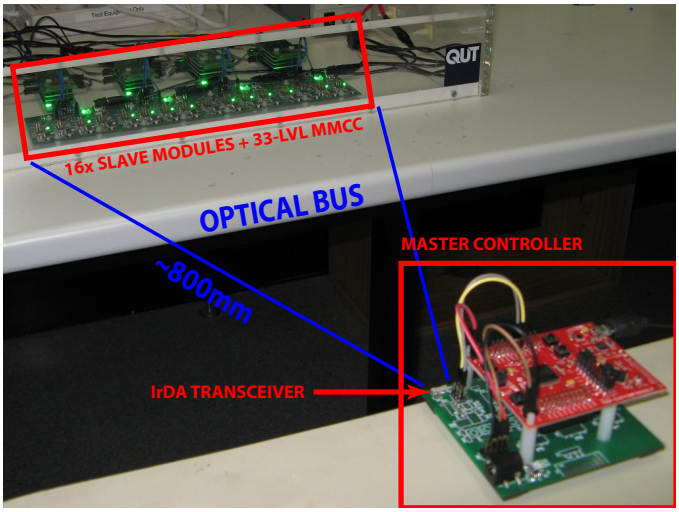

Fig. 4. Physical layout of 33-level MMCC prototype showing physical isolation between the master controller and slave hardware.

transceivers. Each module features a Texas Instruments MSP430F2132 microcontroller [9] and a Rohm RPM971-H14 IrDA transceiver [10]. Each module is capable of controlling a full-bridge via its PWM module. The selected microcontroller features a flexible UART peripheral which can provide encoding/decoding of IrDA signals as well as automatic baud rate detection for LIN implementation. Four independent modules were implemented onto a single PCB to allow easy interfacing with the stackable MMCC modules (see fig. 3).

The clock source for each slave micrcontroller was its on-chip digitally controlled oscillator configured to operate nominally at 16 MHz with a typical accuracy of approximately $\pm 1\,\%$.

C. Master controller

The master controller which broadcasts the modulating signal onto the optical bus was implemented using a MSP430F5529 development board coupled to the same IrDA tranciever module used on the slave modules (via a spare PCB with only the transceiver module populated, see fig. 4). The master controller 16 MHz clock source was derived from the on-board 1 MHz crystal.

D. Physical configuration

A total of sixteen independent switching modules and optical bus transceivers were arranged inside a transparent perspex safety box for testing (see fig. 2). Each full-bridge switching module was powered from a separate isolated 12 V plug-pack and all sixteen modules were connected in series. Switching modules were arranged in stacks of four for convenient connection to the slave controllers. A single 5 V power supply powered all slave controllers.

The master controller was placed outside the safety box, approximately 750 mm away from the slave transceivers and oriented towards the slave modules.

V. Controller Implementation

A. Master controller

The master controller was configured to broadcast a 16-bit modulating word onto the optical bus at a fixed frequency. For this work a sinusoidal modulating signal at 60 Hz fundamental frequency was selected. This signal was generated using direct digital synthesis (DDS) and a 4096 point quarter-wave sine table.

The update rate of the modulating word was selected as 3.906 kHz as a convenient (power of two) division of the clock frequency and close to full utilisation of the available bandwidth of the optical bus at 115.2 kb/s. Transmission of the modulating word was scheduled by a timer and interrupt driven.

The UART was configured as 8-bit with one stop bit and odd parity. Additionally the multi-processor address bit feature was enabled, which inserts an additional bit, the polarity of which signifies whether the transmitted byte should be treated an address or data. This feature was not used for addressing, but rather, as a way for the slave controllers to discriminate between the low- and high-bytes of the modulating word. The IrDA encoder function of the UART peripheral was also enabled.

B. Slave controller

The slave controller UART was configured to receive the 16-bit modulating word being broadcast by the master controller. The address bit was used to discriminate between the high- and low-bytes of the modulating word. If any parity or framing errors were detected in either byte, the whole word was discarded and the last correctly received value used.

The PWM output was configured in up-down mode to implement unipolar modulation. The counter compare registers were updated at both top and bottom, allowing both the rising and falling edges of each switching cycle to be modulated. Due to the 16 MHz limit on the system clock, only 12-bit PWM resolution could be achieved. A switching frequency of

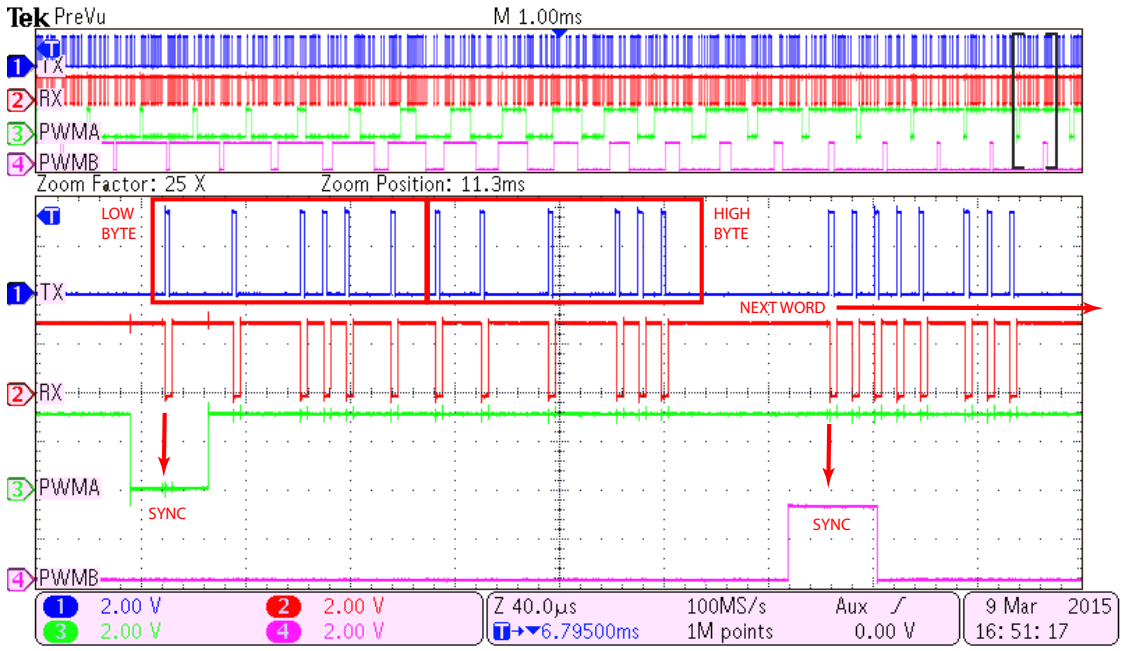

Fig. 5. Oscilloscope capture showing optical communication between the master module and a single slave module and detailed timing of a single PWM cycle. Shown are the master module IrDA transmitter input (CH1, blue, 2V/div), slave module IrDA reciever output (CH2, red, 2V/div) and slave module PWM outputs (each phase of the full-bridge, CH3&4, green & magenta, 2V/div).

1.953 kHz was selected such that each edge of the PWM was modulated by a new control word from the master controller. The PWM was configured to update the compare registers synchronously at the top and bottom of the counter cycle using the most recently received modulating word. Only the most significant twelve bits of the modulating word were utilised.

The slave modules were synchronised to the falling edge of the first start bit of each 16-bit word transmitted from the master controller. This was achieved by adjusting the DCO frequency of the slave microcontroller to maintain a phase lock with transmissions on the optical bus. A second timer was configured in capture mode on the slave microcontroller to act as a phase detector, triggered by the falling edge of the IrDA receiver output. The timer was reset each switching cycle by the PWM interrupt. A fixed phase offset could then be trivially introduced by adding or subtracting a fixed value to the captured phase delay.

VI. Experimental Results

Figure 5 details the operation of one of the sixteen slave controller modules. In the top part of the window the PWM of the slave module over a 10 ms period (approximately half a 60 Hz cycle) can be seen. In the bottom window detailed timing over a portion of a PWM cycle is shown. The PWM of the slave module has been synchronised with the falling edge of the received start bit (a zero phase offset in the case of the observed module). The 16-bit modulating word is transmitted by the master over an interval of approximately 200 µs; a small amount of idle time on the optical bus can then be observed prior to the transmission of the next 16-bit modulating word in the second half of the PWM cycle.

Figure 6 shows the resulting multilevel waveform produced by the sixteen independent modules when synchronised to the modulating signal broadcast by the master controller. Note that only 31 voltage levels are visible in this waveform due to the 90 % modulation depth. The modulating signal is clearly evident in the multilevel waveform. Synchronisation is achieved across the sixteen slave modules, as evidenced by figure 7. There are artefacts present in the multilevel waveform, however, that indicate perfect synchronisation has not been achieved. This can be attributed to two factors; firstly, up to 2 µs of jitter that was observed in the phase synchronisation, and secondly, the indeterminacy in the way the slave controller was implemented such that phase lock could occur at either the top or bottom of the carrier signal (i.e. 180 degrees out of phase).

Other minor issues with the controller were also identified during testing, particularly glitches in the PWM due to an absence of shadowing of the compare registers. Missed edges resulted in significant glitches in the 60 Hz waveform. This problem was exacerbated by high modulation depths due to extremely short pulse widths. These issues will be addressed in future revisions and enhancements to the simple controller structures presented in the work, as discussed in the following section.

VII. Future Work

A. Modulation strategy

Improved performance of the prototype presented in this work should be achievable though the application of improved modulation techniques. Many compromises were made in the development of the controllers in this work for the sake of simplicity, as comprehensive functionality was not a requirement to demonstrate proof of concept. As an example, it should be

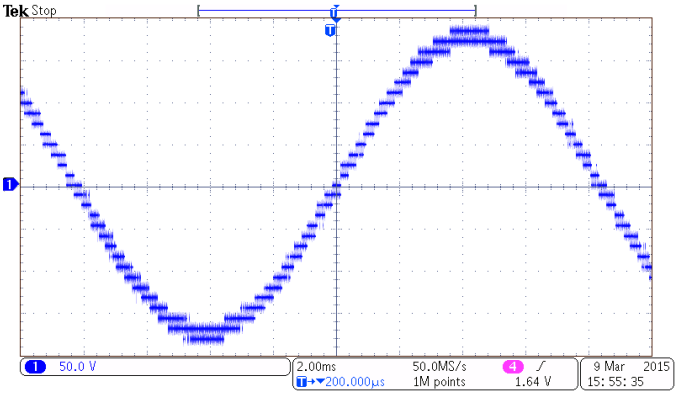

Fig. 6. Output waveform of 33-level MMCC converter prototype operating at 60 Hz 120 Vrms (90% modulation depth).

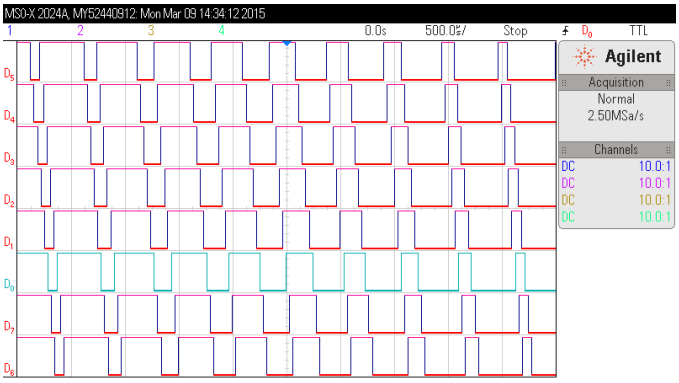

Fig. 7. PWM output of first eight slave modules showing synchronised phase offsets.

possible to achieve improved phase synchronisation by moving to a continuous counter mode for the PWM synthesis, avoiding some of the hardware restrictions of the MSP430, and allowing the PWM timer to also be used for the phase synchronisation function.

B. Improved bandwidth

In this work the bandwidth of the implemented converter was largely limited by the baud rate of the optical bus, with the IrDA transceiver in SIR mode. It should be possible to achieve substantially higher baud rates by instead operating the IrDA transceiver in MIR or FIR modes. In these modes the bandwidth will instead be limited by the maximum clock speed and UART capability of the microcontroller. With the current hardware, at least a four times increase in baud rate should be possible. It should also be possible to get additional bandwidth gains by reducing overheads in the protocol (e.g. eliminate unnecessary resolution, frame packing etc.).

C. Bidiectional communication

It is of interest to explore options for bidirectional communication using this optical bus technique. This would allow slave modules to provide feedback to the master. Ultimately this could facilitate closed loop control in which slave modules report locally measured values back to the master, which subsequently performs the global control. Alternatively, bidirectional communication presents the opportunity for distributed control, whereby modules share information necessary to perform local control, without the need for a master.

D. Addressing

Addressing of individual modules may be of interest in certain applications or control structures. Addressing may also be necessary to allow bidirectional communication on the bus (to avoid the need to implement some form of bus arbitration). The prototype hardware developed has ample capacity to explore protocol options for addressing and implementation of auto-addressing functionality.

VIII. Conclusion

A low-cost, half-duplex optical communication bus for control signal isolation in modular or multilevel power electronic converters has been presented in this paper. The concept has been inspired by the automotive LIN bus, where the one-wire physical layer is instead replaced by optical transceivers. The proposed optical bus has been validated experimentally using low-cost microcontrollers and IrDA transceivers in a 33-level MMCC converter operating at 120 V_{RMS} and 60 Hz.

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