RELIABILITY-ENERGY-PERFORMANCE OPTIMISATION IN COMBINATIONAL CIRCUITS IN PRESENCE OF SOFT ERRORS

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CERTIFICATE OF APPROVAL

I confirm that, to the best of my knowledge, this thesis is from the student's own work and effort, and all other sources of information used have been acknowledged. This thesis has been submitted with my approval.

Dr. Alex Bystrov
Prof. Alex Yakovlev

To my wonderful mother whose affection and love make me to get such success

To the soul of my father who was and will always be my role model

To my beloved wife who supported me to reach this stage

To my lovely kids Abulgasem, Salma, Zakaria, Sadeem and Yahia

— Mohamed

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ABSTRACT

The reliability metric has a direct relationship to the amount of value produced by a circuit, similar to the performance metric. With advances in CMOS technology, digital circuits become increasingly more susceptible to soft errors. Therefore, it is imperative to be able to assess and improve the level of reliability of these circuits. A framework for evaluating and improving the reliability of combinational circuits is proposed, and an interplay between the metrics of reliability, energy and performance is explored.

Reliability evaluation is divided into two levels of characterisation: stochastic fault model (SFM) of the component library and a design-specific critical vector model (CVM). The SFM captures the properties of components with regard to the interference which causes error. The CVM is derived from a limited number of simulation runs on the specific design at the design time and producing the reliability metric. The idea is to move the high-complexity problem of the stochastic characterisation of components to the generic part of the design process, and to do it just once for a large number of specific designs. The method is demonstrated on a range of circuits with various structures.

A three-way trade-off between reliability, energy, and performance has been discovered; this trade-off facilitates optimisations of circuits and their operating conditions.

A technique for improving the reliability of a circuit is proposed, based on adding a slow stage at the primary output. Slow stages have the ability to absorb narrow glitches from prior stages, thus reducing the error probability. Such stages, or filters, suppress most of the glitches generated in prior stages and prevent them from arriving at the primary output of the circuit. Two filter solutions have been developed and analysed. The results show a dramatic improvement in reliability at the expense of minor performance and energy penalties.

To alleviate the problem of the time-consuming analogue simulations involved in the proposed method, a simplification technique is proposed. This technique exploits the equivalence between the properties of the gates within a path and the equivalence between paths. On the basis of these equivalences, it is possible to reduce the number of simulation runs. The effectiveness of the proposed technique is evaluated by applying it to different circuits with

a representative variety of path topologies. The results show a significant decrease in the time taken to estimate reliability at the expense of a minor decrease in the accuracy of estimation. The simplification technique enables the use of the proposed method in applications with complex circuits.

Journal and magazines publications:

1. **Mohamed A. Abufalgha**; Alex Bystrovv, *Reliability-energy-performance interplay in combinational circuits*, (to be submitted), IEEE Transactions on Device and Materials Reliability.

   This journal paper extends the material published in the conference paper *Design-time reliability evaluation for digital circuits*. This extension includes applying the proposed method to evaluate the reliability of large circuits which have been chosen from ISCAS-85 benchmarks. Also, two filter solutions to improve the reliability of combinational circuits have been analysed, and a solution for the problem of time-consuming analogue simulations is introduced and evaluated. This journal paper is written in such a way as to summarise the material that is introduced in this thesis.

Conference publications:

1. **Mohamed A. Abufalgha**; Alex Bystrov, *Derivation of the reliability metric for digital circuits*, 2017 22nd IEEE European Test Symposium (ETS), PP 1-2, May 2017.

   The studies underpinning this paper can be found in Chapters 3, 5. In it a new method for evaluating the reliability of a combinational circuit is introduced briefly but without a comprehensive presentation due to the limited space allowed. In this paper, the reliability of a circuit is evaluated and introduced in terms of a trade-off relationship with the energy consumption and performance of the circuit. Also, a method for improving the reliability of the circuit is introduced.

2. **Mohamed A. Abufalgha**; Alex Bystrov, *Design-time reliability evaluation for digital circuits*, 2017 IEEE 23rd International Symposium on On-Line Testing and Robust System Design (IOLTS), pp 39-44, July 2017.

    The studies underpinning this paper can be found in Chapters 3, 5, as with the previous paper. However, in this paper the proposed methods for evaluating and improving the reliability of combinational circuits are introduced in more detail. Also, the proposed method is applied to a multipath circuit to evaluate its reliability.

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LIST OF ALGORITHMS

ACRONYMS

SET single event transient

SEE single event effect

LET linear energy transfer

PV parameter vector

PDF probability density function

UMC united microelectronics corporation

PIPB propagation-induced pulse broadening

SEU single event upset

SFM stochastic fault model

CVM critical vector model

r_{SET} the rate of neutron particle

ISCAS international symposium on circuits and systems

Vdd supply voltage

IC integrated circuit

ICs integrated circuits

CUT circuit under test

CMOS complementary metal oxide semiconductor

SPICE simulation program with integrated circuit emphasis

SER soft error rate

ISCAS international symposium on circuits and systems

FIT failure in time

CRs cosmic rays

MC   monte carlo

SEMT single event multiple transient

DVFS dynamic voltage frequency scaling

Part I

Thesis Chapters

INTRODUCTION

1.1 MOTIVATION

A reliability metric can be defined as the ability of a system to continue to deliver its specified function without failure for a given period of time [27]. Reliability is one of the aspects of the value produced by a system or a circuit within a system. This value has several components For example, the reliability which can be defined as the percentage of the valid results. The energy which represents the cost of the valid results. The performance which is the number of valid results per unit of time. The unit cost which reflects the cost of the device including non-recurring engineering costs. Some of these components positively contribute to the value of the circuit, such as reliability and performance. However, some of them are negative contributors which decrease the value of the circuit, such as energy and unit cost. This study addresses all of these issues in application to design of combinational circuits rather than entire systems. In particular, this fits in the overall concept of dependability, which is the ability of a system to deliver a service that can justifiably be trusted [9, 97]. The taxonomy of dependability from [9] can be expanded as shown in Fig. 1.1. The blocks framed by black lines are relevant to the work described in this thesis. The blocks with a white background are those which are introduced in this study to the existent taxonomy. The reason for this is that dependability makes no sense if it is applied to a system which has no worthwhile level of performance. Moreover, one cannot say that the dependability of a system is high if it is achieved at the expense of very high energy or cost. The present work investigates a three-way trade-off involving reliability, energy and performance (REP) metrics, so that one can optimise these metrics to the technical requirements of a design. The unit cost is also addressed in looking for a method to increase the reliability metric by adding modifications which are inexpensive in terms of area, energy and performance using the filters which are introduced in Chapter 5.

Dependability threats are events affecting one or more of the dependability attributes of a system. These threats can be categorised as faults, errors and
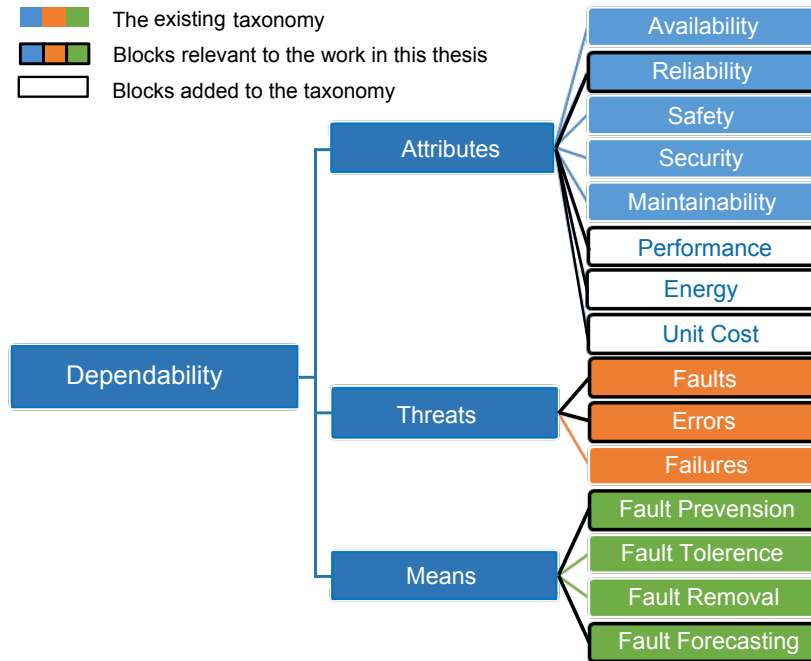
Figure 1.1: The taxonomy of dependability.

failures [9, 27]. In this work, the focus is on faults and errors, as they affect the circuit-level design. Faults, in our case, are transient faults caused by neutron particles hitting the silicon in a combinational circuit. Errors are the manifestations of faults at the primary output of the circuit.

To attain dependability of a system, various approaches are proposed each of which is used in such a way to achieve one or more attributes of dependability. These approaches can be classified into four categories: fault prevention, fault tolerance, fault removal and fault forecasting [8, 61]. This work contributes to fault prevention in Fig 1.1 by adding a filtering technique. It also contributes to fault forecasting by performing the reliability estimation of combinational circuits. This is conducted off-line at design time. Both filters and reliability estimation techniques are evaluated with regard to the negative contributors to the value (energy and cost), and their effect on the positive contributors (reliability and performance).

1.1.1 *Reliability of Combinational Circuits*

Scaling of complementary metal oxide semiconductor (CMOS) technology during the last four decades has been achieved by reducing voltage levels and the feature size of transistors. This has led to doubling the density of the

embedded transistors in the same size of chip every 1-2 years [29, 42]. So, the susceptibility of digital circuits to radiation-induced soft errors has increased, and the reliability of these circuits becomes a major concern for the designers of integrated circuits (ICs) [109]. This is can be seen clearly in Fig. 1.2, showing that in 1990 the minimum linear energy transfer (LET) that was needed to cause a glitch at a circuit node which would subsequently propagates to cause an error was $15MeV.cm^2/mg$. However, in 2004, an LET equal to $2MeV.cm^2/mg$ was sufficient to cause a glitch at the output terminal with a duration of a few nanoseconds [38, 59, 100]. Therefore, we need to know the extent to which the reliability of a combinational circuit may be affected by these errors and how is it possible to exploit available operation points such as values of supply voltage (Vdd) or minor changes in the circuit's structure in order to achieve reliable performance.
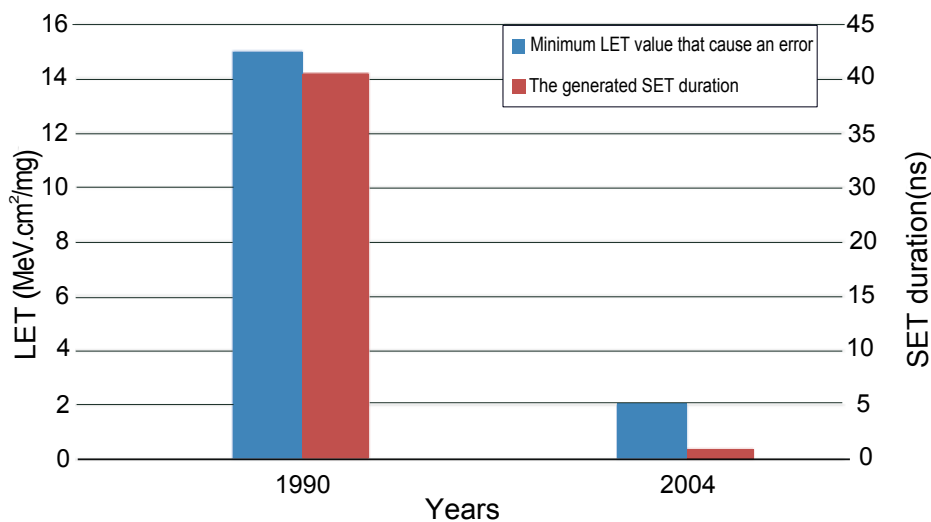
Figure 1.2: The effect of CMOS technology scaling on the susceptibility of electronic circuits to soft errors.

1.1.2 *Switching from Power-Performance Optimisation to Reliability-Energy-Performance Optimisation.*

For many years, the predominant target for ICs designers was to increase the performance of new designs regardless of their power consumption. With technology scaling, however, a higher number of devices are included in the same chip area, and power dissipation has become a crucial issue that

should be taken into account during design time [2, 101]. Power management techniques have been suggested to tackle problems associated with power dissipation in some applications, such as battery-mobile and wearable systems [88], where ultra-low power consumption and energy supply are considered to be crucial constraints among the design requirements [10, 92].

The most commonly used technique in power management is dynamic voltage frequency scaling (DVFS), which relies on lowering the voltages and/or frequency of a circuit in order to reduce the consumed power or energy. The relationship between the dynamic power and the voltage and frequency of a circuit can be described by the equation $p \propto FV^2$, where F is the operating frequency and V is the voltage that is needed for the circuit to operate in a stable manner [66, 88]. However, the use of the DVFS technique affects the reliability of that circuit. This is because decreasing the supply voltage of the circuit leads to a decrease in the critical charge of the nodes of the circuit, which means that low energy particles become a major cause of soft errors [39, 135, 141].

Thus, a reliability metric should be included in the classical power-performance trade-off to become a reliability-energy-performance trade-off.

1.2   THESIS SCOPE AND CONTRIBUTIONS

The thesis addresses the problem of evaluating the reliability of combinational circuits in terms of changes in performance and energy. Performance and energy consumption are calculated according to the value of Vdd applied to the circuit. This work considers transient faults caused by neutron particles which may affect digital circuits during its normal operation. The research work in this thesis focuses on studying the generation and propagation of transient pulses at various voltages. This enables us to evaluate precisely the reliability metric and to study the effect of circuit parameters on transient pulse propagation. This research is conducted at the circuit level of abstraction.

The major contributions of this thesis can be summarised as follows:

- Reliability, energy consumption and performance metrics are combined in one trade-off interplay. This relationship allows us to explore the change in reliability due to changing one or both the other metrics of performance and energy consumption. So, performance and/or energy consumption can be tuned depending on their criticality for the application so as to

control the reliability. This is accomplished by a new proposed method for the evaluation of reliability at low levels of implementation in the bottom-up design flow. This design flow can be seen in Fig. 1.3, which shows two main aspects of system design architecture which are the implementation and verification paths. So, using this approach, we are able to address reliability issues at the stage of designing a circuit as a group of logic gates and flip-flops. If issues with circuit reliability are detected, it is possible to rectify them in the early stages of implementation.
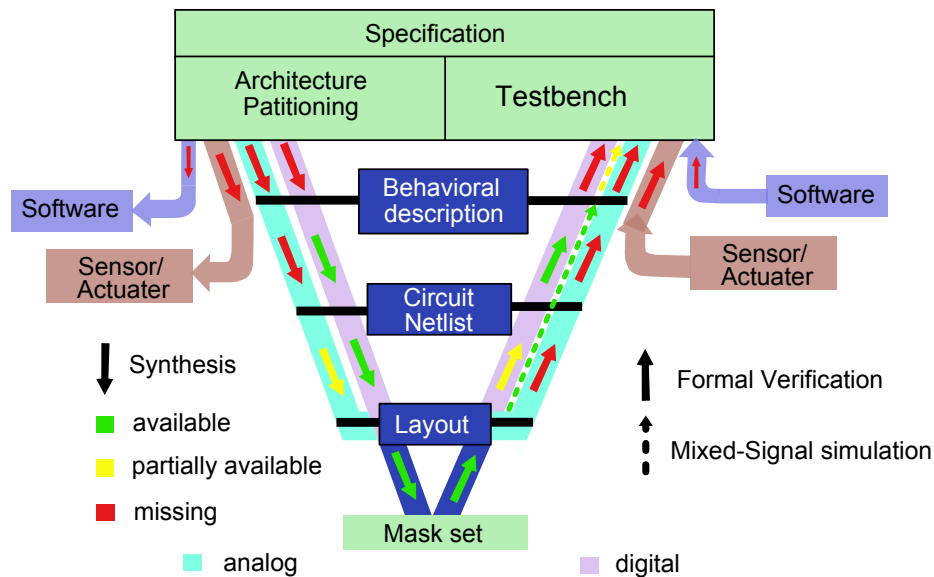
Figure 1.3: The V-Cycle of System Design Architecture [43].

The core idea of the proposed method is based on splitting the reliability evaluation process into two levels of characterisations: a platform-level stochastic interference model and a circuit-level model:

– The platform-level interference model is fixed and applicable to any design or system under test. For example, it may include a probability density function (PDF) of neutron energy and a model of the current pulse in the transistor as a function of the neutron energy, transistor size and type, source-drain voltage, temperature, etc. Its purpose is to characterise the interference, possibly expressed in non-electrical terms (*for example* particle energy distribution), as electrical effects, (*for example* pulses of current having their magnitude, duration and arrival time described stochastically). This is done just once at design time and not specific to a particular design but is universal for every component in the circuit.

– The circuit-level model is the core idea of the proposed method. This model converts the stochastic description of the electrical interference (the current pulse caused by neutron strike) into the probability of error at the circuit output. This is achieved by finding the critical values for the interference parameter beyond which it causes an error; *for example* an incorrect output value written into a flip-flop. The critical values are found by a series of analogue simulation runs on the circuit. Then, given knowledge of the critical values of the interference parameter, it becomes possible to analytically recalculate the stochastic model of the interference into the probability of an output error or correct operation (reliability).

• In this work, neutron particle strikes are chosen to be the cause of the faults in a digital circuit. So, in order to apply the proposed method for the estimation of the reliability of combinational circuits, we need to model the transient current pulse that is generated because of the particle strike. This model needs to be chosen carefully, as it has a significant impact on the accuracy of the estimated reliability. A model introduced in [80] is used. In this model, the effect of a neutron strike is represented as a dependent current source added to a BSIM4 Spice model of a MOSFET transistor. Moreover, the energy of the particles is expressed as a metric of LET, because it is the effect of their interaction with the transistor that matters here and not their kinetic energy. This model is attached using the Cadence tool in circuit-level simulation to inject an single event transient (SET) into the faulty node.

• The effect of logical masking and electrical masking on the generated SET is taken into account by using analogue simulation to find the critical values of the SETs at the output of the circuit under test (CUT). In some soft error rate (SER) techniques, such as FASER [137], a predefined trapezoidal shape has been used to represent the generated transient pulse rather than using a fault model to generate it. Models are also used to implicitly include the effect of logical masking and electrical masking, which caused ignoring the effect of propagation-induced pulse broadening (PIPB). Using these models accelerates the estimation process, but also decreases the precision of the obtained results.

• A technique to improve the reliability of combinational circuits is proposed. In this technique, a filter stage is added at the primary outputs of the

CUT. This filter stage suppresses most of the glitches generated in the prior stages. Two filter solutions have been developed and analysed. The first increases the size of the output gate, and the other is implemented by adding an RC circuit at the primary outputs of the circuit. Different types of filters contribute to improving the reliability of the circuit to different extents. Also, the effect of these filter stages on the circuit metrics of energy consumption and performance are studied in detail.

- To tackle the time consumption problem encountered when using analogue simulations, a simplification technique is proposed. This technique relies on finding the equivalence between the gates within a path and the equivalence between paths. This equivalence can be determined according to the contribution of these gates to the overall probability of error in the circuit. The results obtained using this technique are compared with the exact results. The comparison shows a minor reduction in the accuracy of the approximate results in favour of a dramatic reduction in computation time.

1.3 THESIS ORGANIZATION AND KEY FINDINGS

This thesis is organized into eight chapters, as follows:

Chapter 1 introduces the concept of the dependability of a system and its attributes, threats and means. This is followed by introducing the main motivations behind this research which are related to the reliability of combinational circuits. Then, a list of the main contributions of this thesis , and lastly the structure of this thesis.

Chapter 2 provides a brief background of areas relevant to the research topic, such as the generation of neutron particles and classifications of the interaction between these particles and any material. It also reviews the ionization process which occurs due to the interaction between neutrons and silicon. In addition, it gives details of the generation and propagation of SETs. Finally, in this chapter we highlight the previous techniques that have been proposed for the estimation of reliability and SER of combinational circuits and their drawbacks.

Chapter 3 introduces a new method for the evaluation of the reliability of combinational circuits. Several examples have been given to show how the proposed method can be applied to a combinational circuit. Also, a brief introduction on the fault model that used in our reliability analysis is given.

Chapter 4 introduces an automation scheme for the proposed method which makes it applicable for estimating the reliability of large circuits. Then, the reliability of different circuits is estimated and introduced. These circuits are chosen from the international symposium on circuits and systems (ISCAS)-85 benchmark circuits depending on their structure and the type of gates that are used to implement those circuits.

Chapter 5 presents a new technique to improve the reliability of combinational circuits. This technique relies on enhancing the inertial delay of the last stages to filter out narrow glitches. Two different solutions have been developed and analysed. The first using active elements where the size of the final stage is modified, and the second using passive cells where a low-pass filter is added at the end of the paths in the combinational circuit. Each of these is valid for work with certain structures of circuits.

Chapter 6 proposes a simplification technique that can be used when estimating the reliability of large circuits in order to reduce the time taken to complete the estimation. The simplicity and acceptable precision of this technique make it usable in circumstances where the time of estimation matters more than the accuracy of the estimated reliability.

Chapter 7 summarises the contributions of this thesis and indicates possible directions for future research.

BACKGROUND AND PREVIOUS WORKS

In this chapter, background information on neutron particles and their classifications is given, and the types of neutron-matter interaction are introduced in some detail. The influence of neutron particles in ionizing a silicon nucleus is described. The concepts of linear energy transfer (LET) and critical charge are also explained in this chapter. Then, the generation and propagation processes of an single event transient (SET) in a digital circuit are reported to provide on account of the physics of these events. An overview is given of relevant work that has been done so far on estimating and mitigating soft errors.

2.1 INTRODUCTION

In this section, a historical background is given of the effect of soft errors on the reliability digital circuits. Soft errors were first observed between 1954 and 1957 when they appeared as random failures in monitoring equipment during tests of nuclear bombs [73]. In 1962, the authors of [125] predicted that with the increasing component density of integrated circuits (ICs), the influence of cosmic rays and heavy ionized particles in affecting the operation of microelectronic circuits would become a major concern. During the 1970 and 1980, researchers began to pay attention to the soft errors induced by radiation and how it affects the reliability of semiconductor devices. However, most of this research was conducted in studies of soft errors in space equipment caused by radiation, since the effects of radiation were a major cause.

It was reported in several studies that radiation-induced soft errors can occur at sea-levels due to alpha particles [82, 83]. Alpha particles are emitted from decaying radioactive material that exists in the packaging of semiconductor devices. These particles penetrate near a storage node in a dynamic RAM, which leads to the creation of electron-hole pairs causing a random single-bit error in that node. In studies published in 1979 and 1980 respectively [47, 142] it was found that soft errors can be generated by the interaction

between neutron particles and the nuclei of silicon, which is the most commonly used material in the manufacture of semiconductor devices. This has been proven in physical experiments carried out on dynamic RAMs. In these experiments, arrays of DRAMs have been irradiated by a flux of neutron particles with different energies. The obtained results showed that one upset occurs for approximately 10^8 $particles/cm^2$. So, by using materials emitting fewer alpha particles, neutron particles have replaced alpha particles as the dominant cause of soft errors in RAMs since 1990 [55].

Up to that time, soft errors were considered to be a reliability issue for memory circuits. However, this belief changed in 1990, when researchers started to explore the effects of radiation on ICs. A study conducted by the authors of [98] investigated the generation of a transient pulse at the output of an inverter and for the first time the acronym SET was used by these authors. Many subsequent studies have examined the effect of radiation on logic circuits. The authors of [12] introduced different propagation scenarios for an SET generated in a combinational circuit. These scenarios mostly depend on the characterization of the generated SET. So, for a SET to be able to propagate to the output flip-flop and cause a soft error, it should be wider than the transition time of the gate that propagates in. In this case, the SET propagates without any attenuation. If the duration of the SET is lower than half of the transition time of the gate, it will be attenuated. However, a SET that has a duration in the range between these two values propagates with minor attenuation leading to its duration being reduced, and eventually it may be attenuated if it is generated in a long path. Accordingly, SETs generated in combinational circuits became a huge concern related to the reliability of microelectronic circuits. These assumptions have been confirmed by subsequent studies [26, 30, 35, 81] in which it has been proven that the effect of SETs becomes more significant with technology scaling, and various techniques were proposed to mitigate these transient pulses before reaching the output of the circuit.

2.2   BACKGROUND ON RADIATION ENVIRONMENTS

To understand the physics of soft errors, we need to know the causes of these errors and how they originate. For many years, the two dominant causes of soft errors at sea-level were alpha and neutron particles. The emission of alpha particles can be prevented by choosing good packaging material or

coating very vulnerable semiconductor components with a thick layer of a polyamide material [7, 67].
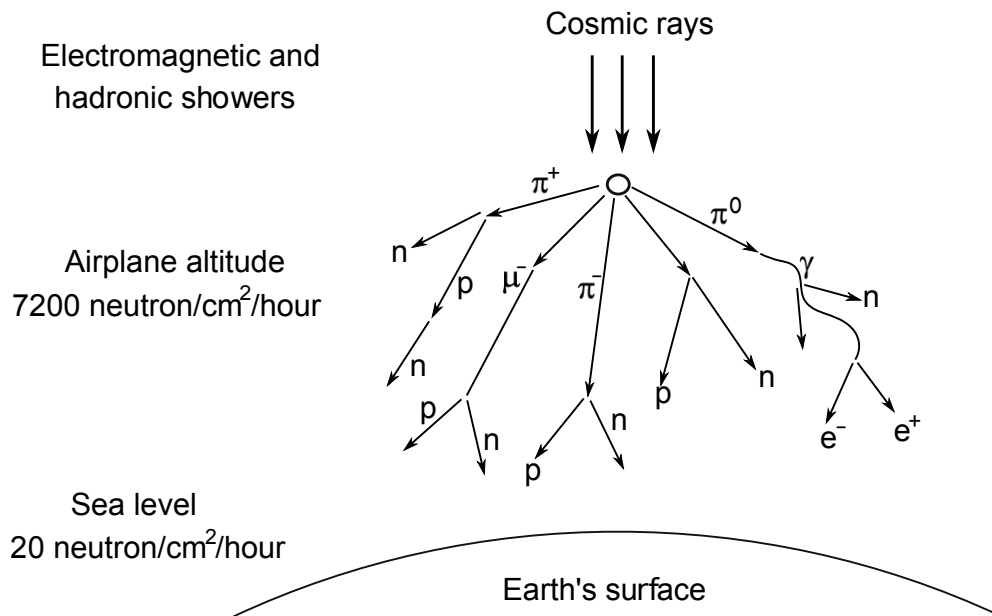
Figure 2.1: Secondary particles produced in the interaction of cosmic rays with the nuclei of atmospheric gases [28].

The other dominant cause is neutron particles. These are generated in the interaction between cosmic rays (CRs) and the nuclei of atmospheric gases. This interaction causes a cascade of nuclear reactions producing secondary particles such as protons, neutrons, muons, and other types of particle as shown in Fig. 2.1. The intensity of these secondaries is significant at an altitude of about 55Km, but the maximum levels can be reached at an altitude of 20km. The concentrations of these particles decrease as they travel to the earth's surface due to their energy being lost and short lifetimes, so that most of them have decayed and are absorbed. Electrons and protons are attenuated by interaction with the atmosphere before reaching the earth's surface. At sea level, only a very small percentage of these secondaries arrive. Due to their nature and longevity, around 1% of neutron particles arrive at sea level. This feature makes this type of particle the most dominant cause of single event effect (SEE) in semiconductor devices [6, 28, 40, 55, 62, 63, 99].

Despite the small percentages of neutron particles which arrive at the earth's surface, they consist of a variety of levels of energy from a few eV to TeV. The distribution of the energies of neutron particles as measured by Goldhagen and Gordon et al. (2004) is shown in Fig. 2.2 [5]. It can be seen from this figure that the flux has three peaks. The first is for high energy

neutrons and is centred around 100 MeV. The second peak is centred at about 1 MeV and represents thermal neutrons. The third peak is for the neutrons with very low energies that have already scattered with materials, and so they are slower and become in thermal equilibrium. In the same figure, the integral flux per square centimetre per hour can be seen, where the flux is divided into three parts according to the density of the particles.

Neutrons can be classified according to their kinetic energy into six different categories as follows [5]:

- Cold neutrons: with kinetic energy E<1 meV.
- Thermal neutrons: with kinetic energy E<0.5 eV.
- Epithermal neutrons: with kinetic energy 50 eV<E<50 keV.
- Fast neutrons: with kinetic energy 50 keV<E<1 MeV.
- Medium energy neutrons: with kinetic energy 1 MeV<E<10 MeV.
- High energy neutrons: with kinetic energy E>10 MeV.
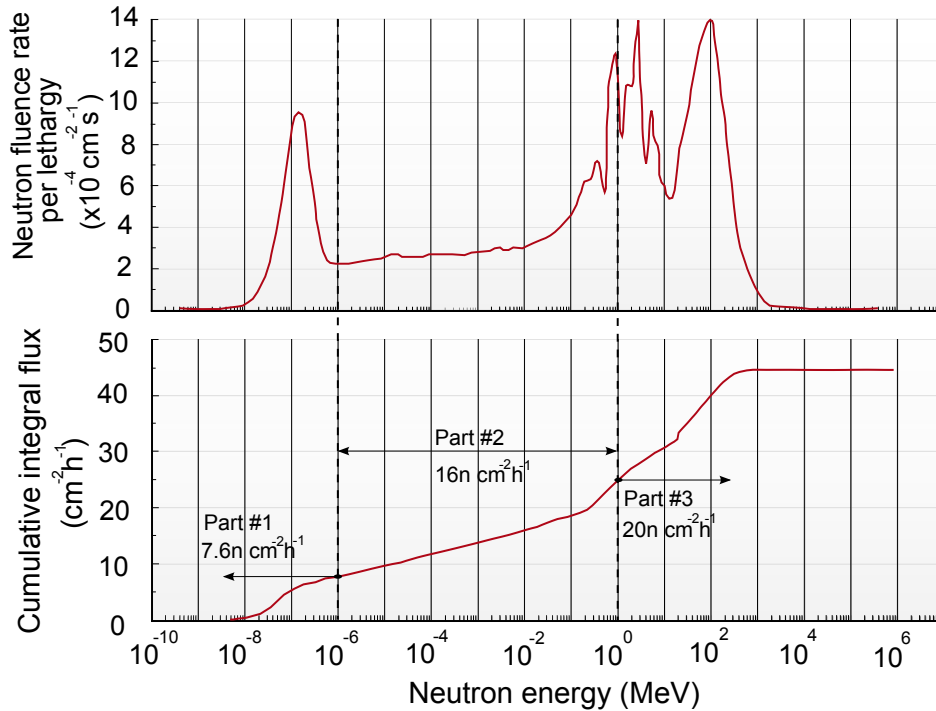
Figure 2.2: The energy distribution of neutron particle flux, and the corresponding cumulated integral flux measured at the roof of the IBM research centre; data is taken from [5].

2.3 INTERACTION OF NEUTRONS WITH MATTER

Neutron particles have the ability to penetrate deep into material. When such penetration occurs, there are three different scenarios. The first is that the penetrating particle has low energy, and so it collides with the material's nucleus. This collision causes the nucleus to be knocked out of the lattice then displacing other nuclei in the lattice. This affects the minority carrier lifetime and mobility, which causes a modification of the electrical characteristics of the component. In the second scenario, a particle with high kinetic energy collides with a nucleus of the material. This collision produces small charged fragments which have the ability to ionize the material directly. In the third scenario, the particle penetrates the material without any interaction with any nucleus. This kind of penetration does not cause any fault in the material [5, 6, 76, 99].

Neutron particles interact with material according to their kinetic energy and the interaction can be classified in two subcategories; scattering and absorption.

2.3.1 *Scattering Interaction*

Scattering interaction can be divided into two further subcategories: elastic and inelastic scattering. In elastic scattering interaction, the total energy of the particle and the nucleus is not modified, and the numbers of protons and neutrons in the nucleus remain the same as before the interaction as shown in Fig 2.3. However, the particle may lose some of its kinetic energy. The magnitude of the lost energy depends on the atomic weight of the nucleus. The lost energy can be calculated using the expression $2EA/(A+1)^2$, where A is the atomic weight of the nucleus, and E is the kinetic energy of the neutron [112].

In inelastic scattering interaction, the energy and direction of the penetrating particle change due to this interaction. Also, some of the particle's energy is transferred to the nucleus, which might leads to a modification of the state of that nucleus so that it has an excited state. Then, the total energy of the neutron and the nucleus after the interaction is less than the original kinetic energy of the penetrating particle, because part of the particle's energy is used to displace the nucleus to the new state. This loss in the kinetic energy of the particle leads to it slowing down and being transformed into another
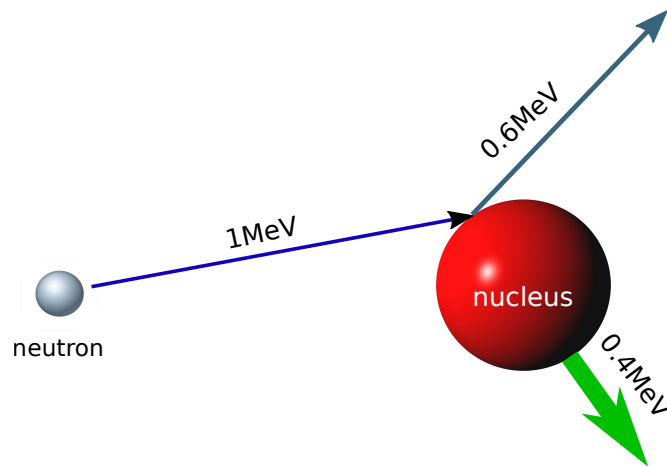
Figure 2.3: Elastic scattering interaction, the total kinetic energy is the same before and after the collision. [6].

type of particle depending on the new energy range, this is shown in Fig 2.4 [6, 99, 112].
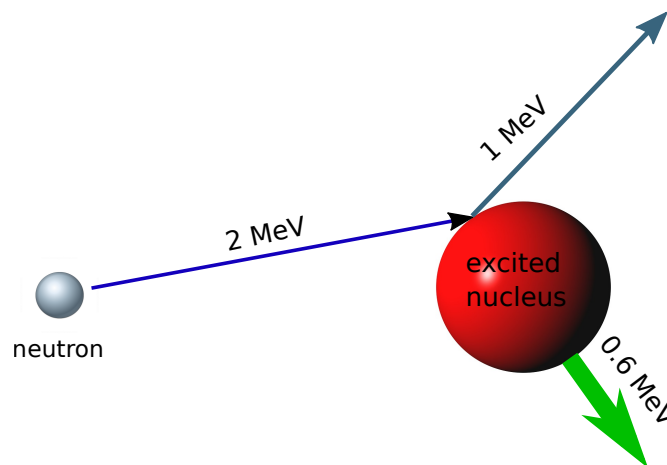
Figure 2.4: Inelastic scattering interaction, the total kinetic energy after the collision is less than the original. [6].

2.3.2   *Absorption Interaction*

Absorption interaction differs from scattering interaction. In this type of interaction, a neutron is absorbed or captured by a nucleus of the penetrated material. So, a large amount of radiation can be emitted and atomic recoil may be produced. The atom eventually breaks into small fragments, each of which can generate a charged particle [6, 54, 76, 112].

Here we are interested on the interaction between neutrons and silicon because silicon is the predominant material used in the semiconductor industry. In the rest of this chapter, the focus is on silicon as an irradiated material.

2.4 IONIZATION

A strike of a neutron particle has been chosen to be a cause of soft errors in the approach followed in the present study. Neutrons are neutral particles and so they do not ionize penetrated material directly. However, when a neutron particle penetrates silicon, this particle may collide with a silicon nucleus, and if the particle's energy is high enough, secondary ions may be produced. These ions travel through the material causing an excitation of electrons, and these electrons then ionise other atoms. This cascading ionization process causes an inducing channel along the path of the ion. The atoms that have lost one of their electrons rearrange themselves to form holes. A high density of electron-hole pairs is then formed in a narrow zone around the ion's track [6]. This ionization process of an atom of silicon can be seen in Fig. 2.5.
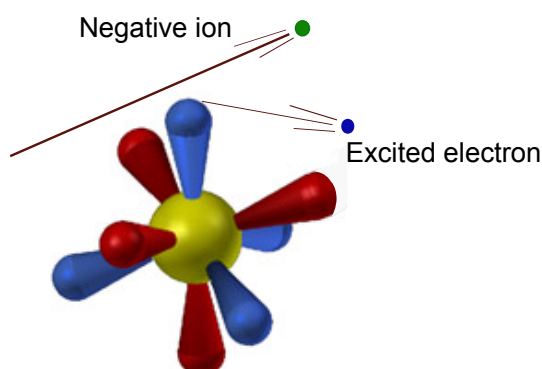
Figure 2.5: A negative ion passes near an atom and causes loosing one of its electrons which causes the ionization of that atom [6].

The normal operation of semiconductor devices boosts the ionization process. For example, when a secondary ion penetrates a region in the targeted node, this region is usually a reverse-biased p-n junction in a transistor. Due to the state of this junction and the potential across its terminals, it becomes sensitive to radiation effects. So a track surrounded by pairs of electrons and holes is generated as a result of the ionization process. This track is called a funnel, and it reshapes the depletion area of that junction as shown in

Fig. 2.6 [4, 6, 14, 91, 122, 131]. The recombination of these electrons and holes is caused by the potential across the terminals of the struck junction. This recombination causes the generation of a transient current pulse which may propagate through the circuit and cause a bit flip in the output flip-flop [56, 64, 128, 129, 139]. The generation and propagation of the transient voltage pulse is covered in detail in Sections 2.7 and 2.8.

Fig. 2.6 shows two neutron particles penetrating a transistor, both of which are high energy particles. One of them collides with a silicon nucleus in the transistor and secondary charged ions are generated. The other particle penetrates the transistor without any interaction and does not cause any fault in the circuit.
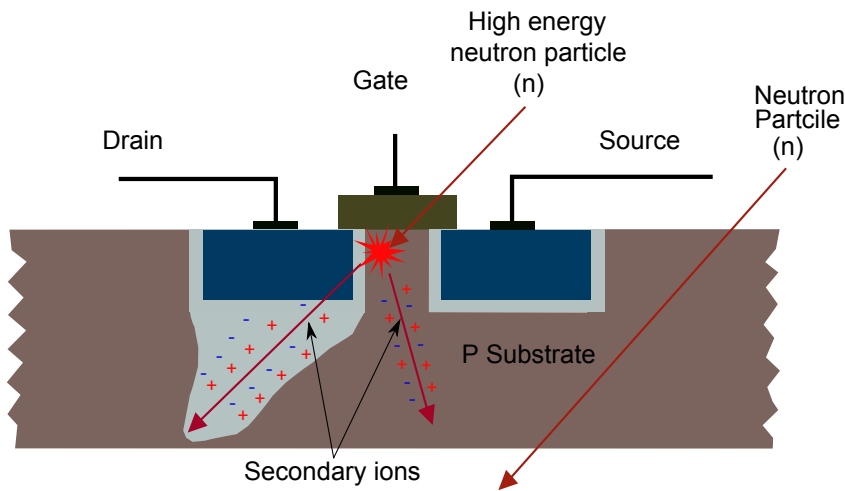
Figure 2.6: Penetration of neutron particles through a semiconductor device, a neutron interacts with a silicon nucleus and a neutron penetrate without any interaction [23, 55].

2.5 LINEAR ENERGY TRANSFER

When a particle travels through a semiconductor device, it loses some of its energy per unit length and this is called stopping power. It can be divided into two components:

1. Electronic stopping power is generated from the interaction or collision between an ionizing particle and an electron of an atom of the targeted material.

2. Nuclear stopping power is generated from the interaction between an ionizing particle and a nucleus of an atom of the targeted material.

Here, we are interested in electronic stopping power because it is the main reason for creation of electron-hole pairs, which is considered to be the first step in the generation of an SEE in a circuit. Electronic stopping power, which is called the LET can be explained as the energy deposited by an ionizing particle per unit of distance along its track. The value of LET depends on the type of ion that is created when the interaction happens. For example, a Magnesium ion has a LET higher than those of Helium or Lithium ions. An ion with higher LET ion causes a stronger effect in the semiconductor device [60].

LET can be expressed by the following equation, which represents the loss of a particle energy E per a unit of distance x [6].

$$LET = -\frac{\Delta E}{\Delta x}. \tag{2.1}$$

The LET in (2.1) is expressed in megaelectronvolts per micrometre. A weighted LET is used to evaluate the ratio of the LET to the density of the targeted material, which is in our case silicon [6].

$$LET = -\frac{1}{\rho}\frac{\Delta E}{\Delta x}, \tag{2.2}$$

where ρ is the density of the targeted material. The unit of the weighted LET in (2.2) is expressed in megaelectronvolts square centimetre per milligram. To convert from LET to weighted LET the targeted material should be known. In our case, it is silicon which has a density of 2.32 g/cm^3. So, the LET that is expressed in $MeV\mu m^{-1}$ can be replaced by its equivalent weighted LET expressed in $MeVcm^2mg^{-1}$ (deposited in silicon) using the following steps [6]:

$$1\,MeV\mu m^{-1} \Leftrightarrow \frac{1\,MeV}{10^{-4}cm \times 2.32 \times 10^3\,mgcm^{-3}} = 4.31\,MeVcm^2mg^{-1}. \tag{2.3}$$

As mentioned earlier, LET describes the average energy that is lost during the passage of an ion across one unit of distance. To express the LET in more convenient units for electronics designers, it is better to express it using the unit of electrical charge, the coulomb. This makes it more comparable with the critical charge of a node and the physical dimensions of that node. The average energy that is needed to create an electron-hole is equal to 3.6 eV,

and if we know that the electron charge is equal to 1.610^{-7} pC, using all these parameters the LET can be expressed as follows [6]:

$$1\,\text{MeV}\mu\text{m}^{-1} \Leftrightarrow \frac{1.6 \times 10^{-7}\,\text{pC} \times 10^{6}\,\text{eV}}{3.6\,\text{eV} \times 1\,\mu\text{m}} = 0.0446\,\text{pC}\mu\text{m}^{-1}. \tag{2.4}$$

Using the two equations (2.3) and (2.4), the charge collected in a semiconductor device due to interaction with a neutron particle can be expressed by the following relationship [65]:

$$Q\left(\frac{\text{pC}}{\mu\text{m}}\right) = 1.035 \times 10^{-2}\text{LET}\,(\text{MeVcm}^2\text{mg}^{-1}), \tag{2.5}$$

where Q is the charge collected in the struck node. From (2.5) the charge that is deposited by a neutron can be obtained if the LET is known [6].

The LET deposited in a material depends on the kinetic energy of the ion and the distance it has travelled in that material. This applies until it reaches the maximum at Bragg peak. After this, the LET starts to decrease as the energy of the particle increases beyond the Bragg peak [22, 99].

2.6   CRITICAL CHARGE

The critical charge of a digital circuit node can be defined as the minimum charge that needs to be deposited by an ionizing particle or which can be collected by that node in order to change the state of that node. The critical charge of a node can be given by the following relation [95]:

$$Q_{\text{crit}} = C_N.Vdd + I_{DP}.T_F, \tag{2.6}$$

where Q_{crit} is the critical charge of a node, C_N is the capacitance of the struck node, Vdd is the supply voltage, I_{DP} is the maximum drain conduction current of the PMOS transistor, and T_F is the flipping time of the node. The term $I_{DP}.T_F$ can be ignored in case of characterise Q_{crit} by using SPICE simulations [95].

From the above equation, it can be noticed that the Q_{crit} of a node mainly depends on the capacitance of the node and the supply voltage that is applied to it. So, with decreasing values of supply voltage (Vdd) and node capacitance due to technology scaling, the value of Q_{crit} of a node is reduced as well.

This leads to increasing the susceptibility of new design technologies to the radiation-induced soft errors [54, 113].

(a) The relation between Q_{crit} and V_{DD}

(b) The relation between Q_{crit} and technology node
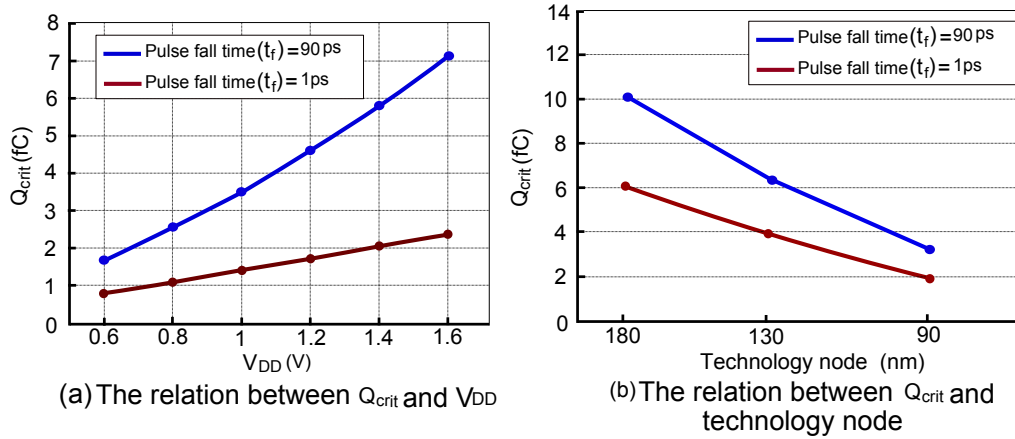
Figure 2.7: The effect of Vdd and technology node on the critical charge Q_{crit} of a node [54].

The effect of supply voltage on the critical charge of a node is illustrated in Fig. 2.7 (a). It is clear from the figure that the critical charge increases with supply voltage. The influence of design technology on the critical charge of a node is shown in Fig. 2.7 (b), and it is clear that the critical charge decreases with technology scaling due to the shrinking of node capacitance.

2.7 SINGLE EVENT EFFECT: MECHANISMS AND CLASSIFICATIONS

To study the reliability of digital circuits and how they are affected by soft errors, we need to understand the mechanism through which such errors are generated. In general the generation of SEEs because of either a direct or an indirect ionization process can be classified into two main categories:

1. A SET is a transient voltage pulse which appears at the output of a gate in a combinational circuit. This transient pulse is generated as a result of the passage of a charged ion across a sensitive junction in that gate. The generation mechanism of this pulse can be divided into three phases, as shown in Fig. 2.8. The first phase is shown in Fig. 2.8 (a), where an ionizing ion passes through a sensitive junction. This passage of the ion leads to generating pairs of electron-hole, and the density of these pairs depends on the charge deposited by the ion. In other words, it depends on the kinetic energy of the ion and the length of the tunnel it has travelled along. Each 3.6eV of deposited energy generates an electron-hole pair. A cylindrical track

of electron-hole pairs is thus formed along the path of the ion in the silicon. The second phase of an SET-generating mechanism is shown in Fig. 2.8 (b). In this stage, the carriers (the electrons and holes) drift and are collected by the local electric field of the junction. The electrons and holes are attracted to the N-substrate and P-substrate respectively. The electron's movement generates a current pulse, and the depletion region is distorted into a funnel shape due to the lack of equilibrium in the charge distribution. The distortion improves and increases the efficiency of the charge collection. These events end after tens of picoseconds, this prompt charge collection has occurred as a result of the existence of a local electric field across the struck junction. The final phase of this mechanism can be seen in Fig. 2.8 (c). In this phase, the funnel collapses and the electrons take a longer time to diffuse into the depletion junction due to the collapse of the junction potential. This stage takes hundreds of picoseconds, and it continues until all excess carriers have combined or diffused away from the depletion layer [6, 11, 122, 131].
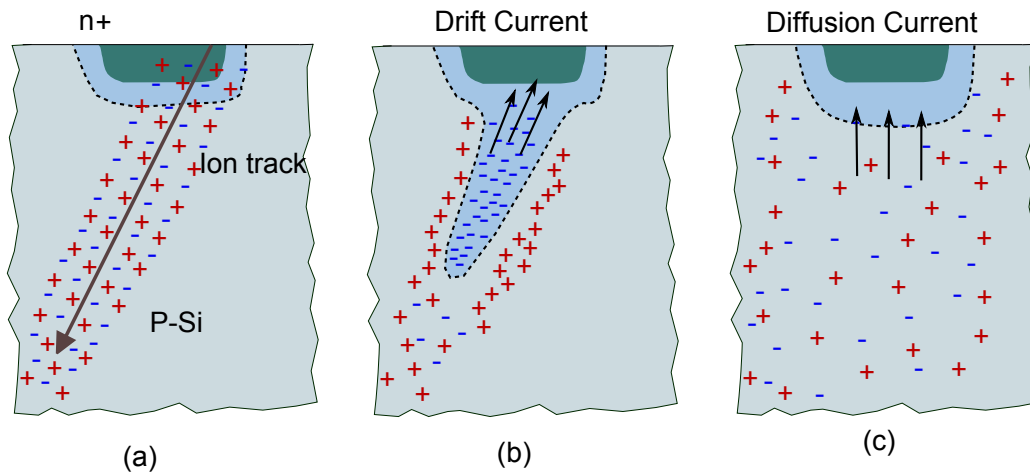
Figure 2.8: Charge deposition and collection caused by the interaction between a charged particle and a reverse-bias junction on a device: (a) an ionizing ion passes through a sensitive junction and pairs of electron-hole are generated; (b) is the drift stage where the electrons and holes are collected because of the effect of the local electrical field at the junction; (c) in this stage the potential of the junction collapses, and all excess carriers combine or diffuse away from the depletion layer [11].

A transient current pulse, as shown in Fig. 2.9, is generated as a result of the charge deposited by the ionizing ion. It can be seen from the figure that the transient current pulse can be divided into two main stages. In the first stage, where the pulse is produced from the prompt collection phase, this part of the pulse has a narrower duration and higher magnitude. The second

part of the pulse is a plateau produced by the diffusion occurring during charge collection, and it has a longer duration and lower magnitude than the first part of the pulse [14, 91].

If the deposited charge in a node is higher than the critical charge of that node, then the generated transient current pulse causes a glitch in the output of the struck node. This glitch is called an SET and it is transient because it is a temporary event caused by a transient effect [6].
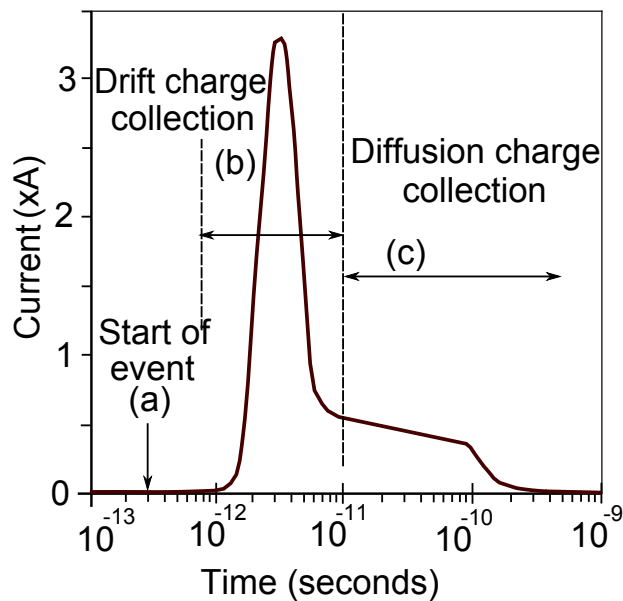
Figure 2.9: Transient current pulse that generated on a sensetive node due to a strike by a charged particle[11].

2. A single event upset (SEU) is a transient event which can be generated directly if the ionization ion hits a sensitive junction in a memory cell or a flip-flop, or it may occur as a result of the propagation of an SET [6]. If an SET generated in a combinational block has sufficient magnitude, it may propagate through a logic path and it might be latched by the next flip-flop or the memory cell and cause a bit flip. This flip is called an SEU [4], which eventually causes a soft error.

2.8 SINGLE EVENT TRANSIENT PROPAGATION

As mentioned in the last section, the interaction between a neutron particle and a semiconductor device in a combinational circuit may generate an SET. This SET may propagate through the combinational block to be latched and cause an SEU or it may be suppressed. There are three masking effects

which may prevent the generated SET from causing a soft error. Logical and electrical masking effects are related to the circuit topology and latching window masking which depends on the latching time of the output flip-flop.

1. The logical masking effect is considered to be one reason to prevent the propagation of glitches through combinational circuits [40]. This type of masking depends on the type of gates that construct the propagation path. This effect may occur on some gates, such as NAND, NOR, AND and OR, depending on their sensitivity to the faulty input line. However, this masking effect cannot happen in other gates, such as NOT, XOR and XNOR, because these gates are always sensitive to any change which occurs in their input lines. A gate is sensitive if any change in the input affects the output of the gate (the output of the gate is dependent on that input) [91]. For example, in a NAND gate has both inputs at logic-1, in this case the gate is sensitive to both inputs, and so if a glitch reaches this gate through any one of these inputs it will propagate and appears in the output of the gate. On the other hand, if both inputs of this gate are at logic-0, in this case the gate is not sensitive and any glitch arrives at one of the gate's inputs will be masked and will not appear in the output of the gate.
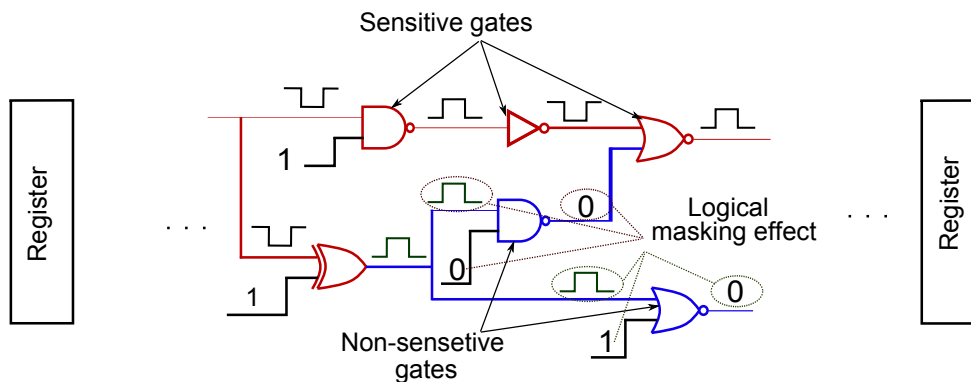
Figure 2.10: The red gates are sensitive, so any glitch arrives to one of their inputs it will propagate. The blue gates are non-sensitive gates, so they have the ability to block the propagated glitches.

Different SETs are shown in Fig. 2.10, some of which are masked and some are propagated depending on the type of propagation gate and its input values.

2. An SET might be attenuated before reaching the output of the combinational block. This effect is called electrical masking [21, 93]. This kind of masking occurs during the propagation of a generated glitch through the gates of a combinational circuit. It occurs as a result of the inertial delay of the gates (the transition time). So, if the propagated glitch does not have sufficient
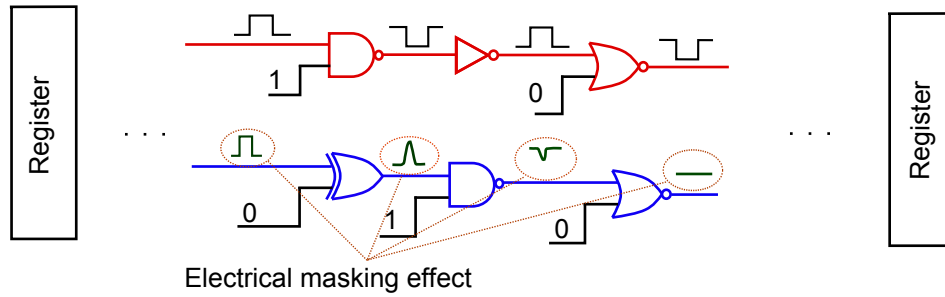
Figure 2.11: Electrical masking that occurs on some gates and attenuates the narrow pulses.

amplitude and duration, it will be attenuated; and sufficient duration here means that the duration of the propagated glitch should be longer than the inertial delay of the gate, otherwise the glitch will be attenuated [13, 37, 120]. This effect increases in slow stages or at sub-threshold voltages where the circuit works at a slow pace.

As reported in [86, 127], when a glitch with duration t_{dur} is propagated through a path and reaches an input of a gate G whose delay time is t_{del}, the propagation scenarios are governed by the relationship between the duration of the propagated glitch and the time delay of the gate as follows:

1. If $t_{dur} \leqslant t_{del}$ the glitch will definitely be masked and will not propagate through the gate.

2. If $t_{del} < t_{dur} \leqslant 2t_{del}$ the glitch propagates through the gate, but the duration and the amplitude of the glitch at the output of the gate are less than its original duration and amplitude. So, in this case, the propagated glitch is attenuated, and it will be masked after propagating through several stages.

3. If $t_{dur} > 2t_{del}$ the glitch will be propagated through the gate without any attenuation.

In general, of all logic gates, the XOR and XNOR gates have the strongest electrical masking effect due to their size [96]. The electrical masking effect caused by some slow gates which affects narrow pulses generated in prior stages is illustrated in Fig. 2.11.

3. The third masking effect is the latching window masking effect. This type of masking related to the sequential part of the system where the generated SET can be registered as an SEU. This masking effect occurs when the propagated glitch does not match the timing of the latching window of the output flip-flop, so that it reaches it before or after the latching window [70, 77]. It is known

that the latching widow consists of the setup time and the hold time. Thus, the duration of the propagated glitch should be wider than or equal to the summation of those times. Narrow glitches may arrive at the right time for the latching window, but may not be latched up due to their short duration [25].
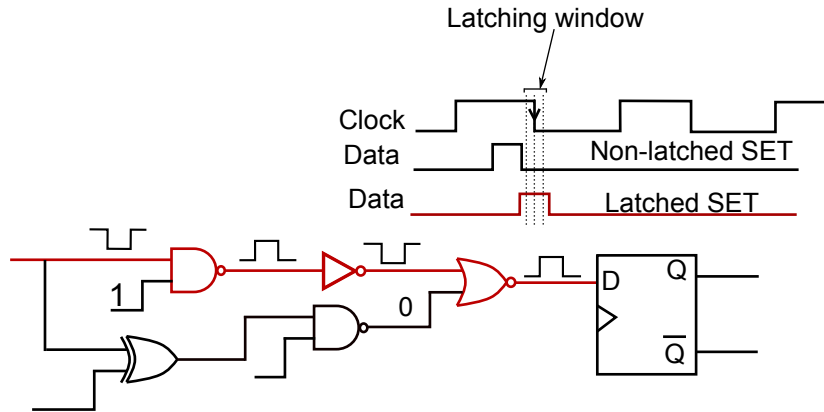
Figure 2.12: Latching window masking that occurs at the sequential part of the system, when the glitch misses the setup and hold times of the flip-flop.

Latching window masking is illustrated in Fig. 2.12, and it can be seen that the SET propagated from the combinational block arrives at the input of the output flip-flop at a certain time. Depending on this arrival time, the glitch may or may not cause an SEU.

2.9 RELATED WORK

Since 1990, soft errors in combinational circuits have been considered to be a significant concern for the reliability of commercial electronics, and so research has been carried out to investigate the effect of radiation on ICs [38]. The scope of this work is to predict the reliability of combinational circuits using analytical techniques. We have targeted the useful period of the circuit's life cycle, as in this period the faults occur as random events because of the randomness of their cause. So, we can eliminate the reliability concerns that result from manufacturing issues. This section describes the techniques that are used to estimate the reliability of combinational circuits and other techniques in the area of the analysis of soft error rate (SER). In this work, we evaluate the reliability of combinational circuits and exploring changes in terms of the voltage that is applied to the circuit. In other words, this study explores the trajectory of reliability when different parameters change

in order to determine how these changes affect the reliability of a circuit under test (CUT).

2.9.1 *Reliability Evaluation Techniques*

Analysing the reliability of digital circuits computationally could be an expensive approach. Therefore, most of the researchers suggest dealing with this problem using analytical or numerical techniques [49, 134].

The probabilistic transfer matrix (PTM) method [105] is used to evaluate the probability of errors at the gate level of abstraction in the presence of transient errors such as soft errors that caused by alpha particles. The main idea of this method is to use a matrix to represent the behaviour of the circuit, and the input values of the circuit are represented by column indices and the output is represented by the row indices. In order to do this, each gate in the circuit needs to be represented by a PTM matrix. An incorrect output is represented by p in the matrix and a correct one is represented by $1 - p$. The PTM matrices of some logic gates are shown in Fig. 2.13.
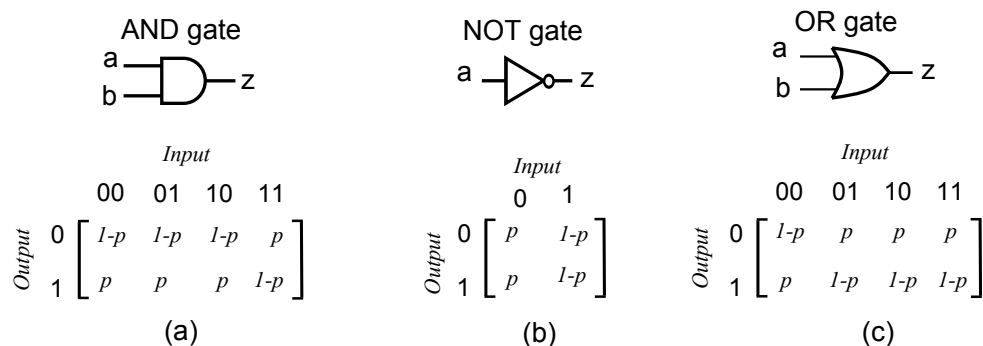
Figure 2.13: Probabilistic transfer matrices of logical gates: (a) AND gate, (b) NOT gate, and (c) OR gate. The symbol p represents an incorrect output of a gate [105].

After finding all PTM matrices of all gates, the PTM of the whole circuit can be found by taking into account the topology of the circuit, so that the inner product is used with serial composition and the tensor product is used with parallel composition. Based on this concept, a computational frame using algebraic decision diagram (ADD) has been developed in [69] to remove the redundant rows or columns in the PTM matrices. This reduces the complexity of the method in order to be applied to the evaluation of the reliability of large circuits. Also, the PTM method has been used as a basic approach in

[15, 102, 119, 133, 136]; however, each adds a specific technique to be used in a certain way. The PTM method is considered a simple approach for use in evaluating the reliability of a circuit; however, it has some drawbacks. For example, the masking effects are not considered, so the reliability of each gate is evaluated regardless of logical and electrical masking effects. Ignoring such effects may cause an overestimation of the circuit's reliability by a factor of 25X in the case of a circuit tree with a logic depth of 7 [137]. Also, when evaluating a circuit's reliability in the presence of soft errors caused by neutron particles, the rates of those particles should be taken into consideration.

The signal probability reliability (SPR) method [45] has been used to evaluate the reliability of combinational circuits in [16, 50]. Analysing logic circuits using input signal probabilities is an old technique mentioned in [104]. This method is a simplified version of the PTM method which avoids the use of intermediate PTM matrices. The basis of the SPR method is to use signal probabilities and the propagation of these probabilities along the cells of the circuit under test. The idea of this method is that each gate output can be described in terms of a four-state signal probabilities matrix, and signal reliability is embedded explicitly in this matrix. For example, consider the following matrix which represents the probabilities of four states of a gate output signal:

$$
P_{2\times2}(\text{signals}) = \begin{bmatrix} P(s = \text{correct } 0) & P(s = \text{incorrect } 1) \\ P(s = \text{incorrect } 0) & P(s = \text{correct } 1) \end{bmatrix}
$$

This matrix can be obtained by multiplying jointly the inputs probabilities signals and the transfer function of the gate. The reliability of a circuit can be found by multiplying the reliability of individual output signals. The drawbacks of this method relate to dealing with reconvergent signals and scalability [41], and so the problem of the complexity of the circuit is not solved by the reference approaches.

2.9.2   *Soft Error Estimation*

SER techniques are used to estimate the susceptibility of circuits to soft errors caused by radiation effects. failure in time (FIT) is used as a measure to quantify the estimated number of failures, and one unit is equivalent to one error per billion hours of circuit operation. Proposed approaches can be classified as *Analytical approaches* and *statistical fault injection approaches*.

Analytical approaches are developed to tackle the scalability problem at the circuit level of abstraction. However, using models to represent the transient pulses which are generated and propagated in a circuit affects the accuracy of the evaluated SER [20].

Various symbolic methods based on binary decision diagram (BDD) and algebraic decision diagram (ADD) have been proposed by the authors of [3, 18, 53, 85, 86, 87, 106, 107, 108, 137, 139]. In these approaches, descriptive models are used to represent the generated transient pulse, and in most of them it is described as a trapezoidal shape with different rise and fall times. To model the propagation process, mathematical models are used to implicitly include the effects of logical masking and electrical masking effects . Using such approaches the time taken for the estimation of the SER is reduced dramatically, especially for large circuits. However, the estimated results are inaccurate due to the use of modelling approaches. It is difficult to characterise a generated SET using a model because it depends on the characterisation of the struck node. So, modelling this pulse using a trapezoidal shape either underestimates or overestimates it. Also, when this SET propagates through a circuit, its shape changes depending on the circuit topology and the type of cells through which the pulse is propagated. So, in some topologies, the propagated pulse suffers from attenuation and when it reaches the output of the circuit it is narrower than the original pulse. However, in some topologies, the propagated pulse suffers from broadness in duration and reaches the output of the circuit wider than it was originally. This is known as propagation-induced pulse broadening (PIPB) [130]. This effect depends on the polarity of the generated pulse. Moreover, some of the proposed techniques use circuit partitioning to parallelize the estimation process in order to decrease processing time, but this technique is not applicable for all digital circuits and it is not possible at all in cases of correlated signals. So, with all the time that is saved in the estimation process, these approaches still suffer from a lack of accuracy.

Other authors [57, 77, 110] have used different current source models to inject the transient current pulse using a single-exponential model or double-exponential model. Regardless of their accuracy using these models leads to an increase in SER accuracy compared to the approaches mentioned in the previous section. Here, the SER of a circuit is calculated by finding the summation of the SERs of all sensitive nodes in the circuit. For each sensitive node, the SER is calculated by finding the probability of the logical, electrical, and latching-window masking effects that affect any generated

pulse at this node. Although the time taken to estimate the SER is reduced using these approaches, they still lack of accuracy because of the employment of mathematical models to simulate the three masking effects. Adifferent a SER analysis method has been designed which uses a parametric waveform model based on the Weibull function to describe a particle strike in [110]. In a further method for analysing and measuring SER in combinational circuits [31], a framework was proposed to estimate soft errors at three levels. At the device-level, the generation of the fault was modelled using TCAD simulation, and then at the gate level, a propagation model simulated the masking effects. An emulation-based platform was subsequently used at the application level to find the contribution of each part of the system under test to the overall SER.

Meanwile a contrasting proposal for an SER estimation technique comprises of two phases of characterisation and propagation introuecd in [77]. In the characterisation phase, a transient pulse is generated using a double-exponential current source model injected into a node and simulated using the HSPICE simulation tool. The characterisation of the SET is stored in lookup tables, and this phase is performed only once for each technology node. The second phase is the propagation phase, in which the propagation of the SETs from the faulty node towards the output flip-flop is described using a propagation algorithm. In this algorithm, the three masking effects are included using a lookup table function so that each node has own generation LUT and propagation LUT. The SER is estimated depending on the results obtained from the propagation phase. An approach was proposed in [52] to estimate neutron-induced SER by incorporating a machine learning technique with monte carlo (MC) radiation simulation. The authors used MC simulation to obtain information about secondary ions and their deposited charge. The machine learning discriminator is used to distinguish whether or not an ion with a certain amount of energy can upset a cell, and it is fed with data collected using a TCAD simulation. This data is obtained by injecting different ions with different amounts of energy into a cell to identify the energy required to upset that cell.

Statistical fault injection approaches have been proposed to estimate the SER of combinational circuits, some of these approaches are proposed in [32, 58, 74, 94, 99, 103, 138]. In [32, 58, 138] the authors proposed a MC simulation-based technique to calculate the SER of a circuit by combining the MC simulation code proposed in [68] with a 3-D TCAD simulator to build models of particles transfer and collision. The particle energies used

in the proposed technique are sampled from the range 1 MeV to 1 GeV, obtained according to Joint Electron Tube Engineering Council (JEDEC) standard. Alternatively, a MC simulation was used to build models representing the generation and propagation of a transient pulse in [74]. Quasirandom sequences proposed in [90] were used for sampling points rather than using the rand() function. The advantage of using this type of sequence is that evenly scattered sampling points throughout the selected space can be obtained. Eventually, these samples are used to build a lookup table containing all SET details. Then, the error rate is calculated using an analytical technique by finding the summation of the computed SERs of all nodes in the CUT.

In another study [94] the MC simulation technique was used to verify the experimental results obtained from physical experiments conducted using accelerated high-energy neutron tests at the Weapon Neutron Research test facility, Los Alamos Neutron Science Center, USA. The authors of [99] used an approach to estimate SER exploits a nuclear database of neutron-silicon interactions that is built using MC simulation. Also, a MC code is used to identify the sensitive zones in a circuit and to generate a list of transient current pulses.

Other researchers have proposed an SER analysis framework to estimate the SER in the presence of single event multiple transient (SEMT) and SET in combinational circuits [103]. The SEMT occurs when a particle strike causes more than one transient pulse due to technology downscaling. For each node, the effects of the three masking mechanisms are modelled and incorporated into the calculation process. The problem of circuit complexity is tackled by dividing the circuit into sub-circuits of different grids, where each grid contains a group of gates and flip-flops. Then the proposed tool is applied to each grid to estimate its SER. Eventually, the overall SER is calculated by summing the SERs obtained for all grids. In this approach, the authors claimed that acceptable accuracy in the results was obtained after 10,000 simulation runs.

Statistical approaches using MC simulation are preferred by some researchers, even though they are time-consuming approaches to achieve reasonable accuracy. However, in some cases, especially if the circuit under test is used in critical applications, the extra time that is taken to estimate reliability is justified.

The use of digital simulations in evaluating the reliability of a circuit does not consume much time and the results can be obtained in a matter of seconds. However, because of the use of models to describe some effects, the

results may suffer from inaccuracies. On the other hand, although using MC simulations is a time-consuming process, the results obtained are accurate. In this work, we propose a method for evaluating the reliability of combinational circuits using analogue simulations. This method is slower than methods that use digital simulations. However, the accuracy is higher, and the results can be obtained quicker than the approaches that use MC.

2.9.3   *Reliability Improvement in Combinational Circuits*

The effect of soft errors on combinational circuits has been eliminated at several levels of abstraction using different traditional methods. In general, these methods focus on enhancing masking mechanisms in order to prevent the propagation of such errors.

At the architectural level, soft errors are detected using software redundancy. Redundant multi-threading (RMT) is a proven method which is built by running multiple threads for the same program, and the results of those threads are compared. If an error is detected, the program is rolled back to a checkpoint to rerun the instructions from that point [71].

At the logic level, hardware redundancy is used to mitigate errors. The most well-known technique is N-modular redundancy (NMR), where N-copies of a circuit connected in parallel perform the same function and the outputs of those copies are connected to a majority voter circuit which chooses the correct output. Usually N=2 or 3 modular, forming dual-modular redundancy (DMR) or triple-modular redundancy (TMR). The cascaded triple modular redundancy (CTMR) method was proposed by John von Neumann in [124]. In this method, unreliable components can be triplicated and connected in parallel to a majority voter, where each component contains triplicate circuits and a voter. The drawback of the hardware redundancy technique is the area overhead because of the duplication or triplication of the circuit, and the area of this type of circuit increases two or three times. As result, the energy consumption of the circuit increases too.

At the circuit level, the gate sizing technique has been suggested to mitigate soft errors, where increasing the size of the transistors in a gate increases the conductance of that gate and as a result the restoration current increases. Also, increasing the transitors' size increases the gate's capacitance, which leads to the increase of its Q_{crit}. To decrease the area overhead, the designers of some techniques suggest choosing the most susceptible gates in the circuit

and to modify their sizes in order to harden them and make them more reliable [75, 106, 140]. These techniques have some drawbacks, such as the area overhead in the circuit and extra energy consumption.

Razor technique has been introduced in [33] to eliminate soft errors by using a delayed clock to detect timing errors that are generated because of the voltage scaling, and it can be used to detect soft errors too. However, this technique has a limited ability to detect such errors due to the duration of some SET pulses. Narrow SETs cannot be detected because their duration is less than the difference between the two clocks that used by Razor. Also from a power consumption perspective, short paths need in some cases to be delayed to prevent the reading of the short paths' next signal as a present signal, and so buffers have to be used to make sure that those signals arrive at the right time. These buffers consume extra power, which may lead to the use of Razor technique to be impractical in some circuits because of the trade-off between low power consumption due to supply voltage scaling, and the extra power consumption caused by the extra buffers. Also, in the case of detecting SETs or SEUs, if these events occur in the shadow latch, the correct data will be replaced by erroneous values [101].

Different on previous work, we propose a filtering technique based on creating a long transition region at the end of a circuit's paths to attenuate short glitches. This technique is implemented by two different structures. The first structure is changing the size of last stage in the path. The second structure is adding an RC filtering circuit at the end of the path. More details on these structure and their effect on the circuit parameters are introduced in Chapter 5

2.10 CONCLUSIONS

In this chapter, a concise background of the radiation environment has been given, explaining how neutron particles are involved in generating soft errors in combinational circuits. The mechanisms of the generation and propagation of an SET are covered in two separate sections due to the importance of this topic in providing a rationale for studying this kind of errors. Relevant work is reported in the last section of the chapter to give a brief background concerning research carried out so far. However, the focus here was on approaches that are concerned with soft errors generated in combinational circuits; that is SETs. Thus, this chapter has provided the background necessary to understand

the nature of soft errors and the effect of neutron particles in digital circuits, paving the way for the following chapters.

DERIVATION OF RELIABILITY

This chapter presents the core idea of the proposed method and how the approach can be applied to a combinational circuit in order to estimate its reliability. For the sake of simplicity, the approach is manually applied to small circuits to explain the main steps in estimating the reliability metric of a circuit. These circuits are two single-path circuits and one simple multipath circuit. The first single-path circuit mimics any individual path that can be taken from a large circuit. The second is a carry path extracted from the international symposium on circuits and systems (ISCAS) c6288 benchmark (16 x 16 multiplier), which is constructed from different logic gates to see the effect of the diversity of cells on a circuit's reliability. The third circuit represents multipath circuits, and is a 3-bit adder which has 7-inputs and 3-outputs and is constructed using 125 gates.

3.1 MODELLING THE TRANSIENT CURRENT PULSE

In order to estimate correctly the error probability in combinational circuits in terms of soft errors caused by neutron particles, we need to choose an accurate model of such an effect. Various models have been introduced for this purpose. For example, Messanger in [84] developed an approximate analytical solution. Wirth in [132] also introduced a mathematical model to predict and explain the relationship between a transient current pulse generated in a device and the radiation dose deposited into that device. However, the double-exponential model is the model most commonly used by soft error researchers in simulation-based experiments due to its simplicity of incorporation in a simulation session. Various authors have used this model in experiments to approximate the transient current pulse generated in digital ICs [56, 79, 110, 126, 128, 129, 139]. In such experiments, a transient current pulse is injected into a CUT to observe the rate of soft errors at the output of the circuit [72].

The double-exponential function used in the double-exponential current source is presented as follows [14]:

$$I(t) = \begin{cases} 0; & t < td1 \\ I_{peak}\left(1 - e^{\frac{-(t-td1)}{\tau1}}\right); & td1 < t < td2 \\ I_{peak}\left(e^{\frac{-(t-td2)}{\tau2}} - e^{\frac{-(t-td1)}{\tau1}}\right); & t > td2 \end{cases} \tag{3.1}$$

In (3.1) the current waveform can be divided into two parts. The first part starts at $td1$, which is the rising part of the waveform, and it continues until $t = td2$. The second part starts at $t > td2$, which is the falling part of the waveform. The rising time is defined by $\tau1$, and the falling time is defined by $\tau2$. I_{peak} is the maximum value of the current pulse.

The main disadvantage of using the double exponential current source is its inaccuracy in representing the physical response of a device. So, if a transient current pulse generated using this model is injected into a digital circuit, it causes a drop in the output voltage of the faulty node. However, this drop may exceed $Vss=0$ V to the negative side, as shown in Fig. 3.1, which leads to an accelerating discharging of the charge deposited in the faulty node at a higher rate compared to the physical response of the struck node. This behaviour is not an accurate simulation of the physical response of the circuit because, in real cases when a particle hits a sensitive junction (usually a reverse-bias junction) in a transistor in a digital circuit, the electrical field across the struck junction collapses due to the decrease in voltage and the glitch generated at the output stops at $Vss=0$ V [14]. As a result, the prompt charge collection process is terminated and the deposited charge takes longer time to be completely discharged from the circuit. This slow discharging process leads to the generation of a longer SET [65]. Overdrive behaviour occures in models that implemented independently on the voltage of the struck node [14, 44]. However, this model can be considered a valid approximation in the cases of low values of LET [14, 24, 35, 65, 111, 123].

3.1.1 *Bias-dependent Current Model*

In this work, a model introduced in [80] and developed in [64] is used. This model is built by performing a 3-D device physics simulation simultaneously with simulation program with integrated circuit emphasis (SPICE) analysis as
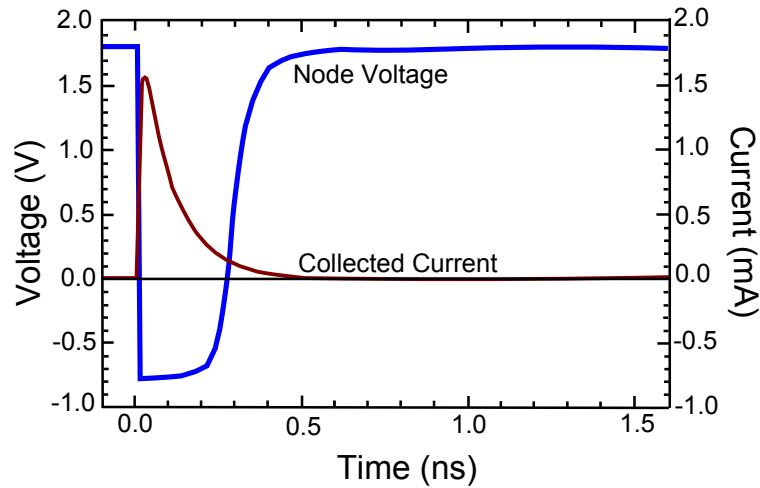
Figure 3.1: The response of a faulty node to a transient current pulse generated by double exponential current model [80]

a fully coupled mixed mode. The behaviour of the simulated current pulse is implemented in such a way as to be very realistic and to follow the physical response of the struck node. This response is illustrated in Fig. 3.2. As can be seen in the figure, the node voltage decreases immediately after the charge collection has begun. So, the response of the faulty node stops at V_{ss}=0 V, due to the collapsing of the electric field of the junction. By comparing the response of the faulty node in Fig. 3.2 with the response introduced in Fig. 3.1, it can be clearly noticed that the transient voltage pulse generated using the bias-dependent current model lasts for longer than the pulse generated using the double-exponential current model. This is due to the differences in discharging rates in the two cases.

The implementation process of this model can be divided into two phases. The first phase is used to model the prompt response of the ionization process. So, this part simulates the pulse caused due to the drift charge collection, and it is responsible for the spike in the current pulse. The second phase is used to model the recombination mechanism. So, this part simulates the pulse generated because of the diffusion charge collection, and it is responsible for the long-taieled pulse (the plateau part). The system of equations that describe this model can be found in [64] and [65].

Transient current pulses are generated at different values of LET and a fixed value of Vdd at 1V using the bias-dependent current source model illustrated in Fig. 3.3(a). As can be seen in the figure, the current pulse is divided into two regions. In the first region, the instant response of the device is represented by a spike pulse which has different peak values depending on the LET value.
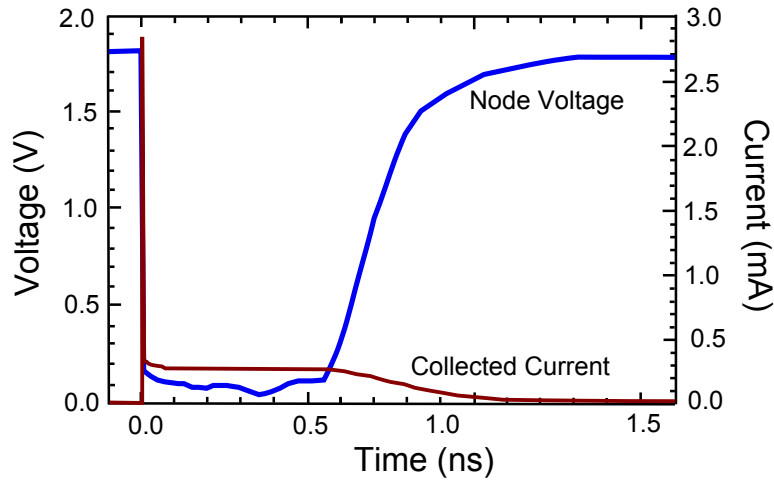
Figure 3.2: Response of a faulty node to a transient current pulse generated by mixed-mode device physics simulation [80].

So, a higher LET value generates a higher amplitude of spike pulse. This spike pulse is intended to simulate the effect of drift charge collection. The other region of the pulse is the plateau region, which is longer than the first one and has a constant magnitude for different values of LET. This is because, in this part of the pulse, the LET affects the duration of the pulse. So, it is obvious that a higher LET value generates a longer pulse duration. This part of the current pulse simulates the charge diffusion phase. The duration of the SET generated in a faulty node is proportional to the duration of this part of the transient current pulse [24].

Transient current pulses generated at different values of Vdd and a fixed value of LET=50 $MeV.cm^2/mg$ using the bias-dependent current source model are illustrated in Fig.3.3(b). As can be seen in the graph, the amplitude of the transient pulse changes according to the value of Vdd. This is expected, because the amount of the collected charge is proportional to the potential of the struck junction [46]. This is one of the advantages of this model, as the amplitude of the generated current pulses is correlated with the voltage applied to the struck node.

3.2 THE PROPOSED APPROACH

We propose a method for evaluating the reliability of combinational circuits without using the time consuming MC simulation tool or expensive physical experiments. This method uses two levels of characterisation: a stochastic
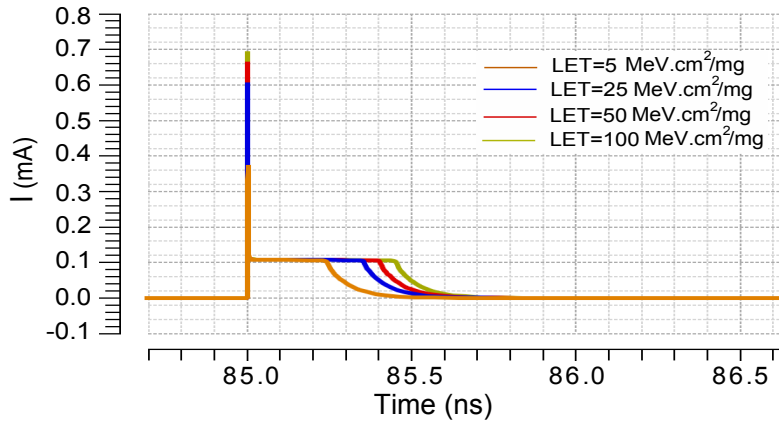
(a) Transient current pulses generated at different LET values and Vdd=1V
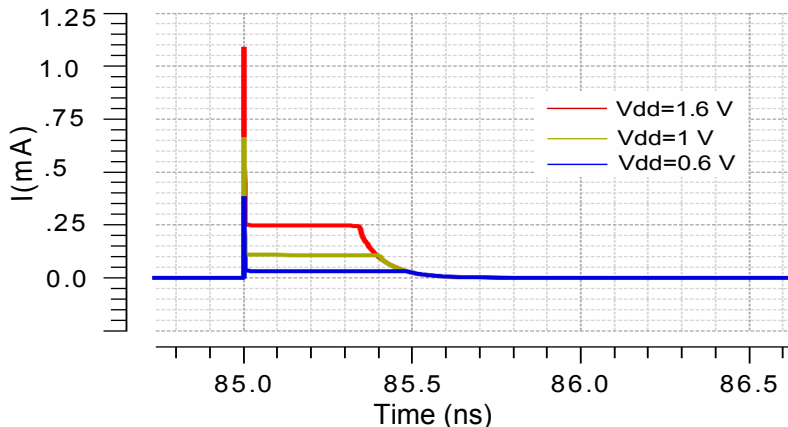
(b) Transient current pulses generated at different Vdd values and LET=50

Figure 3.3: Transient current pulses generated using bias-dependent current model.

fault model (SFM) of the component library and a design-specific critical vector model (CVM). The idea is to move the high-complexity problem of the stochastic characterisation of parameters into the generic part of the design process, and do it just once for a great number of specific designs.

The SFM captures variations in the parameters of a library component with regard to the interference causing transient faults at the component output, and is meant to be obtained at the design time, similar to timing library files. It may include a probability density function (PDF) of the particle energy and a model of the generated transient current pulse as a function of the neutron energy. Its purpose is to represent the cause of faults, and so it is fixed and applicable to any design or system under test. The stochastic fault model (SFM) possibly expressed in non-electrical terms (for example, particle energy distribution), or as electrical effects (for example, a voltage pulse at a gate output with its magnitude, duration and arrival time described

stochastically). The parameters of the electrical effects form a parameter vector (PV) used further in the derivation of the critical vector model (CVM).

The CVM is derived from a limited number of simulation runs on the specific design, and it represents the boundary between the erroneous and error-free operation, w.r.t. the PV. In the above example, the PV includes the shape (a function of LET) and arrival time of a voltage pulse. A number of analogue simulations are performed to determine the LET-time pairs representing boundary conditions between error and no error at the primary output.

Finally, the probability of error-free operation is calculated by combining the SFM and CVM as a probability of the PV not reaching the critical values of CVM.

3.3 UNIFORM SINGLE-PATH CIRCUIT

A long chain of inverters intended to mimic a single path through an arbitrary logic circuit is used as a part of a digital circuit operating under voltage-frequency scaling. Frequency is chosen as a performance metric. It is determined for each value of Vdd applied to the circuit, by simulating the circuit and measuring the propagation delay, with no margins added. The circuit includes 205 identical inverters implemented with united microelectronics corporation (UMC) 90 nm foundry design kit. All transistors are 80 nm in length (which is standard for this library), the pull-down transistor is 400 nm, and the pull-up is 800 nm in width (these values are similar to those used in a commercial standard-cell library), with standard threshold voltage and standard Vdd=1 V. Between the inverters there are wires whose parasitic capacitance we simulate as 2 fF capacitors (which is typical capacitance of a short interconnect wire). The schematic view of this circuit is shown in Fig. 3.4.
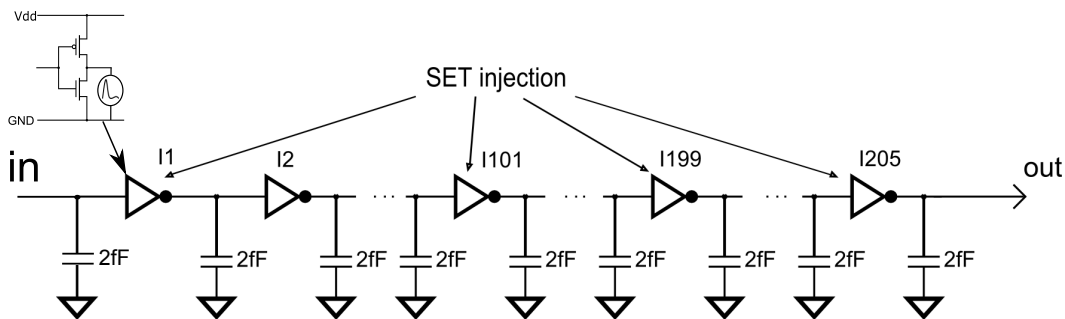
Figure 3.4: Chain of inverters circuit.

In order to estimate the reliability of this circuit, a transient current pulse is generated using the bias-dependent current source model and injected into a single gate in each simulation run (e.g., the left inverter I1 in Fig. 3.4). Examples of SET pulses in a single strength inverter under two different Vdd values of 0.4 V and 1 V and a range of LET values can be seen in Fig. 3.5 . In this model, the particle energy is expressed as a metric of LET; this is because we are interested not in the energy of the particles, but rather the effect of their interaction with the transistor.
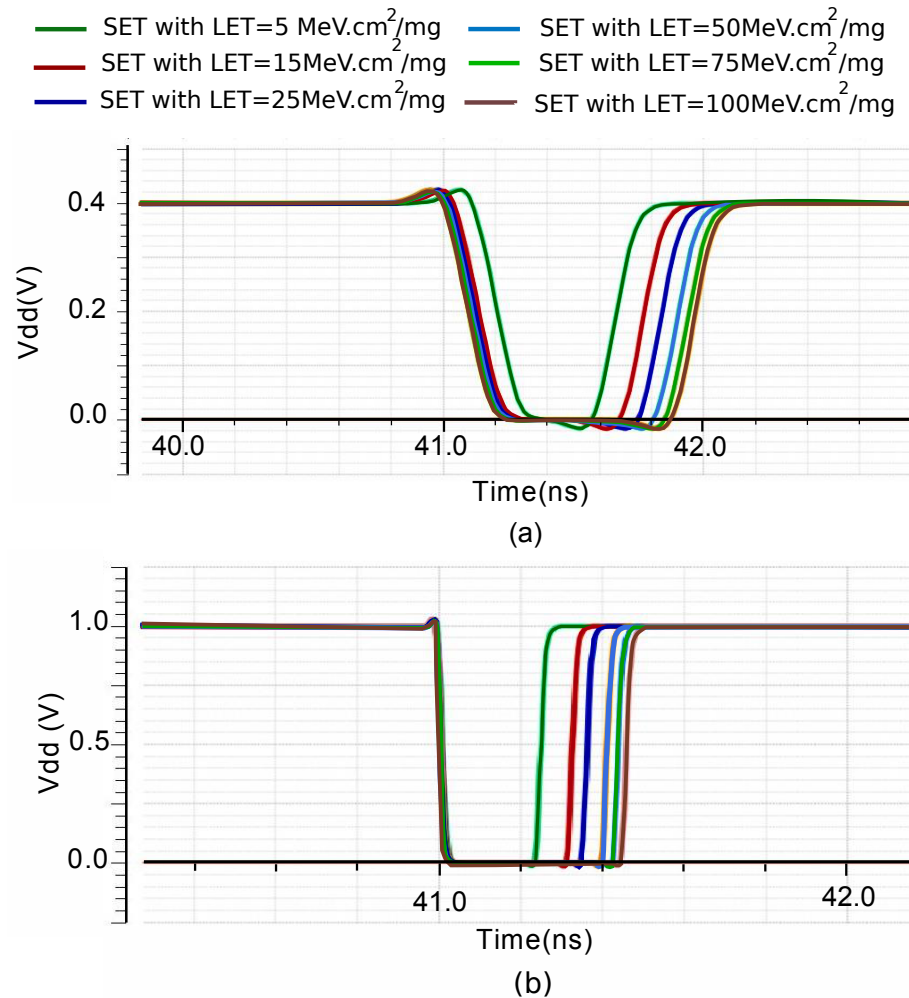
Figure 3.5: A family of SET pulses registered at the output of the circuit for different LET values. (a) at Vdd = 0.4 V, (b) at Vdd = 1 V

3.3.1 *Evaluating the Reliability of Chain of inverters Circuit*

In this section the main steps for deriving the reliability of the single-path circuit are described, where the SFM is converted into a value of reliability according to the properties of the circuit (expressed as CVM). The first objective of this stage is to determine whether or not an SET would cause an output error in the whole circuit comprising multiple gates (a long chain of inverters in our example) or not. The second objective is to calculate the probability of error-free operation, or reliability.

An output error is defined as an SEU, when an SET is latched by a flip-flop connected to the output of a combinational circuit [14, 116, 120]. The difficulty here is that not all SETs result in SEUs. Some SETs disappear before the clock signal or appear too late w.r.t. it. Furthermore, the magnitude of the SET may be below the threshold of the flip-flop sampling, or its duration may be insufficient to be latched. Also, it may disappear while propagating through the path due to inertial delay behaviour exhibited in individual stages, leading to suppression of pulses of short duration. For an SET to be registered as a soft error, it should arrive at the same time as the rising edge of the clock with a magnitude in excess of Vdd/2. This is illustrated in Fig. 3.6. An early particle strike causes a glitch in a circuit, and this glitch propagates and arrives early before the rising edge of the clock. So, this glitch does not cause soft error. The same is the case if a particle hits the circuit and causes a glitch which arrives after the rising edge of the clock.
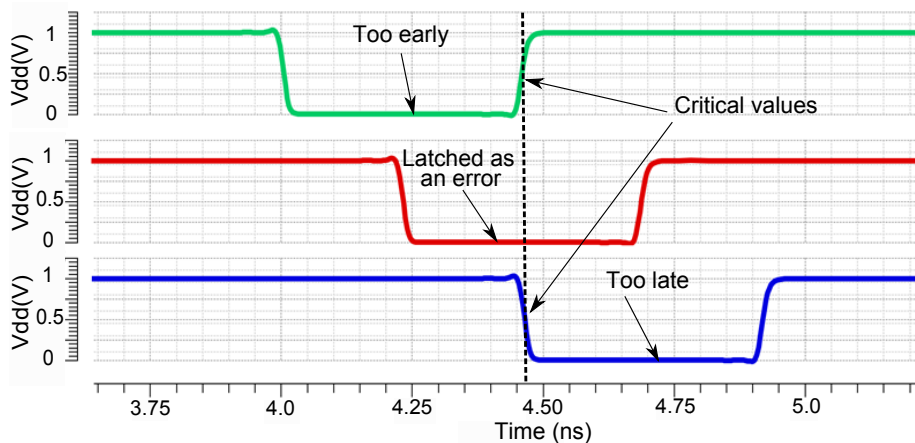
Figure 3.6: Different glitches arrived on different times.

The first objective is achieved by identifying the PV (in this experiment it is an SET characterised in terms of two parameters - the LET and arrival time)

and simulating the circuit in order to determine the critical values of this vector (PV values causing a transition at the end of the clock cycle).

The critical values of the interference vector in the case of an SET injected in stage number 101 at Vdd=1 V, are illustrated in Fig. 3.7. These critical values determine the boundary line that separates the error and no error zones. The clock period defined as a propagation delay without any margins is T=4.06 ns. It is easy to adjust the results to any timing margins used in a particular design. For the other stages in the path, the diagrams are very similar but shifted left for low stage numbers and right for high numbers. For example, the error zones of stages 1 and 205 in Fig. 3.7 show the difference between the error zones of the three stages.
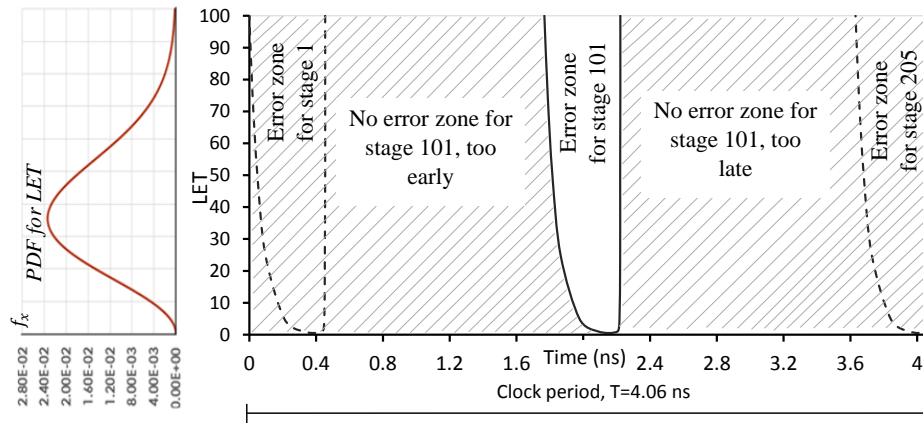
Figure 3.7: Critical values of the interference vector.

The second objective is achieved by using the graph in Fig. 3.7 to calculate the probability P_{err} of the circuit being in the error zone. For this, we use the PDF f_x for the LET value x and the PDF f_t for the SET arrival time t. The former is known from the fault model and the latter has a uniform distribution due to the asynchronous nature of SET events. The value of P_{err} in (3.3) is calculated for a single clock cycle, where the clock period is adjusted to the propagation delay for each Vdd value. The PDF are for the clock cycle where an SET took place, but in real cases the SET does not occur in every clock cycle and so it needs to be multiplied by the rate of neutron particles in one clock cycle.

$$P_{err} = \frac{\iint_{error\,zone} f_x(x).f_t(t)\,dx.dt}{\int_{t=0}^{T} \int_{x=0}^{\infty} f_x(x).f_t(t)\,dx.dt}.T.r_{SET}. \tag{3.2}$$

Note that the PDF of the arrival time is a constant; that is, $f_t(t_a) = 1/T$ where T is the clock period. The the rate of neutron particle (r_{SET}) is a constant

representing SET rate. Instead of the infinite integration limit for x, we choose a value of 100, since the probability of exceeding this limit is negligible [19].

The denominator in (3.2) is equal to 1 because the integration is for the whole clock period and the whole energy range. So, (3.2) can be simplified to:

$$P_{err} = \int_{t=0}^{T} \int_{x=0}^{x=100} Z(x,t).f_x(x).f_t(t)\ dx.dt.r_{SET}, \tag{3.3}$$

where $Z(x,t)$ is the error zone function which can determined as:

$$Z(x,t) = \begin{cases} 0 & \text{outside the error zone} \\ 1 & \text{inside the error zone} \end{cases}. \tag{3.4}$$

The integrals in (3.3) are computed numerically because $Z(x,t)$ is determined through simulation. The PDF of LET in Fig. 3.7 is defined according to the Maxwell-Boltzmann formula:

$$f_x(x) = \sqrt{\frac{2}{\pi}}.\frac{x^2 e^{-x^2/(2a^2)}}{a^3}, \tag{3.5}$$

where $a = \frac{\mu}{2}\sqrt{\frac{\pi}{2}} \approx 25.06$

This is for the probability of error when an SET is injected into any single stage in the path. The overall error probability of the path is calculated by summing the error probabilities of all individual gates. For low SET rates it is reasonable to assume that no more than a single SET can take place in the path in any particular clock cycle, which means that the (3.3) is applicable to the path error, and r_{SET} becomes the SET rate in the path.

The reliability of the circuit is calculated as the probability of the absence of an error, i.e. $P_{reliability} = 1 - P_{err}$.

3.3.2   *Results*

The proposed method is applied to the CUT for a range of values of Vdd to explore how the trajectory of reliability changes with supply voltage. The error probabilities are calculated for individual gates as shown in Fig. 3.8 where the SET rate was chosen as r_{SET}=20 n.cm^{-2}.h^{-1} [6]. By comparing the error

probability of the first inverter with that of the 199th inverter, we can find that there is a slight difference between these probabilities. So it is sufficient to calculate the error probability of one gate and multiply it by the number of gates. However, in the case of gates located near the output, their error probabilities differ at very low voltages. So, they need to be calculated in order to obtain accurate results. It is interesting that the probability of error at the last stage is lower than those of the prior stages. This is because glitches generated in prior stages suffer from broadness, especially those generated with high LET values [34]. This broadness increases the probability of these glitches being latched by the output flip-flop. However, there is no path attached to the last stage, and hence any glitch generated in this stage would not be affected by this broadness, and a lower error probability results.
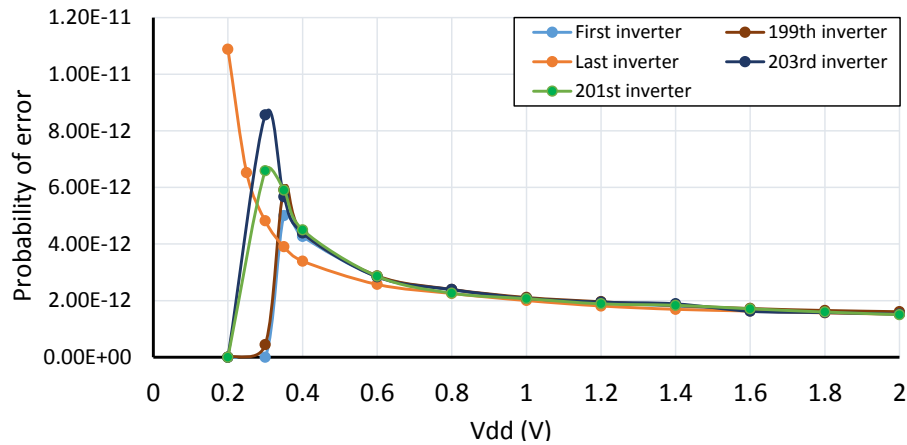
Figure 3.8: Error probability of different single stages vs Vdd.

Note that in these diagrams error probability is calculated per single clock cycle rather than per seconds of operation. This metric is relevant to the completion of fixed computational tasks. The overall error probability of the circuit is calculated by combining the error probabilities of all gates in the path as illustrated in Fig. 3.9.

A three-way trade-off between reliability, energy and performance (REP) is depicted in Fig. 3.10, which is one of the main contributions of this work. The circuit performance represents the frequency that is calculated at particular Vdd values. The energy that is consumed by the circuit is calculated by integrating the total power per one clock cycle. This figure can be divided into three regions. The first region is above the nominal voltage, where the circuit reliability and performance improve slightly versus an extreme increase in energy consumption. In the second region below the nominal voltage, where
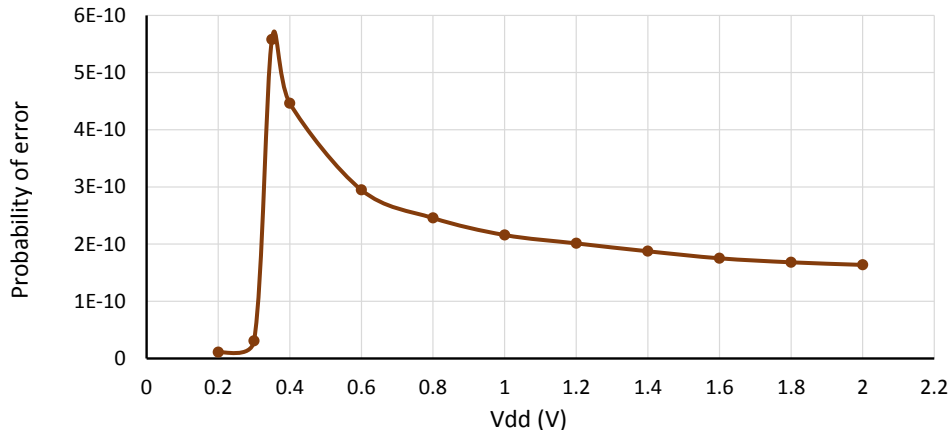
Figure 3.9: Overall error probability of the circuit vs Vdd.

the circuit optimization based on power and performance trade-off works, the reliability of the circuit decreases dramatically to reach the lowest value at Vdd=0.35 V. This region is also known as the low-energy corner, where both reliability and performance drop rapidly, which results in a recommendation to avoid this region. In the third region, at very low voltages, the reliability of the circuit improves again to reach its highest value. This increase in the circuit reliability occurs due to the increase in the inertial delay of the gates at these values of Vdd. So, they act as filters for narrow SETs. This is a promising result for extremely low-power designs. This property is exploited by implementing a slow stage at the output terminals to work as a filter, and more details of this are given in Chapter 5.

3.4 NON-UNIFORM PATH

In this section, the reliability of a non-uniform path circuit is derived using the proposed method. This path is extracted from the c6288 benchmark circuit and it is constructed using 125 gates, including NOR, NAND, and NOT gates. The wires between the gates are modelled as 2 fF capacitors, and a schematic view of this path is shown in Fig. 3.11. The NOT gate is identical to the NOT gate used in the uniform-single path circuit. The width of the pull-up and pull-down transistors on the NAND and NOR gates is chosen so that it gives the same drive characteristics as the NOT gate. For the NAND gate the width of pull-up and pull-down transistors are 800 nm, and for the NOR gate the widths are 1600 nm and 400 nm for pull-up and pull-down
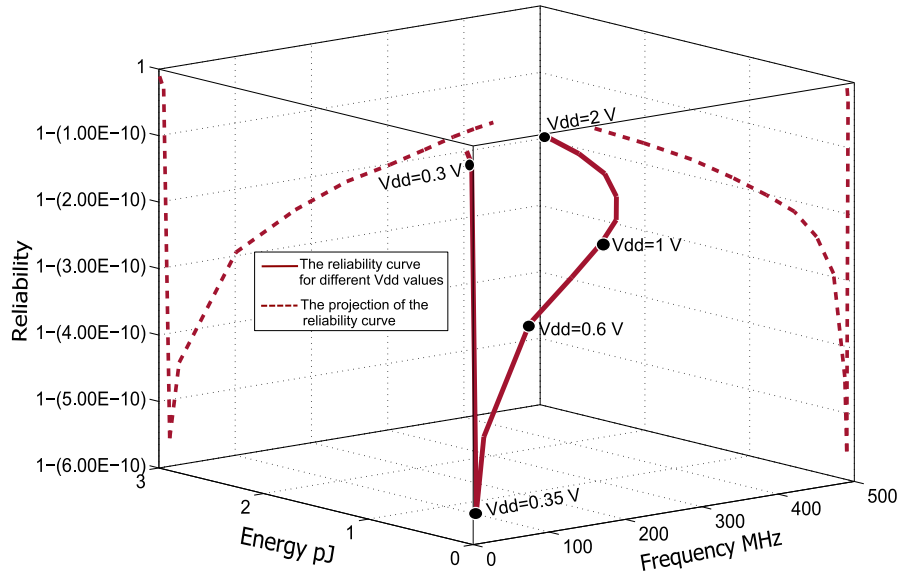
Figure 3.10: Reliability trajectory of the uniform path changes with changing the energy consumption and the performance, the data of this figure can be found in Table A.1.

transistors respectively. These values are calculated using the logical effort method by considering the inverter as a standard gate [121].
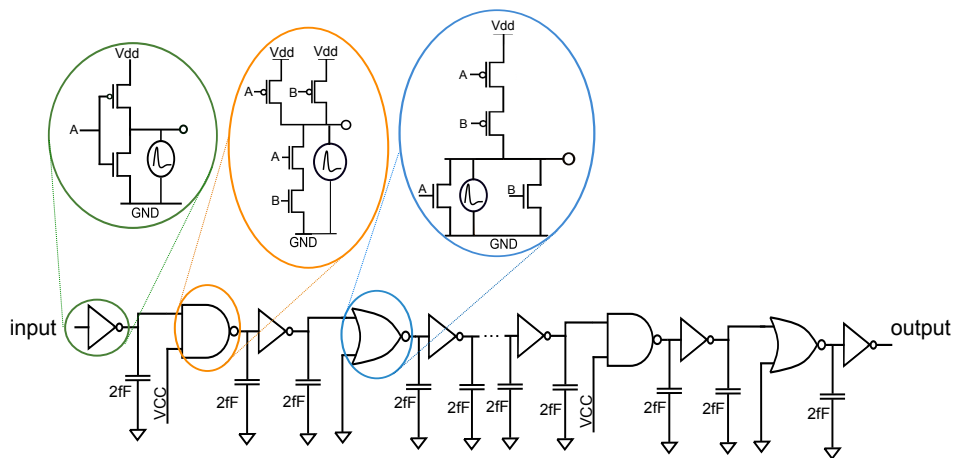
Figure 3.11: Non-uniform single-path circuit extracted from c6288 benchmark (the carry path).

This path is studied to see the impact of using various types of gates on the generation and propagation of SET pulses. To do so, three different SETs are generated in three different gates (NOT, AND and NOR). These gates are chosen from among the prior stages to allow the propagation effect to take place with the generated SETs. The duration of the generated SETs is

measured at the output of the faulty gates as shown in Fig.3.12. The durations were 395 ps, 407 ps and 398 ps for the SETs generated in NOT, NAND and NOR gates respectively. These pulses were generated at Vdd=1 V, and LET=50 $MeV.cm^2/mg$. The durations of these pulses are measured again at the output of the path and found to be 532 ps, 546 ps and 538 ps respectively as shown in Fig.3.13. By comparing the durations of the SETs before and after propagation, it can be noticed that their duration is broadened. This occurs as a result of the accumulated effect of PIPB, which occurs due to the dissimilarities in cell sizes and also depends on the polarity of the generated SET [36, 48, 37]. As the broadness of a pulse increases, so does the probability of it being latched by the output flip-flop. So, the effect of pulse broadness can be reflected negatively in the error probability at the prior stages as can be seen in Fig.3.14 where the error probabilities of the prior stages (gate No. 2 or gate No. 82) are higher than those error probabilities of the later gates (gate No. 114 or gate No. 122).
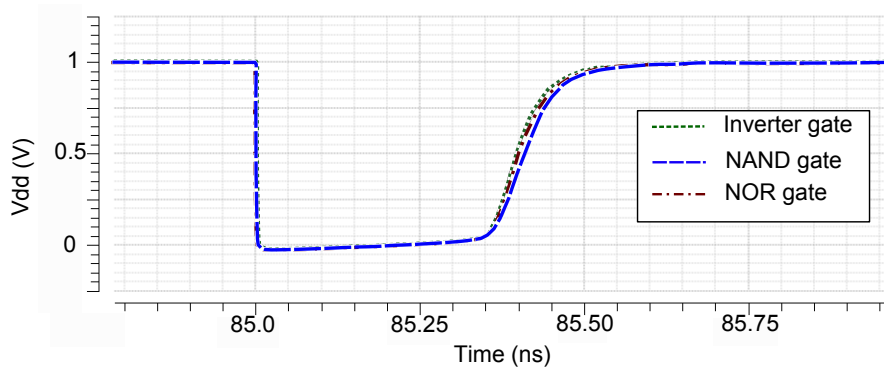
Figure 3.12: Transient pulses registered at the output of faulty gates.
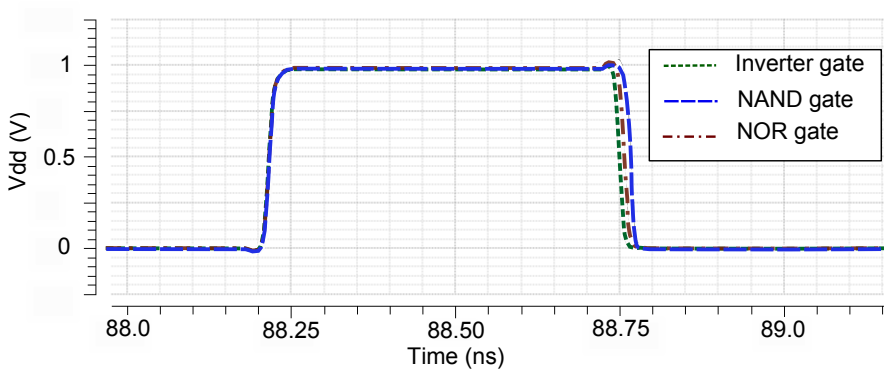
Figure 3.13: Transient pulses registered at the output of the circuit.

3.4.1 *Results*

To evaluate the reliability of this path, the same procedure is used as in the earlier example with the inverters. Transient current pulses corresponding to a range of LET values (1, 2, 5, 25, 50, 75, and 100 $MeV.cm^2/mg$) are generated and injected into each gate in the path. One transient pulse is injected in each simulation run. The output of the path is observed to obtain the critical values of the SETs. Then the error probability of each individual gate is calculated. The error probabilities of some intermediate gates are shown in Fig. 3.14. In this figure, we can see the impact of the location of the faulty stage on the error probability of that stage. In general, the error probability curves can be divided into two regions: the first region is 2 V⩾Vdd⩾0.6 V, where the error probability curves are very close to each other. This may be due to the equivalence of the attenuation effect in this voltage range. The second region of sub-threshold voltages is at Vdd<0.6 V, where the error probability of each stage differs from those of other stages, depending on the location of the stage. In this voltage range, the attenuation effect plays an important role in glitch propagation. So, most of the glitches that are generated in the prior stages are electrically masked.
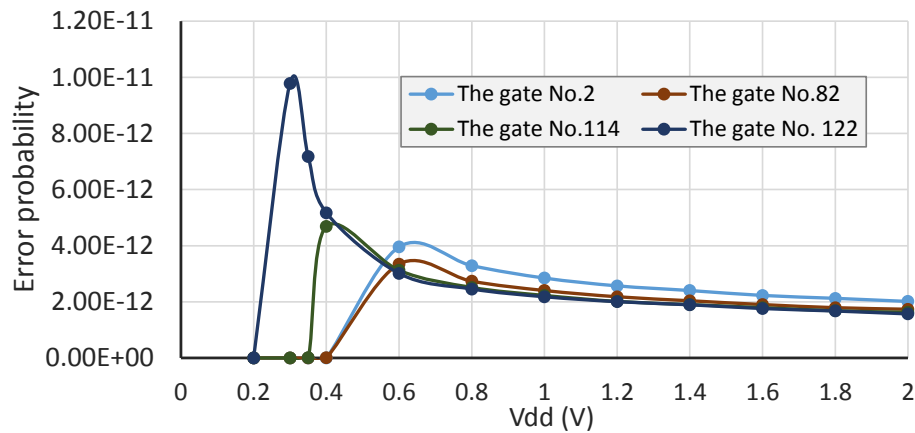
Figure 3.14: Error probability of intermediate gates vs Vdd.

The error probability of the last stage in the path is shown in Fig. 3.15. The trend of error probability at this stage differs from the error probabilities of all prior stages, especially at very low voltages. This is because of its location at the end of the path, so there is no stages effect on the generated glitches.

The values of error probabilities of the chosen intermediate stages can be seen in Table 3.1. In this table, the differences between the error probabilities
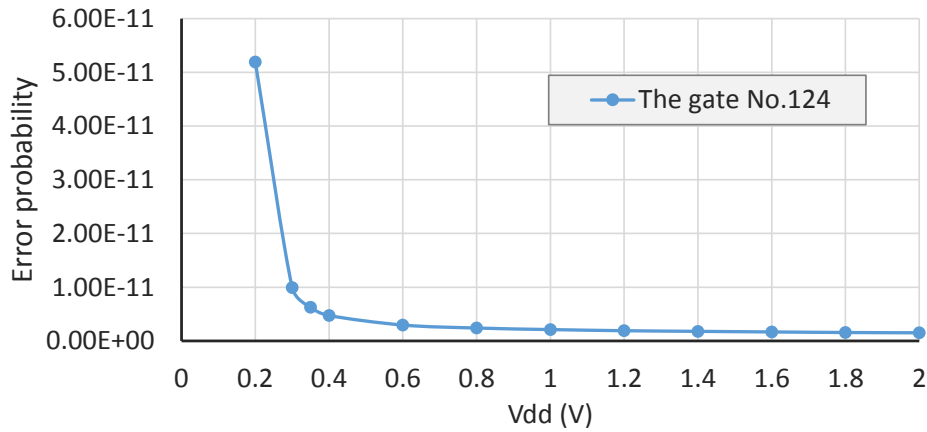
Figure 3.15: The error probability of the last stage vs Vdd.

Table 3.1: Error probabilities of individual gates corresponding to Vdd values.

Vdd (V)	Gate No.2	Gate No.82	Gate No.114	Gate No.122	Gate No.124
2.00	2.01E-12	1.74E-12	1.63E-12	1.57E-12	1.51E-12
1.8	2.12E-12	1.79E-12	1.68E-12	1.67E-12	1.57E-12
1.6	2.23E-12	1.90E-12	1.79E-12	1.76E-12	1.68E-12
1.4	2.40E-12	2.04E-12	1.90E-12	1.89E-12	1.78E-12
1.2	2.57E-12	2.18E-12	2.01E-12	2.01E-12	1.90E-12
1.00	2.85E-12	2.40E-12	2.23E-12	2.18E-12	2.12E-12
0.8	3.29E-12	2.74E-12	2.51E-12	2.46E-12	2.40E-12
0.6	3.96E-12	3.35E-12	3.12E-12	3.01E-12	2.96E-12
0.4	1.00E-17	4.89E-15	4.69E-12	5.17E-12	4.73E-12
0.35	1.00E-17	1.00E-17	1.32E-14	7.18E-12	6.29E-12
0.3	1.00E-17	1.00E-17	1.00E-17	9.78E-12	9.95E-12
0.2	1.00E-17	1.00E-17	1.00E-17	1.00E-17	5.19E-11

of different stages can be clearly noticed. In general, around the nominal voltage, the last stage (gate No. 124) has the lowest error probability, and the second stage (gate No. 2) has the highest, because the effect of PIPB. This broadness affects negatively on the reliability of the circuit. However, this situation changes at very low voltages.

After obtaining the error probabilities of all gates in the path, the overall error probability of the path is calculated by combining these probabilities as seen in Fig. 3.16. The overall error probability of the circuit increases gradually with the scaling down of Vdd to reach a peak value at Vdd=0.4 V,

and then it decreases dramatically to reach the lowest values at Vdd=0.2 V and 0.3 V.

The reliability of the whole circuit is calculated and introduced in Fig. 3.17. The reliability trajectory in the figure is plotted using a solid line, and this changes with the energy consumption and the performance of the circuit. The dashed lines in the figure are trajectories which represent the reliability metric on the two-dimensional planes; the reliability-energy plane and performance-reliability plane.

The reliability of the circuit is traded-off with energy consumption and performance of the circuit. It can be seen from the reliability figure that circuit reliability decreases with the scaling down of Vdd to reach the lowest reliable operating point at Vdd=0.4 V, and this point represents the highest error probability of the circuit as shown in Fig. 3.16. Then the circuit becomes more reliable again with the scaling of Vdd below 0.4 V, to reach the most reliable operating point at Vdd=0.3 V. It is possible to exploit this point of operation where the circuit does not consume a large amount of energy in low-performance tolerance applications. There is another region at Vdd=0.2 V where the circuit reliability compared to at the previous Vdd value 0.3 V becomes less reliable.

The trend of the reliability curve is different from the results for the chain of inverters, and this can be attributed to the attenuation effect of NAND and NOR gates at low voltages. Because of this attenuation effect it is observed that no SET pulses generated in the first 80 gates at values of Vdd below 0.4 V arrived at the output of the circuit. This is because of the electrical masking effect
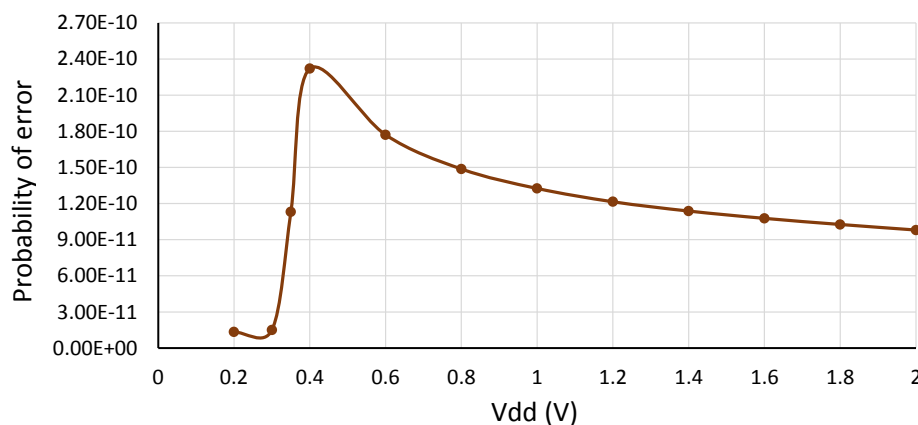
Figure 3.16: Overall error probability of the non-uniform circuit vs Vdd
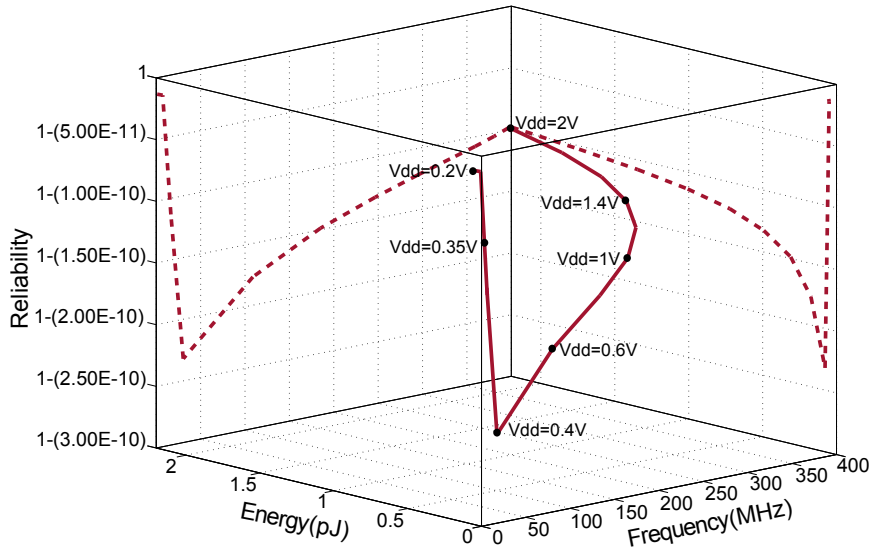
Figure 3.17: Reliability, energy and performance trade-off relationship for the non-uniform path circuit, the data of this figure can be found in Table A.2.

3.5 MULTIPATH CIRCUITS

Multipath circuits contain a limited number of single paths depending on their complexity and topology. So, any generated SET may propagate through different gates and paths to arrive at one or more output terminals, or it may be attenuated because of electrical or logical masking effects. Electrical masking occurs when an SET attenuated during the propagation through a path due to the inertial delay of the stages in the path. Meanwhile, logical masking effect prohibits an SET from propagation to one of the primary outputs. Such an effect may occur as a result of the generated SET being propagated through a non-sensitive input of a gate, such as NOR or NAND gate in a combinational circuit. For example, if an SET propagates through the non-sensitive input of a NAND gate, it will be masked by the other sensitive input of the gate. In order to derive the reliability of multipath circuits, all of these effects should be taken into account to prevent under- or over-estimating the reliability of the CUT.

In multipath circuits, paths may have various topologies. For example, *divergent paths* where one path diverges into two or more paths (fan-out), or *reconvergent paths* where two or more paths meet at one node (fan-in). However, all these paths, whatever their internal topology, start with the location of a

fault and finish with one or more primary output. In the proposed method, we perform simulation to obtain the error zone of each output and combine them to find the union of all of these error zones. Then, the error probability of that fault location can be calculated with regards to the union of the error zones of all outputs. An example is given below to explain the idea of this paragraph.

For example, consider a 3-bit full adder benchmark circuit to estimate its reliability, the schematic view of this circuit is shown in Fig. 3.18. The CUT is constructed from various gates include; NAND, NOR, NOT, and XOR gates, with 7-primary inputs and 3-primary outputs. The same gate specifications as those used in the previous circuits have been used in this circuit too. The wires between the gates are modelled as 2fF capacitors as in the single-paths examples.
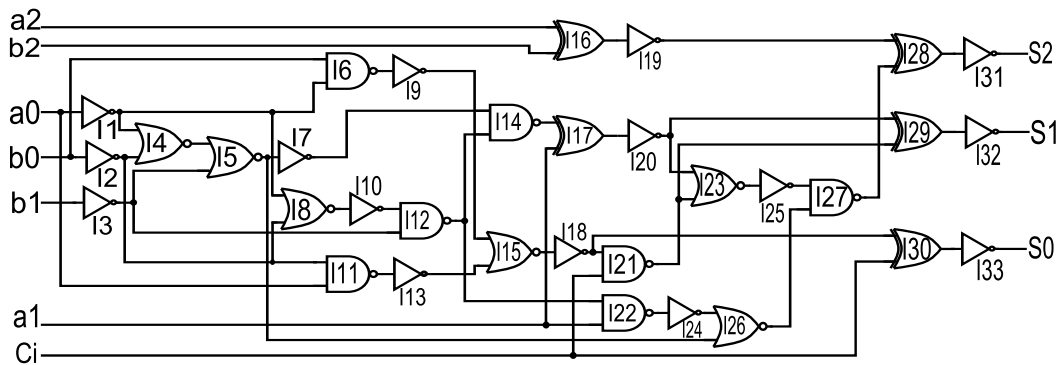
Figure 3.18: 3-bit full adder circuit.

To show how our method can be applied to multipath circuits, a transient current pulse is injected into the inverter I1. As a result of this, an SET is generated at the targeted inverter and propagated through sensitive paths to reach the output of the circuit. The sensitive paths are those paths that are sensitized to the generated SET and lead it to arrive at the output terminals without any masking. The configuration of such paths depends on the input vector that is applied to the circuit. For example, we consider the vector $X1 = \langle a0, a1, a2, b0, b1, b2, ci \rangle = \langle 0, 0, x, 1, 0, x, 0 \rangle$, as an input combination for the circuit, and the sensitive paths under this vector are shown in Fig. 3.19. So, by applying this input combination, the generated SET propagates to reach the primary outputs $S0$ and $S1$.
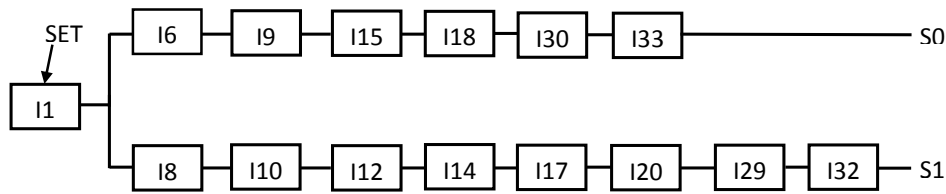
Figure 3.19: Sensitive paths for the gate I1 for the input combination X1.

3.5.1   *Deriving the reliability of the circuit*

The same steps have been followed in this case as in the single-path case. The difference here is that in multipath circuits, the generated SET might propagate to more than one primary output. In this case, all arriving SETs should be considered in finding the CVM.

We simulate the circuit number of times, and each time a fixed Vdd value and a range of LET values are applied to the circuit as has been applied in the single-path circuits in the aforementioned sections. This time, however, the critical values of the PV are registered when at least one of the paths (where two of them exist in this example) produces a borderline error where the output voltage exceeds 50% of Vdd. The critical values of the PV of the SETs propagated through the first path to reach the primary output S0 are illustrated in Fig. 3.20. This figure shows the borderline between error and no error zones at output S0. Due to the shortened path structure of this circuit, the size of the error zone compared with the clock cycle is relatively large, unlike in the single-path case. The critical values of the PV of the other path that is connected to the primary output S1 can be seen in Fig. 3.21.

The union of the two error zones of both outputs S0 and S1 forms the error zone of gate I1, as can be seen Fig. 3.22. As can be seen in the figure, the overall error zone is wider than the error zone of each path. Therefore, a greater number of paths through which a SET propagates lead to a wider error zone in the circuit.

The same procedure is applied to the other input vectors, $X2 = \langle 0, 0, x, 1, 0, x, 0 \rangle$ and $X3 = \langle 0, 1, x, 1, 0, x, 0 \rangle$. In this case, it is assumed that the whole input set consists of only three vectors for simplicity. The critical values of the PV for these two input vectors are found, and the overall error and no error zones of the circuit are obtained. Then, the error probabilities of gate I1 at those two input combinations are calculated.
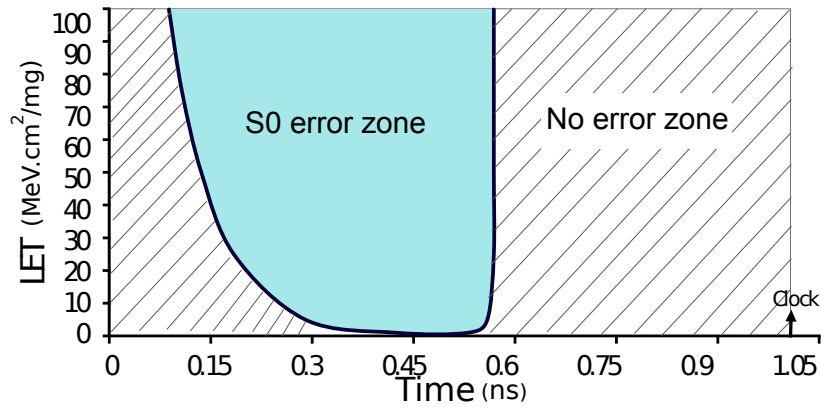
Figure 3.20: The critical values of the SETs that are generated at the gate I1 and propagated to $S0$ under input X1.
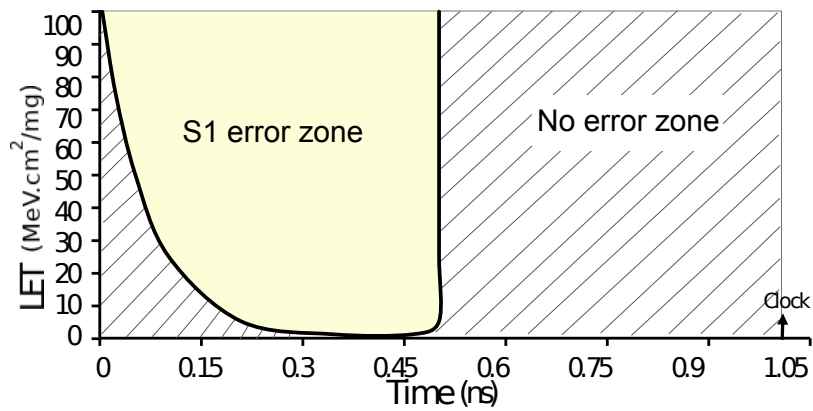
Figure 3.21: The critical values of the SETs that generated at the gate I1 and propagated to $S1$ under input X1.
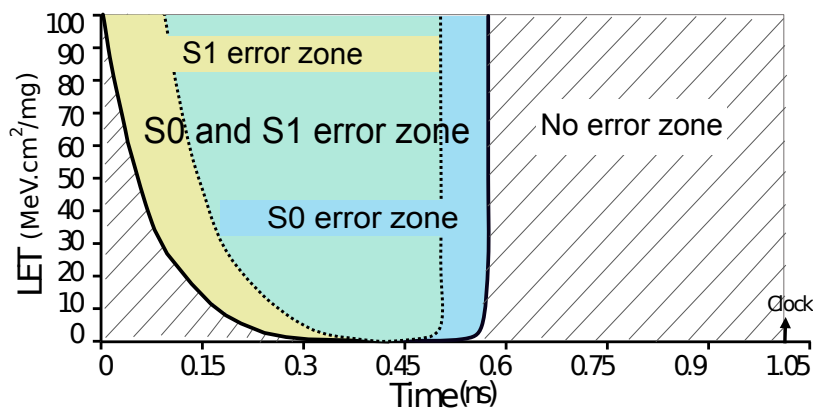
Figure 3.22: Critical values of the SETs generated in the gate I1 and propagated to the two primary outputs $S0$ and $S1$.

In order to calculate the error probability of I1 under the whole set of input combinations, one needs to know the probability of occurrence of each vector

in the input stream, which is part of the circuit specifications. We specify them, for example, as $F_{X1} = 30\%$, $F_{X2} = 20\%$ and $F_{X1} = 50\%$. Then, the weighted average of the error probabilities will be:

$$P_{err}^{I1} = \sum_{i=1}^{n} F_{Xi} \cdot P_{erri}, \tag{3.6}$$

where P_{err}^{I1} is the error probability of gate I1, n is the number of input vectors, and P_{erri} is the error probability at a certain input vector.

The same procedure is repeated for each gate and the error probability of all gates in the circuit is calculated. The overall error probability of the circuit is calculated by finding the summation of all error probabilities of individual gates.

$$P_{err} = \sum_{j=1}^{m} P_{err}^{Ij}, \tag{3.7}$$

where m is the number of instances in which an SET is generated and arrives at the primary output under the specified input vectors.

(3.7) is used to calculate the overall error probability at different values of Vdd.

3.5.2 *Results*

After finding the overall error probability of the circuit, reliability is calculated using the relationship $P_{reliability} = 1 - P_{err}$. The trajectory of reliability the circuit is shown in Fig. 3.23. The figure demonstrates the trade-off between reliability, energy consumption and performance of the circuit. The trajectory circuit's reliability at Vdd >1 V does not show a significant improvement compared with the increase in the consumed energy, which is doubled around 4 times. So, we recommend avoiding this operating region. At the values of Vdd $\leqslant 1$ V, the reliability of the circuit decreases rapidly, which is associated with a slight decrease in the circuit's energy consumption and a sharp decrease in performance. For values of Vdd <0.35 V, reliability improves dramatically without a huge cost in terms of energy. This is a recommended operating point for very low-power applications.

In this circuit example, the logic depth was 9 stages, and so the electrical masking effect is not strong. By comparing the reliability trajectory of this circuit and that of the non-uniform single path shown in Fig. 3.17, we can see that the reliability of long paths is higher than that of short paths at the low-energy corner.
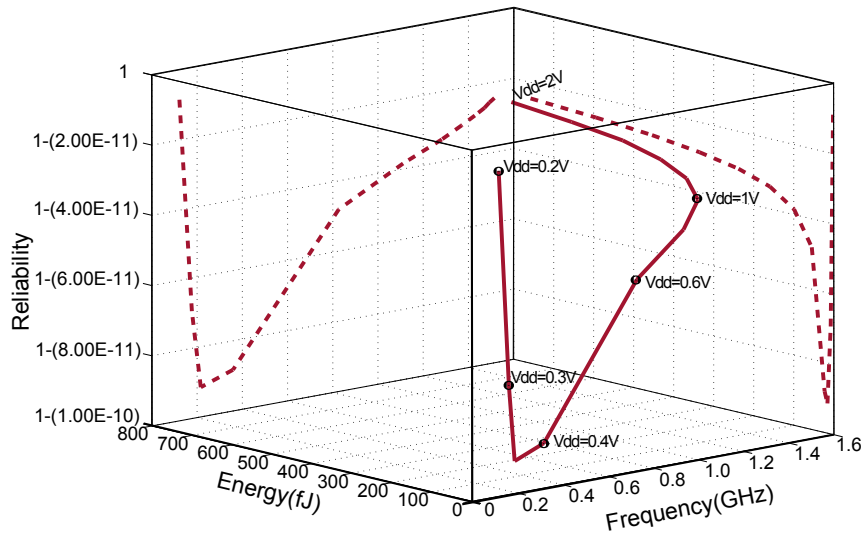
Figure 3.23: Reliability, energy consumption and performance trade-off in the 3-bit full adder circuit, the data of this figure can be found in Table A.3.

Up until this stage, small circuits have been used as examples to demonstrate how the proposed method can be applied to estimate the reliability of digital circuits. In order to apply this method to large benchmark circuits, the process needs to be automated. The automation scheme for this method is introduced in detail in the next chapter.

3.6 CONCLUSION

In this chapter, the proposed approach is introduced in detail, and examples with different topologies are given to show how the proposed method works.

For simplicity, a single-path circuit built from a chain of identical inverters has been introduced to illustrate the main steps that have been followed to derive the reliability of a circuit. Also, another example of a single-path circuit that represents the carry path of the c6288 benchmark circuit has been given. In this example the path is constructed with different types of gates,

with different drive strengths. The trade-off between reliability, energy and performance has been explored for both circuits. In both cases the reliability of the circuits decreases sharply at Vdd $\leqslant$ 1.2 V where the circuit optimization based on power and performance trade-off works. However, unexpectedly, the reliability of the circuits improves again at very-low values of Vdd. This highlights a new operating region that can be exploited where the circuit can operate reliably with very low energy consumption. This is noticed as a common characteristic in all examples.

In multipath circuits, the same steps as in single-path circuits have been followed, but in this case, the union of all critical values should be determined at the output terminals. This is because the generated SET propagates through different paths to arrive different output terminals. The dissimilarity of path lengths widens the error zone of those paths. Also, the number of sensitive paths contributes proportionally to the widening of the error zone of the gate. As a result of these effects, the probability of error increases. This preliminary example of a multipath circuit has been given to explain how the reliability estimation method can be applied to this kind of circuits.

AUTOMATING THE PROPOSED APPROACH

This chapter presents details of the automation of the reliability estimation approach proposed in this work. This automation scheme enables us to derive the reliability of large circuits.

In the automation scheme, the reliability evaluation process is divided into two phases: the simulation phase and the computation phase. The simulation phase is performed to find the critical values of the PV of the circuit (CVM). The computation phase is then used to calculate the error probability of the circuit by jointly processing the data collected using the simulation phase with the SFM of the interference. These two phases are presented in detail in the next two sections. To validate the automation scheme, it is applied to different benchmark circuits chosen from the ISCAS-85 library.

The ISCAS-85 benchmark circuits are used by researchers to evaluate the performance and quality of CAD tools. They have been widely used since being introduced in netlist form at the International Symposium of Circuits and Systems in 1985. However, their high-level designs have not been revealed. For research purposes, the functions and structures of these circuits are characterised by using well-defined components such as multiplexers, ALUs, and decoders [51].

4.1 SIMULATION PHASE

This phase is concerned with finding the critical values vector of the glitches (PV). This is done by writing a script by using OCEAN environment which is used with Cadence simulation tool. The block diagram of this process is shown in Fig. 4.1. This process starts by generating different transient current pulses corresponding to different LET values. The pulses vary in terms of magnitude and duration depending on the LET value that is used to generate each pulse. This ensures that the CUT is being tested under the whole range of effective neutron flux. In each simulation run, one current pulse is injected into a certain gate in the circuit. The output of the circuit is observed to register the critical values of the propagated glitches.
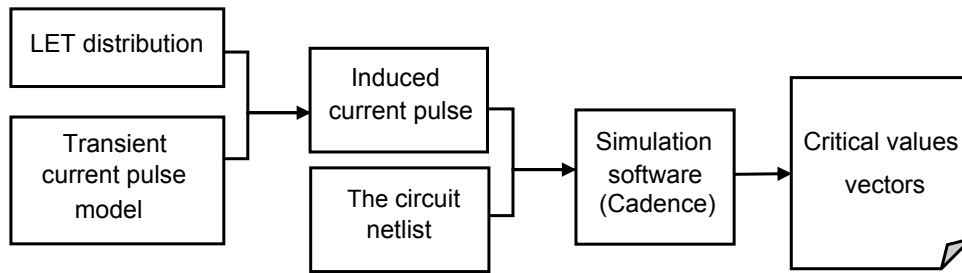
Figure 4.1: Process flow of finding CVM values

The pseudocode that describes the steps of this phase is shown in Algorithm 4.1. In this code, a circuit netlist is copied N times, where N is the number of gates in the circuit. Each copy of the circuit netlist contains one faulty gate. The simulation starts by applying the strongest SET can be generated in the circuit. This pulse is generated at Vdd=2 V and LET=100 $MeV.cm^2/mg$. Up until this step, we are testing weather or not the gate is *vulnerable* to the effect of the injected transient pulse, where the gate is vulnerable if it generates an SET. In a case where the gate is vulnerable and the generated SET arrives at the primary output of the circuit, the whole testing range of LET and Vdd is applied to the gate. Otherwise, the script skips this gate and tests the next one. After performing the simulation, the output of this process is the critical values vector of a faulty gate in the circuit. The simulation is run N times to examine all of the gates in the circuit netlist.

Algorithm 4.1 Pseudocode of the script used to find the critical values vectors of the vulnerable gates in a circuit

---

```
 1: for each gate i in the circuit  do
 2:    Inject the transient current pulse to the gate
 3:    Make a copy of the netlist
 4: end for
 5: for each netlist i in the circuit netlists N do
 6:    if a glitch with LET=100, Vdd=2 propagated to the circuit output
       then
 7:        Apply a range of LETs and a range of Vdd values
 8:        Find the critical values of all the glitches
 9:        Save the results in a text file
10:    end if
11: end for
```

The results obtained from this phase are the critical values vectors of all the PVs of the circuit saved in a text file. These results contain the same information as that presented in Fig. 3.22. In this form, the results can be read by the next phase in order to estimate circuit reliability.

4.2 ERROR PROBABILITY CALCULATION

This is the second phase of reliability estimation, where the probability of errors is calculated by processing the data obtained from the simulation phase. The block diagram of this process is shown in Fig .4.2. The critical values vectors and the PDF of the LET represent the input of this process. The error zone of each gate is determined. However, if there are more than one error zones, their union will be determined and accounted as the error zone of that gate. The probability of the error zone is calculated and multiplied by the rate of neutrons in one clock cycle to obtain the error probability of that gate. For each Vdd value applied to the circuit, the corresponding propagation delay is calculated and assigned as the operating clock period. After obtaining the error probabilities of all vulnerable gates in the circuit, the overall error probability of the circuit is calculated. The steps of the script used in this phase are shown in Algorithm 4.2.
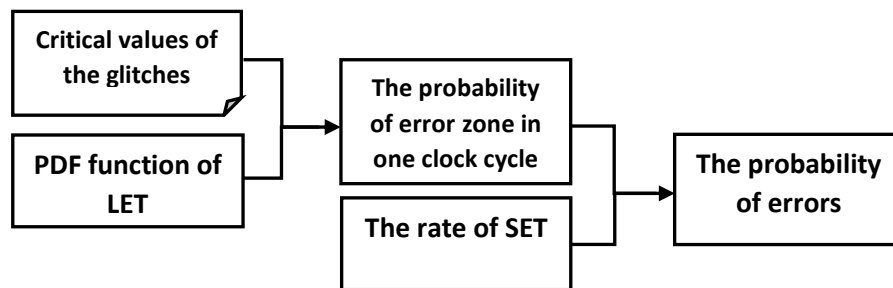
Figure 4.2: Process flow of calculating the error probability phase.

4.3 BENCHMARK RELIABILITY ESTIMATION

Several benchmark circuits have been chosen to derive their reliability using the proposed approach, and the specifications of the circuits chosen are shown in Table 4.1. Each circuit is selected to be different from the others in terms of structure and the length of paths. The impact of these differences on a circuit's reliability is explored in this section.

Table 4.1: Specifications of the benchmark circuits chosen to evaluate the reliability metric. [51].

Circuit	Function	No. of input lines	No. of output lines	No. of logic gates	No. of functional blocks
c432	27-channel interrupt controller	36	7	274	5
c499	32-bit SEC circuit	41	32	348	2
c1908	16-bit SEC/DED circuit	33	25	1211	6
c6288	16 x 16 multiplier	32	32	2,672	240

Algorithm 4.2 Pseudocode of the script used to calculate the error probability of a circuit.

```
 1: Perr=0
 2: for each sensitive gate i in the circuit  do
 3:    for each Vdd value from the Vdd range  do
 4:        Read the critical values of the glitches
 5:        Determine the error zones
 6:        if there are more than one error zone then
 7:            Find the union of the error zones
 8:        end if
 9:        Calculate the probability of the error zones
10:        Calculate the rate of neutrons per one clock cycle
11:        Calculate the error Probability of the gate Perr_g
12:    end for
13:    Calculate the error probability of the circuit Perr = Perr + Perr_g
14: end for
```

The error probability of each circuit is calculated several times with different input combinations, which have been randomly selected. These input combinations are assumed to be independent of each other. Then the average of the error probabilities obtained has been taken in calculating the overall error probability (P_{err}) of the circuit. Subsequently, the overall error probability is used to calculate the reliability of the circuit according to the relation $P_{reliability} = 1 - P_{err}$.

The three-way trade-off relation between reliability, performance and energy consumption (REP) is obtained for the selected benchmark circuits. Frequency is used as a performance metric for the CUTs, which is calculated by finding the propagation delay that is needed for an input signal to arrive the primary output terminal of the circuit. As each circuit has more than one primary output, so the propagation delay of the longest path has been chosen to be the propagation delay of the whole circuit. The energy metric is derived by integrating the total consumed power per one clock cycle.

The reliability trajectory of circuit c432 can be seen in Fig. 4.3. Most of the paths in this circuit are short, so the effect of electrical masking on the propagated SETs is not high, which leads to the propagation of most of the glitches that are generated in the circuit. As can be seen in the figure, the reliability of the circuit decreases sharply with reduction in the frequency and energy consumption of the circuit, reaching a minimum level at Vdd=0.35 V. Then the reliability increases again at Vdd=0.2 V as the effect of attenuation is noticeable at this Vdd value. However, the reliability of the circuit at very

low voltages does not improve significantly. This can be attributed to the property of short paths where the final gates can have an effective impact on the reliability of the circuit compared with the effect of other gates within a path.
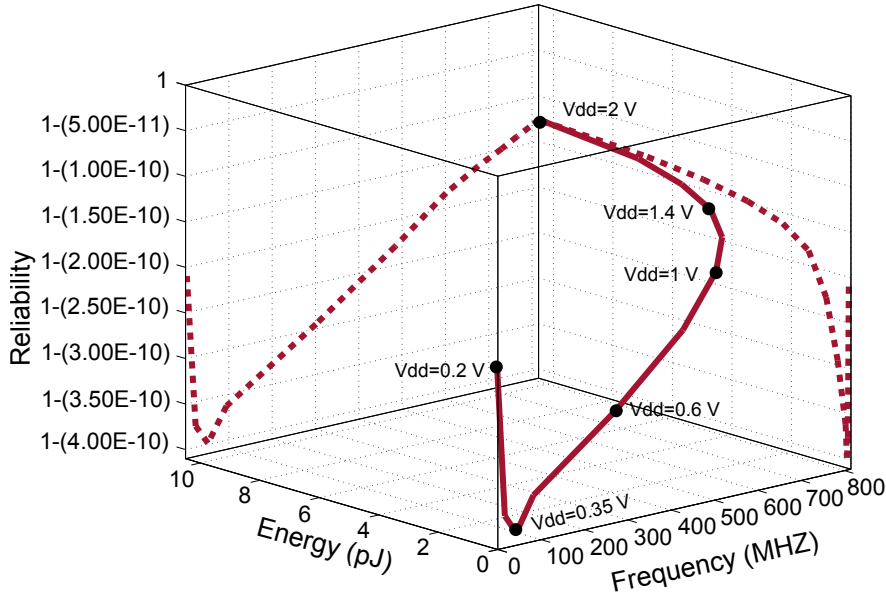
Figure 4.3: Reliability, performance and energy trade-off of circuit c432, the data of this figure can be found in Table A.4.

The reliability curve of c499 circuit is illustrated in Fig. 4.4. This circuit is considered to be a short-path circuit too. In this figure, we can see the trend of the reliability curve which drops steadily to reach the lowest reliable operating point at Vdd=0.35 V. Then it suddenly shoots up to reach the highest reliability level at Vdd=0.2 V. All glitches are attenuated at this Vdd value, even those generated in the final stages. This is because, in this circuit, the output gates are XOR gates which are considered to be large gates that have large delays [96], and so their electrical masking is very high. By comparing the reliability curves of this circuit and c432 circuit, we can see the positive impact of using large gates at the output terminals.

The reliability trajectory of circuit c1908 is shown in Fig. 4.5. This circuit is considered to have combination of short and medium-length paths. This structure has a negative impact on the reliability of the circuit at low voltages. In general, the reliability of the circuit falls steadily with decreases in frequency and energy consumption to reach the lowest level at Vdd=0.4 V. Then, the reliability increases sharply again at Vdd=0.3 V because of the attenuation of
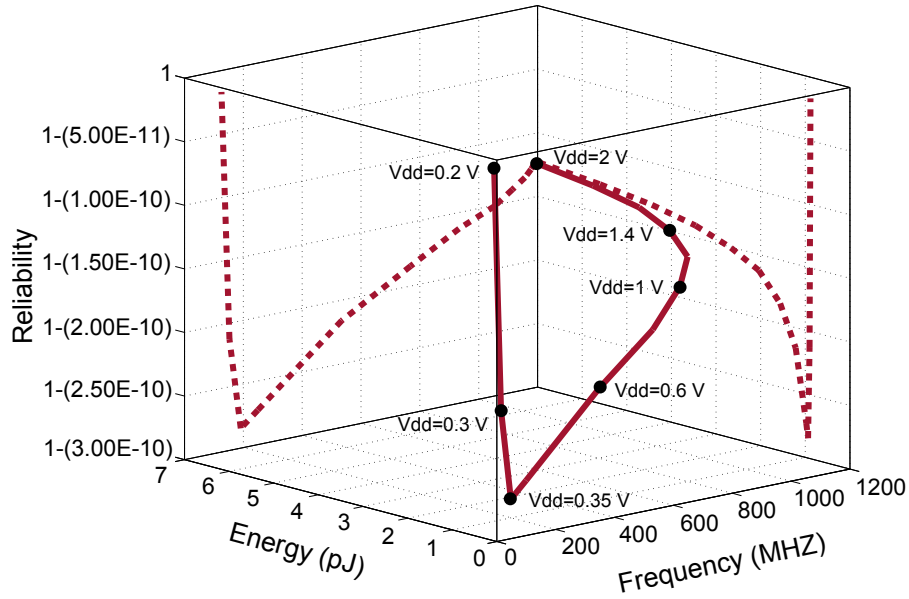
Figure 4.4: Reliability, performance and energy trade-off of circuit c499, the data of this figure can be found in Table A.5.

most of the generated glitches. At Vdd=0.2 V the effect of electrical masking on the prior stages is very high; however, the glitches that are generated at the final stages are widened tremendously to increase the error probability of the circuit at this Vdd value. Also, the high number of output gates relative to the number of the gates in the circuit and the type of these gates affects negatively on the reliability of the circuit at Vdd=0.2 V.

The reliability trajectory of circuit c6288 is illustrated in Fig. 4.6. The trend of the reliability trajectory of this circuit is slightly different from that of circuit c1908, and it is close to the reliability trend of circuit c499. The reliability is decreased to reach the lowest level at Vdd=0.6 V. Then it increases sharply to achieve the highest reliable point of the circuit at Vdd=0.2 V. Due to the implementation of the circuit with a long-path structure, the electrical masking effect at low voltages is very high. This leads to the attenuation of all the generated glitches except those at the output gates. As a result, the circuit reliability is improved dramatically at low voltages compared with the c1908 circuit.

In general, we notice that there is a common property here which is shared between all circuits whose reliability has been derived. This property can be stated as the golden finding of this chapter, which is that the same level of reliability of a circuit can be reached twice, once with high energy consump-
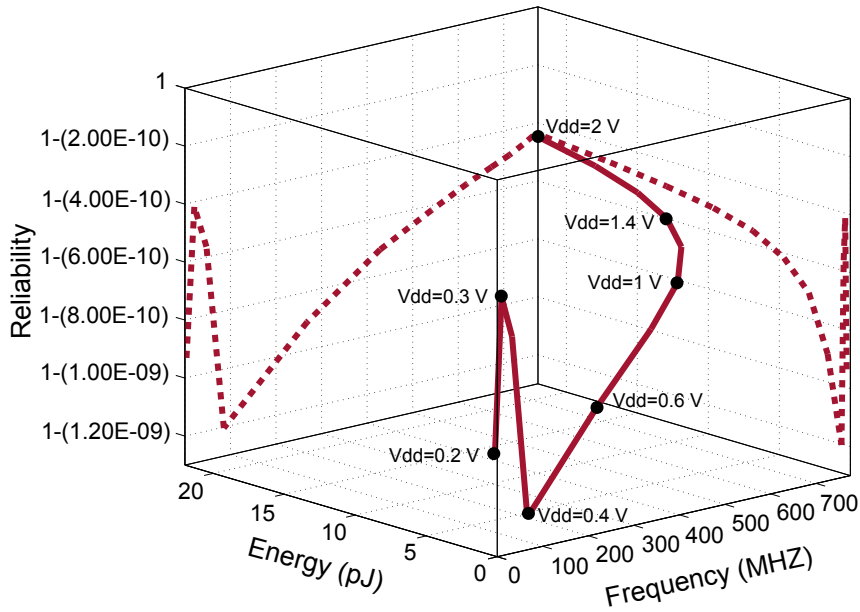
Figure 4.5: Reliability, performance and energy trade-off of circuit c1908, the data of this figure can be found in Table A.6.
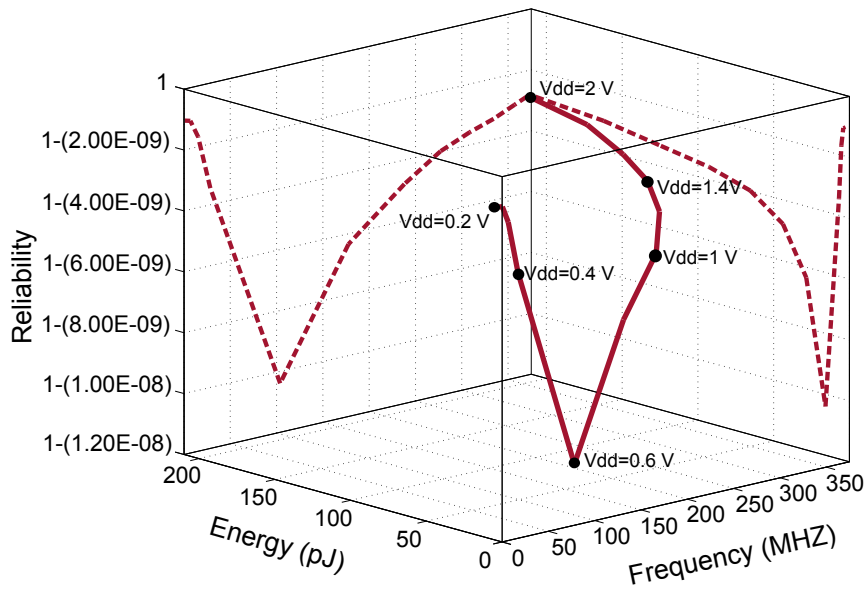
Figure 4.6: Reliability, performance and energy trade-off relation of circuit c6288, the data of this figure can be found in Table A.7.

tion and the other with low energy consumption at very low voltages. This property can be exploited in low-speed applications where the circuit can

be tuned between a high-reliability and low-energy consumption mode or a high-reliability and high-energy consumption mode.

The number of vulnerable gates in each benchmark circuit is calculated for each input combination. This number is not fixed and changes from one simulation run to another depending on the input combination that is applied to the circuit. So, the average number of vulnerable gates has been taken and is shown in Table 4.2. Also, depending on the number of vulnerable gates, the simulation time is calculated and this increases with the number of vulnerable gates. The average of the simulation time of each circuit can be seen in Table 4.2. The time is calculated according to the time that is spent on each simulation run and aggregated for the whole circuit.

Table 4.2: Number of vulnerable gates and the total simulation time of each circuit.

Circuit	No. of vulnerable gates	The simulation time (minuts)
c432	60	210
c499	65	355
c1908	260	1820
c6288	650	23148

4.4 STOPPING CRITERION

Due to the difficulty of deriving the reliability of these circuits for all input combinations, reliability is derived for a group of input combinations which are randomly selected. This leads to obtaining several results for each circuit. The average of the reliabilities obtained is calculated and considered to represent the reliability of the circuit. However, the number of selected input combinations needs to be determined, as this the number of the simulations that are needed to deliver precise results depends on this. In this work, we used the *standard error* (SE) metric to measure the convergence between the results obtained. So, the simulations stops when a convergence between the reliabilities obtained is achieved.

The SE is calculated according to the equation: Standard Error SE$=\sigma/\sqrt{n}$, where σ is the standard deviation of the obtained results and n is the number of results obtained.

The SE is calculated for overall error probabilities, and the SE values along with the number of the applied input combinations of circuit c432 are illustrated in Fig. 4.7. The convergence between the results can be noticed clearly, where the results that are obtained by applying the first five input combinations have a high values of SE which means that the level of convergence is very low. Eventually, the values of SE are reduced as a result of including more results. After applying 13 or 14 input combinations to the circuit, the values of the SE become very small. So, the convergence between the results is very high and it is possible to stop the simulation because the addition of any new result will have a negligible effect on the overall average.
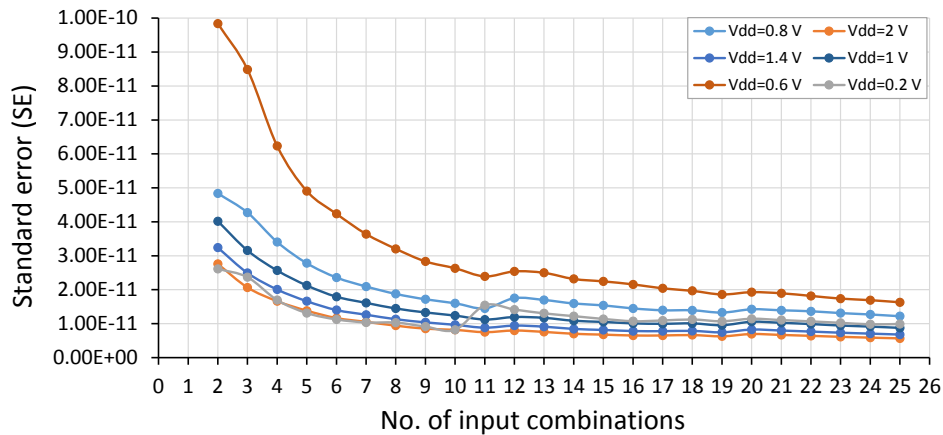
Figure 4.7: Standard error calculated for the error probabilities of different input combinations of circuit c432. There is a convergence in the results after 10 input combinations.

The convergence between the obtained error probabilities of circuit c499 is calculated and illustrated in Fig. 4.8. As can be seen in the figure, there is a quick convergence in the results occurs after applying 3 input combinations. However, it was a temporary witch disappeared with more input combinations. The real convergence occurs after applying 16 input combinations. Also, we can notice that the results converge with different trends according to Vdd values. For example, at Vdd=0.2 V the error probabilities of the circuit have converged after applying 10 input combinations to the circuit, which is faster than the results at other Vdd values. Moreover, it can be noticed that all SE values at this Vdd value are less than the other SE values. So, the results at this value of Vdd are very close to each other.

The SE of the error probabilities of circuit c1908 is shown in Fig. 4.9. It can be seen in the figure that convergence occurs in the results after 9 or 10 input combinations. However, at Vdd=0.3 V, the results converge earlier after 6 input combinations.
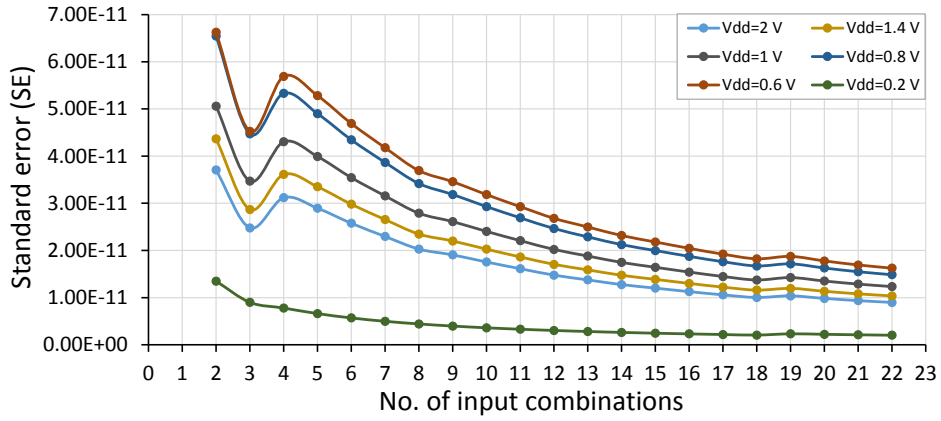
Figure 4.8: Standard error calculated for the error probabilities of different input combinations of circuit c499. The convergence occurred after 15 or 16 input combinations.
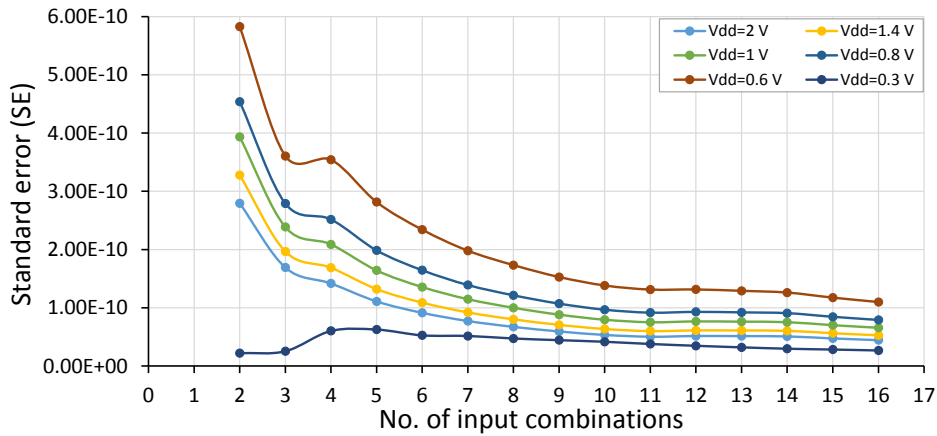
Figure 4.9: Standard error calculated for the error probabilities of different input combinations of circuit c1908, showing a convergence in the results after 9 or 10 input combinations.

The convergence of the error probabilities of circuit c6288 can be seen in Fig.4.10. The results show high divergence when applying a few input combinations; however, after applying 11 input combinations to the circuit, the results showed a good convergence. This convergence increases when more input combinations are applied. However, we stopped the simulation process after applying 16 input combinations and achieving reasonable convergence.

4.5 CONCLUSION

In this chapter, the main contribution of the method for deriving a circuit's reliability is automated to be applicable to large circuits. As example, circuits are selected from ISCAS-85 benchmark circuits and their reliability is estimated.
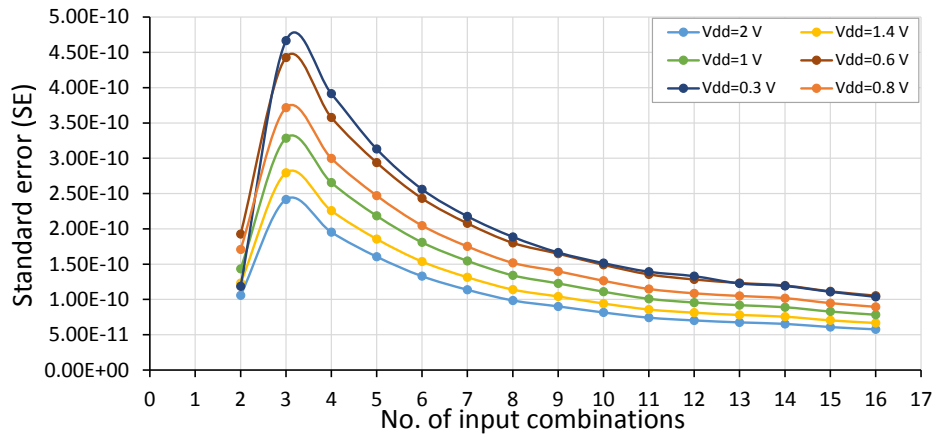
Figure 4.10: Standard error calculated for the error probabilities of different input combinations of circuit c6288, good convergence in the results occurring after 11 input combinations.

The reliability of each circuit is evaluated at a group of input combinations which are randomly selected and then the average is taken and considered to represent as the reliability of the circuit.

The reliability of each circuit has a unique trajectory depending on its structure. In the case of circuits with short paths, the glitches that generated in the final stages impact negatively on the reliability of the circuit. This is because the number of gates within a path is not high enough to make this effect negligible. However, the output gates even in short-path circuits have a positive impact on the reliability of the circuit. Some gates, such as XNOR and XNOR gates, have the ability to attenuate the generated glitches. So, the reliability of the circuits implemented using these kinds of gates improves dramatically at very low voltages. The reliability of long-path circuits usually improves at very low voltages due to the dominant effect of prior gates, where the electrical masking effect attenuates most of the generated glitches. So, the effect of the final stages are negligible compared with the effect of the prior stages.

The standard error metric is adopted as a criterion for when to stop all simulations performed to estimate the reliability of large circuits. Once convergence has occurred in the results obtained, the simulations is stopped and the average of the results obtained is calculated. This approach is usually acceptable in large circuits which require time-consuming simulations.

IMPROVING THE RELIABILITY OF COMBINATIONAL CIRCUITS

This chapter introduces a new technique which can be used to mitigate the soft errors that are generated in combinational circuits. This technique relies on enhancing the inertial delay of the last stages to filter out narrow glitches. It is suggested based on our observations while performing the simulation experiments. It was noticed that slow stages filter out most of the glitches that propagate through them. As a result, the reliability of the circuit is improved. We exploit that effect by making the final stage slower than other prior stages so as to increase the propagation delay of that stage and allowing it to work as a filter. This technique is implemented using active elements where the size of the final stage is modified, and using passive cells where a low-pass filter is added at the end of the paths in the combinational circuit. The results show a dramatic improvement in circuit reliability at the expense of a minor increase in energy consumed and a small decrease in circuit performance.

5.1 INTRODUCTION

During the propagation of a transient pulse, it may suffer from degradation in amplitude and duration. This degradation is caused by the gates through which that pulse propagates. Degradation in amplitude could occur if the input of a certain gate is switched to the opposite state before the output of the gate is completely switched to the new state [1]. This usually occurs when the inertial delay of the gate is longer than the duration of the propagated glitch. So, this causes a distortion in narrow glitches and they do not reach the full amplitude of the waveform. Also, when a circuit works at very low voltage, the propagation delay of the gates increases which causes attenuating the propagated glitches that have a duration lower than the transition time of these gates [78, 93, 117, 131].

5.2   CIRCUIT RELIABILITY WITH ACTIVE FILTER STAGE

In this type of filtering technique, the parameters of the final stage (here, the size of transistors) in the path are increased so that it works as a filtering stage. By increasing the size of this stage, it becomes slower and has a longer inertial delay compared with other stages in the path. By doing this, this stage is enabled to filter out most of the SETs pulses generated in prior stages. In fact, some of them are attenuated completely, and those which are not are reduced in duration. This filter stage is more effective when the circuit works at low voltage.
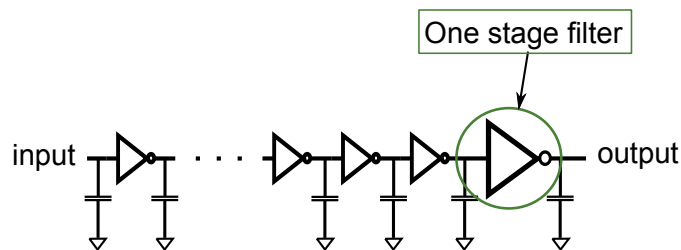
(a) A schematice view shows the one stage filter
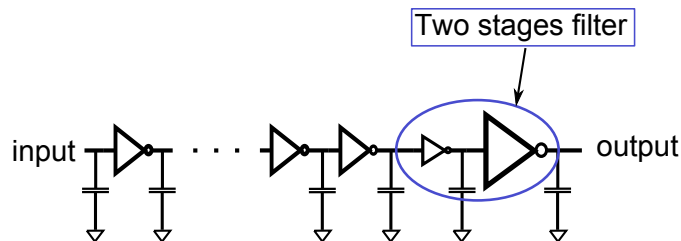
(b) A schematice view shows the two stages filter

Figure 5.1: Schematic views for the circuit with the filter stage.

As an example, the proposed technique is applied to the circuit constructed with a chain of inverters and described in Section 3.3 to improve its reliability. In this experiment, either the last stage only or the last two stages are replaced with gates of different sizes, and the schematic view of the circuit with the filter stage is demonstrated in Fig. 5.1. The weakest filter in the experiment is implemented as a 16x-size inverter at the primary output, while the strongest is constructed of a 0.5x inverter driving a 32x inverter (denoted as 0.5x+32x). The idea of using two-stage combinations comes from the fact that the logical effort method [121] effectively doubles the inertial delay. Altogether, the fol-

lowing filters are simulated: 1x (no filter), 16x, 24x, 32x, 0.5x+16x, 0.5x+24x, 0.5x+32x.

The overall error probability of the circuit before and after adding the filter stage is shown in Fig. 5.2. In general, the overall error probability of the circuit is reduced by different degrees depending on the strength of the filter stage. The lowest error probability is calculated in the case of using the filter with the longest propagation delay (0.5x+32x).
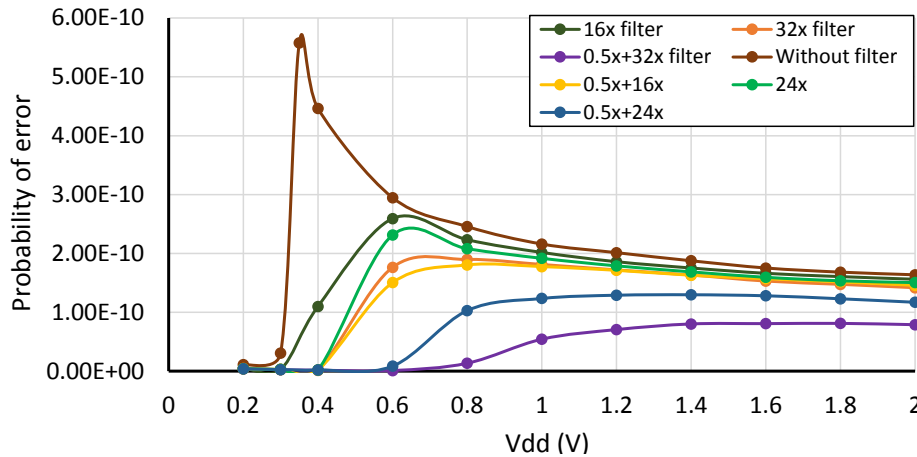
Figure 5.2: Overall error probability of the circuit with and without a filter stage.

As can be seen from Fig. 5.2, the 32x and 0.5x+16x filters produce almost the same effect, as expected according to the logical effort method. Therefore, the 0.5x+24x and 0.5x+32x filters are equivalent to 48x and 64x. At low voltages, the filtering effect increases because the propagation delay of the filter becomes longer compared to the glitch duration.

The reliability of the circuit before and after adding the filter stage is illustrated in Fig. 5.3. It can be seen from the figure that the reliability trajectory of the circuit is shifted into more reliable regions according to the filter strength. The most reliable operation is obtained by applying the 0.5x+32x filter, but the circuit with this stage consumes more energy as can be seen in the energy-reliability projection in the same figure. In general, the reliability improvement is associated with a change in the performance and energy consumption of the circuit which decreases and increases respectively by different values depending on the strength of the filter stage. So, increasing the filter strength leads to improving circuit reliability but also an increased energy-performance penalty. These penalties are studied in more detail in the next section.
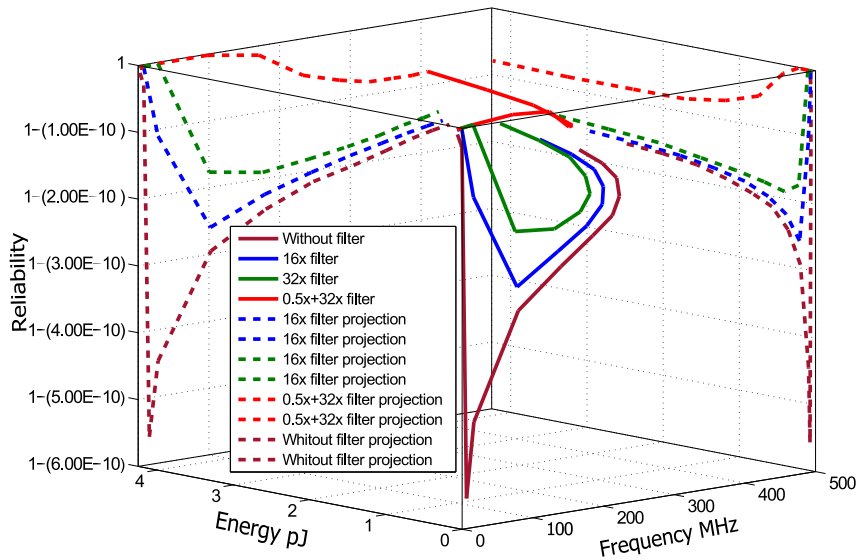
Figure 5.3: Energy-Reliability-Performance trade-off before and after adding the filter stage, the data of this figure can be found in Table A.8.

The percentage reduction of the error probability due to adding the filter stage to the circuit is calculated for each filter size and shown in Fig. 5.4. The error suppression percentage values reflect how much the circuit reliability has improved. The figure shows that, as the supply voltage decreases, more errors are suppressed and dissipated. These suppression values vary according to the strength of the filter used. Also, in the same figure, it can be seen that the two most powerful filters in suppressing errors are 0.5x+32x and 0.5x+24x.
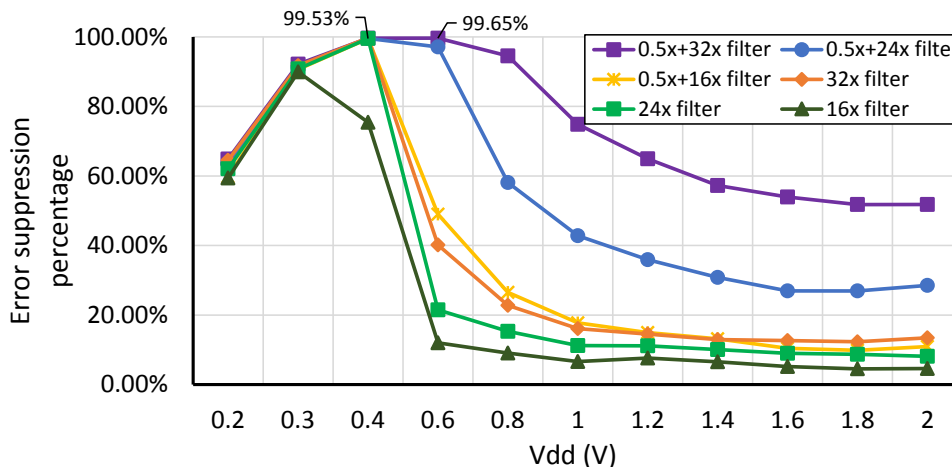
Figure 5.4: Error suppression percentage vs Vdd.

5.3 ACTIVE FILTER STAGE EVALUATION

The filter stage is a modified stage inserted into a circuit to eliminate the glitches generated in that circuit. So, in order to identify the advantages and the disadvantages of this stage, its effect on circuit parameters is studied. The main three parameters that are assessed before and after the filter stage is added are performance, energy consumption, and the area occupied by the circuit.

5.3.1 *The Performance Change*

The performance of the circuit is calculated directly by finding the propagation delay of the whole path. This is accomplished by summing the propagation delays of all gates in the path. The propagation delay of the circuit is affected by the filter stage whose delay is increased due to its change in size, and so the performance of the whole path is affected by this stage. Fig. 5.5 shows the extent to which the filter stage with different strengths causes the performance of the circuit to deteriorate. It can be noticed that the percentage reduction decreases at low voltages, so that the influence of the filter stage on performance increases at high voltages. This can be attributed to the fact that the circuit at low voltages is already working at a low performance level, and so the extra delay does not make much difference. In general, the percentages of performance reduction are acceptable values when compared with the improvements in reliability achieved.
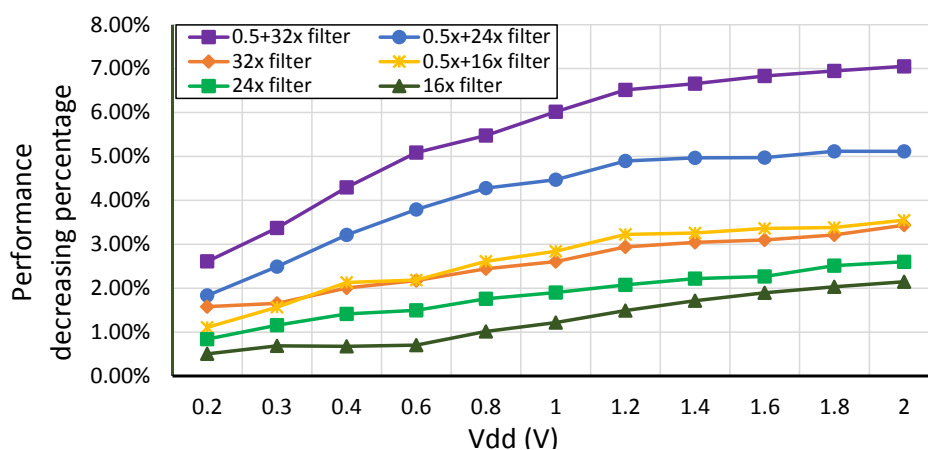
Figure 5.5: Effect of the filter stage on the performance of the circuit.

5.3.2   *Change in Energy Consumption*

Increasing the size of the transistors in a gate has a significant effect on their switching speed. They take extra time to switch from one logic state to another compared with regular gates in the same technology library. In other words, the transition time of the signal that propagates through those stages is longer than the transition time in normal stages. This slowness in switching speed leads to increases in the short-circuit current. As a result of this, the energy consumed by the circuit increases [118, 89]. The extra energy consumption due to the addition of the filter stage is calculated and demonstrated in Fig. 5.6. It can be noticed that the extra amount of energy that is consumed by the circuit in the presence of a filter stage depends on the strength of the filter itself. So, the 0.5x+32x filter contributes to the highest percentage of extra energy consumption. However, this percentage varies with variations in Vdd values. Moreover, if we compare the 32x and 0.5x+16x filters we can notice that, from the energy consumption and error reduction perspectives, it is better to use the two-stage structure.
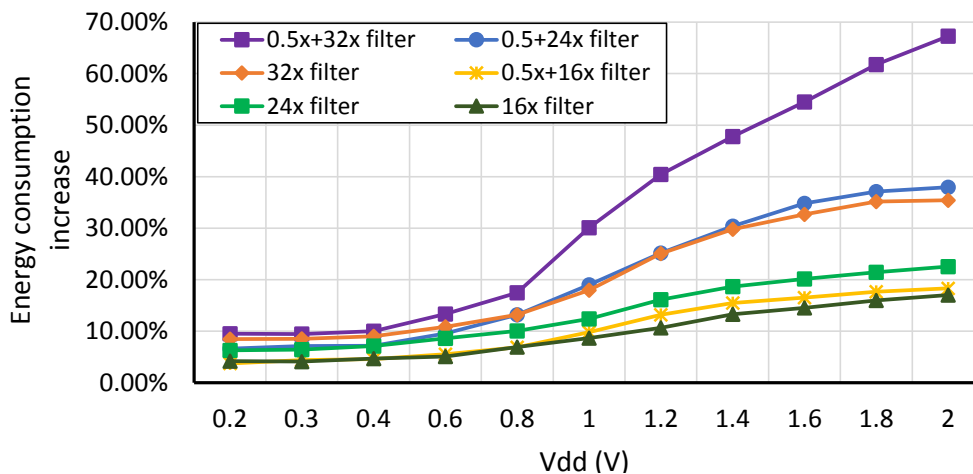
Figure 5.6: Effect of the filter stage on the energy consumption of the circuit.

5.3.3   *Area Overhead*

Area overhead is a major concern for chip designers, and so we studied the effect of the filter stage on the area of the circuit by comparing the area before and after adding this stage. The area overhead of the circuit can be seen in Fig. 5.7. It can be said that it this in the acceptable range compared with the

area overhead caused from using other techniques at system level such as triple modular redundancy (TMR), or information redundancy.
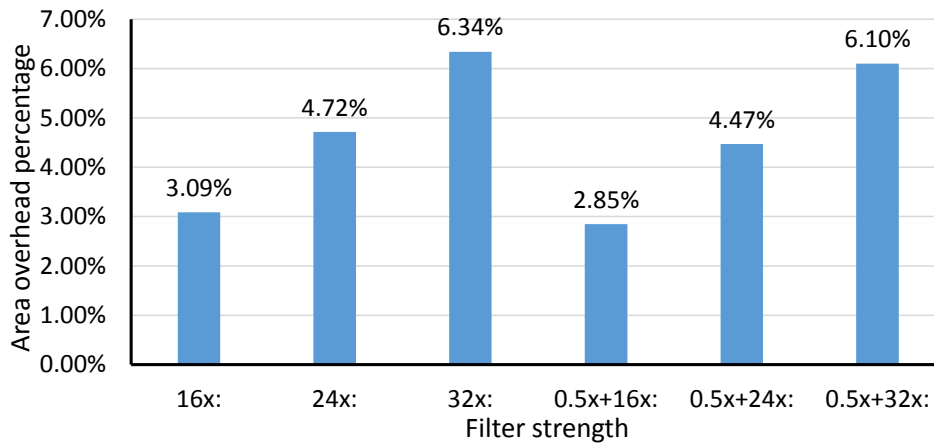
Figure 5.7: Effect of the filter stage on the circuit area

The filtering technique that is proposed in this section uses standard cells that could be used for any CMOS circuit implementation, and we merely need to tune the size of these special cells to meet the requirements of reliability and energy consumption. These filters with a certain strength are able to suppress the propagated SETs by 99.6% at the expense of a minor increase in the energy consumption of the circuit. Using this technique to improve the reliability of a circuit is more effective with circuits constructed using long paths. This can be attributed to the fact that, in this kind of circuit, the extra energy consumption or reduction in performance caused by the filter stage is very small compared with the original energy consumption or performance of the circuit. This may be also true in the case of the area overhead penalty. However, in combinational circuits that have short paths, especially those with high numbers of primary outputs, increasing the size of the final stage is not a practical approach. This approach is applied to c432 and c1908 combinational circuits, and the extra energy consumption and performance reduction penalties are shown in Table 5.1. As can be seen in the table, in the case of c432, the extra energy consumption reaches unacceptable levels, especially at high voltages.

This provided the motivation to propose the implementation of the filter stage using passive components, which is introduced in the next section in detail.

Table 5.1: Effect of using 0.5x+32x filter stage on c432 and c1908 circuits (%).

Vdd(V)	error suppression		performance reduction		energy consumption	
	c432	c1908	c432	c1908	c432	c1908
2.0	50.49	38.21	33.08	13.66	256.05	175.45
1.8	50.05	35.79	33.49	14.03	298.25	162.01
1.6	50.06	33.93	33.94	14.44	284.96	146.22
1.4	51.20	33.15	34.73	14.99	260.18	126.86
1.2	54.36	33.00	35.36	15.66	227.47	103.83
1.0	57.69	35.78	36.74	16.43	178.72	76.27
0.8	66.35	49.88	38.17	17.00	112.74	47.40
0.6	78.74	81.42	37.93	17.24	57.43	25.28
0.4	70.55	74.65	39.92	17.39	40.33	17.09
0.35	51.03	21.64	39.12	16.52	43.07	17.62
0.3	-2.69	-73.13	37.85	14.39	47.12	19.06
0.2	-203.1	-255.5	36.06	11.11	83.33	30.89

5.4   CIRCUIT RELIABILITY WITH PASSIVE FILTER STAGE

The same concept that was used in the previous section is used here. However, other components are used here to reduce the consumption of extra energy. So, the active filter stage is replaced by an RC circuit (low-pass filter) to filter out the narrow glitches before they arrive at the primary output of the circuit. The resistor (R) and capacitor (C) values are chosen to filter glitches with durations $\leqslant$ 500 Ps, because this is the dominant duration noticed during the experiments performed. The whole idea of our technique is to add a slow stage to create a transitional region able to attenuate most of the propagated glitches. The main steps of the process that is used to select the type and strength of filters are shown in Fig. 5.8. The filter type can be determined according to the topology of the circuit. An active filter stage is effective with circuits that have long paths due to the high energy consumption and performance penalties with short-path circuits. However, a passive stage filter can be used effectively with both circuit topologies.

The passive filter stage is added to the c432 and c1908 ISCAS-85 benchmark circuits to improve their reliability. This is introduced in the next sections.
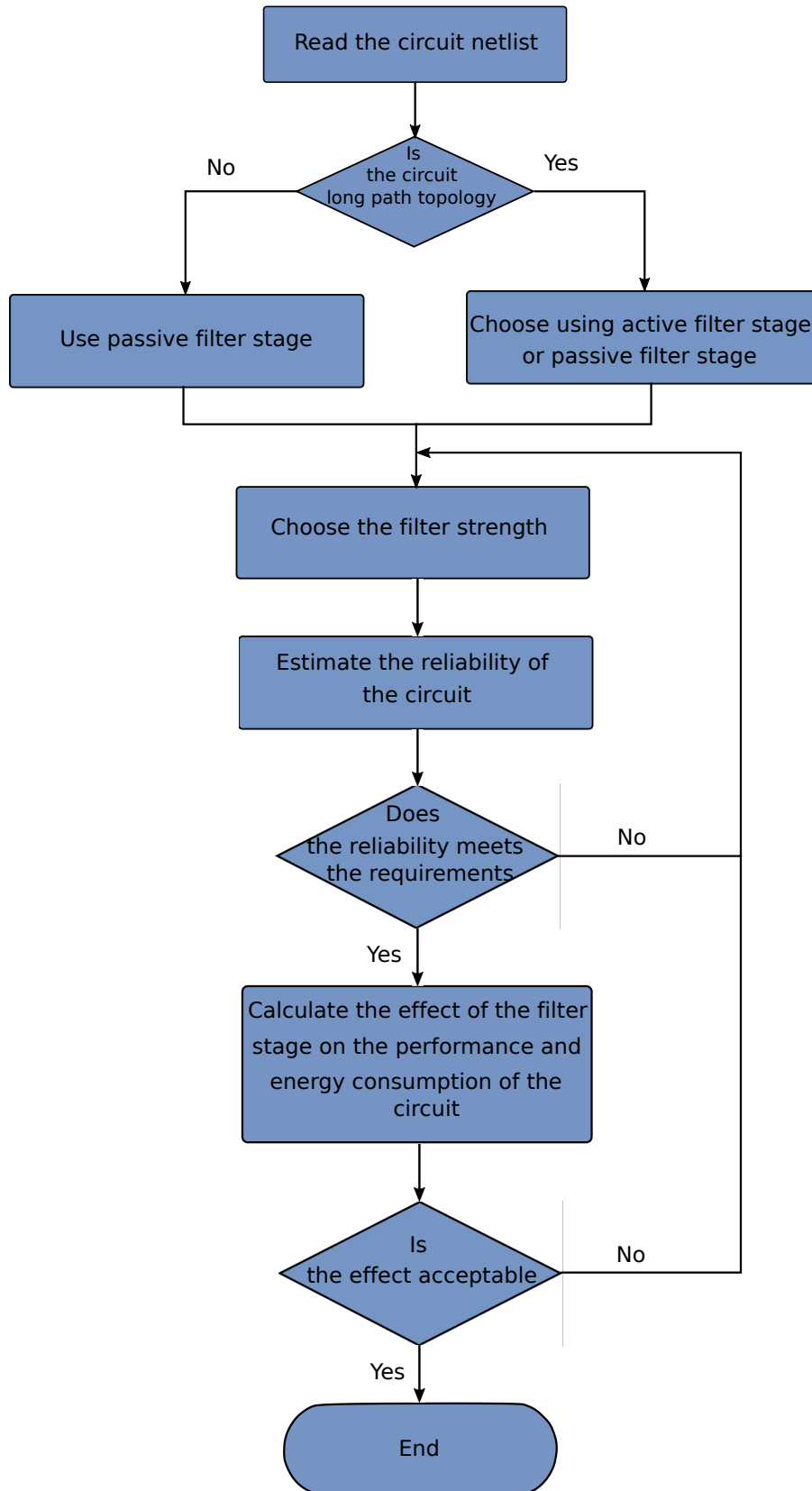
Figure 5.8: Flowchart of the systematic method of selecting filters type and strength.
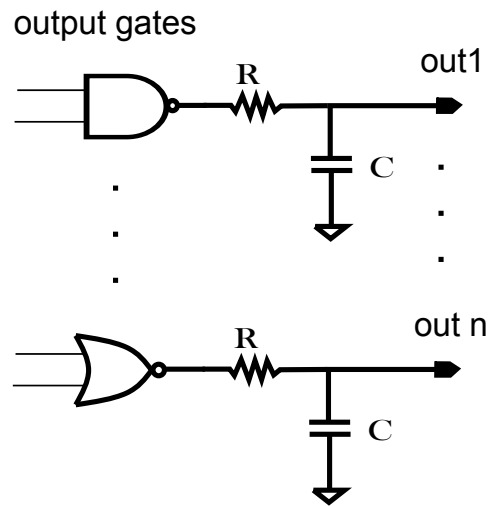
Figure 5.9: RC filters connected to circuit outputs

5.4.1 *Improving the Reliability of c432 Circuit*

The RC circuit is connected to all the output terminals of the circuit, as shown in Fig. 5.9. These RC circuits add a delay to the transition edges of the propagated signals and so in cases of narrow pulses, and due to their short duration they do not reach their full amplitude, which leads to them being attenuated.

The reliability of the circuit is evaluated after adding different passive filters with different values of capacitor. We fixed the value of the resistor at 10 kΩ, and the capacitor value is changed to values of 30, 40 and 50 fF. So, the passive filter is implemented at different strengths, the weakest with R=10 kΩ and C=30 fF, and the strongest with R=10 kΩ and C=50 fF. As a result of applying these filters to the circuit, its reliability improved according to the filter stage's strength. The reliability of the circuit before and after adding the filter stage is shown in Fig. 5.10. As can be seen in the figure, there is a significant improvement in circuit reliability. This improvement varies depending on the value of Vdd and the strength of the filter stage. The effect of the filter stage on the reliability metric is shown in the solid lines. The dashed lines show projections of the reliability metric against the energy consumption and performance of the circuit. The best reliability trajectory is achieved by applying the strongest filter stage (with C=50 fF) to the circuit. The reliability of the circuit in this case is very high and it is not correlated with the value of Vdd of the circuit as it was before the addition of the filter stage. Moreover, an interesting finding here is that at Vdd=0.3 V, the reliability of the circuit

was at its lowest level before adding the filter stage. However, after adding the weakest filter stage (with C=30 fF) to the circuit, this point (Vdd=0.3 V) becomes the most reliable point in the reliability trajectory. The lowest reliable point is shifted to the higher Vdd value of 0.6 V.
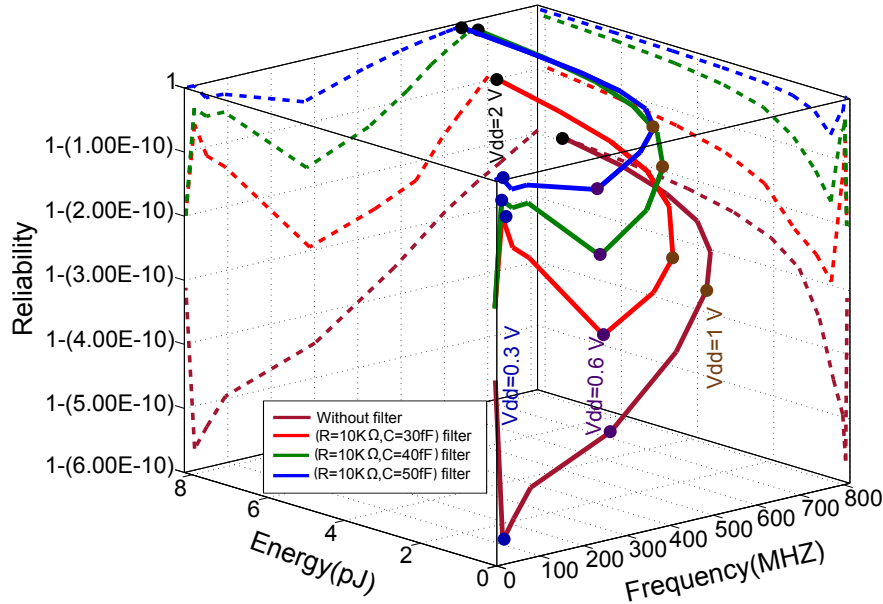
Figure 5.10: The reliability improvement of the circuit c432 that occurred due to adding the passive filter stage, the data of this figure can be found in Table A.9

The error elimination rates are calculated by finding the percentage reduction in error probability of the circuit due to the addition of the filter stage. The percentage reductions in error probability (or error suppression percentages) are shown in Fig. 5.11. It is clearly shown that, in the case of using the strongest filter with C=50 fF, most of the errors generated in the circuit are eliminated. In general, the percentage of error elimination decreases gradually when scaling the Vdd down to 0.6 V, and then it increases again at lower Vdds values. The trend of these curves correlates with the behaviour of the reliability improvement trajectories shown in Fig. 5.10.

This filtering circuit yields effective results in terms of improving the reliability of the circuit due to its ability to suppress the generated glitches. The cost of these improvements is an increase in the energy consumption of the circuit and a reduction in the performance. In order to validate the proposed
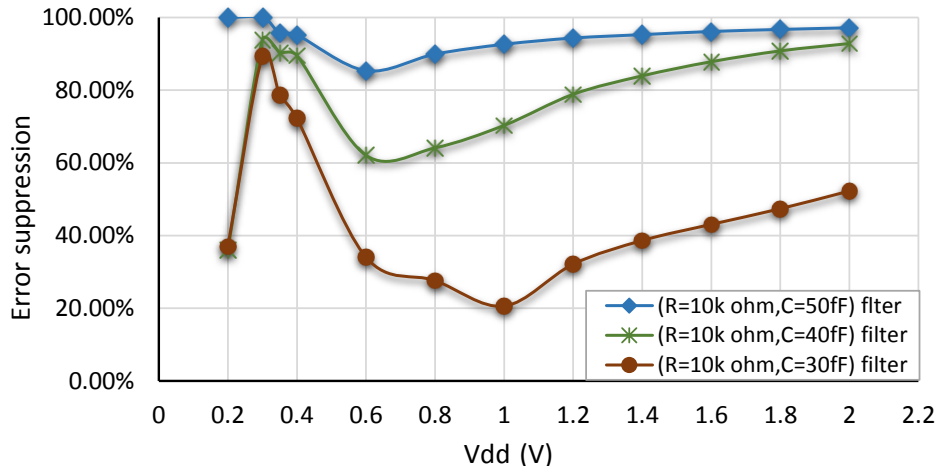
Figure 5.11: Error suppression percentage of c432 circuit vs Vdd.

filtering circuit, these penalties are calculated and introduced in details in the next section.

5.4.1.1 *Evaluation of the Filtering Circuit*

The performance reduction due to the addition of the filtering stage to the circuit is calculated and the results are shown in Fig. 5.12. In general, the trend of performance reduction is correlated with the Vdd value of the circuit, where the reduction in performance decreases gradually with the scaling down of the Vdd of the circuit. However, at Vdd $\leqslant$ 0.8 V, the performance reduction decreases sharply to reach its lowest level of around 2%. Also, by comparing the performance reduction according to filter stage strength, it can be noticed that the stronger filters lead to the highest performance reduction penalty. The curves of the performance of the circuit before and after adding the filter stage are introduced in Appendix C.

  The energy consumption of the circuit increases due to the addition of the filtering circuit by various percentages depending on the filter strength and the voltage of the circuit. The percentage increases are shown in Fig. 5.13. The trend here differs from the trend of performance reduction, where the extra energy consumed by the filtering circuit increases with the scaling down of voltage. This is because, when scaling the voltage of the circuit down, less energy is consumed, and so the amount of the energy that is consumed by the filtering circuit becomes relatively large. The curves of the energy consumption of the circuit can be found in Appendix C. However, when the voltage is scaled down to below the subthreshold voltage, the extra energy
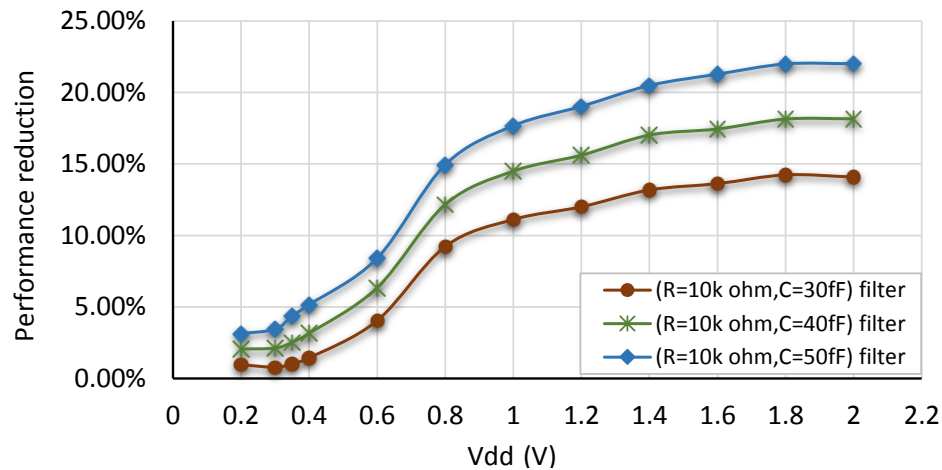
Figure 5.12: Effect of the filter stage on the performance of c432 circuit
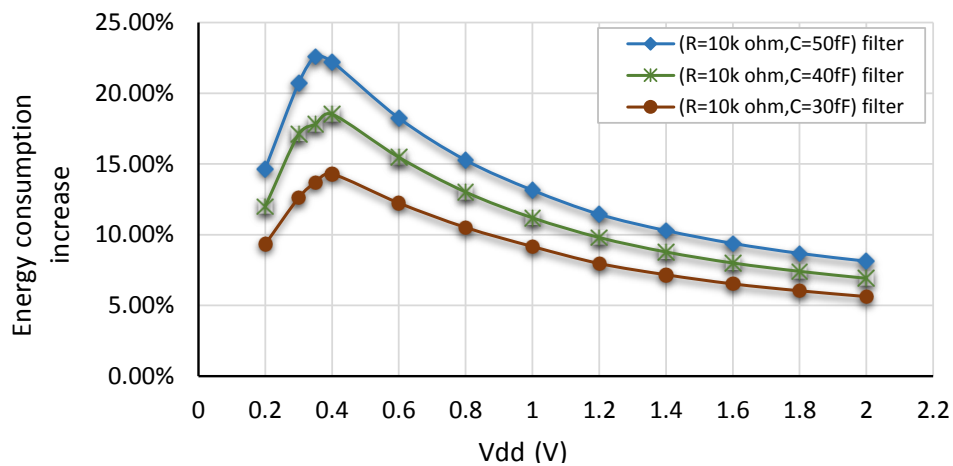
Figure 5.13: Effect of the filter stage on the energy consumption of c432 circuit

consumption decreases to reach around 12%. All the filters exhibit the same trend in extra energy consumption, but with different values.

5.4.2 *Improving the Reliability of the c1908 Circuit*

The passive filtering circuit is applied to the c1908 benchmark circuit to improve its reliability. The same procedure as in the previous section is followed, so that filters with different strengths are applied to the circuit, and the weakest is implemented with a C=30 fF capacitor, and the strongest with a C=50 fF capacitor.
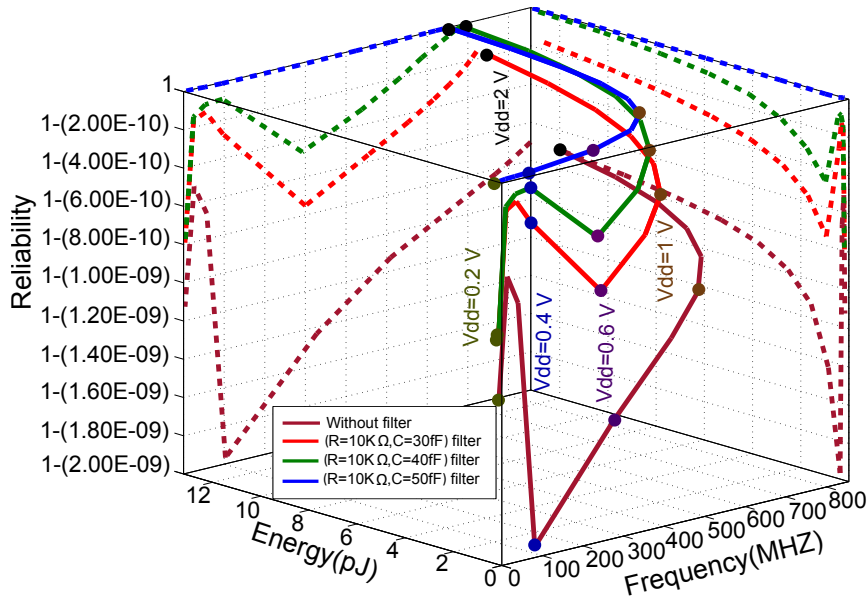
Figure 5.14: Reliability improvement of c1908 circuit that occurred due to adding
the passive filter stage, the data of this figure can be found in Table
A.10.

The reliability of the circuit before and after adding the filtering circuit
is shown in Fig. 5.14. The figure shows that the reliability of the circuit is
improved remarkably. This improvement correlates significantly with filter
strength. It is noteworthy that the reliability of the circuit at Vdd=0.4 V before
adding the filtering circuit was at its lowest level; however, this changes
promptly after adding the filtering circuit and circuit reliability increases
drastically to reach its highest level. It is noticed that the effectiveness of
the filtering circuit is very high at low voltages; however, the reliability of the
circuit has been improved significantly at all Vdd values.

The degree of error suppression due to the application of the passive filtering
stage to the circuit is calculated and shown in Fig. 5.15. From the results
in the last chapter, we found that, in the voltage range 0.6 V⩽Vdd<2 V, the
error probability of the circuit increases with the scaling down of Vdd of the
circuit; however, the percentages of suppressed errors decrease. This means
that the filtering circuit has a fixed filtering rate regardless of the voltage
that is applied to the circuit. The highest suppression percentage occurred
at Vdd=0.4 V, which matches the highest error probability of the circuit. In
terms of the filter strength, more than the 99.5% of errors are suppressed as
a result of applying the strongest filter stage to the circuit.
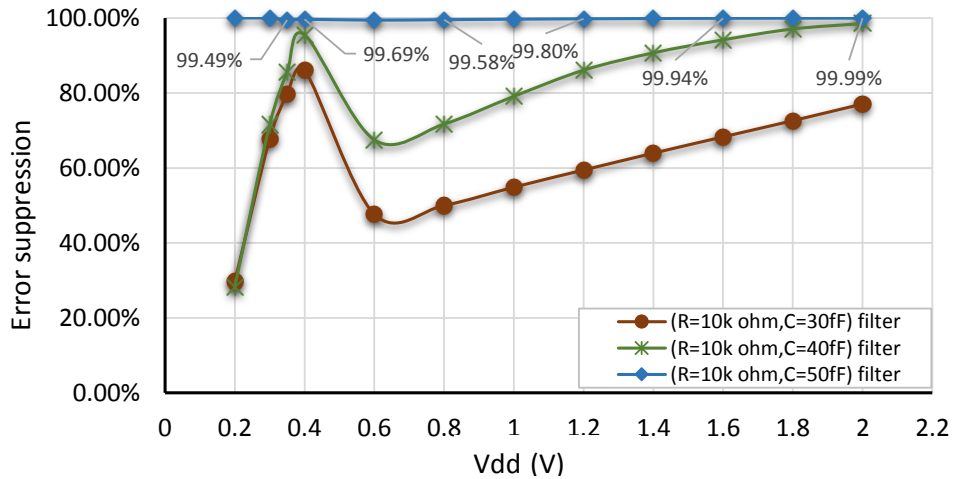
Figure 5.15: Error suppression percentage of c1908 circuit vs Vdd.

5.4.2.1 *Evaluation of Passive Filter Stage*

The performance of the circuit is reduced due to the addition of the filtering circuit. This reduction is the cost of improving the reliability of the circuit. We calculated this reduction by finding the extra propagation delay that is added to the circuit with each filter type. These percentage reductions are shown in Fig. 5.16. The biggest reduction in circuit performance occurred due to the use of the filtering circuit with C=50 fF, with a maximum reduction around 24% at Vdd =2 V. However, this reduction decreases with scaling the voltage down, to reach around 7% at Vdd=0.2 V. The other two filtering circuits with C=40 fF and C=30 fF cause a reduction in performance of the circuit too. The maximum reductions were around 20% and 15% at Vdd=2 V respectively. It can be noticed that the influence of the filtering circuit in reducing circuit performance decreases steadily as the Vdd declines from 1.2 V to 0.4 V. The performance of the circuit with and without the filter stage is shown in Appendix C.

The effect of the filtering stage on the energy consumption of the circuit is studied too. This is essential in order to evaluate the use of this stage with large benchmark circuits. The extra energy consumption caused by the filtering stage is calculated and shown in Fig. 5.17. It can be noticed from the figure that the increase in energy consumption depends on the filter strength, where the filtering stage with C=50 fF has the highest impact on the energy consumption of the circuit. Moreover, the influence of the filtering circuit on the energy consumption of the circuit increases gradually with the scaling down of the voltage to Vdd=0.35 V. Below this Vdd value the extra energy
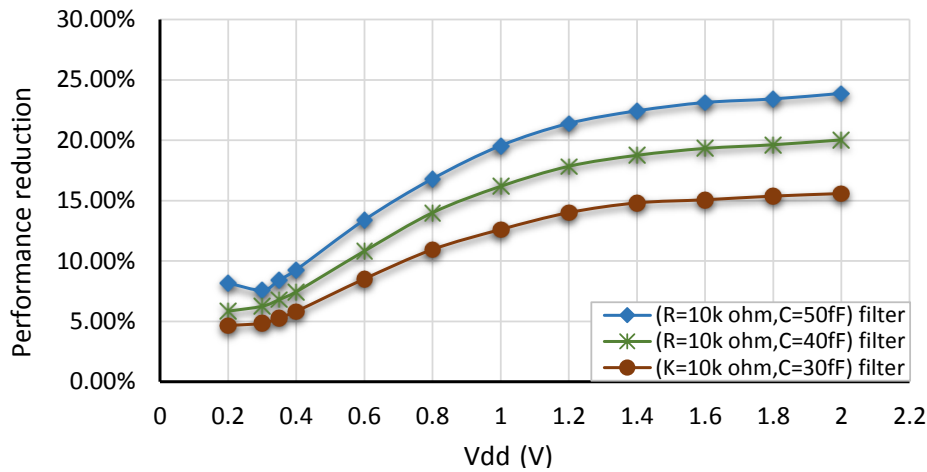
Figure 5.16: The effect of the filter stage on the performance of c1908 circuit
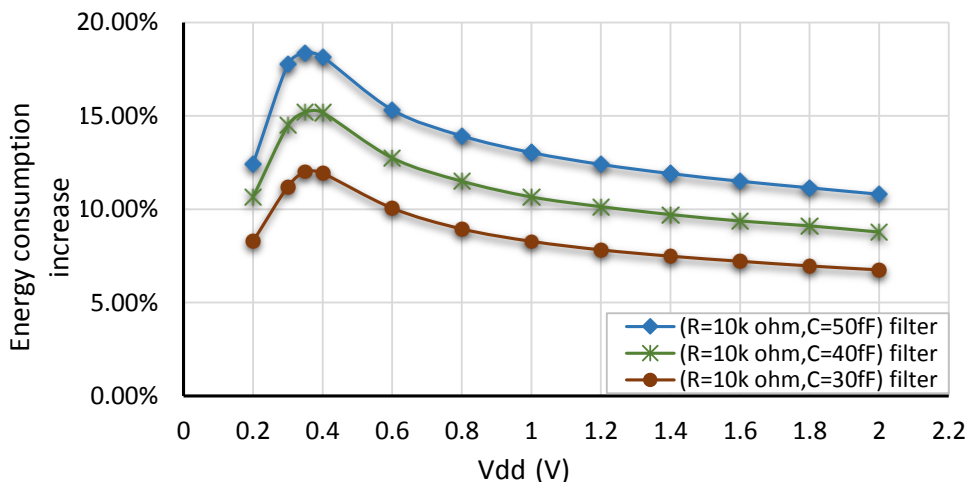
Figure 5.17: The effect of the filter stage on the energy consumption of c1908 circuit

consumption decreases with reductions in Vdd. The energy consumption of the circuit with and without the filter stage is introduced in Appendix C.

Table 5.2 shows a comparison between the proposed technique and various techniques that are used to mitigate soft errors in combinational circuits. Our technique suffers from a high penalty in the performance compared with other techniques. However, it outperforms these techniques and can provide high average error reductions up to 96.2% as well as low energy consumption.

Table 5.2: Comparison between the proposed technique and other techniques.

Used approach	Error reduction	Performance reduction	Energy consumption
Proposed (R=10k, C=30fF)	39.9%	11.8%	8.6%
Proposed (R=10k, C=40fF)	74.7%	15.3%	10.8%
Proposed (R=10k, C=50fF)	96.2%	18.6%	13%
Choudhury *et al.* [21]	95.5%	Not reported	30.6%
Raji *et al.* [109]	67.3%	3.2%	Not reported
Zhou *et al.* [140]	53%	5.1%	20.9%

5.5 CONCLUSIONS

By taking a close look at the results, we can develop a good idea of the trade-off between circuit reliability, energy consumption and performance according to the effect of each filter on each parameter.

The reliability of a circuit can be improved by inserting a filter stage at the end of the circuit paths. The filter stages used in this work can be categorised in two types: active and passive filter stages.

The active filter stage is constructed by changing the size of one or two of the gates located at the end of the path. The one-stage filter is implemented by changing the size of the final stage, where the two-stages filter is implemented by changing the size of the last two stages. The reliability of the circuit is evaluated again after adding the filter stage to the circuit. The new results show a remarkable improvement in circuit reliability, where most of the generated SETs are attenuated, and the error probability is decreased by around 99% at some Vdd values, which is considered to be a dramatic decrease in error probability. However, the duration of those SETs which were not attenuated decreased by around 50%, which leads to a decreased chance of these SETs being captured by the output flip-flop. By adding this stage to a circuit, the performance of the circuit is reduced by around 3% to 7%, and the energy consumption of the circuit is increased by different values depending on the filter strength; for the strongest filter it was between 10% to 65%. These values

represent the worst case; however, they are considered acceptable values in the light of the improvements in reliability.

A passive filter stage is proposed for use with large circuits to reduce the performance and energy consumption penalties produced by using the active filter stage. This filter stage is implemented using passive components; a resistor and capacitor. The results obtained show dramatic improvements in the reliability of the circuits after adding this filter stage. This improvement varies from one filter to another depending on filter strength. This comes as a result of the elimination of errors due to the filter stage, which reached around 99% in the case of the use of the strongest filter. The passive filter stage is evaluated by studying its effect on circuit parameters such as performance and energy consumption. The results obtained with our technique are compared with results that are reported using various other techniques, they are considered acceptable. However, the level of improvement in reliability that is achieved using our technique is higher than that achieved using the reference technique.

SIMPLIFICATION APPROACH USING EQUIVALENT GATES FOR THE EVALUATION OF THE RELIABILITY OF LARGE CIRCUITS

In this chapter a simplification technique is proposed to estimate an *approximate reliability* of complex circuits where the estimation process is time-consuming. This technique trades-off the accuracy of estimated reliability against estimation time. The results obtained show a high match between the approximate and the exact values of reliability.

6.1 INTRODUCTION

The method that is proposed for the evaluation of the reliability of a circuit in this work is based on dividing the problem into two levels of characterization. The first level is involved in representing the cause of the fault and the second with finding the boundaries between error and no-error zones (the CVM). The latter needs a number of simulation runs to be accomplished. For small circuits, these simulations can be completed in a short time, but in the case of large circuits or systems they may take a long time to finish depending on the complexity of the object under test. Thus, it is important to find a technique to approximate the estimated reliability leading to decreased estimation time.

During the calculation of the probability of error of combinational circuits, we noticed that the effect of electrical masking on the propagation of glitches depends on the value of the Vdd applied to the CUT. So, it increases at low voltages due to increases in the inertial delay of the stage in which the glitch propagates. Based on this observation, an approximation approach is proposed which depends on the equivalence of the gates within the same path. The equivalence of gates can be seen in Fig. 6.1, where the error probabilities of individual gates that are chosen from a path are calculated and shown. The figure can be divided into two regions. the first region at very-low voltages (Vdd<0.6 V) and the second region at around the nominal voltage of 0.6 V≤Vdd≤2 V. At very-low voltages, the location of the gate has a big impact on the error probability of that gate. This is because of the attenuation effect

on the generated glitches changes according to the location of the faulty gate, where it decreases in the case of faulty gates located near the primary output. So, gates can be divided into equivalent gates and non-equivalent gates. Equivalent gates are located near to each other and far from the primary output of the circuit, and non-equivalent gates are those located near the primary output and their error probabilities differ from one gate to another. On the other hand, in the voltage range 0.6 V⩽Vdd⩽2 V, all gates have nearly the same impact on the overall error probability of a circuit. Accordingly, the suggested simplification approach is divided into two sub-sections depending on operating region. The first sub-section is for around nominal voltage, and the second is where very low voltages are applied.
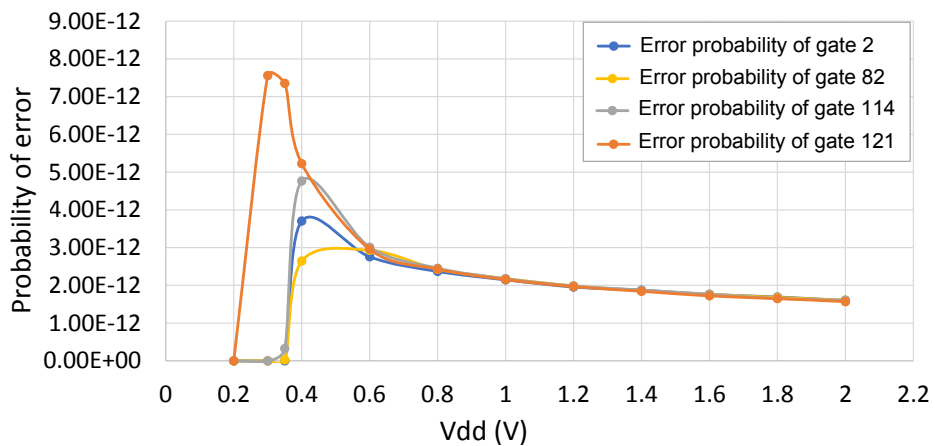
Figure 6.1: Average error probability of different gates selected from different locations within a single path circuit.

6.2 APPROXIMATE RELIABILITY OF DIFFERENT PATH TOPOLOGIES

The simplification technique is applied to different path topologies which can be found in any multipath circuit. The structure of these topologies helps in understanding the core idea of the simplification technique, and how we can differentiate between equivalent and non-equivalent gates.

6.2.1 *At Around Nominal Voltage*

This section introduces the use of the simplification technique at 0.6 V ⩽ Vdd ⩽ 2 V. In this voltage range, the effect of all gates in a path on the overall error probability is nearly equal. This is because the electrical masking that

causes an attenuation in generated glitches does not change significantly in adjacent gates. This causes a negligible change in the duration of the propagated glitches.

The simplification formula that is proposed to estimate the approximate reliability in this voltage range is:

$$P_{err} = m * P_{err}^{Ij}, \tag{6.1}$$

where m is a constant representing the number of vulnerable gates, and P_{err}^{Ij} is the error probability of a gate (j). We recommend choosing a value of j at the end of the path to reduce the number of simulated gates, which leads to significantly reduced simulation time.

The first example is a single path that was introduced in Section 3.4, which is chosen to show how the simplification technique can be used to estimate the approximate reliability of a single path. The block diagram of this path is shown in Fig. 6.2, and it is constructed from various types of gates; NAND, NOR, and NOT.
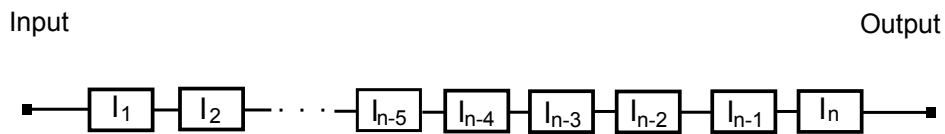
Figure 6.2: Block diagram of a single path-circuit containing n gates.

The approximate error probability of the circuit is calculated several times using (6.1). Each time, we choose a gate from a different location in the path, where a different value of j is chosen to find the value of P_{err}^{Ij}, and then it is multiplied by the number of vulnerable gates within the path. This enables us to explore the effect of gate location on the accuracy of the approximate reliability. As a result, several approximate error probabilities for the circuit have been obtained, as shown in Fig. 6.3. In this figure, we are interested in the error probability curves from Vdd=0.6 V to 2 V, where all of the approximate error probabilities match the exact one.

The accuracy of the approximate error probabilities for the circuit is calculated by comparing the approximate error probability with the exact one in each case. The error caused by using the approximation formula, which is called *the approximation error* in the rest of this Chapter, is shown in Table
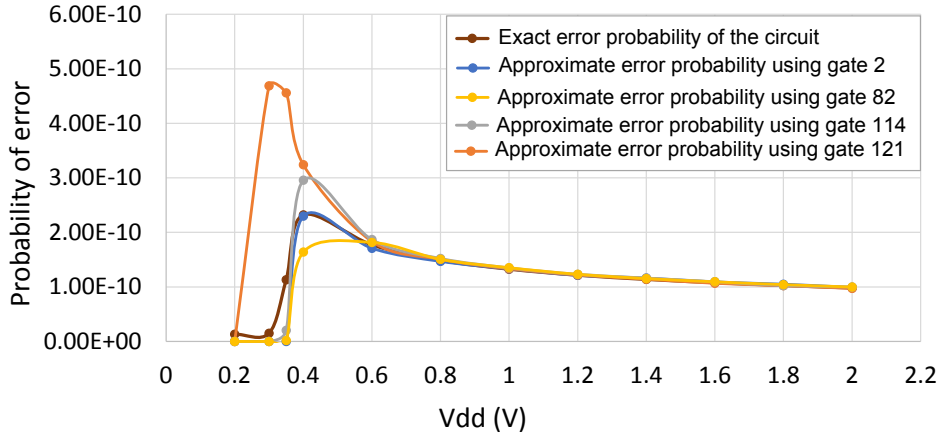
Figure 6.3: Overall error probability of the path calculated by using both exact and approximate approaches.

6.1. As can be seen in the table, the approximation error caused by using the error probability of the gate No.121 is the lowest. However, in general, all values of approximation error can be considered to be acceptable.

Table 6.1: Approximation error caused by calculating the overall error probability using the error probability of different gates in the path (%).

Vdd (V)	gate 2	gate 82	gate 114	gate 121
2.0	1.0	1.8	1.8	0.8
1.8	2.23	1.5	0.2	0.4
1.6	1.3	1.5	1.5	1.0
1.4	2.1	1.3	2.1	0.4
1.2	0.2	1.3	1.3	0.3
1.0	0.4	2.0	1.8	0.7
0.8	1.3	1.3	2.3	1.3
0.6	3.5	2.5	5.5	3.5
Avg.	1.5	1.7	2.1	1.1

The approximate reliability of the path has been obtained by using the approximate error probability of the circuit calculated using the error probability of the gate No. 121 as shown in Fig. 6.4. It can be seen from the figure that the approximate reliability and the exact reliability of the path are very close to each other.

The second example is another type of path topology, which includes divergent paths. This topology is common in multipath circuits, where a certain
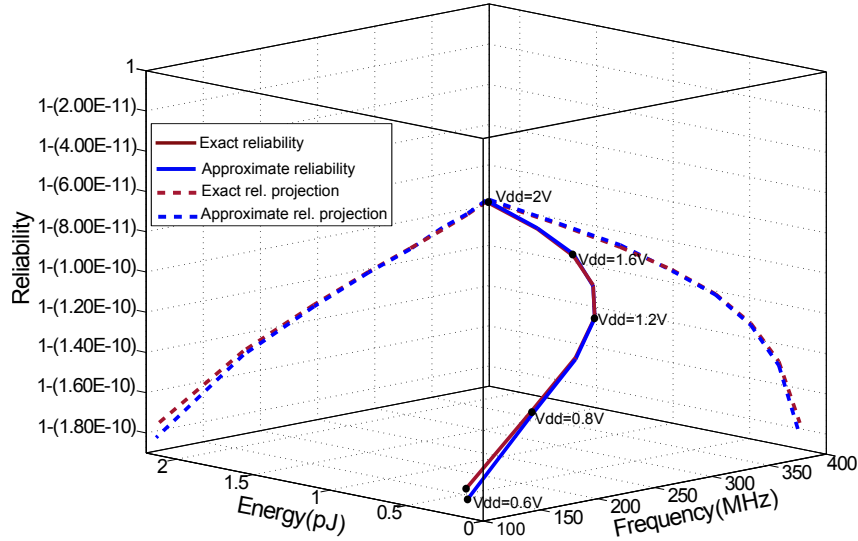
Figure 6.4: Approximate and exact reliability for the single path with the Vdd range
0.6 V⩽Vdd⩽2 V.

gate drives more than one fan-out. The structure of this kind of path is shown
in Fig. 6.5.
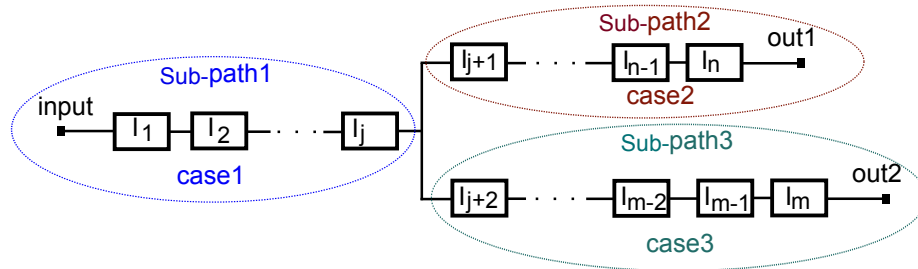
Figure 6.5: Block diagram of a circuit with forked path topology.

In order to estimate the approximate reliability of this topology, the circuit
is divided into three sub-paths. The gates in each sub-path contribute to the
overall error probability to unique extents which may differ from the gates in
the other sub-paths depending on the location and the number of these gates.
In terms of error probability, sub-path1 has unique characteristics compared
with the other sub-paths, where any glitch generated in this sub-path may
propagate to both output terminals out1 and out2. This leads to an increased
error probability for any gate in this sub-path. However, any glitch generated
in sub-path2 or sub-path3 may propagate to either out1 or out2. As a result

of this, the error zone that determines the error probability of any gate in sub-path1 is wider than the corresponding zones in sub-path2 or sub-path3, as can be seen in Fig. 6.6. The expansion that has occurred in the error zone of sub-path1 is caused by the difference between the propagation times of sub-path2 and sub-path3. So, the arrival of the glitch at the output terminals at different times increases the probability of that glitch being latched by the output flip-flop. This difference in the error zones affects the error probabilities of these sub-paths, as can be seen in Fig. 6.7. Because of the similarity in the error probabilities of the gates of sub-path2 and sub-path3, the approximate error probability of those two sub-paths can be calculated using the error probability of any gate from either of them and aggregating them to both sub-paths. This assumption is adopted here in calculating the approximate error probability of the whole path circuit using the least possible numbers of simulated gates.

(a) Error zone of case 2

(b) Error zone of case 3

(c) Error zone of case 1
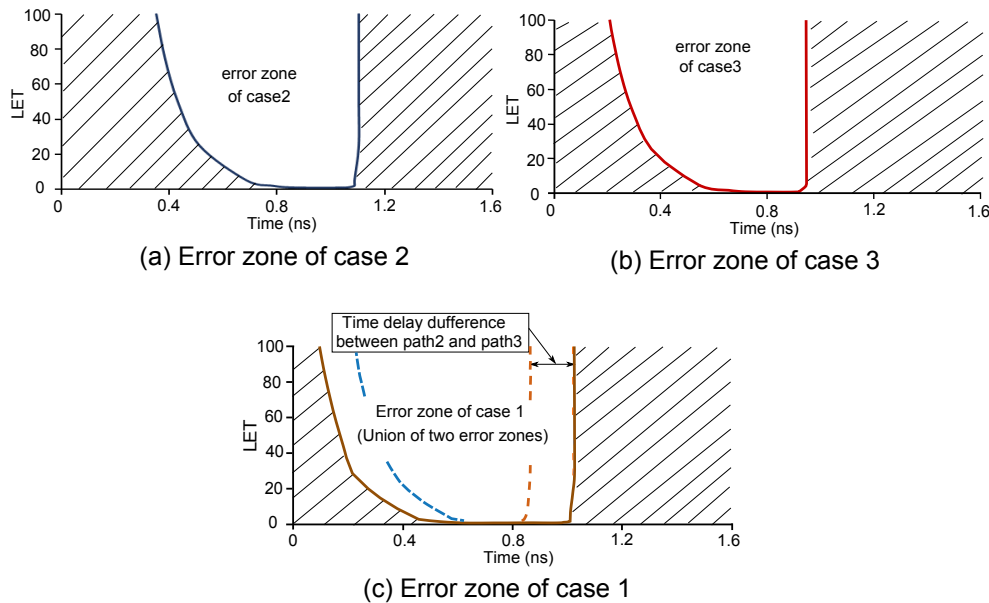
Figure 6.6: Error zones of different gates chosen from different sub-paths.

To estimate the approximate reliability of this kind of path, we have applied the same simplification formula in 6.1 to just two sub-paths: sub-path1, and either sub-path2 or sub-path3. So, for these two sub-paths, the same procedure as in the first example has been followed. The approximate error probability of sub-path1, P_{err1}, is calculated by applying 6.1 to this sub-path. One gate is chosen at the end of the sub-path to reduce the simulation time, and the error probability of that gate is multiplied by the number of the vulnerable gates in sub-path1. As the gates of the two sub-paths (sub-path2,
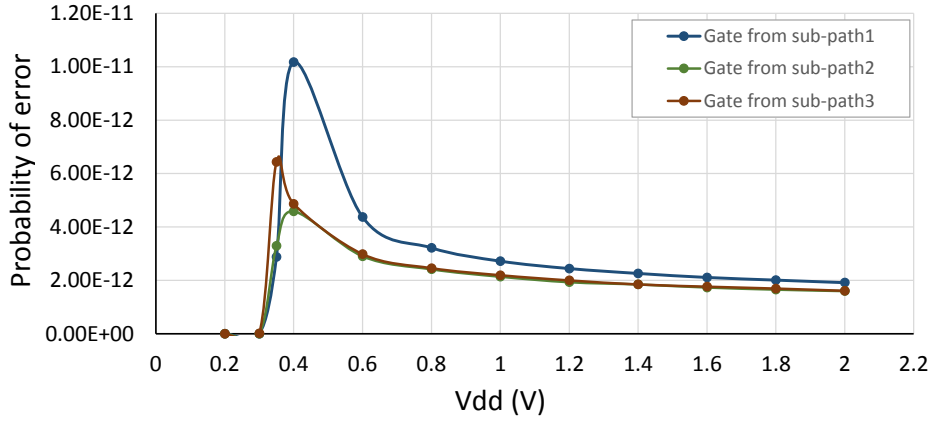
Figure 6.7: Error probability caused by different gates located in different sub-paths.

and sub-path3) are equivalent to each other, so one gate from one sub-path is chosen to calculate its error probability, then this value is multiplied by the number of the vulnerable gates on both sub-paths. P_{err2} represents the error probability of sub-path2 and sub-path3. The overall error probability is calculated from the summation of these two error probabilities $P_{err} = P_{err1} + P_{err2}$.
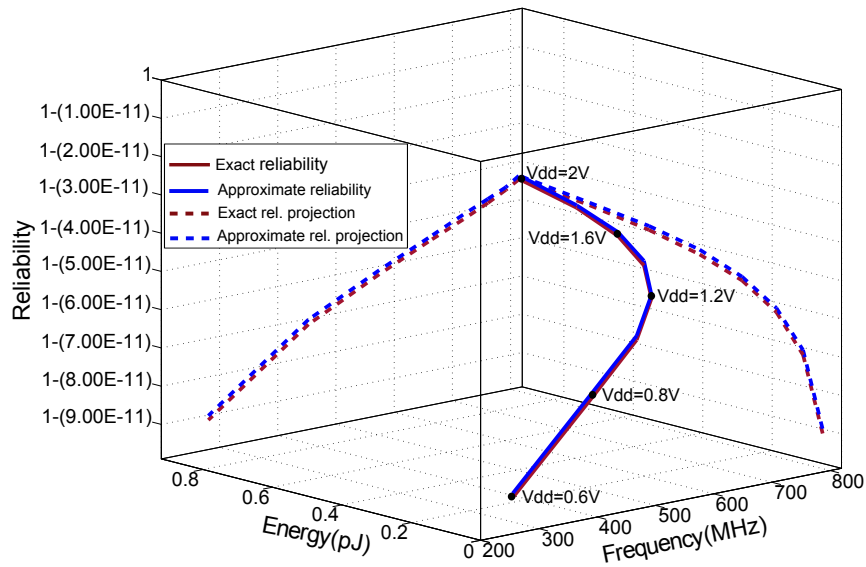
Figure 6.8: Approximate and exact reliability of the divergent path for the Vdd range: 0.6V⩽Vdd⩽2V.

Both input values of 0 and 1 are applied to the path and the overall error probability is calculated as the average value of the two error probabilities obtained. Then the approximate reliability of this topology is calculated as shown in Fig. 6.8. The exact reliability is also calculated in order to compare the two trends. The approximate reliability matches the exact one.

The difference in propagation delay of sub-path2 and sub-path3 can be reduced by reducing the difference between the lengths of those two sub-paths. Also, it can be reduced by adding a filter or a buffer stage at the end of short paths to add the required delay so that both signals arrive at the output terminals at the same time.

The third example is a topology with reconvergent paths, and the structure of this topology can be seen in Fig. 6.9.
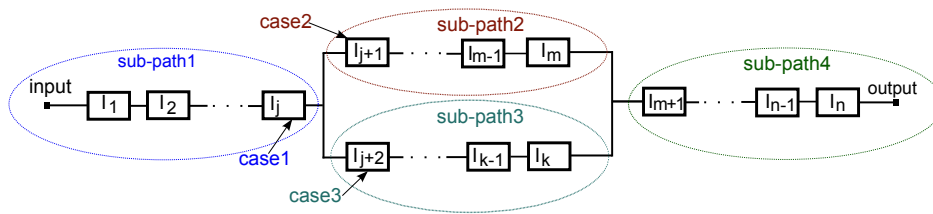
Figure 6.9: Block diagram of a reconvergent topology path circuit.

In order to apply our simplification approach to this topology, it is divided into four sub-paths, sub-path1, sub-path2, sub-path3, and sub-path4. Any glitch generated in sub-path1 has three different scenarios in propagating to the primary output. The first is that this glitch may propagate through instance I_{j+1} and be masked at instance I_{j+2} to arrive at the output terminal through sub-path2. The second scenario is that it may propagate through instance I_{j+2} and be masked at I_{j+1} to arrive at the output terminal through sub-path3. The third scenario is that it may split into two glitches, and those propagate through both sub-paths (sub-path2 and sub-path3). In this case, the two propagated glitches recombine again at the fan-in instance I_{m+1}, and the new glitch may be wider or narrower than the original glitch depending on the arriving time and the type of recombining instance. The arrival time is related to the number of instances in sub-path2 and sub-path3, and the type of instance depends on the circuit structure. The recombination cases of the split glitch can be seen in Fig. 6.10.

The gates of each sub-path contribute to the overall error probability by approximately the same values. So, the error probability of each sub-path is calculated using (6.1) by simulating one gate from each sub-path to calcu-
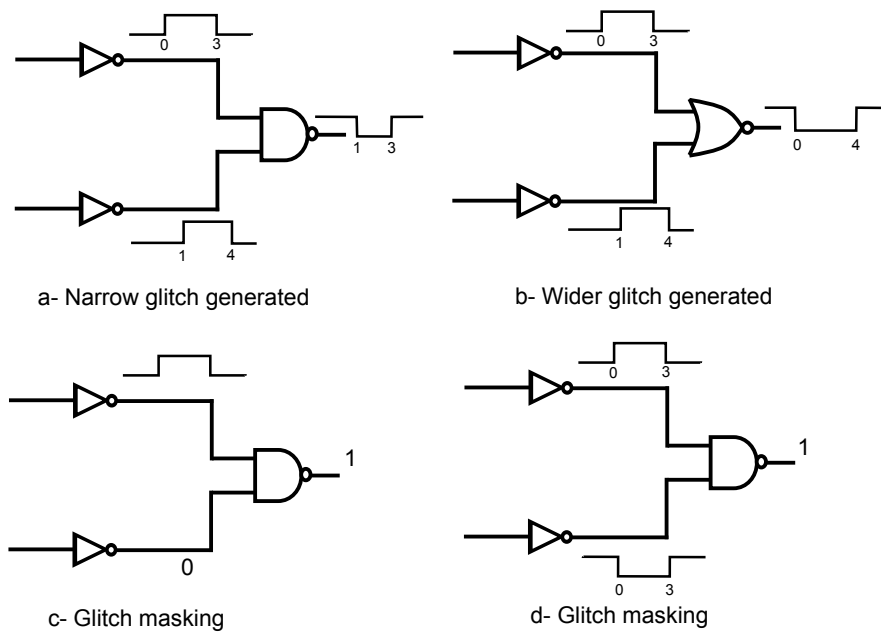
Figure 6.10: The possible recombination cases of tow glitches propagated through two different sub-paths.

late its error probability and then multiplying this value by the number of vulnerable gates in that sub-path. The error probability of sub-path1 is P_{err1}. The approximate error probability of sub-path2 and sub-path3, P_{err2}, is found using the same process as in the previous example. The error probability of sub-path4 P_{err4} is calculated by calculating the error probability of a chosen gate and multiplying it by the number of vulnerable gates.

The approximate error probability of each sub-path is calculated for the two input values of 0 and 1. The summation of the average of these error probabilities has been found, which is the approximate overall error probability. By using the approximate overall error probability, the approximate reliability of this topology path is calculated and shown against the exact reliability in Fig. 6.11. As seen in the figure, the approximate reliability trajectory is very close to the exact one.

6.2.2   *Including Very Low Voltages*

In this section, another simplification formula is introduced, which is valid at the nominal voltage and very low voltages (0.2 V$\leqslant$Vdd$\leqslant$2 V). This formula is proposed based on the behaviour of the gates at very-low voltages, as can be seen in Fig. 6.1. In this figure, the error probability of prior stages within a
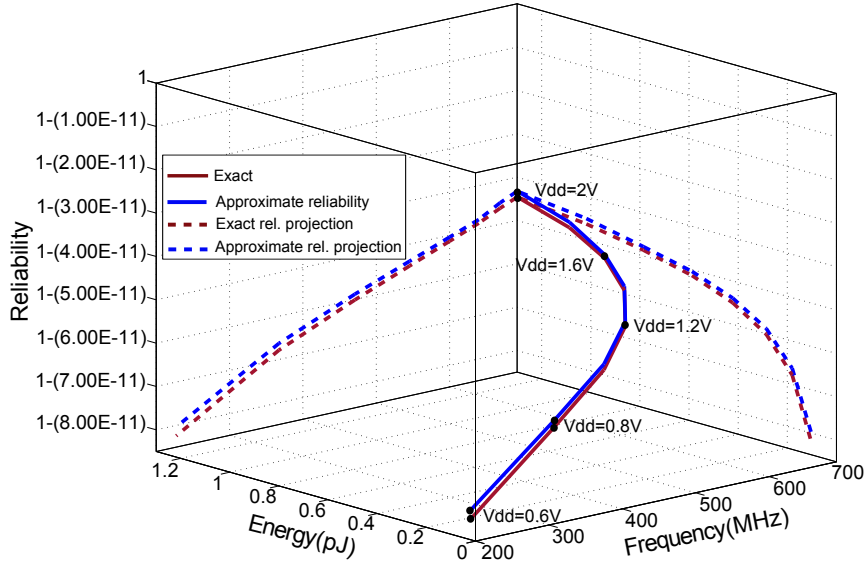
Figure 6.11: Approximate and exact reliability of the reconvergent path for the Vdd range: 0.6V⩽Vdd⩽2V.

path is negligible at very low voltages (Vdd⩽0.4 V) because of the attenuation effect. However, in the case of stages that are close to the output terminal, the duration of generated glitches is quite wide, and they have a tremendous effect on the overall error probability. Therefore, the last six or five gates in a path should be included in the formula that is suggested to approximate the reliability of digital circuits at very low voltages. This formula is introduced in (6.2).

$$P_{err} = m * P_{err}^{I_j} + \sum_{k=n-4}^{n} P_{err}^{I_k}, \qquad (6.2)$$

where n is the number of all vulnerable gates within a path, and m is the number of vulnerable gates located away from the output terminal (equivalent gates). We adopt a value of m=n-5. $P_{err}^{I_j}$ is the error probability of a gate that is chosen from the equivalent gates. $P_{err}^{I_k}$ is the error probability of the last five gates connected to the primary output (the non-equivalent gates), k= n-4, n-3, n-2, n-1 and n.

(6.2) is constructed using two terms, the first for the equivalent gates (the multiplication part), and the other for the non-equivalent gates (the summation part). The accuracy of values of approximate reliability derived

using this formula can be adjusted according to requirements. So, if accuracy is more important, we need to increase the number of gates that are used in the summation part to include more gates from the non-equivalent gates. On the other hand, to reduce the estimation time, the number of gates that are used in the multiplication part should be increased.

The same examples of topologies that were used in the previous section have been also used in this section.

The first example is the single-path circuit illustrated in Fig. 6.2 which is used to evaluate approximate reliability. A gate from the path is chosen to calculate its error probability. This gate represents gate j in (6.2). In this case, the path is constructed using 125 gates, of which there are 62 vulnerable gates, so n=62 and m=57. The error probability of the last five gates in the path is calculated and included in the summation part of the formula, and those for the rest of the vulnerable gates are used in the multiplication part.

The approximate reliability of the path is calculated and shown against the exact value of reliability in Fig. 6.12. The figure shows that the approximated reliability trajectory matches the exact one, with only minor deviation.
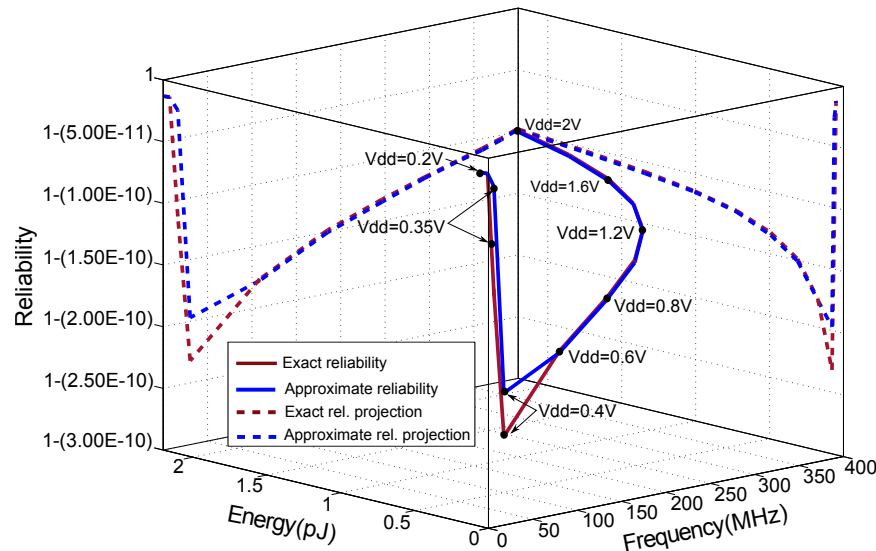
Figure 6.12: Approximate and exact reliability of the single path at the Vdd range from 0.2 V to 2 V.

The second example is the divergent path that is illustrated in Fig. 6.5. The same procedure as in the previous section is followed for this type of path, and so it is divided into three sub-paths: sub-path1, sub-path2 and sub-path3.
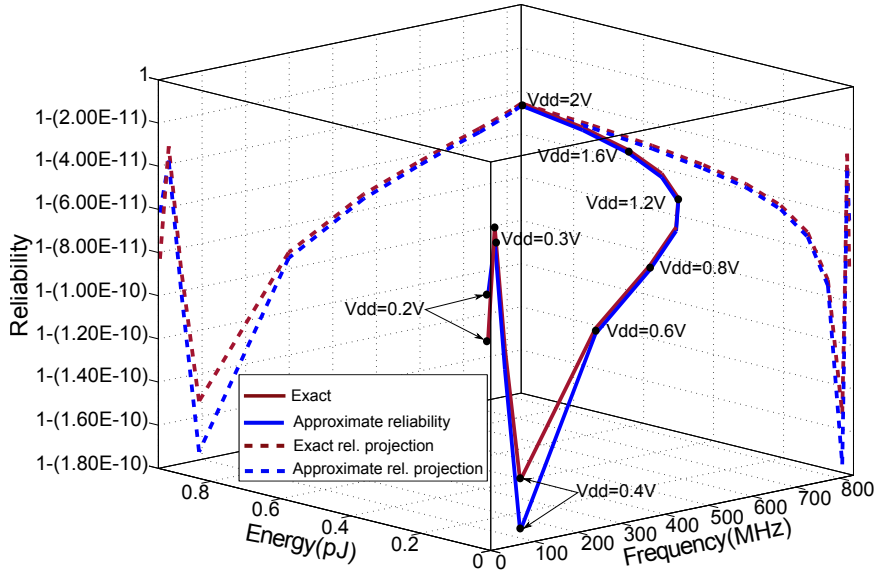
Figure 6.13: Approximate and exact reliability of the divergent path in the Vdd range
$0.2 \text{ V} \geqslant \text{Vdd} \leqslant 2 \text{ V}$.

The approximate error probability of sub-path1 is found by using the first part of (6.2) (the multiplication part) because this path is not connected to the output terminals directly and all gates on this sub-path are equivalent. The error probability of one gate in the middle of the path has been calculated and multiplied by the number of vulnerable gates on sub-path1. However, the approximate error probability of the other two sub-paths is calculated using both terms of (6.2) (multiplication and summation). Due to the equivalence of the structure of the two sub-paths, it is sufficient to choose one gate from one sub-path and to use aggregation for the two sub-paths. So, one gate has been chosen from sub-path2 whose error probability is calculated and multiplied by the number of vulnerable gates in both sub-paths. The last five vulnerable gates within sub-path2 have been simulated to find their error probability and applied to the second part of (6.2).

The approximate reliability of this topology is compared to the exact one in Fig. 6.13. The figure shows high matching between the approximate and exact reliability trajectories.

The third example is the reconvergent topology that is shown in Fig. 6.9. In this example, the approximate error probability of sub-path4 is calculated using both terms of (6.2). However, the approximate error probability of the

three other sub-paths is calculated by using the multiplication part of the formula.
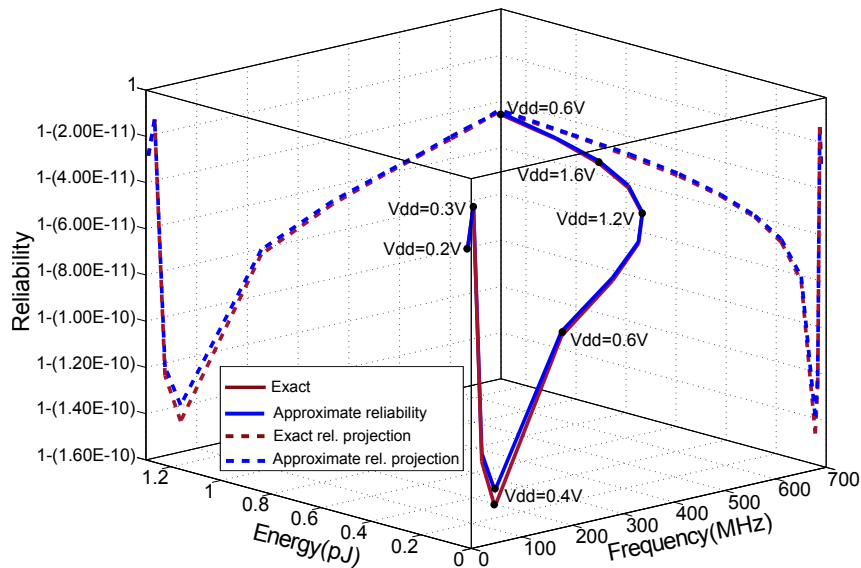
Figure 6.14: Approximate and exact reliability of the reconvergent path in the Vdd range: 0.2 V⩾ Vdd ⩽2 V.

The approximate reliability of this path is found and shown in Fig. 6.14. The figure shows that there is a high similarity between the exact and approximate reliability trajectories.

6.3 ESTIMATING THE APPROXIMATE RELIABILITY OF COMPLETE CIRCUITS

In this section, we show how the simplification approach can be applied to complete circuits to find their approximate reliability.

In the case of evaluating the approximate reliability of paths, we were interested in the equivalent and non-equivalent gates. This concept can also be applied to complete circuits provided that equivalent gates are found. This can be achieved by extracting the sensitive paths of the whole circuit. These paths are constructed using a group of sensitive gates which enable any generated glitch to propagate and arrive at the primary output of the circuit without any logical masking. In terms of sensitivity, logical gates can be categorised into two types. The first type of gates are always sensitive regardless of their input value, such as NOT, XOR and XNOR. The second

type have sensitivity depending on their input values, such as NAND, NOR, OR and AND.

The flowchart of the process used to calculate the approximate reliability of a combinational circuit is shown in Fig. 6.16, and the pseudocode of this process is introduced in Algorithm 6.1. It starts by applying an input combination to the circuit as initial values of their input terminals. These values are propagated through the whole circuit. Then, by using forward tracking, all the sensitive gates and their sensitive inputs are recognised and marked. By using backwards-traversing search, the sensitive paths are built starting from the primary output gates. Any sensitive path ends when a non-sensitive gate is found or if a primary input terminal of the circuit is arrived at. Then, the sensitive paths obtained are categorised according to type of path topology in order to find the equivalent gates and the equivalence between sub-paths. It is noticed that most of the paths have a divergent path topology, with differences in the numbers of forked paths. Vulnerable gates are found and categorised into groups depending on the contribution of each gate to the overall error probability of the circuit. So, by knowing the number of times the gate has appeared in the sensitive path list, we can know how much that gate contributes to the overall error probability. For example, consider the path topology shown in Fig. 6.15(a), and the extracted sensitive paths of this topology shown in Fig. 6.15(b). The gates are categorised into four different groups. Group 1 represents the gates that have the highest impact on the error probability of the circuit, due to their existence in all the sensitive paths. Group 2 contains gates which appear in three sensitive paths. Group 3 contains gates appearing in two sensitive paths, and group 4 contains gates appearing just once in the sensitive paths.

Any vulnerable gate is not included in the sensitive paths, but is discarded, because any glitch generated in that gate will be blocked by the logical masking effect. Then, from each group, a gate is chosen to calculate its error probability and this is multiplied by the number of vulnerable gates in that group.

A subcircuit that includes the chosen gates is selected and simulated. Simulating a small subcircuit rather than the whole circuit speeds up the simulation process dramatically.

(a) Block diagram of a path topology

(b) Sensitive paths with categorized gates
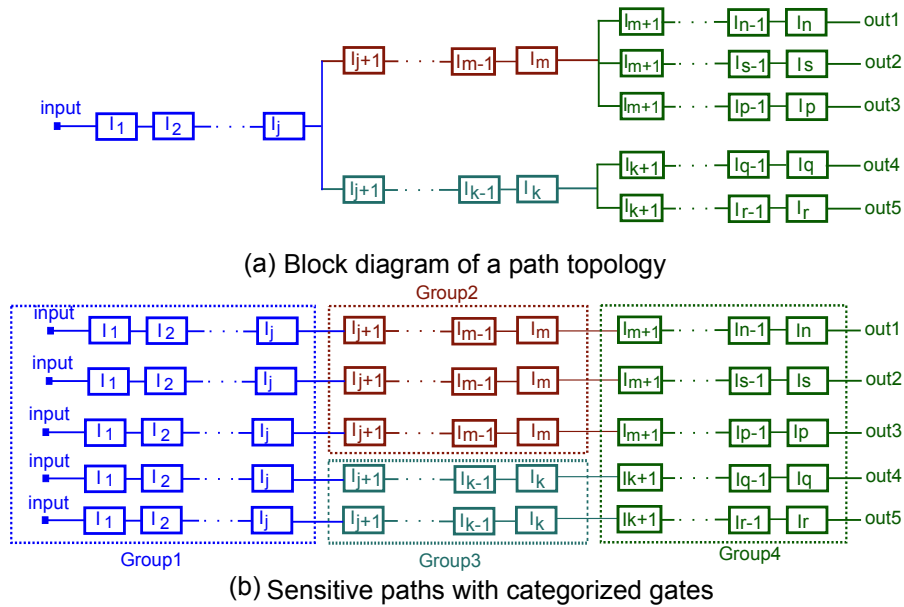
Figure 6.15: Sensitive paths extracted from a path topology to explain the method used to categorise the equivalent gates.

6.3.1 Around Nominal Voltage

Two benchmark circuits are chosen as examples to evaluate their approximate reliability. These two circuits are c432 and c1908.

The first example is the c432 benchmark circuit, and its specifications are introduced in Table 4.1. To apply the simplification technique to this circuit, the sensitive paths have been extracted using Algorithm 6.1 for a specific input combination. These paths are categorised depending on their topology. Then the vulnerable gates are categorized according to their contribution to the overall error probability of the circuit. By using (6.1) the approximate error probability of the circuit has been calculated. This process is repeated for different input combinations which are selected randomly, and different values of circuit reliability have been obtained. The average of these values is found and shown in Fig .6.17 along with the exact reliability value. As can be seen in the figure, the approximate reliability is very accurate compared with the exact one.

The same procedure as used in Section 6.2 is followed. So, the approximate reliability is found in both cases of around the nominal voltage and around the whole voltages range.

The second example is the c1908 benchmark circuit, and the specifications of this circuit can be found in Table 4.1. The sensitive paths of the circuit are
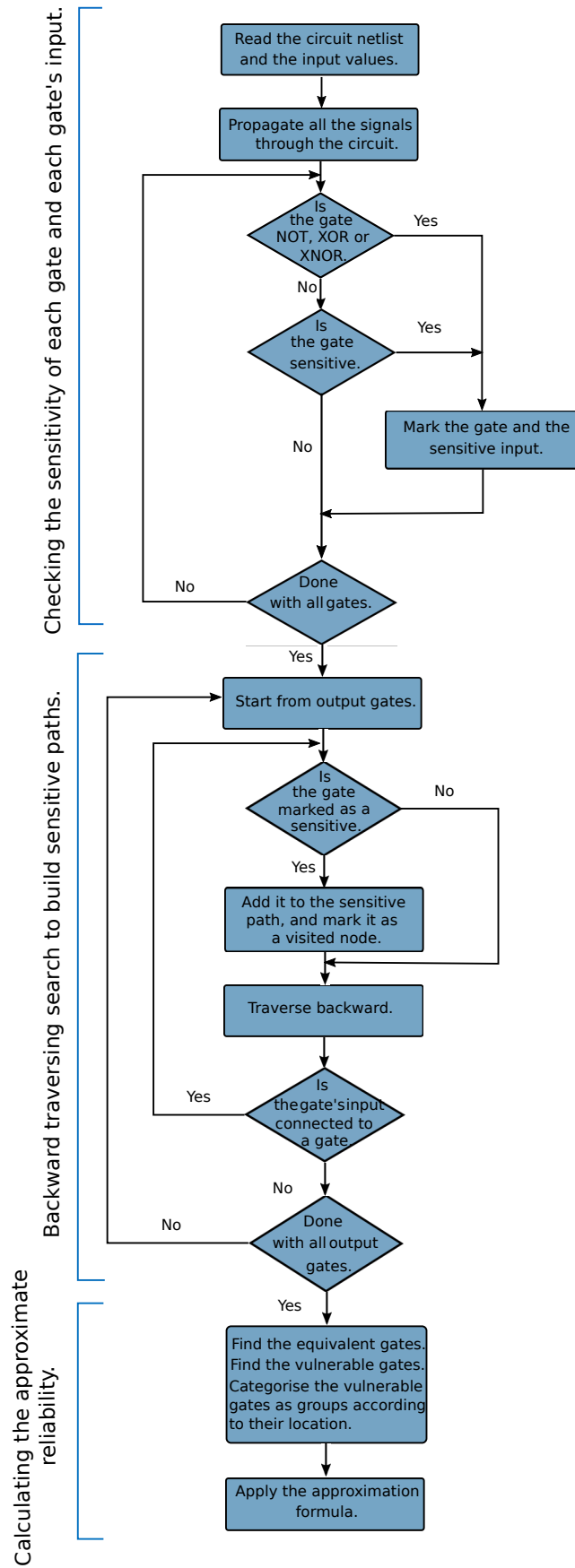
Figure 6.16: The flowchart of the process that is followed to calculate the approximate reliability of a combinational circuit.

Algorithm 6.1 Finding the sensitive paths and vulnerable gates of large circuits to apply the simplification approach.

1: Enter the input values
                                    ▷ Forward simulation performed in linear time
2: Propagate all the signals through the circuit
                        ▷ check the sensitivity of each gate and each gate's input
3: **for** Each gate i in the netlist **do**
4:     Determine the type of the gate
5:     **if** The gate is NOT, XOR or XNOR **then**
6:         Mark the gate and its input as sensitive
7:     **else**
8:         Test the gate if it is sensitive or not
9:         **if** The gate is sensitive **then**
10:            Determine which input is sensitive
11:            Mark the gate as a sensitive gate
12:            Mark the sensitive input
13:        **end if**
14:    **end if**
15:    Save all the sensitive gates and nodes
16: **end for**
                            ▷ Backward traversing to build the sensitive paths
17: **for** Each output gate on the circuit netlists **do**
18:     **if** This gate is marked as sensitive **then**
19:         Add the gate to the sensitive path
20:         Traverse backward and check all gates
21:         Mark all visited nodes
22:         Add any sensitive gate to the sensitive path
23:         **if** Not sensitive gate is found or the input terminal is
    arrived **then**
24:             Stop and start over from unvisited gate
25:         **end if**
26:     **end if**
27: **end for**
        ▷ Find the equivalence between gates and apply the approximation
    formula
28: **for** All the sensitive paths **do**
29:     Find the equivalent gates
30:     Find the vulnerable gates and categorise them to different groups
31:     Apply the formula to find the error probability of the circuit
32: **end for**

---

obtained and the vulnerable gates are categorised using Algorithm 6.1. Due to the complexity of the circuit, the number of forked paths was higher than in the circuit in the previous example. This leads to an increase in the number of gates chosen to represent the vulnerable gates in the circuit. By using
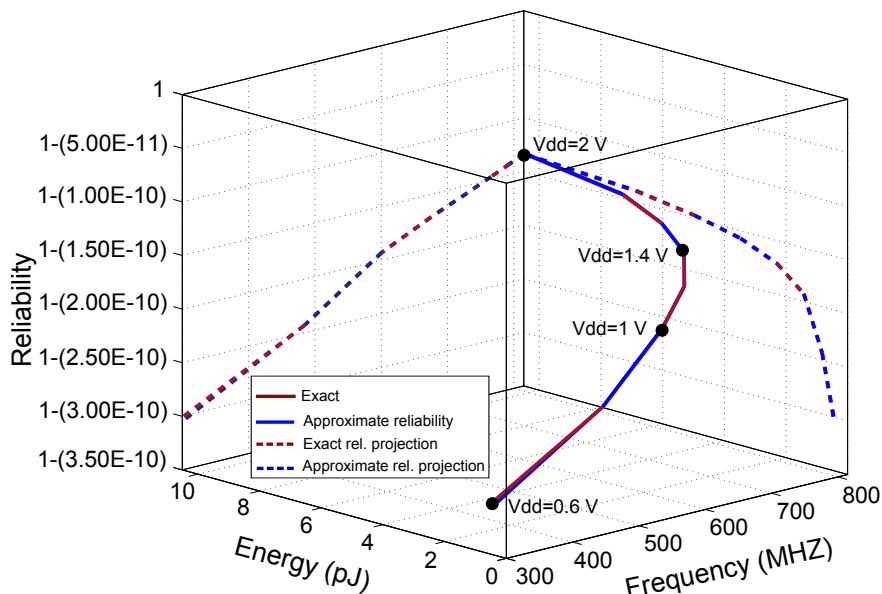
Figure 6.17: The approximate reliability and the exact reliability of the circuit c432 in the range 0.6 V⩽Vdd⩽2 V, it shows a minor contrast between two trajectory.

(6.1) the approximate error probability of the circuit has been calculated. For different input combinations, different approximate values of circuit reliability are obtained. The average of these values is found and compared with the exact reliability value in Fig. 6.18. The approximate reliability shows high accuracy compared with the exact reliability.

6.3.2 *Including Very-Low Voltage*

In this section, the simplification formula in (6.2) is used to evaluate the approximate reliability of the previous two circuits. In this case, we need to include more gates from the non-equivalent gates for the simplification formula for the sub-paths that are connected to primary outputs.

The first example, the approximate reliability of the circuit c432 is evaluated. The same procedure that was followed in the previous section is applied to this case. However, for the sub-paths that are connected to the primary outputs, the error probabilities of at least five vulnerable gates is calculated and included in the error probability calculation formula, as is done in Section 6.2.2.
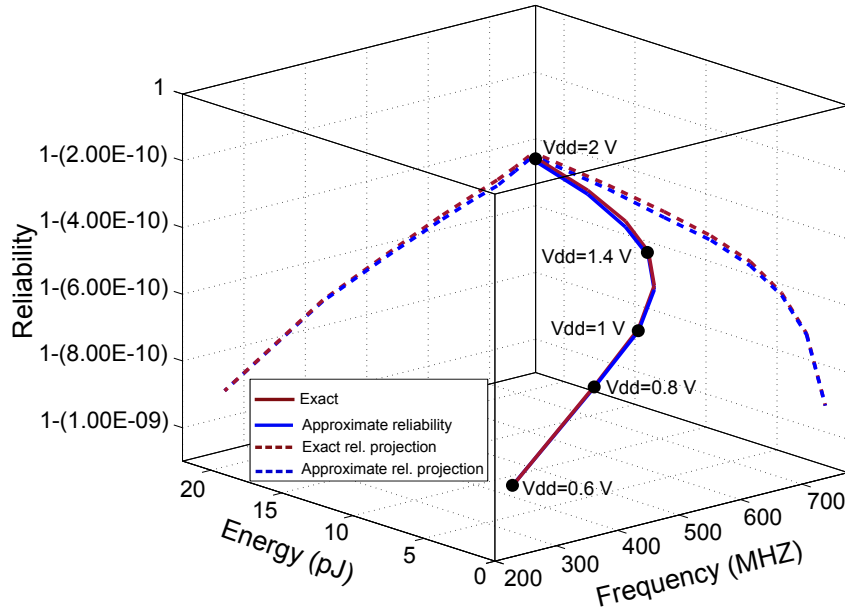
Figure 6.18: Approximate and exact reliability of circuit c1908 in the range: 0.6 V⩽Vdd⩽2 V, showing a minor contrast between the two trajectories.

The approximate reliability of the circuit is calculated by using the average of the error probabilities which are obtained for different input combinations. Fig. 6.19 shows the approximate reliability and the exact reliability, and it can be seen that both trajectories are very close to each other.

Due to the random selection of a group of input combinations to calculate the approximate reliability of the circuit, we need to estimate the convergence between the values of reliability obtained to stop the calculation process. The same procedure is used as explained in Chapter 4, and so the standard error metric is used to calculate the level of convergence. The convergence between the results is shown in Fig. 6.20. As can be seen in the figure, convergence between the results obtained first appeared after applying 10 input combinations. The estimation process is stopped after applying 15 input combinations to the circuit, where an acceptable convergence between the results has occurred.

The second example is evaluating the approximate reliability of circuit c1908. The same procedure is followed as for c432 circuit, but the number of gates chosen is larger in this case due to the length of some paths and the complexity of the circuit. The error probabilities of the last five vulnerable gates are included in the calculation of the approximate error probability of the circuit in the case of paths that are connected to primary inputs. The
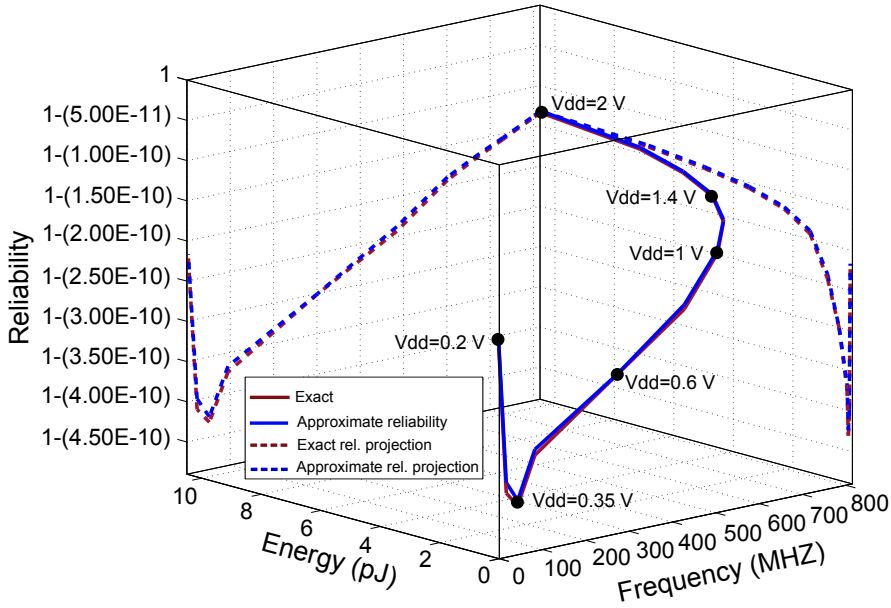
Figure 6.19: Approximate and exact reliability of circuit c432 in the range: 0.2 V⩽Vdd⩽2 V, showing a minor contrast between the two trajectories.
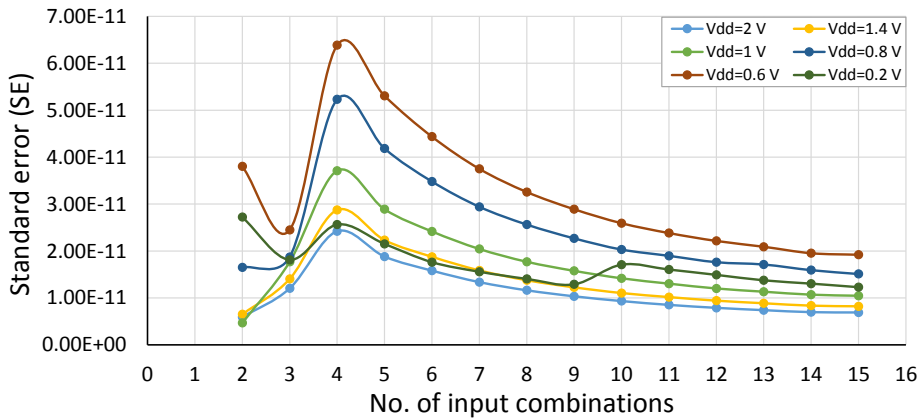
Figure 6.20: Standard error calculated for the error probabilities of different input combinations of circuit c432, showing a convergence in the results after 12 input combinations.

(6.2) is used to calculate the approximate error probability of the circuit. The approximate reliability of the circuit is calculated and shown with the exact one in Fig. 6.21. The figure shows a high similarity between both reliability trajectories.

Due to the use of various input combinations in evaluating the reliability of the circuit, the convergence between the estimated reliabilities is calculated by using the same procedure as in the last example. So, the standard error
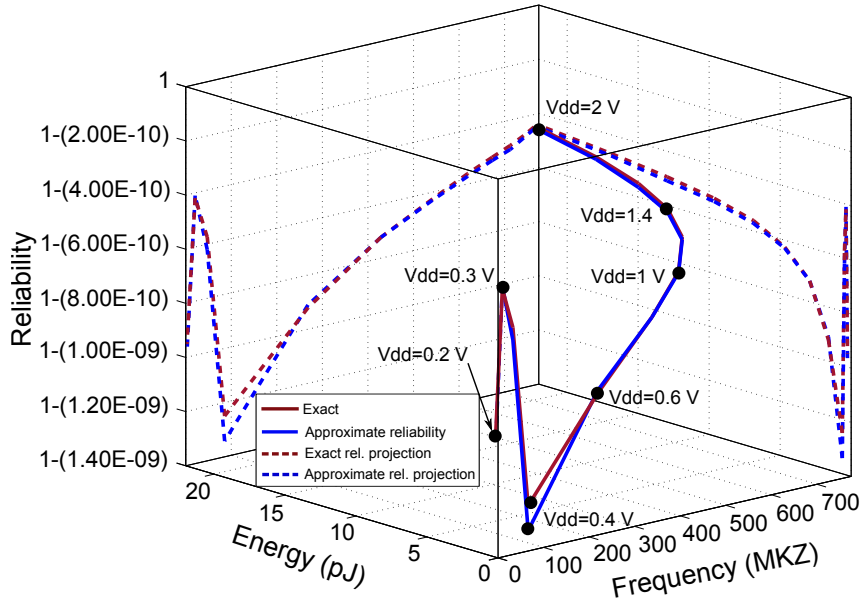
Figure 6.21: Approximate and exact reliability of circuit c1908 in the range: 0.2 V⩽Vdd⩽2 V, it shows a minor contrast between two trajectory.

metric is calculated for all obtained reliabilities and the results are shown in Fig. 6.22. The figure shows that convergence between the obtained results starts after applying 10 input combinations to the circuit. The estimation process is stopped after obtaining the error probability of the circuit for 15 input combinations.
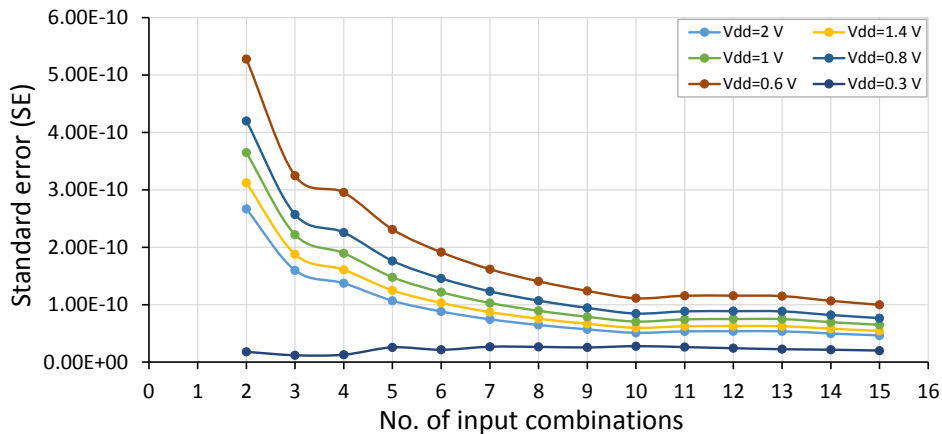
Figure 6.22: Standard error calculated for the error probabilities of different input combinations of circuit c1908, showing a convergence in the results after 10 input combinations.

6.4   EVALUATION OF THE SIMPLIFICATION APPROACH

Table 6.2: Reduction in simulation time and approximation error obtained from applying the approximation approach at the range (0.6 V$\leqslant$Vdd$\leqslant$2 V).

Circuit type	No. of gates	Time reduction	Approximation error
Single path	125	93x	3.5%
Divergent path	52	21x	2.3%
Reconvergent path	72	19X	3.1%
c432	274	60x	1.3%
c1908	1211	173x	3.5%

The use of the proposed simplification technique for evaluating the approximate reliability of combinational circuits leads dramatically reduced simulation time. However, this reduction is associated with an imprecision in the evaluation of reliability, which is called in this work the approximation error. The reduction in simulation time and approximation error are calculated at the nominal voltage range for all the previous examples and the results are shown in Table 6.2. The approximate error in this table is calculated as the average value of all the approximate errors that are calculated at different Vdd values. As can be seen in the table, with increases in the number of gates in a circuit, the reduction in simulation time increases. So, this reduction has an exponential relationship with the number of gates within a circuit. However, in the case of divergent and reconvergent path topologies, the time reductions were 21x and 19 x respectively because of the difference between the topologies.

Due to the inclusion of more gates in the simplification formula that has been suggested in order to obtain the approximate reliability in the low voltage range, the simulation time increases compared with the other formula. This is also applicable to the approximation error, which increased too. The reductions in simulation time and approximate error percentages for all previous examples can be found in Table 6.3. In general, the use of the simplification technique in the voltages range from 0.2 V to 2 V achieves a noticeable acceleration in the evaluation process, with an acceptable reduction in the accuracy of the results.

Table 6.3: Percentage error and time saved obtained from applying the approximation approach at the Vdd range (0.2 V$\leqslant$ Vdd $\leqslant$2 V).

Circuit type	No. of gates	Time reduction	Approximation error
Single path	125	30x	8.1%
Divergent path	52	9x	5.1%
Reconvergent path	72	12X	4.7%
c432	274	24x	3.2%
c1908	1211	74x	7.4%

6.5 CONCLUSIONS

In this chapter, a simplification approach is introduced. This approach is proposed to tackle the problem of time consumption when evaluating the reliability of large circuits. The proposed approach relies on dividing the gates of any combinational circuit into two groups: equivalent and non-equivalent gates. The equivalent gates are those which contribute to the overall error probability of the circuit by nearly the same value. The equivalence property of the gates depends on two main factors: the voltage applied to the circuit and the location of the gate. At the nominal voltage, all gates within a path are equivalent. However, at low voltages, the equivalence between gates within a path decreases in the gates located near the output terminal of the circuit.

To show how this approach is used, the operating voltage of a combinational circuit is divided into two ranges: around the nominal voltage range and in the whole voltage range where very low voltages are included. These ranges are proposed due to the difference in the behaviour of the logic gates within the same path in the two ranges. The first voltage range is around the nominal voltage where all gates are equivalent in terms of their contribution to the overall error probability of the circuit. So, the circuit reliability can be evaluated by simulating a few gates which represent all the vulnerable gates in the circuit. By using a simple formula, the error probabilities of the chosen gates are multiplied by the number of the vulnerable gates. The second range is where very low voltages are included in the evaluation range. At this range, the error probabilities of the gates located near the primary output of a circuit are included in the formula that is used to evaluate the reliability of the circuit. This is because their effect is different from that of the other gates within the same path.

This approach is applied with different path topologies and complete circuits. The results show that a dramatic decrease in reliability estimation time is traded-off with the accuracy of approximate reliability.

CONCLUSIONS AND FUTURE WORK

7.1 SUMMARY AND CONCLUSION

Shrinking technology size is providing an opportunity for embedding higher numbers of transistors on a single integrated circuit (IC) chip. It also is the main reason for the decreasing the voltage applied to these ICs. On the other hand, the level of flux neutron particles at ground level is constant. This leads to an increasing need to deal with reliability issues in these circuits. The present thesis addresses two main concerns related the reliability of combinational circuits, which are analysing and improving reliability. In terms of reliability analysis, a new approach is proposed for the evaluation and analysis of the reliability of a circuit along with its performance and energy consumption. In terms of reliability improvement, a new technique is suggested in which standard cells are used.

A new method of deriving the reliability metric for digital circuits has been introduced in this work. The reliability metric is derived without expensive Monte Carlo simulations or physical experiments; however, the use of an analytical method makes its inclusion in ECAD logic synthesis tools possible. This method can be used prior to circuit fabrication and any reliability issues can be discussed in advance and rectified at an early stage of implementation. The core idea of this method is to divide the evaluation process into two levels of characterisations: a stochastic library-specific characterisation of the interference and design-specific characterisation. The former characterisation is fixed and can be applied to different designs which is moved into the platform development stage. Design-specific characterisation represents the parameters of electrical effects registered at the output of the design under test. It is specific to the design and can be obtained by design companies using a number of simulation runs to derive the reliability of their designs.

In this work, the characterisation of interference is represented by the PDF of neutron energy and a fault model which is fixed and used with all combinational circuits. Design-specific characterisation employs the critical values of the SETs that have arrived at the primary output of the CUT which

are related to the circuit whose reliability is being assessed. The transient pulse that results from the interaction between a neutron particle and a transistor in the CUT is modelled using a bias-dependent current source. The most important feature of this model is the dependence of the generated transient pulse on the voltage and bias of the struck node. This model is used with Cadence simulation tool to inject various SETs with different durations according to different values of LETs.

The first set results obtained of the proposed method demonstrate a complex trade-off between the three metrics of reliability, energy consumption and performance. In this work, we evaluate the reliability metric of a circuit at different Vdd values, and then the energy consumption and frequency are determined according to these Vdd values. The energy consumption in digital circuits can be divided into dynamic and leakage energy [115]. The switching activity of a digital circuit during the performance of a computation task is the main reason for the dissipation of dynamic energy. However, the energy that is consumed by a digital circuit when it remains connected to the voltage supply whether or not it is performing useful computation is called leakage energy. In the latest technologies, leakage energy plays a major role in determining energy consumption. Several solutions have been suggested to reduce the energy consumption of digital circuits. One of the most commonly used techniques is dynamic voltage frequency scaling (DVFS), which addresses this problem by scaling down the Vdd applied to the circuit due to the quadratic dependence of dynamic energy consumption on Vdd. However, reducing Vdd causes a reduction in the circuit's frequency, and so it takes longer to perform a given task. Consequently, total energy consumption increases due to the increase in leakage energy. In this work, the total energy consumption (dynamic and static) is calculated according to each value of Vdd applied to the circuit. In general, these results show that, above the nominal voltage of 1-1.2 V, the reliability metric of a circuit has improved slightly at the expense of a considerable increase in the energy consumption. Below the nominal voltage where the circuit optimization is based on power and performance trade-off works, the reliability of the circuit decreases dramatically to reach its lowest value at a certain value of Vdd. This region is also known as the low-energy corner, where both reliability and performance drop rapidly, resulting in a recommendation to avoid this zone. At very low voltages the reliability of the circuit improves again to reach the highest level. This improvement can be explained by the fact that, at these values of Vdd the gates act as filters for

narrow SETs, leading to decreases in the error probability in the circuit. This is a promising result for extremely low-power designs.

The results obtained in this work reveal that different factors impact on the reliability of a circuit. The first factor is the Vdd applied to the circuit, It has been found that, in the case of high Vdd, the reliability of the circuit is high and it decreases when Vdd is scaled down. This is because in our analysis the rate of neutron particles per clock cycle is calculated. So, in the case of operations with short clock periods (high voltages), the circuit receives a lower number of neutron hits than during long clock period operations (low voltages).

The second factor is the structure of combinational circuits, including the number of gates, the length of paths, and the number and type of output gates. Circuits with high numbers of gates are usually less reliable than those with fewer gates. This is because more gates means more sensitive nodes and, as a result, more glitches are generated. Also, with high numbers of gates, there are high numbers of branches. This increases the chance of propagating the generated glitches to several paths, which leads to an increasing probability of errors. Circuits with long paths are more reliable than those with short paths, especially at low voltages. This can be attributed to the electrical masking effect which increases in long paths. Increasing the number of the outputs of a circuit has a negative impact on its reliability. This is because large numbers of output gates in a circuit lead to an increasing probability of propagating the generated SETs to the output flip-flops. As a result of this, the probability of error increases. The type of output gate has an impact on the reliability of a circuit. We found that, when implementing a circuit with large gates such as XOR and XNOR gates at the output terminal blocks, most of the propagated SETs are masked, which increases the reliability of the circuit.

The third factor is the combinational input, which has a direct relationship with the vulnerability and the logical masking effect of gates. In this study we took into account the SETs generated on NMOS transistors only. So, specific input values make a gate vulnerable; for example, the NOT gate does not generate an SET if its input is at logic 1. The logical masking effect depends on the type of gate, so it may occur in some gates and not in others. Even in those gates that may be affected by the logical masking effect, this depends on the input values. In this work, we applied different combinational inputs to the circuits under test, and these inputs were randomly chosen. The differences between the results obtained are obvious; however, in our case the average

of the levels of reliability obtained are calculated and used to represent the reliability of the circuit.

Designing ultra-low power circuits can have a positive impact on the reliability of these circuits with further impacts on energy consumption. In this type of circuit, the operating clock increases with decreasing supply voltage at a rate higher than the increase in SET duration [17]. Consequently, more SETs are attenuated, which improves reliability. Therefore, ultra-low power circuits may be an attractive solution for reducing energy consumption and increasing reliability.

The reliability metric improved dramatically at the expense of a minor increase in energy consumption and a decrease in performance. This reliability improvement is obtained by adding slow stages at the output terminals to filter the propagated glitches. Two types of filter stage are suggested in this work: active filter and passive filter stages. The active filter stage is implemented using a logic gate and is more effective in long paths rather than short paths, due to the accumulation effect of the energy consumption and the propagation delay. The passive filter stage is implemented by using a resistor and capacitor and can be used with both long- and short-path circuits.

The problem of time-consuming simulations that are needed to evaluate the reliability of large circuits has been solved by using a simplification technique. The results that are obtained by using this technique are evaluated and compared with the exact results. The comparison showed a high accuracy of the approximate reliability obtained using the simplification technique and a dramatic reduction in the simulation time. This technique is based on the equivalence of the function of gates within the path, and equivalence between paths. So, in order to estimate a circuit's reliability it is sufficient to simulate a segment of the CUT that contains several gates which are equivalent to all vulnerable gates in the circuit. An algorithm is implemented for application to large circuits in order to choose these gates based on their location and the structure of the circuit.

7.2   CRITICAL REVIEW AND FUTURE WORK

The objectives of this research include opening a new horizon in low-energy and high reliable design. Therefore, many research directions can be indicated from this work to analyse and study reliability of combinational circuits. The

limitations of this work and directions for future research are discussed as follows:

•*Time-consuming analogue simulation:* a limitation of the proposed technique is that it depends on the complexity of the CUT. In the case of large circuits, a large number of simulations runs is required in order to estimate reliability. This limitation is solved by proposing a simplification technique which leads to dramatic reductions in estimation time at the expense of accuracy. This limitation can also be solved by proposing a technique which can work on two levels of abstraction, where the circuit level is used in generating an SET due to a particle hit, and the gate level is used to propagate that SET and to observe its duration at the output terminals.

•*Impact of variabilities occurring in the field:* the continuous scaling of complementary metal oxide semiconductor (CMOS) technology increases the vulnerability of digital circuits to ageing mechanisms. An ageing mechanism such as negative-bias temperature-instability (NBTI) has a negative impact on the susceptibility of these circuits to soft errors. This can be attributed to the fact that NBTI increases the absolute threshold voltage of PMOS transistors by more than 50 mV in ten years [114]. Also, it reduces the critical charge of a node by reducing the restoring current of the pull-up network [113]. In this work, we derive the reliability metric in terms of generating an SET without taking ageing mechanisms into account. More research can be launched to analyse and derive the reliability metric of a circuit by combining the effect of neutron particles with one or more ageing mechanism. This can be done using the proposed method if a stochastic characterisation of the mechanism under study is provided.

•*Subthreshold logic:* circuits need to be carefully designed in order to operate in subthreshold logic. In such a region of operation, the integrity of digital signals degrades dramatically because of the indifference between active and leakage currents. Also, variations in the process and supply voltage become more significant and impact on the performance of the circuit. According to our findings, the reliability of a combinational circuit improves dramatically in this operating region; however, designing such a circuit to operate in this region is still a challenging topic.

The three-way trade-off explore extends the traditional concept of dynamic voltage-frequency scaling (DVFS) by adding the reliability metric. This will help in the selection of the operating point for circuits regarding their reliability. It can also facilitate the emergence of a new generation of power management

designs which controls the reliability dynamically, power or energy reliability management; PRM or ERM.

The reliability metric is derived without extremely expensive Monte Carlo simulations or physical experiments, which makes its inclusion into ECAD logic synthesis tools possible. This method may become an enabler in achieving the reliability closure for a system at an early design stage, similar to how the timing closure is addressed.

Part II

Thesis Appendices

RELIABILITY AND PROBABILITY OF ERRORS DATA

Table A.1: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of the chain of inverters circuit.

Vdd (V)	Frequency (MHz)	Energy (J)	Error probability	Reliability
2.0	436.87	2.55E-12	1.63E-10	1-(1.63E-10)
1.8	413.56	2.00E-12	1.70E-10	1-(1.70E-10)
1.6	384.32	1.55E-12	1.78E-10	1-(1.78E-10)
1.4	347.95	1.16E-12	1.88E-10	1-(1.88E-10)
1.2	302.39	8.40E-13	2.01E-10	1-(2.01E-10)
1.0	246.43	5.72E-13	2.20E-10	1-(2.20E-10)
0.8	178.79	3.62E-13	2.47E-10	1-(2.47E-10)
0.6	101.20	2.01E-13	2.99E-10	1-(2.99E-10)
0.4	26.06	9.11E-14	1.69E-10	1-(1.69E-10)
0.35	13.95	7.25E-14	1.12E-10	1-(1.12E-10)
0.3	6.21	5.97E-14	2.28E-11	1-(2.28E-11)
0.2	0.82	6.90E-14	4.55E-11	1-(4.55E-11)

Table A.2: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of the non-uniform path circuit.

Vdd (V)	Frequency (MHz)	Energy (J)	Error probability	Reliability
2.0	397.30	2.20E-12	9.80E-11	1-(9.80E-11)
1.8	380.66	1.74E-12	1.03E-10	1-(1.03E-10)
1.6	359.20	1.35E-12	1.08E-10	1-(1.08E-10)
1.4	331.02	1.01E-12	1.14E-10	1-(1.14E-10)
1.2	294.38	7.23E-13	1.22E-10	1-(1.22E-10)
1.0	246.43	4.92E-13	1.33E-10	1-(1.33E-10)
0.8	185.08	3.10E-13	1.49E-10	1-(1.49E-10)
0.6	108.79	1.73E-13	1.77E-10	1-(1.77E-10)
0.4	30.32	7.80E-14	2.32E-10	1-(2.32E-10)
0.35	16.42	6.20E-14	1.13E-10	1-(1.13E-10)
0.3	7.24	5.00E-14	1.51E-11	1-(1.51E-11)
0.2	1.00	5.30E-14	1.33E-11	1-(1.33E-11)

Table A.3: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of the 3-bit adder circuit.

Vdd (V)	Frequency (GHz)	Energy (J)	Error probability	Reliability
2.0	1.52	7.58E-13	2.46E-11	1-(2.46E-11)
1.8	1.49	5.95E-13	2.56E-11	1-(2.56E-11)
1.6	1.47	4.54E-13	2.69E-11	1-(2.69E-11)
1.4	1.43	3.36E-13	2.85E-11	1-(2.85E-11)
1.2	1.37	2.38E-13	3.07E-11	1-(3.07E-11)
1.0	1.28	1.60E-13	3.36E-11	1-(3.36E-11)
0.8	1.11	9.91E-14	3.84E-11	1-(3.84E-11)
0.6	0.83	5.47E-14	4.81E-11	1-(4.81E-11)
0.4	0.36	2.26E-14	8.83E-11	1-(8.83E-11)
0.35	0.22	1.55E-14	9.15E-11	1-(9.15E-11)
0.3	0.18	7.50E-15	6.94E-11	1-(6.94E-11)
0.2	0.12	1.41E-15	7.30E-12	1-(7.30E-12)

Table A.4: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of c432 circuit.

Vdd (V)	Frequency (GHz)	Energy (J)	Error probability	Reliability
2.0	815.66	1.04E-11	1.26E-10	1-(1.26E-10)
1.8	794.28	6.85E-12	1.32E-10	1-(1.32E-10)
1.6	765.7	4.97E-12	1.39E-10	1-(1.39E-10)
1.4	729.93	3.48E-12	1.49E-10	1-(1.49E-10)
1.2	675.22	2.29E-12	1.62E-10	1-(1.62E-10)
1.0	601.32	1.42E-12	1.84E-10	1-(1.84E-10)
0.8	484.26	8.32E-13	2.29E-10	1-(2.29E-10)
0.6	301.11	4.44E-13	2.95E-10	1-(2.95E-10)
0.4	94.73	1.81E-13	3.62E-10	1-(3.62E-10)
0.35	51.81	1.37E-13	3.99E-10	1-(3.99E-10)
0.3	23.34	1.04E-13	3.77E-10	1-(3.77E-10)
0.2	3.14	7.20E-14	2.10E-10	1-(2.10E-10)

Table A.5: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of c499 circuit.

Vdd (V)	Frequency (GHz)	Energy (J)	Error probability	Reliability
2.0	1070.32	6.19E-12	1.10E-10	1-(1.10E-10)
1.8	1056.41	4.81E-12	1.15E-10	1-(1.15E-10)
1.6	1035.95	3.64E-12	1.20E-10	1-(1.20E-10)
1.4	993.05	2.67E-12	1.27E-10	1-(1.27E-10)
1.2	932.84	1.88E-12	1.38E-10	1-(1.38E-10)
1.0	811.69	1.25E-12	1.50E-10	1-(1.50E-10)
0.8	647.25	7.70E-13	1.71E-10	1-(1.71E-10)
0.6	412.54	4.30E-13	2.03E-10	1-(2.03E-10)
0.4	127.68	1.90E-13	2.60E-10	1-(2.60E-10)
0.35	69.88	1.50E-13	2.71E-10	1-(2.71E-10)
0.3	31.64	1.10E-13	1.99E-10	1-(1.99E-10)
0.2	4.35	1.90E-13	3.68E-12	1-(3.68E-12)

Table A.6: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of c1908 circuit.

Vdd (V)	Frequency (GHz)	Energy (J)	Error probability	Reliability
2.0	764.53	2.15E-11	4.40E-10	1-(4.40E-10)
1.8	741.84	1.69E-11	4.63E-10	1-(4.63E-10)
1.6	712.25	1.30E-11	4.88E-10	1-(4.88E-10)
1.4	672.95	9.65E-12	5.15E-10	1-(5.15E-10)
1.2	618.81	6.89E-12	5.54E-10	1-(5.54E-10)
1.0	541.71	4.67E-12	6.16E-10	1-(6.16E-10)
0.8	428.45	2.92E-12	7.12E-10	1-(7.12E-10)
0.6	268.46	1.60E-12	9.04E-10	1-(9.04E-10)
0.4	85.54	6.26E-13	1.20E-09	1-(1.20E-09)
0.35	47.24	4.71E-13	5.64E-10	1-(5.64E-10)
0.3	20.65	3.62E-13	4.17E-10	1-(4.17E-10)
0.2	2.72	3.39E-13	9.55E-10	1-(9.55E-10)

Table A.7: Error probability and reliability data corresponding with the value of the supply voltage, energy consumption and frequency of c6288 circuit.

Vdd (V)	Frequency (GHz)	Energy (J)	Error probability	Reliability
2.0	370.37	2.07E-10	2.85E-09	1-(2.85E-9)
1.8	357.14	1.62E-10	3.02E-09	1-(3.05E-9)
1.6	334.45	1.25E-10	3.33E-09	1-(3.35E-9)
1.4	308.64	9.27E-11	3.58E-09	1-(3.55E-9)
1.2	277.01	6.54E-11	3.99E-09	1-(3.95E-9)
1.0	238.1	4.39E-11	4.79E-09	1-(4.75E-9)
0.8	177.62	2.85E-11	6.34E-09	1-(6.35E-9)
0.6	103.84	1.58E-11	1.04E-08	1-(1.04E-8)
0.4	28.46	6.91E-12	3.45E-09	1-(3.45E-9)
0.35	15.3	5.34E-12	1.68E-09	1-(1.65E-9)
0.3	6.84	4.07E-12	1.09E-09	1-(1.09E-9)
0.2	0.92	2.64E-12	1.04E-09	1-(1.04E-9)

Table A.8: Data of Figure 5.3, shows the relation between reliability, energy consumption and performance for the circuit chain of inverters in the cases: without filter, with 16x, 32x, 32x+0.5x filters.

Vdd (V)	Without filter			16x filter			32x filter			32x+0.5x filter		
	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.
2.0	438.60	2.53E-12	1-(1.64E-10)	429.18	2.96E-12	1-(1.56E-10)	423.53	3.43E-12	1-(1.42E-10)	407.66	4.24E-12	1-(7.89E-11)
1.8	414.94	2.01E-12	1-(1.68E-10)	406.50	2.33E-12	1-(1.61E-10)	401.61	2.72E-12	1-(1.47E-10)	386.10	3.25E-12	1-(8.11E-11)
1.6	386.10	1.55E-12	1-(1.75E-10)	378.79	1.78E-12	1-(1.66E-10)	374.13	2.06E-12	1-(1.53E-10)	359.71	2.40E-12	1-(8.07E-11)
1.4	348.43	1.17E-12	1-(1.87E-10)	342.47	1.32E-12	1-(1.75E-10)	337.84	1.52E-12	1-(1.63E-10)	325.23	1.73E-12	1-(8.02E-11)
1.2	303.03	8.40E-13	1-(2.01E-10)	298.51	9.29E-13	1-(1.86E-10)	294.12	1.05E-12	1-(1.72E-10)	283.29	1.18E-12	1-(7.06E-11)
1.0	246.31	5.73E-13	1-(2.16E-10)	243.31	6.23E-13	1-(2.02E-10)	239.88	6.76E-13	1-(1.81E-10)	231.48	7.45E-13	1-(5.43E-11)
0.8	178.89	3.61E-13	1-(2.46E-10)	177.08	3.86E-13	1-(2.23E-10)	174.53	4.09E-13	1-(1.90E-10)	169.09	4.24E-13	1-(1.34E-11)
0.6	101.11	2.00E-13	1-(2.95E-10)	100.40	2.10E-13	1-(2.59E-10)	98.91	2.22E-13	1-(1.76E-10)	95.97	2.27E-13	1-(1.04E-12)
0.4	26.56	9.14E-14	1-(4.46E-10)	26.38	9.56E-14	1-(1.10E-10)	26.03	9.96E-14	1-(1.31E-12)	25.42	1.01E-13	1-(1.60E-12)
0.35	14.08	7.27E-14	1-(5.58E-10)	13.98	7.62E-14	1-(4.98E-11)	13.83	7.96E-14	1-(1.83E-12)	13.53	8.05E-14	1-(1.95E-12)
0.3	6.22	5.98E-14	1-(3.06E-11)	6.17	6.23E-14	1-(3.09E-12)	6.11	6.49E-14	1-(2.53E-12)	6.01	6.55E-14	1-(2.39E-12)
0.2	0.81	6.91E-14	1-(1.09E-11)	0.81	7.20E-14	1-(4.42E-12)	0.80	7.49E-14	1-(3.86E-12)	0.79	7.56E-14	1-(3.82E-12)

• Freq.=Frequency, Rel.=Reliability, En.=Energy

Table A.9: Data of Figure 5.10, shows the relation between reliability, energy consumption and performance for the circuit c432 in the cases: without filter, with R=10 kΩ and C=30 fF, R=10 kΩ and C=40 fF, R=10 kΩ and C=50 fF filters.

Vdd (V)	Without filter			(R=10 kΩ, C=30 fF) filter			(R=10 kΩ, C=40 fF) filter			(R=10 kΩ, C=50 fF) filter		
	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.
2.0	815.66	7.52E-12	1-(1.95E-10)	700.77	7.94E-12	1-(9.31E-11)	667.56	8.04E-12	1-(1.40E-11)	636.13	8.13E-12	1-(5.52E-12)
1.8	794.28	5.75E-12	1-(2.04E-10)	681.20	6.10E-12	1-(1.07E-10)	650.20	6.18E-12	1-(1.88E-11)	619.58	6.25E-12	1-(6.72E-12)
1.6	765.70	4.26E-12	1-(2.16E-10)	661.38	4.54E-12	1-(1.23E-10)	632.11	4.60E-12	1-(2.63E-11)	602.77	4.66E-12	1-(8.33E-12)
1.4	729.93	3.04E-12	1-(2.31E-10)	633.71	3.26E-12	1-(1.42E-10)	605.69	3.31E-12	1-(3.72E-11)	580.38	3.35E-12	1-(1.09E-11)
1.2	675.22	2.07E-12	1-(2.54E-10)	594.18	2.24E-12	1-(1.72E-10)	569.80	2.27E-12	1-(5.36E-11)	546.75	2.31E-12	1-(1.44E-11)
1.0	601.32	1.33E-12	1-(2.88E-10)	534.47	1.45E-12	1-(2.29E-10)	514.14	1.48E-12	1-(8.56E-11)	495.05	1.51E-12	1-(2.13E-11)
0.8	484.26	7.99E-13	1-(3.57E-10)	439.56	8.83E-13	1-(2.58E-10)	425.35	9.03E-13	1-(1.28E-10)	411.86	9.21E-13	1-(3.60E-11)
0.6	301.11	4.33E-13	1-(4.46E-10)	288.93	4.86E-13	1-(2.94E-10)	282.01	5.00E-13	1-(1.69E-10)	275.79	5.12E-13	1-(6.53E-11)
0.4	94.73	1.89E-13	1-(4.96E-10)	93.37	2.16E-13	1-(1.38E-10)	91.74	2.24E-13	1-(5.20E-11)	89.85	2.31E-13	1-(2.39E-11)
0.35	51.81	1.46E-13	1-(5.37E-10)	51.28	1.66E-13	1-(1.14E-10)	50.51	1.72E-13	1-(5.21E-11)	49.55	1.79E-13	1-(2.30E-11)
0.3	23.34	1.11E-13	1-(5.67E-10)	23.15	1.25E-13	1-(6.03E-11)	22.84	1.30E-13	1-(3.50E-11)	22.53	1.34E-13	1-(5.30E-14)
0.2	3.14	7.50E-14	1-(3.12E-10)	3.11	8.20E-14	1-(1.97E-10)	3.07	8.40E-14	1-(2.00E-10)	3.04	8.60E-14	1-(2.30E-14)

- Freq.=Frequency, Rel.=Reliability, En.=Energy

Table A.10: Data of Figure 5.14, shows the relation between reliability, energy consumption and performance for the circuit c1908 in the cases: without filter, with R=10 kΩ and C=30 fF, R=10 kΩ and C=40 fF, R=10 kΩ and C=50 fF filters.

Vdd (V)	Without filter			(R=10 kΩ, C=30 fF) filter			(R=10 kΩ, C=40 fF) filter			(R=10 kΩ, C=50 fF) filter		
	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.	Freq. (MHz)	En. (J)	Rel.
2.0	854.70	1.19E-11	1-(7.03E-10)	721.50	1.27E-11	1-(1.61E-10)	683.53	1.29E-11	1-(1.02E-11)	650.62	1.31E-11	1-(9.06E-14)
1.8	833.33	9.32E-12	1-(7.34E-10)	705.22	9.97E-12	1-(2.01E-10)	669.79	1.02E-11	1-(2.14E-11)	638.16	1.04E-11	1-(2.26E-13)
1.6	806.45	7.14E-12	1-(7.74E-10)	684.93	7.65E-12	1-(2.45E-10)	650.62	7.81E-12	1-(4.50E-11)	619.96	7.96E-12	1-(4.69E-13)
1.4	769.23	5.29E-12	1-(8.24E-10)	655.31	5.69E-12	1-(2.97E-10)	625.00	5.80E-12	1-(7.64E-11)	596.66	5.92E-12	1-(9.81E-13)
1.2	714.29	3.76E-12	1-(8.87E-10)	614.25	4.05E-12	1-(3.60E-10)	586.85	4.14E-12	1-(1.23E-10)	561.48	4.22E-12	1-(1.75E-12)
1.0	632.91	2.52E-12	1-(9.84E-10)	553.10	2.73E-12	1-(4.44E-10)	530.50	2.79E-12	1-(2.05E-10)	509.16	2.85E-12	1-(2.96E-12)
0.8	510.20	1.57E-12	1-(1.13E-09)	454.34	1.71E-12	1-(5.65E-10)	438.79	1.75E-12	1-(3.19E-10)	424.45	1.78E-12	1-(4.75E-12)
0.6	327.87	8.55E-13	1-(1.44E-09)	299.94	9.41E-13	1-(7.51E-10)	292.40	9.64E-13	1-(4.66E-10)	283.93	9.86E-13	1-(8.13E-12)
0.4	103.20	3.69E-13	1-(1.97E-09)	97.18	4.13E-13	1-(2.72E-10)	95.51	4.25E-13	1-(8.83E-11)	93.63	4.36E-13	1-(6.17E-12)
0.35	57.05	2.83E-13	1-(6.67E-10)	54.02	3.17E-13	1-(1.35E-10)	53.16	3.26E-13	1-(9.58E-11)	52.25	3.35E-13	1-(3.37E-12)
0.3	25.95	2.14E-13	1-(5.10E-10)	24.69	2.38E-13	1-(1.64E-10)	24.32	2.45E-13	1-(1.45E-10)	23.98	2.52E-13	1-(1.11E-17)
0.2	3.49	1.69E-13	1-(1.13E-09)	3.32	1.83E-13	1-(7.92E-10)	3.28	1.87E-13	1-(8.08E-10)	3.20	1.90E-13	1-(1.11E-17)

• Freq.=Frequency, Rel.=Reliability, En.=Energy

DERIVING THE RELIABILITY CODES

B.1 FINDING CVM VALUES OF A CIRCUIT, OCEAN SCRIPT.

```
simulator( 'spectre )

option( ?categ 'turboOpts 'uniMode "APS" )

for( i 0 2671
        sprintf(i_str "%d" i)
        netlist_name = strcat("netlist_", i_str)
        design(  buildString(list("/scratch/tmp_simulations/c6288/c1/spectre/
            schematic/", netlist_name, "/netlist"), ""))
        resultsDir( buildString(list("/scratch/tmp_simulations/c6288/c1/spectre
            /schematic/", netlist_name), "") )

modelFile(
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
        DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_25IO_NVT
        _V021.lib.scs" "tt")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
        DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_25IO_V
        111.lib.scs" "tt")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
        DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_NCAP25_V
        113.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
        DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_varmis
        _25_rf_V011.lib.scs" "typ")
```

```
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_33IO_GOX
    52_VT21.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_25IO_RF_
    V021.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90-resistor
    -control-V041.scs" "")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_BJT_V
    111.lib.scs" "tt_bip")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_DIODE_V
    101.mdl.scs" "")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_LL12_RF_
    V021.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_LLLVT12_
    RF_VTAB.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_LL12_V
    102.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_LLHVT12_
    V101.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
    DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_LLLVT12_
    V102.lib.scs" "tt")
```

```
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_LLNVT12_
    V011.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90SP_NCAP
    10_V112.lib.scs" "typ")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_NCAP12_
    LL_V102.lib.scs" "typ")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_SP10_V
    061.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_SPHVT10_
    V111.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_SPLVT10_
    V102.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_SPNVT10_
    V011.lib.scs" "tt")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_mimcaps
    _20f_kf_V011.lib.scs" "typ")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_momcaps_
    V041.lib.scs" "typ")
'("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
    N-1P9M-LOW_K_UMK90FDKLMC00000OA-FDK-Ver.A01_PB/UMK90FDKLMC00000OA_A01_
    DESIGNKIT/UMK90FDKLMC00000OA_A01/umc90nm/../Models/Spectre/L90_vardiop_
    rf_v011.lib.scs" "typ")
```

```
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_varmis
        _12_llrf_V021.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/momcaps_
        array_vp3_rfvcl_V011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/momcaps_
        array_vp4_rfvcl_V011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/rnhr_rf_V
        011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/rnnpo_rf_V
        011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/rnppo_rf_V
        011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_varmis
        _10_sprf_V011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/bond_pad_v
        011.lib.scs" "typ")
    '("/home/dk/UMC/90nm/1.4_P2/Designkits/Cadence_6.1/G-9FD-LOGIC_MIXED_MODE90
        N-1P9M-LOW_K_UMK90FDKLMC000000A-FDK-Ver.A01_PB/UMK90FDKLMC000000A_A01_
        DESIGNKIT/UMK90FDKLMC000000A_A01/umc90nm/../Models/Spectre/L90_SP10_RF_
        V021.lib.scs" "tt")
    '("/home/CAMPUS/b5000001/tutorial/csou.lib.scs" "")
)
stimulusFile( ?xlate nil
```

```
        "/scratch/tmp_simulations/c6288/c1/spectre/schematic/netlist/_graphical_
            stimuli.scs")


out = outfile("results/CVM.txt" "a")

myvdd=list( 2 1.8 1.6 1.4 1.2 1 0.8 0.6 0.4 0.35 0.3 0.2 )

prog(() foreach((vvdd) myvdd


        desVar("vdd" vvdd)


        vd=vvdd*0.5



        LoadList1 = list( 100 75 50 25 5 2 1 )


                foreach((let) LoadList1

                desVar( "a" let )




                analysis('tran  ?start "80n" ?stop "150n"  )

                envOption('analysisOrder  list("tran") )



                temp( 27 )

run()
selectResult( 'tran )
;plot(getData("/out545") getData("/out1581") getData("/out1901") getData("/out
    2223") getData("/out2548") getData("/out2877") getData("/out3211") getData
    ("/out3552") getData("/out3895") getData("/out4241") getData("/out4591")
    getData("/out4946") getData("/out5308") getData("/out5672") getData("/out
    5971") getData("/out6123") getData("/out6150") getData("/out6160") getData
    ("/out6170") getData("/out6180") getData("/out6190") getData("/out6200")
    getData("/out6210") getData("/out6220") getData("/out6230") getData("/out
```

```
    6240") getData("/out6250") getData("/out6260") getData("/out6270") getData
    ("/out6280") getData("/out6287") getData("/out6288") )


tr2=cross(v("/out545" ?result "tran") vd 1 "falling" nil nil  )
tr1=cross(v("/out545" ?result "tran") vd 1 "rising" nil nil  )


if((tr1==nil) then tr1=0)
if((tr2==nil) then tr2=0)


tr3=cross(v("/out1581" ?result "tran") vd 1 "rising" nil nil  )
tr4=cross(v("/out1581" ?result "tran") vd 1 "falling" nil nil  )


if((tr3==nil) then tr3=0)
if((tr4==nil) then tr4=0)


tr5=cross(v("/out1901" ?result "tran") vd 1 "rising" nil nil  )
tr6=cross(v("/out1901" ?result "tran") vd 1 "falling" nil nil  )


if((tr5==nil) then tr5=0)
if((tr6==nil) then tr6=0)


tr7=cross(v("/out2223" ?result "tran") vd 1 "falling" nil nil  )
tr8=cross(v("/out2223" ?result "tran") vd 1 "rising" nil nil  )


if((tr7==nil) then tr7=0)
if((tr8==nil) then tr8=0)


tr9=cross(v("/out2548" ?result "tran") vd 1 "falling" nil nil  )
tr10=cross(v("/out2548" ?result "tran") vd 1 "rising" nil nil  )


if((tr9==nil) then tr9=0)
if((tr10==nil) then tr10=0)


tr11=cross(v("/out2877" ?result "tran") vd 1 "falling" nil nil  )
tr12=cross(v("/out2877" ?result "tran") vd 1 "rising" nil nil  )


if((tr11==nil) then tr11=0)
if((tr12==nil) then tr12=0)


tr13=cross(v("/out3211" ?result "tran") vd 1 "falling" nil nil  )
```

```
tr14=cross(v("/out3211" ?result "tran") vd 1 "rising" nil nil  )


if((tr13==nil) then tr13=0)
if((tr14==nil) then tr14=0)


tr15=cross(v("/out3552" ?result "tran") vd 1 "falling" nil nil  )
tr16=cross(v("/out3552" ?result "tran") vd 1 "rising" nil nil  )


if((tr15==nil) then tr15=0)
if((tr16==nil) then tr16=0)


tr17=cross(v("/out3895" ?result "tran") vd 1 "falling" nil nil  )
tr18=cross(v("/out3895" ?result "tran") vd 1 "rising" nil nil  )


if((tr17==nil) then tr17=0)
if((tr18==nil) then tr18=0)


tr19=cross(v("/out4241" ?result "tran") vd 1 "falling" nil nil  )
tr20=cross(v("/out4241" ?result "tran") vd 1 "rising" nil nil  )


if((tr19==nil) then tr19=0)
if((tr20==nil) then tr20=0)


tr21=cross(v("/out4591" ?result "tran") vd 1 "falling" nil nil  )
tr22=cross(v("/out4591" ?result "tran") vd 1 "rising" nil nil  )


if((tr21==nil) then tr21=0)
if((tr22==nil) then tr22=0)


tr23=cross(v("/out4946" ?result "tran") vd 1 "falling" nil nil  )
tr24=cross(v("/out4946" ?result "tran") vd 1 "rising" nil nil  )


if((tr23==nil) then tr23=0)
if((tr24==nil) then tr24=0)


tr25=cross(v("/out5308" ?result "tran") vd 1 "falling" nil nil  )
tr26=cross(v("/out5308" ?result "tran") vd 1 "rising" nil nil  )


if((tr25==nil) then tr25=0)
if((tr26==nil) then tr26=0)
```

```
tr27=cross(v("/out5672" ?result "tran") vd 1 "falling" nil nil  )
tr28=cross(v("/out5672" ?result "tran") vd 1 "rising" nil nil  )

if((tr27==nil) then tr27=0)
if((tr28==nil) then tr28=0)

tr29=cross(v("/out5971" ?result "tran") vd 1 "falling" nil nil  )
tr30=cross(v("/out5971" ?result "tran") vd 1 "rising" nil nil  )

if((tr29==nil) then tr29=0)
if((tr30==nil) then tr30=0)

tr31=cross(v("/out6123" ?result "tran") vd 1 "falling" nil nil  )
tr32=cross(v("/out6123" ?result "tran") vd 1 "rising" nil nil  )
if((tr31==nil) then tr31=0)
if((tr32==nil) then tr32=0)

tr33=cross(v("/out6150" ?result "tran") vd 1 "falling" nil nil  )
tr34=cross(v("/out6150" ?result "tran") vd 1 "rising" nil nil  )

if((tr33==nil) then tr33=0)
if((tr34==nil) then tr34=0)

tr35=cross(v("/out6160" ?result "tran") vd 1 "falling" nil nil  )
tr36=cross(v("/out6160" ?result "tran") vd 1 "rising" nil nil  )

if((tr35==nil) then tr35=0)
if((tr36==nil) then tr36=0)

tr37=cross(v("/out6170" ?result "tran") vd 1 "falling" nil nil  )
tr38=cross(v("/out6170" ?result "tran") vd 1 "rising" nil nil  )

if((tr37==nil) then tr37=0)
if((tr38==nil) then tr38=0)

tr39=cross(v("/out6180" ?result "tran") vd 1 "falling" nil nil  )
tr40=cross(v("/out6180" ?result "tran") vd 1 "rising" nil nil  )

if((tr39==nil) then tr39=0)
```

```
if((tr40==nil) then tr40=0)


tr41=cross(v("/out6190" ?result "tran") vd 1 "falling" nil nil  )
tr42=cross(v("/out6190" ?result "tran") vd 1 "rising" nil nil  )


if((tr41==nil) then tr41=0)
if((tr42==nil) then tr42=0)


tr43=cross(v("/out6200" ?result "tran") vd 1 "falling" nil nil  )
tr44=cross(v("/out6200" ?result "tran") vd 1 "rising" nil nil  )


if((tr43==nil) then tr43=0)
if((tr44==nil) then tr44=0)


tr45=cross(v("/out6210" ?result "tran") vd 1 "falling" nil nil  )
tr46=cross(v("/out6210" ?result "tran") vd 1 "rising" nil nil  )


if((tr45==nil) then tr45=0)
if((tr46==nil) then tr46=0)


tr47=cross(v("/out6220" ?result "tran") vd 1 "falling" nil nil  )
tr48=cross(v("/out6220" ?result "tran") vd 1 "rising" nil nil  )


if((tr47==nil) then tr47=0)
if((tr48==nil) then tr48=0)


tr49=cross(v("/out6230" ?result "tran") vd 1 "falling" nil nil  )
tr50=cross(v("/out6230" ?result "tran") vd 1 "rising" nil nil  )


if((tr49==nil) then tr49=0)
if((tr50==nil) then tr50=0)


tr51=cross(v("/out6240" ?result "tran") vd 1 "falling" nil nil  )
tr52=cross(v("/out6240" ?result "tran") vd 1 "rising" nil nil  )


if((tr51==nil) then tr51=0)
if((tr52==nil) then tr52=0)


tr53=cross(v("/out6250" ?result "tran") vd 1 "falling" nil nil  )
tr54=cross(v("/out6250" ?result "tran") vd 1 "rising" nil nil  )
```

```
if((tr53==nil) then tr53=0)
if((tr54==nil) then tr54=0)


tr55=cross(v("/out6260" ?result "tran") vd 1 "falling" nil nil  )
tr56=cross(v("/out6260" ?result "tran") vd 1 "rising" nil nil  )


if((tr55==nil) then tr55=0)
if((tr56==nil) then tr56=0)


tr57=cross(v("/out6270" ?result "tran") vd 1 "falling" nil nil  )
tr58=cross(v("/out6270" ?result "tran") vd 1 "rising" nil nil  )


if((tr57==nil) then tr57=0)
if((tr58==nil) then tr58=0)


tr59=cross(v("/out6280" ?result "tran") vd 1 "falling" nil nil  )
tr60=cross(v("/out6280" ?result "tran") vd 1 "rising" nil nil  )


if((tr59==nil) then tr59=0)
if((tr60==nil) then tr60=0)


tr61=cross(v("/out6287" ?result "tran") vd 1 "falling" nil nil  )
tr62=cross(v("/out6287" ?result "tran") vd 1 "rising" nil nil  )


if((tr61==nil) then tr61=0)
if((tr62==nil) then tr62=0)


tr63=cross(v("/out6288" ?result "tran") vd 1 "falling" nil nil  )
tr64=cross(v("/out6288" ?result "tran") vd 1 "rising" nil nil  )


if((tr63==nil) then tr63=0)
if((tr64==nil) then tr64=0)

if(((vvdd==2) && (let==100) && (tr1==0) && (tr3==0) && (tr5==0) && (tr7==0) &&
    (tr9==0) && (tr11==0) && (tr13==0) && (tr15==0) && (tr17==0) && (tr19==0)
    && (tr21==0) && (tr23==0) && (tr25==0) && (tr27==0) && (tr29==0) && (tr
    31==0) && (tr33==0) && (tr35==0) && (tr37==0) && (tr39==0) && (tr41==0) &&
    (tr43==0) && (tr45==0) && (tr47==0) && (tr49==0) && (tr51==0) && (tr53==0)
```

```
   && (tr55==0) && (tr57==0) && (tr59==0) && (tr61==0) && (tr63==0)) then
      return())


ocnPrint(?output out  let,tr1,tr2,tr3,tr4,tr5,tr6,tr7,tr8,tr9,tr10,tr11,tr12,tr
   13,tr14,tr15,tr16,tr17,tr18,tr19,tr20,tr21,tr22,tr23,tr24,tr25,tr26,tr27,tr
   28,tr29,tr30,tr31,tr32,tr33,tr34,tr35,tr36,tr37,tr38,tr39,tr40,tr41,tr42,tr
   43,tr44,tr45,tr46,tr47,tr48,tr49,tr50,tr51,tr52,tr53,tr54,tr55,tr56,tr57,tr
   58,tr59,tr60,tr61,tr62,tr63,tr64 )
)
)
)
)
```

B.2   CALCULATING THE ERROR PROBABILITY OF A CIRCUIT, C-LANGUAGE CODE.

```c
#include <stdio.h>
#include <stdlib.h>
#include <math.h>


//this function calculates the probability of LET
double errb(int i);


int main()
{


// This part reading the LET value and the intersection between the output
    waveform and Vdd/2
// (the parameter vectors )PV, where i is number of simulations according to
    different value of LET and n number of the outputs
// that the glitch is propagated to.
// var1 is LET value, var the starting and finishing the glitch (the glitch
    period)



FILE *fp1;
FILE *fp2;
FILE *fp3;
fp1 = fopen("c1908/RCfilter/r10c50.txt", "r");
fp2 = fopen("c1908/RCfilter/errorfile-r10c50.txt","a");
fp3 = fopen("c1908/clock.txt", "r");

double err;
float rate,prob,nr=20;
float mins[7], maxs[7],minb[7], maxb[7],t[7][7],var1[7],let1[7],probability
    [12],minimum,minimumb;
float trs[7],trb[7],tr[7],v[12],T[12];
int i,ii,iii,nn,n,k,kk,m,jj,j=0,out=50,let[7];
float lit[out],vars[7][out],varb[7][out],var[7][out];
    //j is number of let values that used in the simulation stage. out: is
        number of glitches critical values
for(j=0;j<12;j++){
  probability[j]=0;
}
```

```c
for (kk=0; kk<350 ;kk++)
{
  for (k=0; k<12 ;k++)
  {
    fscanf(fp3," %f %f",&v[k],&T[k]);
    prob=0;
    err=0;
    maxs[0]=0;
    for (i = 0 ; i < 7 ; i++)
    {
      minimum=350;
      minimumb=350;
      fscanf(fp1, "%f ",&var1[i]);
      for(n=0 ; n<out ; n+=2)
      {
        lit[n]=0;
        fscanf(fp1, "%f  %f ",&var[i][n],&var[i][n+1]);
        if ((var[i][n] != 0) && (var[i][n+1] != 0) && (var[i][n] > var[i][n+1])
            )
        {
          lit[n] = var[i][n];
          var[i][n] = var[i][n+1];
          var[i][n+1] = lit[n];
        }
      }
    }
    for (i = 0 ; i < 7 ; i++)
    {
      for(n=0 ; n<out ; n++)
      {
        varb[i][n] = 0;
        vars[i][n] = 0;
      }
    }

    for(n=0 ; n<out ; n++)
    {
      if ((var[0][n] != 0) && (var[0][n] < minimum))
      {
        minimum=var[0][n];
```

```c
      maxs[0]=var[0][n+1];
    }
  }
  for (i = 0 ; i < 7 ; i++)
  {
    for(n=0 ; n<out ; n+=2)
    {
     if ((var[i][n] != 0) && (var[i][n] > maxs[0] ))
     {
       varb[i][n]=var[i][n];
       varb[i][n+1]=var[i][n+1];
       if (varb[i][n] < minimumb)
       {
         minimumb=varb[i][n];
       }
     }
    }
  }
  printf ( "\n minimumb= %f", minimumb );
  for (i = 0 ; i < 7 ; i++)
  {
    for(n=0 ; n<out ; n+=2)
    {
      if ((var[i][n] != 0) && (var[i][n] <= maxs[0] ))
      {
        vars[i][n]=var[i][n];
        vars[i][n+1]=var[i][n+1];
        printf( "\n \t %f  %f  %f  %d",vars[i][n],vars[i][n+1],var1[i],n);
      }
    }
  }
  mins[0]=maxs[0]=maxs[1]=maxs[2]=maxs[3]=maxs[4]=maxs[5]=maxs[6]=minimum;
  minb[0]=maxb[0]=maxb[1]=maxb[2]=maxb[3]=maxb[4]=maxb[5]=maxb[6]=minimumb;
  for(i=0 ; i<7 ; i++)
  {
    for(n=0 ; n<out ; n++)
    {
      if (  vars[i][n] > maxs[i])
      {
        maxs[i]=vars[i][n];
```

```c
    }
    if (  varb[i][n] > maxb[i])
    {
      maxb[i]=varb[i][n];
    }
  }
}
for (m=0 ; m<6 ; m++)
{
  let1[m+1]=(var1[m]+var1[m+1])/2;
  let[m+1] = ceil (let1[m+1]);
}
let[0]=var1[6];
for(nn=0 ; nn<7 ; nn++)
{
  printf("\n %f   %f  \t  %f   %f \n",maxs[nn],mins[0],maxb[nn],minb[0]);
}
for (ii=1; ii<7 ; ii++)
{
  trs[ii]=fabs(maxs[ii-1]-maxs[ii]);
  printf(" \n trs = %f  \n",trs[ii]);
}
for (ii=1; ii<7 ; ii++)
{
  trb[ii]=fabs(maxb[ii-1]-maxb[ii]);
  if (maxb[ii] == minb[0])
  {
    trb[ii]=fabs(maxb[ii-1]-minb[0]);
  }
printf(" \n trb =[%d] %f  \n",ii,trb[ii]);
}
trb[0] = maxb[6] - minb[0];
trs[0] = maxs[6] - mins[0] ;
printf("v= %f  %f \n",v[k],trs[0]);
for (jj=0; jj<7; jj++)
{
  tr[jj]=trs[jj]+trb[jj];
  printf(" \n\n %d %f %f %f \n",let[jj],tr[jj],maxs[jj],mins[0]);
}
printf("v= %f",v[k]);
```

```c
    rate = (nr/ 3600.00)*T[k]*1e-9 ;
    for(iii=0 ; iii<7 ; iii++ )
      {
        err = err+ errb(let[iii])*tr[iii]/T[k];
      }
    prob=err*rate;
    probability[k]=probability[k]+prob;
    fprintf(fp2," %f \t  %.3e  %0.3e \n",v[k],prob,probability[k]);
    printf(" %f \t  %.3e  %0.3e  %0.3e \n",v[k],prob,err,probability[k]);
    }
}

return 0;
}

double errb(int i)
 {
 double f[100];
 double pi = 3.141592654;
 double a, g, d, sum;
 a = 20 * sqrt(pi / 2);
 int j;
 j = i;
 sum = 0;
 double prob;
 do
 {
   g = (i * i) / (2 * a * a);
   d = exp(-g);
   f[i] = (sqrt(2 / pi))*(((i * i)*d) / (a*a*a));
   i = i + 1;
 }
 while (i<101);
       while (j < 100)
         {
      sum = sum + f[j] + f[j + 1];
          j = j + 1;
         }
 prob = sum / 2 * 1;
 return prob;
```

```
}
```

C

ENERGY CONSUMPTION AND PERFORMANCE

C.1 ENERGY CONSUMPTION AND PERFORMANCE OF CHAIN OF INVERTERS CIRCUIT.

The performance of chain of inverters circuit is affected by the filter stage, this effect is introduced in C.1.
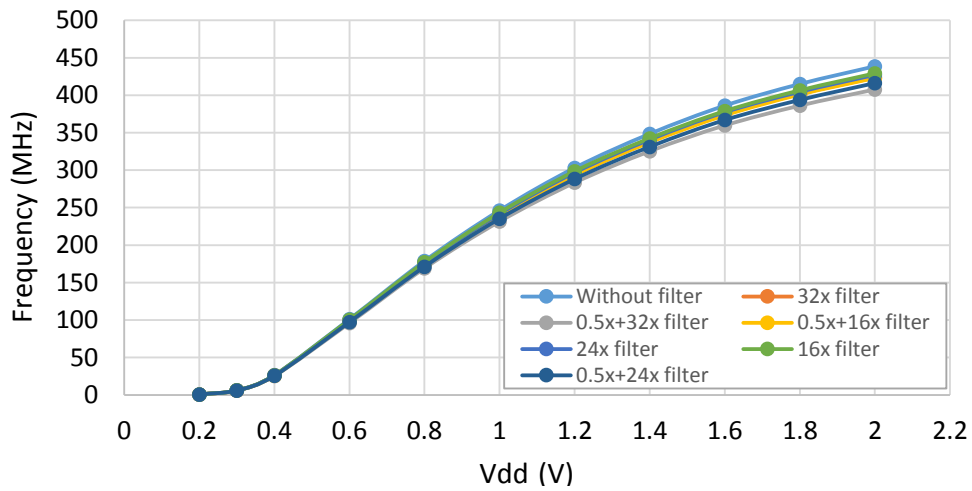
Figure C.1: The effect of the filter stage on the performance of the chain of inverters circuit.

The energy consumption of chain of inverters circuit is affected by the filter stage, this effect is introduced in C.2.
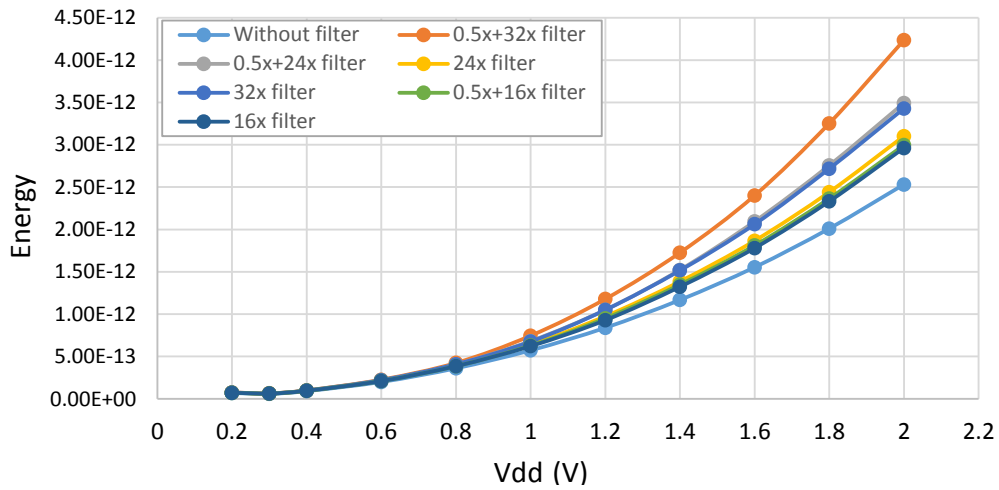
Figure C.2: The effect of the filter stage on the energy consumption of the chain of inverters circuit.

C.2   ENERGY CONSUMPTION AND PERFORMANCE OF C432 CIRCUIT.

The performance of c432 circuit is affected by the filter stage, this effect is introduced in C.3.
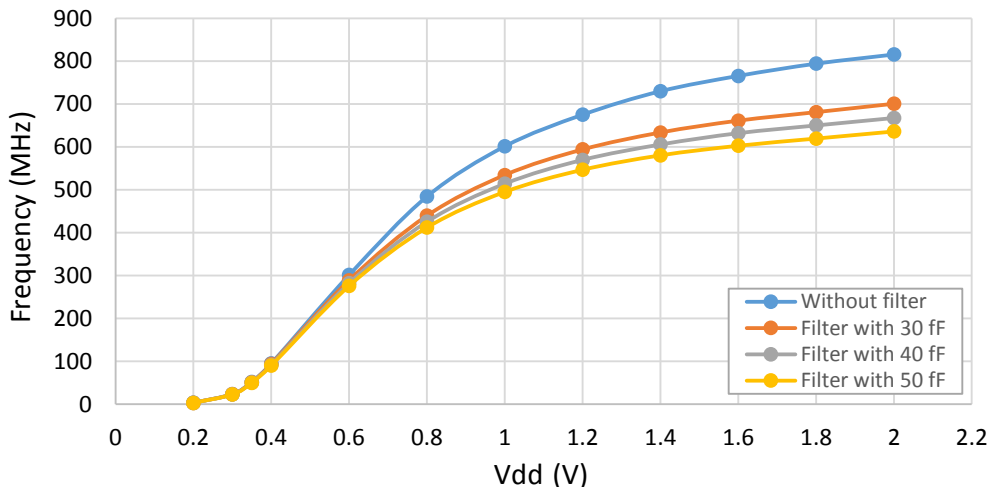
Figure C.3: The effect of the filter stage on the performance of c432 circuit

The energy consumption of chain of inverters circuit is affected by the filter stage, this effect is introduced in C.4.
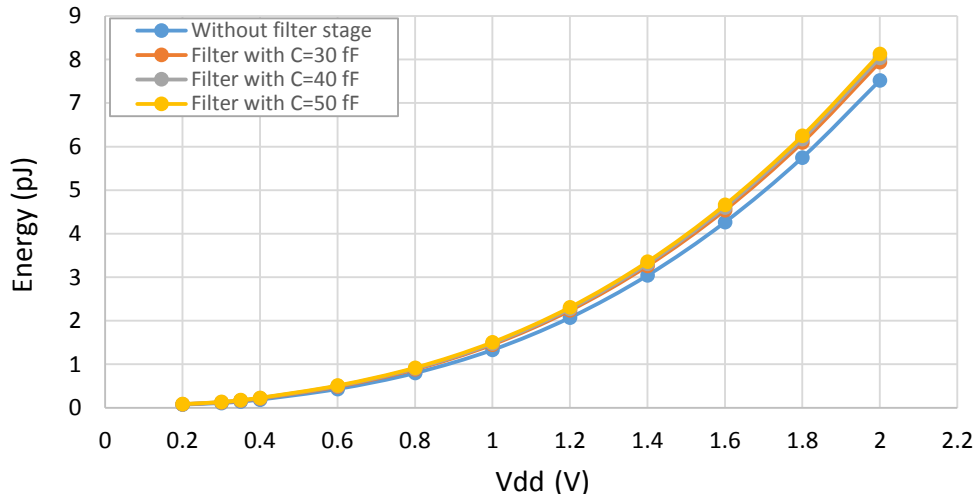
Figure C.4: The effect of the filter stage on the energy consumption of c432 circuit

C.3 ENERGY CONSUMPTION AND PERFORMANCE OF C1908 CIRCUIT.

The performance of c1908 circuit is affected by the filter stage, this effect is introduced in C.5.
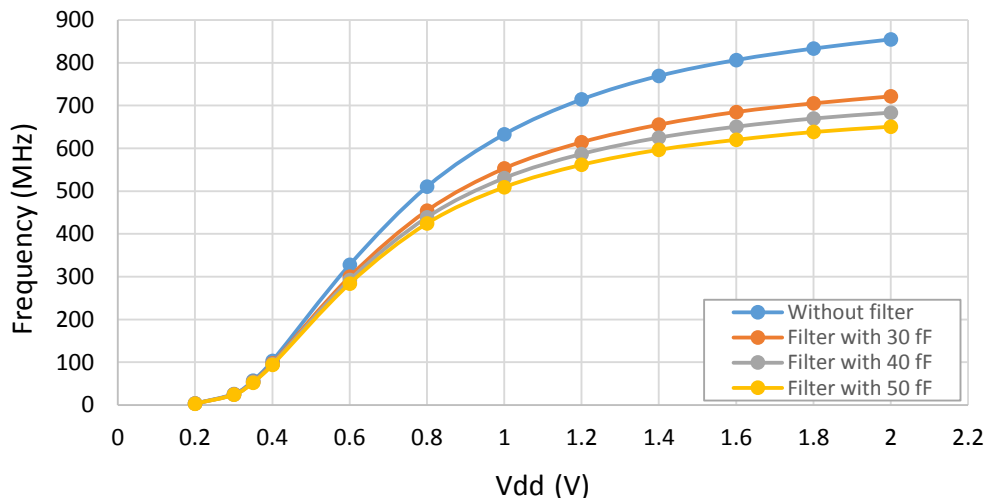
Figure C.5: The effect of the filter stage on the performance of c1908 circuit

The energy consumption of c1908 circuit is affected by the filter stage, this effect is introduced in C.6.
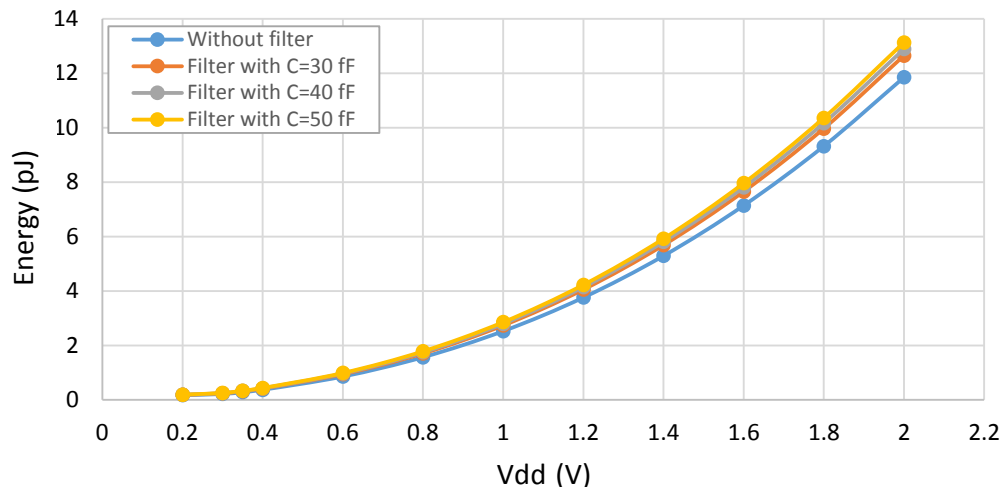
Figure C.6: The effect of the filter stage on the energy consumption of c1908 circuit

Part III

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