Modular DC/DC Converter Topologies for Off-shore DC Collection Point

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Abstract

With the development of the economy, the demand for energy has been substantially growing. Wind power, particularly from offshore wind farms, is one of the best solutions. In Europe, installed capacity had exceeded 8GW by 2105 and will probably reach 40GW in 2020. These ambitious plans require the establishment of large-scale wind farms with more efficient transmission systems. The high voltage direct current (HVDC) transmission system is an effective way to deliver large-scale energy over long distances with lower power losses. However, due to the growth of large-scale offshore wind energy system, the connection between the farms and HVDC transmission lines is more challenging. Medium-voltage DC (MVDC) collection networks are a promising technology for such integration, aiming to eliminate voltage difference. High-voltage high-power DC/DC converters are the key enabler for MVDC grids. But the present lack of suitable high-voltage high-power DC/DC converter topologies is preventing the development of DC networks. Several high-voltage high-power topologies have proposed in previous studies, but most such topologies involve design compromises in terms of switching losses, limited conversion ratios, and lack of modular design, lack of electrical isolation features.

This thesis presents three novel modular DC/DC topologies, which are developed based on the conventional modular multilevel converter (MMC), to enable the integration of off-shore wind farms with high voltage direct current (HVDC) transmission systems. The first topology is a unidirectional single-phase modular DC/DC converter, and the second is a unidirectional three-phase modular DC/DC converter consisting of a windfarm-side three-phase modular multilevel (MMC) inverter and a series-connected diode rectifier module linked by a special decoupled medium frequency transformer. The third topology is a bidirectional three-phase modular DC/DC converter where a three-phase MMC inverter produces a controllable AC voltage connected at the primary side of a three-phase decoupled medium frequency transformer. The secondary output voltages decoupled into three identical but 120-degree phase-shifted voltages. Simulations using MATLAB/Simulink are reported to demonstrate the effectiveness of the proposed converters. Moreover, a low voltage scaled-down prototype of the unidirectional

single-phase modular DC/DC converter is developed to validate its feasibility experimentally.

Keywords: Modular multilevel converter, offshore wind farm, unidirectional/bidirectional modular DC/DC converters, HVDC system.

Dedication

I dedicate this thesis to my grandparents, parents, and girlfriend.

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List of Symbols

B_{pk} : Maximum allowable core flux density

f_{AC} : Fundamental AC frequency

f_c : Carrier frequency

I_{cir} : Circulating current

I_{Px} : AC output current

I_{xU} : Upper arm current

I_{xL} : Lower arm current

I_{dc1} : Input DC current

I_{dc2} : Output DC current

$I_{P\alpha\beta}$: Orthogonal pair of the primary AC current

I_{Pdq} : D-axis and q-axis components of the primary AC current

J : Current density

k_p : Proportional constant

k_i : Integral constant

k : Unbalanced factor

K_v : Voltage waveform factor

K_u : Window utilization ratio

L_{Parm} : Primary arm inductance

L_{Sarm} : Secondary arm inductance

L_o : Output inductance

P_{copper} : Copper losses

P_{dc2} : Output power

P_{core} : Core losses

P_d : Dielectric losses

P_T : Transformer losses

P_{IGBT_x} : IGBT losses

R_c : Carrier-reference frequency ratio

T_1 : Upper Switch

T_2 : Lower Switch

V_c : Submodule capacitor voltage

V_{SM} : Submodule output voltage

V_{dc1} : Input DC voltage

V_{dc2} : Output DC voltage

V_{Px} : Primary output AC voltage

V_{xU} : Upper arm voltage

V_{xL} : Lower arm voltage

V_s : Secondary equivalent voltage

$V_{P\alpha\beta}$: Orthogonal pair of the primary AC voltage

V_{Pdq} : D-axis and q-axis components of the primary AC voltage

V_{core} : Core volume

λ_1 : Submodule number of primary MMC per arm

λ_2 : Module number of secondary diode bridge rectifiers

λ_3 : Module number of secondary one-leg MMC modules

η : Efficiency

List of Abbreviations

AC	: Alternating current
CPS	: Carrier phase shift
DC	: Direct current
DSP	: Digital signal processor
DAB	: Dual active bridge
GTO	: Gate turn-off thyristor
HVDC	: High voltage direct current
HVAC	: High voltage alternating current
IGBT	: Insulated gate bipolar transistor
IPOS	: Input parallel output series
ISOS	: Input series output series
IPOP	: Input parallel output parallel
ISOP	: Input series output parallel
ISIPOS	: Input series input parallel output series
KVL	: Kirchhoff voltage laws
MMC	: Modular multilevel converter
MFT	: Medium frequency transformer
PD	: Phase deposition
SPWM	: Sinusoidal pulse width modulation
SM	: Submodule
SAB	: Single active bridge
VSC	: Voltage source converter

Chapter 1. Introduction

1.1 Historical Development of HVDC Systems

In 1882, the French physicist Marcel Deprez used a DC generator installed in the Miesbach coal mine to send electricity at 2kV to an international exhibition in Munich via 57 km of telegraph line, completing the first ever test [1]. With the development of the modern economy, the demand for electricity in society has been rapidly increasing. However, due to the lower voltage in early versions of transmission systems, a huge power loss resulted. This problem becomes worse over longer distances, thus hindering the development of DC transmission systems.

In the 1880s and 1890s, the principle of multi-phase AC circuits was gradually mastered, and transformers and induction motors were created which greatly enhanced voltage levels, transmission capacity and power system reliability. As a result, AC has almost completely replaced DC and has developed into today's massive power systems. However, DC transmission still has advantages, such as delivering large-scale energy over long distances with less power loss, and no capacitive AC current for long-distance transmission [2]. Therefore, many countries, including the United States, Sweden, and Germany, continued to investigate HVDC technology and developed pilot projects. However, after the successful development of the controllable mercury arc rectifier in 1928, HVDC transmission systems began to develop rapidly [3].

Since the 1950s, the demand for electricity has been growing considerably, and the scale of power systems has further expanded. Meanwhile, the the AC system has encountered a series of insurmountable technical difficulties. On the other hand, successful research into high-power converters has overcome the technical obstacles to HVDC transmission. All of these factors have contributed to the development of current HVDC systems.

In 1970, the American company GE developed the first thyristor. This overcame the

shortcomings of the mercury arc valve, such as high reverse-arc failure rates, low reliability and the inconvenience of operation and maintenance [4]. The operational performance and reliability of HVDC transmission can be improved, and this promotes the development of HVDC transmission technology.

In recent years, developers of HVDC technology have accomplished a historical breakthrough based on voltage source converter (VSC) technology and fully-controlled power electronic power devices, such as the gate turn-off thyristor (GTO) and insulation gate bipolar transistors (IGBTs) [5-7]. This technology introduces fully-controlled power electronics into the field of DC transmission systems and significantly improve the controllability and flexibility of DC transmission technology.

1.2 Comparison of HVDC and HVAC Transmission Systems

Two kinds of transmission system coexist in modern transmission engineering: high voltage AC (HVAC) transmission and high voltage DC (HVDC) transmission [8]. Both of these two transmission methods have advantages and disadvantages. The following comparison of HVDC and HVAC transmission systems illustrates their respective value in applications.

The advantages of HVAC transmission are mainly manifested in the areas of power generation and distribution. According to the principle of electromagnetic induction, the alternator can economically and easily convert other forms of mechanical energy and chemical energy into electricity [9]. The cost of AC sources and substations is lower than for a DC power supply and DC converter stations with the same power. Meanwhile, AC can be easily boosted and stepped down using transformers, which is very convenient when delivering power.

The advantages of HVDC transmission are mainly manifested in the processes of power transmission, as described below:

1) Compared with three-wire three-phase HVAC transmission, only two wires are required for DC transmission. Therefore, based on the same cross-sectional area of the transmission line and current density when transferring the same power, a one-third saving in DC transmission lines and insulation materials can be achieved even without considering skin effects [10-12]. If

skin effects and other types of losses, such as dielectric loss in insulating material and eddy current loss from magnetic induction, are taken into consideration, the cross-sectional area of AC transmission lines will be 1.33 times bigger when compared with DC transmission lines transmitting the same level of power [10-12]. Therefore, the amount of wire used in DC transmission is almost half that in AC transmission. Meanwhile, the structure of the DC transmission tower is simpler than for three-phase AC transmission, and the area occupied by the line corridor is also smaller [10-12].

2) In some special cases, underground and submarine cables are necessary when high-voltage transmission lines pass cities and narrow seaways respectively. Due to the presence of coaxial capacitors between the cable core and the earth, no-load capacitor current is significant in HVAC transmission lines [13]. For instance, a 200kV cable has a capacitance of about 0.2μF per kilometre, requiring about 3×103kVar of reactive power [13]. Whereas in DC transmission, there is essentially no capacitive current applied to the cable due to the small voltage fluctuations. It is worth noting that the consumption of this reactive power of the transmission lines per kilometre can be calculated by the following equation:

$$Q_{c\_loss} = 2 \cdot \pi \cdot f_{AC} \cdot C_{equivalent} \cdot {V_{line}}^2 \tag{1.1}$$

Where f_{AC} is the fundamental frequency of the transmission system ($f_{AC} = 50\text{Hz}$); V_{line} and $C_{equivalent}$ are the voltage and equivalent capacitance of the transmission lines.

3) When using AC for long-distance transmission, a significant phase shift in the voltage will occur at both ends of the power transmission system [10], which requires complex compensation. Otherwise, a large circulating current may form in the power transmission system which would damage equipment or cause outage accidents.

1.3 Offshore Wind Farm System

Due to topographic factors, wind speeds at different altitudes on land vary greatly, which leads to large changes in wind speed in the vertical direction. As a result, imbalances in the forces acting on the top and bottom of the wind turbines cause the transmission system to be

easily damaged [14-17]. However, there is no such problem at sea, where the surface is very flat with almost no resistance, and the average wind speed is high with less variation compared to that on land. Moreover, changes in wind direction at sea are also smaller than on land, and so the wind energy at sea is more stable. It is well known that the power generated by a wind turbine is proportional to the cube of the wind speed, and the wind speed at sea is about 20% higher than that on land [14-17]. Therefore, the annual generating capacity of an offshore wind turbine can be 70% higher than that on land.

A larger power generation capacity means larger wind turbine blades, which leads to restrictions on their transport on land. However, this would be much easier at sea. Furthermore, onshore wind farms possess other restrictions such as the availability of land resources and other environmental and operational constraints. Moreover, most major developed cities in the world are situated on the coast, which means that offshore wind energy is the most attractive source of energy. Therefore, it can be concluded that offshore wind power will have broader prospects in future global energy supply systems.

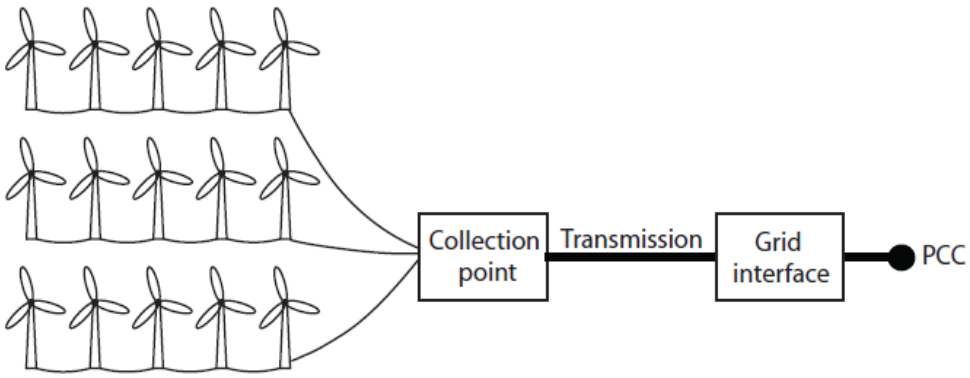
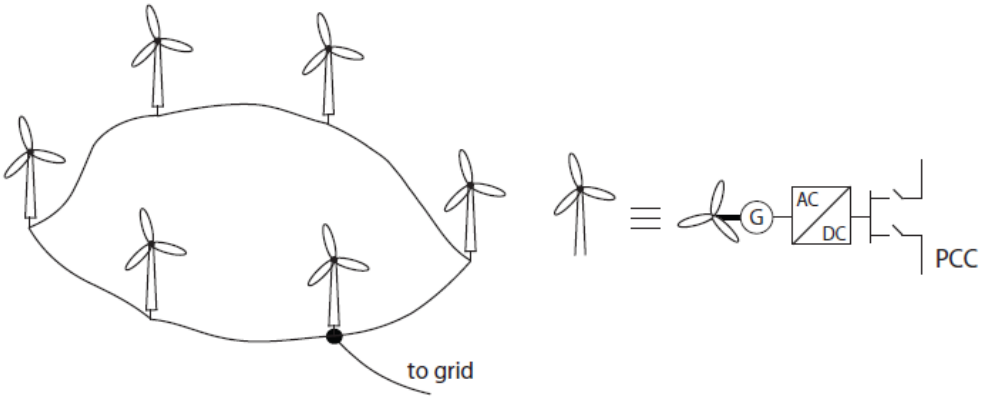


Figure 1.1 A basic offshore transmission system [2].

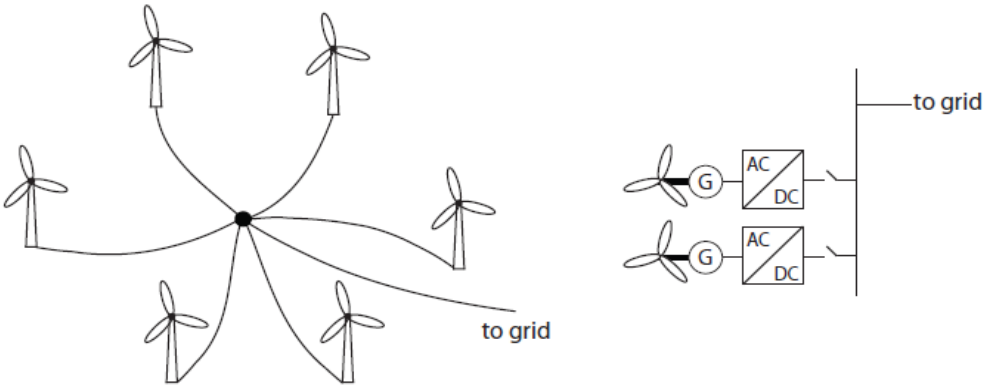
Offshore wind power systems usually consist of offshore wind farms, power transmission cables, and distribution lines, as shown in figure 1.1 [2] [18] [19]. Many wind turbines are grouped and connected to a local AC or DC grid to form an offshore wind farm. This local grid is then connected to the power transmission cable via a converter or transformer, and eventually, the energy is transmitted to the onshore power distribution system.

In a wind farm, there are generally two types of wind turbine connection, which are star and

loop connections as shown in figure 1.2. The different layouts of offshore wind farm transmission systems are also shown below [2]. (It is worth noting that the layouts of offshore shown in figures 1.3, 1.4 and 1.5 are star connection, and figure 1.6 is loop connection).



(a)



(b)

Figure 1.2 Wind turbine connection mode: (a) loop connection (b) star connection[2].

1) AC collection for wind farms:

Figure 1.3 shows a typical schematic diagram of the AC collection of a wind farm, where the output voltage of each wind turbine is generally about 690V [2] [18]. However, for a wind power system with AC collection mode, the voltage level of the AC connection network for the wind turbines is between 20kV and 35kV [18], which requires the output terminal of each wind turbine to be connected to a medium voltage transformer in order to raise the voltage level and render it suitable for connection to the AC network. Then another high voltage transformer is employed on the offshore platform, as shown in figure 1.3, and this boosts the voltage to facilitate the employment of HVAC transmission lines.

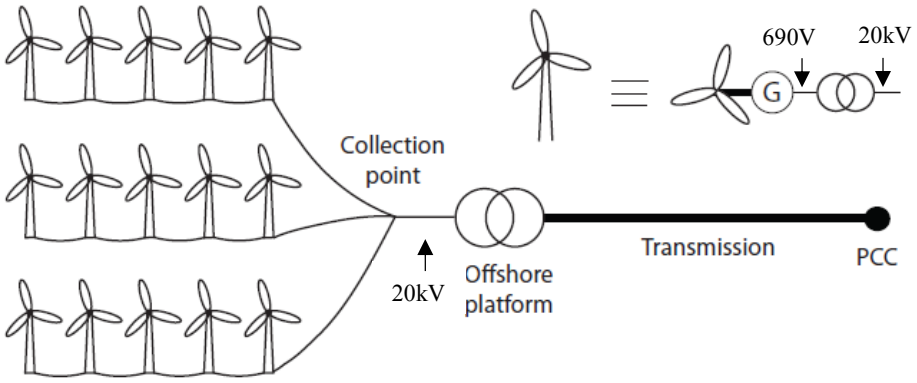


Figure 1.3 General offshore HVAC transmission system with AC collection network [2].

2) Mixed AC/DC collection for wind farm:

Similarly to the AC collection arrangement described above, power is here collected using an AC medium voltage network. Transformers are again employed to raise the voltage produced by the wind turbines, and then another high voltage transformer is employed between the AC collection point and the rectifier side of the HVDC transmission lines, as illustrated in figure 1.4 [2] [18].

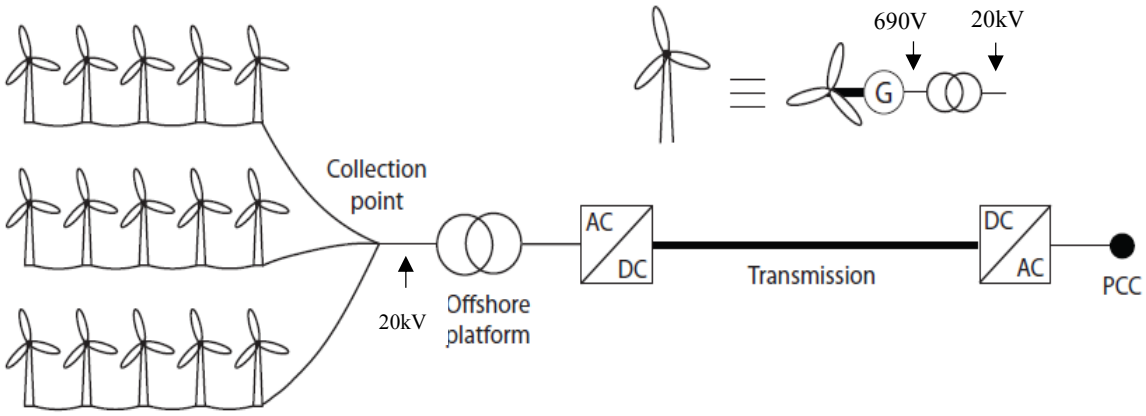


Figure 1.4 General offshore windfarm HVDC transmission system with mixed AC/DC collection network [2].

3) DC collection: parallel-connected wind turbines

Unlike the previous collection scenario, each wind turbine, in this case, is equipped with an AC/DC rectifier with an output voltage of about 690V. However, the typical voltage of the DC

collection network for an offshore system is between 20kV to 40kV, and therefore a medium voltage DC/DC converter is required to raise the voltage [2] [18]. The output of the medium voltage DC/DC converters will then serve as input to the high voltage DC/DC converter that facilitates the connection with the HVDC transmission lines.

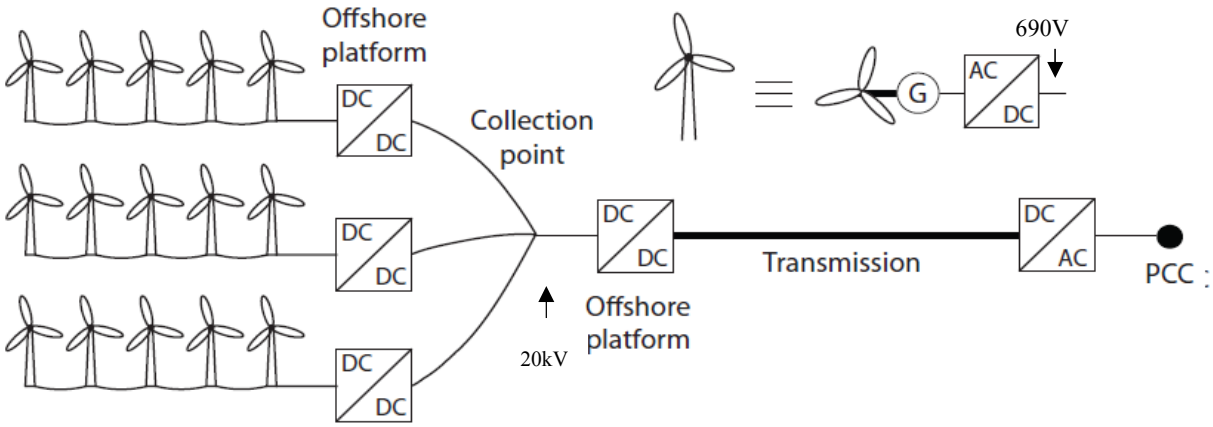


Figure 1.5 General offshore HVDC transmission system with a DC collection (parallel-connected wind turbines) network [2].

4) DC collection: series-connected wind turbines

In this case, all wind turbines in the same cluster are connected in series as shown in figure 1.6. This enables the achievement of high voltage without additional DC/DC boost converters. However, if one wind turbine is out of service, then the other wind turbines need to compensate for the voltage loss, which results in increased voltage stress and energy loss [2] [18].

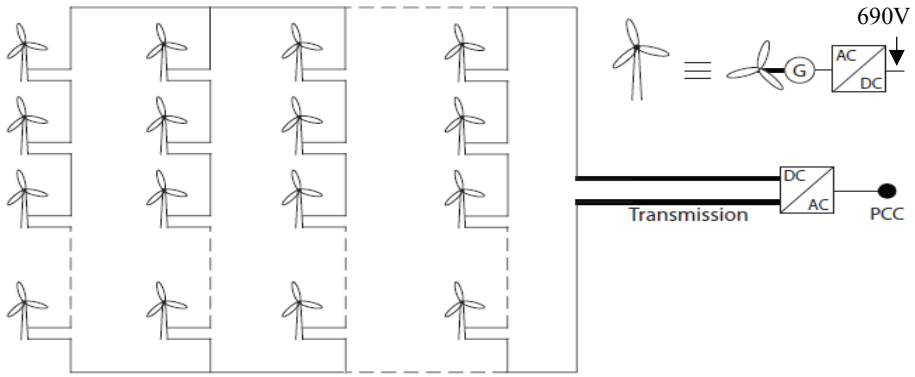


Figure 1.6 General offshore HVDC transmission system with DC collection (series-connected wind turbines) network [2].

1.4 Real Examples of Offshore HVDC Systems

At present, many offshore HVDC systems have been built by large companies such as Siemens, ABB, C-EPRI, and Alstom. Table 1.1 shows the detailed parameters of some typical offshore HVDC projects.

Table 1.1 Detailed parameters of some typical offshore HVDC projects [19].

Wind Park	Power (MW)	Voltage (kV)	Cable Length(km)	Manufacturer	Commissioning
BorWin1	400	±150	200	ABB	2009
DolWin1	800	±320	165	ABB	2015
DolWin2	900	±320	135	ABB	2017
HelWin1	576	±250	130	Siemens	2015
HelWin2	690	±320	130	Siemens	2015
SylWin1	864	±320	210	Siemens	2015
BorWin2	800	±300	200	Siemens	2015
BorWin3	900	±320	160	Siemens	Expected in 2019
DolWin6	900	±320	90	Siemens	Expected in 2023
DolWin3	800	±320	160	Alstom	2017
DolWin5	900	–	115	Tennet	(To be built by 2025)
BorWin5	900	–	125	Tennet	(To be built by 2025)

Projects developed by ABB [19]:

1) **BorWin1 offshore HVDC project (2009):** BorWin1 was the first offshore HVDC project in Germany. This project is used to connect Park BARD Offshore1 and other wind farms near Borkum to the European power grid, where the cable length is 200km, and the rated voltage and power are ±150kV and 400MW respectively.

2) **DolWin1 offshore HVDC project (2015)**: This HVDC project was designed to provide the grid connection of offshore wind farms off the coast of Germany and to transmit power to the German power grid, where the cable length is 165km, and the rated voltage and power are ±320kV and 800MW respectively.

3) **DolWin2 offshore HVDC project (2017)**: This project has a similar function to the above DolWin1 project and is also employed to transmit offshore wind power to the German power

grid, where the cable length is 135km, and the rated voltage and power are ±320kV and 900MW respectively.

Projects developed by Siemens [19]:

1) **HelWin1 offshore HVDC project (2015)**: HelWin1 is part of the German Energy Transition program. It was built to connect two offshore wind farms, Nordsee and Meerwind, to the German power grid, where the cable length is 130km, and the rated voltage and power are ±250kV and 576MW respectively.

2) **HelWin2 offshore HVDC project (2015)**: This project was built to transmit the offshore wind energy to the German power grid, where the cable length is 130km, and the rated voltage and power are ±320kV and 690MW respectively.

3) **SylWin1 offshore HVDC project (**2015): This project was used to connect the offshore wind farm Dan Tysk to the power grid of Germany. The cable length is 210km, and the rated voltage and power are ±320kV and 864MW respectively.

4) **BorWin2 offshore HVDC project (2015):** This project is used to connect two offshore wind farms, Veja Mate and Global Tech 1, to Germany power grid, where the cable length is 200km, and the rated voltage and power are ±300kV and 800MW respectively.

5) **BorWin3 offshore HVDC project (2015):** This project is the most recent offshore HVDC project in Germany. It is expected to be finished in 2019. The cable length of this project is 200km, and the rated voltage and power are ±300kV and 800MW respectively.

The project developed by Dong Alstom: [19]

1) **DolWin3 offshore HVDC project (2017)**: This project is used to transport offshore wind power to the German power grid, where the cable length is 160km, and the rated voltage and power are ±320kV and 800MW respectively.

1.5 Objectives of the Thesis

The main objectives of the thesis are:

- To conduct a comprehensive literature review that can contribute to the development of modular multi-level DC/DC converters.
- To propose novel step-up modular multi-level DC/DC converters which are highly modular and where the voltage stress of the submodules is considerably reduced compared to the conventional DC/DC converters.
- To develop detailed analytical models for each proposed converter to identify and understand the various parameters that define their operating characteristics.
- To conduct a comparison with conventional DC/DC converters that demonstrates the superiority of the proposed converters.
- To develop a low-voltage scaled-down laboratory prototype to validate the feasibility of the proposed converter experimentally.

1.6 Thesis Contributions and Publications

The main original contributions of this research work are as follows:

- A novel unidirectional single-phase modular DC/DC converter is developed (Chapter 4).
- A control method based on a rotating reference frame is developed for the proposed unidirectional single-phase modular DC/DC converter (Chapter 4).
- A novel unidirectional three-phase modular DC/DC converter is proposed (Chapter 5).
- A control strategy based on the d-q rotating reference frame for the proposed unidirectional three-phase modular DC/DC converter is developed (Chapter 5).
- A novel bidirectional three-phase modular DC/DC converter is developed (Chapter 6).

- Two different d-q vector control strategies are developed for the primary and secondary sides of the proposed bidirectional three-phase modular DC/DC converter (Chapter 6).
- A comparison of the proposed DC/DC converters and their existing counterparts is conducted to demonstrate the superiority of the proposed converters (Chapter 7).

Reports of most of the above outcomes have been published in the following papers:

Journals:

[1] **He Liu**, Mohamed Dahidah, James Yu, R.T. Naayagi, and Matthew Armstrong "Design and control unidirectional DC/DC modular multilevel converter for offshore DC collection point: theoretical analysis and experimental validation," *IEEE Transactions on Power Electronics*, August 2018. (Accepted).

[2] **He Liu**, Mohamed Dahidah, James Yu, R.T. Naayagi, and Matthew Armstrong "Unidirectional DC/DC modular multilevel converter for offshore wind farm with the control strategy based on stationary frame," *IET Journal of engineering*, July 2018. (Accepted)

Conferences:

[3] **He Liu**, Mohamed Dahidah, Matthew Armstrong, and R.T. Naayagi "High voltage high power DC/DC modular multilevel converter for offshore windfarm DC collection point," in *Proceedings of the Power Electronics Machines and Drives 8th IET International Conference*, April 2016, pp.1-6.

[4] **He Liu**, Mohamed Dahidah, James Yu, R.T. Naayagi, and Matthew Armstrong "A novel modular multilevel step-up DC/DC converter for offshore systems," in *Proceeding of the Industrial Electronics 2017 IEEE 26th International Symposium*, June 2017, pp.576-581.

[5] **He Liu**, Mohamed Dahidah, James Yu, R.T. Naayagi, and Matthew Armstrong "Unidirectional DC/DC modular multilevel converter for offshore wind farm with the control strategy based on stationary frame," in *Proceedings of the Power Electronics Machines and Drives 9th IET International Conference*, June 2018.

[6] Mohamed Dahidah, **He Liu**, and Vassilios Agelidis "Reconfigurable converter with multiple-voltage multiple-power for E-mobility charging," in *Proceeding of the Power Electronics International Conference*, May 2018.

1.7 Dissertation Outline

The rest of the thesis is organised as follows:

Chapter 2 provides a literature review of conventional high-voltage high-power DC/DC converters which can be employed to build medium-voltage DC (MVDC) collection networks to eliminate extra conversion stages and improve system reliability.

Chapter 3 introduces the basic theoretical analysis of MMCs in terms of the configuration, operational principles, switching modulation methods, submodule voltage control strategies, and arm power fluctuation characteristics. Moreover, a simplified mathematical model of the MMC is also derived in this chapter, which establishes the theoretical basis for the proposed control strategy and modular DC/DC converters developed later.

Chapter 4 proposes a unidirectional single-phase modular DC/DC converter. Detailed theoretical design analysis is presented, and parameters that affect the operation of the proposed converter are defined and thoroughly discussed. This includes configuration, mathematical modelling, and power transfer capability. A control method for the proposed converter based on a rotating reference frame is also developed in this chapter. The performance of the proposed converter is validated through simulation.

Chapter 5 proposes a unidirectional three-phase modular DC/DC converter. As in Chapter 4, the proposed converter in this chapter is also analysed in detail in terms of configuration, mathematical modelling, and power transfer capability. A control strategy based on the d-q rotating reference frame for the proposed converter is derived. Simulation studies under different operating conditions are discussed.

Chapter 6 presents a bidirectional three-phase modular DC/DC converter. The detailed theoretical design process of the proposed converter is also presented. Two different kinds of d-q vector control strategy are developed for the primary and secondary side of the proposed converter. The proposed converter and its control strategy are validated through various simulations.

Chapter 7 analyses and calculates in detail the different losses in the proposed converter and compares them with losses in corresponding competitive topologies. Also, the structure of the

circuit topologies and the overall efficiency and component utilization are compared as well.

Chapter 8 introduces a low-voltage scaled-down laboratory prototype. It details the theoretical design process of the submodule capacitor, arm inductor, and output filter. A case study of a medium frequency transformer is also presented in this chapter. Moreover, the development of a control platform is also briefly introduced. Experimentally validated results are then discussed and analyzed.

Chapter 9 concludes this thesis. Further work is also recommended.

Chapter 2. Conventional High-Voltage High-Power DC/DC Converters

2.1 Introduction

The HVDC transmission system is an effective way to deliver large-scale energy over a long distance with lower power losses [20-22]. Large-scale offshore wind energy systems are increasingly common, and the connection between multiple farms is becoming more challenging. Medium-voltage DC collection networks are a promising technology for such integration, aiming to eliminate extra conversion stages and improve system reliability [36-39]. High-voltage high-power DC/DC converters, and especially modular multilevel DC/DC converters have gradually become key enablers for the DC grid. In this chapter, various high-voltage high-power DC/DC converters are investigated and reviewed. These can be broadly classified as cascaded, consisting of multiple converter modules [23-25], and modular multilevel topologies [26-27].

2.2 Cascaded Modular DC/DC Converters

Most notably, dual active bridge (DAB) or single active bridge (SAB) converters have received a great deal of attention from researchers due to their distinctive features, such as galvanic isolation and the ability to operate at the high switching frequency. However, the high-voltage and high-power requirements of DC/DC converter-based HVDC systems necessitate series and parallel combinations at both the power semiconductor devices and converter module levels [28]. Such systems are commonly referred to as cascaded modular DC/DC converters. According to the different connection modes, cascaded modular DC/DC converters can be divided into four basic types as shown in figure 2.1: 1) input-parallel output-series (IPOS) [29-40]; 2) input-parallel output-parallel (IPOP) [41-48]; 3) input-series output-parallel (ISOP) [49-65]; 4) input-series output-series (ISOS) [66-74]. Furthermore, the inputs

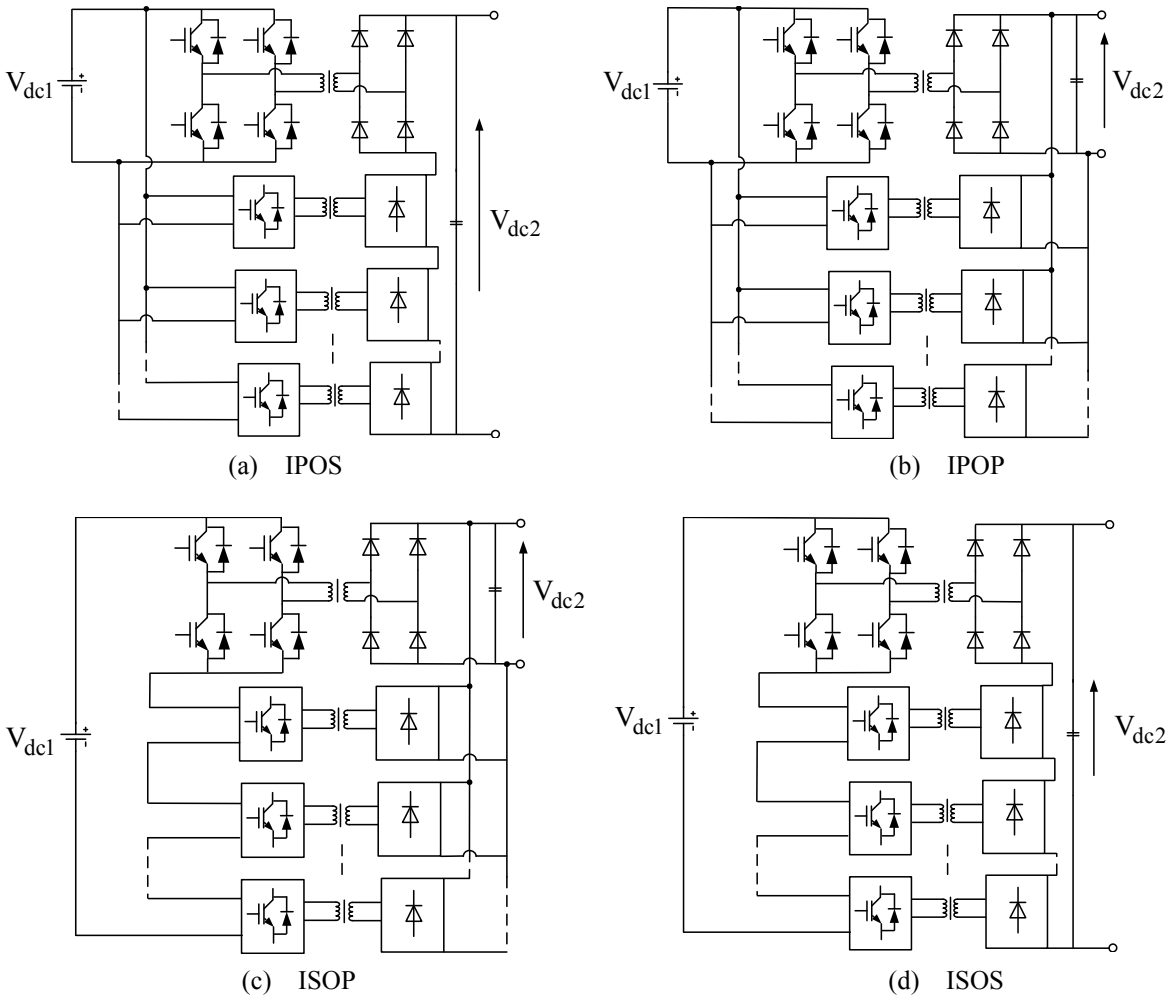


Figure 2.1 Schematic diagrams of unidirectional cascaded DC/DC converters: (a) input-parallel output-series (IPOS); (b) input-parallel output-parallel (IPOP); (c) input-series output-parallel (ISOP); (d) input-series output-series (ISOS).

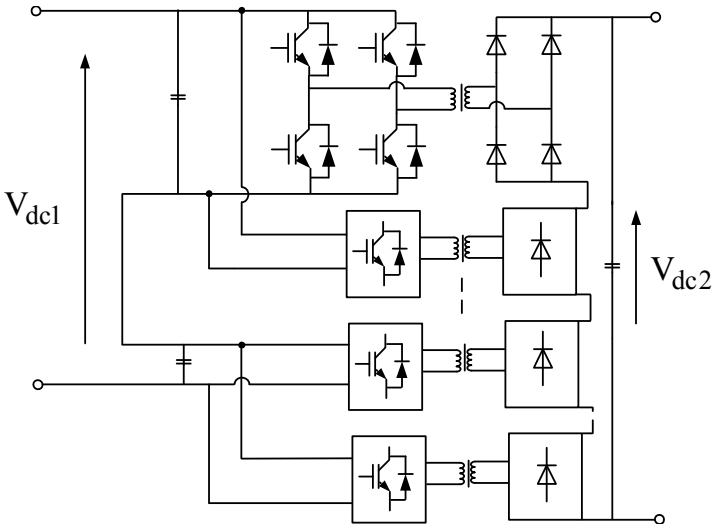


Figure 2.2 Schematic diagram of unidirectional cascaded input-series-input-parallel output-series (ISIPOS) DC/DC converter.

and outputs of these four types of series-parallel configurations can be further combined [28], thereby obtaining enhanced hybrid series-parallel combined topologies, as shown in figure 2.2 [28]. An input-series-input-parallel configuration can effectively decrease the voltage and current stress of the power devices at the primary side. The output-series configuration at the secondary side makes the converter more suitable for high voltage applications. At present, cascaded modular DC/DC converters are widely employed in many engineering applications due to their specific advantages, which include highly modular design, lower voltage and current stress, redundancy characteristics, and higher power density. According to the characteristics of different configurations, each type of cascade modular DC/DC converter has particular applications. For example, the ISOS configuration is suitable for applications where input and output voltages are higher, while the IPOP configuration is suitable for applications where the input and output currents are higher. The IPOS configuration is always employed for applications with high input current and high output voltage, whereas the ISOP configuration is found in applications involving high input voltage and high output current.

Several studies have investigated SAB/DAB submodule-based cascaded DC/DC converters as a DC collection point for HVDC systems [28] [75]. However, for such a converter, the soft switching operation is required when operating with high switching frequency. But due to the operational characteristics of SAB/DAB, full soft switching can only be achieved with limited ranges of load and input voltage, which substantially limits the efficiency and the performance of the converter due to increased switching losses [76].To address this problem, an external large resonant inductor is usually connected in series with the transformer so as to extend the soft switching range, but the large inductance has a detrimental effect on the performance of the converter since it results in increased duty cycle losses as well as severe voltage ringing due to the resonance between the inductance and junction capacitance [77]. The concept of using a saturation inductor instead of a linear inductor has been discussed [78], and this effectively extends the soft switching range with lower conduction losses and without significant duty cycle loss. However, a large core is required for thermal dissipation, limiting the whole system's power density and large-scale application. Also, more recently an improved soft switching range with conduction losses eliminated was achieved using additional active switches [79-81].

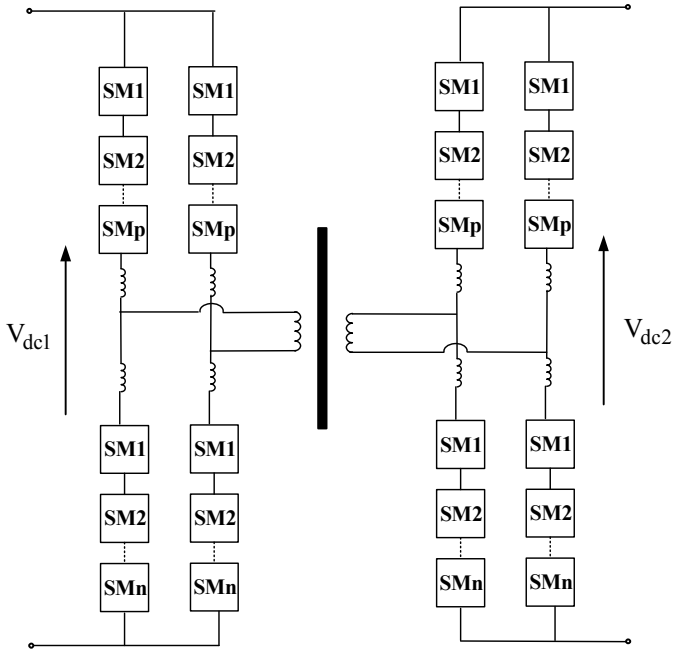
However, the added switches complicate control and increase switching losses, especially in a larger-scale system.

In addition to the methods described above, there is a simpler way to reduce losses. This involves making the converters operate at low frequency. However, it is rare to find a cascaded modular DC/DC converter operating at low or medium frequency (e.g.<500Hz), because the power density of the whole system will be substantially reduced due to the need for large numbers of low or medium frequency transformers and corresponding heat dissipation systems. This would seriously restrict the large-scale engineering applications of cascaded topologies, especially for the offshore platforms with limited space [28] [75].

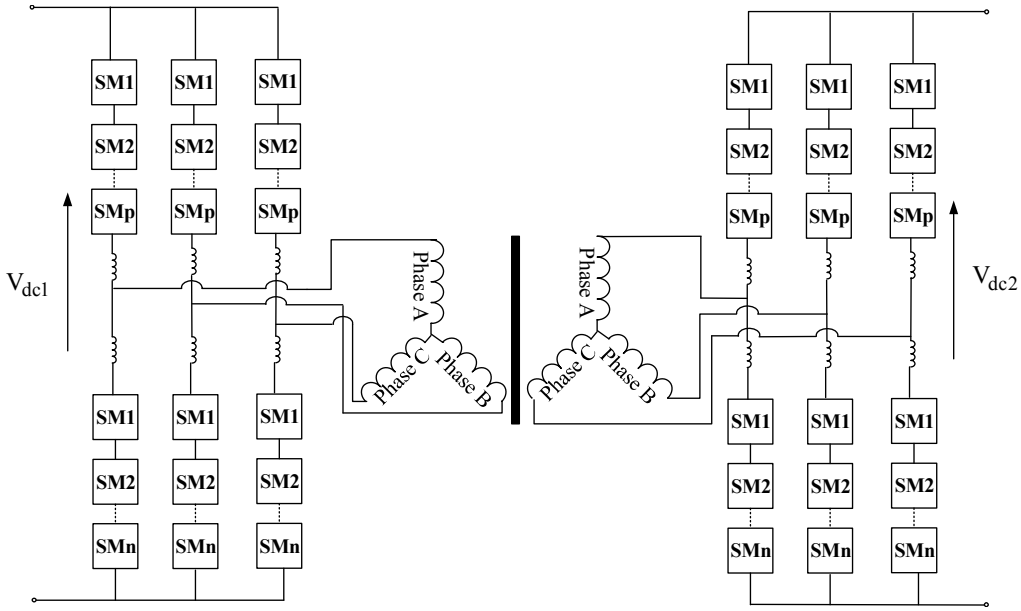
2.3 Modular Multilevel DC/DC Converters

Modular multilevel converters (MMC) as a DC collection point for HVDC systems have also received close attention in recent years, due to the following distinct advantages in the applications with HVDC systems [82-95]:

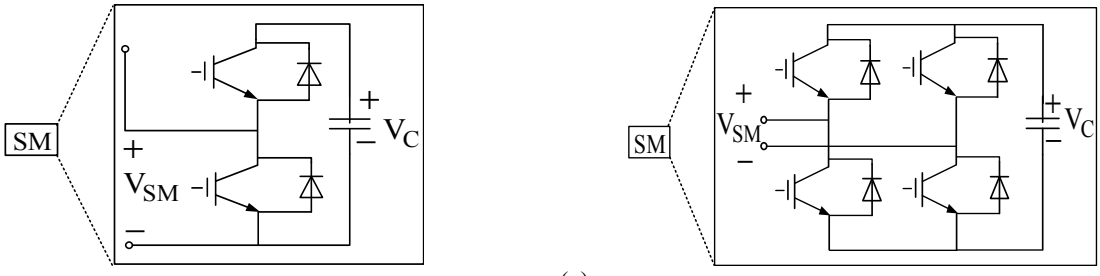
- The number of submodules (SMs) in modular multilevel DC/DC converters can be changed to meet different input/output voltage level requirements in the HVDC system.
- Redundancy in modular multilevel DC/DC converters could effectively improve the reliability of the whole HVDC system.
- Low harmonics waveforms can easily be achieved since a large number of SMs is required when modular multilevel DC/DC converters operate in an HVDC system.
- Due to the highly modular design of modular multilevel DC/DC converters, the development cycle and cost of the whole HVDC system are significantly reduced.
- Generally, most modular multilevel DC/DC converters operate at the low/medium frequency in the HVDC system, hence decreasing switching losses.



(a)



(b)



(c)

Figure 2.3 Two MMC-based DC/DC converters: (a) single-phase; (b) three-phase; (c) their possible half-bridge and full-bridge submodules.

Although modular multilevel DC/DC converters have many advantages in applications of HVDC systems, there are also some challenges. It is well known that when modular multilevel DC/DC converters are used in an HVDC system, large numbers of SMs are required. This not only increases costs but also complicates the control system. Also, a large number of SMs requires an additional control system to balance their voltages, which would be a big challenge associated with modular multilevel DC/DC converters in real engineering applications of HVDC systems.

Different studies [82-95] have proposed a series of MMC-based DC/DC converters as shown in figure 2.3, functioning as a DC collection point for HVDC systems. At present, most MMC-HVDC projects that are put into operation use the half-bridge-based SM, since it has distinct advantages which include the need for fewer power devices, lower system costs, and higher operational efficiency. However, when a DC fault occurs, the MMC itself does not have the capability of active protection, and so the fault needs to be isolated with additional relay protection equipment. To handle DC faults through the action of the MMC itself, many researchers have conducted extensive investigations and proposed various SM configurations with the capability of protection against faults. The most representative configurations of this kind of MMC consist of full-bridge SMs [96-100]. However, the number of power devices required for a full-bridge SM-based MMC is twice that of a half-bridge SM based MMC, which would not only increase costs but also decrease the efficiency of the whole system [101-105]. Also, a hybrid MMC that consists of full-bridge and half-bridge SMs can also provide a DC fault blocking capability, but without a significant increase in the number of power devices compared with a full-bridge SM-based MMC [101-105].

2.4 Research Prospects for High-Voltage High-Power DC/DC Converters

At present, HVDC systems based on modular multilevel DC/DC converters have gradually become the main focus of research, compared to cascaded modular multilevel converters or any other conventional two-level DC/DC converters. However, current research on modular

multilevel DC/DC converters mainly considers mathematical models [92] [98] [101], switching modulation [83] [88] [91] [93] [97] [99], voltage balance control [89] [95], DC-fault blocking [94] [96], SM pre-charging [106], and circulating current suppression [95]. The development of modular multilevel DC/DC converter topologies is still at an early stage. In real engineering applications, the topologies of the modular multilevel DC/DC converters available are very limited. To address this problem, some efforts have been made by researchers to develop more topologies, but many of these involve design compromises in terms of switching losses, limited conversion ratios, and the lack of electrical isolation features. Therefore, in this thesis, an offshore HVDC system will be taken as the application background for modular multilevel DC/DC converters to develop different topologies that can function as DC collection points.

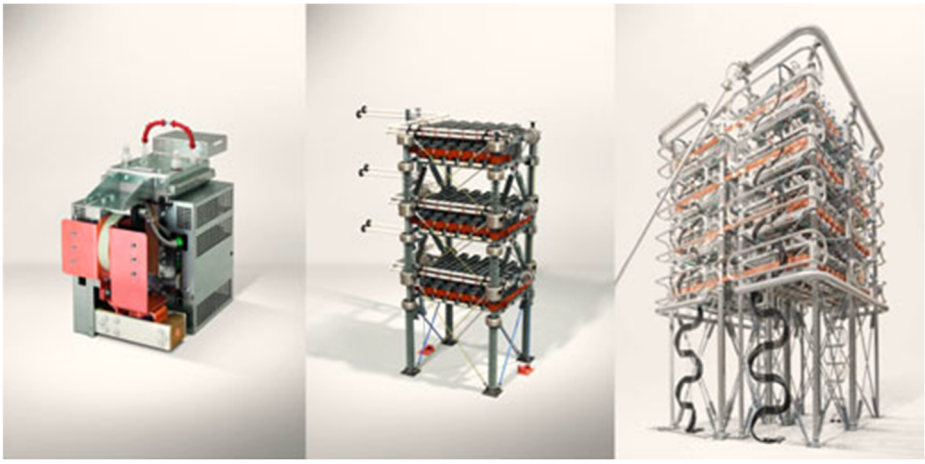
2.5 Summary

This chapter has reviewed the most popular high-voltage high-power DC/DC converters proposed in recent years, including cascaded modular and modular multilevel DC/DC converters. The basic structural characteristics and advantages and disadvantages of these converters have been briefly introduced. Also, the likely directions of further research into high-voltage high-power DC/DC converters have also been considered.

Chapter 3. Basic Theory and Analysis of MMC

3.1 Introduction

The use of the modular multilevel converter (MMC) in high-voltage high-power (HVDC) systems has several advantages, such as low voltage and current stress, feature modularity, high-quality output waveforms, and fault tolerance operation [93]. Hence that has been an increased interest in this topology in the industry and among researchers. Nowadays, more and more HVDC projects have been built based on the MMC topology, as indicated in figure 3.1 which shows a commercial MMC topology developed by Siemens in August 2013 [107]. This chapter focuses on the basic theory of MMC and puts forward the theoretical basis for the proposed control strategies and MMC-based DC/DC converters discussed in the following Chapters 4, 5, and 6.



(a) (b) (c)

Figure 3.1 Commercialized MMC-based HVDC project: (a) submodule of the MMC; (b) MMC arm; (c) complete structure of the MMC [107].

3.2 The Configuration of the MMC and its Basic Operating Principles

Figure 3.2 shows a simplified schematic diagram of a three-phase MMC, where each phase

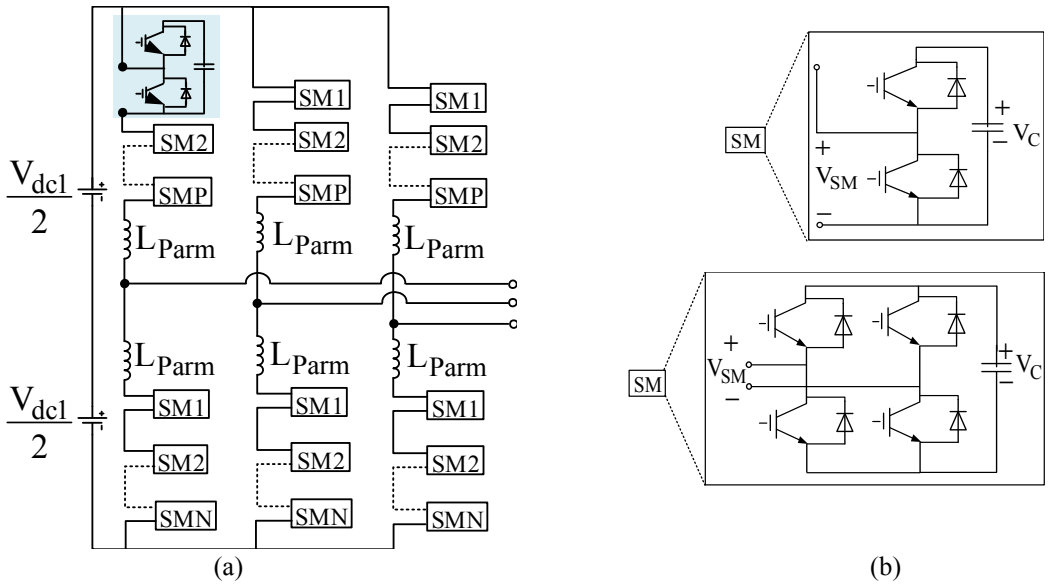


Figure 3.2 Configuration of: (a) three-phase MMC; (b) its possible half-bridge and full-bridge SMs.

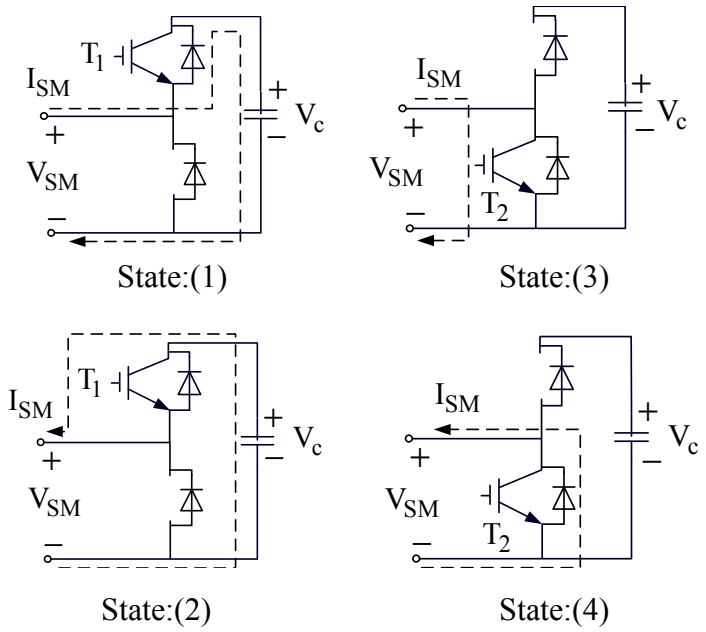


Figure 3.3 Operating states of half-bridge SM.

Table 3.1 Half-bridge SM states of MMC

States	T_1	T_2	I_{SM}	V_{SM}	Submodule
1	ON	OFF	> 0	V_c	charging
2	ON	OFF	< 0	V_c	discharging
3	OFF	ON	> 0	0	By-passed
4	OFF	ON	< 0	0	By-passed

consists of half-bridge/full bridge-based submodules (SMs). It is worth noting that the design is fully modular and can be easily expanded as required by simply adding more modules. Each

phase includes two arm inductors which function as reactors to limit the arm current ripple. The DC voltage source is connected at the DC side of the MMC and three-phase AC voltages can be obtained at the output AC side. Because the half-bridge SM-based MMC is used in the following topology design, the operating modes of the half-bridge SM are described below.

Table 3.1 lists the possible operating modes of the half-bridge-based-SM, where the current directions are schematically presented in figure 3.3 [108]. Taking the upper arm of Phase-a as an example, each SM is either inserted or bypassed, leading the voltage of Phase-a to be either increased or decreased by an SM capacitor voltage,V_c respectively.

When T_2 is turned on and T_1 is turned off, if the current flowing to the SM, $I_{SM} > 0$, the SM is by-passed. Similarly, when T_2 is turned on and T_1 is turned off, if the current flowing to the SM, $I_{SM} < 0$, the SM is also by-passed. Conversely, when T_2 is turned off and T_1 is turned on, if the current flowing to the SM, $I_{SM} > 0$, the SM is in the charging state. Similarly, when T_2 is turned off and T_1 is turned on, if the current flowing to the SM, $I_{SM} < 0$, the SM is in the discharging state.

3.3 Mathematical Model of MMC

It is well known that there are many switches and energy storage components such as arm inductors and SM capacitors, in the circuit of the MMC, which leads to the need for a high-order, discrete mathematical model. Therefore, to simplify the process of analysis, a simplified model of the MMC is required. This can be obtained by a series of transformations as shown in figure 3.4. From figure 3.4, it can be seen that, based on the circuit configuration of the MMC, the physical model of the MMC is given and simplified to an average model through three steps of simplification and coordinate transformation. Finally, the desired low-order and continuous model is achieved, which can substantially decrease the complexity of the analysis of the MMC.

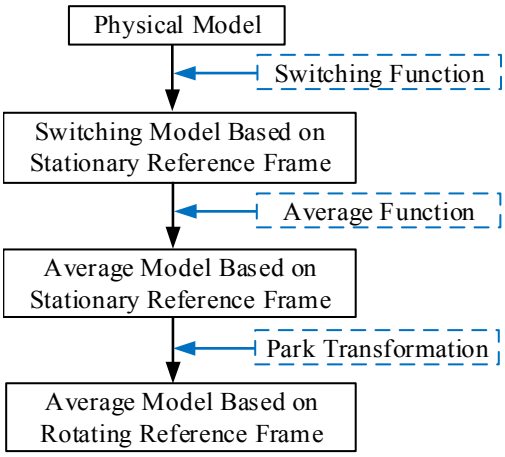


Figure 3.4 Derivation process of a simplified mathematical model of MMC.

3.3.1 *Switching model of MMC*

Figure 3.5 shows the equivalent circuit of one-leg (Phase-a) of the MMC, where V_{dc1} and I_{dc1} are its DC input voltage and current respectively, V_{aU} and V_{aL} are the voltages of the upper and lower arm of Phase-a respectively, I_{aU} and I_{aL} are the currents of the upper and lower arms of Phase-a respectively, E_{Pa} is the equivalent output phase voltage as shown in figure 3.5(b) and V_{Pa} is the output AC voltage, and I_{cir} and I_{Pa} are the circulating and ouput AC currents respectively.

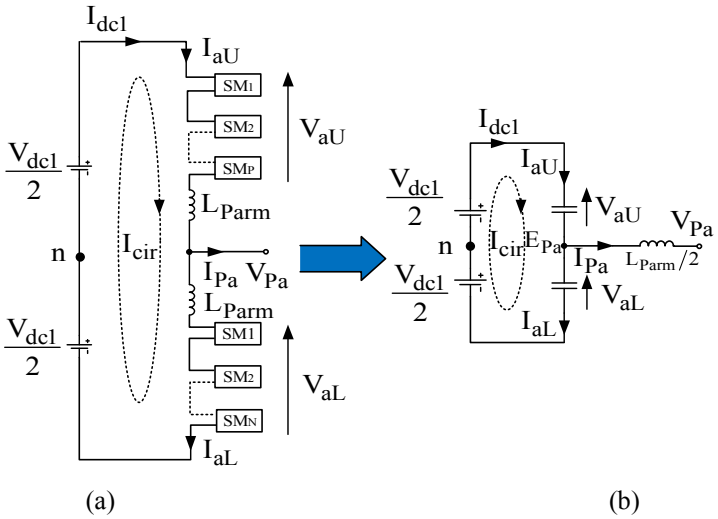


Figure 3.5 One-leg MMC, (a) schematic diagram of the one-leg MMC and (b) equivalent circuit.

From figure 3.5, the upper and lower arm currents of the Phase-a leg can be expressed by:

$$I_{aU} = I_{Pa}/2 + I_{cir} \tag{3.1}$$

$$I_{aL} = -I_{Pa}/2 + I_{cir} \tag{3.2}$$

where the circulating current, I_{cir}, flows through both the upper and lower arms.

It should be noted that the circulating current has no effect on the output phase current and can be expressed as:

$$I_{cir} = (I_{aU} + I_{aL})/2 \tag{3.3}$$

Concerning (3.1) and (3.2), the equation for output AC current I_{Pa} can be expressed in terms of upper and lower arm currents as:

$$I_{Pa} = I_{aU} - I_{aL} \tag{3.4}$$

If *n* is a neutral point, applying the Kirchhoff voltage laws (KVL) to the one-leg MMC shown in figure 3.5(a) allows the upper and lower voltages to be derived as:

$$V_{aU} = \frac{V_{dc1}}{2} - V_{Pa} - L_{Parm}\frac{dI_{aU}}{dt} \tag{3.5}$$

$$V_{aL} = \frac{V_{dc1}}{2} + V_{Pa} - L_{Parm}\frac{dI_{aL}}{dt} \tag{3.6}$$

Combining (3.5) and (3.6), the output phase voltage V_{Pa} can be expressed as:

$$V_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) - \frac{1}{2}L_{Parm}\frac{d(I_{aL}-I_{aU})}{dt} \tag{3.7}$$

Substituting (3.4) into (3.7), the equivalent output phase voltage E_{Pa} can be given by:

$$E_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) = V_{Pa} + \frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} \tag{3.8}$$

Therefore, the mathematical model of the one-leg MMC can be derived by rearranging (4.8) as:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} = E_{Pa} - V_{Pa} \tag{3.9}$$

Therefore, the equivalent circuit of one-leg MMC can be obtained as shown in figure 3.5(b) based on the equation (3.9).

Then, by introducing the switching function into (3.5) and (3.6), the upper and lower arm voltages can be expressed as:

$$V_{aU} = \frac{V_{dc1}}{2} - V_{Pa} - L_{Parm}\frac{dI_{aU}}{dt} = \sum_{i=1}^{\lambda_1} S_{aU_i} V_{SM\_aU\_i} \tag{3.10}$$

$$V_{aL} = \frac{V_{dc1}}{2} + V_{Pa} - L_{Parm}\frac{dI_{aL}}{dt} = \sum_{i=1}^{\lambda_1} S_{aL_i} V_{SM\_aL\_i} \tag{3.11}$$

where λ_1 is the number of SMs per arm of the MMC, $V_{SM\_aU\_i}$ and $V_{SM\_aL\_i}$ are the i^{th} SM voltages of the upper and lower arm in Phase-a respectively, and S_{aU_i} and S_{aL_i} are the i^{th} SM switching function of the upper and lower arms in Phase-a respectively.

Rearranging (3.10) and (3.11), and taking the current flowing to the SM capacitor into consideration, the following switching model of MMC is derived:

$$\begin{cases} L_{Parm}\frac{dI_{aU}}{dt} = \frac{V_{dc1}}{2} - V_{Pa} - \sum_{i=1}^{\lambda_1} S_{aU_i} V_{SM\_aU\_i}\ (i = 1,2,\dots\lambda_1) \\ L_{Parm}\frac{dI_{aL}}{dt} = \frac{V_{dc1}}{2} + V_{Pa} - \sum_{i=1}^{\lambda_1} S_{aL_i} V_{SM\_aL\_i}\ (i = 1,2,\dots\lambda_1) \\ C\frac{dV_{SM\_aU\_i}}{dt} = S_{aU_i} i_{aU} (i = 1,2,\dots\lambda_1) \\ C\frac{dV_{SM\_aL\_i}}{dt} = S_{aL_i} i_{aL} (i = 1,2,\dots\lambda_1) \end{cases} \tag{3.12}$$

where *C* is the capacitance of the SM.

Similarly, the average model for Phases b and c of the MMC can also be obtained in the same manner. Therefore, the overall average model of the three-phase MMC can be expressed as:

$$\begin{cases} L_{Parm}\frac{dI_{a,b,cU}}{dt} = \frac{V_{dc1}}{2} - V_{Pabc} - \sum_{i=1}^{\lambda_1} S_{a,b,cU_i} V_{SM\_a,b,cU\_i} (i = 1,2,\dots\lambda_1) \\ L_{Parm}\frac{dI_{a,b,cL}}{dt} = \frac{V_{dc1}}{2} + V_{Pabc} - \sum_{i=1}^{\lambda_1} S_{a,b,cL_i} V_{SM\_a,b,cL\_i}\ (i = 1,2,\dots\lambda_1) \\ C\frac{dV_{SM\_a,b,cU\_i}}{dt} = S_{a,b,cU_i} i_{a,b,cU} (i = 1,2,\dots\lambda_1) \\ C\frac{dV_{SM\_a,b,cL\_i}}{dt} = S_{a,b,cL_i} i_{a,b,cL} (i = 1,2,\dots\lambda_1) \end{cases} \tag{3.13}$$

where $V_{SM\_abcU\_i}$ and $V_{SM\_abcL\_i}$ represent the i^{th} SM voltages of the upper and lower arms in Phases a, b, and c, respectively, and S_{abcU_i} and S_{abcL_i} are the i^{th} SM switching functions of upper and lower arms in Phases a, b, and c, respectively. It should be noted that the three phases of MMC are annotated as *a,b,c* in (3.13).

3.3.2 *Average model of MMC*

The process of deriving the average model of the MMC represents the process of averaging the discrete switching function and different electrical quantities such as voltages and currents. The whole process can be explained as follows.

a) The process of averaging the discrete switching function

In order to reduce the order of the mathematical model of the MMC, it is assumed that all the SM capacitor voltages of the three Phases a, b, and c are well balanced and ripple-free, which means that every single SM voltage is equal to the average voltage value of all the SMs in the three phases of the MMC. This can be expressed, taking Phase-a as an example, as follows:

$$V_{SM\_aU\_i} = V_{SM\_aL\_i} = V_{SM} \quad (i = 1,2, \dots \lambda_1) \tag{3.14}$$

where V_{SM} is the average SM voltage of the three-phase MMC.

Substituting (3.14) into (3.10) and (3.11) respectively, the switching functions of the upper and lower arms can be expressed as [109]:

$$\frac{1}{V_{SM}}\left(\frac{V_{dc1}}{2} - V_{Pa} - L_{Parm}\frac{dI_{aU}}{dt}\right) = \sum_{i=1}^{\lambda_1} S_{aU_i} \tag{3.15}$$

$$\frac{1}{V_{SM}}\left(\frac{V_{dc1}}{2} + V_{Pa} - L_{Parm}\frac{dI_{aL}}{dt}\right) = \sum_{i=1}^{\lambda_1} S_{aL_i} \tag{3.16}$$

As mentioned above, V_{Pa} is the output AC voltage of Phase-a, which can be defined as:

$$V_{Pa} = \hat{V}_m \sin(\omega t) \tag{3.17}$$

where $\hat{V}_m$ is the peak value of the output AC voltage, V_{Pa}.

Let M_1 be the modulation index of the MMC output AC voltage. Therefore, the peak output voltage, $\hat{V}_m$, can then be given by:

$$\hat{V}_m = \frac{1}{2}M_1 V_{dc1} = \frac{1}{2}M_1\lambda_1 V_{SM} \tag{3.18}$$

Substituting (3.17) and (3.18) into (3.15) and (3.16), the SM switching function can be obtained as follows:

$$\frac{\lambda_1}{2} - \frac{1}{2}M_1\lambda_1 \sin(\omega t) - \frac{1}{V_{SM}}L_{Parm}\frac{dI_{aU}}{dt} = \sum_{i=1}^{\lambda_1} S_{aU_i} \tag{3.19}$$

$$\frac{\lambda_1}{2} + \frac{1}{2}M_1\lambda_1 \sin(\omega t) - \frac{1}{V_{SM}}L_{Parm}\frac{dI_{aL}}{dt} = \sum_{i=1}^{\lambda_1} S_{aL_i} \tag{3.20}$$

According to the operating characteristics of the MMC, the voltage drop across the arm inductor is quite small where most of input DC voltage falls on the SMs of each phase, and hence it can be neglected [109]. Therefore, from (3.19) and (3.20), a further simplified SM switching function can be obtained as follows:

$$\frac{\lambda_1}{2} - \frac{1}{2}M_1\lambda_1 \sin(\omega t) = \sum_{i=1}^{\lambda_1} S_{aU_i} \tag{3.21}$$

$$\frac{\lambda_1}{2} + \frac{1}{2}M_1\lambda_1 \sin(\omega t) = \sum_{i=1}^{\lambda_1} S_{aL_i} \tag{3.22}$$

According to a previous study [109], the average SM switching function can be obtained by dividing the (3.21) and (3.22) by the numbers of SMs per arm, λ_1, and the corresponding equations are shown as follows:

$$\frac{1}{2} - \frac{1}{2}M_1 \sin(\omega t) = \overline{S_{aU_i}} \tag{3.23}$$

$$\frac{1}{2}+\frac{1}{2}M_1\sin(\omega t)=\overline{S_{aL_\iota}} \tag{3.24}$$

where $\overline{S_{aU_\iota}}$ and $\overline{S_{aL_\iota}}$ are the SM average switching functions of the upper and lower arms in Phase-a respectively.

From (3.23) and (3.24), the SM average switching function is derived as the superposition of the DC and AC components. To facilitate the subsequent coordinate transformation, the average SM switching functions are defined as follows:

$$\overline{S_{aU_\iota}}=\frac{1}{2}D_{dc}-D_a \tag{3.25}$$

$$\overline{S_{aL_\iota}}=\frac{1}{2}D_{dc}+D_a \tag{3.26}$$

where D_{dc} and D_a represent the DC and AC components of the SM average switching functions respectively.

b) The process of averaging electrical quantities

In general, the average values of continuous electrical quantities such as current and voltage can be obtained from the following generalized mathematical expression:

$$\bar{x}(t)=\frac{1}{T}\int_{t-T}^{t}x(t)\,dt \tag{3.27}$$

where $\bar{x}$ and T represent the average values of x and cycle time respectively.

According to (3.9) and (3.24), the average model of Phase-a can be expressed as:

$$\begin{cases} L_{Parm}\frac{d\overline{I_{aU}}}{dt}=\frac{\overline{V_{dc1}}}{2}-\overline{V_{Pa}}-\sum_{i=1}^{\lambda_1}\overline{S_{aU_\iota}V_{SM\_aU\_\iota}}(i=1,2,\dots\lambda_1) \\ L_{Parm}\frac{d\overline{I_{aL}}}{dt}=\frac{\overline{V_{dc1}}}{2}+\overline{V_{Pa}}-\sum_{i=1}^{\lambda_1}\overline{S_{aL_\iota}V_{SM\_aL\_\iota}}(i=1,2,\dots\lambda_1) \\ C\frac{d\overline{V_{SM\_aU\_\iota}}}{dt}=\overline{S_{aU_\iota}I_{aU}}(i=1,2,\dots\lambda_1) \\ C\frac{d\overline{V_{SM\_aL\_\iota}}}{dt}=\overline{S_{aL_\iota}I_{aL}}(i=1,2,\dots\lambda_1) \end{cases} \tag{3.28}$$

where $\overline{I_{aU}}$ and $\overline{I_{aL}}$ are the average values of the upper and lower arm currents in Phase-a respectively, $\overline{V_{dc1}}$ and $\overline{V_{Pa}}$ are the average values of the input DC voltage and output AC voltage of Phase-a respectively, $\overline{V_{SM\_aU\_\iota}}$ and $\overline{V_{SM\_aL\_\iota}}$ are the i^{th} submodule average voltages of the upper and lower arm in Phase-a respectively, and $\overline{S_{aU_\iota}}$ and $\overline{S_{aL_\iota}}$ are the i^{th} submodule average functions of upper and lower arm in Phase-a respectively.

Substituting (3.14), (3.25) and (3.26) into the average model of Phase-a with equation (3.28)

and rearranging the equations yields:

$$\begin{cases} L_{Parm}\frac{d\overline{I_{aU}}}{dt} = \frac{\overline{V_{dc1}}}{2} - \overline{V_{Pa}} - \frac{\lambda_1}{2}D_{dc}\overline{V_{SM}} + \lambda_1 D_a\overline{V_{SM}} \\ L_{Parm}\frac{d\overline{I_{aL}}}{dt} = \frac{\overline{V_{dc1}}}{2} + \overline{V_{Pa}} - \frac{\lambda_1}{2}D_{dc}\overline{V_{SM}} - \lambda_1 D_a\overline{V_{SM}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{2}D_{dc}\overline{I_{aU}} - D_a\overline{I_{aU}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{2}D_{dc}\overline{I_{aL}} + D_a\overline{I_{aL}} \end{cases} \tag{3.29}$$

Similarly, the average models of Phases b and c can be obtained in the same manner. Therefore, the average model of the three-phase MMC can be expressed as:

$$\begin{cases} L_{Parm}\frac{d\overline{I_{a,b,cU}}}{dt} = \frac{\overline{V_{dc1}}}{2} - \overline{V_{Pa,b,c}} - \frac{\lambda_1}{2}D_{dc}\overline{V_{SM}} + \lambda_1 D_{a,b,c}\overline{V_{SM}} \\ L_{Parm}\frac{d\overline{I_{a,b,cL}}}{dt} = \frac{\overline{V_{dc1}}}{2} + \overline{V_{Pa,b,c}} - \frac{\lambda_1}{2}D_{dc}\overline{V_{SM}} + \lambda_1 D_{a,b,c}\overline{V_{SM}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{2}D_{dc}\overline{I_{a,b,cU}} - D_{a,b,c}\overline{I_{a,b,cU}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{2}D_{dc}\overline{I_{a,b,cL}} + D_{a,b,c}\overline{I_{a,bc,L}} \end{cases} \tag{3.30}$$

It is worth noting that the three phases of the MMC are annotated as *a,b,c.*

Concerning the (3.4), the average value of the output AC current of Phase-a can be expressed in terms of the upper and lower arm currents as:

$$\overline{I_{Pa}} = \overline{I_{aU}} - \overline{I_{aL}} \tag{3.31}$$

To further simplify the average model with (3.30), it is setting that:

$$\overline{I_{Pa}}^{*} = \overline{I_{aU}} + \overline{I_{aL}} \tag{3.32}$$

Substituting (3.31) and (3.32) into (3.30) and rearranging, so that the equations are added to and subtracted from each other, a further simplified average model of Phase-a can be obtained:

$$\begin{cases} L_{Parm}\frac{d\overline{I_{Pa}}}{dt} = 2\overline{V_{Pa}} - 2\lambda_1 D_a\overline{V_{SM}} \\ L_{Parm}\frac{d\overline{I_{Pa}}^{*}}{dt} = \overline{V_{dc1}} - \lambda_1 D_{dc}\overline{V_{SM}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{4}D_{dc}\overline{I_{Pa}}^{*} + \frac{1}{2}D_a\overline{I_{Pa}} \end{cases} \tag{3.33}$$

Similarly, the further simplified average models of Phases b and c can be obtained in the same manner. Therefore, the further simplified average model of the three-phase MMC can be expressed as:

$$\begin{cases} L_{Parm}\frac{d\overline{I_{Pa,b,c}}}{dt} = 2\overline{V_{Pa,b,c}} - 2\lambda_1 D_{a,b,c}\overline{V_{SM}} \\ L_{Parm}\frac{d\overline{I_{Pa,b,c}}^{*}}{dt} = \overline{V_{dc1}} - \lambda_1 D_{dc}\overline{V_{SM}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{4}D_{dc}\overline{I_{Pa,b,c}}^{*} + \frac{1}{2}D_{a,b,c}\overline{I_{Pa,b,c}} \end{cases} \tag{3.34}$$

It is worth noting again that the three phases of the MMC are annotated as *a,b,c*.

Concerning the (3.1), (3.2) and (3.32), it can be easily seen that:

$$\overline{I_{Pa}}^{*} + \overline{I_{Pb}}^{*} + \overline{I_{Pc}}^{*} = 6\overline{I_{cir}} = 2\overline{I_{dc1}} \tag{3.35}$$

where $\overline{I_{dc1}}$ and $\overline{I_{cir}}$ are the average input DC current and circulation current of the MMC respectively.

Adding the three Phases a, b, and c of the second and third equations in (3.34), and then substituting (3.35) into (3.34), the final simplified average model of MMC is obtained:

$$\begin{cases} L_{Parm}\frac{d\overline{I_{Pa,b,c}}}{dt} = 2\overline{V_{Pa,b,c}} - 2\lambda_1 D_{a,b,c}\overline{V_{SM\_Pa,b,c}} \\ L_{Parm}\frac{d\overline{I_{dc1}}}{dt} = \frac{3}{2}\overline{V_{dc1}} - \frac{3}{2}\lambda_1 D_{dc}\overline{V_{SM}} \\ C\frac{d\overline{V_{SM}}}{dt} = \frac{1}{6}D_{dc}\overline{I_{dc1}} + \frac{1}{6}D_{a,b,c}\overline{I_{Pa,b,c}} \end{cases} \tag{3.36}$$

According to (3.36), the equivalent circuit of the final simplified average model of the MMC is presented in figure 3.6.

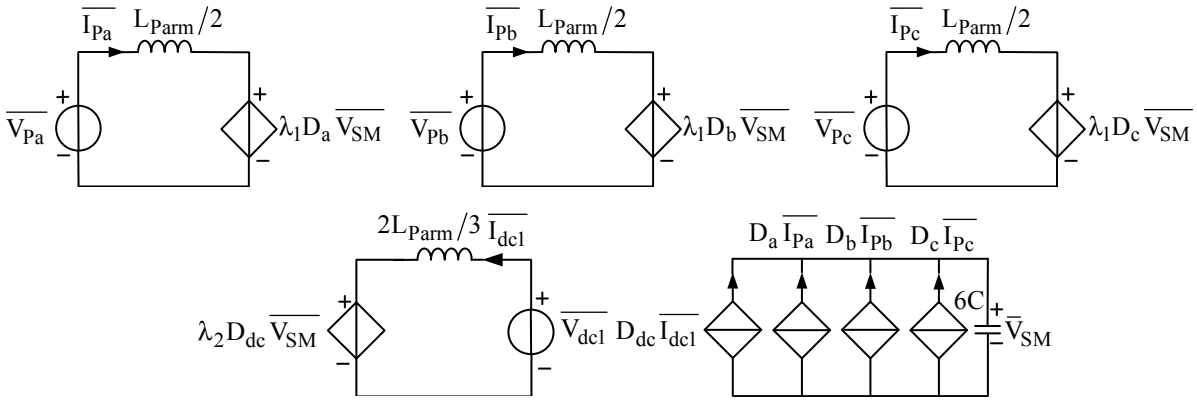


Figure 3.6 Equivalent circuit of the final simplified average model of the MMC.

3.3.3 *dq rotating average model of MMC*

The d-q rotating average model of the MMC can be obtained by transferring the average model of the three-phase MMC in (3.36) from a stationary to a rotating reference frame using the PARK transformation matrix as shown in (3.37).

$$C_{3s/2r} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - 120^{\circ}) & \cos(\theta + 120^{\circ}) \\ \sin\theta & \sin(\theta - 120^{\circ}) & \sin(\theta + 120^{\circ}) \end{bmatrix} \cdot \begin{bmatrix} V_{Pa} \\ V_{Pb} \\ V_{Pc} \end{bmatrix} \tag{3.37}$$

Where θ is the angle change of d-q rotating reference frame, which can also express as $\theta =$

ωt (ω is the fundamental angular speed of the system).

Applying the transformation matrix of (3.37) into the (3.36) yields:

$$\begin{cases} \frac{d}{dt}\begin{bmatrix}\overline{I_d}\\ \overline{I_q}\end{bmatrix} = \frac{2}{L_{Parm}}\begin{bmatrix}\overline{V_d}\\ \overline{V_q}\end{bmatrix} - \frac{2\lambda_1}{L}\begin{bmatrix}D_d\\ D_q\end{bmatrix}\overline{V_{SM}} - \begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\begin{bmatrix}\overline{I_d}\\ \overline{I_q}\end{bmatrix} \\ \frac{d\overline{I_{dc1}}}{dt} = -\frac{3\lambda_1}{2L_{Parm}}D_{dc}\overline{V_{SM}} + \frac{3}{2L_{Parm}}\overline{V_{dc1}} \\ \frac{d\overline{V_{SM}}}{dt} = \frac{1}{6C}D_{dc}\overline{I_{dc1}} + \frac{1}{6C}\begin{bmatrix}D_d\\ D_q\end{bmatrix}^T\begin{bmatrix}\overline{I_d}\\ \overline{I_q}\end{bmatrix} \end{cases} \quad (3.38)$$

According to (3.38), the equivalent circuit of the *d-q* rotating average model of the MMC is illustrated in figure 3.7.

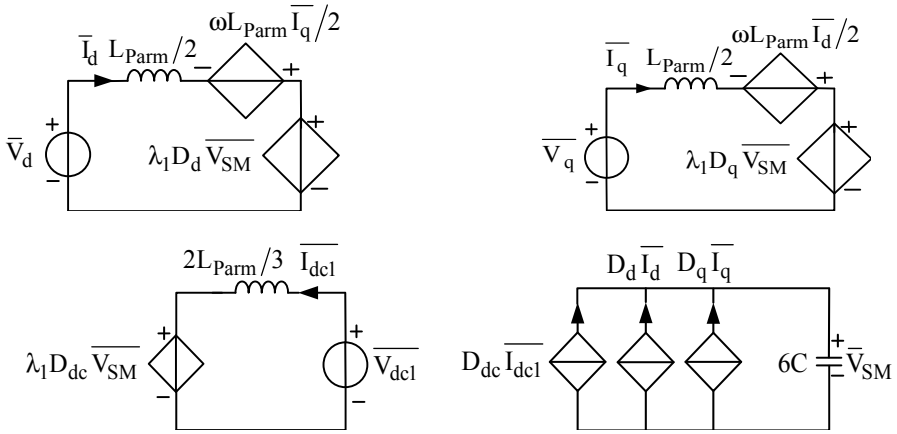


Figure 3.7 Equivalent circuit of the *dq* rotating average model of the MMC.

It is worth noting that the objectives of the modelling are to understand the operation characteristics of the MMC from the perspective of mathematics. Moreover, this section is the theoretical basis for the derivation of the mathematical model of the following proposed topologies in Chapters 4, 5, and 6. Also, the proposed control strategies in Chapters 4, 5, and 6 are developed based on the d-q rotating model shown in this section.

3.4 Power Fluctuation Characteristics in the Arms of the MMC

One of the most challenging aspects of the MMC is to maintain control over the voltage of the SM capacitors. Therefore, it is very important to analyze and understand energy stored and the power flowing between the SMs and the converter arms [108] [110]. To simplify the analysis, the following assumptions are made: 1) the effects of the converter's arm inductance are

neglected; 2) only the fundamental component of the MMC output AC voltage is considered; and 3) only one-leg (i.e. Phase-a) of the MMC converter is considered as an example. Moreover, it is worth noting that the equivalent circuit shown in figure 3.8 is not the actual physical circuit of MMC, which is just pure voltage and current loop and used to analysis the power fluctuation in the circuit. Therefore, the output AC current and voltage of Phase-a can be approximately expressed as:

$$V_{Pa} = \hat{V}_m \sin(\omega t) \tag{3.39}$$

$$I_{Pa} = \hat{I}_m \sin(\omega t - \emptyset) \tag{3.40}$$

where V_{Pa} and $\hat{V}_m$ are the instantaneous output AC voltage and its peak value respectively and I_{Pa} and $\hat{I}_m$ are the instantaneous output AC current and its peak value respectively.

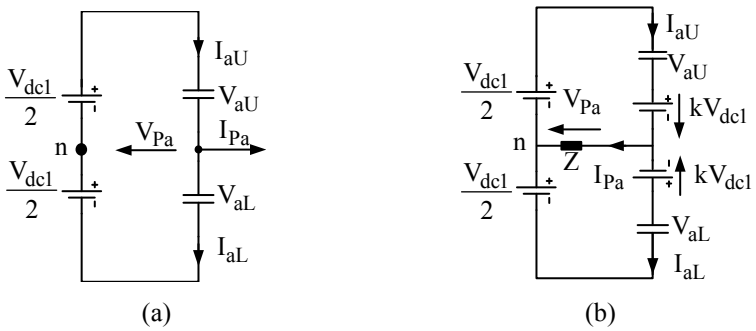


Figure 3.8 Equivalent circuit of one-leg MMC: (a) balanced energy condition; (b) unbalanced energy condition.

The equivalent circuit of a balanced one-leg MMC is shown in figure 3.8 (a), where the upper and lower submodules are modelled as a voltage source. Furthermore, unbalanced energy across the upper and lower arm causes a DC offset to the output AC voltage, which is presented as a DC source denoted by kV_{dc1} where k is defined as the unbalanced factor, $\mathrm{k} \in [-0.1, 0.1]$ [8] in the upper and lower arms as shown in figure 3.8 (b).

Therefore, applying KVL, the upper and lower arm voltages can respectively be defined by (3.41) and (3.42).

$$V_{aU} = \frac{V_{dc1}}{2} - \hat{V}_m \sin \omega t + kV_{dc1} \tag{3.41}$$

$$V_{aL} = \frac{V_{dc1}}{2} + \hat{V}_m \sin \omega t - kV_{dc1} \tag{3.42}$$

Let M_1 be the modulation index of the MMC output AC voltage. Therefore, the peak output

voltage of the one-leg MMC can be then given by:

$$\hat{V}_m = \frac{1}{2} M_1 V_{dc1} \tag{3.43}$$

Rearranging (3.43), the input DC voltage can be expressed as:

$$V_{dc1} = \frac{2\hat{V}_m}{M_1} \tag{3.44}$$

Substituting (3.44) into (3.41) and (3.42) yields:

$$V_{aU} = \frac{\hat{V}_m}{M_1} - \hat{V}_m \sin \omega t + k\frac{2\hat{V}_m}{M_1} \tag{3.45}$$

$$V_{aL} = \frac{\hat{V}_m}{M_1} + \hat{V}_m \sin \omega t - k\frac{2\hat{V}_m}{M_1} \tag{3.46}$$

It is well-known that a DC voltage offset will produce a DC current, denoted as I_{ki} in the upper and lower arms, which is caused by the effect of the unbalanced energy. From figure 3.8 (b), the upper and lower arms currents can be defined as:

$$I_{aU} = I_{dc1} + \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) - I_{ki} \tag{3.47}$$

$$I_{aL} = I_{dc1} - \frac{1}{2}\hat{I}_m \sin(\omega t - \emptyset) + I_{ki} \tag{3.48}$$

As the introduced unbalanced voltage sources are only DC, consequently the resulting currents are DC as well. Furthermore, this current flows through the load impedance, which is naturally inductive; however, only the resistive part of the impedance needs to be considered since the current is DC. (It is noting that DC current offset, I_{ki}, is not the circulating current, which will combined with output AC current of MMC to flow through the load impedance.)

Therefore, the unbalanced DC current, I_{ki}, in the circuit can be calculated by:

$$I_{ki} = \frac{kV_{dc1}}{R} \tag{3.49}$$

where *R* is the load resistance.

Neglecting the power losses in the circuit, the power flowing from the DC side is equal to the power consumed at the AC side of the MMC. Hence,

$$P_{dc} = P_{ac} = V_{dc1} I_{dc1} = \frac{1}{2}\hat{V}_m \hat{I}_m \cos\emptyset + 2I_{ki} \cdot kV_{dc1} \tag{3.50}$$

where V_{dc1} and I_{dc1} are the input DC voltage and current respectively, and $\cos\emptyset$ is the power factor. It is important to note that $2I_{ki} \cdot kV_{dc1}$ is the power consumed caused by DC bias on the AC load.

By substituting $\hat{V}_m$ of (3.43) and I_{ki} of (3.49) into (3.50), the input DC current can be obtained by:

$$I_{dc1} = \frac{1}{4} M_1 \hat{I}_m \cos \emptyset + \frac{4k^2 \hat{V}_m}{R \cdot M_1} \tag{3.51}$$

Now, substituting (3.43), (3.49) and (3.51) into (3.47) and (3.48) yields:

$$I_{aU} = \frac{1}{4} M_1 \hat{I}_m \cos \emptyset + \frac{4k^2 \hat{V}_m}{R \cdot M_1} + \frac{1}{2} \hat{I}_m \sin(\omega t - \emptyset) - \frac{2k \hat{V}_m}{M_1} \tag{3.52}$$

$$I_{aL} = \frac{1}{4} M_1 \hat{I}_m \cos \emptyset + \frac{4k^2 \hat{V}_m}{R \cdot M_1} - \frac{1}{2} \hat{I}_m \sin(\omega t - \emptyset) + \frac{2k \hat{V}_m}{M_1} \tag{3.53}$$

From the above analysis, the instantaneous power of the upper and lower arms is expressed by:

$$P_{aU} = V_{aU} \times I_{aU} = \left(\frac{\hat{V}_m}{M_1} - \hat{V}_m \sin \omega t + k \frac{2\hat{V}_m}{M_1}\right) \cdot \left[\frac{1}{4} M_1 \hat{I}_m \cos \emptyset + \frac{4k^2 \hat{V}_m}{R \cdot M_1} + \frac{1}{2} \hat{I}_m \sin(\omega t - \emptyset) - \frac{2k \hat{V}_m}{M_1}\right] \tag{3.54}$$

$$P_{aL} = V_{aL} \times I_{aL} = \left(\frac{\hat{V}_m}{M_1} + \hat{V}_m \sin \omega t - k \frac{2\hat{V}_m}{M_1}\right) \cdot \left[\frac{1}{4} M_1 \hat{I}_m \cos \emptyset + \frac{4k^2 \hat{V}_m}{R \cdot M_1} - \frac{1}{2} \hat{I}_m \sin(\omega t - \emptyset) + \frac{2k \hat{V}_m}{M_1}\right] \tag{3.55}$$

By integrating (3.54) and (3.55) over one fundamental period, one can obtain the energy variation in the upper and lower arms as follows:

$$E_{aU} = \int_0^{2\pi} P_{aU} dt = \frac{\pi \hat{V}_m}{R} \left(\frac{16 \hat{V}_m k^3}{{M_1}^2} + k \hat{I}_m R \cos \emptyset - \frac{4 \hat{V}_m k}{{M_1}^2}\right) \tag{3.56}$$

$$E_{aL} = \int_0^{2\pi} P_{aL} dt = -\frac{\pi \hat{V}_m}{R} \left(\frac{16 \hat{V}_m k^3}{{M_1}^2} + k \hat{I}_m R \cos \emptyset - \frac{4 \hat{V}_m k}{{M_1}^2}\right) \tag{3.57}$$

Equations (3.56) and (3.57) describe the effect of the unbalanced factor *k* on the arm energy, where, in the case of *k*=0, the energy transferred to the upper and lower arms over one cycle is zero, i.e. $E_{aU} = E_{aL} = 0$. However, when $k \neq 0$, although the transferred energy in one cycle between upper and lower arms remains zero, i.e.$E_{aU} + E_{aL} = 0$; but there will be an unbalanced energy, i.e.$E_{aU} = E_{aL} \neq 0$, which causes deviations in the SM capacitor voltages, and therefore an energy exchange between the upper and lower arms is necessary. Furthermore, as the circulating current influences the charging and discharging of the SM capacitors, therefore it is mandatory to control the circulating current to achieve voltage balance.

3.5 Switching Modulation of the MMC

This section considers the most commonly used methods for the switching modulation of the MMC, which can be broadly divided into two categories 1) space vector-based algorithms and 2) voltage level-based algorithms [2]. At present, most research has focused on voltage level-based algorithms, and there are only a few studies of space vector-based algorithms. This is because voltage level-based algorithms are more easily implemented, especially for an MMC with a large number of SMs. However, with increasing numbers of SMs, the complexity of control in space vector-based algorithms grows considerably. From figure 3.9, the voltage level-based algorithms can be further classified into two types in terms of different switching frequencies. It is well known that high-frequency modulation strategies are commonly developed based on phase-shifted [111] or level-shifted carrier waveforms [112]. Moreover, low-frequency modulation strategies such as selective harmonics elimination (SHE) [113] and nearest level modulation (NLM) [114] are also preferred for the MMC, due to the advantage of lower switching losses. However, as with space vector-based algorithms, increasing the numbers of SMs leads to increased complexity in the control of SHE and NLM. Taking SHE as an example, the process of finding switching angles for each SM becomes quite complex, and a heavy computational load is involved when the numbers of the SMs increase, which would seriously restrict real engineering application [107].

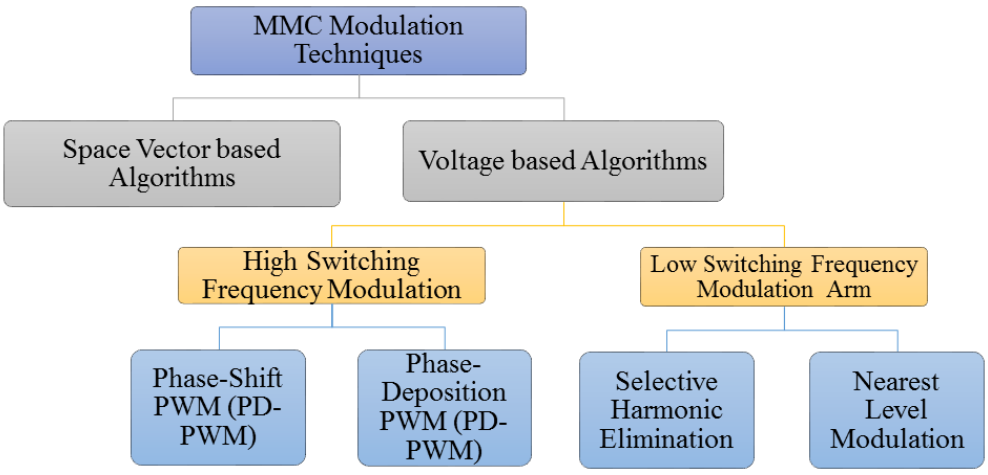
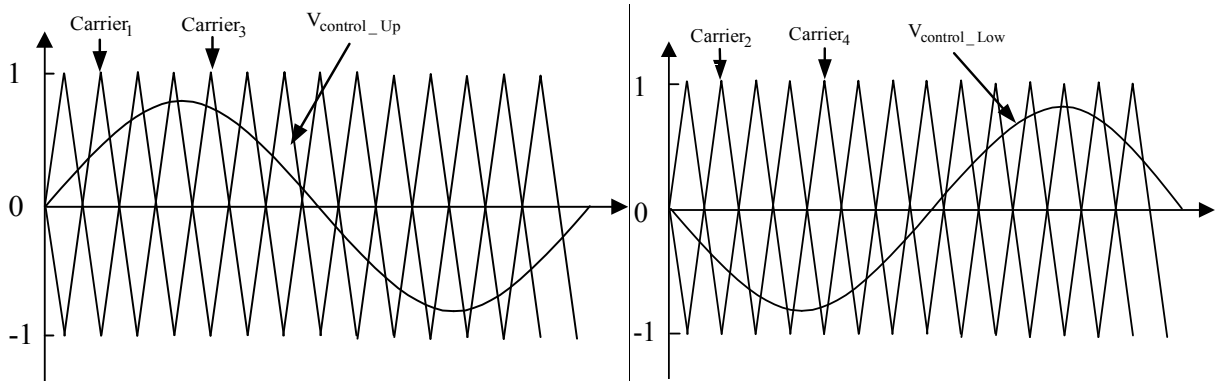


Figure 3.9 Different modulation strategies for the MMC.



(a) (b)

Figure 3.10 Carrier phase-shift modulation strategies(CPS-PWM): (a)upper arm modulation; (b) lower arm modulation.

In this project, a carrier phase-shifted PWM (CPS-PWM) method is applied for the proposed converter. Taking two SMs per arm MMC as an example, the modulation voltage of the upper and lower arms are compared with triangular carriers waveforms $Carrer_1 \sim Carrier_4$, of which phase shift by an angle of $\pi/2$ (2 is the SM number per arm). Moreover, there are 180^o phase shift among upper and lower arm control waveforms as shown in figure.3.10 (a) and (b). The introduction of the phase shift angles modifies the rising and falling edge of the output voltage into multiple staircases (e.g. 2N+1 levels, where N is submodule module number per arm). Based on the CPS-PWM modulation strategy, the amplitude of the output AC voltage of MMC can be controlled from 0 to $\pm \mathrm{M}V_{dc1}$, $\mathrm{M} \in [0, 1]$.

3.6 SM Voltage Balance Control of the MMC

It is well known that the SM capacitors in the MMC are always working in the dynamic mode of charging and discharging, which readily causes voltage imbalances in the SM's capacitor. Therefore, the control of SM capacitor voltage balance is fundamental to the whole MMC control system. In general, voltage balance control is achieved by feeding back the SM capacitor voltages. At present, the most well-known voltage balance control techniques are a PI controller-based balance control strategy [115] and the sorting algorithm [116].

3.6.1 *PI controller-based capacitor voltage balance control strategy*

According to reference [115], the PI controller-based SM voltage balance control of the

MMC can be divided into two parts: average arm voltage control and SM voltage control. It is worth noting that this PI controller-based capacitor voltage balance control strategy is applied to the control of the converters proposed in Chapters 4, 5, and 6.

a) SM capacitor voltage control:

Figure 3.11 illustrates a schematic diagram of an SM voltage balancing control strategy for a one-leg (Phase-a) MMC, where $V_{SM\_2\lambda_1}$ and V_{SM}^{ref} are the SM measured voltage and its reference value respectively, I_{aU} and I_{aL} are the upper and lower arm currents respectively. In figure 3.11, where ± 1 can be obtained by function sign(x), when $x < 0$, its output is -1; when $x > 0$, its output is 1, representing positive or negative arm current respectively. The equivalent mathematical model of the SM capacitor voltage control loop can be expressed by the following equations:

Upper arm:

$$V_{SM\_Factor} = \begin{cases} K_p\left(V_{SM}^{ref} - V_{SM\_2\lambda_1}\right), i_{aU} > 0 \\ -K_p\left(V_{SM}^{ref} - V_{SM\_2\lambda_1}\right), i_{aU} < 0 \end{cases} \tag{3.58}$$

Lower arm:

$$V_{SM\_Factor} = \begin{cases} K_p\left(V_{SM}^{ref} - V_{SM\_2\lambda_1}\right), i_{aL} > 0 \\ -K_p\left(V_{SM}^{ref} - V_{SM\_2\lambda_1}\right), i_{aL} < 0 \end{cases} \tag{3.59}$$

Where V_{SM_Factor} is output modulation factor of SM voltage control loop which will add with control waveform to compare with carrier waveforms as shown in figure3.11. According to (3.58) and (3.59),when $V_{SM}^{ref} < V_{SM\_2\lambda_1}(\lambda_1 \epsilon 1,2,3,\ldots)$: if I_{aU}, I_{aL}>0, the modulation factor V_{SM_Factor} is negative, therefore, the product of I_{aU} or I_{aL} and V_{SM_Factor} forms a negative power to discharge the SM capacitor; if I_{aU}, I_{aL},<0, the modulation factor V_{SM_Factor} is positive, therefore, the product of I_{aU} or I_{aL} and V_{SM_Factor} also forms a negative power to discharge the SM capacitor. when $V_{SM}^{ref} > V_{SM\_2\lambda_1}(\lambda_1 \epsilon 1,2,3,\ldots)$: if I_{aU} , I_{aL} >0, the modulation factor V_{SM_Factor} is positive, therefore, the product of I_{aU} or I_{aL} and V_{SM_Factor} forms a positive power to charge the SM capacitor; if I_{aU}, I_{aL},<0, the modulation factor V_{SM_Factor} is negative, therefore, the product of I_{aU} or I_{aL} and V_{SM_Factor} also forms a positive power to charge the SM capacitor.

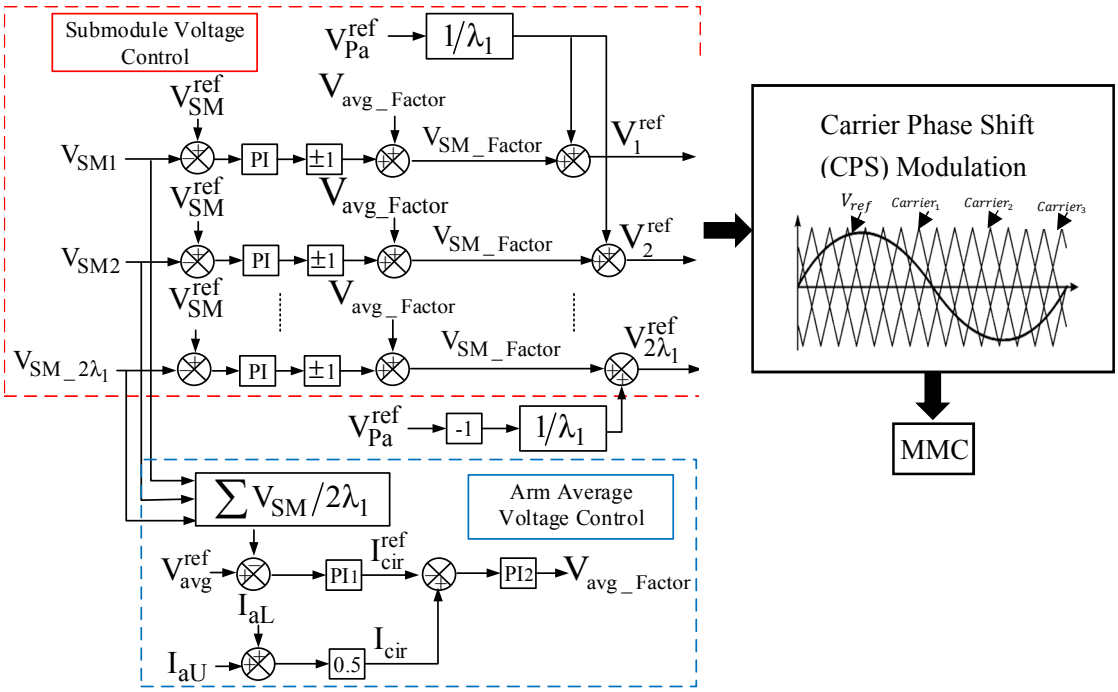


Figure 3.11 Schematic diagram of voltage balancing controllers, including SM voltage (red dotted line) control and arm average voltage control (blue dotted line).

b) Average arm voltage control:

Figure 3.11 also shows a block diagram of the average voltage control, which consists of two control loops: the inner circulating current control and the outer arm average voltage control [109]. In figure 3.11, the circulating current reference, I_{cir}^{ref}, is produced by the controller PI_1, which is acting on the error between the measured average voltage V_{avg}, and its reference value V_{avg}^{ref} of Phase-a. If $I_{cir} \neq I_{cir}^{ref}$, this means that an imbalance exists in the power exchanged between the upper and lower arms, and then the PI_2 is employed to modulate the magnitude of the circulating current in order to eliminate this error. The equivalent mathematical model of the submodule voltage control loop can be expressed by the following equations:

$$I_{cir}^{ref} = K_p\left(V_{avg}^{ref} - V_{avg}\right) + K_i \int \left(V_{avg}^{ref} - V_{avg}\right)dt \tag{3.60}$$

$$V_{avg\_Factor} = K_p\left(I_{cir} - I_{cir}^{ref}\right) + K_i \int \left(I_{cir} - I_{cir}^{ref}\right)dt \tag{3.61}$$

Where V_{SM_Factor} is output modulation factor of SM voltage control loop which will add with control waveform to compare with carrier waveforms as shown in figure3.11.

3.6.2 *Sorting algorithm*

The sorting algorithm sorts the SM capacitor voltages of the upper and lower arms and then, according to the required SM number to be inserted and arm current direction in the circuit, it is determined which SM should be inserted or bypassed is determined. The detailed implementation process of this method is shown as follows:

It is well known that, when the MMC operates in the normal state, the required number of SMs to be inserted in each phase must be equal to λ_1, where λ_1 is the number of the SMs per arm. Taking the lower arm as an example, when this arm is put into one SM, the corresponding upper arm needs to bypass one SM at the same time so as to maintain the total number of SMs inserted in each phase to be equal to λ_1. If the lower arm current $I_{aL} > 0$, the SMs with smaller capacitor voltage in the lower arm will be put into the circuit and charged. Meanwhile, the remaining of the SMs in the lower arm will be by-passed in the circuit. If the lower arm current $I_{aL} < 0$, the SMs with higher capacitor voltage in the lower arm will be put into the circuit and discharged. Similarly, the rest of the SMs in the lower arm will be by-passed. For upper arm SMs, the operating mode is exactly the same. When the upper arm current $I_{aU} > 0$, the SMs with smaller capacitor voltage in the upper arm would be put into the circuit and charged. Conversely, when the upper arm current $I_{aU} < 0$, the SMs with higher capacitor voltage in the upper arm will be put into the circuit and discharged. The whole implementation process of the sorting algorithm is shown schematically in figure 3.12.

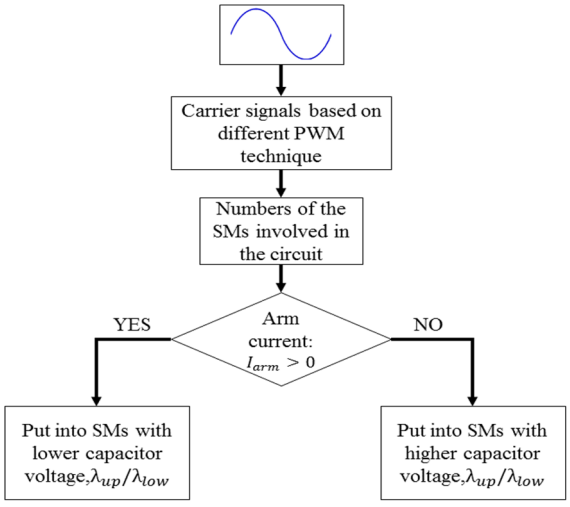


Figure 3.12 Process of the sorting algorithm.

The sorting algorithm has many advantages, including ease of implementation and fast response (A heavy computational load is unnecessary for the sorting algorithm, which would increase the response of this method). However, these advantages come at the expense of increases in the switching frequency of power devices such as IGBT modules, which would cause higher switching losses and hence decrease the overall efficiency of the converter. To solve this problem, many optimized sorting algorithms have been proposed which can effectively decrease the switching frequency and achieve similar control results. Since this is beyond the scope of this project, no further details of this are given.

3.7 Summary

Chapter 3 has mainly introduced the configuration of the MMC and its basic operating principles. Based on the physical model of the MMC, a continuous, low-order mathematical model of MMC is developed. To further understand the operating characteristics of the MMC, the characteristics of power fluctuations in the arms are derived and analyzed in detail. Moreover, the most commonly utilized methods for achieving the switching modulation of the MMC have been investigated and classified. Finally, two common SM voltage balance control strategies were briefly reviewed.

Chapter 4. Unidirectional Single-Phase DC/DC Modular Multilevel Converter

4.1 Introduction

This chapter presents the design, modelling and analysis of the proposed unidirectional single-phase modular DC/DC converter, which enables the integration of an off-shore wind farm with a high-voltage direct current (HVDC) transmission system. The proposed converter consists of a single-phase modular multilevel converter (MMC) inverter coupled with series-connected diode bridge rectifier modules through a medium frequency transformer with multiple secondary windings. The modularity of the proposed converter enables scalability for different voltage levels. In addition to galvanic isolation, the transformer also provides a stepping gain to the output voltage.

4.2 Configuration of the Proposed Converter

Figure 4.1 shows a simplified schematic diagram of the proposed DC/DC converter, where a single-phase (two-leg) or one-leg MMC inverter producing a controllable AC voltage is connected at the primary side of a medium frequency (400Hz) transformer [117]. The DC output voltage is obtained through series-connected full-bridge rectifier modules at the multi-winding secondary side of the transformer. It is worth noting that the design is fully modular at both sides and can be easily expanded by adding more modules as required. The DC output voltage is controlled via control of the AC voltage of the MMC at the primary side.

As can be seen from figure 4.1, the number of secondary windings of the proposed DC/DC converter with a single transformer is high, which increases the complexity of the transformer and thereby decreases its reliability. To address this issue, another version is proposed in figure 4.2, where multiple transformers are used. With the multiple transformers, the number of secondary windings of each transformer can be reduced, simplifying the transformer design.

For simplicity, the following analysis is only presented for a single transformer topology with single-phase (two-leg) MMC as shown in figure 4.1(a). However, it should be noted that this analysis is applicable to other topologies as well since they have the same operating principles, power transfer characteristics, and control system.

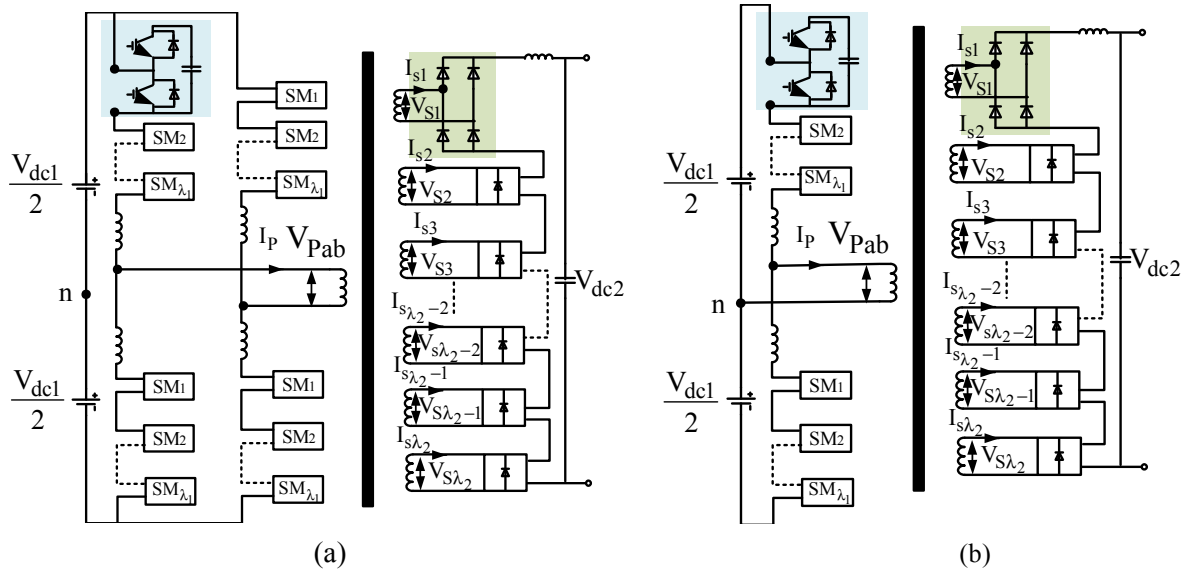


Figure 4.1 Proposed modular DC/DC converter with single transformer: (a) single-phase (two-leg) MMC-based DC/DC converter; (b) one-leg MMC-based DC/DC converter.

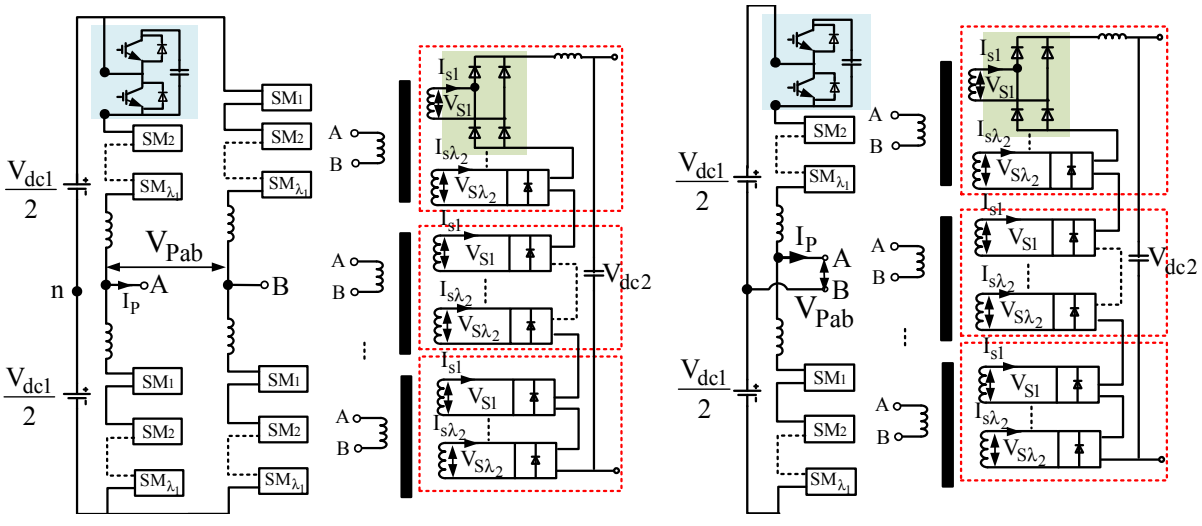


Figure 4.2 Proposed modular DC/DC converter with multiple transformers: (a) single-phase (two-leg) MMC-based DC/DC converter; (b) one-leg MMC-based DC/DC converter.

4.3 Mathematical Model

***For the primary side*:** Figure 4.3 shows the equivalent circuit of one-leg (Phase-a) of the MMC, where V_{dc1} and I_{dc1} are its DC input voltage and current respectively, V_{aU} and V_{aL} are the voltages of the upper and lower arms of Phase-a respectively, I_{aU} and I_{aL} are the currents of the upper and lower arms of Phase-a respectively, E_{Pa} is the equivalent output phase voltage as shown in figure 4.3(b), V_{Pa} is the output AC voltage, and I_{cir} and I_{Pa} are the circulating and ouput AC currents respectively.

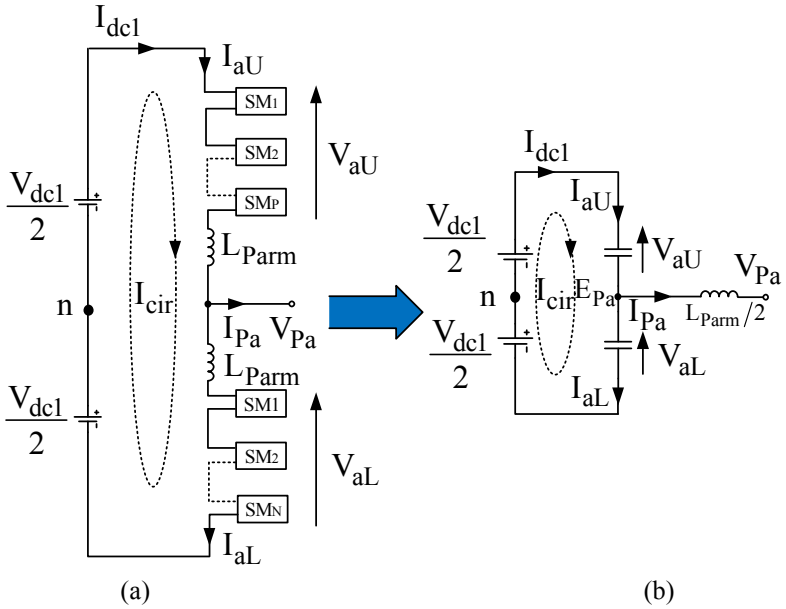


Figure 4.3 One-leg MMC: (a) schematic diagram of the one-leg MMC; (b) equivalent circuit.

From figure 4.3, the upper and lower arm currents of the Phase-a leg can be expressed by:

$$I_{aU} = I_{Pa}/2 + I_{cir} \tag{4.1}$$

$$I_{aL} = -I_{Pa}/2 + I_{cir} \tag{4.2}$$

where the circulating current, I_{cir}, flows through both the upper and lower arms.

It should be noted that the circulating current has no effect on the output phase current and can be expressed as:

$$I_{cir} = (I_{aU} + I_{aL})/2 \tag{4.3}$$

Concerning (4.1) and (4.2), the equation for the output AC current, I_{Pa}, can be expressed in terms of upper and lower arm currents as:

$$I_{Pa} = I_{aU} - I_{aL} \tag{4.4}$$

If *n* is the neutral point, the Kirchhoff voltage law (KVL) is applied to the one-leg MMC shown in figure 4.3(a), and the upper and lower voltages can be derived as:

$$V_{aU} = \frac{V_{dc1}}{2} - V_{Pa} - L_{Parm}\frac{dI_{aU}}{dt} \tag{4.5}$$

$$V_{aL} = \frac{V_{dc1}}{2} + V_{Pa} - L_{Parm}\frac{dI_{aL}}{dt} \tag{4.6}$$

Combining (4.5) and (4.6), the output phase voltage V_{Pa} can be expressed as:

$$V_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) - \frac{1}{2}L_{Parm}\frac{d(I_{aL}-I_{aU})}{dt} \tag{4.7}$$

Substituting (4.4) into (4.7), the equivalent output phase voltage E_{Pa} can be given by:

$$E_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) = V_{Pa} + \frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} \tag{4.8}$$

Therefore, the mathematical model of the one-leg MMC can be derived by rearranging (4.8) as:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} = E_{Pa} - V_{Pa} \tag{4.9}$$

According to (4.9), the equivalent circuit of Phase-a can be presented as shown in figure 4.3(b). Similarly, the mathematical model of the second leg of MMC (i.e. Phase-b), can be given by:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pb}}{dt} = E_{Pb} - V_{Pb} \tag{4.10}$$

where E_{Pb} and V_{Pb} are the equivalent output phase voltage and output AC voltage of Phase-b respectively, and I_{Pb} is the ouptut AC current of Phase-b.

Combining (4.9) and (4.10), the mathematical model of the single-phase (two-leg) MMC can be expressed as:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} - \frac{1}{2}L_{Parm}\frac{dI_{Pb}}{dt} = (E_{Pa} - E_{Pb}) - (V_{Pa} - V_{Pb}) \tag{4.11}$$

For simplicity, let:

$$E_{Pab} = E_{Pa} - E_{Pb} \tag{4.12}$$

$$V_{Pab} = V_{Pa} - V_{Pb} \tag{4.13}$$

Hence, (4.11) can be re-written as:

$$\frac{1}{2}L_{Parm}\frac{d(I_{Pa}-I_{Pb})}{dt} = E_{Pab} - V_{Pab} \tag{4.14}$$

For a single-phase (two-leg) MMC, the relationship between the output currents of Phases a and b can be expressed as :

$$I_P = I_{Pa} = -I_{Pb} \tag{4.15}$$

where I_P is the transformer's primary current in the proposed converter.

Substituting (4.15) into (4.14) yields:

$$L_{Parm}\frac{dI_P}{dt} = E_{Pab} - V_{Pab} \tag{4.16}$$

where E_{Pab} and V_{Pab} can be considered as the transformer's equivalent primary voltage and primary terminal voltage respectively.

***For the secondary side*:** From figure 4.1(a), the secondary side of the transformer is made of a combination of individual and isolated diode bridge rectifier modules. This can be regarded as a series connection of voltage sources ($V_{s1}, V_{s2}, \dots, V_{S\lambda_2}$), which can be seen in the figure 4.1(a). Therefore, the total equivalent voltage at the secondary side of the transformer, V_s, can be expressed as:

$$V_s = V_{s1} + V_{s2} + \cdots + V_{S\lambda_2} \tag{4.17}$$

where λ_2 is the number of diode bridge rectifier modules at the secondary side.

If the equivalent primary-to-secondary winding turns ratio is R_t and the turns ratio between the primary and each individual secondary winding is T_r, the equivalent secondary volatge, V_s, when referred to the primary side, can then be given by:

$$V_{Pab} = V_s R_t = V_{s1}\frac{T_r}{\lambda_2} + V_{s2}\frac{T_r}{\lambda_2} + \cdots + V_{S\lambda_2}\frac{T_r}{\lambda_2} \tag{4.18}$$

Substituting (4.16) into (4.18), and with the transformer's leakage inductance L_k referred to the primary side, the primary referred equivalent circuit of the proposed converter converter can be expressed by (4.19) and schematically represented as in figure 4.4.

$$(L_{Parm} + L_k)\frac{dI_P}{dt} = E_{Pab} - V_s R_t \tag{4.19}$$

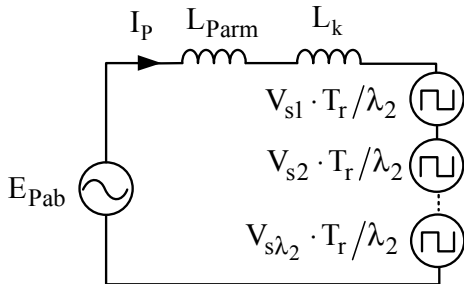


Figure 4.4 Equivalent circuit of the proposed converter referred to the primary side.

4.4 Output Power Characteristics

4.4.1 *The typical voltage waveform*

To simplify the analysis of the proposed converter, the following assumptions are made for the output voltage waveform of the MMC: 1) the SM capacitor voltages are well balanced and ripple-free; 2) the converter is operating with a unity modulation index; and 3) with a high number of SMs, the resulting output AC waveform is approximately sinusoidal. The well-known carrier-phase-shift pulse width modulation (CPS-PWM) technique is applied to control the MMC in this work. The principles of operation of CPS-PWM are described in Chapter 3 [111].

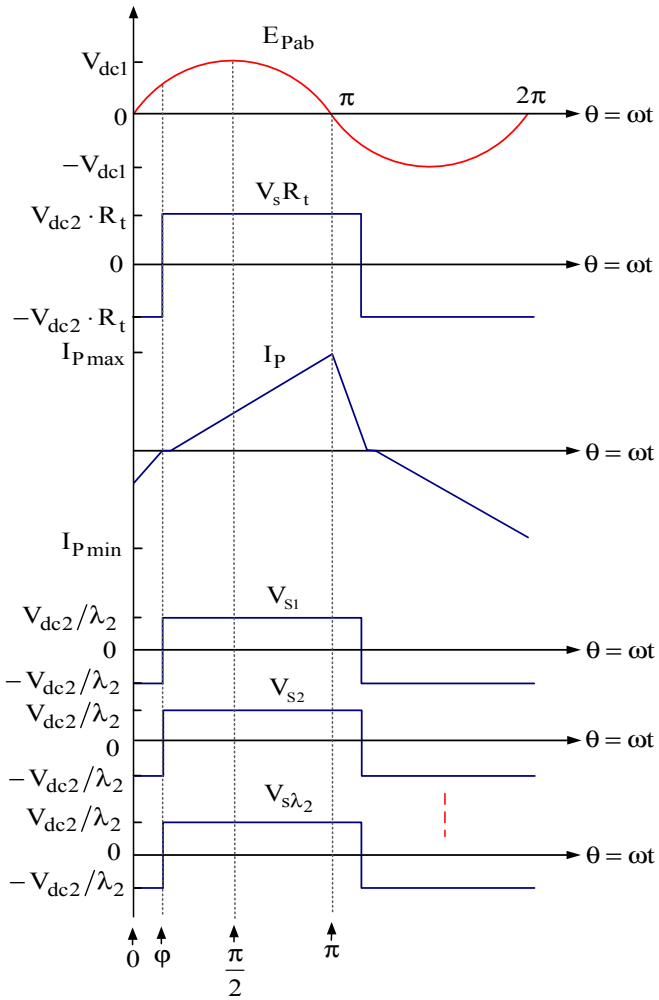


Figure 4.5 Primary equivalent AC voltage, E_{Pab}; equivalent secondary voltage referred to the primary side, $V_S R_t$; secondary AC voltages of each winding of transformer, $V_{S1}, V_{S2}, \ldots, V_{S\lambda_2}$.

Given the above assumptions, the ideal primary and referred secondary voltage waveforms of the proposed converter can be represented as shown in figure 4.5, where the power is transferred from V_{dc1} to V_{dc2} (in a unidirectional power flow). As discussed in Section 4.3, V_s is the equivalent secondary AC voltage, which is equal to $V_s = V_{s1} + V_{s2} + \cdots + V_{s\lambda_2}$, and φ is the phase shift angle by which the primary equivalent AC voltage, E_{Pab}, leads the secondary equivalent AC voltage, V_s.

4.4.2 *Derivation of output power*

Once again, the analysis below takes the following two assumptions into account: 1) the AC output waveform is symmetrical, and therefore only half of the cycle is considered for the output power derivation; 2) for simplicity, the peak values of E_{Pab} and V_s are equal to V_{dc1} and V_{dc2} respectively ignoring any voltage drop across the circuit components). From figure 4.5, the output power can be derived based on the following operating intervals:

Interval 1 *(*$0 \leq \theta < \varphi$*)*:

As can be noticed in figure 4.5, during this interval $V_s(\theta)$ is equal to $-V_{dc2}$ and its referred primary voltage is $-V_{dc2}R_t$. Therefore, $E_{Pab}(\theta)$ and $I_P(\theta)$ can be expressed as:

$$E_{Pab}(\theta) = V_{dc1}\sin(\theta) \tag{4.20}$$

$$I_P(\theta) = I_P(0) + \frac{1}{\omega L}\int_0^{\theta}[E_{ab}(\theta) - R_t V_s(\theta)]d\theta \tag{4.21}$$

where ω is the fundamental angular frequency of the system, and L is the equivalent inductance of the converter which is equal to $L = L_{arm} + L_k$.

Replacing $V_s(\theta)$ by $-V_{dc2}$ and substituting (4.20) into (4.21), yields:

$$I_P(\theta) = I_P(0) + \frac{1}{\omega L}\left[2V_{dc1}\sin(\frac{\theta}{2})^2 + R_t V_{dc2}\theta\right] \tag{4.22}$$

According to (4.22), when $\theta = \varphi$, one gets:

$$I_P(\varphi) = I_P(0) + \frac{1}{\omega L}(V_{dc1} - V_{dc1}\cos\varphi + V_{dc2}R_t\varphi) \tag{4.23}$$

According to (4.20) and (4.22), the output energy during this interval can be obtained by:

$$\mathrm{E}_1 = \int_0^{\varphi} V_s(\theta)\cdot I_P(\theta)d\theta = -\frac{{R_t}^2{V_{dc2}}^2\varphi^2}{2\omega L} - V_{dc2}R_t\varphi I_P(0) - \frac{R_t V_{dc1}V_{dc2}[\varphi - \sin(\theta)]}{\omega L} \tag{4.24}$$

Interval 2 *($\varphi \le \theta < \pi$)*:

During this interval, $V_s(\theta)$ is equal to V_{dc2} and $E_{Pab}(\theta)$ remains equal to $V_{dc1}\sin(\theta)$, and therefore $I_P(\theta)$ can be expressed as:

$$I_P(\theta) = I_P(\varphi) + \frac{1}{\omega L}\int_{\varphi}^{\theta}[E_{Pab}(\theta) - R_t V_s(\theta)]\, d\theta \tag{4.25}$$

Substituting $V_s(\theta) = V_{dc2}$, $E_{Pab}(\theta) = V_{dc1}\sin(\theta)$ and (23) into $I_P(\theta)$ with (4.25) yields:

$$I_P(\theta) = I_P(0) + \frac{1}{\omega L}[V_{dc1} - V_{dc1}\cos\varphi - R_t V_{dc2}\theta + 2R_t V_{dc2}\varphi] \tag{4.26}$$

From (4.26), at $\theta = \pi$, one can get:

$$I_P(\pi) = I_P(0) + \frac{1}{\omega L}[2V_{dc1} - \pi R_t V_{dc2} + 2R_t V_{dc2}] \tag{4.27}$$

Similarly, the output energy during this interval is given by:

$$\mathrm{E}_2 = \int_{\varphi}^{\pi} V_s(\theta)\cdot I_P(\theta)d\theta = -\frac{R_t V_{dc2}}{2\omega L}[(2V_{dc1}\varphi - 2\pi V_{dc1} - 2V_{dc1}\sin(\theta) + \pi^2 R_t V_{dc2} + 3R_t V_{dc2}\varphi^2 - 2\pi L I_P(0) + 2L\varphi I_P(0) - 4\pi R_t V_{dc2}\varphi)] \tag{4.28}$$

Therefore, from (4.24) and (4.28), the output power of the proposed converter can be calculated as:

$$P_{out} = \frac{E_1 + E_2}{\pi} \tag{4.29}$$

Owing to the half-cycle symmetry, $I_P(0) = -I_P(\pi)$ [118-119]. Therefore, according to (4.27), the intial current $I_P(0)$ can be calculated as:

$$I_P(0) = \frac{2V_{dc1} - \pi R_t V_{dc2} + 2R_t V_{dc2}\varphi}{2\omega L} \tag{4.30}$$

Substituting the (4.24), (4.28), and (4.30) into (4.29), the output power of the proposed converter at any phase shift angle, φ, can be expressed by:

$$P_{out}(\varphi) = \frac{2GV_{dc1}^2\sin(\varphi)}{\pi\omega L} \tag{4.31}$$

where $\mathrm{G} = \frac{V_{dc2}R_t}{V_{dc1}}$ and is defined as the primary-referred DC voltage gain, which is often known as the DC conversion ratio [118-119].

4.4.3 *Output power characteristics*

Similar to the case with the conventional single active bridge (SAB) DC/DC converter [112], the phase shift angle φ is defined as the point where the primary current, I_P, crosses zero, which means that $I_P(\varphi) = 0$. Using this relationship of $I_P(\varphi) = 0$ gives:

$$G = \frac{2\cos(\varphi)}{\pi} \tag{4.32}$$

Substituting (4.32) into (4.31), yields:

$$P_{out}(\varphi) = \frac{4V_{dc1}^2 \sin(\varphi)\cos(\varphi)}{\pi^2 \omega L} \qquad (0 \leq 0 \leq \pi) \tag{4.33}$$

It should be noted that (4.33) is derived based on the assumption of a unity modulation index, M_1= 1, which corresponds to the maximum power transfer capability of the proposed converter.

For simplicity, the output power is normalized to a base power of $P_{base} = \frac{4V_{dc1}^2}{\pi^2 \omega L}$, which results in:

$$P_{out}(\varphi) = M_1^2 \sin(\varphi)\cos(\varphi) \qquad (0 \leq 0 \leq \pi) \tag{4.34}$$

where the modulation index $M_1 \in [0,1]$ is introduced in order to derive the generalized equation of ouput power.

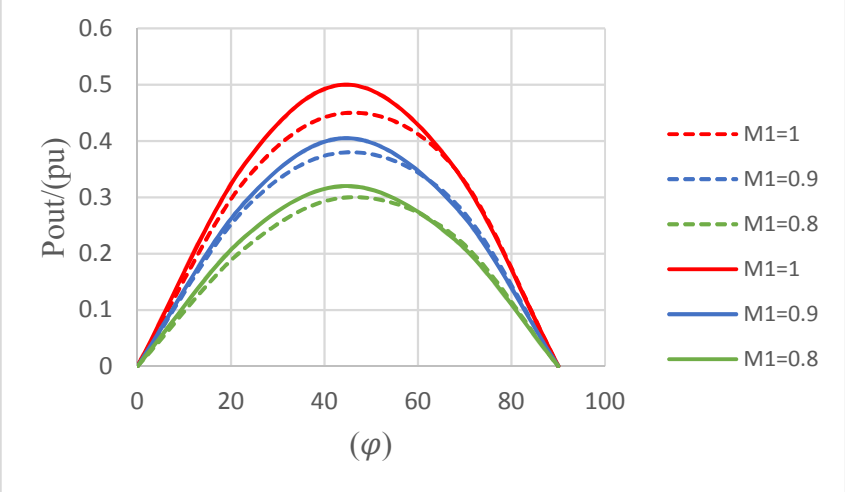


Figure 4.6 Normalized output power versus phase shift angle φ of the proposed converter with different values of modulation index (M_1); the solid line represents theoretical results and the dashed line represents simulation results.

Figure 4.6 illustrates the variation in normalized power of (4.34) to the phase shift angle φ, (and it should be noted that the solid line represents theoretical results and the dashed line represents simulation results based on the parameters shown in table 4.1. Furthermore, it is also clear from figure 4.6 that the power transfer capability of the proposed converter is influenced by the modualation index, M_1, and the phase shift angle, φ, where the highest power is achieved with a unity modulation index. In theory, the maximum output power occurs at the point at which $\frac{dP_{out}}{d\varphi} = 0$, for which $\varphi = \frac{\pi}{4}$. However, when taking into considersion the losses in the circuit and non-ideal sinusoidal primary AC voltage, the maximum output power point will deviate from $\varphi = \frac{\pi}{4}$ as shown in figure 4.6.

4.5 Control Strategy of the Proposed Converter

In this work, the primary single-phase MMC is operated as a controllable voltage source to produce an AC voltage with constant amplitude and frequency so as to control the output voltage and current of the cascaded diode bridge rectifiers (It is noting that the secondary DC side is loaded by a fixed resistor. Therefore, the control/setting of power is achieved by the primary voltage of the transformer).

Figure 4.7 shows the voltage control using the *dq* synchronous reference frame for the primary side single-phase MMC. Here I_P and V_{Pab} represent the primary AC current and voltage respectively, and $I_{P\alpha\beta}$ and $V_{P\alpha\beta}$ are the orthogonal pair of the primary AC current and voltage respectively, I_{Pdq} and V_{Pdq} are the transformed d-axis and q-axis components of the primary AC current and voltage respectively, and f_{AC} and L_{Parm} are the fundamental AC frequency and the arm inductance of the primary single-phase MMC respectively.

The control strategy presented in figure 4.7 transforms an orthogonal pair consisting of the actual primary AC voltage V_{Pab} (i.e. $V_{Pab} = V_{P\alpha}$) and the fictitious voltage $V_{P\beta}$ utilising the phase delay method from a stationary to a rotating reference frame. The component of the AC voltage in the *dq* frame then becomes a DC value, where a zero error voltage PI controller can

then

be used. In this control method, V_{Pd_ref} is set to the rated peak value of AC voltage, V_{Pq_ref} is set to zero and the fundamental AC frequency is set to f_{AC}. MMC SM voltages were also regulated and balanced using the control method presented in Chapter 3, which is based on a simple PI controller [115]. The *dq* transformation matrix from a stationary to rotating reference frame is given as:

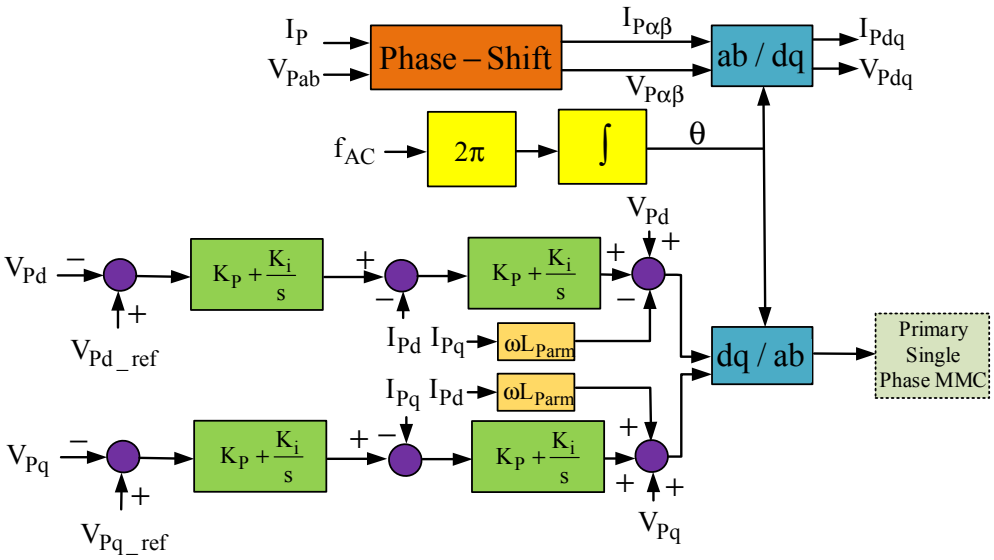


Figure 4.7 Schematic diagram of the proposed control strategy based on the d-q rotating reference frame.

$$C_{2s/2r} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} V_{Pd} \\ V_{Pq} \end{bmatrix} \tag{4.35}$$

According to the analysis in Section 4.3, the mathematical model of the primary single-phase MMC of the proposed converter can be expressed by:

$$L_{Parm}\frac{dI_P}{dt} = E_{Pab} - V_{Pab} \tag{4.36}$$

where E_{Pab} is the equivalent primary voltage of the transformer.

Applying the transformation matrix of (4.35) into the (4.36) yields:

$$\begin{cases} L_{Parm}\dfrac{dI_{Pd}}{dt} - \omega L_{Parm} I_{Pq} = E_{Pd} - V_{Pd} \\ L_{Parm}\dfrac{dI_{Pq}}{dt} + \omega L_{Parm} I_{Pd} = E_{Pq} - V_{Pq} \end{cases} \tag{4.37}$$

Vector control can be divided into control over the inner and outer loops. The outer loop is used

to produce the reference I_{Pd_ref} and I_{Pq_ref}, which are utilized by the inner loop to regulate the control waveform. According to figure 4.7 and equation (4.37), the control waveform based on the *dq* synchronous reference frame can be expressed as:

$$\begin{cases} E_{Pd} = \left(K_p + \frac{K_i}{s}\right)\left(I_{Pd\_ref} - I_{Pd}\right) + V_{Pd} - \omega L_{Parm} I_{Pq} \\ E_{Pq} = \left(K_p + \frac{K_i}{s}\right)\left(I_{Pq\_ref} - I_{Pq}\right) + V_{Pq} + \omega L_{Parm} I_{Pd} \end{cases} \tag{4.38}$$

where k_p and k_i are the proportional and integral constant of the PI controller respectively.

4.6 Simulation Results

A simulation model of the proposed converter rated at 10 MW/140kV was developed with the parameters tabulated in table 4.1 using MATLAB/SIMULINK to validate the feasibility and effectiveness of the proposed system and its control system. According to reference [118], 10MW wind turbines will be the next longer-term target to be conquered according to the technology trends, and 150 kV is a typical voltage for the HVDC transmission lines [118]. Therefore, a 10MW and 150 kV were respectively selected as the rated power and output DC voltage for the proposed converter. Moreover, the parameters of the other components such as SM capacitors and arm inductors can be evaluated according to the power component selection methods shown in Chapter 8, which have been detailed introduced, analyzed and calculated. Therefore, no further details are presented at here. It is worth noting that 400Hz is selected as the fundamental AC frequency of all these four topologies, which is chosen to give a trade-off between switching losses and the size of the system [117]. If the converters operate at a low frequency such as 50Hz, the power density of the whole system will be substantially reduced due to the need for low-frequency transformers and corresponding heat dissipation systems. This would seriously influence the large-scale engineering application of the topologies, especially for an offshore platform with limited space.

In this model, the single-phase MMC at the primary side was constructed using fourteen half-bridge SMs per arm, and there were fourteen series-connected diode-bridge rectifier modules at the secondary side of the medium frequency transformer. Furthermore, a medium-frequency transformer with turn ratios of $W_P : W_{S1} : W_{S2} : \cdots : W_{S14} = 1:1:1:\cdots:1$ was chosen, where W_P

and W_{S1} to W_{S14} are the primary winding and the corresponding secondary winding-one to winding-fourteen respectively.

Table 4.1 Simulation parameters

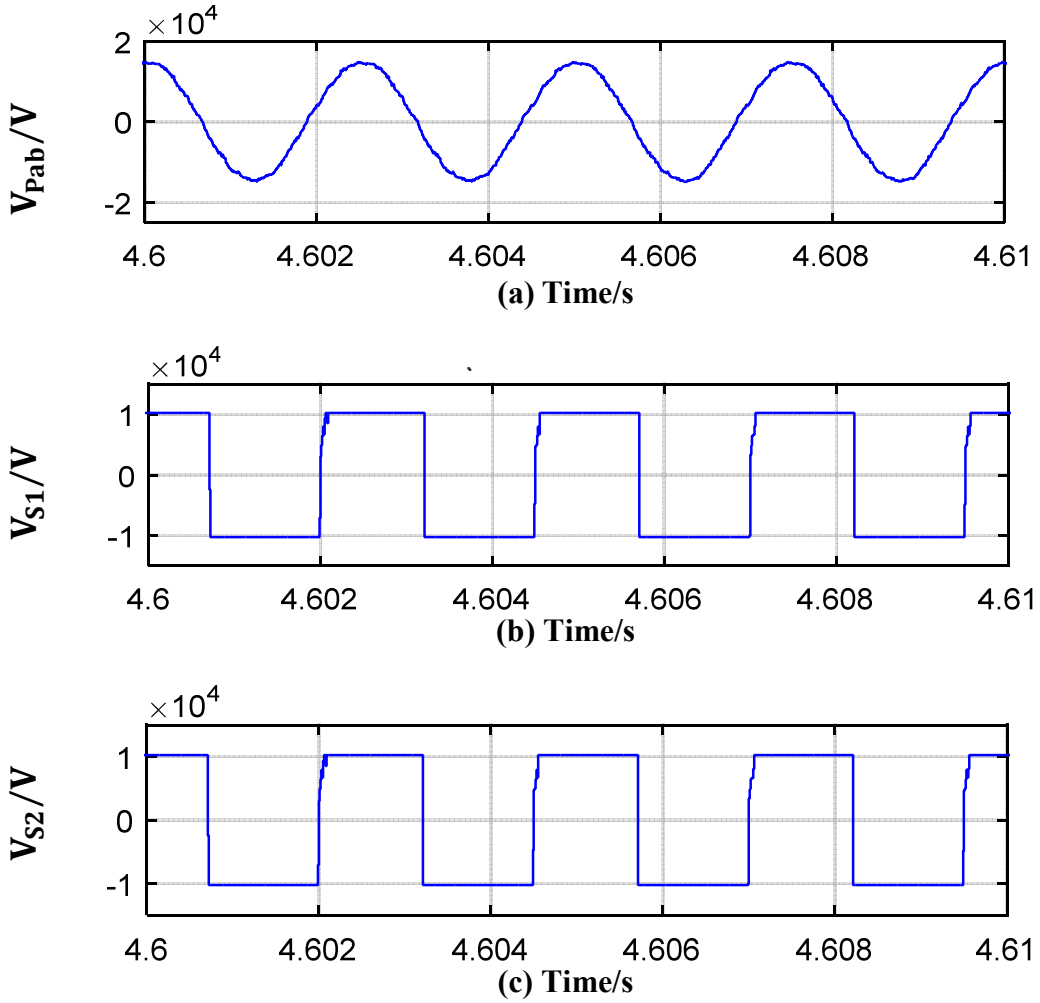
PARAMETER	Value
Rated power	10MW
Input DC voltage	15kV
Output DC voltage	140kV
Output load resistor	2kΩ
Number of MMC's SM per arm	14
Number of diode-bridge rectifier modules	14
Transformer ratio	1:14
SM capacitor of MMC	3.6mF
Arm Inductor	1mH
Output capacitor	3mF
Output inductor	0.33mH
Switching frequency	2kHz
AC fundamental frequency	400Hz

Figure 4.8 and 4.9 show the steady-state performance of the proposed converter. The 400Hz AC voltages at the primary and secondary sides of the transformer are shown in figure 4.8, and the corresponding currents at the primary and secondary sides of the transformer are depicted in figure 4.9. It is worth noting that the peak of the secondary currents is just about one-fourteenth of that of the primary one, which effectively reduces the current rating of the associated diode-bridge-rectifier modules. It can be further reduced if more windings on the secondary side are considered. Because the fourteen diode bridge rectifier modules employed at the secondary side have similar AC voltages and currents, therefore just four of the fourteen diode bridge rectifier modules are taken as examples to show their waveforms.

The performance of voltage balance control is demonstrated in figure 4.10, where it can be observed that the capacitor voltages are perfectly controlled and are close to one-fourteenth of the input DC voltage 15kV/14. It is worth noting that, when the switch turned on, SM capacitor turned into charging mode immediately, which is the reason why there is an initial transient fluctuation in figure 4.10. In an actual engineering application, a pre-charging system can be employed to charge the SM capacitor before turning on the converter which can effectively limit initial transient fluctuation. The output DC voltage of the proposed converter is shown in

figure 4.11 and, with the given transformer turns ratio in this study, the average output DC voltage is maintained at around 140kV.

The performance of the proposed control strategy was further investigated and confirmed with a 50% step change of the output power. Figure 4.12 shows the dynamic response of the proposed controller when the load changes at $t = 2.5s$, causing the output current I_{dc2} and power P_{dc2} to rapidly decrease, while the transformer primary AC voltage and output DC voltage of the proposed converter are maintained at constant levels, which confirms the effectiveness of the proposed control system.



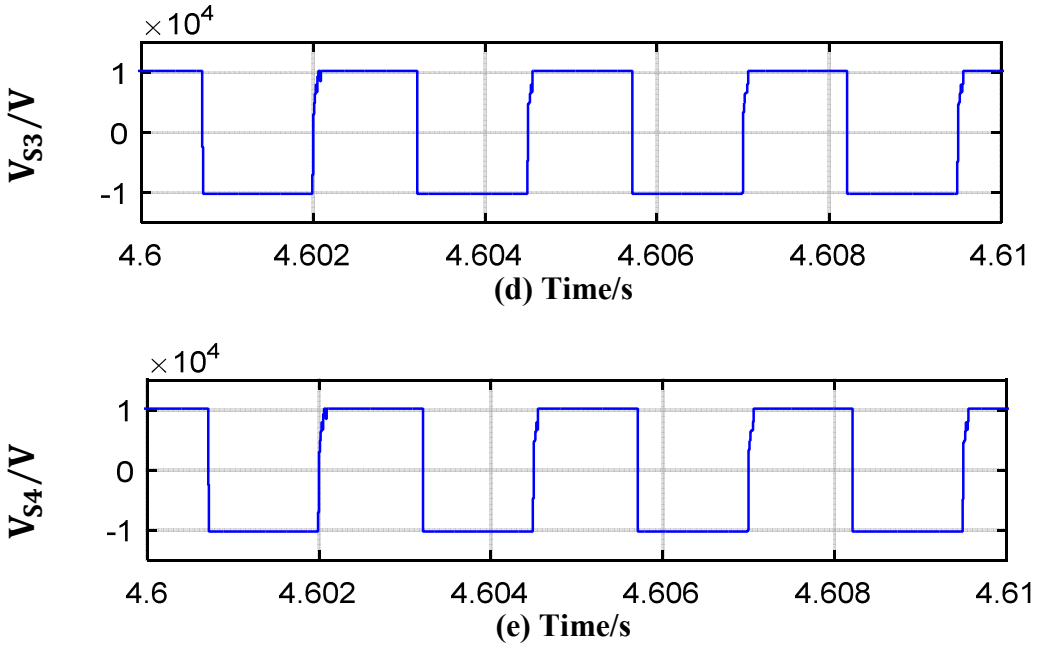
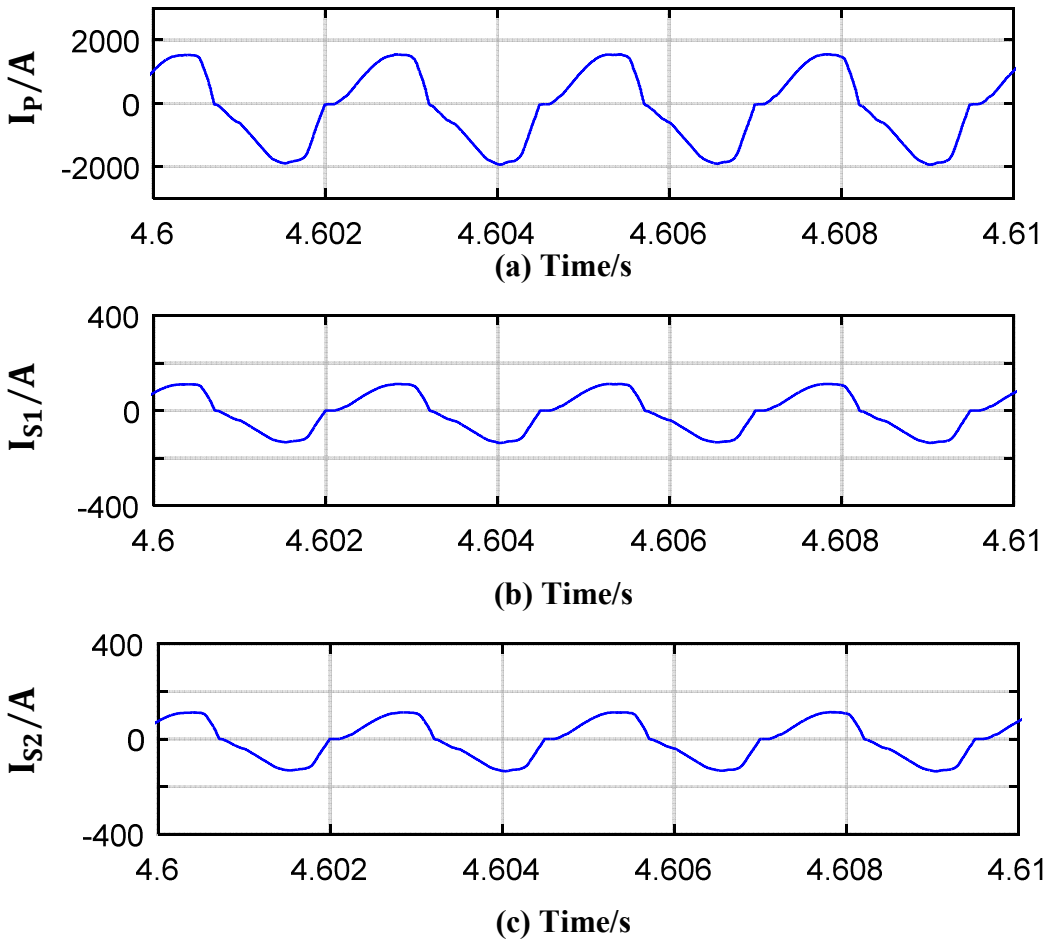


Figure 4.8 Transformer voltage waveforms: (a) primary terminal voltage V_{Pab}; (b) secondary winding-one voltage V_{S1}; (c) secondary winding-two voltage V_{S2}; (d) secondary winding-three voltage V_{S3}; (e) secondary winding-four voltage V_{S4}.



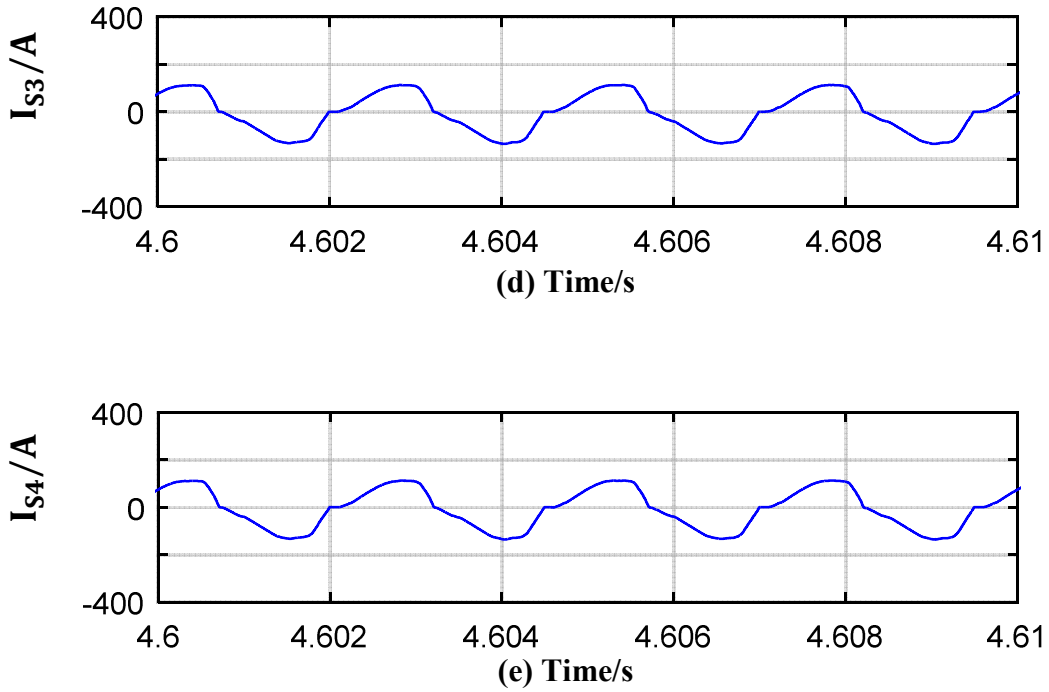


Figure 4.9 Transformer current waveforms: (a) primary current I_P; (b) secondary winding-one current I_{S1}; (c) secondary winding-two current I_{S2}; (d) secondary winding-three current I_{S3}; (e) secondary winding-four current I_{S4}.

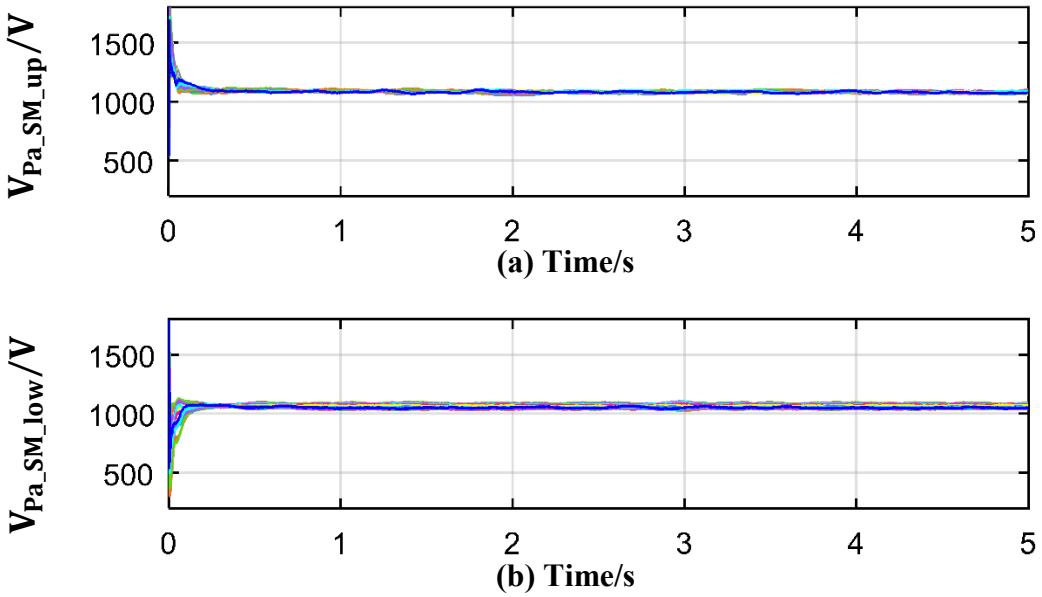


Figure 4.10 Upper and lower SM voltages.

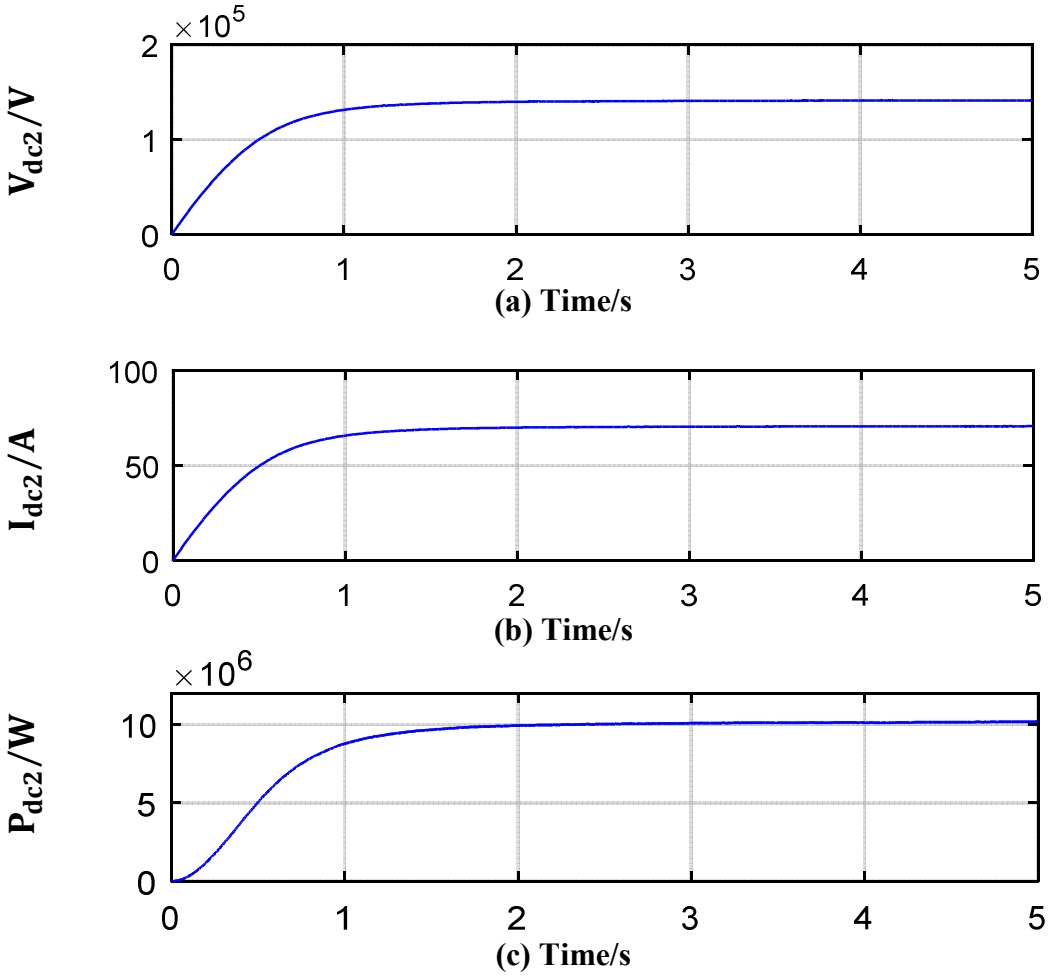
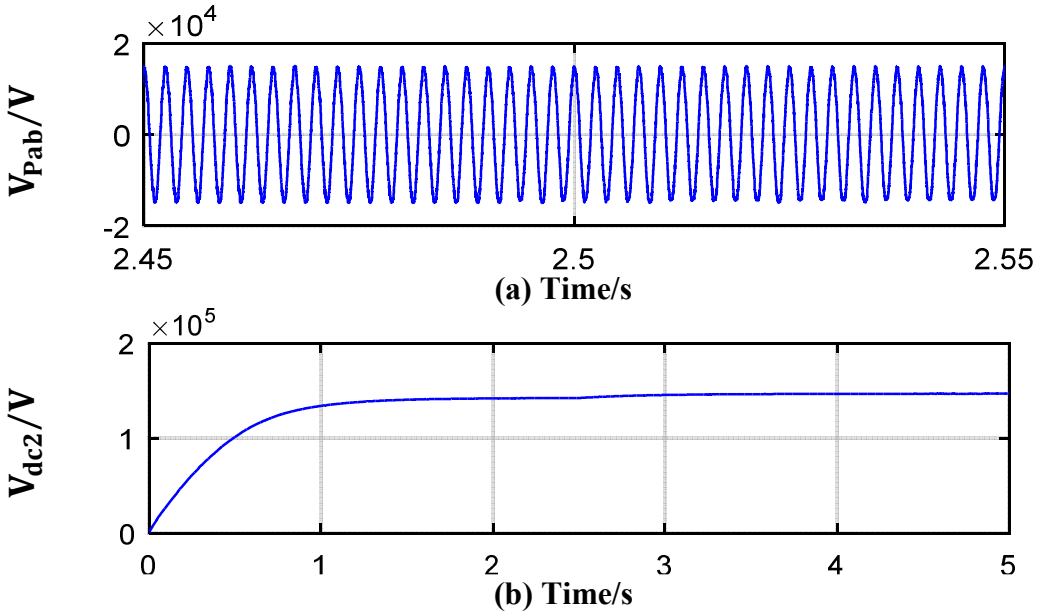


Figure 4.11 Output waveforms of the proposed converter under steady-state operation: (a) output DC voltage; (b) output DC current; (c) output power.



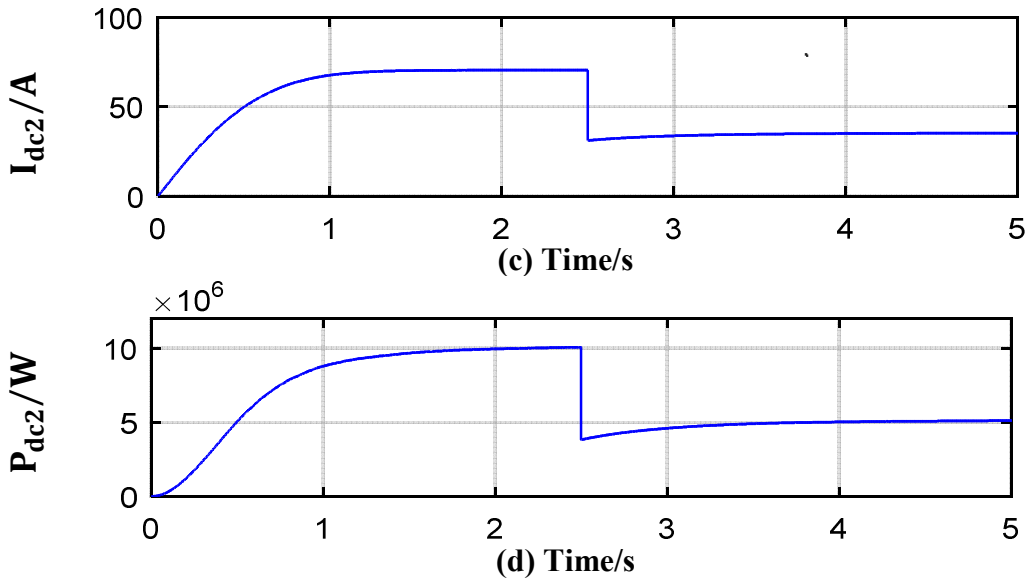


Figure 4.12 Output waveforms of the proposed converter under a 50% step change at 2.5s: (a) transformer primary terminal voltage waveform; (b) output DC voltage, (c) output DC current; (d) output power.

4.7 Summary

Chapter 3 has proposed a unidirectional single-phase modular DC/DC converter. To understand the operating characteristics of the proposed converter, a detailed theoretical design analysis is presented and discussed thoroughly. This includes a description of the circuit configuration, derivation of the mathematical model and an analysis of the output power characteristics. Moreover, a control method based on the rotating reference frame is developed for the proposed converter. Finally, simulation results are also presented.

Chapter 5. Unidirectional Three-Phase DC/DC Modular Multilevel Converter

5.1 Introduction

This chapter builds on the previous chapter and extends the converter to a three-phase version. The proposed converter consists of a wind farm-side three-phase modular multilevel converter (MMC) and a series-connected rectifier module linked by a special decoupled medium frequency transformer. The transformer decouples the three-phase input voltage into three individual isolated single–phase voltages with 120-degree displacement. As the intended application requires only a unidirectional power flow, this enables the use of simple diode bridge rectifier modules at the output side. The modular structure of the proposed system also reduces the voltage and current stresses of the semiconductor power devices. It is worth noting that the modularity and expandability of the proposed topology enable it to be used as a power electronics transformer for different voltage levels if required. Similarly, the system is managed through the control of the primary side converter only, without any feedback from the output DC side.

5.2 Configuration of the Proposed Converter

As can be seen from figure 5.1, the proposed converter utilizes an MMC at the primary side of the special decoupled medium-frequency transformer. The secondary output voltages are decoupled into three identical, but 120-degree phase-shifted voltages. The primary three phases of this transformer are connected in a star configuration, and the secondary windings of each phase are further split into multiple windings (which would theoretically be any number, but two windings are used here) to maximize the output voltage. It is noting that such a three-phase decoupled transformer can be built by the three single-phase transformers of which primary

side are connected in star and secondary side of each transformer are divided into multiple windings. To more clearly describe transformer configuration, an example of a three-phase decoupled transformer which is built by the three single-phase transformers is shown in figure 5.1c. The use of the three-phase MMC as an inverter at the primary side takes full advantage of its characteristics including modular design, scalability, and high-quality output waveform with low harmonic distortion. Meanwhile, in the applied combined rectifier at the secondary side, it is easy to stack the necessary number of submodules (SMs), and therefore it is suitable for applications with different voltage levels.

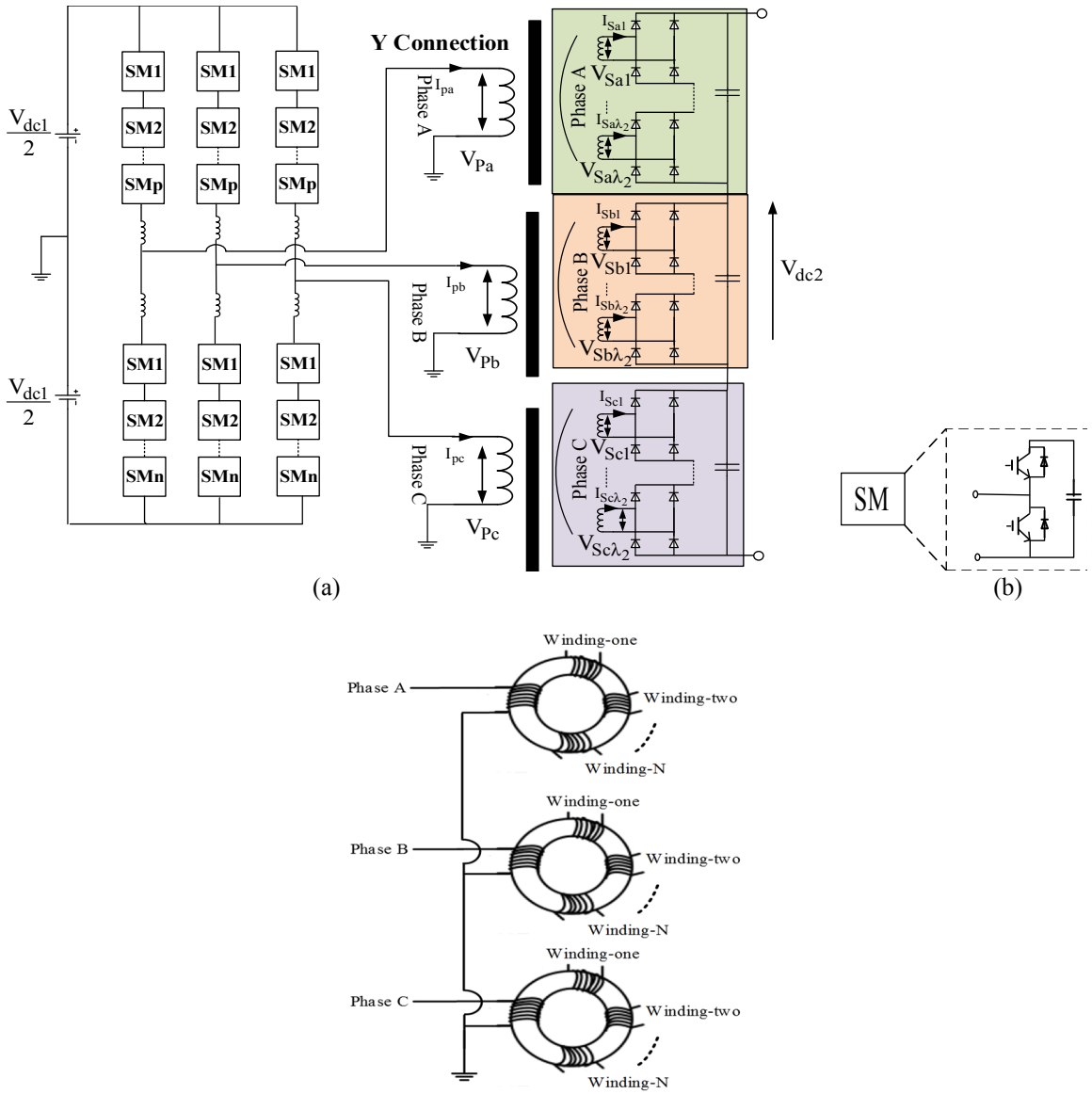


Figure 5.1 Configuration of (a) the proposed DC/DC converter, (b) half-bridge based SM at the primary side of the proposed converter, and (c) three single-transformers based three-phase decoupled transformer.

5.3 Mathematical Model

***For the primary side*:** Figure 5.2 shows the equivalent circuit of Phase-a of the MMC, where V_{dc1} and I_{dc1} are the converter's input DC voltage and current respectively, V_{aU} and V_{aL} are the voltages of the upper and lower arms of Phase-a respectively, I_{aU} and I_{aL} are the currents of the upper and lower arms of Phase-a respectively, E_{Pa} is the equivalent output phase voltage as shown in figure 5.2(b), V_{Pa} is the output AC voltage, and I_{cir} and I_{Pa} are the circulating and ouput AC currents respectively.

$$I_{aU} = I_{Pa}/2 + I_{cir} \tag{5.1}$$

$$I_{aL} = -I_{Pa}/2 + I_{cir} \tag{5.2}$$

where the circulating current, I_{cir}, is flowing through both the upper and lower arms.

It should be noted that the circulating current has no effect on the output phase current and is given by:

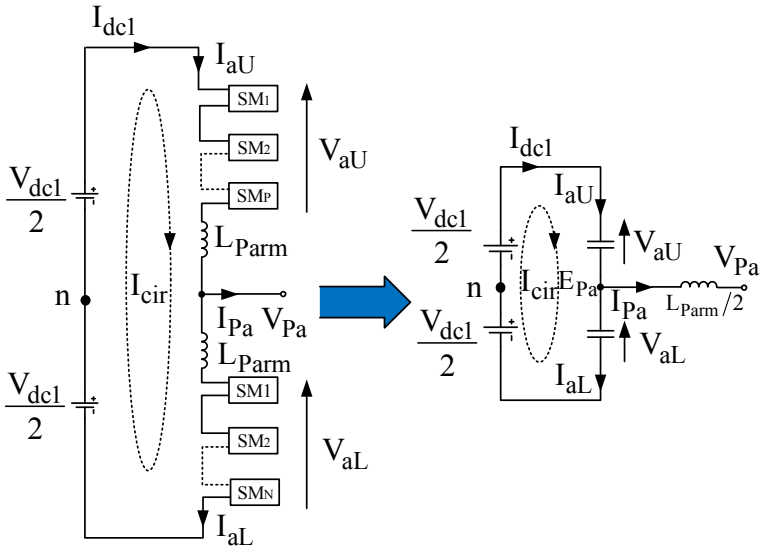


Figure 5.2 Phase-a: (a) schematic diagram; (b) equivalent circuit.

$$I_{cir} = (I_{aU} + I_{aL})/2 \tag{5.3}$$

Concerning (5.1) and (5.2), the AC output current, I_{Pa}, can be expressed in terms of the upper and lower arm currents as:

$$I_{Pa} = I_{aU} - I_{aL} \tag{5.4}$$

Letting *n* be the neutral point and applying the Kirchhoff voltage law (KVL) for Phase-a, as shown in figure 5.3(a), one can determine the upper and lower voltages as:

$$V_{aU} = \frac{V_{dc1}}{2} - V_{Pa} - L_{Parm}\frac{dI_{aU}}{dt} \tag{5.5}$$

$$V_{aL} = \frac{V_{dc1}}{2} + V_{Pa} - L_{Parm}\frac{dI_{aL}}{dt} \tag{5.6}$$

The output voltage V_{Pa} can be expressed by combining (5.5) and (5.6) as follows:

$$V_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) - \frac{1}{2}L_{Parm}\frac{d(I_{aL}-I_{aU})}{dt} \tag{5.7}$$

By substituting (5.4) into (5.7), the equivalent output phase voltage E_{Pa} can be given as:

$$E_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) = V_{Pa} + \frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} \tag{5.8}$$

Therefore, the mathematical model of Phase-a can be derived by rearranging (5.8) as:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} = E_{Pa} - V_{Pa} \tag{5.9}$$

According to (5.9), the equivalent circuit of Phase-a can be represented as in figure 5.3 (b).

Similarly, the mathematical model of Phases b and c of the MMC inverter at the primary side are given by:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pb}}{dt} = E_{Pb} - V_{Pb} \tag{5.10}$$

$$\frac{1}{2}L_{Parm}\frac{dI_{Pc}}{dt} = E_{Pc} - V_{Pc} \tag{5.11}$$

where E_{Pb} and E_{Pc} are the equivalent output voltages of Phase-b and Phase-c respectively, whereas V_{Pb} and V_{Pc} are the AC output voltages of Phase-b and Phase-c respectively, and I_{Pb} and I_{Pc} are the AC ouptut currents of Phase-b and Phase-c respectively. Furthermore, it should be noted that each phase has exactly the same inductance, as denoted by L_{Parm}.

***For the secondary side*:** From figure 5.1, individual diode bridge rectifier modules are cascaded at the secondary side of the transformer, and can be regarded as a series connection of voltage sources ($V_{Sa1}, V_{Sa2}, \dots, V_{Sa\lambda_2}$ for Phase-a; $V_{Sb1}, V_{Sb2}, \dots, V_{Sb\lambda_2}$ for Phase-b; and $V_{Sc1}, V_{Sc2}, \dots, V_{Sc\lambda_2}$ for Phase-c). Therefore, the total equivalent voltages of each phase at the secondary side of the transformer, V_{sa}, V_{sb}, and V_{sc}, are given by:

$$V_{Sa} = V_{Sa1} + V_{Sa2} + \cdots + V_{Sa\lambda_2} \tag{5.12}$$

$$V_{Sb} = V_{Sb1} + V_{Sb2} + \cdots + V_{Sb\lambda_2} \tag{5.13}$$

$$V_{Sc} = V_{Sc1} + V_{Sc2} + \cdots + V_{Sc\lambda_2} \tag{5.14}$$

where λ_2 is the number of diode bridge rectifier modules in each decoupled phase at the

secondary side of the transformer.

If the equivalent primary-to-secondary winding turns ratio of each of Phases a, b, and c is R_t and the turns ratio of primary to each individual secondary winding within each phase is T_r, then the equivalent secondary voltages V_{Sa}, V_{Sb} and V_{Sc} when referred to the primary side can then be given by:

$$V_{Pa} = V_{Sa}R_t = V_{Sa1}\frac{T_r}{\lambda_2} + V_{Sa2}\frac{T_r}{\lambda_2} + \cdots + V_{Sa\lambda_2}\frac{T_r}{\lambda_2} \tag{5.15}$$

$$V_{Pb} = V_{Sb}R_t = V_{Sb1}\frac{T_r}{\lambda_2} + V_{Sb2}\frac{T_r}{\lambda_2} + \cdots + V_{Sb\lambda_2}\frac{T_r}{\lambda_2} \tag{5.16}$$

$$V_{Pc} = V_{Sc}R_t = V_{Sc1}\frac{T_r}{\lambda_2} + V_{Sc2}\frac{T_r}{\lambda_2} + \cdots + V_{Sc\lambda_2}\frac{T_r}{\lambda_2} \tag{5.17}$$

Substituting (5.15), (5.16) and (5.17) into (5.9), (5.10) and (5.11) respectively, and with the transformer's leakage inductance L_k of each phase referred to the primary side, the primary referred equivalent circuit of the proposed converter can be expressed by (5.18) and is schematically illustrated in figure 5.3.

$$\begin{cases} (\frac{L_{Parm}}{2} + L_k)\frac{dI_{Pa}}{dt} = E_{Pa} - V_{Sa}R_t \\ (\frac{L_{Parm}}{2} + L_k)\frac{dI_{Pb}}{dt} = E_{Pb} - V_{Sb}R_t \\ (\frac{L_{Parm}}{2} + L_k)\frac{dI_{Pc}}{dt} = E_{Pc} - V_{Sc}R_t \end{cases} \tag{5.18}$$

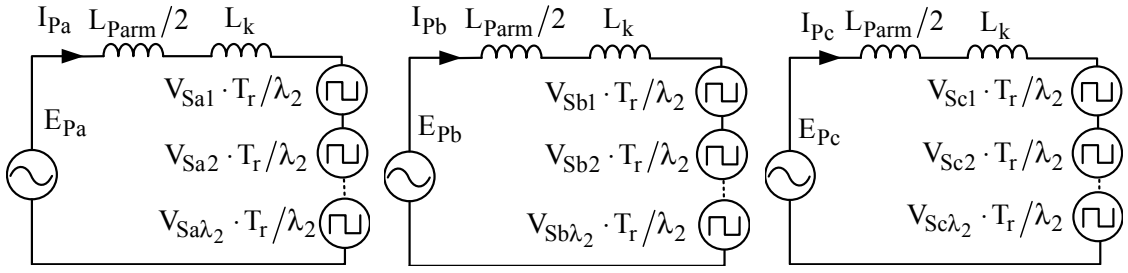


Figure 5.3 Equivalent circuit of the proposed converter referred to the primary side.

5.4 Output Power Characteristics

5.4.1 *Typical voltage waveforms*

To simplify the analysis and facilitate easy understanding, the following assumptions are made for the output voltage waveform of the MMC: 1) the SM capacitor voltages are well-balanced and ripple-free; 2) the converter operates with a unity modulation index; and 3) the

high number of SMs results in an approximately sinusoidal output AC waveform. It is worth noting also that, in this work, the well-known carrier-phase-shift pulse width modulation (CPS-PWM) technique is applied. A detailed analysis and the principles of operation of CPS-PWM have been well documented and are readily available in Chapter 3 [111], and therefore no further details are presented in this chapter.

Given the assumptions described above, the ideal primary and secondary referred voltage waveforms of the three phases of the proposed converter can be obtained as shown in figure 5.4, where power is transferred from the high voltage side to the low voltage side in unidirectional power flow. Taking Phase-a as an example, as mentioned earlier, V_{sa} is the equivalent Phase-a voltage at the secondary side which is equal to $V_{Sa} = V_{Sa1} + V_{Sa2} + \cdots + V_{Sa\lambda_2}$, and φ is the phase shift angle by which the primary equivalent Phase-a voltage, E_{Pa}, leads the equivalent Phase-a voltage of the secondary side, $V_{Sa} \cdot R_t$.

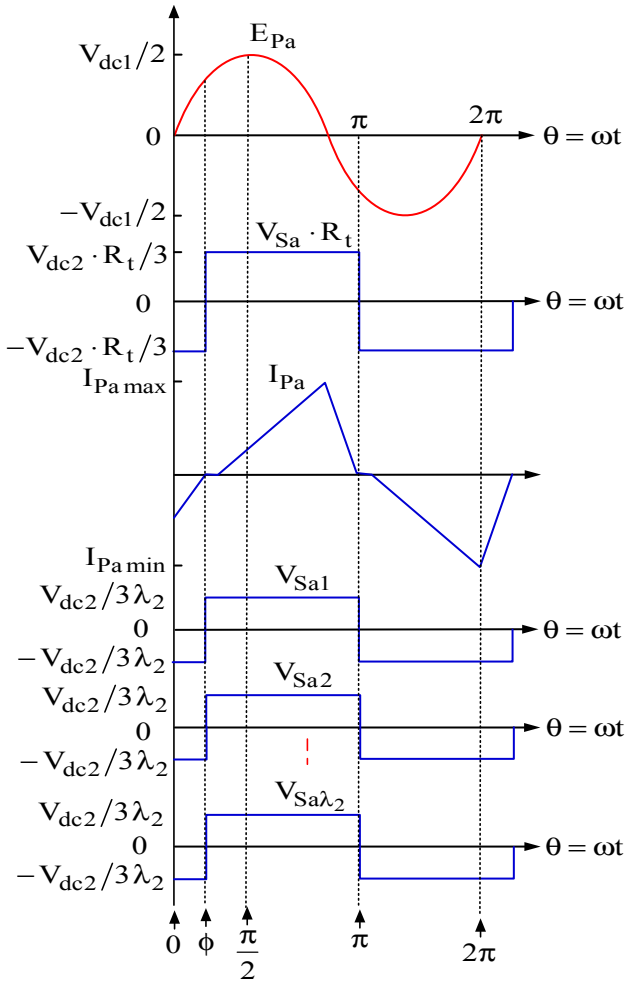


Figure 5.4 Phase-a: primary equivalent AC voltage, E_{Pa}; equivalent secondary volatge refer to the primary side, $V_{Sa}R_t$; secondary AC voltages of each winding of transformer, $V_{Sa1}, V_{Sa2}, \ldots, V_{Sa\lambda_2}$.

5.4.2 *Derivation of the output power*

It should be noted that in the following analysis the following assumptions are made: 1) owing to the waveform symmetry, only a half-cycle of the AC waveform is considered for the output power derivation; and 2) for simplicity, the peak value of the primary equivalent AC voltage of Phase-a, E_{Pa}, is equal to $\frac{V_{dc1}}{2}$ (ignoring any voltage drop across the circuit components).

According to figure 5.1, the decoupled three Phases a, b, and c at the secondary side of the transformer are connected in series, and each will withstand one-third of the output voltage, $\frac{V_{dc2}}{3}$. Therefore, the peak value of the secondary equivalent AC voltage of Phase-a, $\hat{V}_{Sa}$, is equal to $\hat{V}_{Sa} = \frac{V_{dc2}}{3}$. From figure 5.4, the output power can be derived as follows.

Interval 1 *(*$0 \leq \theta < \varphi$*)*:

As can be noticed in figure 5.4, during this interval, $V_{Sa}(\theta)$ is equal to $-\frac{V_{dc2}}{3}$, and its primary refered voltage is $-\frac{V_{dc2}}{3}R_t$. Therefore, $E_{Pa}(\theta)$ and $I_{Pa}(\theta)$ can be written as:

$$E_{Pa}(\theta) = \frac{V_{dc1}}{2}\sin(\theta) \tag{5.19}$$

$$I_{Pa}(\theta) = I_{Pa}(0) + \frac{1}{\omega L}\int_0^{\theta}[E_{Pa}(\theta) - R_t V_{Sa}(\theta)]d\theta \tag{5.20}$$

where ω is the fundamental angular frequency of the system, and L is the equivalent inductance of the converter which is equal to $L = \frac{L_{Parm}}{2} + L_k$.

Replacing $V_{Sa}(\theta)$ by $-\frac{V_{dc2}}{3}$ and substituting (5.19) into (5.20), yields:

$$I_{Pa}(\theta) = I_{Pa}(0) + \frac{1}{\omega L}\left[V_{dc1}\sin(\frac{\theta}{2})^{2} + \frac{V_{dc2}}{3}R_t\theta\right] \tag{5.21}$$

According to (5.21), when $\theta = \varphi$, one gets:

$$I_{Pa}(\varphi) = I_{Pa}(0) + \frac{1}{\omega L}\left(\frac{V_{dc1}}{2} - \frac{V_{dc1}}{2}\cos\varphi + \frac{V_{dc2}}{3}R_t\varphi\right) \tag{5.22}$$

According to $V_{Sa}(\theta) = -\frac{V_{dc2}}{3}$ and (5.21), the output energy during this interval can be obtained by:

$$\mathrm{E}_1 = \int_0^{\varphi} V_{Sa}(\theta)\cdot I_{Pa}(\theta)d\theta = -\frac{{R_t}^2{V_{dc2}}^2\varphi^2}{18\omega L} - \frac{V_{dc2}}{3}R_t\varphi I_{Pa}(0) - \frac{R_t V_{dc1}V_{dc2}[\varphi - \sin(\theta)]}{6\omega L} \tag{5.23}$$

Interval 2 *($\varphi \le \theta < \pi$)*:

During this interval, $V_{Sa}(\theta)$ is equal to $\frac{V_{dc2}}{3}$ and $E_{Pa}(\theta)$ remains equal to $\frac{V_{dc1}}{2}\sin(\theta)$; therefore, $I_{Pa}(\theta)$ can be expressed as:

$$I_{Pa}(\theta) = I_{Pa}(\varphi) + \frac{1}{\omega L}\int_{\varphi}^{\theta}[E_{Pa}(\theta) - R_t V_{Sa}(\theta)]\, d\theta \tag{5.24}$$

Substituting $V_{Sa}(\theta) = \frac{V_{dc2}}{3}$, $E_{Pa}(\theta) = \frac{V_{dc1}}{2}\sin(\theta)$ and (5.22) into $I_{Pa}(\theta)$ with (5.24) yields:

$$I_{Pa}(\theta) = I_{Pa}(0) + \frac{1}{\omega L}\left[\frac{V_{dc1}}{2} - \frac{V_{dc1}}{2}\cos\varphi - \frac{V_{dc2}}{3}R_t\theta + \frac{2V_{dc2}}{3}R_t\varphi\right] \tag{5.25}$$

From (5.25), at $\theta = \pi$, one gets:

$$I_{Pa}(\pi) = I_{Pa}(0) + \frac{1}{\omega L}\left[V_{dc1} - \frac{V_{dc2}}{3}\pi R_t + \frac{2V_{dc2}}{3}R_t\right] \tag{5.26}$$

Similarly, the output energy during this interval is given by:

$$\mathrm{E}_2 = \int_{\varphi}^{\pi} V_{Sa}(\theta)\cdot I_{Sa}(\theta)d\theta = -\frac{R_t V_{dc2}}{18\omega L}[3V_{dc1}\varphi - 3\pi V_{dc1} - 3V_{dc1}\sin(\theta) + \pi^2 R_t V_{dc2} + 3R_t V_{dc2}\varphi^2 - 6\pi L I_{Pa}(0) + 6L\varphi I_{Pa}(0) - 4V_{dc2}\pi R_t\varphi] \tag{5.27}$$

Therefore, from (5.23) and (5.27), the output power of Phase-a of the proposed converter can be calculated from:

$$P_{out\_a} = \frac{E_1 + E_2}{\pi} \tag{5.28}$$

Owing to the half-cycle symmetry, $I_{Pa}(0) = -I_{Pa}(\pi)$ [118-119]. Therefore, according to (5.26), the intial current $I_{Pa}(0)$ can be calculated by:

$$I_{Pa}(0) = \frac{3V_{dc1} - \pi R_t V_{dc2} + 2R_t V_{dc2}\varphi}{6\omega L} \tag{5.29}$$

Substituting the (5.23), (5.27), and (5.29) into (5.28), the output power of Phase-a of the proposed converter for any phase shift angle, φ, is given by:

$$P_{out\_a}(\varphi) = \frac{GV_{dc1}^2\sin(\varphi)}{3\pi\omega L} \tag{5.30}$$

where *G* is defined as the primary-referred DC voltage gain of the proposed converter, which is equal to $\mathrm{G} = \frac{V_{dc2}R_t}{V_{dc1}}$ and is often known as the DC conversion ratio [119].

5.4.3 *Output power characteristics*

Similar to the case in a conventional single active bridge (SAB) DC/DC converter [119], the phase shift angle φ is the angle where the primary current, I_{Pa} crosses zero, which means that $I_{Pa}(\varphi) = 0$. Using this relationship, one gets:

$$G = \frac{3\cos(\varphi)}{\pi} \tag{5.31}$$

Substituting (5.31) into (5.30) yields:

$$P_{out\_a}(\varphi) = \frac{V_{dc1}^2 \sin(\varphi)\cos(\varphi)}{\pi^2 \omega L} \tag{5.32}$$

It should be noted that (5.32) is derived based on the assumption that the modulation index M_1= 1, which corresponds to the maximum power transfer capability of the proposed converter.

For simplicity, the output power is normalized to a base power of $P_{base} = \frac{3V_{dc1}^2}{\pi^2 \omega L}$, which results in:

$$P_{out\_a}(\varphi) = \frac{1}{3} M_1^2 \sin(\varphi)\cos(\varphi) \quad (0 \le 0 \le \pi) \tag{5.33}$$

where a modulation index $M_1 \in [0,1]$ is introduced in order to derive the generalized equation of the ouput power.

Similarly, the output power of Phase-b and Phase-c can also be obtained in the same manner:

$$P_{out\_b}(\varphi) = \frac{1}{3} M_1^2 \sin(\varphi)\cos(\varphi) \quad (0 \le 0 \le \pi) \tag{5.34}$$

$$P_{out\_c}(\varphi) = \frac{1}{3} M_1^2 \sin(\varphi)\cos(\varphi) \quad (0 \le 0 \le \pi) \tag{5.35}$$

Therefore, the total output power can be calculated as:

$$P_{out\_Total}(\varphi) = P_{out\_a}(\varphi) + P_{out\_b}(\varphi) + P_{out\_c}(\varphi) = M_1^2 \sin(\varphi)\cos(\varphi) \ (0 \le 0 \le \pi) \tag{5.36}$$

Figure 5.5 illustrates the variation in the normalized power of (5.36) concerning the phase shift angle φ (where the solid line represents theoretical results and the dashed line represents simulation results based on the parameters listed in table 5.1). Furthermore, figure 5.5 clearly indicates that the power transfer capability of the proposed converter is influenced by the modulation index, M_1, and the phase shift angle, φ, where the highest power is achieved with a unity modulation index. In theory, the maximum output power occurs at the point of which

$\frac{dP_{out\_norm}}{d\varphi} = 0$, for which $\varphi = \frac{\pi}{4}$. However, when taking losses in the circuit and the non-ideal sinusoidal primary AC voltage into considersion, the maximum output power point will slightly deviate from $\varphi = \frac{\pi}{4}$, as shown in figure 5.5.

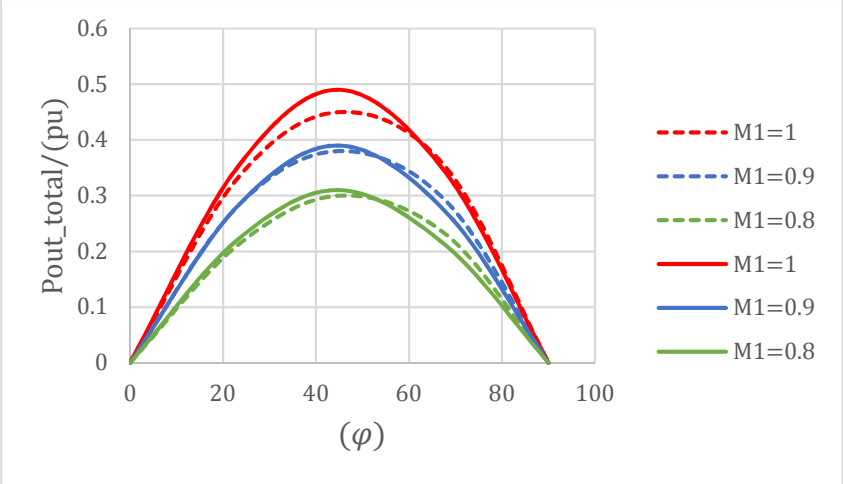


Figure 5.5 Normalized output power versus phase shift angle φ of the proposed converter with different values of modulation index (M_1); the solid line represents theoretical results and the dashed line simulation results

5.5 Control Strategy of the Proposed Converter

In this work, the primary Three-phase MMC is operated as a controllable voltage source to produce an AC voltage with constant amplitude and frequency so as to control the output voltage and current of the cascaded diode bridge rectifiers (It is noting that the secondary DC side is loaded by a fixed resistor. Therefore, the control/setting of power is achieved by the primary voltage of the transformer).

Figure 5.6 shows a schematic diagram of the *dq* vector-based control method for the three-phase MMC inverter at the primary side. Here I_{Pabc} and V_{Pabc} represent the primary three-phase AC currents and voltages respectively, I_{Pdq} and V_{Pdq} are the transfered d-axis and q-axis components of the primary three-phase AC currents and voltages respectively, and f_{AC} and L_{Parm} are the fundamental AC frequency and arm inductance of the primary three-phase MMC inverter respectively.

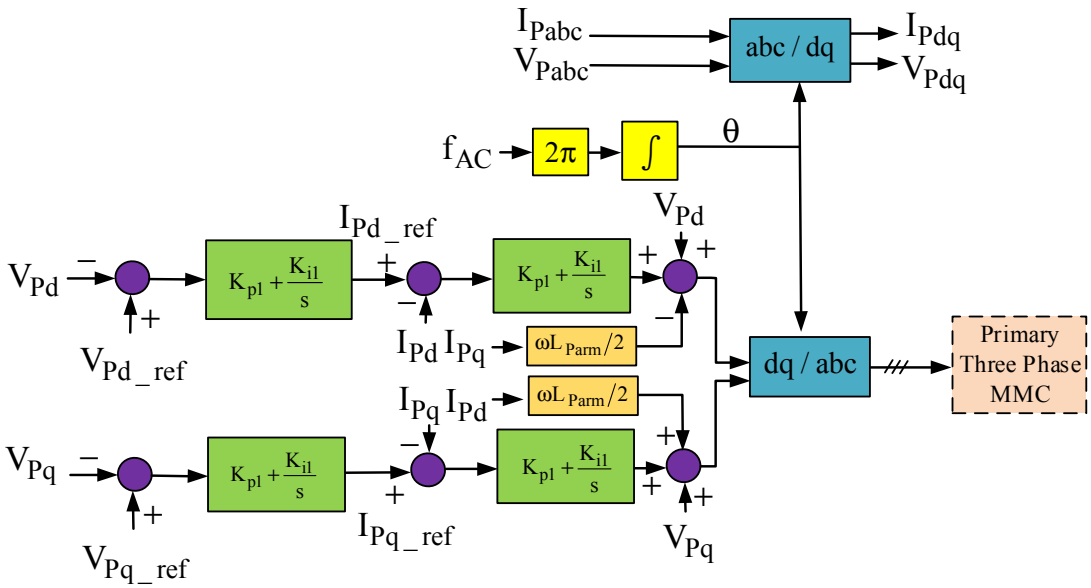


Figure 5.6 Control system for the primary three-phase MMC-based inverter.

Figure 5.6 transforms the three-phase system from a stationary to a rotating reference frame, so that the component of AC voltage/current in the *dq* frame becomes a DC value, and then a zero-error voltage PI controller can be used. In this control method, V_{Pd_ref} is set to the rated peak value of AC voltage, and V_{Pq_ref} is set to zero. MMC SM voltages are also regulated and balanced using the control method presented in Chapter 3, which is based on a simple PI controller [115]. The *dq* transformation matrix for the primary control system from the stationary to a rotating reference frame is given as:

$$C_{3s/2r} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - 120^{\circ}) & \cos(\theta + 120^{\circ}) \\ \sin\theta & \sin(\theta - 120^{\circ}) & \sin(\theta + 120^{\circ}) \end{bmatrix} \cdot \begin{bmatrix} V_{Pa} \\ V_{Pb} \\ V_{Pc} \end{bmatrix} \tag{5.37}$$

According to the analysis in Section 5.3, the mathematical model of the primary three-phase MMC of the proposed converter can be expressed as:

$$\begin{cases} \frac{1}{2} L_{Parm} \frac{dI_{Pa}}{dt} = E_{Pa} - V_{Pa} \\ \frac{1}{2} L_{Parm} \frac{dIP_{b}}{dt} = E_{Pb} - V_{Pb} \\ \frac{1}{2} L_{Parm} \frac{dI_{c}}{dt} = E_{Pc} - V_{Pc} \end{cases} \tag{5.38}$$

where E_{Pa}, E_{Pb}, and E_{Pc} can be considered as the equivalent primary three-phase voltages of the transformer.

Applying the transformation matrix of (5.37) into (5.38) yields:

$$\begin{cases} L_{Parm}\frac{dI_{Pd}}{dt} - \omega L_{Parm} I_{Pq} = E_{Pd} - V_{Pd} \\ L_{Parm}\frac{dI_{Pq}}{dt} + \omega L_{Parm} I_{Pd} = E_{Pq} - V_{Pq} \end{cases} \quad (5.39)$$

Vector control can be divided into two parts over the inner and outer loops. The outer loop is used to produce the references I_{Pd_ref} and I_{Pq_ref} which are utilised by the inner loop control to regulate the converter's control waveform. According to figure 5.6 and (5.39), the control waveform based on the *dq* synchronous reference frame can be expressed as:

$$\begin{cases} E_{Pd} = \left(K_p + \frac{K_i}{s}\right)\left(I_{Pd\_ref} - I_{Pd}\right) + V_{Pd} - \omega L_{Parm} I_{Pq} \\ E_{Pq} = \left(K_p + \frac{K_i}{s}\right)\left(I_{Pq\_ref} - I_{Pq}\right) + V_{Pq} + \omega L_{Parm} I_{Pd} \end{cases} \quad (5.40)$$

where k_p is the proportional constant which is used to improve the transient response of the control system, and k_i is the integral constant of the PI controller.

5.6 Simulation Results

To validate the theoretical analysis and assess the effectiveness of the proposed converter, a simulation model of 12 MW/150kV was developed using MATLAB/SIMULINK software with the parameters listed in table 5.1. In this work, each phase of the MMC converter at the primary side was constructed with five half-bridge SMs per arm. On the secondary side, each decoupled phase has two common diode bridge rectifier modules connected in series.

The primary three-phase AC voltage and the decoupled voltages at the secondary side are presented in figures 5.7-5.10, where two identical decoupled voltages at the secondary side are obtained from each primary input phase. It should also be noted that the other pairs of the secondary decoupled voltages are shifted by 120-degrees, as illustrated in figure 5.8-5.10. It is worth mentioning that higher numbers of windings (with more diode bridge rectifier modules) at each secondary decoupled phase can be considered if a higher voltage is required at the output side. The primary three-phase AC current at the primary side and the decoupled currents at the secondary side are shown in figures 5.11 and 5.12. Similar to the voltage waveforms, two identical decoupled currents at the secondary side are obtained from each primary input phase.

The performance of the balance control method is also confirmed and demonstrated in figure

5.13 (taking Phase-a of the primary MMC as an example). The capacitor voltages of SMs are tightly controlled at their reference values as shown in figure 5.13(a) for the capacitor voltages of the upper arm SMs and figure 5.13(b) for the capacitor voltages of the lower arm SMs, each at 15kV/5.

The output DC voltage, current, and power of the proposed converter are shown in figure 5.14. The average output DC voltage is maintained around 150kV.

The performance of the proposed control strategy was further investigated and confirmed with a 40% step change of the output power. Figure 5.15 shows the dynamic response of the proposed controller when the load is changed at $t = 1.5s$, where it can be seen that the output DC current and power decrease rapidly, while the output DC voltage and primary three-phase AC voltage are maintained at constant levels, which confirms the effectiveness of the proposed control system.

Table 5.1 Simulation parameters

Parameter	Value
Rated power	12MW
Input DC voltage	15kV
Output DC voltage	150kV
Output load resistor	1900Ω
SM numbers of primary MMC per arm	5
Numbers of diode bridge rectifier module at secondary	6
Transformer ratio	1:10
Submodule capacitor of primary MMC	3.6mF
The inductance of primary MMC per arm	1mH
Output capacitor	1mF
Output inductor	0.33mH
Switching frequency	2000Hz
AC fundamental frequency	400Hz

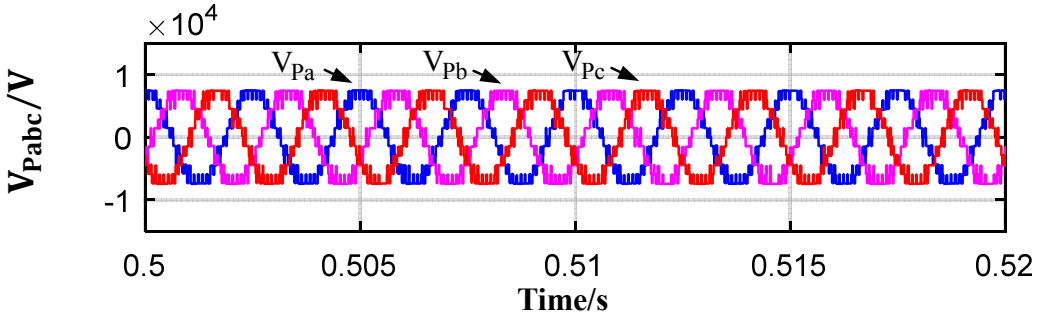


Figure 5.7 Transformer primary three-phase AC voltages.

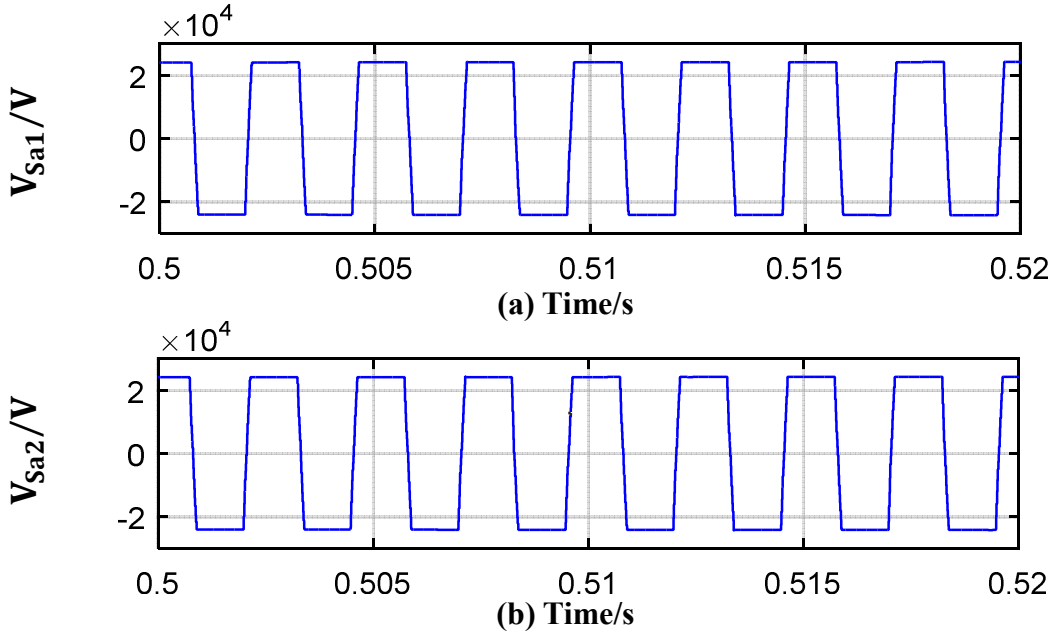


Figure 5.8 Transformer secondary side Phase-a AC voltage waveforms: (a) module-one; (b) module-two.

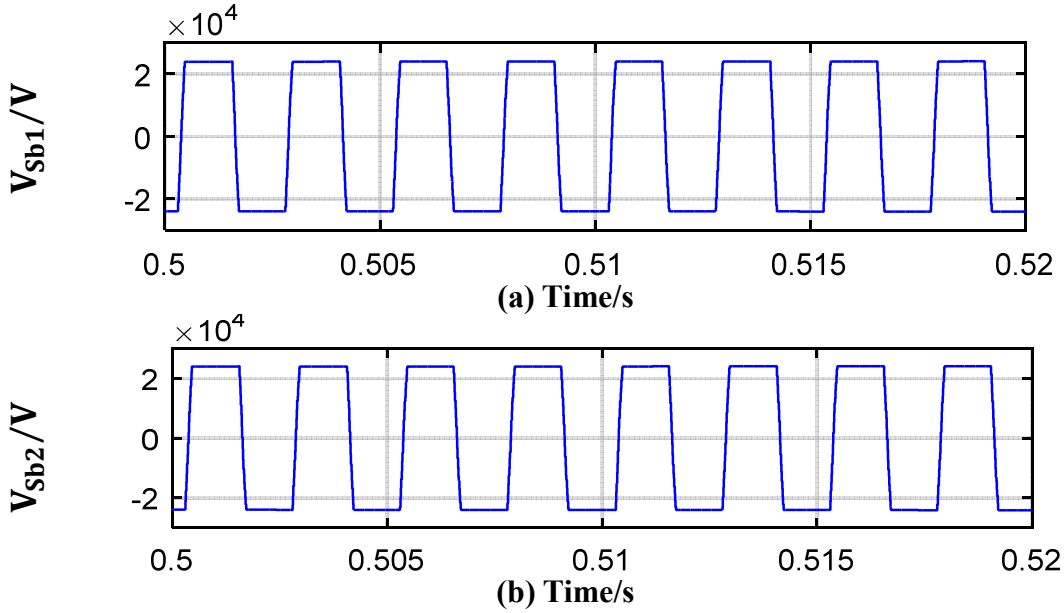
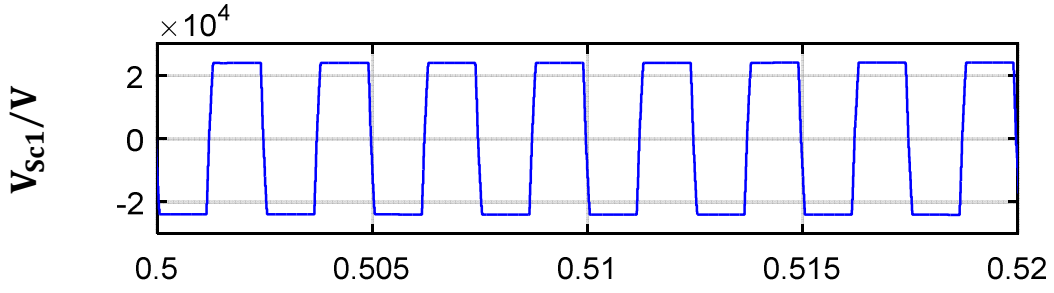


Figure 5.9 Transformer secondary side Phase-b AC voltage waveforms: (a) module-one; (b) module-two.



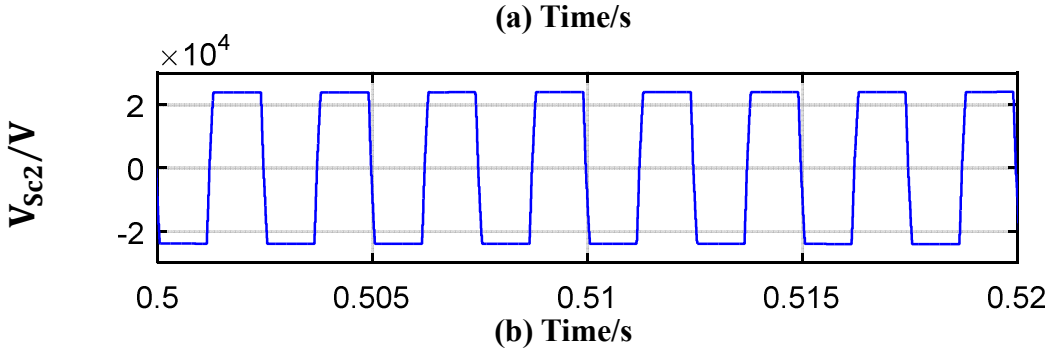


Figure 5.10 Transformer secondary side Phase-C AC voltage waveforms: (a) module-one; (b) module-two.

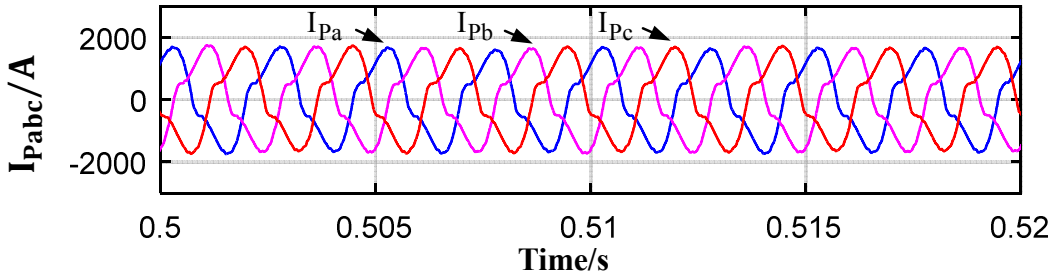
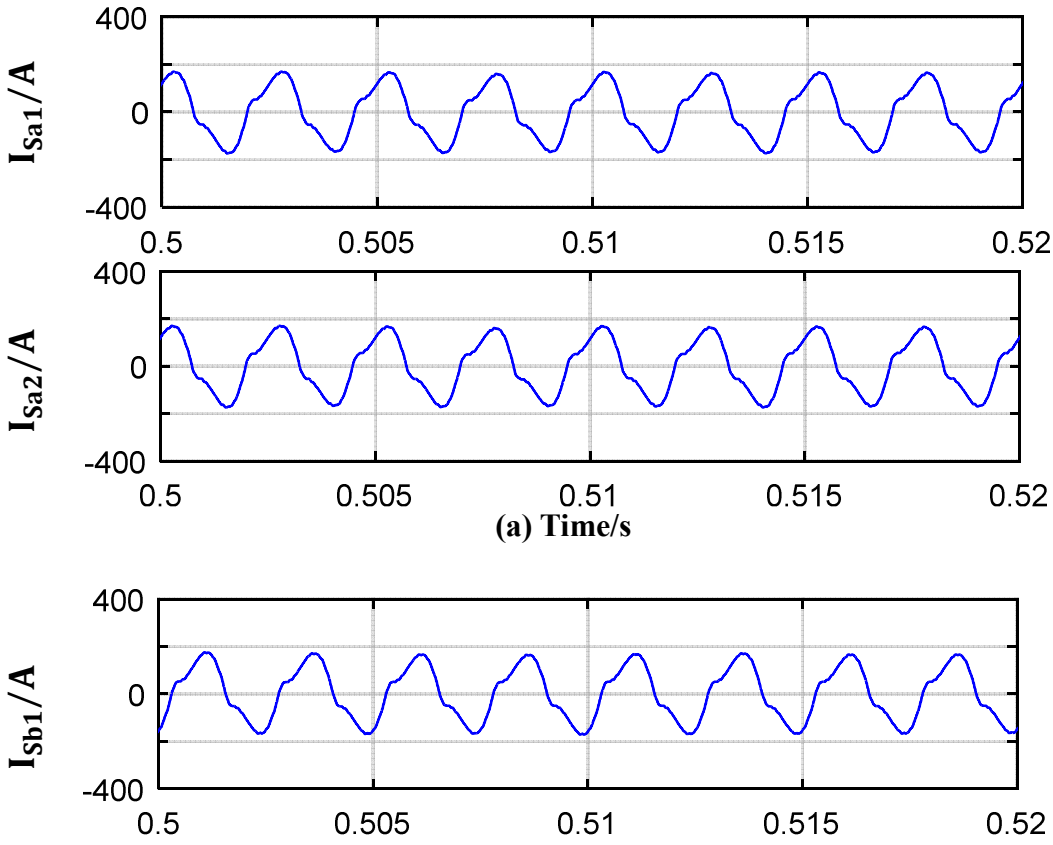


Figure 5.11 Transformer primary three-phase AC currents.



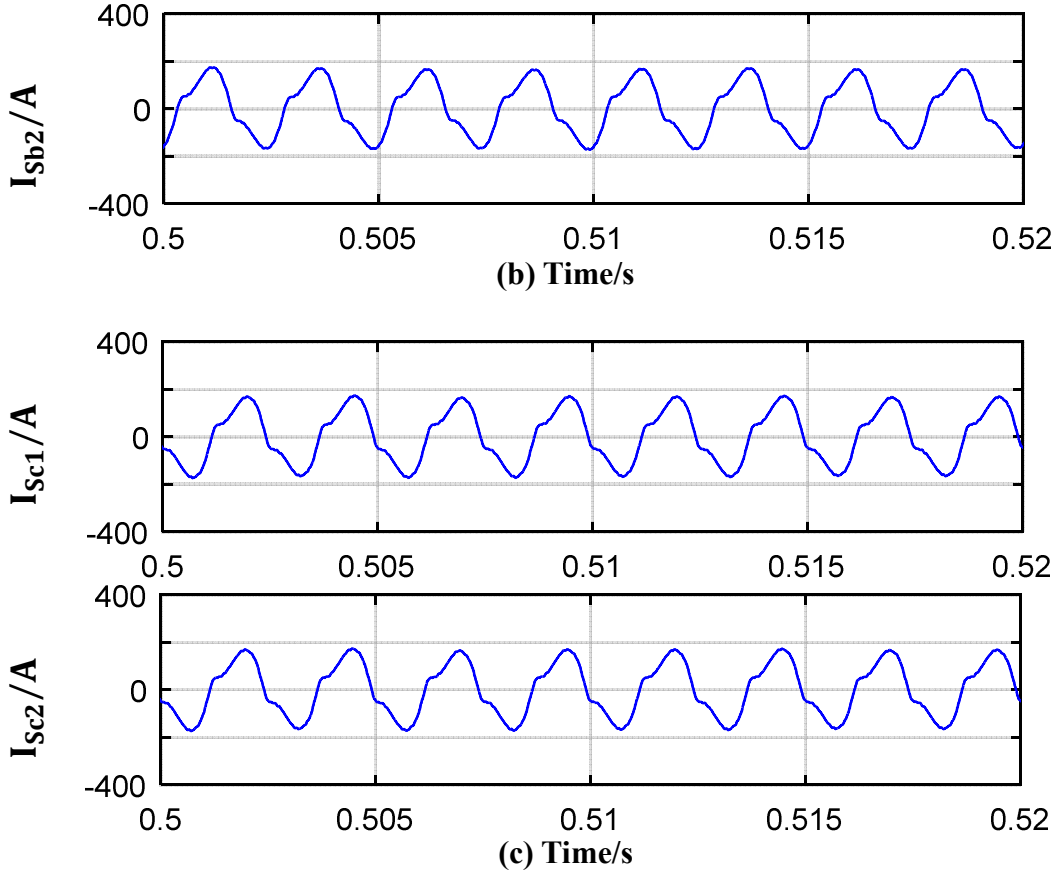


Figure 5.12 Transformer current waveforms: (a) secondary side Phase-a module-one and module-two AC current; (b) secondary side Phase-b module-one and module-two AC current; (c) secondary side Phase-c module-one and module-two AC current.

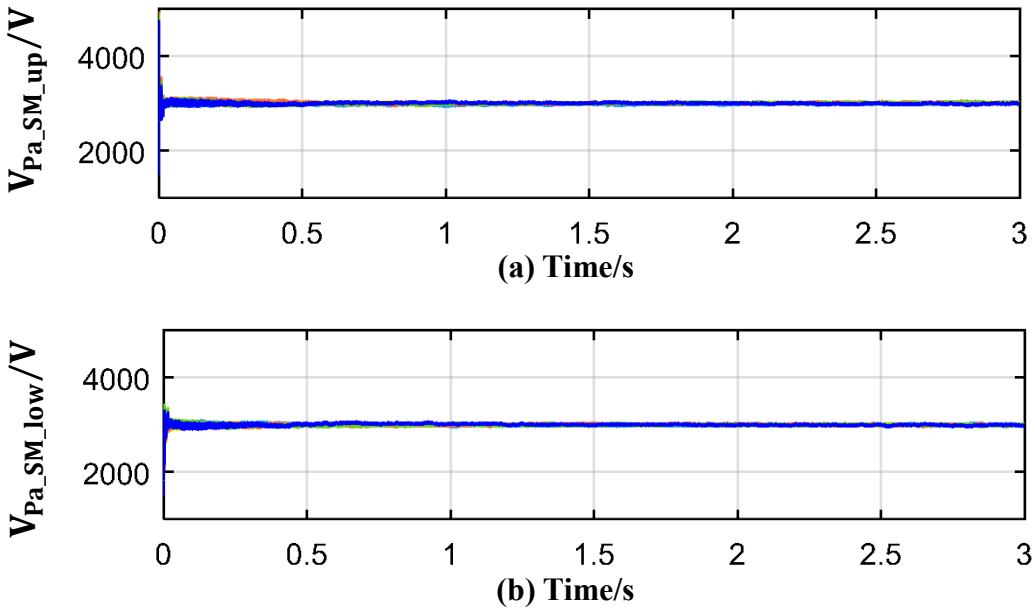


Figure 5.13 Primary Phase-a: (a) upper SM voltages and (b) lower SM voltages.

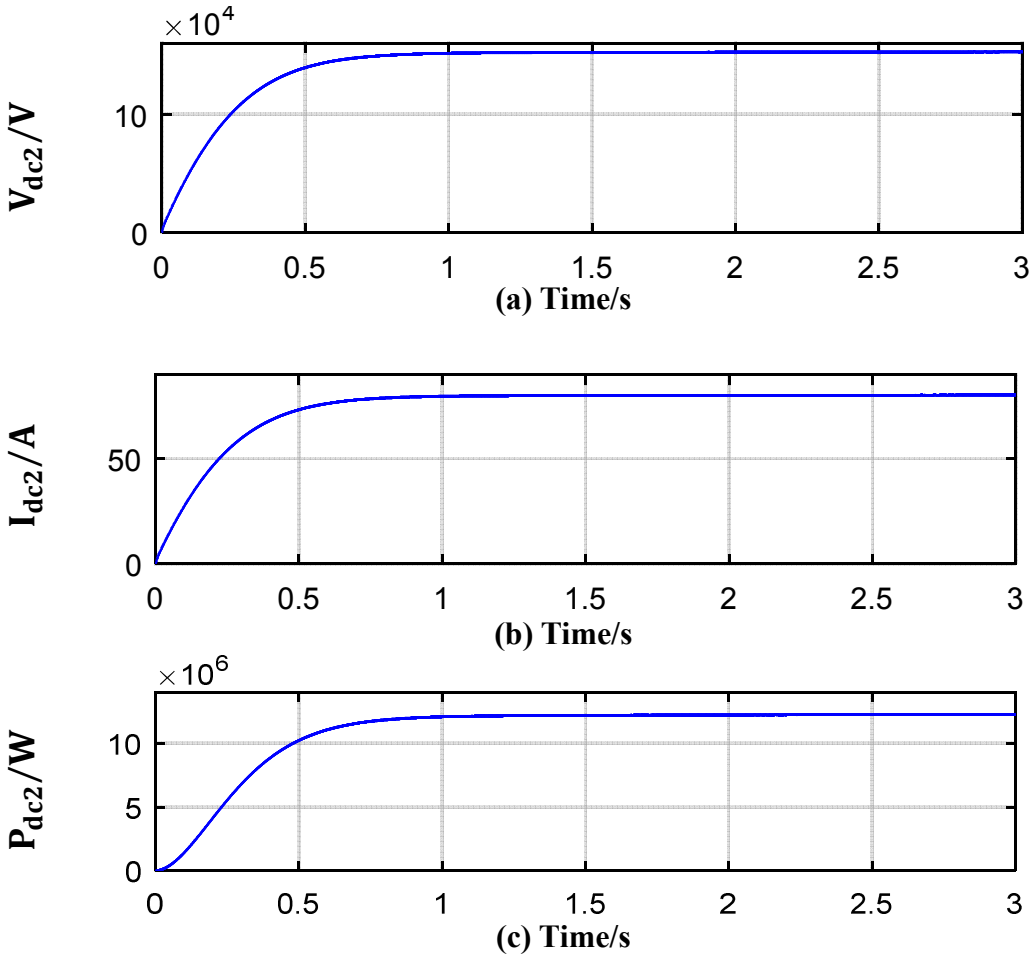
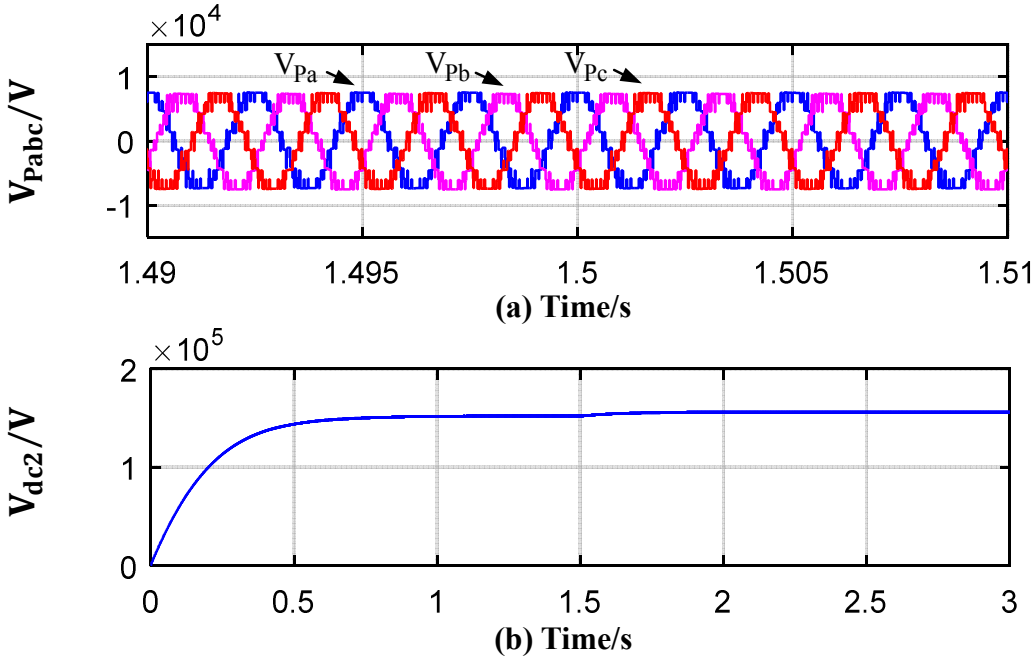


Figure 5.14 Output waveforms of the proposed converter under steady-state operation: (a) output DC voltage; (b) output DC current; (c) output power.



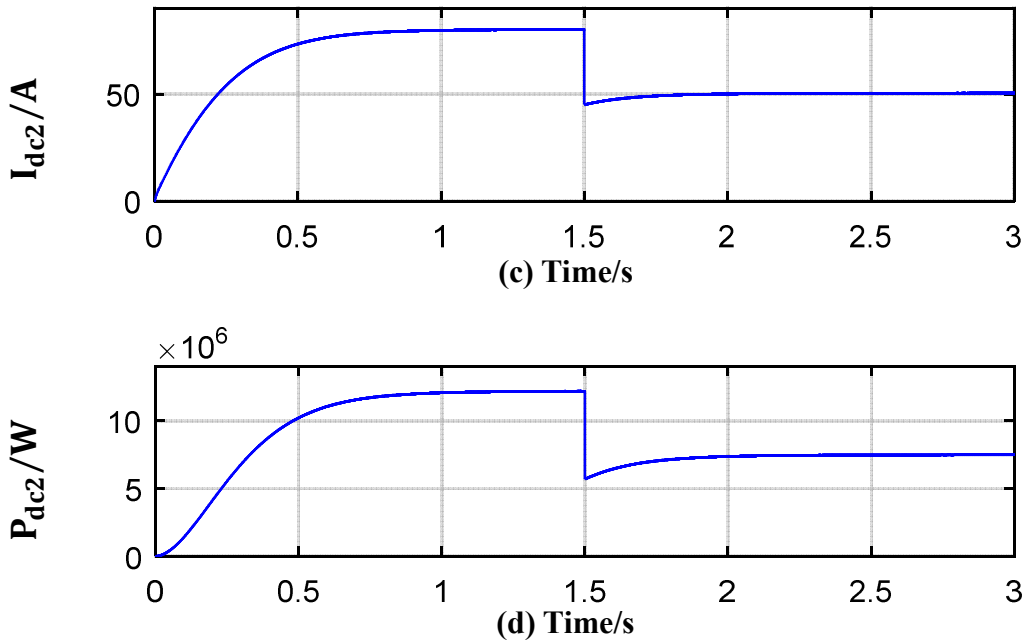


Figure 5.15 Output waveforms of the proposed converter under a 40% step change at 1.5s:(a) transformer primary three-phase AC voltages; (b) output DC voltage; (c) output DC current; (d) output power.

5.7 Summary

Chapter 5 has proposed a unidirectional three-phase modular DC/DC converter. To understand the operating characteristics of the proposed converter, a detailed description of the circuit configuration, derivation of the mathematical model and analysis of the output power characteristics of the proposed converter are presented and thoroughly discussed. Moreover, a control method based on a rotating reference frame is developed for the proposed converter. Finally, simulation results are also presented.

Chapter 6. Bidirectional Three-Phase DC/DC Modular Multilevel Converter

6.1 Introduction

Unlike previous chapters, this chapter presents the design and analysis of a bidirectional three-phase modular DC/DC converter incorporating a three-phase modular multilevel converter (MMC) inverter topology with a three-phase decoupled transformer. At this time, the DC voltage is collected at the secondary side of the transformer through series-connected one-leg MMC rectifier modules. The proposed system is highly modular and has lower voltage stress on the half-bridge-based submodule (SM). A high DC conversion ratio is achieved by increasing the number of series-connected one-leg MMC rectifier modules as well as through adjusting the transformer ratio.

6.2 Configuration of the Proposed Converter

Figure 6.1 shows a simplified schematic diagram of the proposed DC/DC converter, where a three-phase MMC inverter is connected at the primary side of a three-phase decoupled medium frequency transformer. The secondary output voltages are decoupled into three identical voltages, phase-shifted by 120-degrees from each other. Moreover, each decoupled phase is further split into multiple windings to maximize the output DC voltage by cascading the MMC-based rectifier modules at the secondary side of the transformer. It is worth noting that the design is fully modular at both sides and can easily be expanded by simply stacking additional modules as required. The proposed topology can also be reconfigured to meet different operating conditions via connecting the output modules in series and parallel if needed.

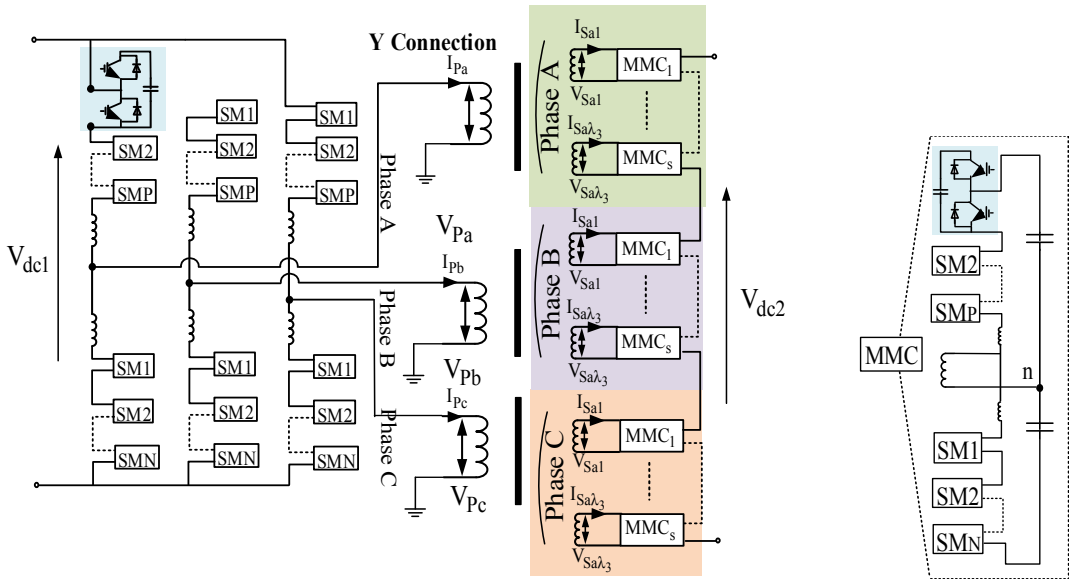


Figure 6.1 The proposed DC/DC converter: (a) configuration; (b) one-leg MMC based module at the secondary side of the proposed converter.

6.3 Mathematical Model

***For the primary side*:** Figure 6.2 shows the equivalent circuit of one-leg (Phase-a) of the MMC inverter, where V_{dc1} and I_{dc1} are the converter's input DC voltage and current respectively, V_{aU} and V_{aL} are the voltages of the upper and lower arm of Phase-a respectively, I_{aU} and I_{aL} are the currents of the upper and lower arms of Phase-a respectively, E_{Pa} is the equivalent output phase voltage as shown in figure 6.2(b), and V_{Pa} is the output AC voltage respectively, I_{cir} and I_{Pa} are the circulating and the AC ouput currents respectively, and L_{Parm} and L_{Sarm} are the arm inductances of the primary and secondary side of the proposed converter respectively.

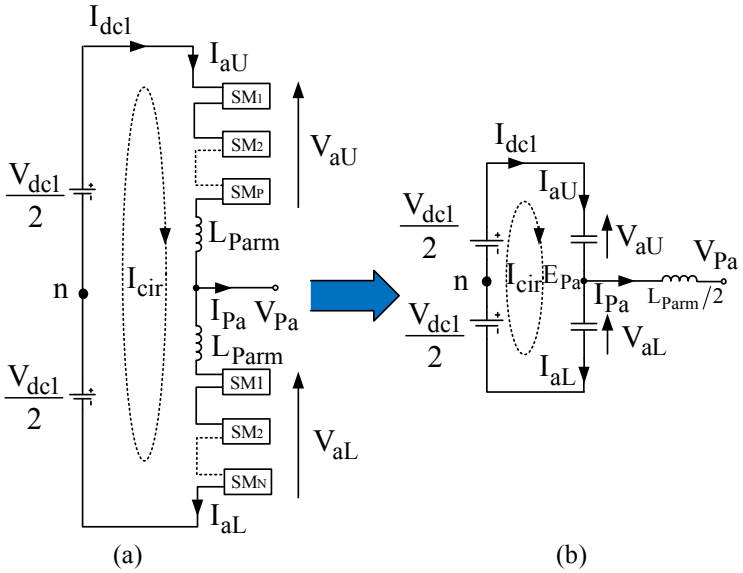


Figure 6.2 The one-leg MMC: (a) schematic diagram; (b) equivalent circuit.

$$I_{aU} = I_{Pa}/2 + I_{cir} \tag{6.1}$$

$$I_{aL} = -I_{Pa}/2 + I_{cir} \tag{6.2}$$

where the circulating current, I_{cir}, is flowing through both the upper and lower arms.

It should be noted that the circulating current has no effect on the output phase current and can be written as:

$$I_{cir} = (I_{aU} + I_{aL})/2 \tag{6.3}$$

Concerning (6.1) and (6.2), the AC output current I_{Pa} can be expressed in terms of the upper and lower arm currents as:

$$I_{Pa} = I_{aU} - I_{aL} \tag{6.4}$$

If *n* is the neutral point, then applying the Kirchhoff voltage law (KVL) at the one-leg MMC shown in figure 6.2(a) gives upper and lower voltages as follows:

$$V_{aP} = \frac{V_{dc}}{2} - V_{Pa} - L_{Parm}\frac{dI_{aP}}{dt} \tag{6.5}$$

$$V_{aL} = \frac{V_{dc}}{2} + V_{Pa} - L_{Parm}\frac{dI_{aN}}{dt} \tag{6.6}$$

By combining (6.5) and (6.6), the output phase voltage V_{Pa} can be expressed as:

$$V_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) - \frac{1}{2}L_{Parm}\frac{d(I_{aL}-I_{aU})}{dt} \tag{6.7}$$

By substituting (6.4) into (6.7), the equivalent output phase voltage E_{Pa} can be given by:

$$E_{Pa} = \frac{1}{2}(V_{aL} - V_{aU}) = V_{Pa} + \frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} \tag{6.8}$$

Therefore, the mathematical model of the one-leg MMC can be derived by rearranging (6.8) as:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pa}}{dt} = E_{Pa} - V_{Pa} \tag{6.9}$$

According to (6.9), the equivalent circuit of Phase-a can be represented as in figure 6.2 (b).

Similarly, the mathematical models of Phase-b and Phase-c of the MMC inverter at the primary side are given by:

$$\frac{1}{2}L_{Parm}\frac{dI_{Pb}}{dt} = E_{Pb} - V_{Pb} \tag{6.10}$$

$$\frac{1}{2}L_{Parm}\frac{dI_{Pc}}{dt} = E_{Pc} - V_{Pc} \tag{6.11}$$

where E_{Pb} and E_{Pc} are the equivalent output voltages of Phase-b and Phase-c respectively, while V_{Pb} and V_{Pc} are the AC output voltages of Phase-b and Phase-c respectively, and I_{Pb} and I_{Pc} are the AC ouptut currents of Phase-b and Phase-c respectively. It should be noted again that each phase has exactly the same inductance, which is denoted as L_{Parm}.

For the secondary side: From figure 6.1, at the secondary side of the transformer, individual and isolated MMC-based modules are cascaded. This can be regarded as a series connection of voltage sources ($V_{Sa1}, V_{Sa2}, \dots, V_{Sa\lambda_3}$ for Phase-a, $V_{Sb1}, V_{Sb2}, \dots, V_{Sb\lambda_3}$ for Phase-b, and $V_{Sc1}, V_{Sc2}, \dots, V_{Sc\lambda_3}$ for Phase-c). Therefore, the total equivalent voltage of each decoupled phase at the secondary side of the transformer, V_{Sa}, V_{Sb}, and V_{Sc}, can be expressed as:

$$V_{Sa} = V_{Sa1} + V_{Sa2} + \cdots + V_{Sa\lambda_3} \tag{6.12}$$

$$V_{Sb} = V_{Sb1} + V_{Sb2} + \cdots + V_{Sb\lambda_3} \tag{6.13}$$

$$V_{Sc} = V_{Sc1} + V_{Sc2} + \cdots + V_{Sc\lambda_3} \tag{6.14}$$

where λ_3 is the number of one leg MMC-based modules of each decoupled phase at the secondary side of the transformer.

If the equivalent primary-to-secondary winding turns ratio of each phase is R_t, and the turns ratio of primary to each individual secondary winding of each phase is T_r, the equivelant secondary voltages V_{Sa}, V_{Sb} and V_{Sc} when referred to the primary side can then be given by:

$$V_{Pa} = V_{Sa}R_t = V_{Sa1}\frac{T_r}{\lambda_3} + V_{Sa2}\frac{T_r}{\lambda_3} + \cdots + V_{Sa\lambda_3}\frac{T_r}{\lambda_3} \tag{6.15}$$

$$V_{Pb} = V_{sb}R_t = V_{sb1}\frac{T_r}{\lambda_3} + V_{sb2}\frac{T_r}{\lambda_3} + \cdots + V_{Sb\lambda_3}\frac{T_r}{\lambda_3} \tag{6.16}$$

$$V_{Pc} = V_{sc}R_t = V_{sc1}\frac{T_r}{\lambda_3} + V_{sc2}\frac{T_r}{\lambda_3} + \cdots + V_{Sc\lambda_3}\frac{T_r}{\lambda_3} \tag{6.17}$$

Substituting (6.15), (6.16) and (6.17) into (6.9),(6.10) and (6.11) respectively, and with the transformer's leakage inductance L_k of each phase referred to the primary side, the primary referred equivalent circuit of the proposed converter can be expressed by (6.18) and schematically represented as in figure 6.3.

$$\begin{cases} (\frac{L_{arm}}{2} + L_k)\frac{dI_{Pa}}{dt} = E_{Pa} - V_{Sa}R_t \\ (\frac{L_{arm}}{2} + L_k)\frac{dI_{Pb}}{dt} = E_{Pb} - V_{Sb}R_t \\ (\frac{L_{arm}}{2} + L_k)\frac{dI_{Pc}}{dt} = E_{Pc} - V_{Sc}R_t \end{cases} \tag{6.18}$$

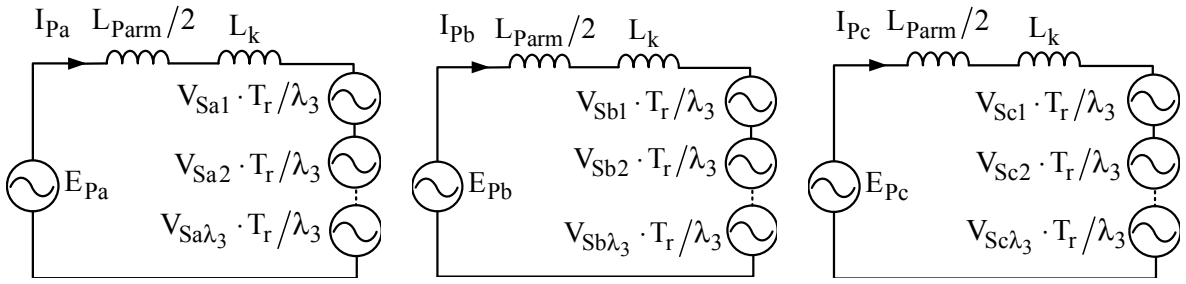


Figure 6.3 Equivalent circuit of the proposed converter referred to the primary side.

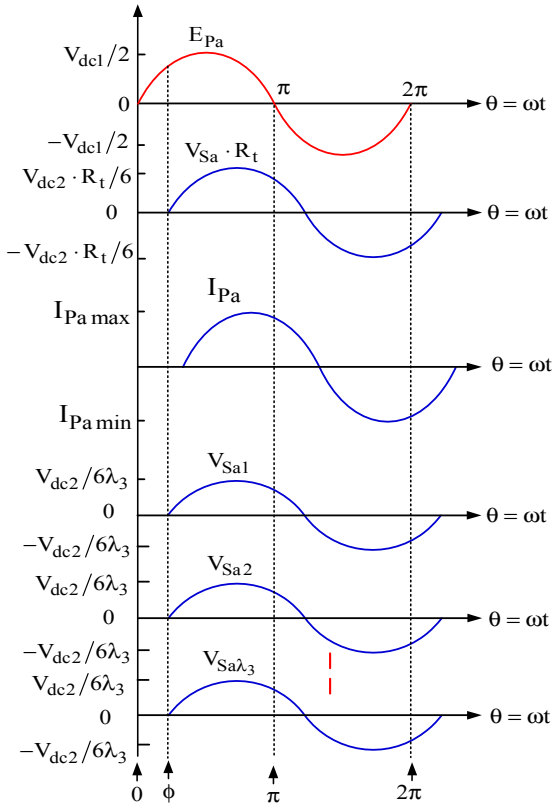


Figure 6.4 Phase-a: primary equivalent AC voltage, E_{Pa}; equivalent secondary voltage referred to the primary side, $V_{Sa}R_t$; secondary AC voltages of each winding of transformer, $V_{Sa1}, V_{Sa2}, \ldots, V_{Sa\lambda_3}$.

6.4 Output Power Characteristics

6.4.1 *Typical voltage waveforms*

To simplify the analysis, the following assumptions are made for the output voltage waveform of the primary side MMC: 1) the submodule capacitor voltages are well-balanced and ripple-free; 2) the converter is operating with a unity modulation index; and 3) the MMC is built with a high number of SMs resulting in an approximately sinusoidal AC output waveform.

Given the above assumptions, and taking Phase-a as an example, the ideal primary and secondary referred voltage waveforms of the proposed converter can be obtained as shown in figure 6.4 (taking Phase-a as example), where the power is transferred from the primary side to the secondary side (and it should be noted that, for the reverse power flow, similar results can be obtained in the same manner). Taking Phase-a as an example, as mentioned above, V_{Sa} is the equivalent Phase-a voltage at the secondary side which is given by $V_{Sa} = V_{Sa1} + V_{Sa2} + \cdots + V_{Sa\lambda_3}$ and φ is the phase shift angle by which the primary equivalent Phase-a voltage, E_{Pa}, leads the equivalent Phase-a voltage of the secondary side, V_{Sa}.

6.4.2 *Derivation of the output power*

It should be noted that, in the subsequent analysis, the following assumptions are made: 1) owing to the symmetry of the waveform, only a half-cycle of the AC waveform is considered for the output power derivation; and 2) for simplicity, the peak value of the primary equivalent AC voltage of Phase-a, E_{Pa}, is equal to $\frac{V_{dc1}}{2}$, (ignoring any voltage drop across the circuit components).

According to figure 6.1, the decoupled three phases at the secondary side of the transformer are connected in series, and each will withstand one-third of the output voltage, $\frac{V_{dc2}}{3}$. Therefore, the peak value of the secondary equivalent AC voltage of Phase-a, $\hat{V}_{sa}$, is equal to $\hat{V}_{sa} = \frac{1}{2} * \frac{V_{dc2}}{3} = \frac{V_{dc2}}{6}$. From figure 6.4, the output power can be derived as follows.

Interval 1 *(*$0 \le \theta < \varphi$*)*:

From figure 6.4, during this interval $E_{Pa}(\theta)$, $V_{Sa}(\theta)$, and $I_{Pa}(\theta)$ can be expressed by:

$$E_{Pa}(\theta) = \frac{V_{dc1}}{2} \cdot \sin(\theta) \tag{6.19}$$

$$V_{Sa}(\theta) = \frac{R_t V_{dc2}}{6} \cdot \sin(\theta - \varphi) \tag{6.20}$$

$$I_{Pa}(\theta) = I_{Pa}(0) + \frac{1}{\omega L}\int_0^{\theta}[E_{Pa}(\theta) - V_{Sa}(\theta)]d\theta \tag{6.21}$$

where ω is the fundamental angular frequency of the system, and L is the equivalent inductance of converter which is equal to $L = \frac{L_{Parm}}{2} + L_k$.

Substituting (6.19) and (6.20) into (6.21) yields:

$$I_{Pa}(\theta) = I_{Pa}(0) + \frac{R_t V_{dc2}\cos(\theta-\varphi) - R_t V_{dc2}\cos(\varphi)}{6\omega L} + \frac{V_{dc1}\sin(\frac{\theta}{2})^2}{\omega L} \tag{6.22}$$

From (6.22), at $\theta = \varphi$, one can get:

$$I_{Pa}(\varphi) = \frac{1}{6\omega L}[3V_{dc1} + 6\omega L I_{Pa}(0) + R_t V_{dc2} - 3V_{dc1}\cos(\varphi) - R_t V_{dc2}\cos(\varphi)] \tag{6.23}$$

According to (6.20) and (6.22), the output energy during this interval can be obtained by:

$$\begin{aligned} \mathrm{E}_1 = \int_0^{\varphi} V_{Sa}(\theta)\cdot I_{Pa}(\theta)d\theta = -\frac{R_t V_{dc2}}{72\cdot\omega L}[&6V_{dc1} + 12\omega L I_{Pa}(0) + R_t V_{dc2} - 6V_{dc1}\cos(\varphi) - \\ &3V_{dc1}\varphi\sin(\varphi) + R_t V_{dc2}\cos\varphi^2 - 12\omega L I_{Pa}(0)\cos(\varphi) - \\ &2R_t V_{dc2}\cos(\varphi)] \end{aligned} \tag{6.24}$$

Interval 2 *(*$\varphi \le \theta < \pi$*)*:

During this interval $E_{Pa}(\theta)$, $V_{Sa}(\theta)$, and $I_{Pa}(\theta)$ can be given by:

$$E_{Pa}(\theta) = \frac{V_{dc1}}{2} \cdot \sin(\theta) \tag{6.25}$$

$$V_{Sa}(\theta) = \frac{R_t V_{dc1}}{6} \cdot \sin(\theta - \varphi) \tag{6.26}$$

$$I_{Pa}(\theta) = I_{Pa}(\varphi) + \frac{1}{\omega L}\int_{\varphi}^{\theta}[E_{Pa}(\theta) - V_{Sa}(\theta)]d\theta \tag{6.27}$$

Substituting (6.23), (6.25) and (6.26) into (6.27) yields:

$$\begin{aligned} I_{Pa}(\theta) = \frac{1}{6\omega L}[&3V_{dc1} + 6\omega L I_{Pa}(0) - 3V_{dc1}\cos(\theta) + R_t V_{dc2}\cos(\theta - \\ &\varphi) R_t V_{dc2}\cos(\varphi)] \end{aligned} \tag{6.28}$$

From (6.28), at $\theta = \pi$, one can get:

$$I_{Pa}(\pi) = \frac{1}{3\omega L}[3V_{dc1} + 3\omega L I_{Pa}(0) - R_t V_{dc2}\cos(\varphi)] \tag{6.29}$$

Similarly, the transferred energy during this interval is given by:

$$\begin{aligned} \mathrm{E}_2 = \int_{\varphi}^{\pi} V_{Sa}(\theta)\cdot I_{Pa}(\theta)d\theta = \frac{R_t V_{dc2}}{72\cdot\omega L}[&6V_{dc1} + 12\omega L I_{Pa}(0) + R_t V_{dc2} + 6V_{dc1}\cos(\varphi) - \\ &3V_{dc1}\varphi\sin(\varphi) - 3R_t V_{dc2}\cos\varphi^2 + 3\pi V_{dc1}\sin(\varphi) + \\ &12\omega L I_{Pa}(0)\cos(\varphi) - 2R_t V_{dc2}\cos(\varphi)] \end{aligned} \tag{6.30}$$

Therefore, from (6.24) and (6.30), the output power of the decoupled Phase-a of the proposed converter can be calculated as:

$$P_{out\_a} = \frac{E_1 + E_2}{\pi} \tag{6.31}$$

Due to half-cycle symmetry, $I_{Pa}(0) = -I_{Pa}(\pi)$ [118-119]. Therefore, according to (6.29), the intial current $I_{Pa}(0)$ can be calculated as:

$$I_{Pa}(0) = -\frac{3V_{dc1} - R_t V_{dc2}\cos(\varphi)}{6\omega L} \tag{6.32}$$

Substituting (6.24), (6.30), and (6.32) into (6.31), the output power of the proposed converter as a function of the phase shift angle, φ is given by:

$$P_{out\_a}(\varphi) = \frac{V_{dc1}V_{dc2}R_t\sin(\varphi)}{24\omega L} \tag{6.33}$$

It should be noted that (6.33) is derived based on the assumption that the modulation index $M_1 = 1$ and $M_2 = 1$ (M_1 and M_2 are the primary and secondary modulation indices respectively), which corresponds to the maximum power transfer capability of the proposed converter.

6.4.3 *Output power characteristics*

For simplicity, the output power is normalized to a base power of $P_{base} = \frac{V_{dc1}V_{dc2}R_t}{8\omega L}$, which yields:

$$P_{out\_a}(\varphi) = \frac{1}{3}M_1 M_2\sin(\varphi) \qquad (-\pi \le 0 \le \pi) \tag{6.34}$$

where the modulation index $M_1 \in [0,1]$ and $M_2 \in [0,1]$ are introduced in order to get the

generalized equation of the output power.

Similarly, the output power of Phase-b and Phase-c can also be obtained in the same manner:

$$P_{out\_b}(\varphi) = \frac{1}{3}M_1M_2\sin(\varphi) \qquad (-\pi \le 0 \le \pi) \tag{6.35}$$

$$P_{out\_c}(\varphi) = \frac{1}{3}M_1M_2\sin(\varphi) \qquad (-\pi \le 0 \le \pi) \tag{6.36}$$

Therefore, the total output power can be calculated as:

$$P_{out\_total}(\varphi) = P_{out\_a}(\varphi) + P_{out\_b}(\varphi) + P_{out\_b}(\varphi) = M_1M_2\sin(\varphi) \quad (-\pi \le 0 \le \pi) \tag{6.37}$$

According to (6.37), the variation in the normalized total output power concerning phase shift angle φ can be obtained as shown in figure 6.5, where it is clear that, when $-\pi \le \varphi \le 0$, power is transferred from the primary side to the secondary side. Conversely, when $0 \le \varphi \le \pi$, the power is transferred from the secondary side to the primary side. The power transfer capability of the proposed converter is influenced by the modulation indices M_1 and M_2, and the phase shift angle φ. In theory, the maximum output power occurs at the point at which $\frac{dP_{out\_total}}{d\varphi} = 0$, for which $\varphi = \pm\frac{\pi}{2}$.

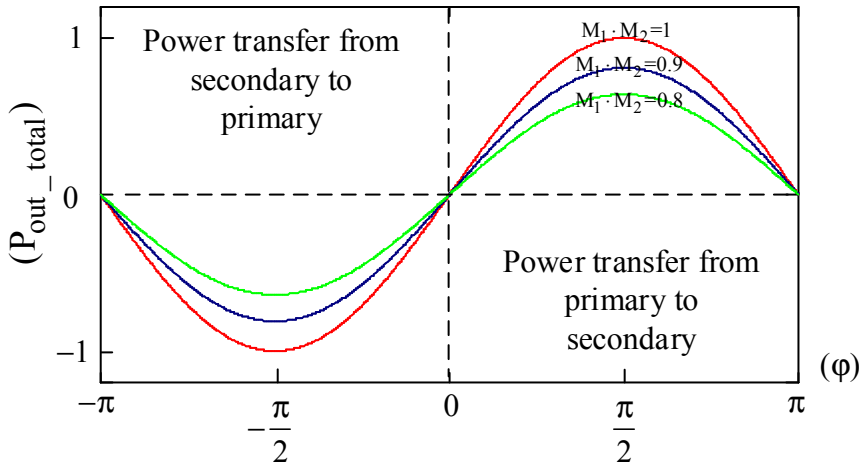


Figure 6.5 Normalized output power versus phase shift angle φ of the proposed converter.

6.5 Control Strategies of the Proposed Converter

a) Control system of the three-phase MMC inverter at the primary side

Figure 6.6 shows the schematic diagram of the *dq* vector-based control method for the three-

phase MMC inverter at the primary side, which is the same as the control strategy of the unidirectional three-phase DC/DC converter proposed in Chapter 5. Therefore, no detailed derivation is presented in this chapter, but rather just brief highlights to facilitate understanding.

In figure 6.6, I_{Pabc} and V_{Pabc} represent the primary three-phase AC current and voltage respectively, I_{Pdq} and V_{Pdq} are the transfered d-axis and q-axis components of the primary three-phase AC current and voltage respectively, and f_{AC} and L_{Parm} are the AC frequency and arm inductance of the primary MMC inverter respectively. The *dq* transformation matrix for the primary control system from the stationary to a rotating reference frame is given as:

$$C_{3s/2r} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta - 120^{\circ}) & \cos(\theta + 120^{\circ}) \\ \sin\theta & \sin(\theta - 120^{\circ}) & \sin(\theta + 120^{\circ}) \end{bmatrix} \cdot \begin{bmatrix} V_{Pa} \\ V_{Pb} \\ V_{Pc} \end{bmatrix} \tag{6.38}$$

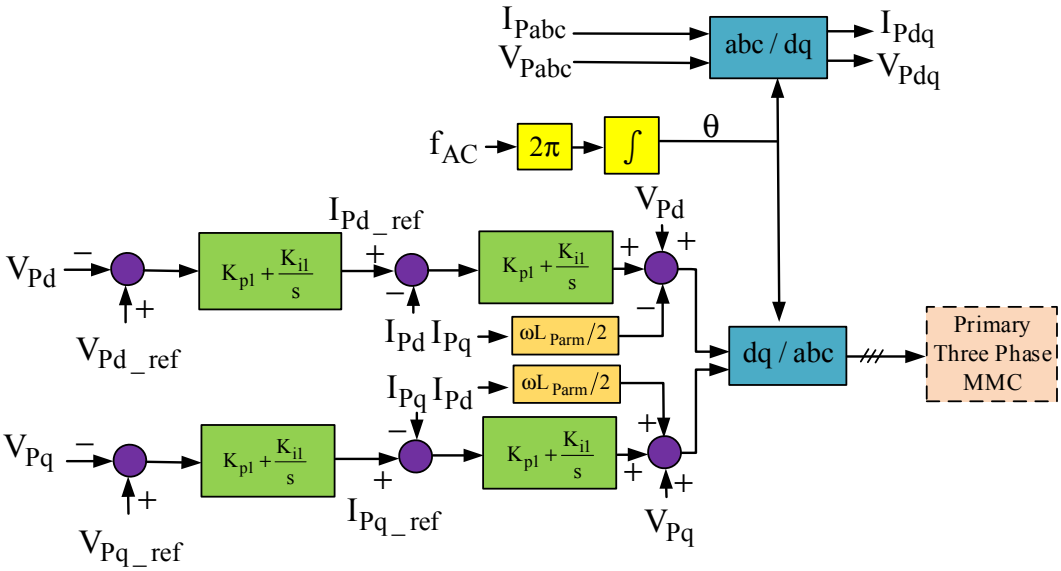


Figure 6.6 Control system for the primary three-phase MMC-based inverter.

As can be seen from figure 6.6, the control system includes two control loops for the outer voltage loop and the inner current loop. The AC voltage is fed back from the primary side of the transformer and compared with its reference value. Then, the resulting AC voltage error is used as an input to the outer loop PI controller. The output of the outer loop PI controller acts as the reference signal for the inner current control loop. In this control method, V_{Pd_ref} is set to the rated peak value of AC voltage, V_{Pq_ref} is set to zero and the AC frequency is set to f_{AC}. Primary MMC SM voltages are also regulated and balanced using the control method presented elsewhere [115] based on a simple PI controller.

b) Control system of the one-leg MMC-based rectifiers at the secondary side:

Figure 6.7 shows the control block diagram for the one-leg MMC based rectifier modules at the secondary side. Here I_{Sa1} and V_{Sa1} are the actual AC voltage and current of the one-leg MMC rectifier module-one, MMC_{a1}, in the decoupled Phase-a respectively, $I_{S\alpha\beta1}$ and $V_{S\alpha\beta1}$ are the current and voltage orthogonal pairs respectively realised by the phase delay of 90-degrees, $V_{out\_MMC_{a1}}$ and $V_{out\_MMC_{a1}\_ref}$ are the MMC_{a1} output DC voltage and its reference value, L_{Sarm} is the arm inductance of the one-leg MMC rectifier module-one, MMC_{a1}, in the decoupled Phase-a (and it should be noted that all other one-leg MMC rectifier modules at the secondary side have the same arm inductance).

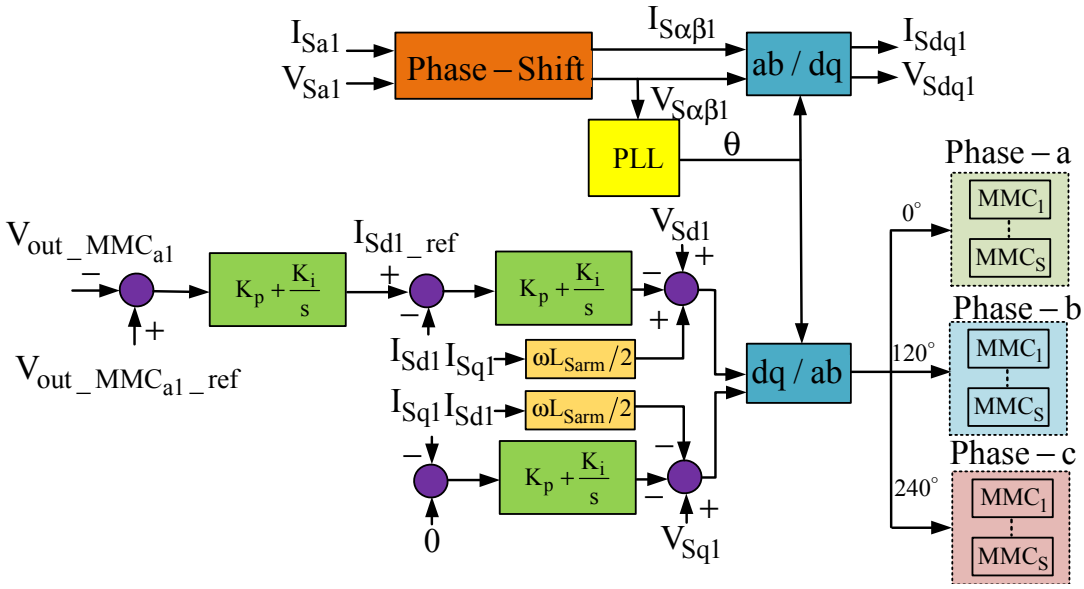


Figure 6.7 Control system for the secondary one-leg MMC-based rectifiers.

From figure 6.7, the secondary side of the proposed converter is controlled by a *dq* vector control method. However, only one-leg MMC rectifier is employed at the secondary side, which requires fictitious values of voltage/current realised by the phase delay of 90-degrees to allow the transformation from a conventional stationery to a rotating frame. This will enable the implementation of the PI controller. As can be seen from figure 6.7, the q-axis current I_{Sq1} can be simply set to zero, which means a unity power factor can be achieved. The whole control system is again realized by two control loops. The outer voltage loop is employed to regulate

the output DC voltage of MMC_{a1} in the decoupled Phase-a and the inner current loop regulates the input AC current of MMC_{a1} in the decoupled Phase-a. The control signals of the other modules in the decoupled Phase-a can be directly obtained from MMC_{a1}. Similarly, the control signals of the one-leg MMC rectifier modules in Phases b and c are also obtained from the MMC_{a1} of the decoupled Phase-a, but with shifts in the phases of 120 and 240 degrees respectively. The *dq* transformation matrix for the secondary control system from the stationary to a rotating reference frame is given as:

$$C_{2s/2r} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} V_{rd1} \\ V_{rq1} \end{bmatrix} \tag{6.39}$$

According to the derivation of the above mathematical model of the proposed converter, the model of the secondary one-leg MMC rectifier module-one, MMC_{a1}, can be easily obtained and expressed as:

$$\frac{L_{Sarm}}{2}\frac{dI_{Sa1}}{dt} = V_{Sa1} - E_{Sa1} \tag{6.40}$$

where E_{Sa1} can be considered as the equivalent AC voltage of MMC_{a1} in the decoupled Phase-a at the secnodary side.

Applying the transformation matrix of (6.39) into (6.40) yields:

$$\begin{cases} L_S\frac{dI_{Sd1}}{dt} - \omega I_{Sq1}\frac{L_{Sarm}}{2} = V_{Sd1} - E_{Sd1} \\ L_S\frac{dI_{Sq1}}{dt} + \omega I_{Sd1}\frac{L_{Sarm}}{2} = V_{Sq1} - E_{Sq1} \end{cases} \tag{6.41}$$

Vector control can be divided into the inner loop and outer loop control. The outer loop is used to produce the reference I_{Sd1_ref} and I_{Sq1_ref}, which are utilised by the inner loop control to regulate the converter's control waveform. According to figure 6.7 and equation (6.41), the control waveform based on the *dq* synchronous reference frame can be expressed as:

$$\begin{cases} E_{Sd1} = V_{Sd1} - \left(K_p + \frac{K_i}{s}\right)\left(I_{Sd1_{ref}} - I_{Sd1}\right) + \omega L_S I_{Sq1} \\ E_{Sq1} = V_{rq1} - \left(K_p + \frac{K_i}{s}\right)\left(I_{Sq1\_ref} - I_{Sq1}\right) - \omega L_S I_{Sd1} \end{cases} \tag{6.42}$$

where k_p is the proportional constant which is used to improve the transient response of the control system, and k_i is the integral constant of the PI controller.

However, the three secondary decoupled phases can also be controlled independently with the control strategy shown in figure 6.8. The main advantage of this control strategy is its ability to regulate decoupled phases in the secondary side independently by fluctuations in the

corresponding decoupled phases, which leads to better control results. This is illustrated in figure 6.8, where each phase has its control system which does not affect the other phases. As the control system of each phase is similar to figure 6.7, therefore no further detailed derivation is presented here.

It is worth noting that the control strategies presented above could control the power transferred from the primary to the secondary side (from the low voltage to the high voltage side) for the proposed converter, which means that the primary three-phase MMC is operated in the mode of inverter, and the secondary one-leg MMC-based cascaded converter is operated in the mode of rectifier. Conversely, when the power is transferred from the secondary to the primary side (from the high voltage to the low voltage side), the primary three-phase MMC is operated in the mode of the rectifier, and the secondary one-leg MMC based cascaded converter is operated in the mode of the inverter. Because the control strategies for the proposed converter to transfer the power from the secondary to the primary side (from the high voltage to the low voltage side) have a derivation process similar to the above, and the proposed converter is used to transfer the power from the primary to the secondary side (from the low voltage to the high voltage side) in this project, therefore no further details need to be given at here.

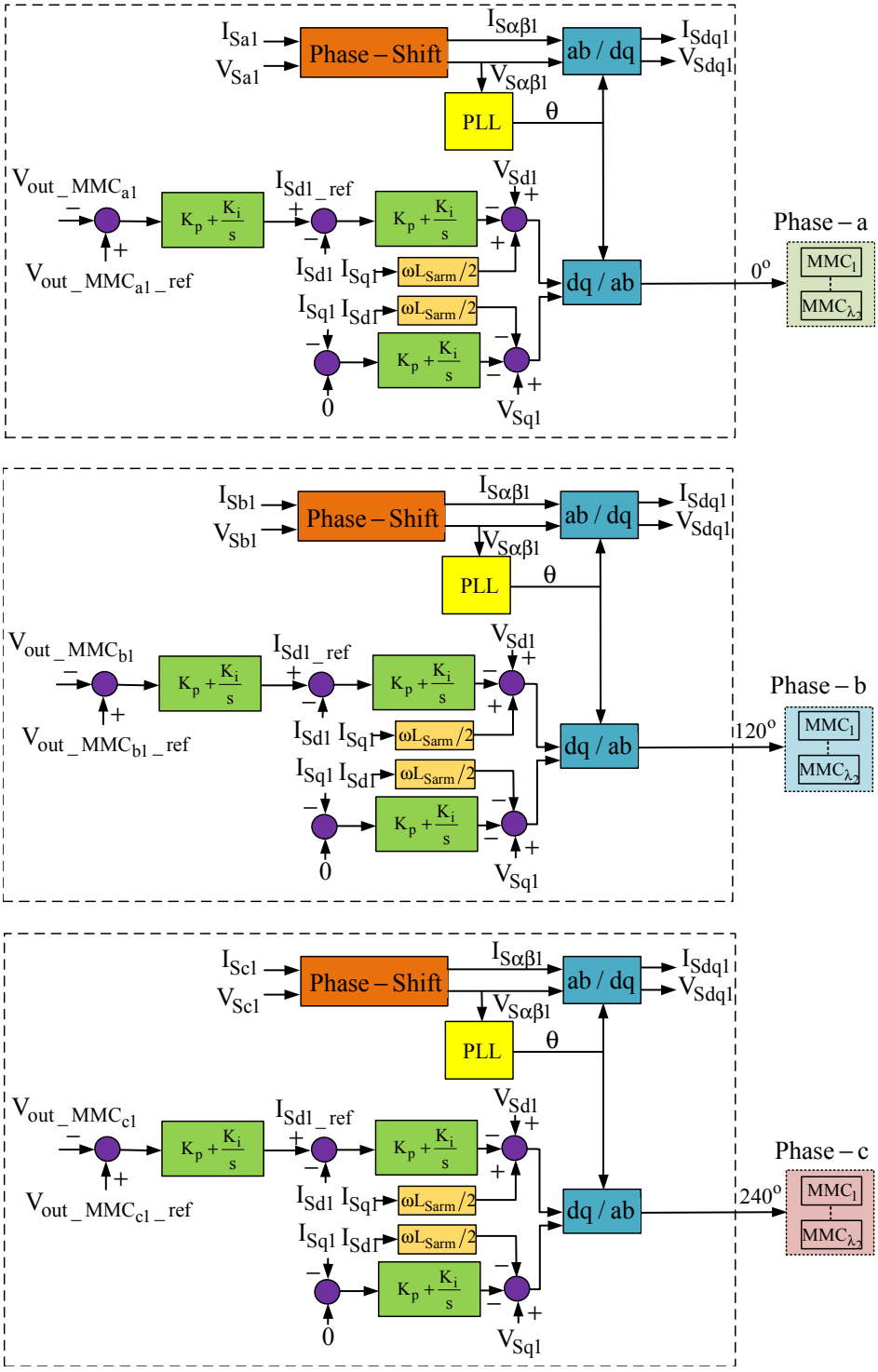


Figure 6.8 Individual control system for the secondary decoupled phases at the secondary side.

6.6 Simulation Results

To validate the theoretical analysis and assess the effectiveness of the proposed converter, a simulation model rated at 12 MW was developed using MATLAB/SIMULINK software with the parameters listed in table 6.1. In this work, each phase of the MMC converter at the primary side was constructed with five half-bridge SMs per arm. On the secondary side, each decoupled phase has two one-leg MMC rectifier modules which are connected in series. Moreover, each one-leg MMC rectifier module consists of five half-bridge SMs per arm. In order to demonstrate the bidirectional power transmission capability of the proposed converter, the following simulation results are divided into two sections including 1) power transferred from the primary to the secondary side (from the low voltage to the high voltage side); and 2) power transferred from the secondary to the primary side (from the high voltage to the low voltage side). It is worth noting that, since the proposed converter is just used to transfer the power from the primary to secondary side (from the low voltage to the high voltage side) in this project, therefore only some of the typical voltage and current waveforms are selected to show the bidirectional power transmission capability of the proposed converter when the power is transferred from the secondary to the primary side (from the high voltage to the low voltage side).

Table 6.1 Simulation parameters

Parameters	Values
Rated power	12MW
Primary DC voltage	15kV
Secondary DC voltage	150kV
Output load resistor	1900Ω
Submodule numbers of primary MMC per arm	5
Submodule numbers of secondary one-leg MMC module per arm	5
Numbers of one-leg MMC module at secondary	6
Transformer ratio	1:3
Submodule capacitor of primary MMC	3.6mF
Submodule capacitor of secondary one-leg MMC module	3.6mF
The inductance of primary MMC per arm	1mH
The inductance of secondary one-leg MMC module per arm	1mH
Output capacitor	3mF
Switching frequency	2000Hz
AC fundamental frequency	400Hz

A) Power transferred from primary to secondary side (from low voltage to high voltage side):

The primary three-phase AC voltage and the decoupled voltages at the secondary side are presented in figures 6.9-6.12, where two identical decoupled voltages at the secondary side are obtained from each primary input phase. It should also be noted that the other pairs of the secondary decoupled voltages are shifted by 120-degrees, as illustrated in figures 6.10-6.12. It is worth mentioning that higher numbers of windings (with more one-leg MMC modules) at each secondary decoupled phase can be considered if a higher voltage is required at the output side. The primary three-phase AC current at the primary and the decoupled currents at the secondary side are shown in figures 6.13 and 6.14. Similar to the voltage waveforms, two identical decoupled currents at the secondary side are obtained from each primary input phase.

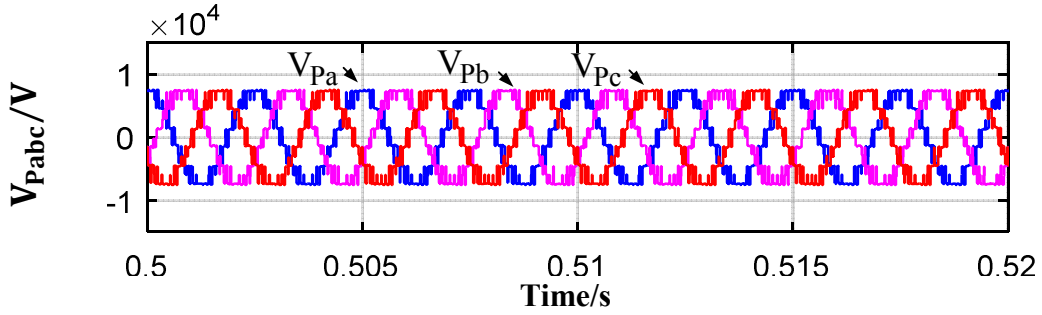


Figure 6.9 Transformer primary three-phase AC voltages.

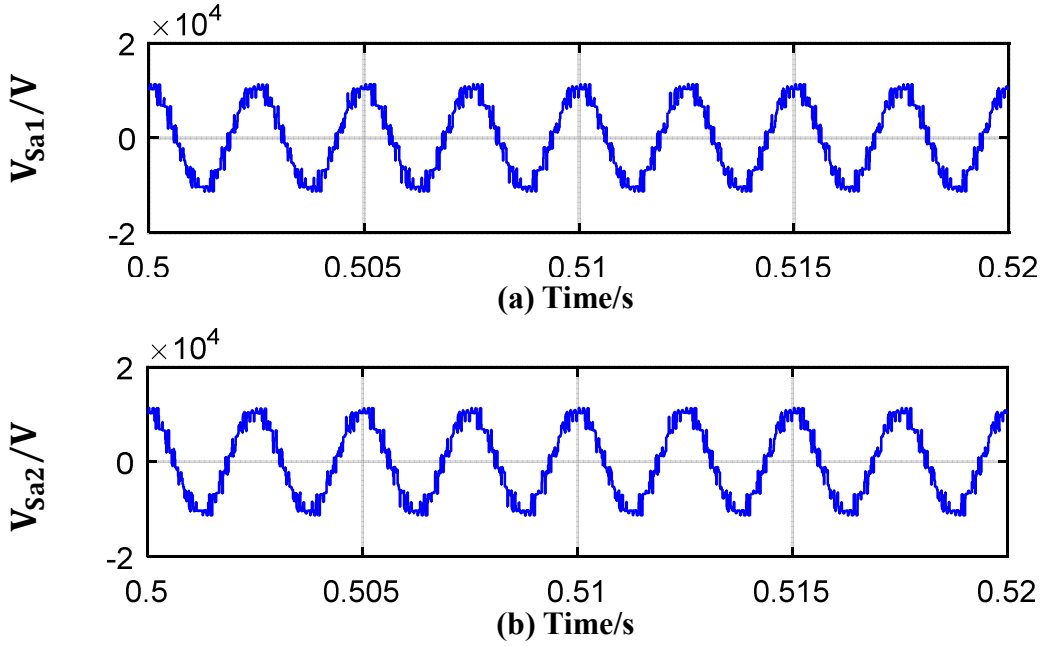


Figure 6.10 Transformer secondary side Phase-a AC voltage waveforms: (a) module-one; (b) module-two.

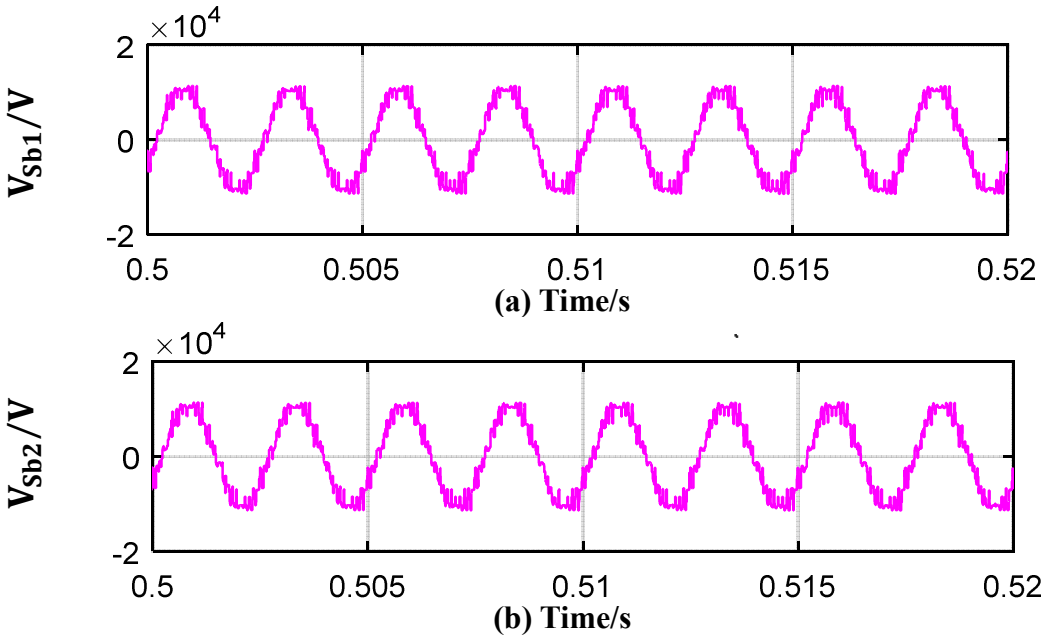


Figure 6.11 Transformer secondary side Phase-b AC voltage waveforms: (a) module-one; (b) module-two.

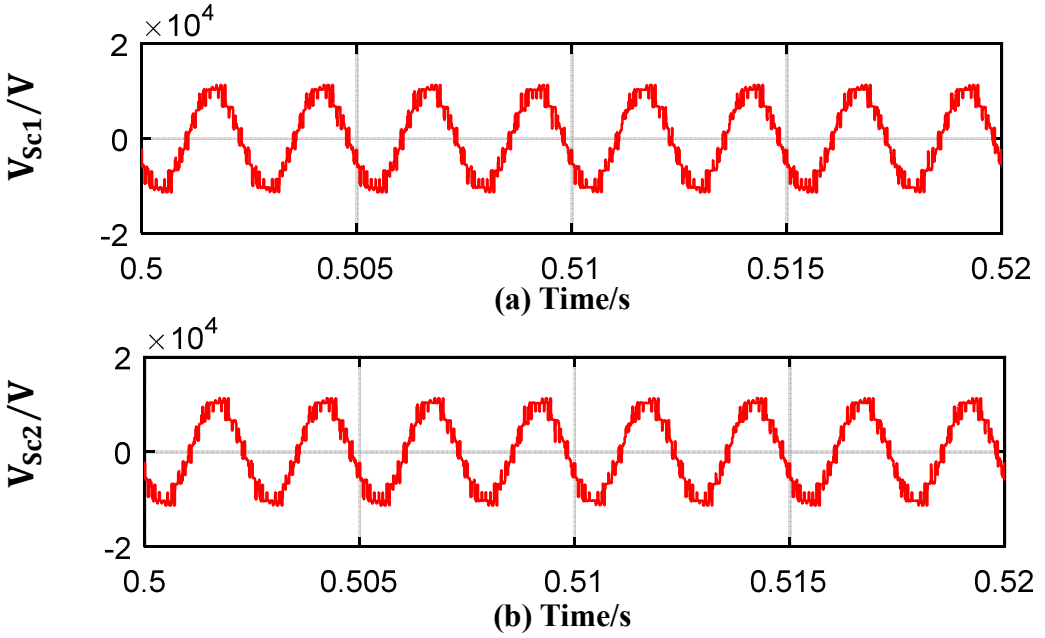


Figure 6.12 Transformer secondary side Phase-c AC voltage waveforms: (a) module-one; (b) module-two.

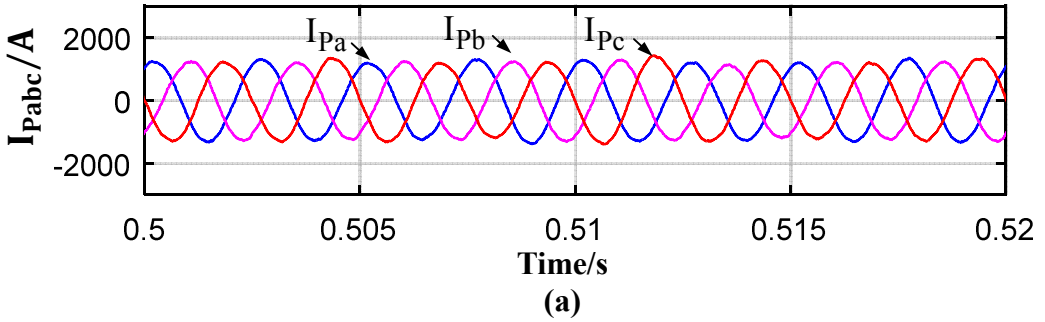


Figure 6.13 Transformer primary three-phase AC currents.

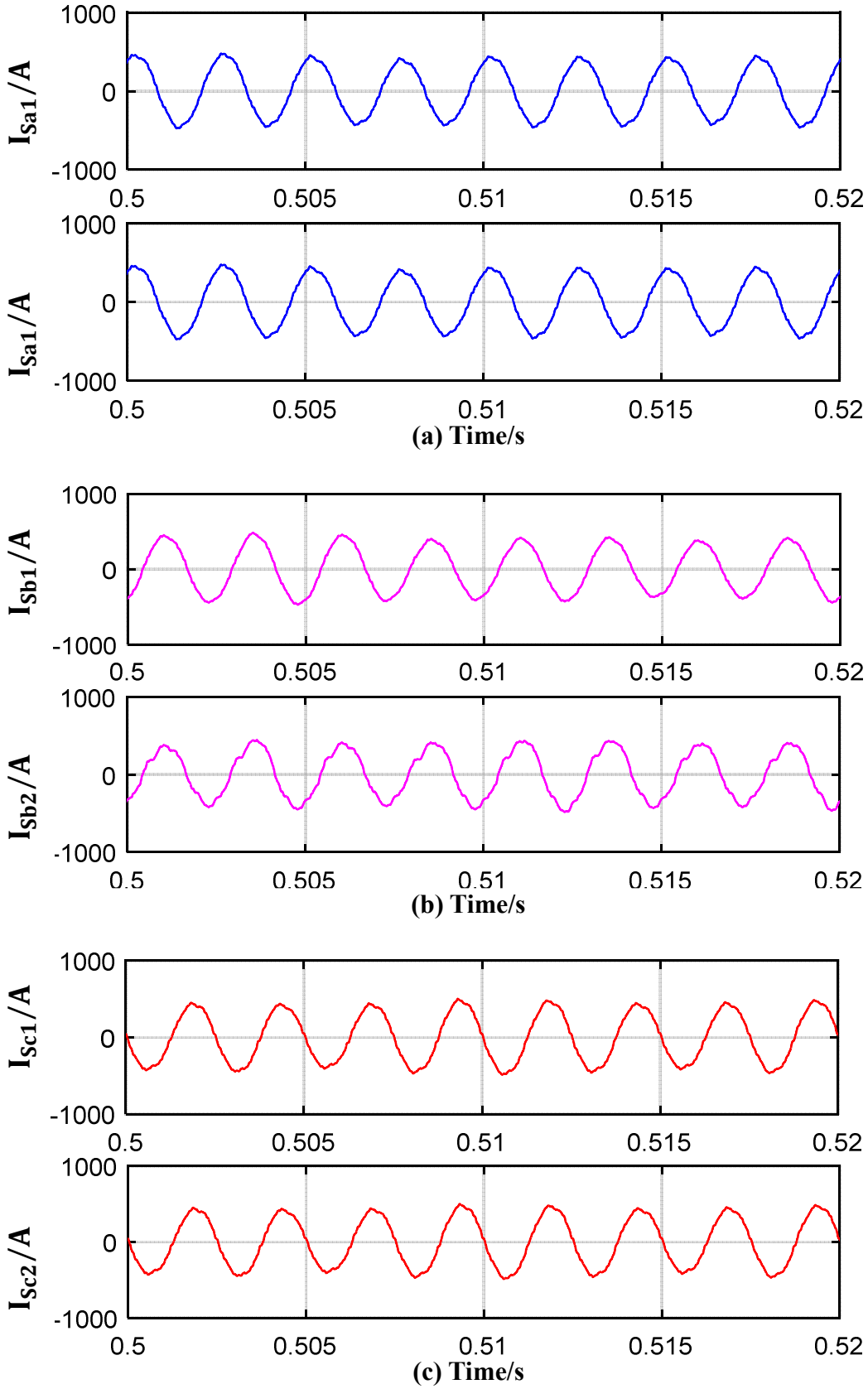


Figure 6.14 Transformer current waveforms: (a) secondary side Phase-a module-one and module-two AC current; (b) secondary side Phase-b module-one and module-two AC current; (c) secondary side Phase-c module-one and module-two AC current.

The performance of the balance control method is also confirmed and demonstrated in figure 6.15 taking Phase-a as an example. The capacitor voltages of the SMs are tightly controlled around their reference values as shown in figure 6.15(a) for the capacitor voltage of the upper arm SMs and figure 6.15(b) for the capacitor voltage of the lower arm SMs, each at 15kV/5. Similarly, the same voltage balance control method is applied to the one-leg MMC modules on the secondary side. As an example, figure 6.16 (a) and (b) show the upper and lower arm SM voltages of MMC_{a_one} of the decoupled Phase-a controlled at 150kV/6*5 (where 6 is the number of one-leg MMC modules and 5 is the number of SMs per arm in the one-leg MMC rectifier module).

The secondary side output DC voltage and current and the power of the proposed converter are shown in figure 6.17 where, with the abovementioned design as shown in table 6.1, the secondary output DC voltage is maintained at around 150kV.

The performance of the proposed control strategy was further investigated and confirmed with a 25% step change in the output power. Figure 6.18 shows the dynamic response of the controller when the load is changed at $t = 1s$, and it can be seen that the output DC current output power decreases rapidly; however, the output DC voltage and primary three-phase AC voltage are maintained at constant levels, which confirms the effectiveness of the proposed control system.

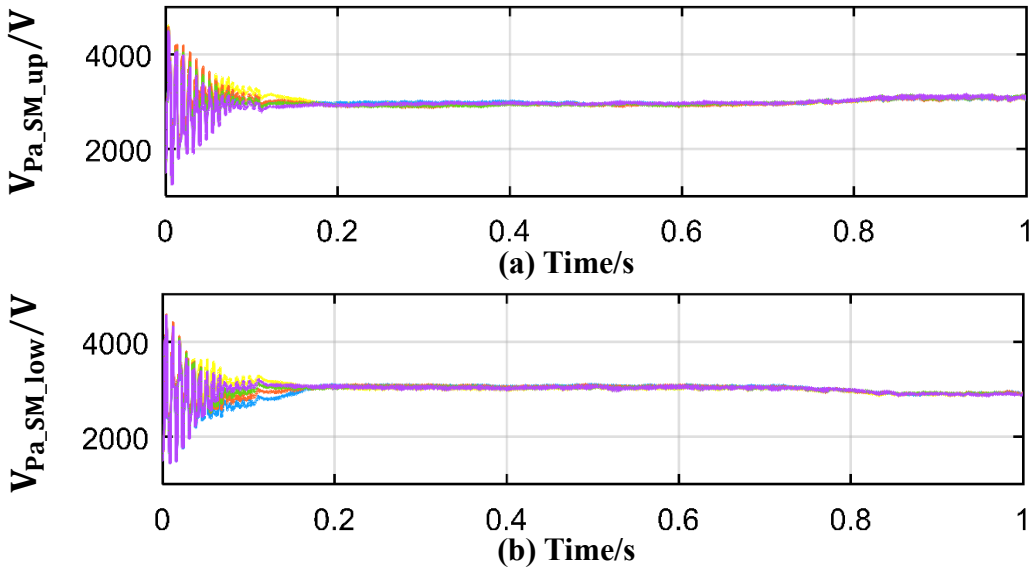


Figure 6.15 Primary Phase-a: (a) upper arm SM voltages; (b) lower arm SM voltages.

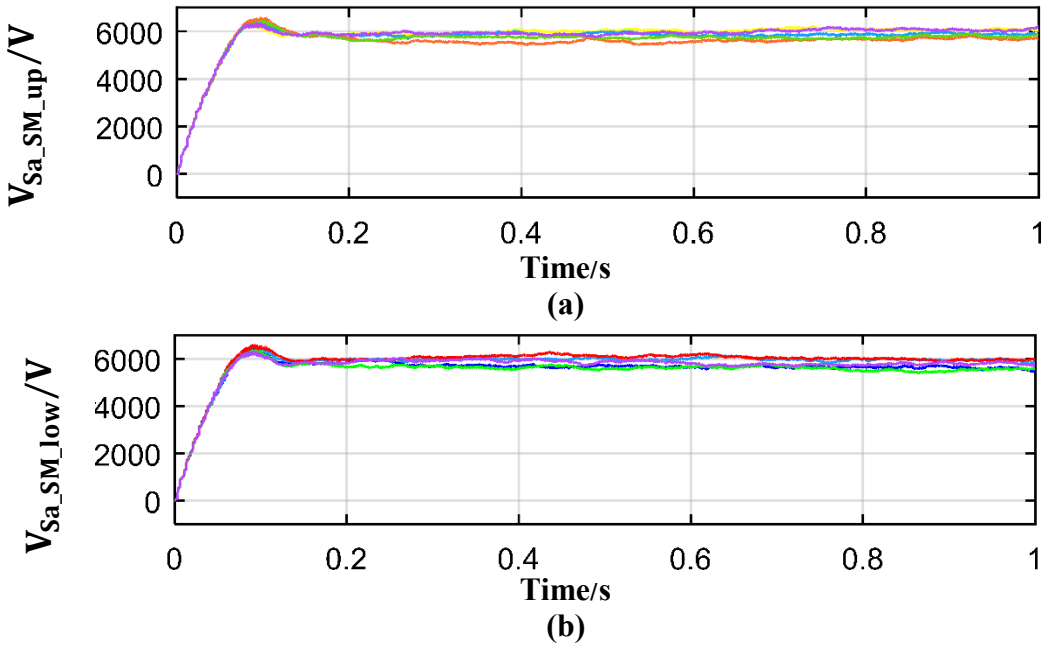


Figure 6.16 Secondary decoupled Phase-a one-leg MMC rectifier module-one: (a) upper arm SM voltages; (b) lower arm SM voltages.

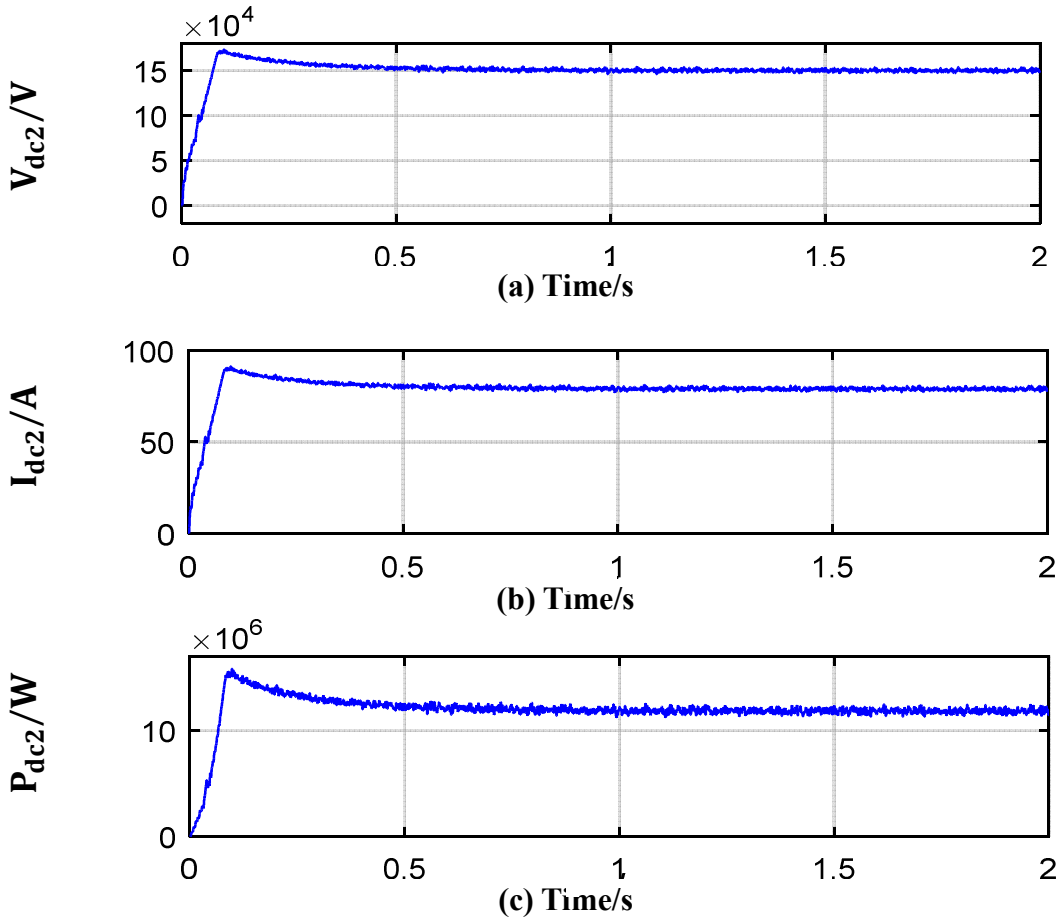


Figure 6.17 Output waveforms of the proposed converter under steady-state operation: (a) output DC voltage; (b) output DC current; (c) output power.

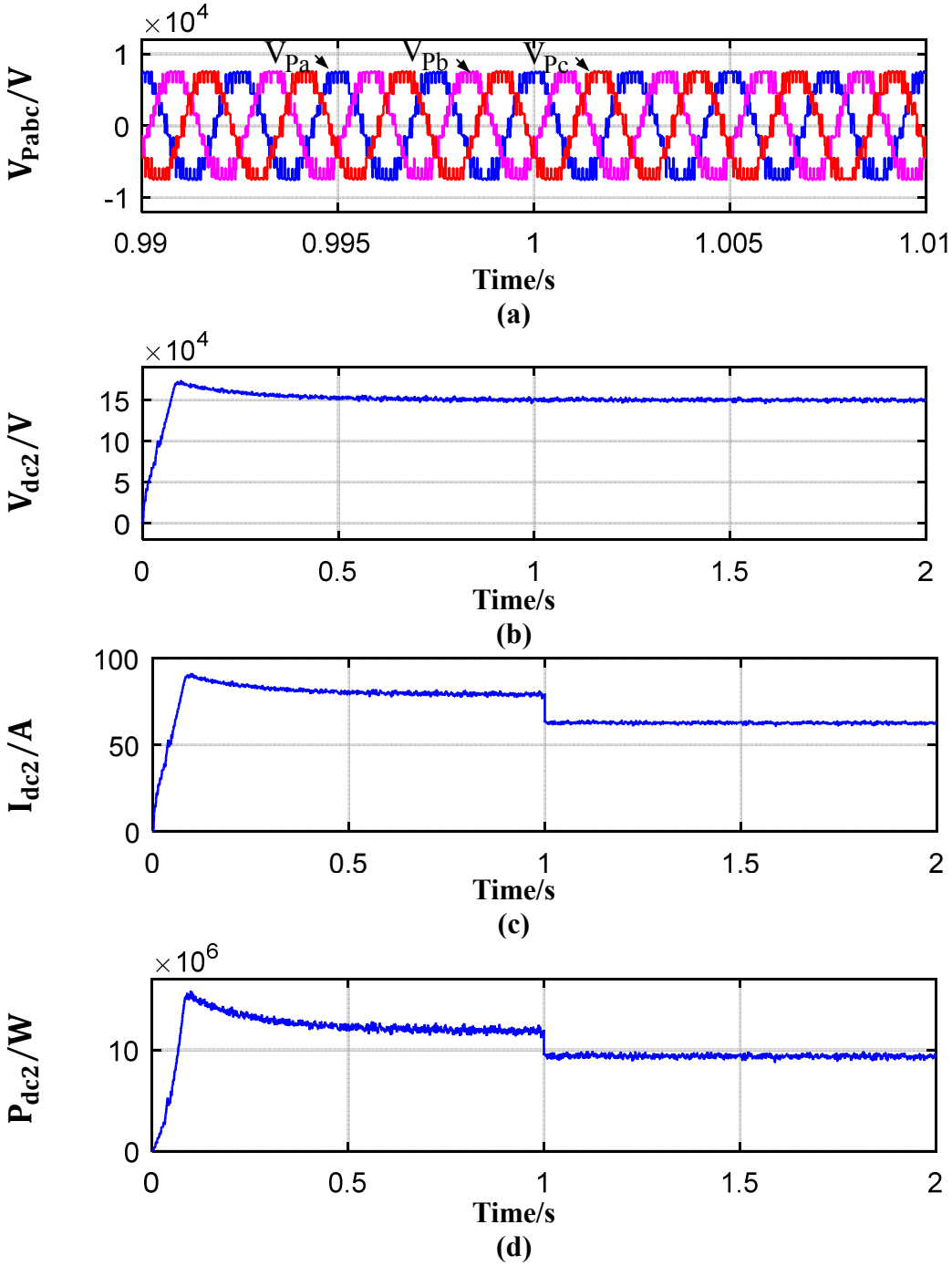


Figure 6.18 Output waveforms of the proposed converter under a 25% step change at 1s: (a) transformer primary three-phase AC voltages; (b) output DC voltage; (b) output DC current; (d) output power.

B) Power transferred from secondary to the primary side (from high voltage to low voltage side):

Figure 6.19 depicts the primary three-phase AC voltage and current waveforms of the proposed converter. The DC output voltage and current and power are shown in figure 6.20

where, with the abovementioned design shown in table 6.1, the output DC voltage is maintained at around 15kV.

The performance of the proposed control strategy was further investigated and confirmed with a 25% step change in the output load. Figure 6.21 shows the dynamic response of the controller when the load changes at $t = 1s$, and it can be seen that the output DC and output power decrease rapidly; however, the output DC voltage is maintained at a constant level, which again confirms the effectiveness of the proposed control system.

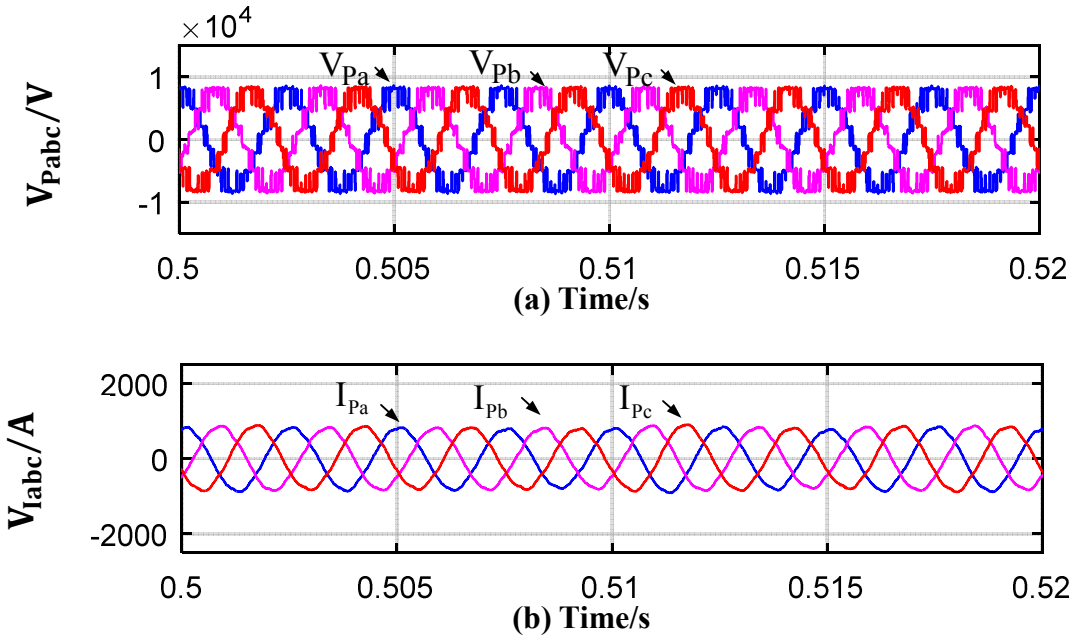
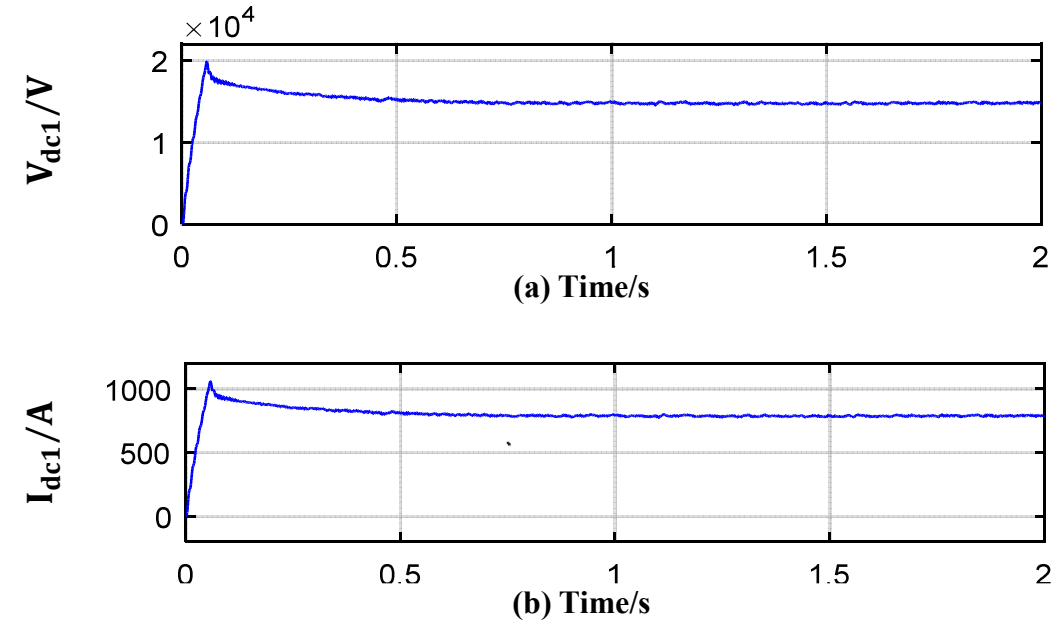


Figure 6.19 Transformer primary side three-phase waveforms: (a) voltage (b) current.



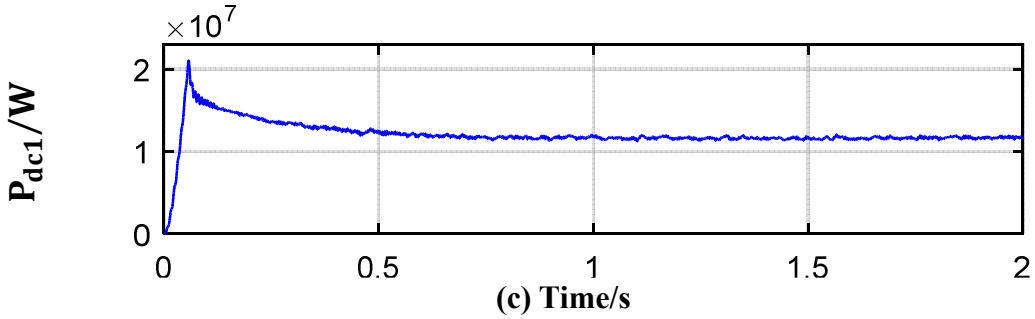


Figure 6.20 Output waveforms of the proposed converter under steady-state operation: (a) primary output DC voltage; (b) primary output DC current; (c) primary output power.

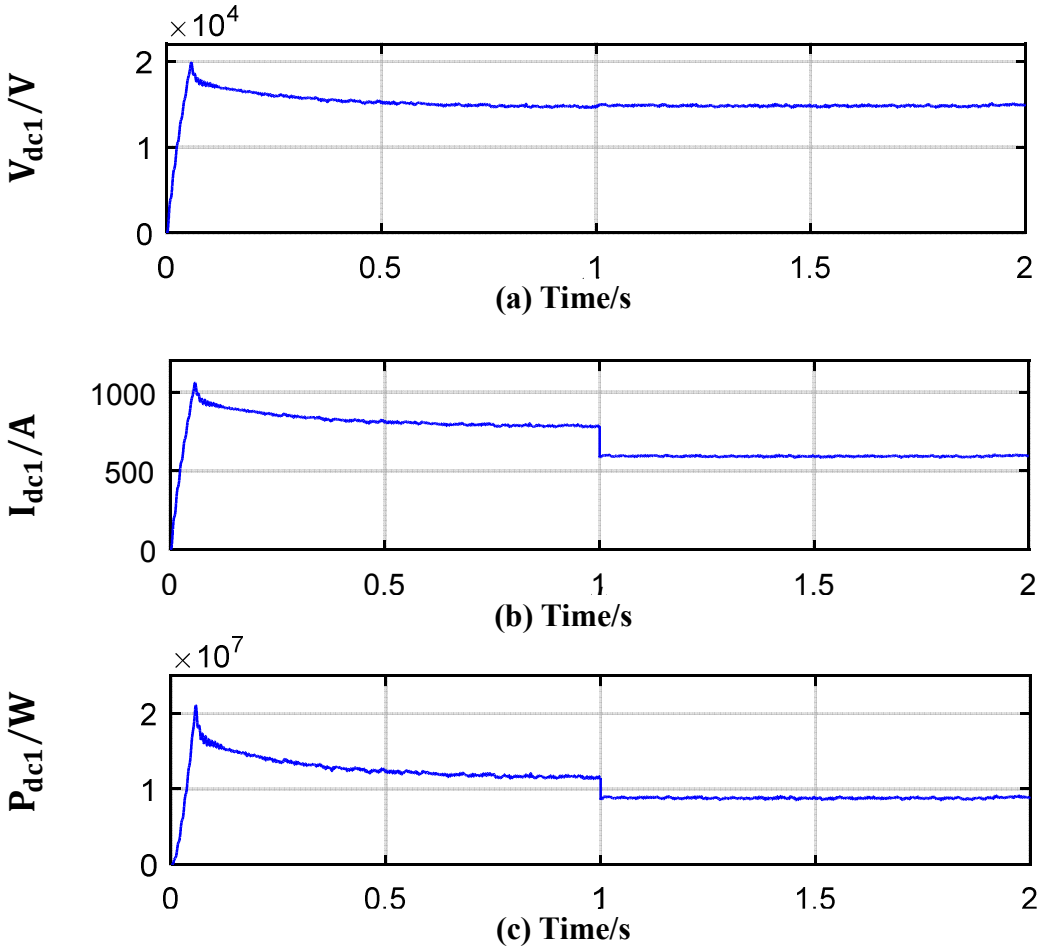


Figure 6.21 Output waveforms of the proposed converter under a 25% step change at 1s: (a) primary output DC voltage; (b) primary output DC current; (c) primary output power.

6.7 Summary

Chapter 6 has proposed a bidirectional three-phase modular DC/DC converter. To understand the operating characteristics of the proposed converter, a detailed description of the circuit configuration, the derivation of the mathematical model and analysis of the output power characteristics of the proposed converter are presented and thoroughly discussed. Moreover, two different *dq* vector control strategies are developed for the primary and secondary sides of the proposed converter. Finally, the performance of the proposed converter and its control strategy are validated through various simulations.

Chapter 7. Calculation of Losses and Comparison of Topologies

7.1 Introduction

It is very important to demonstrate the superiority of the proposed converters compared to other competitive DC/DC converters. In addition to comparing the structures of the circuit topologies, evaluations of the losses involved, and system efficiency are essential as well. Therefore, Chapter 7 presents a detailed analysis and calculation of different losses in the proposed converter and compares them with those of other competitive topologies.

7.2 Calculation of Losses in the IGBT Modules of the MMC

Since all of the converters proposed in this dissertation employ an MMC at the primary side, therefore the calculation of losses is based on the inversion mode of the MMC, although the same method can be used for both rectifier and inverter operating modes. To simplify the analysis, the following assumptions are made: 1) only the fundamental component of the AC output current of the converter is considered in the power loss calculation; and 2) power is equally shared between the three phases of the MMC. Furthermore, the current flow characteristics of cascaded DC/DC converters, such as input series output series (ISOS) or input parallel output series (IPOS) systems, have been fully introduced and analyzed elsewhere [29-40] [66-74]. Hence no further details are given here.

It is well known that, in the three-phase MMC, the input DC current, I_{dc1} will be evenly distributed between the three legs, and the AC output currents of each phase are evenly distributed between the upper and lower arms as illustrated in figure 7.1(a) [95-98]. Taking Phase-a as an example, its upper arm current can be expressed as:

$$I_{aU}(t) = \frac{I_{dc1}}{3} + \frac{1}{2}\hat{I}_{Pa}\sin(\omega t - \delta) \tag{7.1}$$

where $\hat{I}_{Pa}$ is the peak value of the Phase-a AC current, and δ is the phase shift angle between the AC voltage and current of Phase-a.

Since CPS-PWM is utilized to control the switches in the proposed MMC converter, therefore the duty cycle (τ) of all switches is defined as follows [115]:

$$\tau(t) = \frac{1+M_1 \sin(\omega t)}{2} \tag{7.2}$$

where M_1 is the modulation index, and ω is the fundamental angular frequency of the output AC phase voltage.

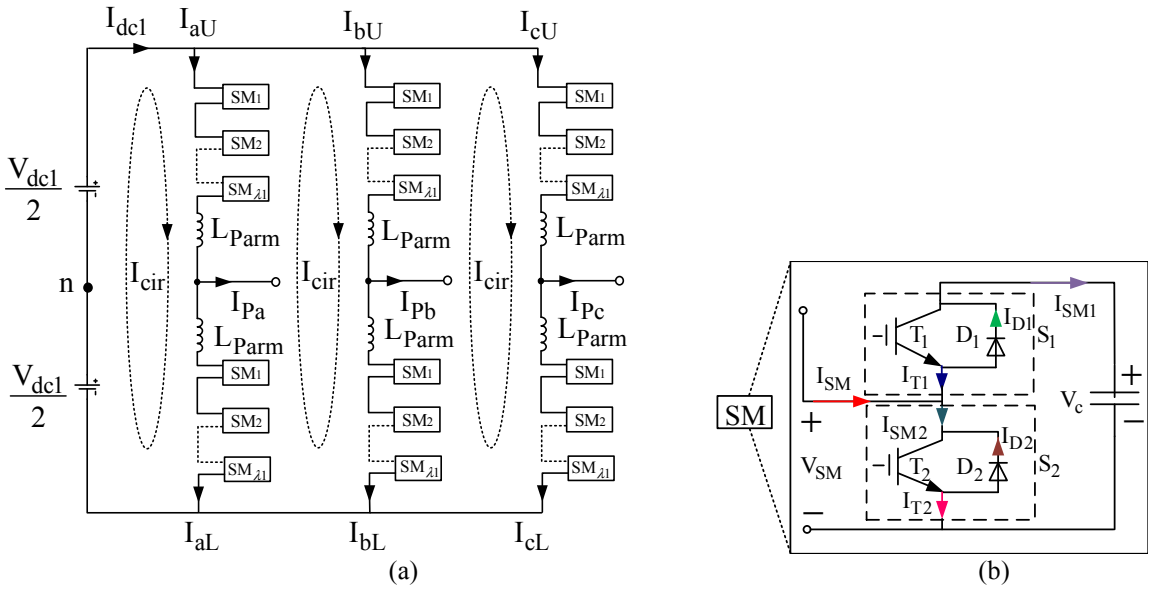


Figure 7.1 Three-phase MMC: (a) current distribution in the arms of the three-phase MMC; (b) current directions in the half-bridge SM.

Table 7.1 SM states of MMC

State	T_1	T_2	I_{SM}	V_{SM}	Submodule
1	ON	OFF	> 0	V_c	Charging
2	ON	OFF	< 0	V_c	Discharging
3	OFF	ON	> 0	0	By-Passed
4	OFF	ON	< 0	0	By-Passed

Table 7.1 lists the possible operating modes of the MMC's submodule (SM), where the current directions are schematically presented in figure 7.1(b) [115]. Taking the upper arm of Phase-a as an example, each SM is either inserted or by-passed, so that the voltage of Phase-a is either increased or decreased by the SM capacitor voltage, V_c. When the modulation signal is greater than the carrier signal, T_2 is turned on and T_1 is turned off, which means that the SM is by-passed. However, on the other hand, when the modulation signal is less than the carrier signal, T_2 is turned off and T_1 is turned on, which means that the SM is inserted in the circuit.

Therefore, if the carrier cycle is T_c, then the conduction time of T_2 when the SM is by-passed is equal to $\tau(t) \cdot T_c$. On the other hand, the conduction time T_1 is equal to $[1-\tau(t)] \cdot T_c$ when the SM is inserted. Therefore, based on the above analysis, the current flowing through the upper and lower IGBT modules S_1 and S_2 respectively can be expressed as:

$$I_{SM1} = [1-\tau(t)] * I_{aP}(t) \tag{7.3}$$

$$I_{SM2} = \tau(t) * I_{aP}(t) \tag{7.4}$$

where $I_{aU}(t)$ is the upper arm current of Phase-a.

Substituting (7.1) and (7.2) into (7.3) and (7.4) yields:

$$I_{SM1} = \frac{1-M_1 \sin(\omega t)}{2} * \left[\frac{I_{dc1}}{3} + \frac{1}{2}\hat{I}_{Pa} \sin(\omega t - \delta)\right] \tag{7.5}$$

$$I_{SM2} = \frac{1+M_1 \sin(\omega t)}{2} * \left[\frac{I_{dc1}}{3} + \frac{1}{2}\hat{I}_{Pa} \sin(\omega t - \delta)\right] \tag{7.6}$$

From (7.5) and (7.6), the effective and average values of the currents flowing through the switches and diodes of SM can be derived as follows:

1) Average current flowing through the diode D_1:

$$I_{D1\_avg} = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{SM1} d\omega t \tag{7.7}$$

Substituting (7.5) into (7.7) yields:

$$I_{D1\_avg} = \frac{1}{2\pi}\left[\frac{\hat{I}_{Pa}}{2} + \frac{\pi I_{dc1}}{6} - \frac{I_{dc1}M_1 \cos(\delta)}{3} - \frac{\pi \hat{I}_{Pa}M_1 \cos(\delta)}{8}\right] \tag{7.8}$$

2) Square of the effective current flowing through the diode D_1:

$$I_{D1\_rms}{}^2 = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{SM1}{}^2 d\omega t \tag{7.9}$$

Substituting (7.5) into (7.9) yields:

$$I_{D1\_rms}{}^2 = \frac{1}{2\pi}\left[\frac{\hat{I}_{Pa}I_{dc1}}{6} + \frac{\pi \hat{I}_{Pa}{}^2}{32} + \frac{\pi I_{dc1}{}^2}{36} + \frac{\hat{I}_{Pa}I_{dc1}M_1{}^2}{12} - \frac{\hat{I}_{Pa}{}^2 M_1 \cos(\delta)}{6} - \frac{I_{dc1}{}^2 M_1 \cos(\delta)}{9} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2}{64} + \frac{\pi I_{dc1}{}^2 M_1{}^2}{72} + \frac{\hat{I}_{Pa}I_{dc1}M_1{}^2 \cos(2\delta)}{36} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2 \cos(2\delta)}{128} + \frac{\pi \hat{I}_{Pa}I_{dc1}M_1 \cos(\delta)}{12}\right] \tag{7.10}$$

3) Average current flowing through the switch T_1:

$$I_{T1\_avg} = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{SM1} d\omega t \tag{7.11}$$

Substituting (7.5) into (7.11) yields:

$$I_{T1\_avg} = -\frac{1}{2\pi}\left[\frac{\hat{I}_{Pa}}{2} - \frac{\pi I_{dc1}}{6} - \frac{I_{dc1}M_1 \cos(\delta)}{3} + \frac{\pi \hat{I}_{Pa}M_1 \cos(\delta)}{8}\right] \tag{7.12}$$

4) Square of the effective current flowing through the switch T_1:

$$I_{T1\_rms}{}^2 = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{SM1}{}^2 d\omega t \tag{7.13}$$

Substituting (7.5) into (7.13) yields:

$$I_{T1\_rms}{}^2 = \frac{1}{2\pi}\left[\frac{\pi \hat{I}_{Pa}{}^2}{32} - \frac{\hat{I}_{Pa} I_{dc1}}{6} + \frac{\pi I_{dc1}{}^2}{36} - \frac{\hat{I}_{Pa} I_{dc1} M_1{}^2}{12} + \frac{\hat{I}_{Pa}{}^2 M_1 \cos(\delta)}{6} + \frac{I_{dc1}{}^2 M_1 \cos(\delta)}{9} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2}{64} + \frac{\pi I_{dc1}{}^2 M_1{}^2}{72} - \frac{\hat{I}_{Pa} I_{dc1} M_1{}^2 \cos(2\delta)}{36} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2 \cos(2\delta)}{128} - \frac{\pi \hat{I}_{Pa} I_{dc1} M_1 \cos(\delta)}{12}\right] \tag{7.14}$$

5) Average current flowing through the switch T_2:

$$I_{T2\_avg} = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{SM2} d\omega t \tag{7.15}$$

Substituting (7.6) into (7.15) yields:

$$I_{T2\_avg} = \frac{1}{2\pi}\left[\frac{\hat{I}_{Pa}}{2} + \frac{\pi I_{dc1}}{6} + \frac{I_{dc1} M_1 \cos(\delta)}{3} + \frac{\pi \hat{I}_{Pa} M_1 \cos(\delta)}{8}\right] \tag{7.16}$$

6) Square of the effective current flowing through the switch T_2:

$$I_{T2\_rms}{}^2 = \frac{1}{2\pi}\int_{\delta}^{\delta+\pi} I_{SM2}{}^2 d\omega t \tag{7.17}$$

Substituting (7.6) into (7.17) yields:

$$I_{T2\_rms}{}^2 = \frac{1}{2\pi}\left[\frac{\hat{I}_{Pa} I_{dc1}}{6} + \frac{\pi \hat{I}_{Pa}{}^2}{32} + \frac{\pi I_{dc1}{}^2}{36} + \frac{\hat{I}_{Pa} I_{dc1} M_1{}^2}{12} + \frac{\hat{I}_{Pa}{}^2 M_1 \cos(\delta)}{6} + \frac{I_{dc1}{}^2 M_1 \cos(\delta)}{9} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2}{64} + \frac{\pi I_{dc1}{}^2 M_1{}^2}{72} + \frac{\hat{I}_{Pa} I_{dc1} M_1{}^2 \cos(2\delta)}{36} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2 \cos(2\delta)}{128} + \frac{\pi \hat{I}_{Pa} I_{dc1} M_1 \cos(\delta)}{12}\right] \tag{7.18}$$

7) Average current flowing through the diode D_2:

$$I_{D2\_avg} = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{SM2} d\omega t \tag{7.19}$$

Substituting (7.6) into (7.19) yields:

$$I_{D2\_avg} = -\frac{1}{2\pi}\left[\frac{\hat{I}_{Pa}}{2} - \frac{\pi I_{dc1}}{6} + \frac{I_{dc1} M_1 \cos(\delta)}{3} - \frac{\pi \hat{I}_{Pa} M_1 \cos(\delta)}{8}\right] \tag{7.20}$$

8) The square of the effective current flowing through the diode D_2 is:

$$I_{D2\_rms}{}^2 = \frac{1}{2\pi}\int_{\delta+\pi}^{\delta+2\pi} I_{SM2}{}^2 d\omega t \tag{7.21}$$

Substituting (7.6) into (7.21) yields:

$$I_{D2\_rms}{}^2 = \frac{1}{2\pi}\left[\frac{\pi \hat{I}_{Pa}{}^2}{32} - \frac{\hat{I}_{Pa} I_{dc1}}{6} + \frac{\pi I_{dc1}{}^2}{36} - \frac{\hat{I}_{Pa} I_{dc1} M_1{}^2}{12} - \frac{\hat{I}_{Pa}{}^2 M_1 \cos(\delta)}{6} - \frac{I_{dc1}{}^2 M_1 \cos(\delta)}{9} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2}{64} + \frac{\pi I_{dc1}{}^2 M_1{}^2}{72} - \frac{\hat{I}_{Pa} I_{dc1} M_1{}^2 \cos(2\delta)}{36} + \frac{\pi \hat{I}_{Pa}{}^2 M_1{}^2 \cos(2\delta)}{128} + \frac{\pi \hat{I}_{Pa} I_{dc1} M_1 \cos(\delta)}{12}\right] \tag{7.22}$$

The average conduction losses of the IGBT modules are calculated over one fundamental AC

period using the above-derived average/effective currents as follows:

$$\overline{P_{D\_con}} = I_{D\_avg}V_{D\_0} + r_{D\_0}I_{D\_rms}^2 \tag{7.23}$$

$$\overline{P_{T\_con}} = I_{T\_avg}V_{T\_0} + r_{T\_0}I_{T\_rms}^2 \tag{7.24}$$

where $\overline{P_{D\_con}}$ and $\overline{P_{T\_con}}$ are the SM's diode and switch average conduction losses respectively within one fundamental AC period, V_{D_0} and V_{T_0} are the threshold voltages of the diode and the switch respectively, and r_{D_0} and r_{T_0} are the forward conduction resistance of the diode and switch respectively. It is worth noting that the blocking state losses are much smaller compared with the conduction losses, and hence they are ignored in this analysis.

According to previous studies [120], the turn-on/off switching losses are approximately proportional to the average current flowing through the switch; therefore, the switching losses over one fundamental AC period can be calculated by:

$$P_{sw} = f_{sw}(E_{on} + E_{off})\frac{V_c I_{T\_avg}}{V_{T\_ref}I_{T\_ref}} \tag{7.25}$$

$$P_{rec} = f_{sw}E_{rec}\frac{V_c I_{D\_avg}}{V_{D\_ref}I_{D\_ref}} \tag{7.26}$$

where f_{sw} is the switching frequency, E_{on} and E_{off} are the switch's turn-on and turn-off energy losses respectively, V_{T_ref} and I_{T_ref} are the reference voltage and current of the switch respectively, E_{rec} is the reverse recovery energy losses of the diode, and V_{D_ref} and I_{D_ref} are the reference voltage and current of the diode respectively. It should be noted that the values of E_{on}, E_{off}, V_{T_ref}, I_{T_ref}, E_{rec}, V_{D_ref}, and I_{D_ref} can be obtained from the datasheet of a particular device.

Note that the IGBT module includes the IGBT part and associated anti-parallel diode part and each half-bridge-based SM includes two IGBT modules; therefore, the total losses of an individual IGBT module can be expressed as:

$$P_{IGBT} = P_{D\_con} + P_{T\_con} + P_{sw} + P_{rec} \tag{7.27}$$

It is worth noting that the losses of the upper and lower IGBT modules in the half-bridge-based SM are different.

Similarly, the total losses of an individual diode at the secondary side can be calculated using (7.23) and (7.26), and can be expressed as:

$$P_{Diode} = P_{D\_con} + P_{rec} \tag{7.28}$$

7.3 Calculation of Losses in the Medium Frequency Transformer

The design of offshore platforms is constrained by the size and weight of the converter, which is largely influenced by the operating frequency. While a high switching frequency can effectively bring the size down, this will lead to undesirable characteristics such as higher core and winding losses as well as higher switching losses. Therefore, care must be taken when designing the transformer in terms of the operating frequency. In this dissertation, a frequency of 400Hz is selected based on the analysis and the trade-off study presented elsewhere [117][121-126].

As the core objective of this work is to propose a different converter topology, and because the detailed design of a transformer is beyond the scope of this dissertation, this chapter only presents a simplified process of transformer design and calculation of losses, which is sufficient to evaluate the losses of the transformer. It is worth noting that the detailed design process of a medium frequency transformer (MFT) is shown in Chapter 8.

7.3.1 *Medium frequency transformer design considerations*

There are various aspects that need to be considered when designing an MFT. These include frequency, core material, and insulation material.

1) Simplified MFT model [127]:

An indication of the influence of frequency on transformer size can be realized through the general transformer design model presented by (7.29).

$$A_w \cdot A_c = \frac{1}{f_{AC}} \cdot \frac{V_{rms} \cdot I_{rms}}{K_v \cdot K_u \cdot J \cdot B_{pk}} \tag{7.29}$$

where A_w and A_c are the cross-sectional area of the magnetic core and the winding respectively, the product of $V_{rms} \cdot I_{rms}$ represents the rated power, f_{AC} is the functional AC frequency, and J and B_{pk} represent the current density in the winding conductors and the maximum allowable core flux density respectively. K_v is a constant related to the voltage waveform (which 4.4 for a sinusoidal waveform and 4 for a square waveform) [127], and K_u

is the window utilization ratio which is generally chosen from between 0.4~0.6 [127].

From (7.29), the product of the core and winding cross-sectional areas can be decreased if the frequency is increased, confirming the benefits that the MFT provides in terms of size, weight and cost when compared with a conventional line frequency transformer [118-120].

2) Core material selection for the MFT

Core materials have a great influence on the MFT's losses, saturation flux density and continuous operating temperature [128]. As an operating frequency of 400 Hz is selected in this project, silicon-steel and amorphous alloy core materials are suitable for low/medium frequency applications. From figure 7.2, one can see that the oriented silicon-steel has a better performance in terms of losses compared to non-oriented silicon-steel when the transformer operates in the low/medium frequency range. However, amorphous alloy core materials have lower losses than any kind of silicon-steel materials, as shown in the same figure. Considering the importance of decreasing the losses from the MFT, the material 'magnetic 2605SA1' [128], which is a type of amorphous alloy material, is selected in this project. It is noting that the detailed lamination thickness of three materials are presented in table 7.2.

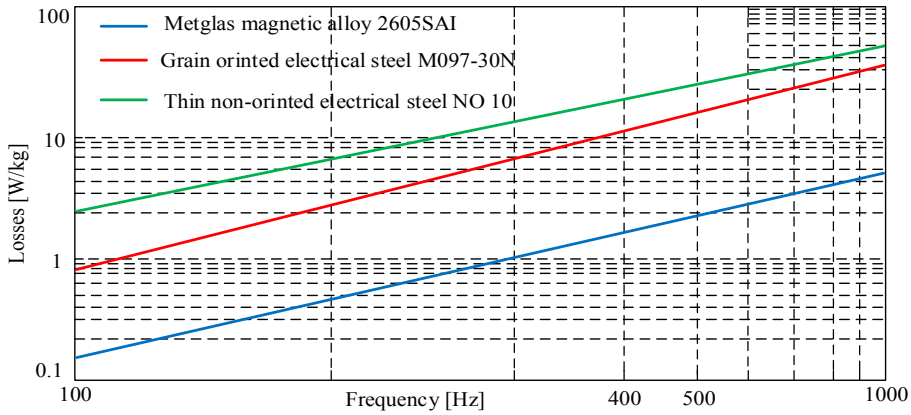


Figure 7.2 Frequency dependency of core losses [128].

Table 7.2 Lamination thickness of three materials [128]

Core material	Lamination thickness
oriented silicon-steel	0.3mm
non-oriented silicon-steel	0.5mm
magnetic 2605SA1	0.025mm

3) Selection of insulation material for the MFT

The proposed converter utilizes an MFT with multiple secondary windings, which involves a multi-layer windings arrangement compared to that in the conventional MFT. Therefore, a more reliable insulation material is required to ensure secure high voltage insulation as well as to enable better thermal management. Epoxy cast resin insulation material exhibits good heat conductivity and high dielectric strength, as shown in table 7.3 [129], and this is, therefore, a good choice.

Table 7.3 Parameters of different insulation materials [129]

Insulation material	Thermal conductivity W/(m·k)	Dielectric strength kV/m	Dielectric constant ε_r
Epoxy resin	0.25	15	3.6
Air	0.03(at 70℃)	3	1.0005
Mica	0.71	11-43	2.5-7
Transformer Oil	0.12	10-15	2.2-2.5
NOMEX	–	27	2.5-4
RTV	1.8	8	–

7.3.2 *Calculation of losses in the transformer*

In general, there are three types of losses in a transformer [2] [130]:

- Copper losses
- Core losses
- Dielectric losses

Copper losses: Copper losses are essentially caused by conductor resistivity and, with skin and proximity effects, these losses increase with frequency. However, using Litz wires greatly reduces these effects, and therefore for this approximate analysis, skin and proximity effects will not be considered [2] [130]. Hence, the copper losses, P_{copper}, are defined as:

$$P_{copper} = RI_{rms}^2 \tag{7.30}$$

where R is the equivalent resistance of the transformer windings and I_{rms} is the effective current flowing through these windings.

Core losses: Core losses include hysteresis and eddy current losses, and these are proportionally influenced by the maximum flux density, which is an important factor in designing a transformer [2] [128]. However, for a given magnetic flux, the flux density is solely determined by the core cross-sectional area. In general, the Steinmetz equation [2] [128] is used to predict core losses, which can be given as follows:

$$P_{core} = kV_{core}{f_{AC}}^{\alpha}B_{pk}^{\beta} \tag{7.31}$$

where P_{core} and V_{core} are the core losses and core volume respectively, B_{pk} is the peak core flux density, and coefficients K, α, and β are determined by the properties of the core material, while f_{AC} is the fundamental AC frequency.

Dielectric losses: These losses are caused by the movements of atoms when an electric field is applied to the insulation material [128]. With an increase in operating frequency, the losses in the insulation material will become very large [128]. However, at low or medium frequency operation, the dielectric losses can be safely neglected [118]. The dielectric losses are depicted by:

$$P_d = U^2 \cdot 2\pi f_{AC} C \cdot \tan(\delta) \tag{7.32}$$

where U is the voltage applied to the insulation material, f_{AC} and C are the fundamental AC frequency and parasitic capacitance of the transformer respectively, and $\tan(\delta)$ is the dissipation factor of the insulation material which can be obtained directly from the manufacturers.

In summary, the total losses of the transformer can be expressed as:

$$P_T = P_{copper} + P_{core} + P_d \tag{7.33}$$

7.4 Evaluation of the Efficiency of the Converters

From the above analysis of losses in the IGBT, diode, and transformer, the total losses of the converter can be obtained. Therefore, the total losses of the converter can be expressed as:

$$P_{loss\_total} = N_{SM}(P_{IGBT\_1} + P_{IGBT\_2}) + N_{Diode}P_{Diode} + N_T P_T \tag{7.34}$$

where N_{SM} is the total number of half-bridge-based SMs employed in the converter, P_{IGBT_1}

is the losses of the upper IGBT module in the half-bridge-based SM, P_{IGBT_2} is the losses of the lower IGBT module in the half-bridge-based SM, and N_{Diode} and N_T are the numbers of diodes and transformers respectively employed in the converter.

According to (7.34), the efficiency of the converter can then be evaluated using:

$$\eta = \frac{P_{out}}{P_{loss\_total}+P_{out}} \tag{7.35}$$

where η and P_{out} represent the efficiency and rated output power of the converter respectively.

7.5 Comparison of Topologies

7.5.1 *Comparison of topologies of the unidirectional DC/DC converters*

The aim of the proposed unidirectional DC/DC converters shown in figures 7.3 and 7.4 is to reduce the complexity of and the losses from the DC converters which serve as collecting points for off-shore wind farms. Therefore, it is very important to evaluate their performance against that of other available unidirectional DC/DC converter topologies. As the natural requirement of such converters is to boost the voltage at the output side, hence the proposed converters are compared with the other unidirectional cascaded ISOS and IPOS configurations illustrated in figure 7.5.

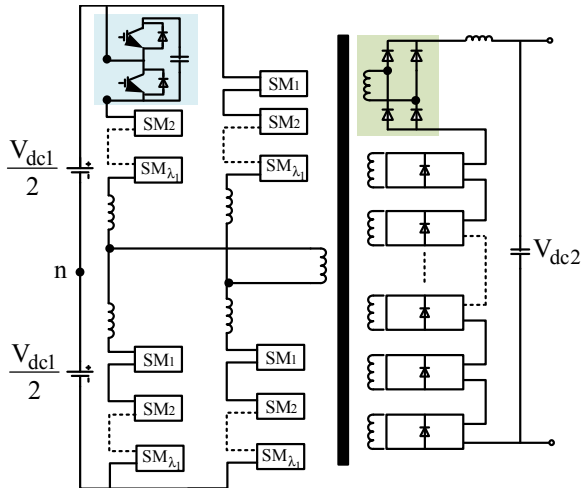


Figure 7.3 Proposed unidirectional single-phase DC/DC converter.

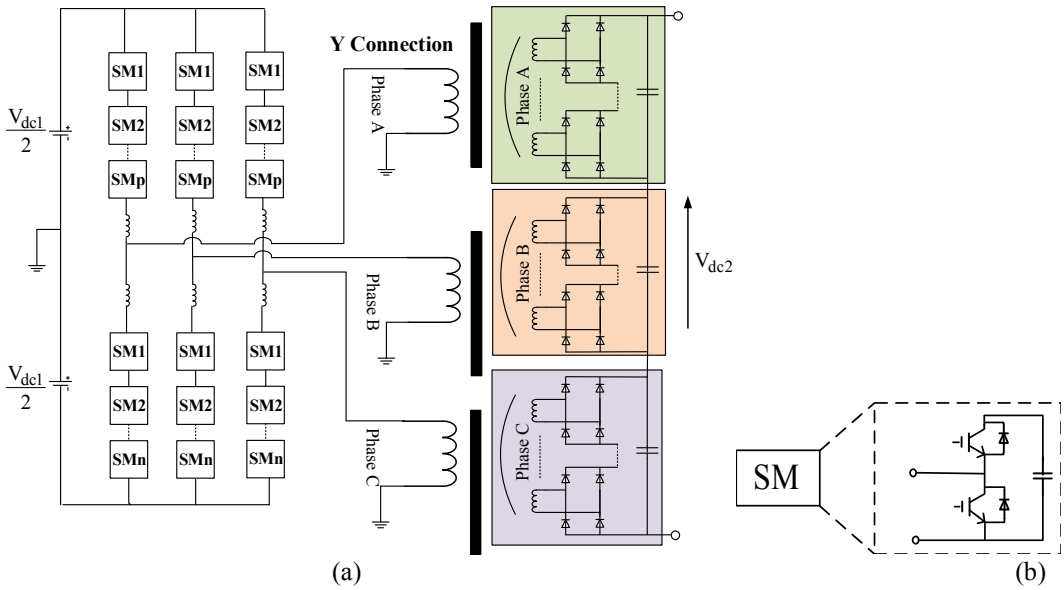


Figure 7.4 Configurations of (a) proposed unidirectional three-phase DC/DC converter; (b) half-bridge based submodule at the primary side of the proposed converter.

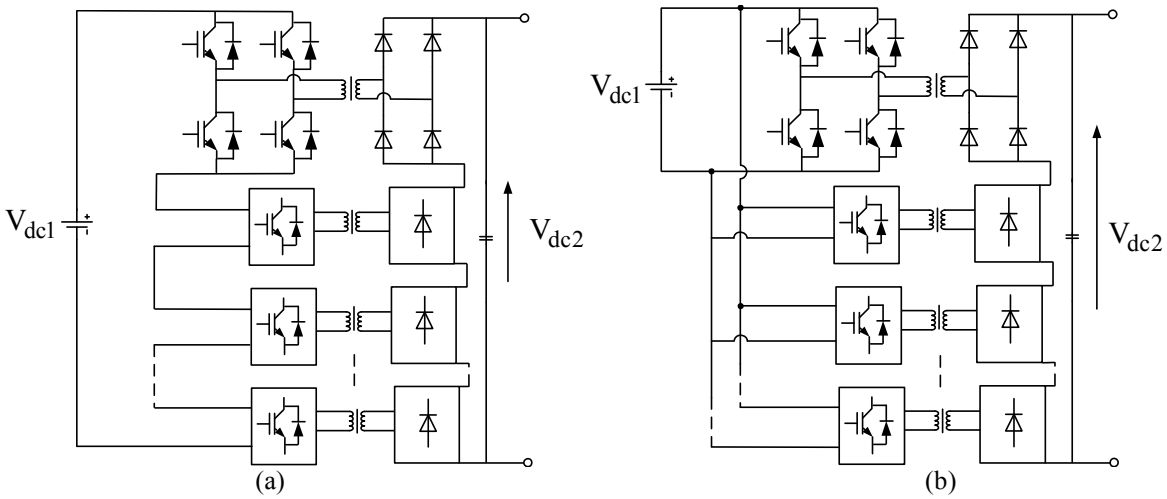


Figure 7.5 Unidirectional cascaded DC/DC converters: (a) input series output series (ISOS); (b) input parallel output series (IPOS).

Secondary diodes arrangement: Table 7.4 shows the parameters of the proposed single and three-Phase DC/DC converters as well as the ISOS and IPOS converters. For a sensible comparison, the converters are all rated at the same power and for the same input and output DC voltages.

The proposed three-phase DC/DC converter utilizes diode-bridge-rectifier modules at the secondary side which are connected in series. In this case, each of the phases of the converter are divided into two windings, and each winding is connected to one common diode bridge rectifier module. Therefore, there are six-diode bridge rectifier modules connected in series to

produce a DC voltage of 140kV. It should be noted that each valve of the diode-bridge-rectifier module consists of five diodes in series, with a voltage blocking capability of 4.5kV each.

Moreover, the other three competitive converters, including the proposed single-phase DC/DC converter and the cascaded ISOS and IPOS converters, utilize fourteen diode bridge rectifier modules connected in series at the secondary side to produce an output DC voltage of 140kV, and each valve of the diode-bridge rectifier module consists of two diodes in series [123], with a voltage blocking capability of 5kV each [131].

Primary IGBT arrangement: The primary sides of the proposed single- and three-phase DC/DC converters, as well as the cascaded ISOS and IPOS converters, are also designed with the same requirements of a blocking voltage capability for each IGBT module at the primary side of 1.07kV. This necessitates a total of 112 IGBT modules for the proposed single-phase DC/DC converter and 168 IGBT modules for the proposed three-phase DC/DC converter, as opposed to 56 IGBT modules for the ISOS converter and 784 IGBT modules for the IPOS converter, as shown in Table 7.4.

Table 7.4 System parameters of the three DC/DC converters

Items	Proposed unidirectional single-phase converter	Proposed unidirectional three-phase converter	Conventional unidirectional ISOS converter	Conventional unidirectional IPOS converter
Rated power	10MW			
Input DC voltage	15kV			
Output DC voltage	140kV			
Total number of IGBT modules at the primary side	112 (28*4)	168 (28*6)	56 (14*4)	784 (14*4*14)
Total number of diode modules at the secondary side	112 (14*8)	120 (20*6)	112 (14*8)	112 (14*8)
Primary rated submodule voltage	1.07kV			
Secondary rated diode voltage	5kV			
Modulation method	Sinusoidal pulse width modulation (SPWM)			
carrier-reference frequency ratio (R_c)	$R_c = f_C/f_{AC}$ =5			
AC frequency (f_{AC})	400Hz	400Hz	400Hz	400Hz
Carrier frequency (f_C)	2kHz	2kHz	2kHz	2kHz

However, it should be noted that, for the conventional ISOS and IPOS converters, the numbers of converter modules on the primary and secondary sides are dependent on each other. If a higher voltage is required at the output side, then the same number of converter modules and their associated transformers must be added at both sides, and hence the losses and complexity increase. However, with the proposed single- and three-phase DC/DC converters, number of modules are independent of each other, and so more rectifier modules can be added at the secondary side without increasing the number of IGBT modules at the primary side.

Frequency selection: For a fair comparison, all four topologies are modulated utilizing sinusoidal pulse width modulation (SPWM) with the same carrier-reference frequency ratio, denoted as R_c, where $R_c = f_C/f_{AC}$ and f_C and f_{AC} are the frequencies of the triangular carrier and fundamental AC reference waveform respectively. It is worth noting that 400Hz is selected as the fundamental AC frequency of all these four topologies, which is chosen to give a trade-off between switching losses and the size of the system. If the converters operate at a low frequency such as 50Hz, the power density of the whole system will be substantially reduced due to the need for low frequency transformers and corresponding heat dissipation systems. This would seriously influence the large-scale engineering application of the topologies, especially for an offshore platform with limited space.

Core volume of transformer: The core volume is determined by the area product equation (which has been detailed introduced in section 7.3.1) and dimensional limits for the different materials-based transformer core (which can be obtained from the manufacturer directly). In this case, amorphous alloy ‘magnetic 2605SA1’ is used as the core of the transformer. According to reference [132], the dimensional limits for amorphous alloy-based transformer core are summarized in table 7.5. Therefore, the core volume can be directly evaluated as shown in table 7.6. It is worth noting that a detail transformer design process is presented in Chapter 8.

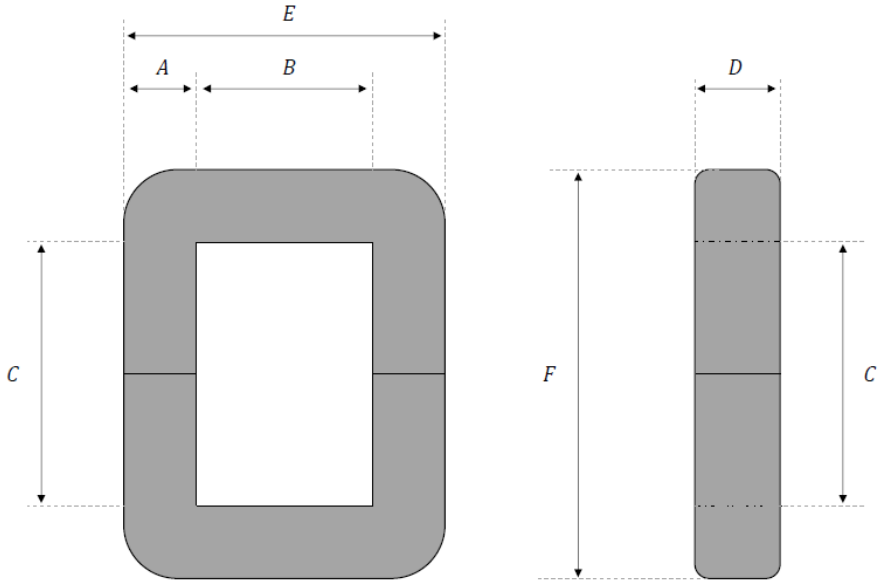


Figure 7.6 Structure dimensions of the transformer core.

Table 7.5 Dimensional limits for amorphous alloy material-based transformer core

Description	Symbols	Minimum (mm)	Maximum (mm)	Increment (mm)
Column width	A	25	75	1
Window width	B	80	250	5
Window height	C	180	600	10
Core mean length	l_m	2(B+C) +4A		
Core total area	A_c	AD		
Core volume	V_c	$l_m A_c$		

Selection of IGBT and diode types: The losses of the topologies are also evaluated based on the analysis presented earlier in Sections 7.2 and 7.3. For this purpose, suitable IGBT modules and diodes must be selected for the converters. As mentioned above, for a sensible comparison, all four DC/DC converters are rated at the same power and the same input and output DC voltage as shown in table 7.4. However, due to the different configurations at the primary side of the converters, the current stress of every single IGBT module is different. Therefore, according to the different current stresses, FZ1200R12HE4 [133] and FZ800R12KE3 IGBT modules [134] are chosen for the primary IGBT modules of the proposed single- and three-phase DC/DC converters respectively, and FZ1600R12HP4 [135] and FZ400R12KE4 IGBT modules [136] for the primary IGBT modules of the cascaded ISOS and IPOS converters respectively. Meanwhile, due to the similar configurations at the secondary side of the converters, the D1131SH diode [129] is selected for all of them. Table 7.7 shows the parameters

of the selected IGBTs and Diodes. It is noting that the parameters of selected IGBT and Diode modules that shown in table 7.7 are based on the $T_j = 125℃$ (T_j is the operating temperature of the components).

Table 7.6 Parameters of the medium frequency transformers

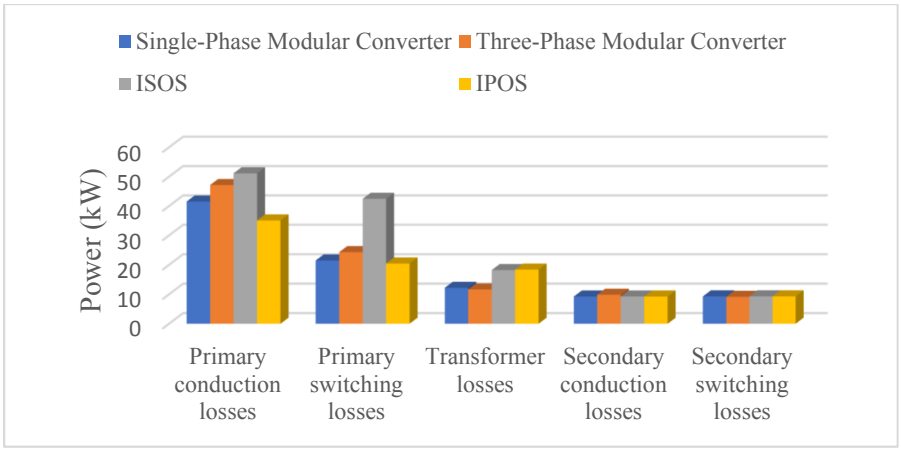
Items	Transformer for proposed unidirectional single-phase converter	Transformer for proposed unidirectional three-phase converter	Transformer for unidirectional ISOS converters	Transformer for unidirectional IPOS converters
Number of transformers	1	3	14	14
Rated power	10MW	3.5MW	0.8MW	0.8MW
Rated frequency	400Hz	400Hz	400Hz	400Hz
Rated primary voltage	10kV	5kV	0.8kV	10kV
Rated secondary voltage	140kV	47kV	10kV	10kV
Primary equivalent resistance	5.2mΩ	2.17mΩ	0.66mΩ	54.29mΩ
Secondary equivalent resistance	580mΩ	192mΩ	54.29mΩ	54.29mΩ
Core material	Magnetic alloy 2605SA1			
Core coefficients for Steinmetz equation	$k = 1.4,\ \alpha = 1.47,\ \beta = 1.52$			
Saturated flux density	1.56T			
Core volume	0.21m^3	0.094m^3	0.033m^3	0.033m^3

Table 7.7 Selected IGBT/Diode parameters

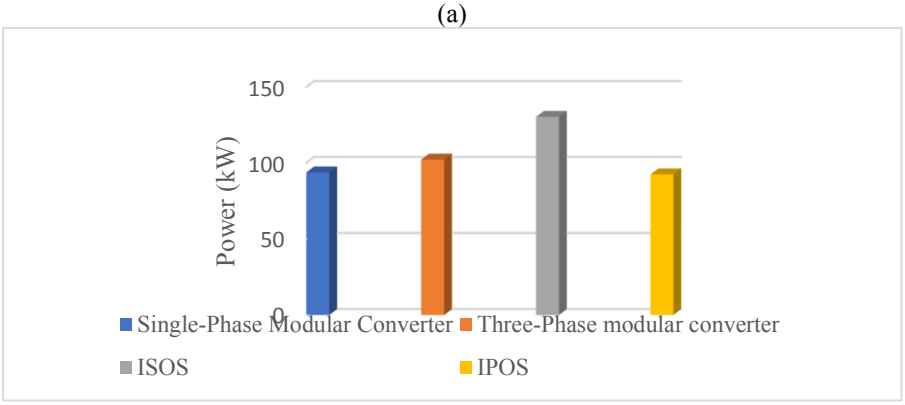
IGBT/diode code	Rated voltage	Rated current
FZ1200R12HE4	1.2kV	1.2kA
FZ800R12KE3	1.2kV	0.8kA
FZ1600R12HP4	1.2kV	1.6kA
FZ400R12KE4	1.2Kv	0.4kA
D1131SH	6.5kV	1.1kA

The losses of the medium frequency transformer are calculated based on the parameters tabulated in Table 7.6, which have been reported elsewhere [128] [130]. The breakdown and total losses are illustrated in figure 7.7, while figure 7.8 shows the efficiency of all the converters for the whole range of output power. As expected, the proposed single-phase and three-phase DC/DC converters show better performance in many respects than as oppose to the cascaded ISOS and IPOS converters, especially in terms of losses and component utilization.

From figure 7.7(b), it can also be seen that the total losses of the proposed single-phase DC/DC and three-phase DC/DC converters are much smaller than those of the cascaded ISOS converter but slightly larger than for the cascaded IPOS converter. However, the number of IGBT modules employed in the cascaded IPOS converter is much higher than in any of the other three converter types, as shown in table 7.4, which makes control more complicated and hence decreases reliability.



(a)



(b)

Figure 7.7 Distribution of power losses in the proposed unidirectional single and three-phase converters and ISOS and IPOS converters for operation at a rated power of 10MW: (a) breakdown of losses; (b) total losses.

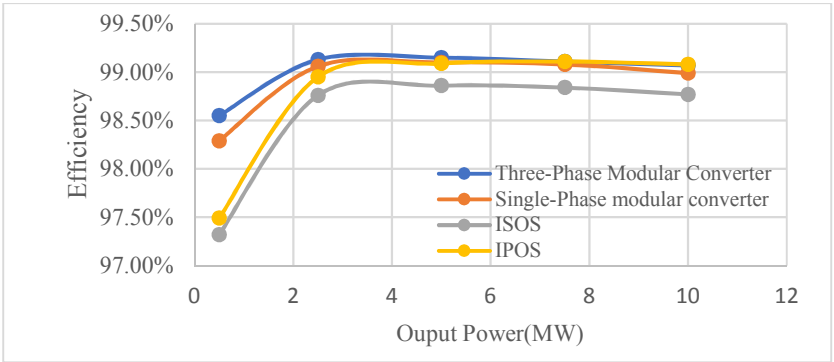


Figure 7.8 Comparison of converters efficiency at different levels of output power.

7.5.2 *Comparison of topologies of the bidirectional DC/DC converters*

The performance of the proposed bidirectional three-phase DC/DC converter shown in figure 7.9 is evaluated via a comparison with other available bidirectional DC/DC converter topologies. Once again, the natural requirement of this converter is to step up the voltage at the output side, and therefore it is compared with the two conventional three-phase MMC-based DC/DC converters shown in figure 7.10, and the bidirectional cascaded ISOS and IPOS configurations shown in figure 7.11.

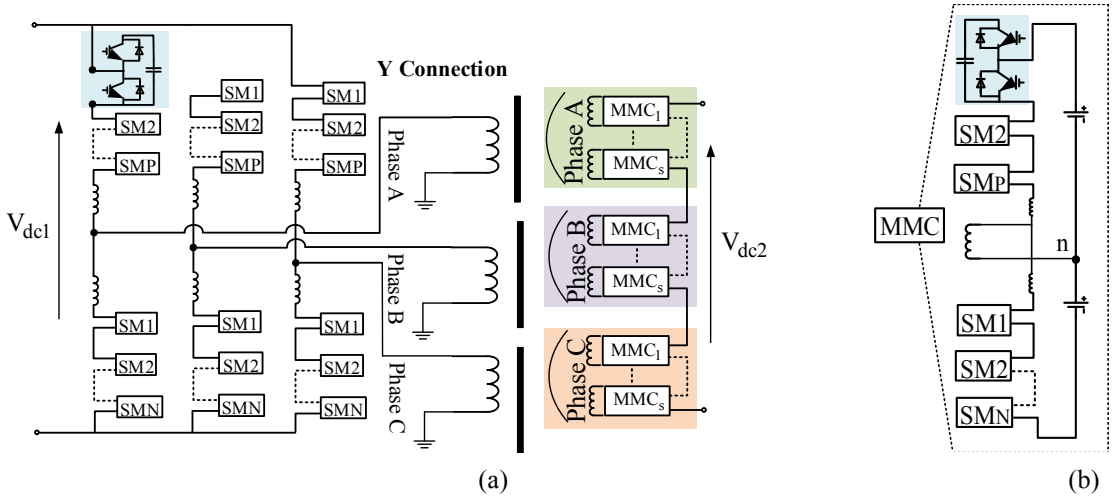


Figure 7.9 Proposed DC/DC converter: (a) configuration; (b) one-leg MMC-based submodule at the secondary side of the proposed converter.

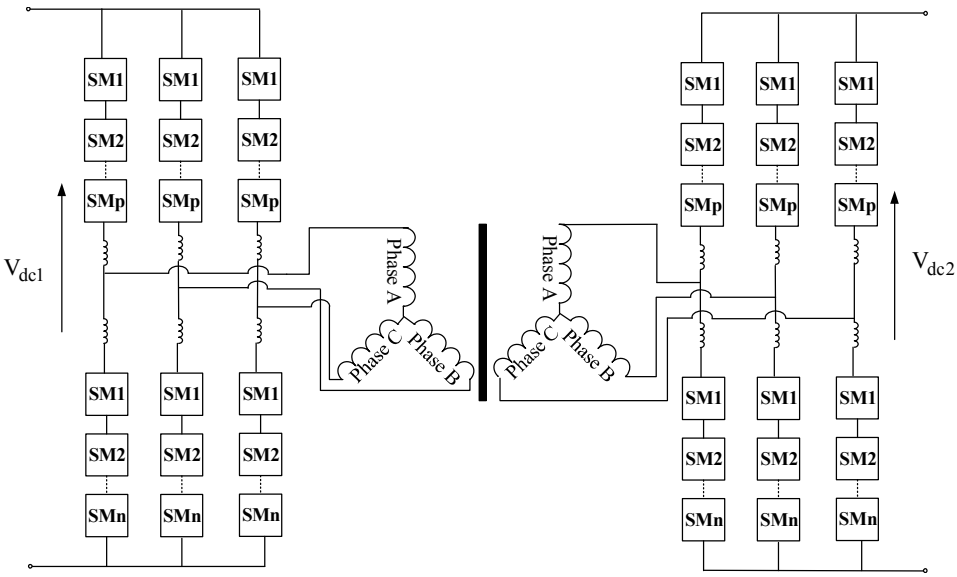


Figure 7.10 Two three-phase MMC-based DC/DC converter.

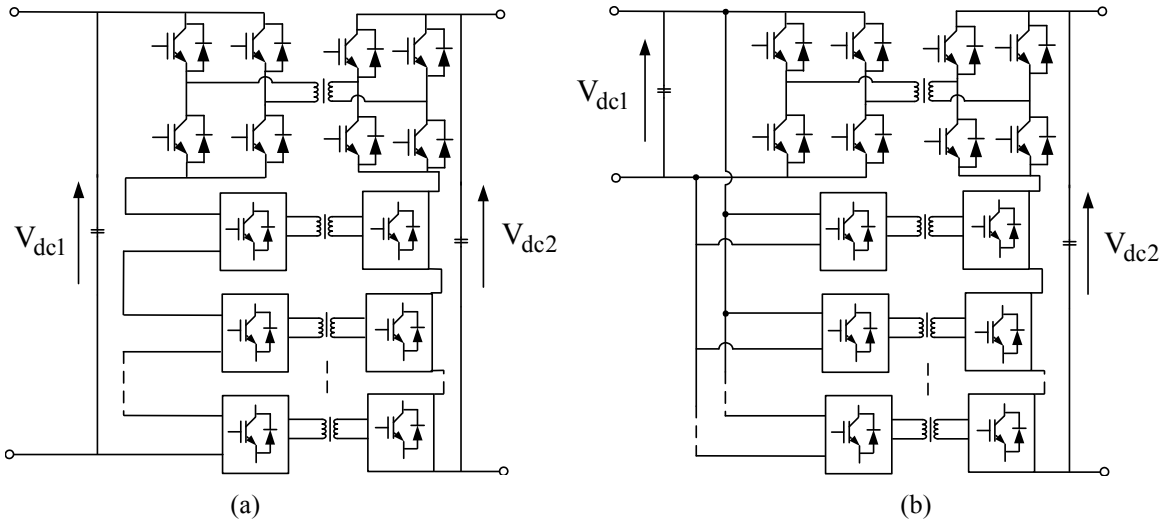


Figure 7.11 Bidirectional cascaded DC/DC converters: (a) input series output series (ISOS); (b) input parallel output series (IPOS).

Primary IGBT arrangement: Table 7.8 portrays the parameters of the proposed and conventional three-phase modular DC/DC converters as well as the cascaded ISOS and IPOS converters. For a sensible comparison, all these converters are rated at the same power and the same input and output DC voltages.

Since the proposed and conventional modular three-phase DC/DC converters employ the same three-phase MMC functioning as inverters at the primary side, therefore they have the same number of half-bridge-based SMs (each including two IGBT modules), the same device ratings, and the same switching and conduction losses as shown in table 7.8 and figure 7.12. Furthermore, the primary side of the proposed and conventional modular three-phase DC/DC converters, as well as the cascaded ISOS and IPOS converters, are designed with the same requirement of a blocking voltage capability of each IGBT module at the primary side of 3kV. This requires a total of 60 IGBT modules for both the proposed and the conventional modular three-phase DC/DC converters, as opposed to 20 IGBT modules for the cascaded ISOS converter and 100 IGBT modules for the cascaded IPOS converter at the primary side, as shown in table 7.8.

However, it should again be noted that, for the cascaded ISOS and IPOS converters, the numbers of converter modules on the primary and the secondary sides are dependent on each other, which is not the case for the proposed and conventional three-phase DC/DC converters.

Table 7.8 System parameters of the three DC/DC converters

Items	Proposed bidirectional three-phase converter	Conventional bidirectional three-phase converter	Bidirectional ISOS converter	Bidirectional IPOS converter
Rated power	12MW			
Input DC voltage	15kV			
Output DC voltage	150kV			
Total number of IGBT modules at the primary side	60 (10*6)	60 (10*6)	20 (4*5)	100 (5*4*5)
Total number of IGBT modules at the secondary side	120 (10*12)	360 (60*6)	120 (6*4*5)	120 (6*4*5)
Primary rated IGBT voltage	3kV			
Secondary rated IGBT voltage	5kV			
Modulation method	Sinusoidal pulse width modulation (SPWM)			
Carrier-reference frequency ratio (R_c)	$R_c = f_C/f_{AC}$ =5			
AC frequency (f_{AC})	400Hz	400Hz	400Hz	400Hz
Carrier frequency (f_C)	2kHz	2kHz	2kHz	2kHz

Secondary IGBT arrangement: In this case, each decoupled phase (Phase-a, Phase-b, and Phase-c) of the proposed three-phase DC/DC converter at the secondary side has two one-leg MMC-based rectifier modules connected in series, and each arm in these modules has 5 half-bridge-based SMs. Therefore, the total number of half-bridge-based SMs at the secondary side is 60 (120 IGBT modules), each having the capability to withstand a voltage of 5kV. With the same design criterion, the two conventional three-phase MMC-based DC/DC converters would need 30 half-bridge-based SMs (60 IGBT modules) per arm, which means that a total of 180 half-bridge-based SMs (360 IGBT modules) are required at the secondary side as opposed to 60 half-bridge-based SMs (120 IGBT modules) in the case of the proposed three-phase DC/DC converter. Therefore, the proposed three-phase DC/DC converter requires only one-third of the number of half-bridge-based SMs compared with conventional three-phase DC/DC converter for the same design requirements. This considerably reduces cost and control complexity, leading to higher reliability and a more cost-effective solution.

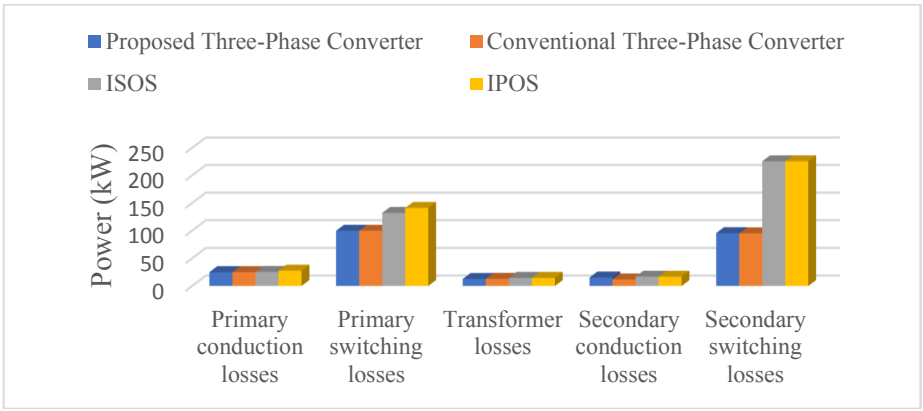
For a sensible comparison, the ISOS and IPOS converters are also designed with the same requirement of a blocking voltage capability of each IGBT module at the secondary side of 5kV. This means that five H-bridge-rectifier modules are connected in series at the secondary side to produce an output DC voltage of 150kV, and each valve of the H-bridge-rectifier module

consists of 6 IGBTs in series, with a voltage blocking capability of 5kV each. Therefore, the cascaded ISOS and IPOS converters require 120 IGBT modules at the secondary side, as shown in table 7.8.

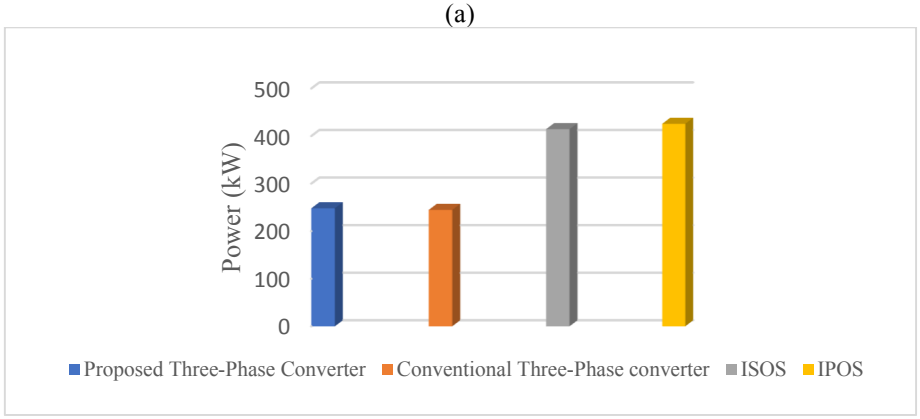
Table 7.9 Selected IGBT parameters

IGBT	Rated voltage	Rated current
FZ800R33KF2C	3.3kV	0.8kA
FZ1500R33HL3	3.3kV	1.5kA
FZ400R33KL2C_B5	3.3kV	0.4kA
FZ250R65KE3	6.5kV	0.25kA

Selection of IGBT and diode types: The losses of the topologies are also evaluated based on the analysis presented above in Sections 7.2 and 7.3 to estimate the efficiency of the four converters across the whole range of output power. For this purpose, suitable IGBTs for the converters must be selected. As mentioned above, for a sensible comparison, all four converters are rated at the same power and the same input and output DC voltages as shown in table 7.8. However, due to the different configurations of the converters, the current stress of each IGBT module is different. Therefore, according to the different current stresses of converters, FZ800R33KF2C IGBT modules [137] are chosen for the primary IGBT modules of the proposed and conventional three-phase DC/DC converters, and the FZ1500R33HL3 [138] and FZ400R33KL2C_B5 IGBT modules [139] for the primary IGBT modules of the cascaded ISOS and IPOS converters respectively. Meanwhile, the FZ250R65KE3 IGBT module [140] is selected for the secondary side of all these four converters. Table 7.9 shows the parameters of the selected IGBTs. It is noting that the parameters of selected IGBT modules that shown in table 7.9 are based on the $T_j = 125℃$ (T_j is the operating temperature of the components).



(a)



(b)

Figure 7.12 Distribution of power losses in the proposed and conventional bidirectional three-phase converters, and bidirectional cascaded ISOS and IPOS converters at 12MW output power (a) breakdown of losses; (b) total losses.

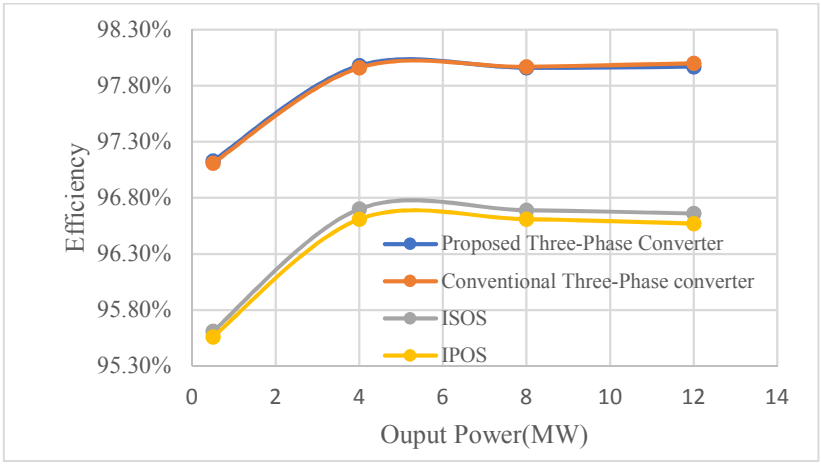


Figure 7.13 Comparison of converters efficiency at different output power levels.

It is worth noting that the decoupled three-phase transformer used in the proposed three-phase converter can be built by using three single-phase transformers. The losses of every single-phase transformer are calculated based on the parameters listed in Table 7.10, assuming

that the three single-phase transformers are identical and have the same parameters. The breakdown and total losses are illustrated in figure 7.12. Figure 7.13 shows the efficiency of all the converters for the whole range of output power. From figures 7.12 and 7.13, the proposed three-phase converter exhibits similar overall losses to those of conventional three-phase converters, but much smaller losses than the ISOS and IPOS converters.

Table 7.10 Parameters of the medium frequency transformers

Items	Transformer for proposed bidirectional three-phase converter	Transformer for conventional bidirectional three-phase converter	Transformer for bidirectional ISOS converters	Transformer for bidirectional IPOS converters
Number of transformers	3	3	5	5
Rated power	4MW	4MW	2.4MW	2.4MW
Rated frequency	400Hz	400Hz	400Hz	400Hz
Rated primary voltage	5kV	5kV	2.1kV	10kV
Rated secondary voltage	18kV	53kV	30kV	30kV
Primary equivalent resistance	1.9mΩ	1.9mΩ	0.63mΩ	14.6mΩ
Secondary equivalent resistance	23.63mΩ	209mΩ	129mΩ	129mΩ
Core material	Magnetic alloy 2605SA1			
Core coefficients for Steinmetz equation	$k = 1.4,\ \alpha = 1.47,\ \beta = 1.52$			
Saturated flux density	1.56T			
Core volume	0.1m^3	0.1m^3	0.068m^3	0.068m^3

7.6 Summary

Chapter 7 has conducted comparisons of the proposed DC/DC converters and conventional DC/DC converters. In addition to comparing the structures of the circuit topologies, evaluations of losses and efficiency are also performed. Moreover, detailed analyses and calculations of the IGBT module and transformer losses are also presented.

Chapter 8. Components Design and Experimental Results of the Unidirectional Single-Phase Modular Multilevel DC/DC Converter

8.1 Introduction

In this chapter, a low-voltage scaled-down laboratory prototype of the proposed unidirectional single-phase modular multilevel DC/DC converter described in Chapter 4 is developed to validate and confirm the feasibility of the topology and its control strategy. The detailed design process of the laboratory prototype of the converter is presented, including component selection, transformer design, and the introduction of the different control boards. Finally, the experimental results are also described in this chapter.

8.2 Design Considerations for the Laboratory Prototype

8.2.1 *Submodule capacitor selection*

It is well known that the submodule capacitance of the MMC is used to limit the capacitor voltage ripple. And this ripple is mainly influenced by the arm current which flows through the submodules (SMs). Therefore, it is crucial to analyze and understand the energy storage in the SMs and the converter arms [141-142].

According to the basic operating principle of the MMC, taking Phase-a as an example, the upper and lower arm voltages V_{aU} and V_{aL}, can be easily obtained and are expressed as:

$$V_{aU} = \frac{V_{dc1}}{2} - \hat{V}_{Pa} \sin \omega t \tag{8.1}$$

$$V_{aL} = \frac{V_{dc1}}{2} + \hat{V}_{Pa} \sin \omega t \tag{8.2}$$

where V_{dc1} is the input DC voltage of the MMC, $\hat{V}_{Pa}$ is the peak value of the output AC phase voltage of Phase-a, and ω is the fundamental angular frequency.

If only the fundamental frequency of the MMC is considered, and there are no harmonics in

the circulating current, the upper and lower arm currents can be obtained from (8.3) and (8.4) [8] respectively.

$$I_{aU} = \frac{1}{4}M_1\hat{I}_{Pa}\cos\emptyset + \frac{1}{2}\hat{I}_{Pa}\sin(\omega t - \emptyset) \tag{8.3}$$

$$I_{aL} = \frac{1}{4}M_1\hat{I}_{Pa}\cos\emptyset - \frac{1}{2}\hat{I}_{Pa}\sin(\omega t - \emptyset) \tag{8.4}$$

where M_1 is the modulation index, $\hat{I}_{Pa}$ is the peak value of the output AC phase current of Phase-a, and $\emptyset$ is the phase shift angle between the AC phase voltage and currrent.

According to (8.1), (8.2), (8.3) and (8.4), the instantaneous power of the upper and lower arms can be expressed as:

$$P_{aU} = V_{aU} \times I_{aU} = \left(\frac{V_{dc1}}{2} - \hat{V}_{Pa}\sin\omega t\right) \cdot \left[\frac{1}{4}M_1\hat{I}_{Pa}\cos\emptyset + \frac{1}{2}\hat{I}_{Pa}\sin(\omega t - \emptyset)\right] \tag{8.5}$$

$$P_{aL} = V_{aL} \times I_{aL} = \left(\frac{V_{dc1}}{2} + \hat{V}_{Pa}\sin\omega t\right) \cdot \left[\frac{1}{4}M_1\hat{I}_{Pa}\cos\emptyset - \frac{1}{2}\hat{I}_{Pa}\sin(\omega t - \emptyset)\right] \tag{8.6}$$

where P_{aU} and P_{aL} are the power flowing to the upper and lower arms respectively.

By integrating (8.5) and (8.6) over one fundamental period, the energy variation in the upper and lower arms can be obtained as follows:

$$E_{aU} = \int_0^{2\pi} P_{aU}dt = \frac{V_{dc1}\hat{I}_{Pa}}{16\omega}(4\sin(\omega t - \emptyset) - M_1\sin(2\omega t - \emptyset) - 2{M_1}^2\sin(\omega t)\cos(\emptyset)) \tag{8.7}$$

$$E_{aL} = \int_0^{2\pi} P_{aL}dt = -\frac{V_{dc1}\hat{I}_{Pa}}{16\omega}(4\sin(\omega t - \emptyset) - M_1\sin(2\omega t - \emptyset) - 2{M_1}^2\sin(\omega t)\cos(\emptyset)) \tag{8.8}$$

where E_{aU} and E_{aL} are the energy stored in the upper and lower arms respectively.

The relation between the amplitude of the alternating voltage and the dc-link voltage is given by:

$$V_{dc1} = \frac{2\hat{V}_{Pa}}{M_1} \tag{8.9}$$

Substituting the (8.9) into the (8.7) and (8.8), yields:

$$E_{aU} = \int_0^{2\pi} P_{aU}dt = \frac{S}{36M_1\omega}(4\sin(\omega t - \emptyset) - M_1\sin(2\omega t - \emptyset) - 2{M_1}^2\sin(\omega t)\cos(\emptyset)) \tag{8.10}$$

$$E_{aL} = \int_0^{2\pi} P_{aL}dt = -\frac{S}{36M_1\omega}(4\sin(\omega t - \emptyset) - M_1\sin(2\omega t - \emptyset) - 2{M_1}^2\sin(\omega t)\cos(\emptyset)) \tag{8.11}$$

where S is the total apparent power transfer of Phase-a, this is

$$S= \frac{1}{2}\hat{V}_{Pa}\hat{I}_{Pa} \tag{8.12}$$

If the energy variations in the upper and lower arms are represented by ΔE_{arm}, according to (8.10) and (8.11), it can be expressed as:

$$\Delta E_{arm} = \max(E_{aU}) - \min(E_{aU}) \tag{8.13}$$

where $\max(E_{aU})$ and $\min(E_{aU})$ represent the peak and minimum values of E_{aU}. It should be noted that, due to the symmetry of the energy in the upper and lower arms, it is sufficient to consider only one of the two arms.

It is assumed that the energy storage in the arm is evenly divided among λ_1 SMs, and therefore the variation in energy of each SM capacitor can be expressed as:

$$\Delta E_{capacitor} = \Delta E_{arm}/\lambda_1 = \max(E_{capacitor}) - \min(E_{capacitor}) \tag{8.14}$$

where $\Delta E_{capacitor}$ is the energy variation in every SM capacitor, and $\max(E_{capacitor})$ and $\min(E_{capacitor})$ represent the maximum and minimum values respectively of the energy stored in the each SM capacitor.

It is well known that the energy stored in a capacitor is proportional to the square of the voltage crossing the capacitor, which can be expressed as:

$$E_{capacitor} = \frac{1}{2}CV_{capacitor}^2 \tag{8.15}$$

where C is the capacitance of the SM capacitor and $V_{capacitor}$ is the voltage crossing the SM capacitor.

According to (8.15), the maximum energy stored in the submodule capacitor occurs when the voltage is at its maximum value, which can be expressed as:

$$\max(E_{capacitor}) = \frac{1}{2}C(V_{avg} + \frac{1}{2}\Delta V)^2 \tag{8.16}$$

where $\max(E_{capacitor})$ represents the maximum energy stored in the SM capacitor, and V_{avg} and ΔV are the average voltage and voltage ripple of the SM capacitor respectively. It is worth noting that, in general, the voltage ripple ΔV is often set from 2% to 10% of the average value.

Similarly, the minimum energy stored in the SM capacitor occurs when the voltage is at its minimum value, which can be expressed as:

$$\min(E_{capacitor}) = \frac{1}{2}C(V_{avg} - \Delta V)^2 \tag{8.17}$$

where $\min(E_{capacitor})$ represents the minimum energy stored in the submodule capacitor.

Substituting (8.16) and (8.17) into (8.13) and rearranging the equation gives:

$$\mathrm{C} = \Delta E_{arm} / \lambda_1 \, \Delta V V_{avg} \tag{8.18}$$

Therefore, with the above analysis and a given specification, the SM capacitance of the experimental platforms (platform-one and platform-two as shown in figures 8.7 and 8.14 respectively) can be estimated:

(1) Specification of platform-one: apparent power S=50VA, angular frequency $\omega = 400$rad/s, modulation index $M_1 = 1$, SM number per arm $\lambda_1 = 3$, average voltage of SM $V_{avg} = 20\mathrm{V}$, power factor $\cos(\emptyset) = 0.9$, phase shift angle $\emptyset = 0.14\pi$, and voltage ripple of SM capacitor $\Delta V = 1\mathrm{V}$.

Substituting above parameters into the (8.10), (8.11), and (8.18), the SM capacitance of platform-one can be calculated, which is about 2.2mF.

(2) Specification of platform-two: apparent power S=100VA, angular frequency $\omega = 400$rad/s, modulation index $M_1 = 1$, SM number per arm $\lambda_1 = 3$, average voltage of SM $V_{avg} = 20\mathrm{V}$, power factor $\cos(\emptyset) = 0.9$, phase shift angle $\emptyset = 0.14\pi$, and voltage ripple of SM capacitor $\Delta V = 1.5\mathrm{V}$.

Substituting above parameters into the (8.10), (8.11), and (8.18), the SM capacitance of platform-two can be calculated, which is about 3.0mF.

It is worth noting that, to simplify the design process of the prototypes, platform-one and two used the same SM board (SM capacitance is 2.2mF) in this project.

8.2.2 *Arm inductor selection*

The arm inductor is an essential circuit component which ensures the normal operation of the MMC. Also, when a short-circuit fault occurs in the MMC, the presence of the arm inductor can effectively inhibit the rate of the short-circuit current rise, thereby protecting the power components in the MMC from damage. Furthermore, as the arm inductance increases, the harmonics in the output AC current will be significantly reduced, thereby reducing the total

harmonic distortion (THD). However, excessive arm inductance will not only affect the speed response of the current but will also reduce the power density of the whole system. Conversely, if the arm inductance is too small, the harmonics in the output AC current will not be effectively filtered out, thereby increasing THD. In summary, the effect of the arm inductance on the overall performance of the converter is very important.

(1) Suppressing circulating current:

According to the literature [143-145], the circulating current has twice the fundamental frequency and circulates through the upper and lower arms. The inductance value can be defined based on the criterion of limiting the second order current component. Equation (8.19) [143-144] can be used in this case:

$$L_{Parm} \geq \frac{5\lambda_1}{48C\omega^2} \tag{8.19}$$

where λ_1 is the SM number per arm, C is the SM capacitance, and ω is the fundamental angular frequency.

Therefore, with the above proposed equation and a given specification, the arm inductance of the experimental platforms (platform-one and platform-two as shown in figures 8.7 and 8.14 respectively) can be estimated:

(1) Specification of platform-one: SM number per arm λ_1=3, angular frequency $\omega = 2\pi f$=$2\pi \cdot 400$ rad/s and SM capacitance $C = 2$mF.
Substituting above parameters into (8.19), it can get that $L_{Parm} \geq 0.025$mH. With the above calculated and simulation results, it selected 0.1mH as the inductance of arm inductor for the platform-one.

(2) Specification of platform-two: SM number per arm λ_1=3, angular frequency $\omega = 2\pi f$=$2\pi \cdot 400$ rad/s and SM capacitance: $C = 3$mF.
Substituting above parameters into (8.19), it can get that $L_{Parm} \geq 0.017$mH. With the above calculated and simulation results, it selected 0.1mH as the inductance of arm inductor for the platform-two.

(2) Inductance selection according to protection:

One common criterion used to choose the size of arm inductance is the protection against a DC-side short-circuit. When a short-circuit fault occurs on the DC side of the MMC, each arm inductor in the system will generate an extremely large current, which will cause serious damage to the power devices in the circuit. Due to their symmetry, the fault currents (e.g.I_{aU} and I_{aL}) of the upper and lower arms will have the same values and rates of rise in current. According to previous research [143-145], the fault rate can be used to size the inductance, as shown in (8.20).

$$L_{arm} = \frac{\lambda_1 V_{capacitor}}{2K} \tag{8.20}$$

where $K = \frac{dI_{aU}}{dt} = \frac{dI_{aL}}{dt}$, $V_{capacitor}$ is the SM capacitor voltage, and λ_1 is the number of SMs per arm.

Taking reference [2] as an example, if the reaction time of circuit breaker that employed in the circuit is 20ms, the maximum allowed current is 2kA, and the input DC voltage is 10kV, according to (8.20), the arm inductance can be calculated which is equal with 0.05H. However, if the reaction time can be decreased to the range of switching-off times of semiconductors, the branch inductance rating will reduce to 5mH (at 50us reaction time). It is noting that due to the experimental platform that used in this project is just a low voltage scaled down laboratory prototype. Therefore, there is no circuit breaker employed in the circuit.

8.2.3 *Consideration of the output filter*

The output filter is another important design aspect. For a secondary combined converter, a set of output filtering inductors and capacitors is employed, which function to eliminate ripple and finally achieve the smooth output waveform required. On the other hand, a suitable filtering inductor is available to limit the falling rate of the diode current in the SM. Therefore, the diode reverse recovery problem can be effectively alleviated. According to a previous study [145],

the values of these variables can be calculated as follows:

$$R_L \cdot C_o \geq (3\sim5)\frac{T}{2} \tag{8.21}$$

$$f_{AC} \geq f_c = \frac{1}{2\pi\sqrt{L_o C_o}} \tag{8.22}$$

where L_o, C_o, T, R_L, f_{AC}, f_c are output filtering inductance and capacitance, a period of AC voltage, output load resistor, the fundamental frequency of AC voltage, and cut-off frequency respectively.

Therefore, with the above equations and a given specification, the inductance and capacitance of output filter of experimental platforms (platform-one and platform-two as shown in figures 8.7 and 8.14 respectively) can be estimated:

(1) Specification of platform-one: fundamental frequency is f_{AC}=400Hz, half-waveform (after rectification) frequency is $f'_{AC} = 2f_{AC} = 800\text{Hz}$, the period is $T = 0.0025s$, and output load resistor $R_L = 20\Omega$.

Substituting above parameters into (8.21), it can get that $C_o \geq 0.4\text{mF}$. With the above calculated and simulation results, it selected 1mF as the capacitance of the output filter for the platform-one. Substituting $C_o = 1\text{mF}$ into (8.22), it can get that the inductance of output filter $L_o \geq 0.04\text{mH}$. Finally, it selected 0.1mH as the inductance of output filter for the platform-one.

(2) Specification of platform-two: fundamental frequency is f_{AC}=400Hz, half-waveform (after rectification) frequency is $f'_{AC} = 2f_{AC} = 800\text{Hz}$, the period is $T = 0.0025s$, and output load resistor $R_L = 40\Omega$.

Substituting above parameters into (8.21), it can get that $C_o \geq 0.2\text{mF}$, With the above calculated and simulation results, it selected 1mF as the capacitance of the output filter for the platform-two. Substituting $C_o = 1\text{mF}$ into (8.22), it can get that the inductance of output filter $L_o \geq 0.04\text{mH}$. Finally, it selected 0.1mH as the inductance of output filter for the platform-two.

8.3 Design Example of Transformer

In this section, a medium frequency transformer is designed using the core geometry approach reported elsewhere [130]. The design specifications of the transformer are shown in Table 8.1.

Table 8.1 Design specification of the medium frequency transformer

1. Input voltage (V_{in})	40V
2.The output voltage of terminal one (V_{out1})	40V
3. The output voltage of terminal two (V_{out2})	40V
4. The output power of terminal one (P_{out1})	35W
5. The output power of terminal two (P_{out2})	35W
6. Frequency, (f)	400Hz
7. Efficiency, (η)	95%
8. Regulation, (α)	5%
9. Maximum flux density, (B_{max})	1.6T
10. Current density, (J)	$450\text{A}/cm^2$
10. Core material	Silicon M6x
11. Window utilization, (K_u)	0.6

The detailed design process is presented as follows:

1). Step One: total apparent power, P_{total}.

$$P_{total} = (P_{out1} + P_{\text{out2}})\left(\frac{1}{\eta} + 1\right) = (35 + 35)\left(\frac{1}{0.95} + 1\right) \approx 144\text{W} \quad (8.23)$$

where P_{out1} and P_{out2} are the output power of the secondary terminals one and two respectively, and η is the efficiency of the transformer.

2). Step Two: electrical conditions factor, K_e.

$$K_e = 0.145\left(K_f\right)^2(f)^2(B_{max})^2(10^{-4}) = 0.145(4.44)^2(400)^2(1.6)^2(10^{-4}) = 117 \quad (8.24)$$

where K_f is the waveform factor, which is equal to 4.44 when the waveform is approximately sinusoidal, and f and B_{max} are the frequency and maximum flux density of the transformer

respectively.

3). Step Three: core geometry factor, K_g.

$$K_g = \frac{P_{total}}{2K_e\alpha} = \frac{144}{2*117*5} = 0.12(cm^5) \quad (8.25)$$

where K_e is the electrical conditions factor obtained from (8.24). P_{total} is the total apparent power obtained from (8.23), and α is defined as a regulation which is the ratio of the losses and output power of the transformer.

4). Step Four: selection of the core according to the geometry factor, K_g.

Table 8.2 shows the detailed parameters of the selected core of the transformer.

Table 8.2 Parameters of the core geometry [130].

1. Lamination number	EI-625
2.Manufacturer	Thomas and Skinner
3. Magnetic path length, (MPL)	9.5cm
4. Core weight, (W_{fe})	170 g
5. Mean length per turn, (MLT)	9.5cm
7. Core area, (A_c)	2.394cm^2
8. Window area, (W_a)	1.890cm^2
9. Area product, (A_p)	4.525cm^4
10. Core geometry factor, (K_g)	0.495cm^5

5). Step Five: number of primary turns, N_P.

$$N_p = \frac{V_{in}(10^4)}{K_f B_{mac} f A_c} = \frac{40(10^4)}{4.44*1.6*400*2.394} = 59 \text{ turns} \quad (8.26)$$

where V_{in} and A_c are the primary input voltage and core cross-sectional area of the transformer respectively.

6). Step Six: input current, I_{in}.

$$I_{in} = \frac{P_{out1}+P_{out2}}{V_{in}\eta} = \frac{70}{40*0.95} \approx 1.84 \text{ A} \quad (8.27)$$

7). Step Seven: primary bare wire area, $A_{wp(B)}$.

$$A_{wp(B)} = \frac{I_{in}}{J} = \frac{1.84}{450} \approx 0.0041 \text{ cm}^2 \quad (8.28)$$

where I_{in} and J are the input current and current density of the transformer respectively.

8). Step Eight: selection of wire according to the bare wire area, $A_{wp(\mathrm{B})}$.

Table 8.3 shows the detailed parameters of the selected wire of the transformer.

Table 8.3 Parameters of the selected wire [130]

1. Product number	AWG-20
2. Wire Bare area, $A_{w(B)}$	5.1880 $cm^2(10^{-3})$
3. Wire area with insulation, A_w	6.0650 $cm^2(10^{-3})$
4. Wire Resistance, R_w	332.3 uΩ/cm
5. Diameter, D	0.0879cm
6. Weight, W_{wire}	0.04726g/cm

(9). Step Nine: primary wire resistance, R_p.

$$R_p = MLT(N_P)(R_w)(10^{-6}) = 9.5 * 59 * 332.3 * 10^{-6} = 0.19\Omega \quad (8.29)$$

where MLT is the mean length per turn, N_P is the primary turns number obtained from (8.37), and R_w is the wire resistance.

(10). Step Ten: number of turns of the secondary terminal-one, $\mathrm{N_{s1}}$.

$$N_{s1} = \frac{N_p V_{out1}}{V_{in}}\left(1 + \frac{\alpha}{100}\right) = \frac{59*40}{40}\left(1 + \frac{5}{100}\right) = 62 \text{ turns} \quad (8.30)$$

where V_{out1} is the output voltage of terminal-one.

12). Step Eleven: bare wire area of the secondary terminal-one, $A_{ws1(B)}$.

$$A_{ws1(B)} = \frac{I_{out1}}{J} = \frac{0.875}{450} = 0.0019 \ cm^2 \quad (8.31)$$

13). Step Twelve: selection of wire according to the bare wire area, $A_{ws1(B)}$. Table 8.3 shows the detailed parameters of the selected wire.

14). Step Thirteen: wire resistance of the secondary terminal-one, R_{s1}, calculation.

$$R_{s1} = MLT(N_{s1})(R_w)(10^{-6}) = 9.5 * 62 * 332.3 * 10^{-6} = 0.196\Omega \quad (8.32)$$

15). Step Fourteen: number of turns of the secondary terminal-two, $\mathrm{N_{s2}}$.

$$N_{s2} = \frac{N_p V_{s2}}{V_{in}}\left(1 + \frac{\alpha}{100}\right) = \frac{59*40}{40}\left(1 + \frac{5}{100}\right) = 62 \text{ turns} \quad (8.33)$$

16). Step Fifteen: bare wire area of the secondary terminal-two, $A_{ws2(B)}$.

$$A_{ws2} = \frac{I_{out2}}{J} = \frac{1}{450} = 0.0022 \ \ cm^2 \tag{8.34}$$

17). Step Sixteen: selection of wire according to the bare wire area, $A_{ws2(B)}$. Table 8.3 shows the detailed parameters of the selected wire.

18). Step Eighteen: wire resistance of the secondary terminal-two, R_{s2}.

$$R_{s2} = MLT(N_{s2})(R_w)(10^{-6}) = 9.5 * 62 * 332.3 * 10^{-6} = 0.196\Omega \tag{8.35}$$

19). Step Nineteen: window utilization, K_u.

$$K_u = K_{up} + K_{us1} + K_{us2} = \frac{N_p A_w}{W_a} + \frac{N_{s1} A_w}{W_a} + \frac{N_{s1} A_w}{W_a} = \frac{59*0.0061+62*0.0061+62*0.0061}{1.89} = 0.587 \tag{8.36}$$

where A_w is the wire area with insulation.

From (8.36), window utilization, K_u, is 0.587, which is smaller than the design specification of 0.6.

8.4 Control System

As a key part of the experimental platform, the control system is developed for this scaled-down prototype. The schematic diagram of the universal control platform is depicted in figure 8.3, where the digital signal processor TMS320F28335 (DSP TMS320F28335) is employed as the main unit of this control system. It handles the voltage and current signals obtained from the interface board and then outputs the pulse width modulation (PWM) signals to the drive circuits through the interface board to control the switches of the primary MMC of the scaled-down prototype. It is worth noting that up to 10 measurements and 12 PWM signals can be processed by the DSP TMS320F28335 and the interface board at the same time. The details of the three main control boards are as follows.

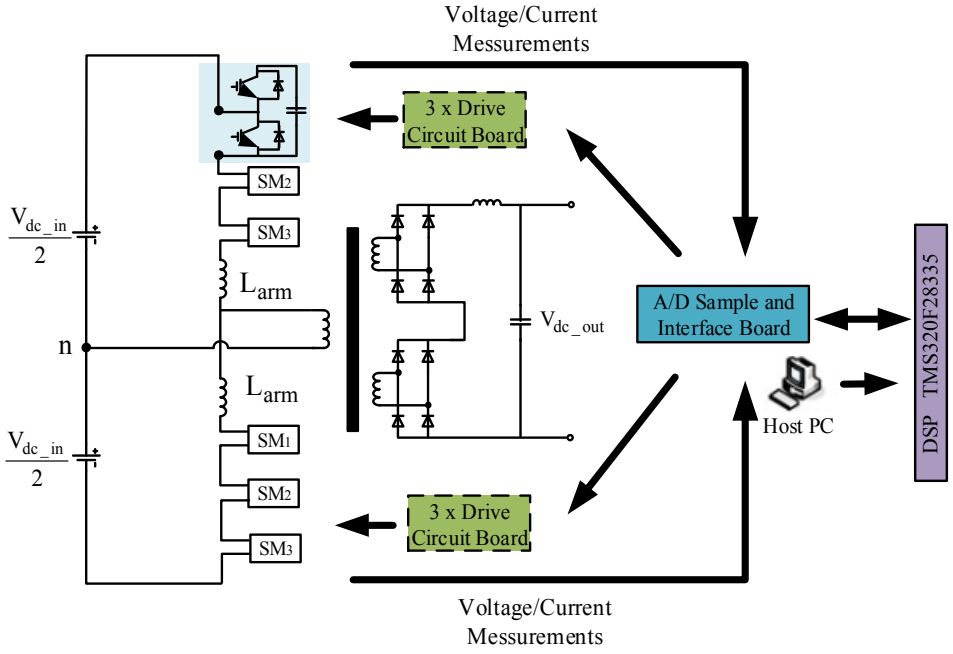


Figure 8.1 Schematic diagram of the control platform.

DSP-TI TMS320F28335 [146]: The TMS320F28335 digital signal processor is one of the TMS320C28X series of floating-point DSP controllers, as shown in figure 8.4, which is produced by Texas Instruments (TI). Compared with the fixed-point DSPs used in the past, this device has high accuracy, low cost, low power consumption, high performance, high integration of peripherals, large data and program storage, and more accurate and faster A/D conversion. The TMS320F28335 has a 150MHz high-speed processing capability, a 32-bit floating-point processing unit, up to 18 PWM outputs, 6 of which are unique to TI's more accurate PWM output (HRPWM), and a 12-bit, 16-channel ADC. Due to its floating-point unit, it can quickly write control algorithms without having to spend too much time and effort dealing with fractional operations, resulting in an average performance increase of 50% compared to previous generations of DSPs. It is also compatible with the fixed-point C28x controller software which has simplified software development, shortened development cycle and reduced development costs.

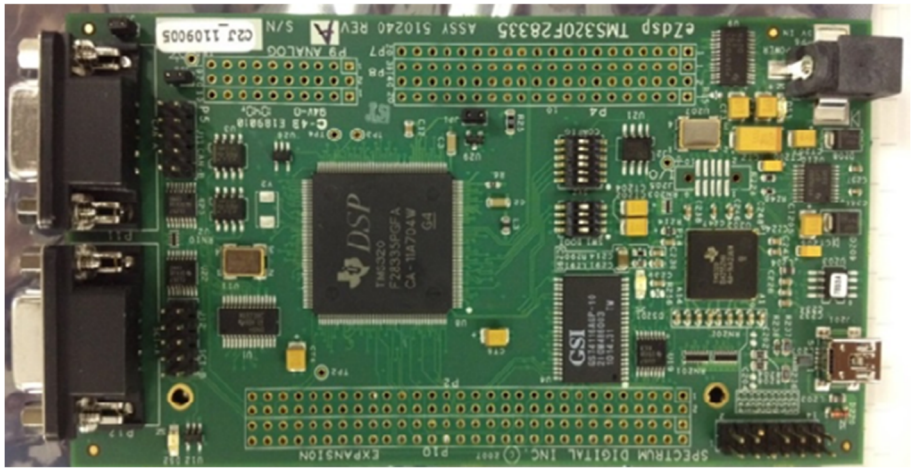
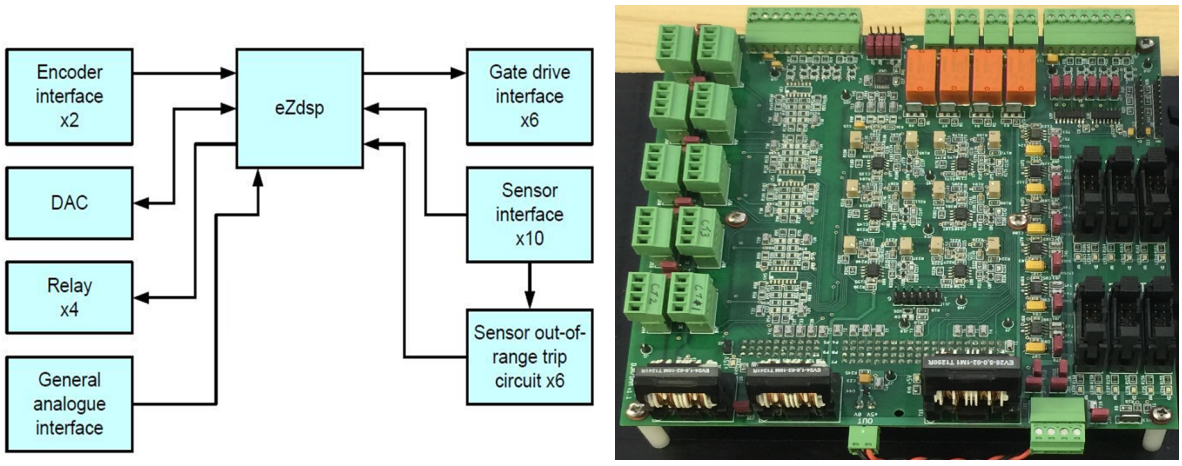


Figure 8.2 TMS320F28335 DSP controller board.

Interface Board: The interface board is designed to connect the DSPTMS320F28335 control board and the power converter hardware, which includes the four relay circuits, six drive circuit interfaces, ten sensor interfaces (ADC), the sensor out-of-range trip circuit, two encoder interfaces, 10 general analogue interfaces and one digital-to-analogue (DAC) interface as shown in figure 8.5. To avoid undesired noise, it is important to physically place the voltage/current sensors and drive circuits away from the power hardware. Therefore, the voltage/current sensors and drive circuits are not integrated on this interface board. However, the interface connectors on this board are designed to be flexible, which can cater for a wide range of different external sensors and gate drive circuits. In general, the external sensors can be directly connected to the sensor connectors on the board without the need for additional circuitry.



(a) (b)

Figure 8.3 Interface board: (a) schematic diagram (b) photograph.

Drive Circuit Board: The drive circuit board applied in this experimental platform includes two identical drive circuits and a common input control interface circuit, and they can operate independently or as a complementary pair as shown in figure 8.6. It should be noted that these two drive circuits on the board are completely isolated from each other to provide gate drive power.

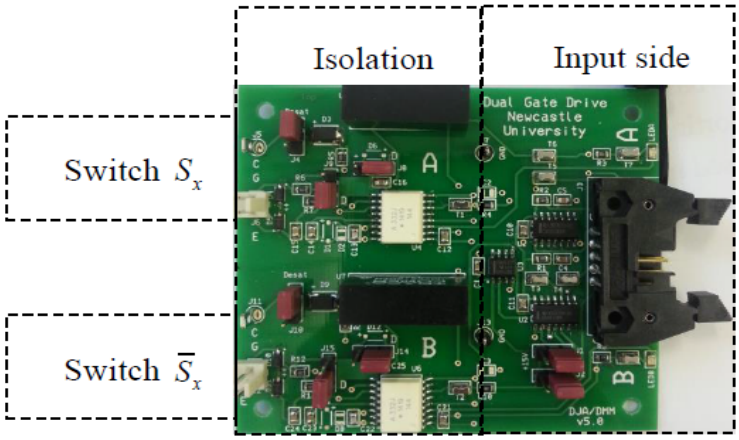


Figure 8.4 Drive circuit board.

8.5 Experimental Results

Low voltage scaled down laboratory prototype is developed to validate and confirm the simulation and the theoretical studies of the proposed converter and the performance of the proposed control strategies. Table 8.4 summarizes the main parameters of the experimental test-rigs, where platform one was built with a single transformer, and platform two was built with two transformers. It is worth noting that the carrier phase shift modulation and PI voltage balance control is shown in Chapter 3, as well as the dq close loop control shown in Chapter 4, comprise the overall control strategy of the experimental test-rigs. It is worth noting that the proposed converter is intended for high-voltage high-power applications; therefore, the simulation is presented for close-to-reality systems. However, implementing such a system in the laboratory is not feasible from the safety and the resources point of view, therefore scaled down prototype is developed as a proof of concept and to validate the proposed control methods and their effectiveness.

The components, SM number, and control system of the prototype were chosen with the following considerations:

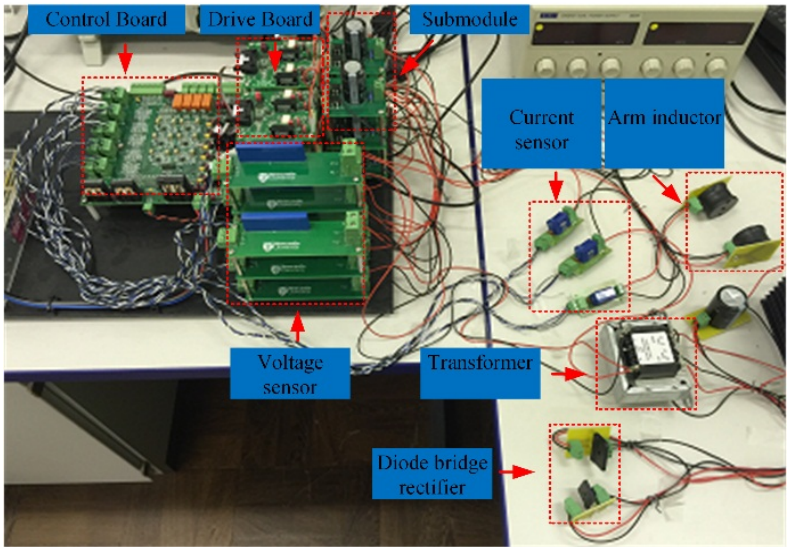
- The components of prototype including SM capacitors, arm inductors, and output filter can be calculated based on the equations shown in section 8.2, which have been detailed introduced, analyzed and calculated.
- The one-leg MMC is used for the primary side of the test-rigs, instead of using single-phase MMC, (e.g., two-legs) as shown in the simulation. This will help to reduce the number of submodules (only 3 SMs) and the control complexity of the test-rig but satisfy the validation of the proposed topology and its control strategy.
- Likewise, as the proposed converter is modular at both sides, only 2 diode-bridge rectifier models are considered at the secondary side for the platform-one, and only 4 diode-bridge rectifier models are considered at the secondary side for the platform-two which is enough to accommodate the requirement of the designed prototype. Once again, due to the modularity feature, this can be easily extended as presented in the simulation, if resources are available.
- As it can be seen from figure 8.7 and 8.14, the test-rigs are developed using the six drive circuit boards, seven voltage sensors, three current sensors, A/D Sample-Interface board, and TMS320F28335DSP control board. However, in real applications, where a large number of submodules is required, different arrangement may be needed, which include a higher number of control boards, more sophisticated controllers such as DSP, FPGA, and CPLD to meet these requirements. In general, most of the large-scale control systems are built by the company, such as ABB and SIEMENS.

Table 8.4 Parameters of experimental platforms

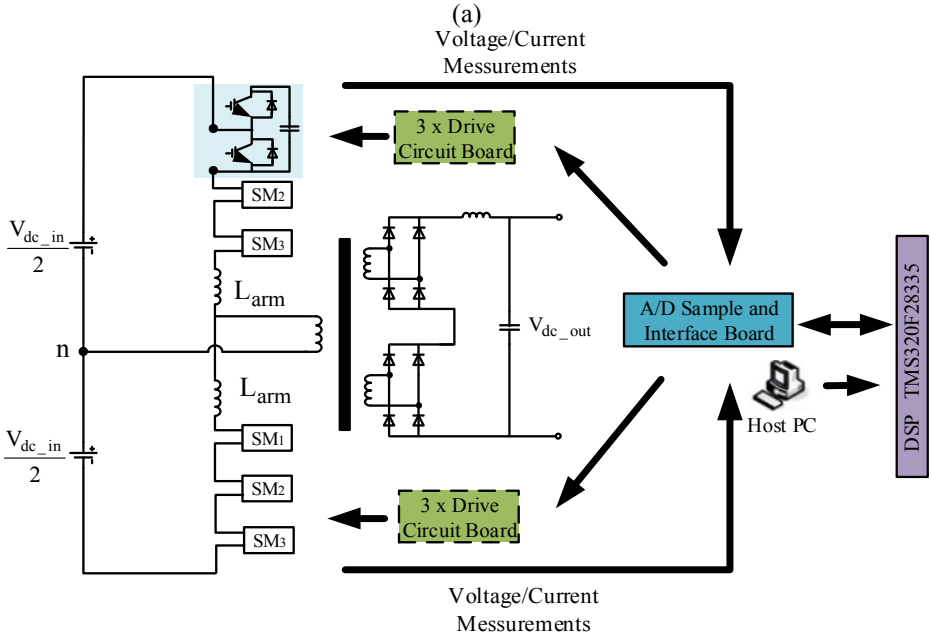
Parameters	Platform one (single transformer)	Platform two (two transformers)
Rated power	45W	90W
Input DC voltage	60V	60V
Output load resistor	20Ω	40Ω
Primary side AC peak voltage of the transformer	±25V	±25V
Primary number of half-bridge SMs per arm	3	3
Secondary number of diode-bridge-rectifier modules	2	4
Transformer number	1	2
Transformer ratio	1:1:1	1:1:1
SM capacitor of MMC	2.2mF	2.2mF
Arm inductor	0.1mH	0.1mH
Output capacitor	1mF	1mF
Output inductor	0.1mH	0.1mH
Switching frequency	2000Hz	2000Hz
AC frequency	400Hz	400Hz
Sampling rate (F28335)	20kHz	20kHz

8.5.1 *Experimental results of laboratory prototype with a single transformer*

Figure 8.7 shows the single transformer-based low-voltage scaled-down experimental test-rig and its schematic diagram, where a one-leg MMC (Phase-a only) consisting of three SMs per arm was used at the primary side. The output voltage is obtained through two series-connected diode-bridge rectifier modules at the secondary side of the transformer. In this work, a 400 Hz medium frequency transformer with double windings on the secondary side was used. The overall control system was developed using the TMS320F28335DSP control board.



(a)



(b)

Figure 8.5 Unidirectional single-phase modular multilevel DC/DC converter with single transformer: (a) scaled down laboratory prototype; and (b) schematic diagram.

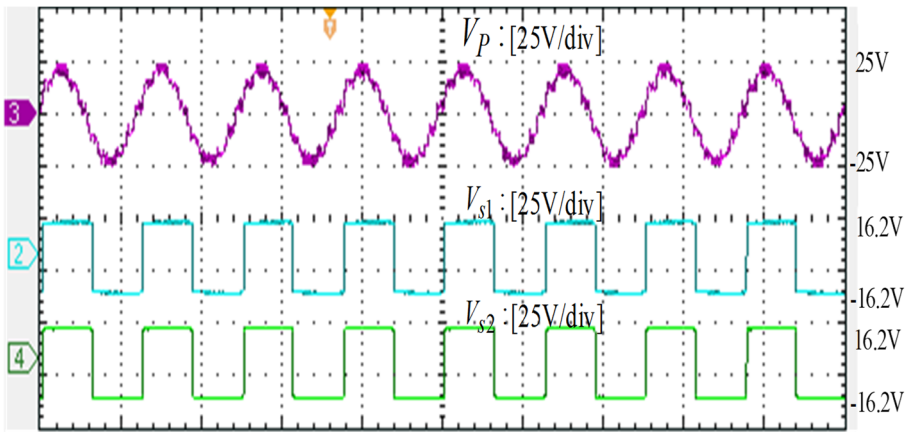
Figure 8.8 shows the steady-state performance of the proposed converter. The 400Hz AC voltages at the primary and secondary sides of the transformer are shown in figure 8.8(a) and the corresponding currents at the primary and secondary transformer are depicted in figure 8.8(b). It is worth noting that the peak of the secondary currents is just about half that of the primary one (i.e. $\frac{I_{p\_peak}}{2} \approx I_{s1\_peak} \approx I_{s2_{peak}}$), which effectively reduces the current rating of the associated diode-bridge-rectifier modules. This can be further reduced if more windings on the secondary side are considered. Figure 8.8(c) shows the experimental output DC voltage and

current waveforms of the proposed converter, which are perfectly smooth and regulated at a constant value, confirming the effectiveness of the proposed control system.

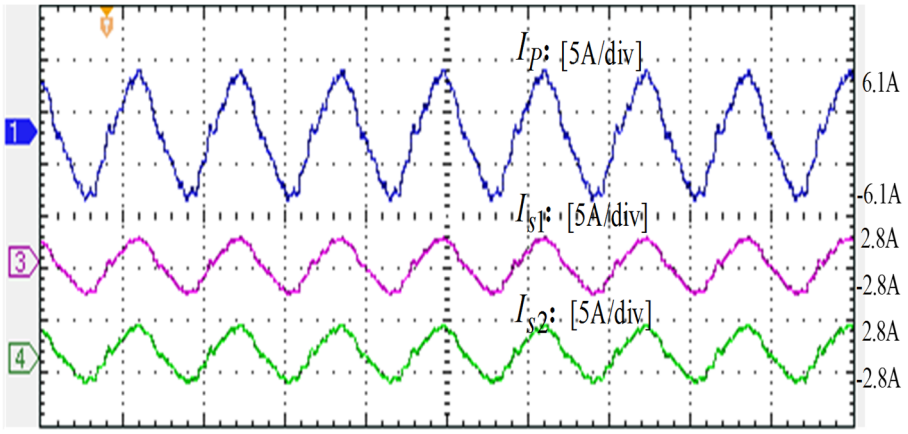
Figure 8.9 shows the performance of the SM voltage balance control, where it can be seen that the capacitor voltages are well-balanced and close to one-third of the DC input voltage (i.e. about 20V). Meanwhile, the voltage ripple of each SM is relatively small.

Figures 8.10 and 8.11 show the output voltage and current waveforms of the diode bridge rectifier modules at the secondary side of the proposed converter, where it can be seen that the output voltage of each diode bridge rectifier module is half of the output DC voltage, (i.e. about 15V).

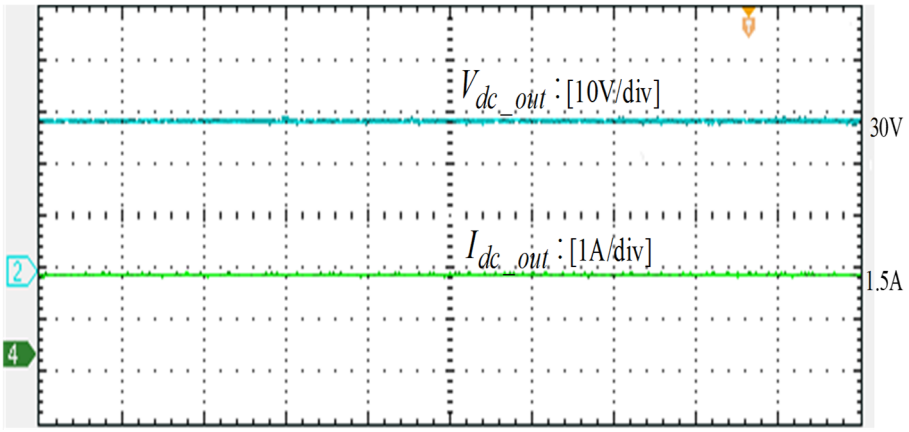
The dynamic performance of the system was experimentally validated with a 50% step change to the load as well. This can be seen in figure 8.12(a), where the output current of the secondary diode bridge rectifier modules changed immediately in response to the variations in the output load. Figure 8.12(b) shows the step change of the primary AC voltage and current, where the primary peak current changes from $I_{P\_peak} \approx \pm 6.1\text{A}$ (peak value of primary current) to $I_{P\_peak} \approx \pm 3\text{A}$ (peak value of primary current after a step change). At the same time, the primary peak voltage, V_{P_peak} remains controlled, which effectively demonstrates the excellent performance of the primary voltage control strategy. Consequently, the output DC current quickly decreased, and the DC voltage remained constant, as illustrated in figure 8.13. This further verifies the effectiveness of the proposed system and its control strategy.



(a) *Time*: [2ms/div]

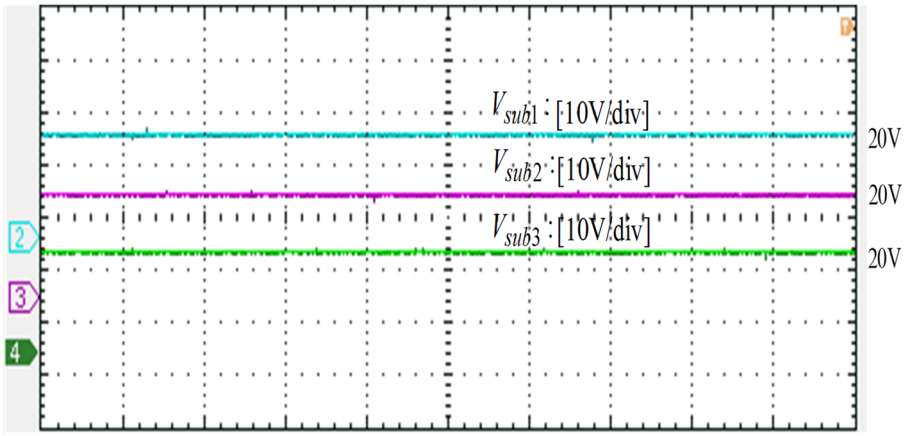


(b) *Time*: [2ms/div]

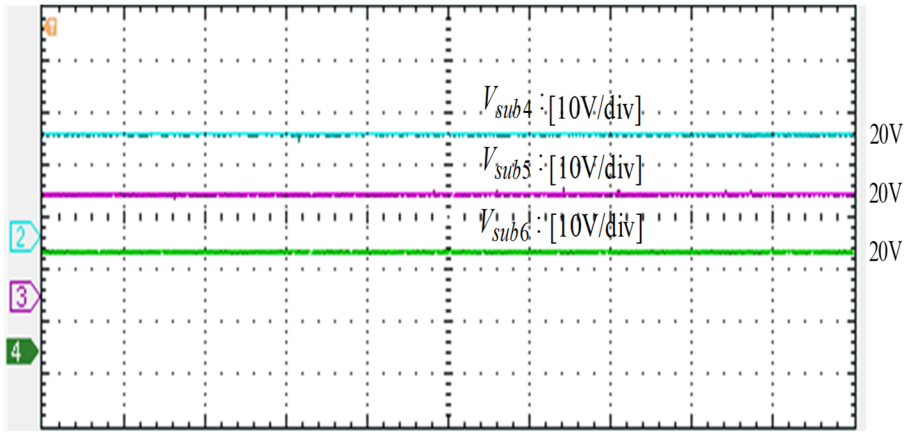


(c) *Time*: [20ms/div]

Figure 8.6 Performance at steady state: (a) transformer primary terminal voltage V_P and secondary winding-one voltage V_{s1} and winding-two voltage V_{s2}; (b) transformer primary current I_P and secondary winding-one current I_{s1} and winding-two current I_{s2}; (c) output DC current I_{dc_out} and voltage V_{dc_out}.

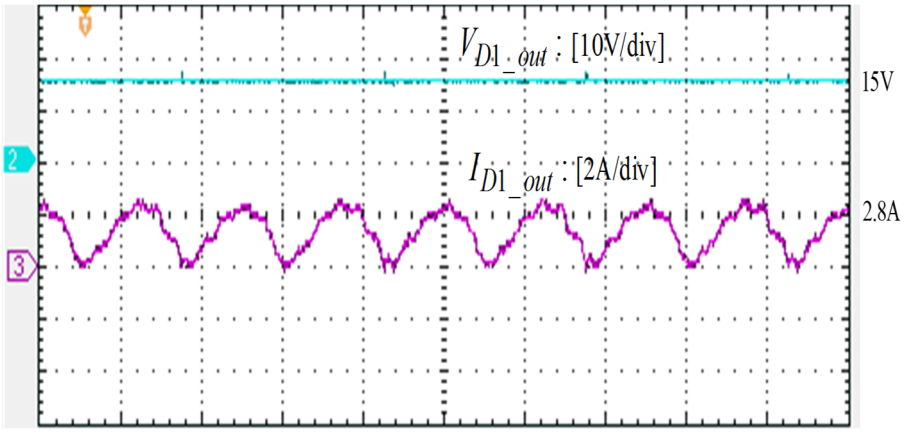


(a) *Time*: [40ms/div]



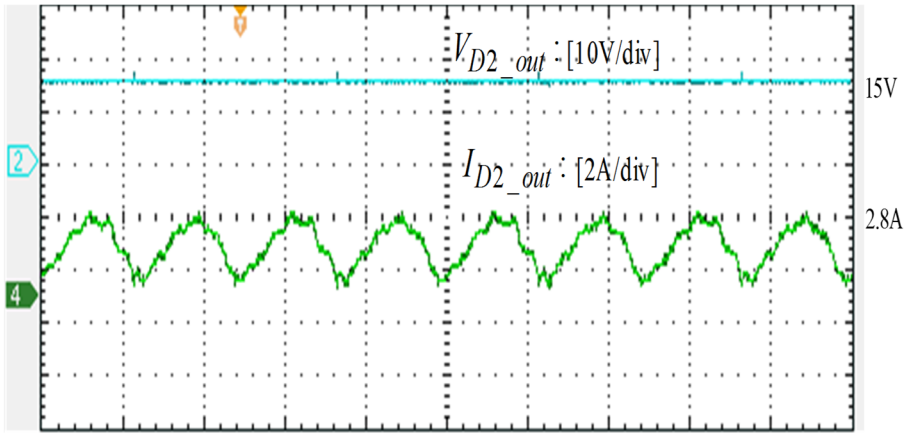
(b) *Time*: [40ms/div]

Figure 8.7 Performance at steady state, (a) upper arm SM voltages V_{sub1}, V_{sub2} and V_{sub3}; (b) lower arm SM voltages V_{sub4}, V_{sub5} and V_{sub6}.



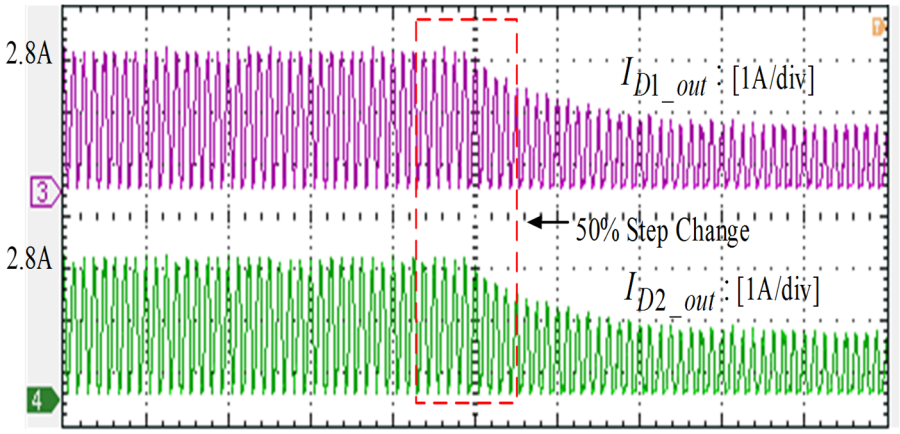
Time: [1ms/div]

Figure 8.8 Performance at steady state: output voltage and current waveforms: secondary diode-bridge-rectifier module-one.

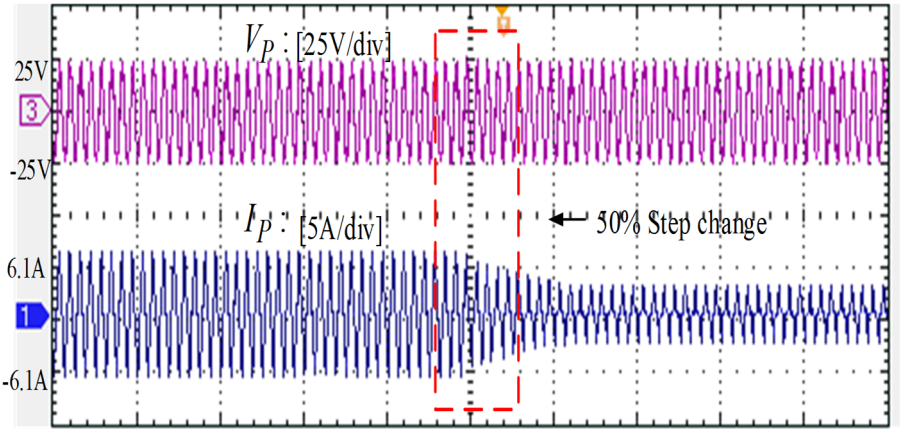


Time: [1ms/div]

Figure 8.9 Performance at steady state: output voltage and current waveforms: secondary diode-bridge-rectifier module-two.

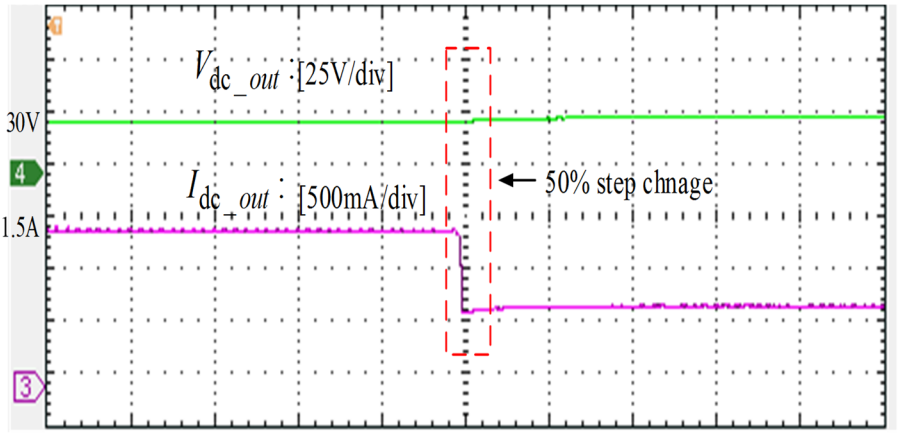


(a) *Time*: [10ms/div]



(b) *Time*: [20ms/div]

Figure 8.10 Dynamic response: (a) output current waveforms of secondary diode-bridge-rectifiers module-one I_{D1_out}, and module-two I_{D2_out}; (b) transformer primary terminal voltage V_P and current I_P.

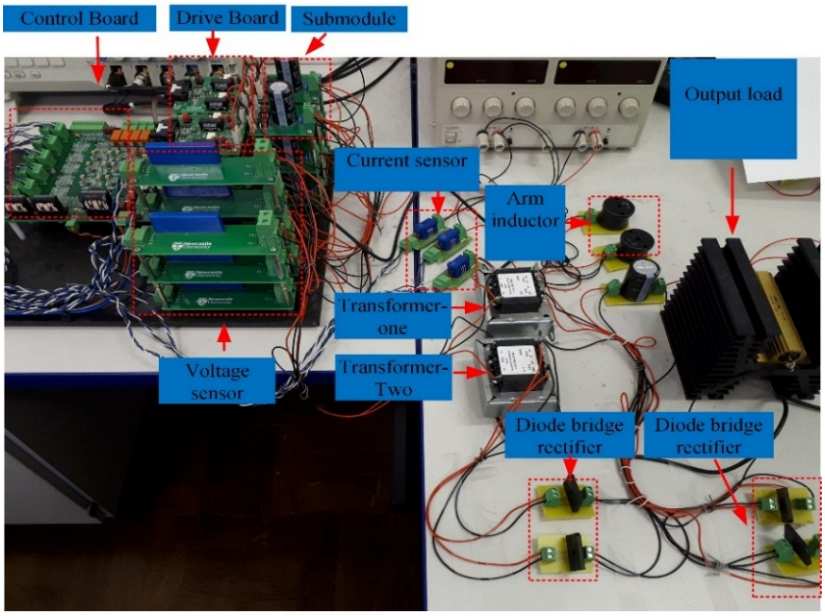


Time: [20ms/div]

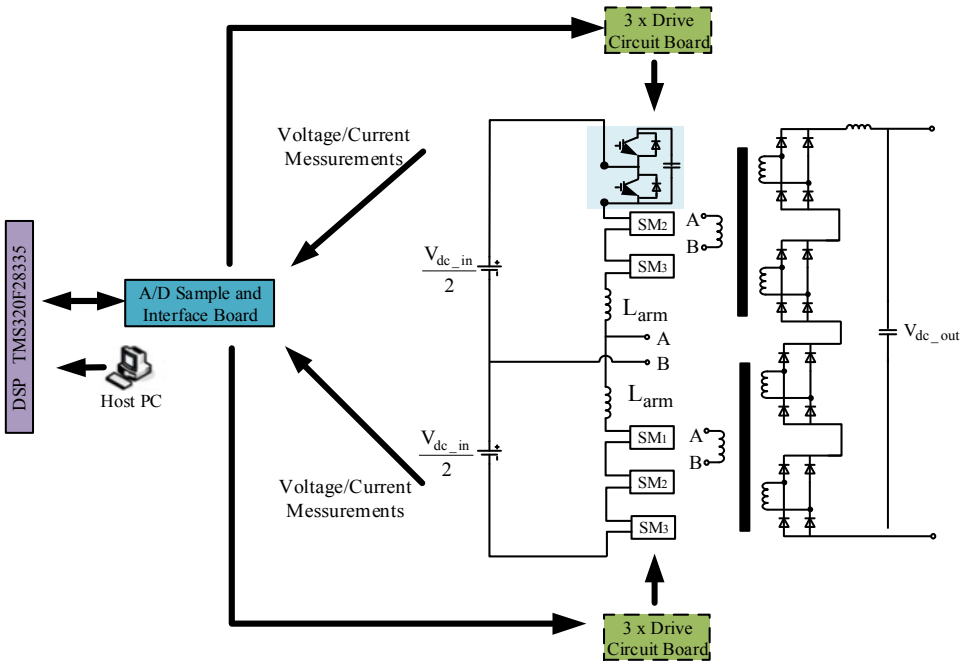
Figure 8.11 Dynamic response: output DC voltage V_{dc_out} and current I_{dc_out}.

8.5.2 *Experimental results of laboratory prototype with two transformers*

Figure 8.14 shows the low-voltage scaled-down experimental test-rig of the unidirectional modular multilevel converter based on two transformers and its schematic diagram, where a one-leg MMC (Phase-a only) consisting of three SMs per arm was used at the primary side.



(a)



(b)

Figure 8.12 Unidirectional single-phase modular multilevel DC/DC converter with two transformers: (a) scaled down laboratory prototype; and (b) schematic diagram.

The output voltage is obtained through the four series-connected diode-bridge rectifier modules at the secondary side of the transformer. In this work, two 400Hz medium frequency transformers with double windings on the secondary side are used. The overall control system was also developed using the TMS320F28335DSP control board.

Figures 8.15-8.19 show the steady-state performance of the proposed converter. The 400Hz AC voltages at the primary and secondary sides of the transformers are shown in figures 8.15 and 8.16, and the corresponding currents at the primary and the secondary side of transformers are depicted in figures 8.17 and 8.18. From the latter figures 8.17 and 8.18, it can easily be seen that the peak value of the secondary currents of each transformer is just half of the primary current (i.e. $\frac{I_{p1\_peak}}{2} \approx I_{s1\_peak} \approx I_{s2_{peak}}$), which effectively reduces the current rating of the associated secondary diode bridge rectifier module. Figure 8.19 shows the experimental output DC voltage and current waveforms of the proposed converter, which are perfectly smooth and regulated at a constant value, confirming the effectiveness of the proposed control system.

Figure 8.20 shows the performance of the SM voltage balance control, where it can be seen that the capacitor voltages are well-balanced and close to one-third of the DC input voltage (i.e. 20V). Meanwhile, the voltage ripple of each SM is relatively small.

Figures 8.21 and 8.22 show the output voltage and current waveforms of the diode bridge rectifier modules at the secondary side of the proposed converter, where it can be seen that the output voltage of each diode bridge rectifier module is one-quarter of the output DC voltage (i.e. about 15V).

The dynamic performance of the system was experimentally validated with a 50% step change to the load as well. This can be seen from figures 8.23 and 8.24, where the output current of the secondary diode bridge rectifier modules changes immediately as a response to the variations in output load. Figure 8.25 (a) shows the step change of the primary AC voltage and current, where the primary peak current changes from $I_{p\_peak} \approx \pm 12\text{A}$ (peak value of primary current) to $I_{p\_peak} \approx \pm 6\text{A}$ (peak value of primary current after a step change). At the same time, the primary peak terminal voltage, V_{p_peak} remains constant, which effectively demonstrates the excellent performance of the primary voltage control strategy. Consequently, the output DC current quickly decreased, and the DC voltage remains constant, as illustrated in

figure 8.25 (b). This further verifies the effectiveness of the proposed system and its control strategy.

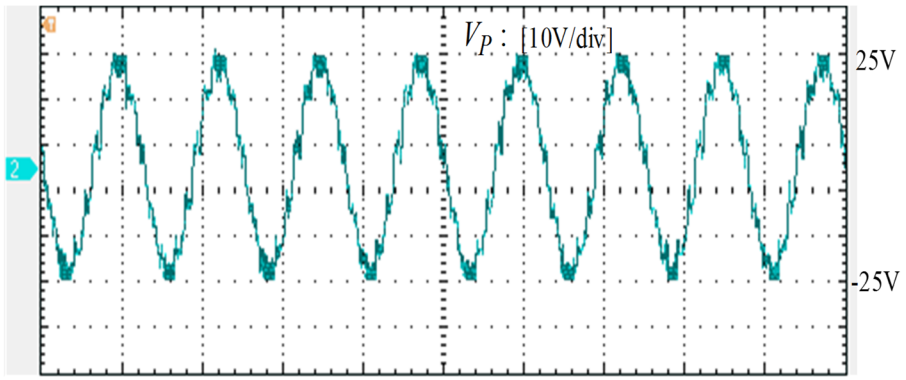
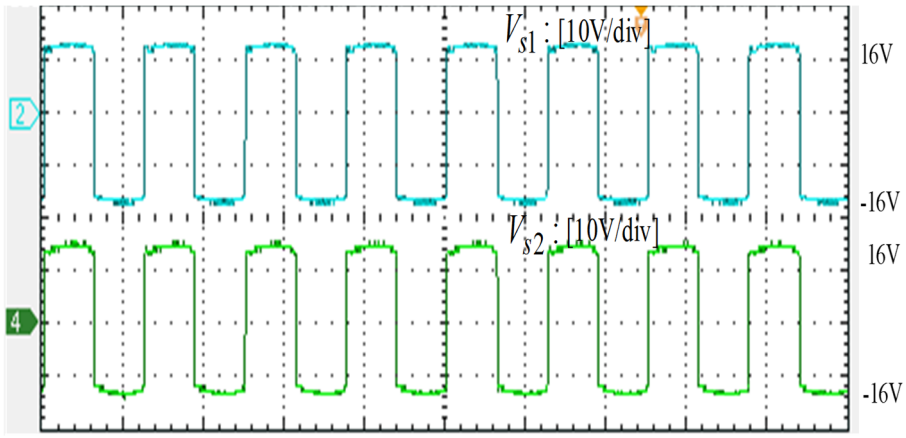


Figure 8.13 Performance at steady state: primary terminal voltage V_P.



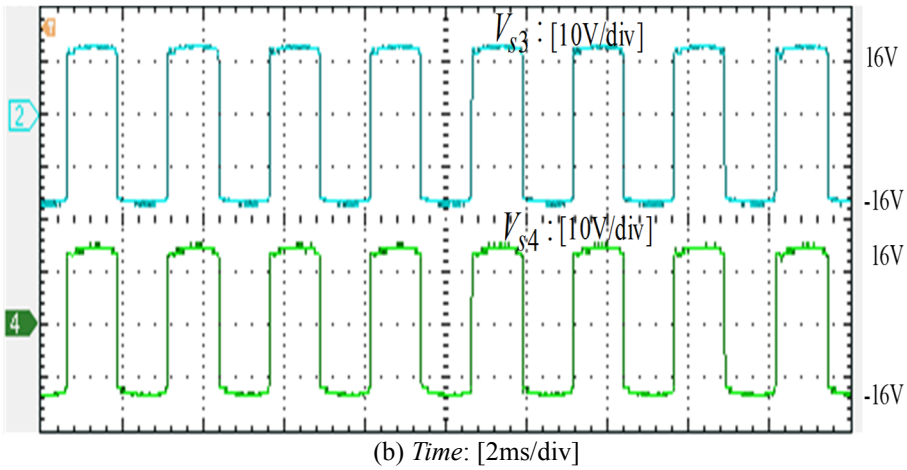


Figure 8.14 Performance at steady state: (a) transformer-one secondary winding-one voltage V_{s1} and winding-two voltage V_{s2}. (b) transformer-two secondary winding-one voltage V_{s3} and winding-two voltage V_{s4}.

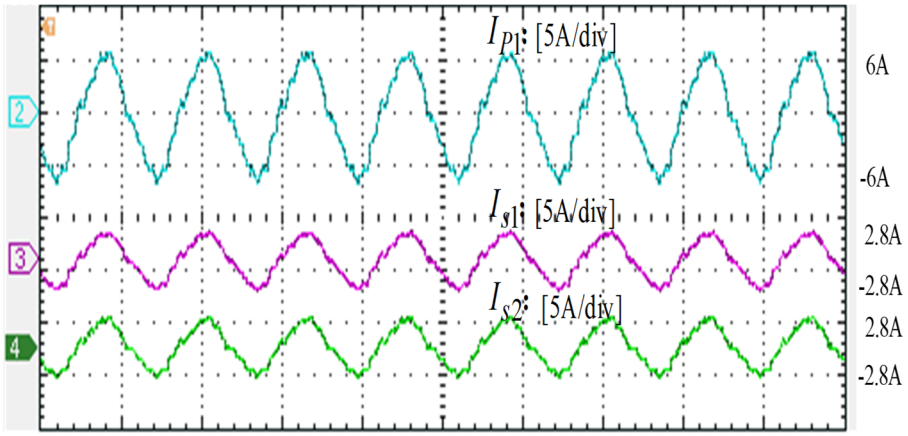


Figure 8.15 Performance at steady state: transformer-one primary current I_{P1} and secondary winding-one current I_{s1} and winding-two current I_{s2}.

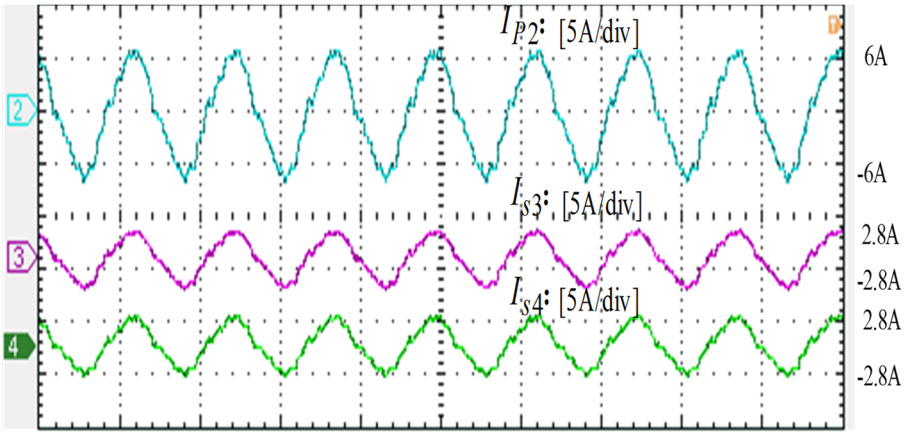


Figure 8.16 Performance at steady state: transformer-two primary current I_{P2} and secondary winding-three current I_{s3} and winding-four current I_{s4}.

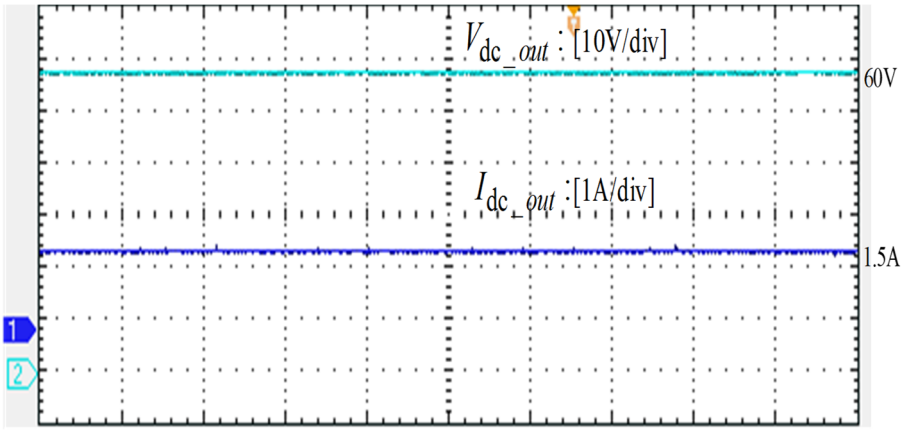
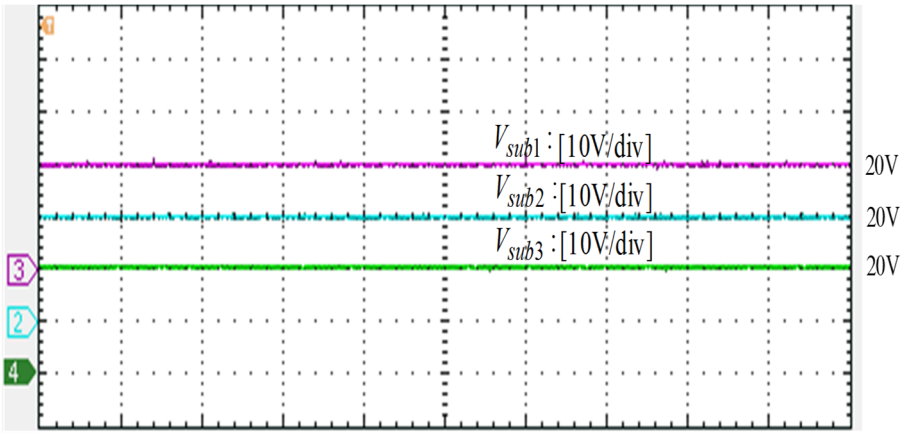
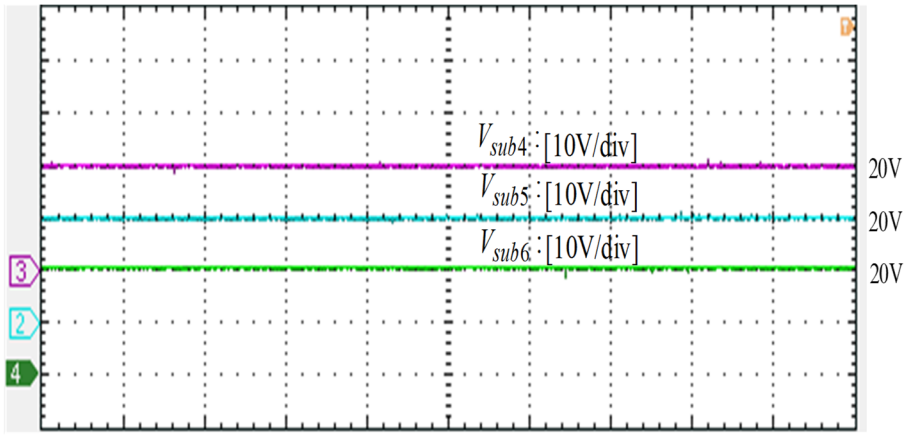


Figure 8.17 Performance at steady state: proposed converter output DC current I_{dc_out} and voltage V_{dc_out}.

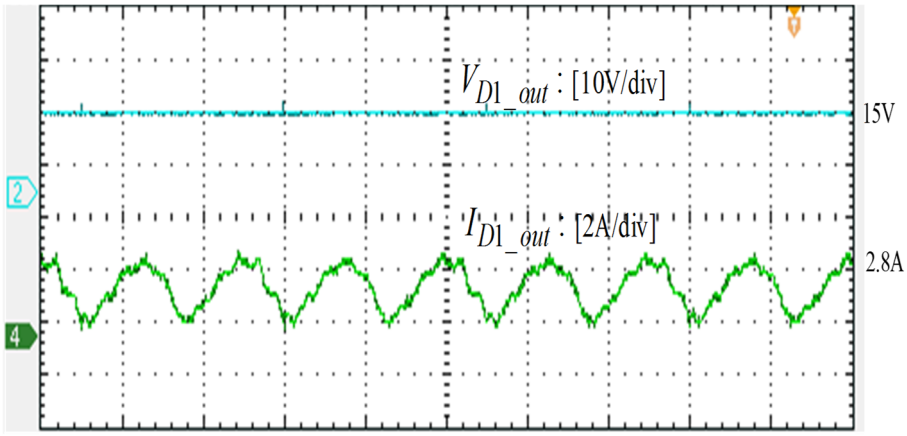


(a) *Time*: [40ms/div]

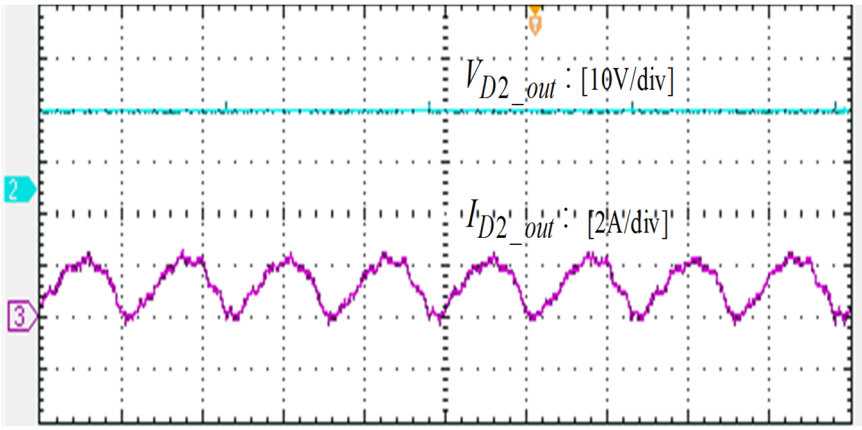


(b) *Time*: [40ms/div]

Figure 8.18 Performance at steady state: (a) upper arm SM voltages V_{sub1}, V_{sub2} and V_{sub3}; (b) lower arm SM voltages V_{sub4}, V_{sub5} and V_{sub6}.

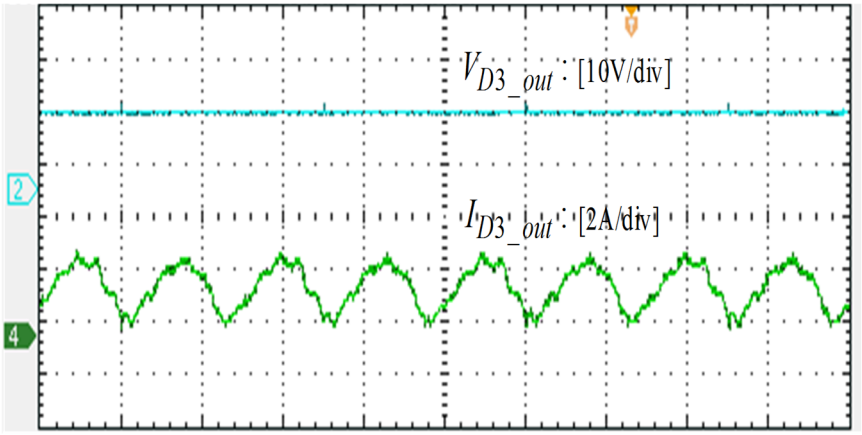


(a) *Time*: [1ms/div]

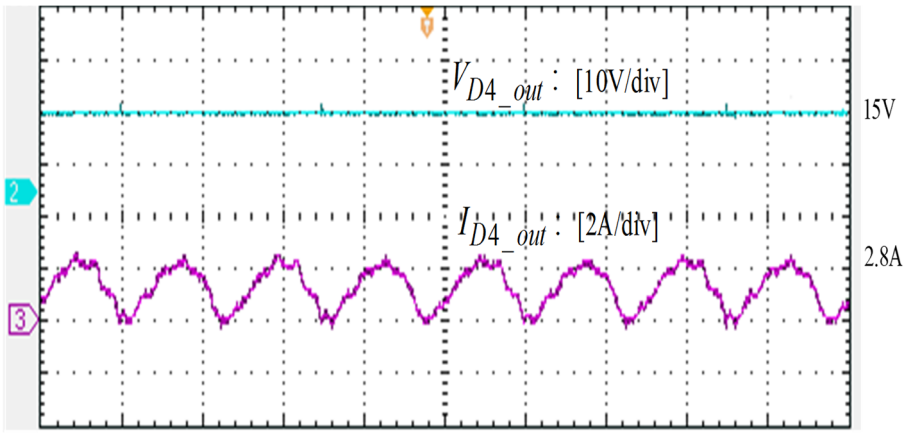


(b) *Time*: [1ms/div]

Figure 8.19 Performance at steady state: output voltage and current waveforms of (a) secondary diode-bridge-rectifier module-one; (b) secondary diode-bridge-rectifier module-two.

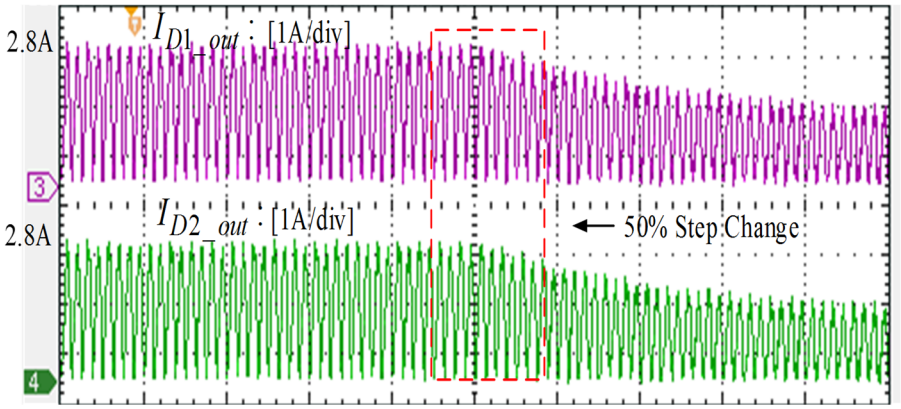


(a) *Time*: [1ms/div]



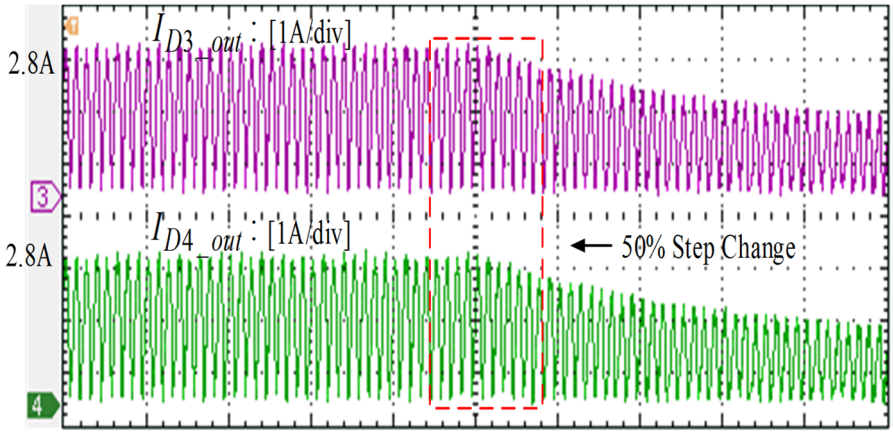
(b) *Time*: [1ms/div]

Figure 8.20 Performance at steady state: output voltage and current waveforms of (a) secondary diode-bridge-rectifier module-three; (b) secondary diode-bridge-rectifier module-four.



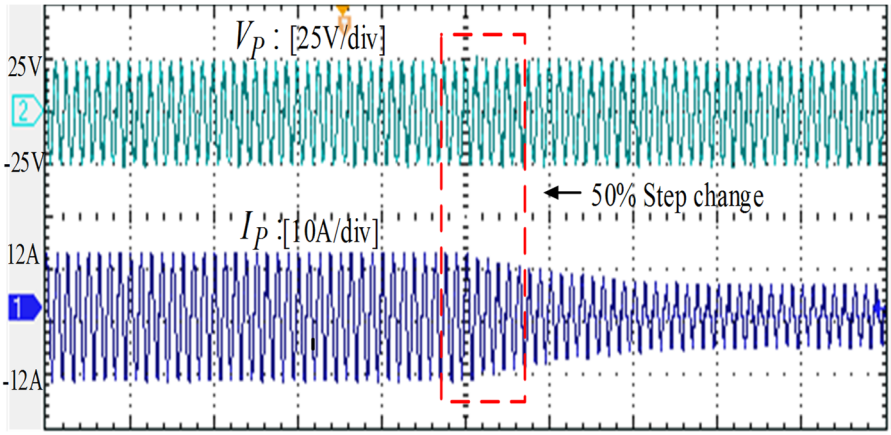
Time: [10ms/div]

Figure 8.21 Dynamic response: output current waveforms of secondary diode-bridge-rectifier module-one I_{D1_out}, and module-two I_{D2_out}.

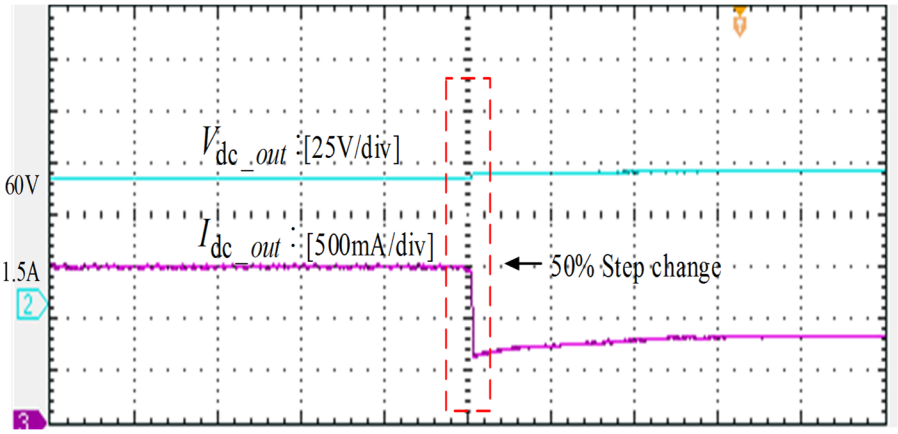


Time: [10ms/div]

Figure 8.22 Dynamic response: output current waveforms of secondary diode-bridge-rectifier module-one I_{D3_out}, and module-two I_{D4_out}.



(a) *Time*: [20ms/div]



(b) *Time*: [20ms/div]

Figure 8.23 Dynamic response: (a) transformer primary terminal voltage V_P and current I_P; (b) output DC voltage V_{dc_out} and current I_{dc_out}.

8.6 Summary

This chapter reports the development and testing of small laboratory prototypes of the proposed unidirectional single-phase modular DC/DC converter. Also, a detailed introduction to the passive components, such as arm inductors, SM capacitors, output filters and medium frequency transformer, all of the control systems for the laboratory prototypes are also described. Finally, the typical experimental results of the proposed unidirectional single-phase DC/DC converter are presented.

Chapter 9. Conclusion and Future Work

9.1 Conclusions

The focus of this thesis has been to develop more modular multilevel DC/DC topologies which can enable the connection of off-shore wind farms with high voltage direct current (HVDC) transmission systems to achieve high voltage DC/DC conversion. The main conclusions of this thesis are summarized as follows：

In Chapter 4, a unidirectional single-phase modular DC/DC converter was developed, which features modularity, expandability, galvanic isolation, and lower device voltage and current ratings. A mathematical model of the proposed unidirectional single-phase modular DC/DC converter was developed. Based on this model, the detailed output power characteristics of the converter are derived. The results illustrate that the power transfer capability of the proposed converter is influenced by the modulation index M_1, and the phase shift angle φ, where the highest power is achieved with a unity modulation index. A control method based on a *dq* rotating reference frame was then developed for the proposed converter. Since the *dq* rotating reference frame control method is generally used for three-phase AC systems, therefore a phase shift is necessary for the proposed single-phase system to achieve the PARK transformation. The topology and control method are validated by simulation and experimental results shown in Chapter 8 confirming the excellence of its performance.

In Chapter 5, a unidirectional three-phase modular DC/DC converter was proposed. A special decoupled medium frequency transformer was used in this topology, which decouples the primary three-phase AC system into three individual phases. Using an analytic process similar to that in Chapter 4, a mathematical model of the proposed unidirectional three-phase modular DC/DC converter is developed. The output power characteristics of the converter are then analyzed in detail. Although the proposed unidirectional three-phase modular DC/DC converter has a different configuration from the proposed unidirectional single-phase modular DC/DC converter described in Chapter 4, they both exhibit similar output power characteristics. The power transfer capability of both converters is influenced by the modulation index M_1 and the

phase shift angle φ, where the highest power is achieved with a unity modulation index. However, compared with the proposed unidirectional single-phase modular DC/DC converter, the proposed unidirectional three-phase modular DC/DC converter is more suitable for high-power applications since the three-phase MMC is used at the primary side. A control strategy based on the *dq* rotating reference frame was then proposed which can act directly on the proposed unidirectional three-phase modular DC/DC converter without the requirement of a phase shift. The performance of the proposed converter and its control strategy are also validated through various simulation results.

In Chapter 6, a bidirectional three-phase modular DC/DC converter was proposed. Similar to the proposed unidirectional three-phase modular DC/DC converter described in Chapter 5, a decoupled transformer was also employed in the topology. Unlike the unidirectional converters proposed in Chapter 4 and 5, the output power of the proposed bidirectional DC/DC converter can be divided into two sections for analysis; when $-\pi \leq \varphi \leq 0$, power is transferred from the high voltage side to the low voltage side, and when $0 \leq \varphi \leq \pi$, power is transferred from the low voltage side to the high voltage side. The power transfer capability of the proposed converter is influenced by the modulation index M_1 and M_2 as well as the phase shift angle φ. Two different *dq* vector control strategies were developed for the primary and secondary side of the proposed converter. However, since a one-leg MMC-based module is used at the secondary side, a phase shift is necessary to achieve the PARK transformation as mentioned in Chapter 4.

In Chapter 7, the proposed unidirectional and bidirectional DC/DC converters were compared with existing DC/DC converter competitors. As expected, the proposed unidirectional single-phase and three-phase DC/DC converters show better performance in many respects compared with unidirectional ISOS and IPOS converters, especially in terms of losses and component utilization. The total losses of the proposed unidirectional single-phase DC/DC and proposed unidirectional three-phase DC/DC converters are much smaller than in the unidirectional ISOS converter but slightly greater than the unidirectional IPOS converter. However, the number of IGBT modules employed in the IPOS converter is much larger than any of the other three DC/DC converters. On the other hand, the proposed bidirectional three-

phase converter increases efficiency by 1% compared to its bidirectional counterpart cascaded bidirectional ISOS and IPOS converters for the whole range of output power. The number of IGBT modules employed in the proposed bidirectional three-phase converter is substantially reduced compared with the conventional bidirectional three-phase DC/DC converters.

9.2 Further Work

1) The basic building block of the MMC employed in the proposed converters is a half-bridge-based SM (HBSM). However, an HBSM-based MMC (HB-MMC) does not have a DC fault blocking capability, and thus additional circuit breakers are necessary to isolate DC faults. This increases the complexity of the converter and thereby its reliability decreases. To address the issues of DC faults, several approaches can be used with an MMC-based circuit topology, one of which is to use a full-bridge SM configuration [137]. In further research, this would be a good option in investigating how to further enhance the proposed topology by incorporating DC fault clearance capability.

2) To reduce the size of the proposed converters, the medium frequency is employed in operating the system, but this will increase switching losses and thereby decrease efficiency. To address this issue, several papers such as [138] have referred to soft-switching techniques for MMCs, which can effectively decrease switching losses and thereby further improve efficiency. In further research, it would be worth investigating how to further enhance efficiency by introducing soft-switching techniques to the proposed converters.

3) In this thesis, three different modular DC/DC converters have been proposed. Detailed theoretical analyses are presented and thoroughly discussed based on sinusoidal modulation method, such as carrier phase shift modulation (CPS-PWM). However, based on different modulation methods like square modulation and triangular modulation, the converters would present different characteristics, especially in terms of power transfer capability and loss evaluation. In further research, the operational characteristics of the proposed converters employing different modulation methods should be investigated; for example, sinusoidal modulation, square modulation, and triangular modulation.

4) Due to the limited resources and laboratory safety measures in this study, the experimental testing in this thesis is based on a scaled-down experimental platform. In future research, it would be useful to perform experimental tests based on a high-voltage high-power prototype which could be bought directly from ABB or Siemens.

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