DC Treasure Box

ELECTRICAL ENGINEERING DEPARTMENT
California Polytechnic State University
Senior Project 2020

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Abstract

An all in one DC resource would enable electronics students to prototype circuits for labs and projects without the need for the lab equipment present on campus. The labs on campus can be physically far, closed, or overcrowded, preventing students from accessing the equipment. Roughly 75% of upper division electrical engineering students do not own power supplies, with even fewer students owning a source measurement unit (SMU). There is a significant need for a product capable of providing standard lab equipment functionality. The functionally this project provides are positive and negative DC power supplies, 4-Quadrant SMU, analog inputs and outputs, digital inputs and outputs, and other multimeter like functionality. This functionality capable of acting autonomously allowing for fast measurement sweeps. These measurement sweeps can be used for the characterization of circuits or components. Characterization and validation of circuits can save lab time and aid in debugging.

1 Intro

> Either write something worth reading or do something worth writing.
>
> *Benjamin Franklin*

Lab equipment is fundamental to the design of any circuit. Power supplies provide voltage and currents to turn on and bias components. Multimeters measure different physical quantities. SMUs can characterize non-linear components. Lab equipment is critical to anyone working with electronics. The purpose of this project is providing a reliable adjustable DC supply and measurement setup that can emulate the capabilities of more advanced lab equipment. The project is used for powering, testing, and characterizing DC circuitry.

2 Customer Needs Assessment

> It is always great when people take interest in your work.
>
> *Margaret H. Hamilton*

When building circuits, either as a electronics hobbyist, student, or professional, it is important to own an adjustable power supply that provides the proper voltages and currents needed. Additionally, multimeters are crucial to take various measurements to verify that a circuit is biased correctly and operating as expected. This equipment, alongside oscilloscopes and function generators, can be expensive and bulky 1-2. This senior project aims to satisfy the need for an adjustable power supply and multimeter whilst staying relatively cheap and compact.

To ensure that this product is desirable to the target markets, a survey given to 30 upper division EE/CPE students attending Cal Poly San Luis Obispo drove the requirements and functionality of the project 30. Questions included indicating desired power supply voltage and current range, multimeter resolution, additional functionalities, and price.

The survey showed a high importance placed on ohmmeter functionality and power supplies with adjustable current limits, with at least 85% of surveyed students stating both having an ohmmeter is important and they use current limits with lab equipment.

Additional customer needs are drawn from the electronics lab series given during the course of undergraduate studies at Cal Poly. The capabilities of the project allow it to characterize components and achieve proper DC-biasing for any circuit given during the electronics lab series. Miscellaneous features such as a continuity checker provide quality of life.

Other customer needs come from analyzing the capabilities of existing benchtop and portable DC resources such as the Agilent E3631A power supply, Keithley 2400 Sourcemeter, and the Analog Discovery 2. The DC Treasure Box is expected to provide performance mimicking some of the capabilities and features of these devices. The product directly competes with Analog Discovery 2, commercial multimeters, and commercial power supplies. It is seen as an alternative to these products, abet somewhat more limited in some aspects.

The Agilent E3631A and Keithley 2400 are far too expensive and advanced to be replaced with this product 3-4. The DC Treasure Box is a much less powerful, much less expensive version of these products and can be seen as entry lab equipment capable of meeting the demands of the consumer market. Agilent and Keithley target the professional and educational sectors, which drive both their impressive specifications and high price point.

Market research done for this project came from a survey given out to Cal Poly students. Section 9.4 in the Appendices shows the survey and complete dataset. Table 2.1 shows selected results at a glance. As part of a project for IME 305 (Operations Research II), the author used a linear programming optimization model to determine the best specifications to focus on given limited time and budget. However, this model was made during Spring Quarter and had no role in determining the specifications. Section 9.5 shows the results of the model.

Table 2.1. Selected Survey Responses

Specification:	**Highest Response**	**% of Response**
Power Supply Voltage Range	-12 – 12V	56.7%
Power Supply Current Range	>1 A	50%
Multimeter Resolution	50µV	43.3%
Current Limiting	Yes	83.3%
Ohmmeter	Yes	86.7%

Table 2.2. Power Supply Specifications

Marketing Requirements	Engineering Specifications	Justification
1) 2) 3) 5)	The DC power supply has three voltage outputs ranges ■ 0V — +6V ■ 0V — +12V ■ 0V — -12V	These voltage ranges encompass what is needed in the electronics laboratory classes. 60% of students surveyed stated +-12V is enough for a power supply. Higher voltages would increase system costs as well as power costs. 40V differential is classified as high voltage.
1) 4)	Each output has adjustable output level settings ■ Minimum setting resolution is 100mV with a minimum accuracy of ±10mV	Adjustable supplies are more flexible and desirable than static output supplies.
5)	Each output can source/sink 100mA maximum continuously	This corresponds to ~1.2W of maximum power on the 12V supply. More than this and the terminal dissipation of components/ICs might not be suitable.
1) 2) 3)	Each output has adjustable current limit settings ■ Settings range from 0mA to 100mA in 1mA increments with an accuracy of ±0.1mA	95% of surveyed students used current limits when building circuits. This is an important feature valuable to the target customers. Current control is necessary in preventing damage to components due to wiring errors.
1) 5)	System is capable of supplying a continuous power of 3W maximum	3W is more than enough to power all student circuits done in lab. 3W is not taxing on the power budget of 15W.
1) 4)	+12V and -12V rails are able to form a split supply scheme	Dual supplies are useful for laboratory settings.

Marketing Requirements

1. System can be used in circuit laboratory classes for the DC biasing/testing of circuits.
2. System cost is under $170, the average price the average student would pay for the product.
3. System runs off USB-C at 5V and 3A for a total power of 15W.
4. System has features desirable to the target market.
5. System is feasible to create in a 9 month period.

Table 2.3. Source Measure Unit Specifications

Marketing Requirements	Engineering Specifications	Justification
1) 4) 5)	System has a voltage range of ±10V System has a current range of ±100mA	±10V and ±100mA is suitable for the characterization of typical semiconductor devices. +10V and +100mA is suitable for powering IC for making quiescent current measurements.
1) 4)	System can force voltage and measure current System can force current and measure voltage	These features define an SMU and allow for characterization of circuits.
1) 4)	SMU has adjustable output level settings ■ Voltage setting resolution is <100mV with an accuracy of <±10mV ■ Minimum current setting resolution is 1mA with an accuracy of <±0.1mA	Adjustable supplies are more flexible and desirable than static output supplies.
1) 4)	SMU has adjustable output limit settings ■ Minimum voltage limit setting resolution is 100mV with an accuracy of ±10mV ■ Minimum current limit setting resolution is 1mA with a minimum accuracy of ±0.1mA	Current and voltage limits are crucial for avoiding damage to circuity.
3) 5)	System is capable of delivering/absorbing a continuous power of 1W maximum	Power delivery/absorption greater than 1W will increase the size of the device or necessitate a fan. 1W does not overtly draw upon the power budget.

Marketing Requirements

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4. System has features desirable to the target market.
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Table 2.4. Analog Input Output Specifications

Marketing Requirements	Engineering Specifications	Justification
1) 4)	System has 4 input pins ■ 2 ±10V pins ■ 2 ±5V pins System has 4 output pins ■ 2 ±10V pins ■ 2 ±5V pins	4 input pins allow for 4 voltage measurements to be taken simultaneously. Important nodes can be measured without having to move leads around. 4 output pins allow for simple DC biasing of nodes. Otherwise resistive dividers or DC power supplies are needed to get variable voltages to nodes.
1) 2) 4) 5)	±10V IO pins have a voltage resolution of <100µV and an accuracy of <±100µV ±5V IO pins have a voltage resolution of <50µV and an accuracy of <±50µV	90% of students surveyed selected 50µV or greater as the minimum voltage resolution desired from a voltmeter, and 45% selected 100µV or greater. Greater resolution requires more expensive ADC/DACs.
1) 4)	Input pins have an input impedance of >1MΩ	Voltmeters are modeled as open circuits, as such should have a high input impedance as to not load the circuit measured or affect readings.
1) 4)	Output pins can supply/sink 10mA of current	Analog outputs aren't meant to drive heavy loads, but should be capable of sourcing/sinking small amounts of current.

Marketing Requirements

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Table 2.5. Digital Input Output Specifications

Marketing Requirements	Engineering Specifications	Justification
1) 4)	System has 4 input pins ■ 4 0V — +5V pins System has 4 output pins ■ 4 0V — +5V pins	4 input pins allow for 4 logic reads to be taken simultaneously. 4 output pins allow for 4 logic outputs to be measured simultaneously. Multiple stages of a digital circuit can be probed to see intermediate logic and debug errors.
1) 4)	Input pins have configurable V_{IH}/V_{IL} Output pins have configurable V_{OH}/V_{OL}	Different logic voltages are used in the electronics series, each logic family studied should be measurable.
2) 5)	Configurable $V_{IH}/V_{IL}/V_{OH}/V_{OL}$ has a voltage resolution of <20mV and an accuracy of <±10mV	Logic voltages don't need to be measured to great precision. Resolution matters less as logic voltages have large swing.
1) 4)	Input pins have an input impedance of >1MΩ	Avoid loading digital circuits and thereby preserving predicted fan-out.
1) 4) 5)	Output pins can drive a 1000pF ‖ 2kΩ load with rise/fall times of 1µs	Fast transition times may be necessary to the operation of a digital circuit. Load conditions are based on common loading conditions other digital outputs are tested under.

Marketing Requirements

1. System can be used in circuit laboratory classes for the DC biasing/testing of circuits.
2. System cost is under $170, the average price the average student would pay for the product.
3. System runs off USB-C at 5V and 3A for a total power of 15W.
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3 Planning

> Above all, don't fear difficult moments. The best comes from them.
>
> *Rita Levi-Montalcini*

Due to the project's somewhat ambitious nature careful thought is put into the total system design. These considerations include power, communication, and design flexibility.

Tradeoffs are made, ensuring the project is feasible for a single undergraduate student to make over the course of less than a year with a budget of a few hundred dollars. Typical power supplies can deliver large amounts of power. The power supplies for this project are far weaker than those on the market. Each power supply can only deliver about 2 watts of power. As the project's purpose is providing a cheap, portable lab environment capable of completing undergraduate laboratory experiments.

Market SMUs and multimeters can of measure (or in the SMU's case, output) kV level signals. The SMU built in this project can only measure/supply voltages from -10V — 10V, and currents of 500µA - 100mA. The upside is that the SMU in this project is built for less than $100, and by a single person.

Each subsystem is designed independently of the other systems. This is done to facilitate the design process; isolating any changes to a subsystem to that block only. The exception of this is each subsystem must interface with serial peripheral interface (SPI) for communication to the microcontroller. SPI is chosen because most digital to analog converters (DACs) and analog to digital converters (ADCs) use SPI for its fast data rates and simple protocol. This method also saves on processing time, as the microcontroller does not need to regulate any other subsystems, it only needs to send and receive data periodically. This vastly simplifies the code the microcontroller executes.

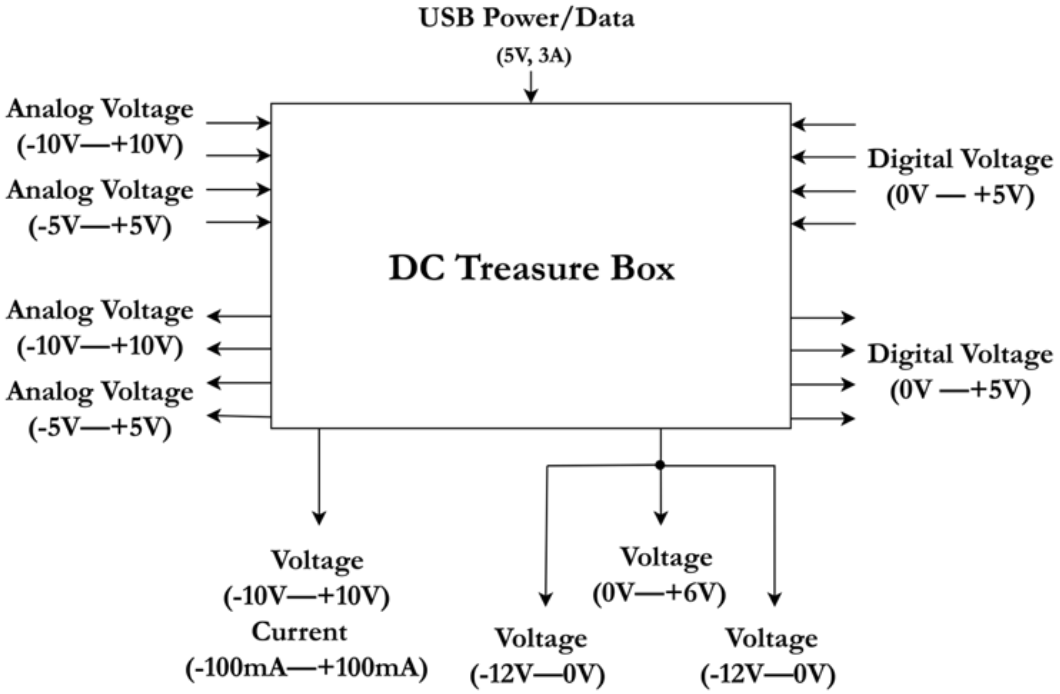


Figure 3.1. Full System Black Box Diagram

Table 3.1. Total System Description

Module	Full System
Inputs	Analog Voltage (-5V—+5V) (x2) Analog Voltage (-10V—+10V) (x2) Digital Voltage (0V—+5V) (x4) USB-C (+5V, 3A) USB-C (Data)
Outputs	Analog Voltage (-5V—+5V) (x2) Analog Voltage (-10V—+10V) (x2) Digital Voltage (0V—+5V) (x4) USB-C (Data) Analog Voltage/Current (-10V—+10V/-100mA—100mA) Analog Voltage (0V—+6V) Analog Voltage (0V—+12V) Analog Voltage (-12V—0V) Data (USB-C)

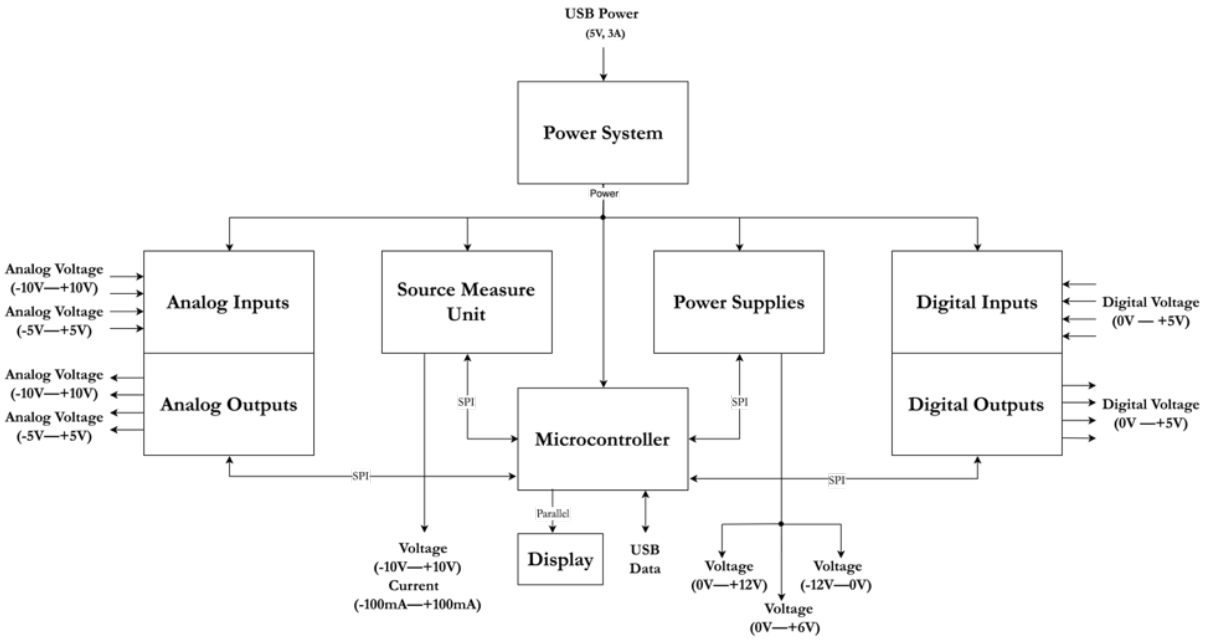


Figure 3.2. Full System Subsystem Diagram

Table 3.2. DC Power Supplies Description

Module	DC Power Supplies
Inputs	Power Supply
Outputs	Analog Voltages (0V-6V, 0V-12V, -12V-0V)
Functionality	Provide adjustable voltage supplies with configurable current drive

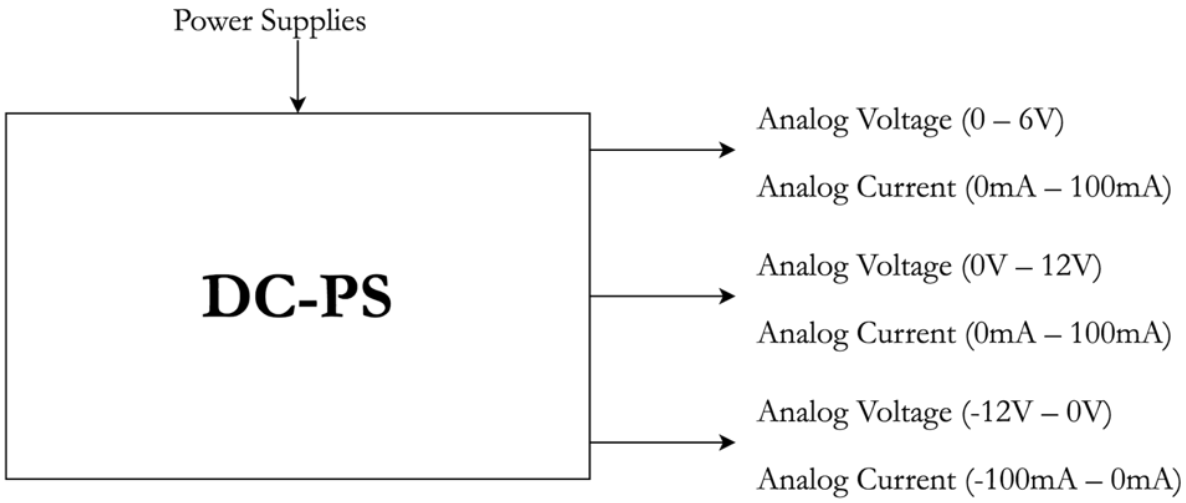


Figure 3.3. DC Power Supplies Black Box Diagram

Table 3.3. Source Measure Unit Description

Module	Source Measure Unit
Inputs	Analog Voltage/Current, Power Supply
Outputs	Analog Voltage/Current
Functionality	Force voltage measure current Force current measure voltage

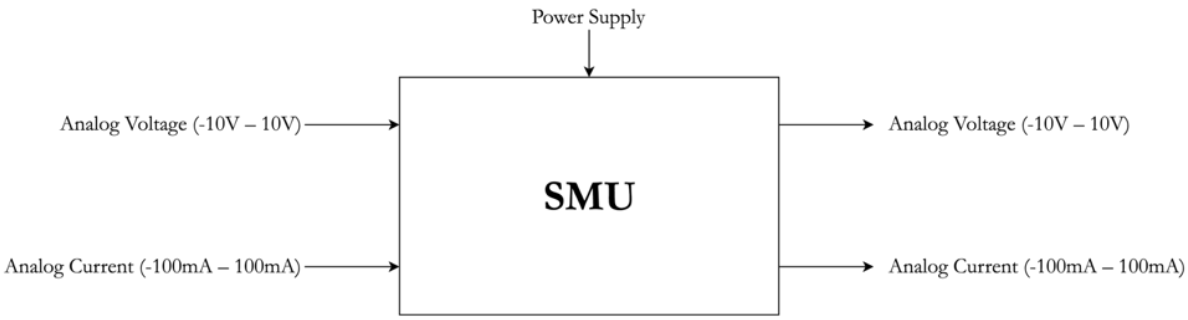


Figure 3.4. Source Measure Unit Black Box Diagram

Table 3.4. Analog Input/Output Description

Module	Analog IO
Inputs	Analog Voltage, Power Supply
Outputs	Analog Voltage
Functionality	Measure analog voltages values in the ranges of ±5V and ±10V. Output analog voltages values (±5V, ±10V).

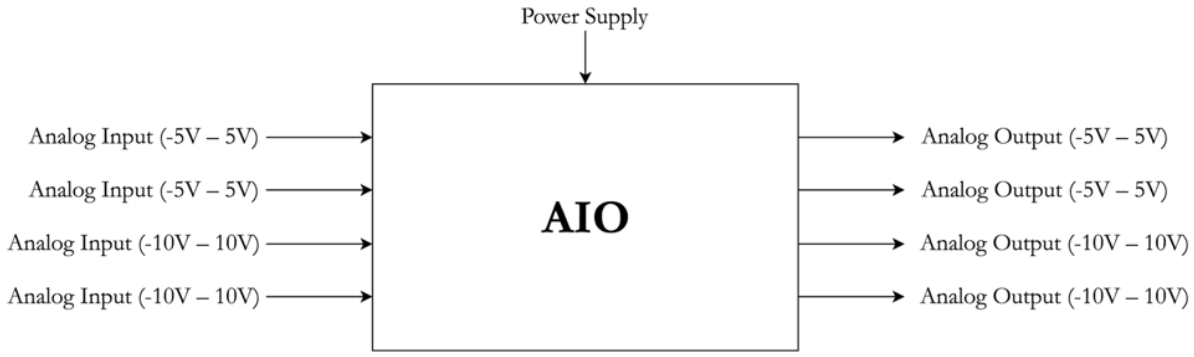


Figure 3.5. Analog Input/Output Black Box Diagram

Table 3.5. Digital Input/Output Description

Module	Digital IO
Inputs	Analog Voltage, Power Supply
Outputs	Analog Voltage
Functionality	Measure digital voltages (0-5V). Output configurable logic high/lows (0-5V).

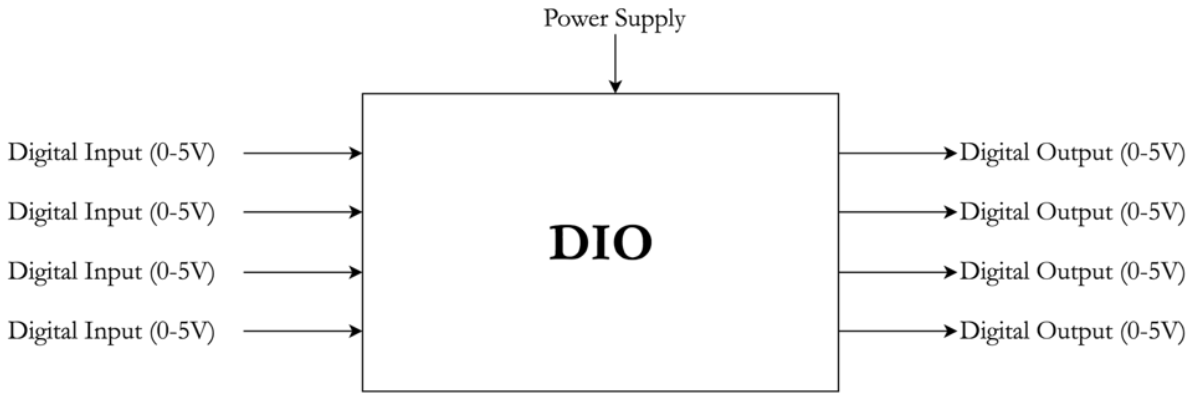


Figure 3.6. Digital Input/Output Black Box Diagram

Table 3.6. Microcontroller Description

Module	Microcontroller
Inputs	SPI, UART, Power Supply
Outputs	SPI, UART
Functionality	Set output levels Read measurements V/I compliance logic Read and write to data file over USB-C Drive visual displays

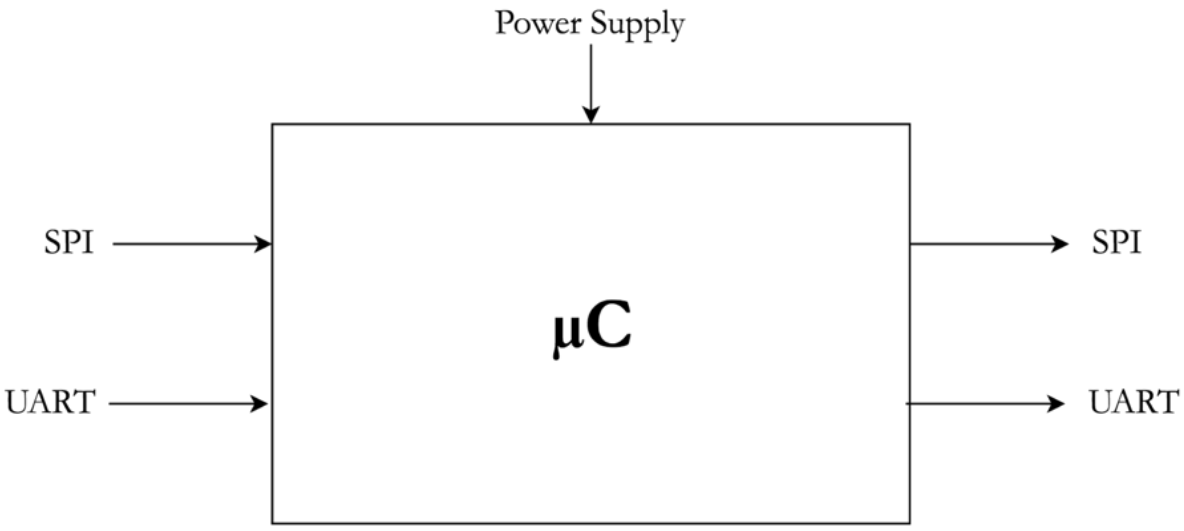


Figure 3.7. Microcontroller Black Box Diagram

4 Progress

4.1 Project Timeline

Each Gantt Chart corresponds a different quarter during the academic years of 2019 to 2020.

Figure 4.1 shows the Fall 2019 Quarter Gantt chart. The chart starts on September 1st, 2019, and counts the days passed since then. Each major event is given an estimated start and end date, which the graph plots. The Specifications and Literature Search are given the most time to complete. The specifications are crucial to get correct, if they are impossible to achieve or not desirable to potential customers the project would be set back significantly. The Literature Search spans the entire quarter as it pertains to every aspect of the project. Sources include design documents, market research, competition analysis, and application notes.

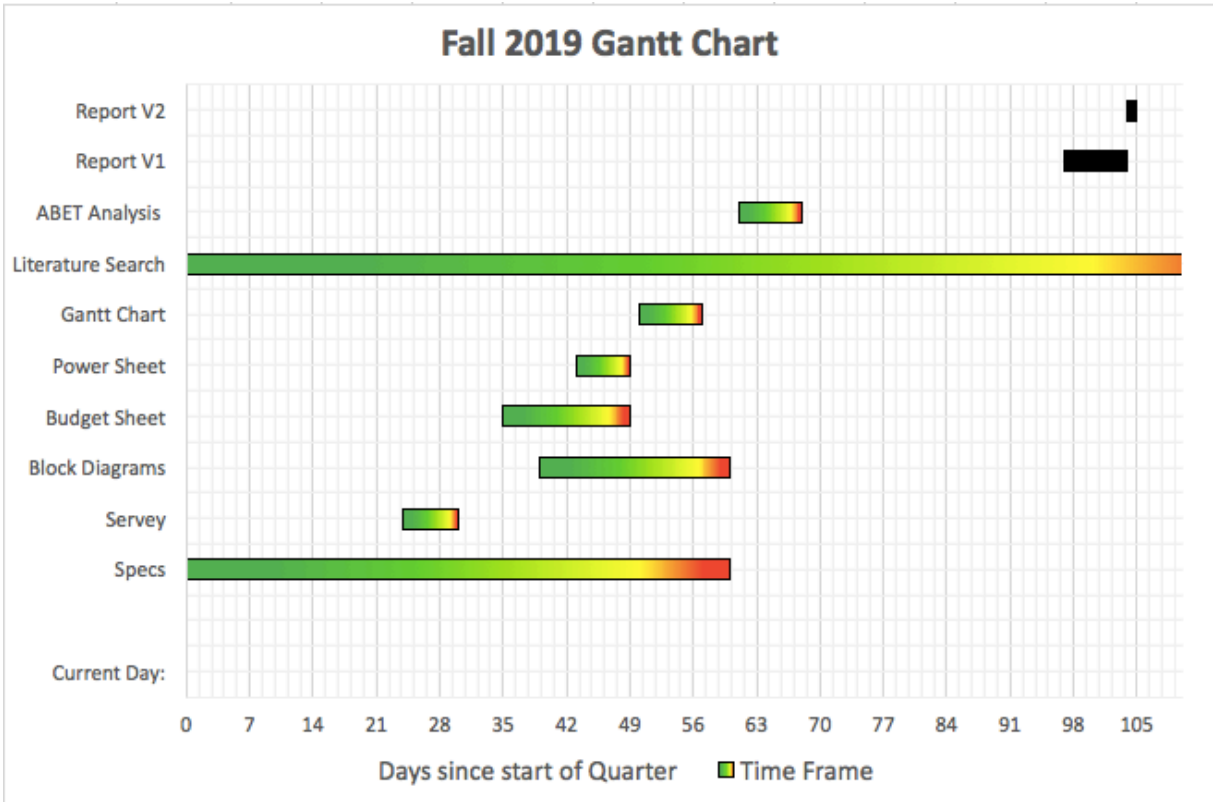


Figure 4.1. Fall Quarter Gantt Chart

Figure 4.2 shows the Winter 2020 Quarter Gantt chart. This chart is primarily focused on subsystem design and layout. The SMU design is by far the most complicated, so it is allocated the most time. The AIO/DIO layout was simplified as they share the same board. This reduces the amount of µC/power supply connections. The µC code involved setting up communcations with the various DACs/ADCs. The project uses 6 different DACs/ADCs chips, meaning this was a lengthy process. The Power Board task is not completed during the Winter Quarter, and is pushed back to Spring Quarter. However, due to time constraints, the author ops to buy a pre-made switch-mode power supply board.

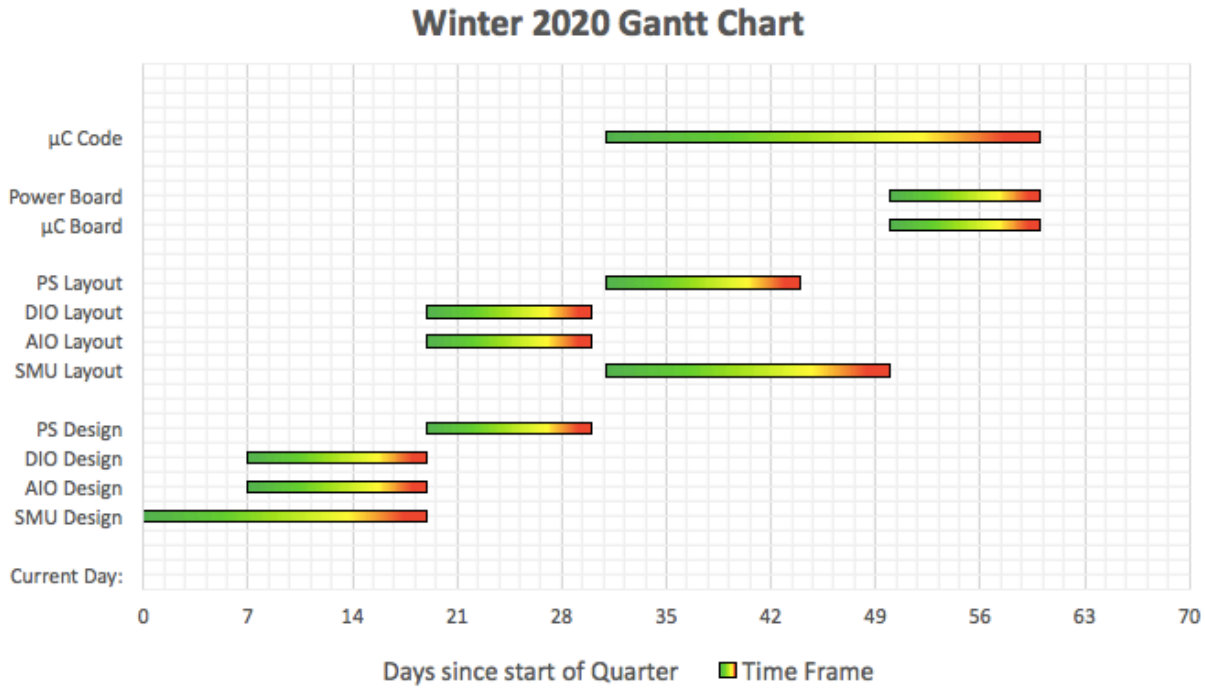


Figure 4.2. Winter Quarter Gantt Chart

Figure 4.2 shows the Spring 2020 Quarter Gantt chart. The quarter is focused on testing, integration, and final report writing. Design and Testing report sections are written as each subsystem completes verification. The µC board acts as a motherboard for the MSP432P401R Launchpad. The Launchpad slots in and has relevant pins mapped to various connectors. The Automation task is the final endeavor; it entails the synchronization of all the subsystems to provide with an automated test/measurement suite.

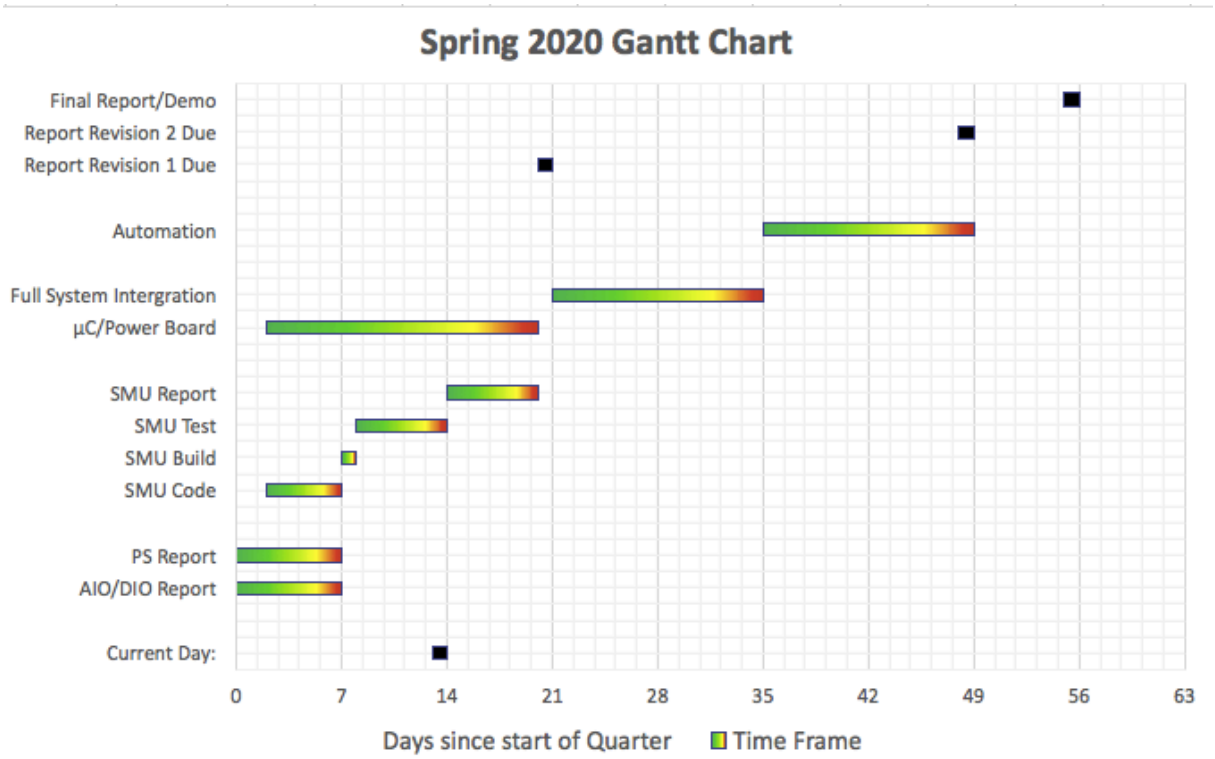


Figure 4.3. Spring Quarter Gantt Chart

4.2 Project Cost

To provide an affordable price to students, the target project price is roughly $200. Figure 4.4 shows the cost breakdown by subsystem. All component costs are calculated assuming a 100 unit purchase quantity. The SMU subsystem was the most expensive. It costs about as much as the power supply and AIO/DIO combined. The bulk of the SMU cost came from the OPA633 ($15.06), INA105 ($9.38), and 4 relays ($2.33 each). These three part types account for more than a third of the total board cost.

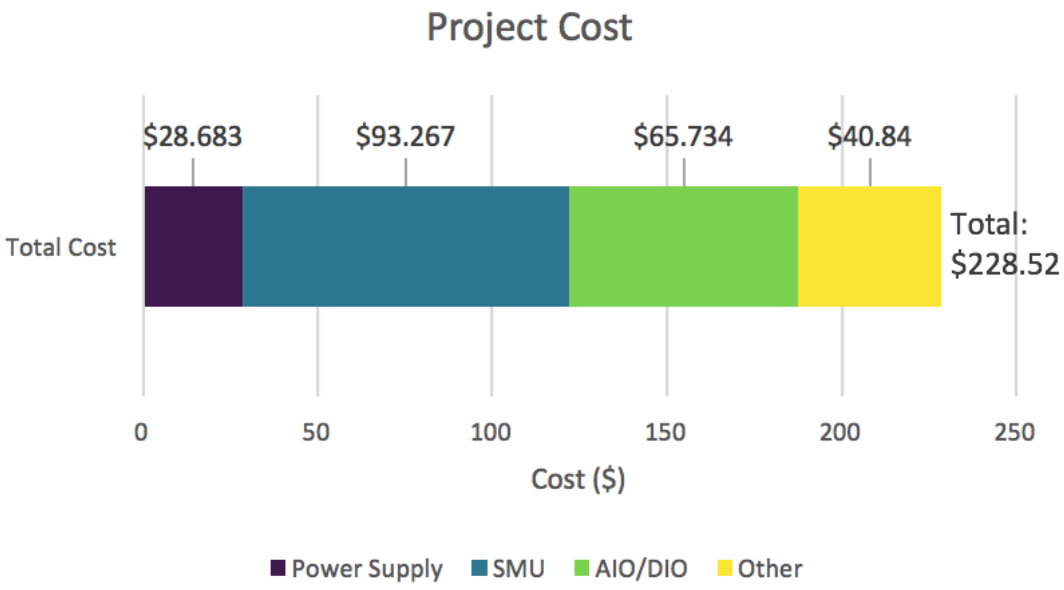


Figure 4.4. Total Project Costs, Including Board Fab and Shipping

Table 4.1. Power Supply BOM

Designator		Package	Quantity	Designation	Price	Extended Price
GND,V-,V+		Banana_Jack	3	Conn_01x01	0.65	1.95
J6,J4		Molex_Micro	2	Conn_01x05	0.77	1.54
C12,C8		CP_Radial_D	2	4.7u	0.2	0.4
C11,C10,C9,C7,C6,C5,C1		C_0805_201	7	0.1u	0.101	0.707
U5	https://www.mouser.com/Prod	TO-220-3_Ve	1	TIP32BG	0.54	0.54
U3,U1	https://www.mouser.com/Prod	TO-220-3_Ve	2	BD239C	0.43	0.86
R15,R16,R14,R13,R12,R11,R10	https://www.mouser.com/Prod	R_0805_201	7	10k	0.059	0.413
U9	https://www.mouser.com/Prod	SOIC-14_3.9x	1	OPA4196	2.89	2.89
U10	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	REF5050AD	2.91	2.91
U8		SOIC-14_3.9x	1	LM339	0.39	0.39
U7		SSOP-14_5.3	1	BU2507FV	4.1	4.1
U6,U4,U2		SOT-23-5_Ha	3	INA198	2.6	7.8
R17		R_0805_201	1	1	0.394	0.394
R9,R8,R7		R_0805_201	3	100m	0.56	1.68
R6,R4,R2		R_0805_201	3	1k	0.131	0.393
R5,R3,R1		R_0805_201	3	2k	0.218	0.654
J3,J2,J1		PinHeader_1	3	Conn_01x02	0.097	0.291
D3,D2,D1		D_0805_201	3	D	0.12	0.36
C4,C3,C2		C_0805_201	3	1u	0.137	0.411
					Subsystem Total	28.683

Table 4.2. SMU BOM

Designator		Package	Quantity	Designation	Price	Extended Price
+5V,-15V,+15V	https://www.mouser.com/Prod	PinHeader_1	3	Screw_Terminal_01x03	0.95	2.85
U11	https://www.mouser.com/Prod	SOT-23-5	1	SN74LVC1G04	0.26	0.26
C35,C19,C18		CP_Radial_D	3	4.7u	0.2	0.6
J2,J5		Molex_Micro	2	Conn_01x06	0.3	0.6
C34,C33,C4,C32,C17,C12,C10,C9,C7,C2	https://www.mouser.com/Prod	C_0603_160	10	0.1u	0.129	1.29
R1	https://www.mouser.com/Prod	R_0603_160	1	150	0.16	0.16
R33,R36,R35,R34,R32,R31,R29,R28,R26,R24,R23,R19,R16,R5,R3,R9	https://www.mouser.com/Prod	R_0603_160	16	10k	0.125	2
Q5,Q8,Q7,Q6	https://www.mouser.com/Prod	TO-92_Inline	4	2N3904	0.284	1.136
U10	https://www.mouser.com/Prod	8VSSOP_4.9x	1	ADC122S051	3.66	3.66
U9	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	REF5050AD	2.91	2.91
U8	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	REF5010AD	2.91	2.91
U7	https://www.mouser.com/Prod	SOIC-14_3.9x	1	OPA4141	4.43	4.43
U6	https://www.mouser.com/Prod	TSSOP-16_4.	1	DAC7565	9.52	9.52
U5	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	LT1126	8.96	8.96
U4	https://www.mouser.com/Prod	SOIC-14_3.9x	1	OPA4197	3.15	3.15
U3	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	INA143	2.72	2.72
U2		DIP-8_W7.62	1	OPA633	15.06	15.06
U1		DIP-8_W7.62	1	INA105	9.38	9.38
R30,R20,R18	https://www.mouser.com/Prod	R_0603_160	3	49.9k	0.026	0.078
R27,R25	https://www.mouser.com/Prod	R_0603_160	6	20k	0.103	0.618
R22,R21	https://www.mouser.com/Prod	R_0603_160	2	1	0.58	1.16
R17	https://www.mouser.com/Prod	R_0603_160	1	60.4k	0.16	0.16
R15,R8	https://www.mouser.com/Prod	R_0603_160	2	1k	0.026	0.052
R14,R7,R13,R12,R11,R10	https://www.mouser.com/Prod	R_0603_160	2	24.9k	0.018	0.036
R6,R4	https://www.mouser.com/Prod	R_0603_160	2	10	0.026	0.052
R2	https://www.mouser.com/Prod	R_1206_321	1	1	0.15	0.15
Q4,Q2	https://www.mouser.com/Prod	SO-8_3.9x4.9	2	DMT6010LSS-13	1.23	2.46
Q3,Q1	https://www.mouser.com/Prod	SO-8_3.9x4.9	2	Si4401FDY-T1-GE3	0.89	1.78
K4,K3,K2,K1	https://www.mouser.com/Prod	Relay_Stande	4	HE721C0500	2.33	9.32
J1		PinHeader_1	1	Conn_01x02	-	
D6,D5,D4,D3,D2,D1	https://www.mouser.com/Prod	D_DO-35_SO	6	1N4148	0.06	0.36
C31,C30,C29,C28,C26,C25,C20,C16,C6,C5,C3,C1	https://www.mouser.com/Prod	C_0603_160	12	1u	0.215	2.58
C27,C24,C23,C22,C21		C_1206_321	5	4.7u	0.487	2.435
C15	https://www.mouser.com/Prod	C_0603_160	1	150n	0.27	0.27
C14,C11		C_0603_160	2	DNP	-	
C13,C8	https://www.mouser.com/Prod	C_0603_160	2	330p	0.08	0.16
					Subsystem Total	93.267

Table 4.3. AIO/DIO BOM

Designator		Package	Quantity	Designation	Price	Extended Price
J18,J17,J16,J15,J14,J13,J12,J11,J10,J9,J8,J7,J6,J5,J4,J3		PinHeader_1	16	Conn_01x01		
C42,C41,C40,C39,C38,C37		C_1206_321	6	2.2u	0.487	2.922
R31,R35,R34,R32,R29,R28,R26,R25		R_0805_201	8	50k	0.046	0.368
R9,R18,R15,R12	https://www.mouser.com/Prod	R_0805_201	4	10k	0.059	0.236
U2		TSSOP-16_4.	1	ADS1220	8.51	8.51
U14	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	REF5050AD	2.91	2.91
U13	https://www.mouser.com/Prod	SOIC-8_3.9x4	1	REF5010AD	2.91	2.91
R38,R37		R_0805_201	2	1	0.394	0.788
C36,C35,C34,C33,C32,C31		C_0805_201	6	1u	0.15	0.9
J1,J2		Molex_Micro	2	Conn_01x10	-	
C30,C29,C27,C25,C23,C21,C16,C15,C14,C13,C12,C11,C10,C9,C8,C7,C6,C5,C4,C3,C2,C1	https://www.mouser.com/Prod	C_0805_201	22	0.1u	0.101	2.222
U12	https://www.mouser.com/Prod	SOIC-14_3.9x	1	OPA4196	2.89	2.89
R36,R33,R30,R27,R20,R17,R14,R11		R_0805_201	8	1k	0.288	2.304
C28,C26,C24,C22		C_0805_201	4	6.8u	0.234	0.936
U7,U6,U5,U4	https://www.mouser.com/Prod	SOIC-8_3.9x4	4	INA145	3.5	14
U11,U9		VSSOP-10_3x	2	DAC084S085	2.41	4.82
U10		SOIC-14_3.9x	1	TLV3544	2.69	2.69
U8		SOIC-14_3.9x	1	LM339	0.39	0.39
U3		TSSOP-16_4.	1	MAX5134AGUE+	9.53	9.53
U1		SOT-23-6_Ha	1	REF3425	3	3
R24,R23,R22,R21		R_0805_201	4	20	0.072	0.288
R19,R16,R13,R10		R_0805_201	4	10	0.072	0.288
R8,R7		R_0805_201	2	13.3k	0.36	0.72
R6,R5		R_0805_201	2	40.2k	0.36	0.72
R4,R3,R2,R1		R_0805_201	4	20k	0.04	0.16
D8,D7,D6,D5,D4,D3,D2,D1	https://www.mouser.com/Prod	D_0805_201	8	D	0.12	0.96
C20,C19,C18,C17		C_0805_201	4	10n	0.068	0.272
					Subsystem Total	65.734

Table 4.4. Misc. BOM

Designator		Package	Quantity	Designation	Price	Extended Price
-	IEEE Student Branch	-	1	MSP432 Lanchpad	5	5
+5V,-15V,+15V	https://www.mouser.com/Pro	PinHeader_1	3	Screw_Terminal_01x03	0.95	2.85
-	https://www.amazon.com/gp/	-	1	B0752TRXDC Buck Bost Power	12.99	12.99
Board Fab Cost (Get 5 boards for $25 (shipping included)), 4 boardsordered total	JLCPCB	-	4	-	5	20
					Subsystem Total	40.84

5 Design

> If analog people can do stupid things, can stupid people do analog things?
>
> *Bob Pease*

To a good approximation, analog system design has a 0% success rate. Fortunately, as time invested and coffee consumed trends toward infinity, the success rate tends to rise, albeit slowly. Expediting this process is convenient to me as I am most regrettably mortal (thus far). Over the course of the past year, various white papers, application notes, and stack exchange questions are collected, arranged, and sanitized to offer baseline designs and convenient topologies put toward use. What's shown below is what remained of the research after torched by the harsh flames of reality. The smoldering ashes I've christened as my senior project are all that's left.

5.1 Power Supply Design

Informally, the power supply requirements are straightforward. The crux of the design is finding a suitable configuration that can vary the voltage at the lower range. A brief look at various linear regulators suggests that this a 'weak point' in their use, as a typical LDO output has a lower limit of roughly 1 – 2V. A look under the hood shows us why this is the case.

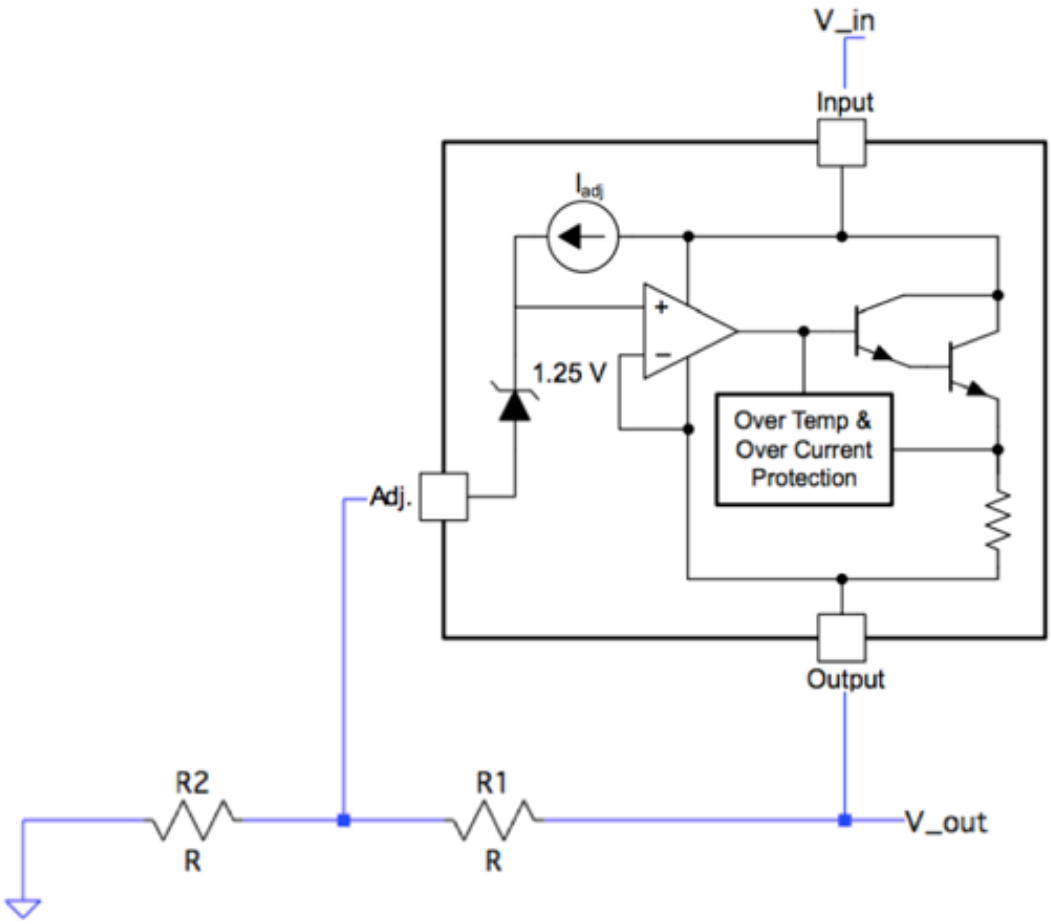


Figure 5.1. Functional Block Diagram of the LM317 in Adjustable Voltage Regulator Configuration [16]

Figure 5.1 shows the simplified LM317 positive voltage regulator internal structure as well as the two external voltage setting resistors R_1 and R_2.

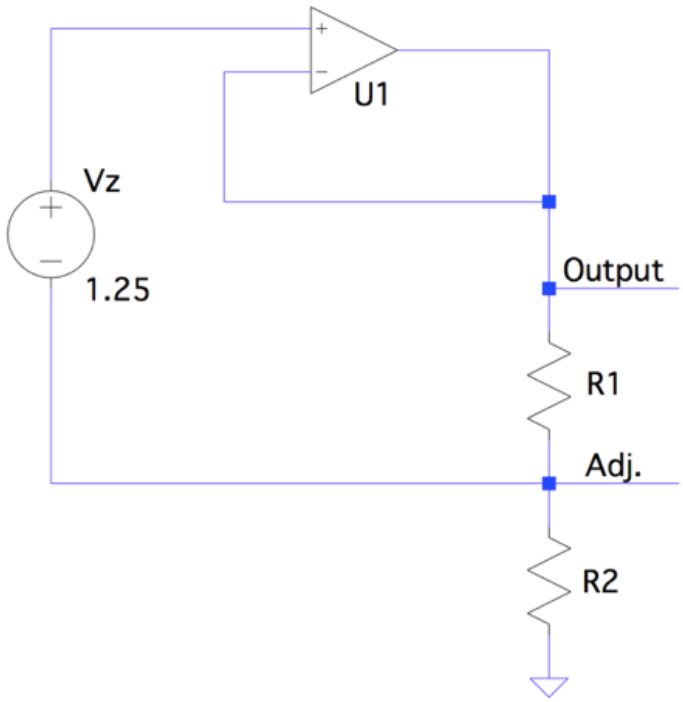


Figure 5.2. Simplified Block Diagram of the LM317

Figure 5.2 shows the simplified LM317 voltage control system. The op-amp U_1 is a voltage follower; the voltage at the inverting and non-inverting terminals is approximately the same. This forces a constant 1.25V across R_1. As the op-amp terminals ideally draw no current, all the current through R_1 passes through R_2. Equation 1 shows the output voltage as a function of the reference voltage V_z and resistor ratio.

$$V_{out} = V_z * (1 + \frac{R_2}{R_1}) \tag{1}$$

Most notably shown above is that the output voltage can only reach a minimum of V_z. For the LM317, V_z is 1.25V, and is a reference voltage that manifested either through a Zener diode or a bandgap reference. This voltage is designed to be sturdy under temperature and not vary under normal operating conditions. Another takeaway is the ratio of R_2 to R_1 sets the ratio of output voltage to reference voltage. If R_1/R_2 is adjustable, the output voltage varies in a predictable fashion.

This behavior is close to what is necessary to construct the adjustable power supply. If instead the resistor ratio is constant and the reference voltage varies, the output voltage should change in a linear manner. Furthermore, if the reference voltage is 0V, the output voltage is 0V, regardless of the resistor ratio. Using this method is how the power supply design came to fruition. 5.3 shows the power supply topology.

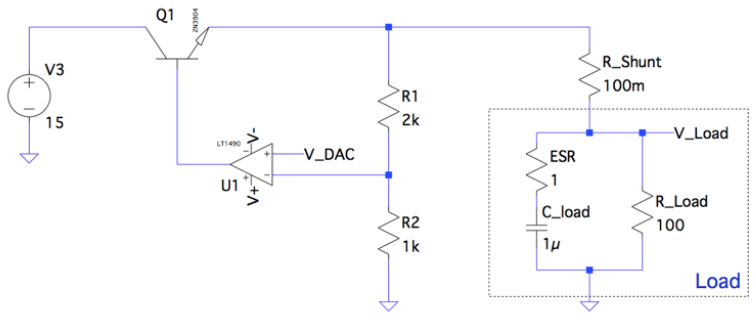


Figure 5.3. Positive Power Supply Design with Characterized Load

The voltage V_{DAC} is referenced to ground, meaning that whatever the DAC voltage appears across R_2 instead of R_1. Equation 2 shows the output voltage as a function of V_{DAC}.

$$V_{out} = V_z * (1 + \frac{R_2}{R_1}) \tag{2}$$

As typical DACs typically output 0 – 5V, and the power supply output is 0 – 12V, a 2:1 resistor ratio sets the overall gain to 3V/V. A DAC voltage of 4V results in an output voltage of 12V. Figure 5.4 shows the DC transfer characteristic.

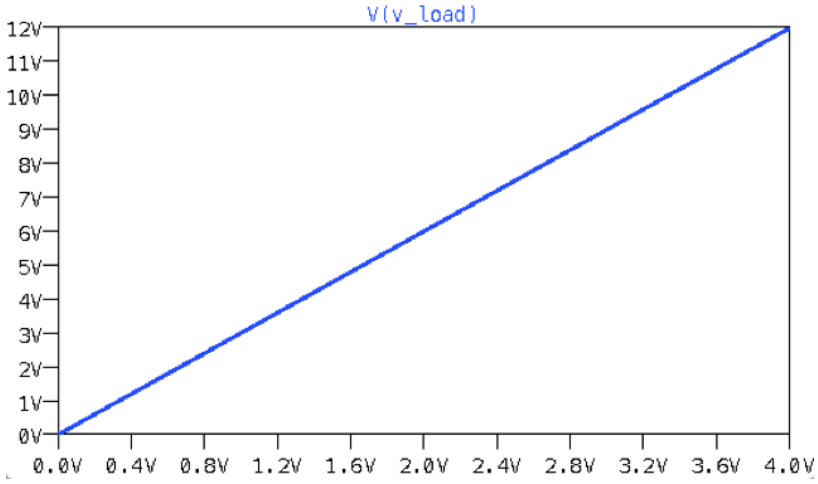
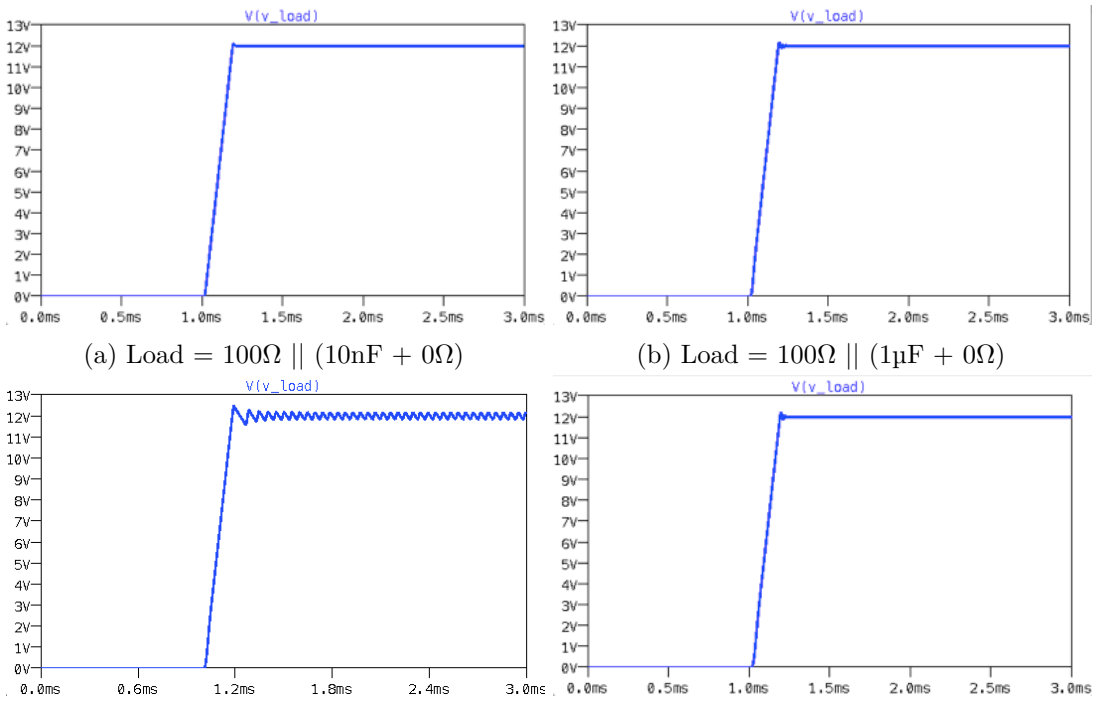


Figure 5.4. Output Voltage VS DAC Voltage

One concern of the design shown in figure 5.3 is stability for large capacitive loads. As this module is used as a power supply, the user may attach large value bypass capacitors to the output. The overall system stability is tested using a DAC output 4V step at t = 1ms for a variety of load conditions.



(a) Load = 100Ω || (10nF + 0Ω)

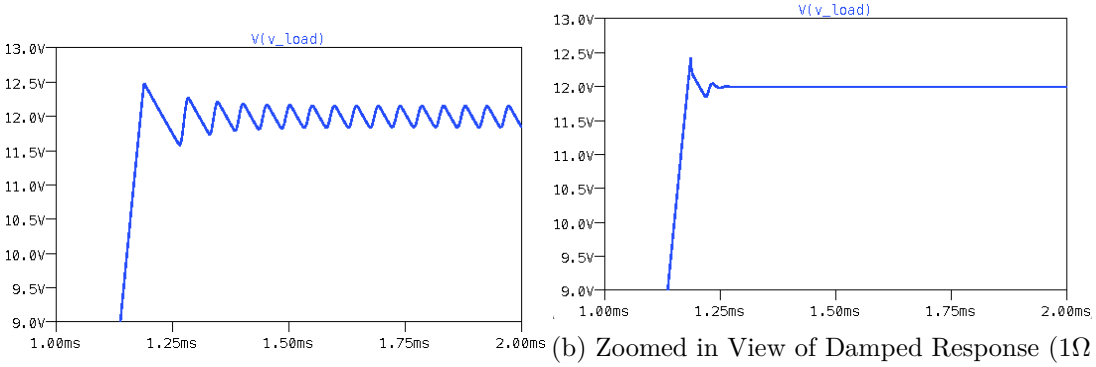
(b) Load = 100Ω || (1µF + 0Ω)

(c) Load = 100Ω || (2µF + 0Ω)

(d) Load = 100Ω || (2µF + 1Ω)

Figure 5.5. Output Transients for Selected Load Characterizations

Figure 5.5 show the effect of different load capacitors on the power supply stability. Figures 5.5a and 5.5b show how small capacitance values and no capacitor equivalent series resistance (ESR) results in a stable output. However, once the load capacitance passes a certain point, the output begins to oscillate. Figure 5.5c shows the output oscillation for a load of 100Ω in parallel with a 2µF capacitor with 0 ESR. Figure 5.6a shows the zoomed in oscillation. These oscillations vanish when the capacitor has roughly a few ohms of ESR. Figures 5.5d and 5.6b show the now damped response.



(a) Zoomed in View of Oscillations (No ESR)

(b) Zoomed in View of Damped Response (1Ω ESR Present)

Figure 5.6. Result of an ESR of 1Ω

Potential instability is a common problem when working with linear regulators 15. Based on figure 5.6, the power supply topology presented is stable.

5.1.1 Component Selection

The DAC chosen is the BU2507FV. This particular DAC has 6 outputs, fulfilling the demand of the 3 voltage control channels and 3 current limit channels. The BU2507FV is 10-bit, which allows a 14.65mV resolution in the power supply output.

The REF5050 is a 0.01% 5V reference capable of sourcing 10mA of current [21]. Because the output current is greater than the BU2507FV maximum current demand, the REF5050 can power the DAC. This saves the board from needing a separate 5V power and 5V reference voltage.

The series pass transistors used are chosen based on of power dissipation, maximum DC collector current, and maximum collector-emitter voltage. BJTs in TO-220-3 packages are desirable for the ability for the addition of a heat sink. The TIP32BG and BD239C are chosen. Both devices have power dissipation (at $T_{amb} \leq 25°C$) of 2W, maximum DC collector current of at least 2 amps, and maximum collector-emitter voltages of at least 80V 22, 23.

5.2 Source Measure Unit Design

The Source Measure Unit (SMU, or also affectionately known to me as the Hell Circuit) proved to be the most difficult module to design. The base functionally of force current, measure voltage and force voltage, measure current was achievable with some research and luck. At low voltages and currents there is no need for range switching, removing a potentially complicated block of a normal SMU. The currents and voltages measured are also in a goldilocks zone; not too small that special considerations are needed for acceptable measurement accuracy and not too large that power dissipation and voltage/current ratings need to be closely examined. The difficult part of designing the SMU was the current and voltage limiting sub-circuits. The project's author for reasons unbeknownst to anyone, decided that in the event of an overvoltage/overcurrent situation, the SMU goes into either constant current or constant voltage mode, rather than turn off. Figure 5.7 shows an example of this behavior.

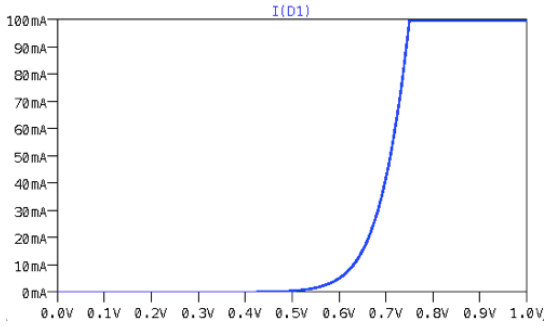


Figure 5.7. Result of Testing a Diode with a Current Limit of 0.1A

Unlike the power supply, the SMU underwent 3 major design revisions over several months. Each revision and its corresponding changes follow.

5.2.1 Revision A

The first attempt at the SMU resulted in a viable circuit in terms of voltage/current output specs. Voltage/current limiting features were not present, and had a 50Ω output impedance in voltage source mode which needed correction. Despite these problems, REV A formed the foundation for subsequent revisions. The SMU REV A design is primarily based on two separate application notes. The first is a 1990 Burr Brown paper concerning implementation and uses of current sources and receivers. The second is a 2000 TI application note on a precision ±10V voltage source. By a stroke of luck, both app notes reference the INA105, a precision unity gain amplifier. Relevant images from both app notes and the corresponding implementation are shown in figures 5.8 and 5.10.

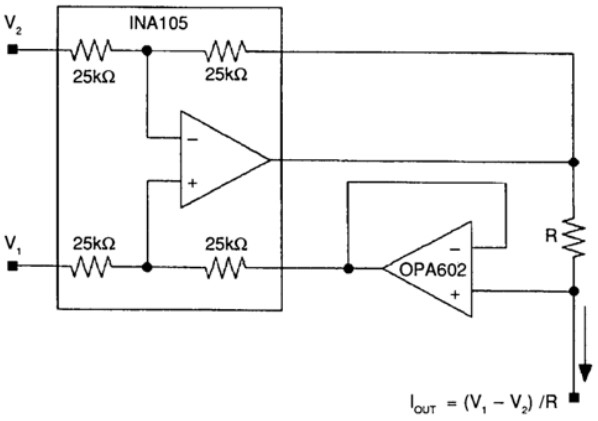


Figure 5.8. Bidirectional Current Source/Sink using the INA105 [6]

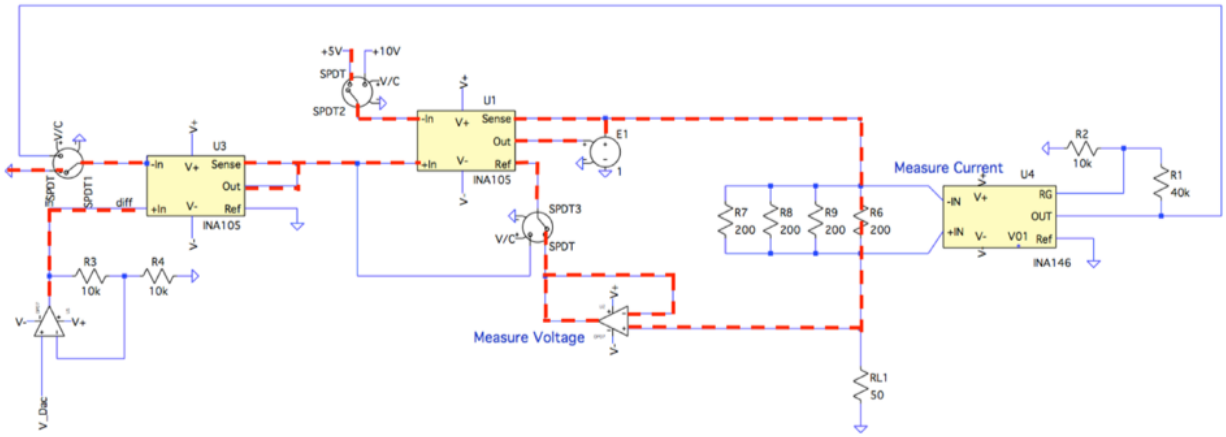


Figure 5.9. Current Source/Sink Implemented (Red Highlight Shows Active Circuitry)

According to the application note, the differential voltage as well as the resistor R set the current delivered to the load [6]. When R is 50Ω, a ±5V differential voltage results in a ±100mA current. In figure 5.9, the input to U_1, is 0-10V. When using a 5V reference voltage, a ±5V differential voltage occurs. With the equivalent R_6 through R_9 parallel resistance of 50Ω, the target current is achieved.

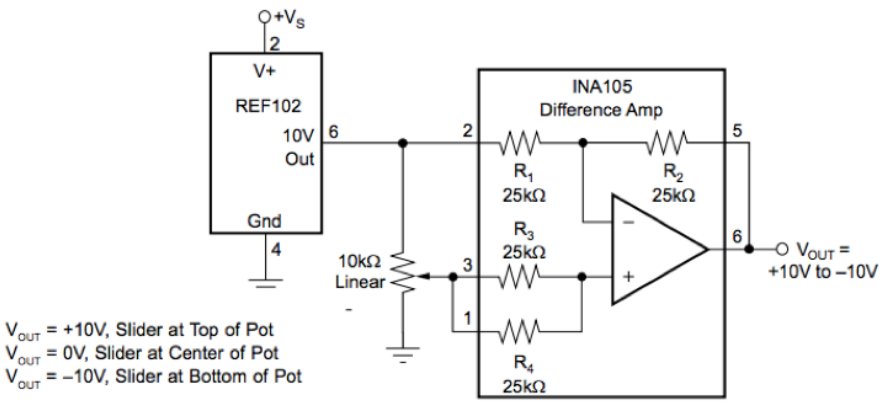


Figure 5.10. Precision ±10V Voltage Source using the INA105 [7]

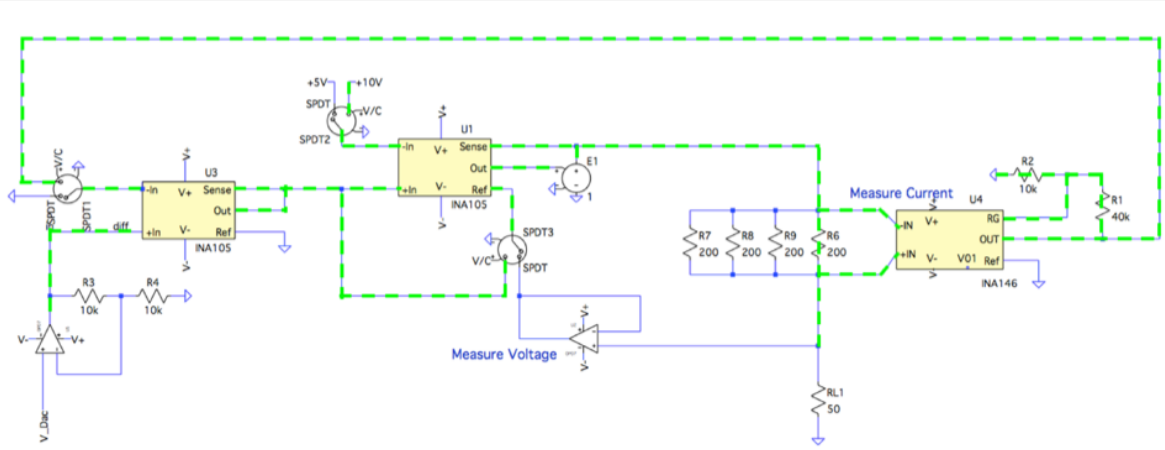


Figure 5.11. Precision ±10V Voltage Source Implemented (Green Highlights Active Circuitry)

In figure 5.11, the input voltage into U_1 varies between 0 – 10V. The non-inverting input to INA105 U_1 is a 10V reference, as per the app note. With this configuration the output voltage of U1 is -10 to 10V. However, the voltage source has an output impedance of 50Ω minimum in this configuration, due to the current setting resistor in the output path. As the 50Ω resistor has a difference amplifier across it for current measurement, the shunt voltage feeds back to the start of the loop to compensates for the drop, drastically reducing the output impedance. Figure 5.12 shows the simulated output impedance with and without the feedback. A relay controls this feedback path, active only when in voltage output mode.

Relays are chosen over solid state switches for a few reasons. The first is the voltage range of the relay exceeds any voltage present in the SMU. Solid state switches need power rails beyond or equal to that of the signals passing though. Some switches are one way, but bidirectional capabilities are needed for this topology. Solid state switches also tend to have a larger on resistance, which causes errors in the circuit voltage transfer function. Finally, relays are selected simply because the author has never used them before and wants to gain familiarity with them.

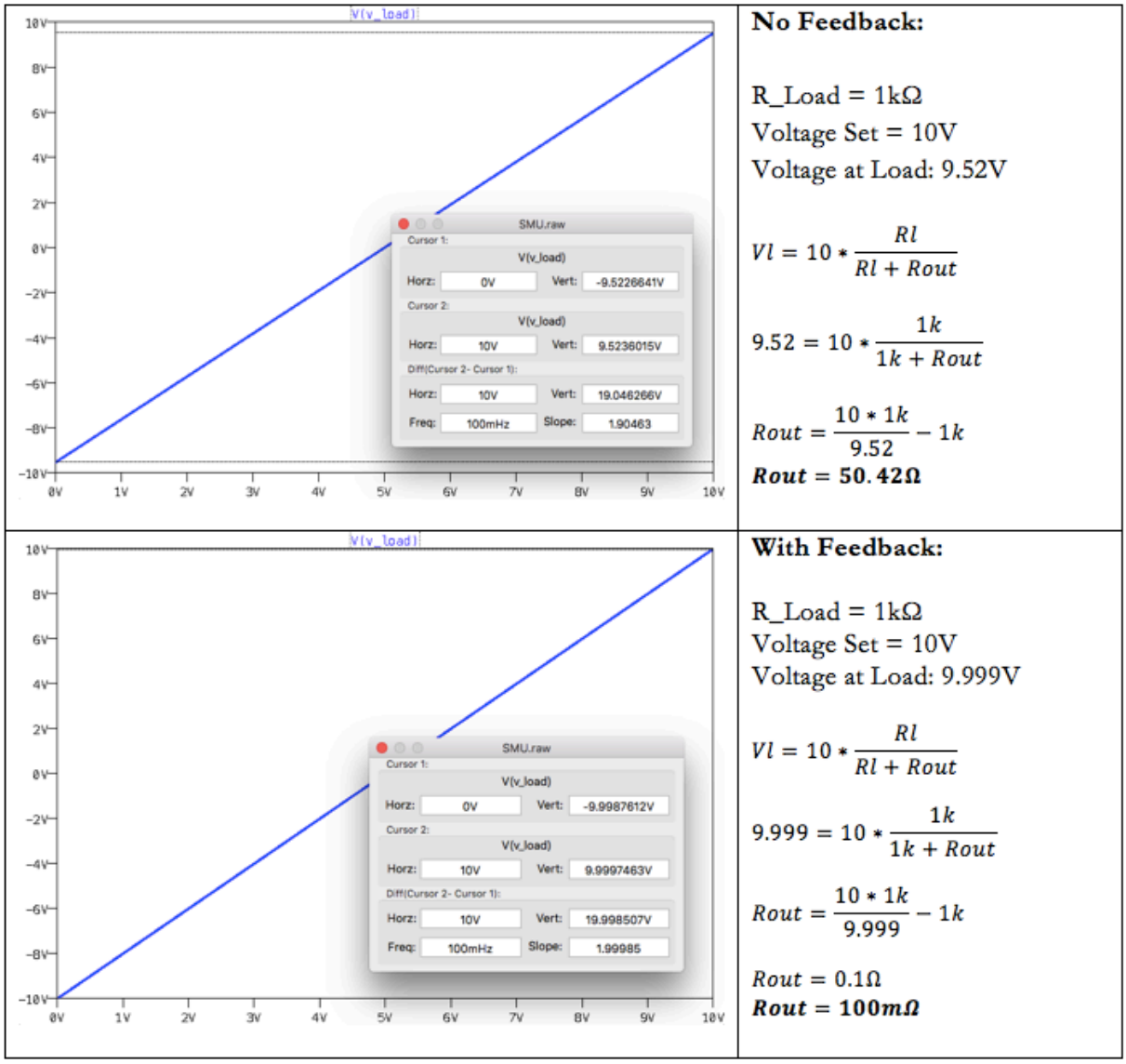


Figure 5.12. Reduction in Output Impedance of the SMU

5.2.2 Revision B

With the SMU core functionality working, additional functionality is added to the next design iteration. Overvoltage and overcurrent protections are critical features of an SMU. These limiters are implemented entirely in hardware. A hardware solution reacts quickly and autonomously. There is no 'chain of command' needed. Unlike the power supply overcurrent/voltage protection, which simply turns off the output, the SMU output should settle at the limited value. This process likely need multiple adjustments, which hogs the microcontroller and is difficult to stabilize. Instead of needing to repeatably sample the load voltage/current to make corrections, a control system consisting of op-amps and MOSFETs make adjustments. Depending on the situation, the MOSFETs operate in off, linear, or saturation. This hardware control allows for a 'set it and forget it' attitude for the µC.

5.2.2.1 Voltage Limiting

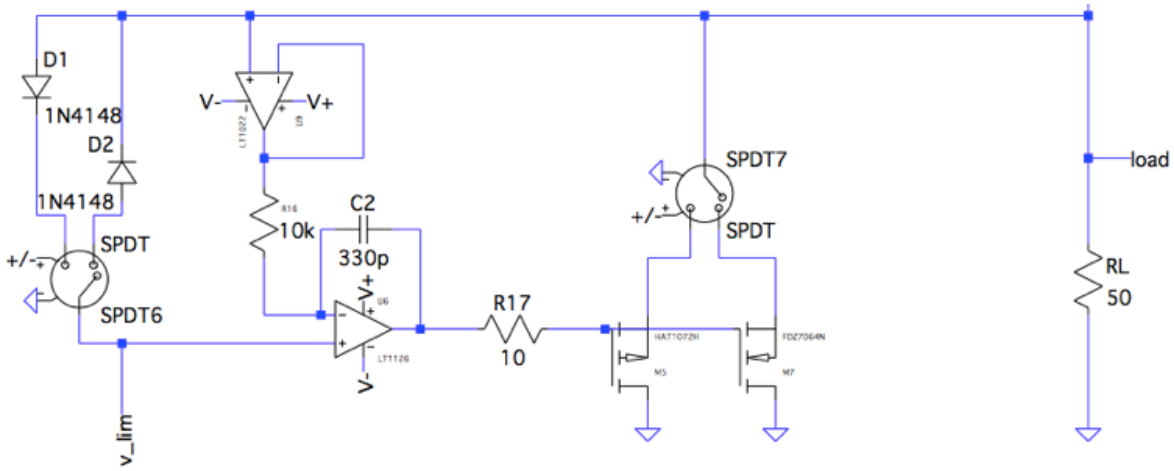


Figure 5.13. SMU Voltage Limiting Circuit

Figure 5.13 shows the control circuitry of the adjustable overvoltage protection. This protection circuit is active when the SMU is in current forcing mode. R_L is the load resistance. M5 and M7 are two FETs in parallel to the load. The concept behind the overvoltage protection is that if the load voltage passes a threshold (V_{lim}), one of the two FETs turns on and takes some of the current that would otherwise flow though the load. The FETs act as voltage controlled resisters in this configuration.

For example, if the output current is set to 10mA, the voltage limit is 5V, and the load resistance is 1kΩ, the FET turns on and siphons 5mA away from the load. The remaining 5mA that pass though the load results in the target 5V maximum. In this instance the FET is acting as a 1kΩ resistor. The FET drain to source resistance varies based on the load resistance and voltage/current set points.

U_6 is an error amplifier that has two main states. In the normal state, when no overvoltage event is happening, U6 saturates at one of the supply rails. This turns either M_5 or M_7 completely off. If an overvoltage event occurs, U6 starts to slew its output. This voltage starts to turn on M_5 or M_7. As the FET turns on, the load voltage starts to drop until it is less than the voltage limit. U_6 amplifies this error and starts to slew its output in the other direction. This causes the FET to raise its resistance, allowing the load voltage to rise again. When the total system is stable, the load voltage converges to the programmed voltage limit. Stability of this system is an unwieldy task. U6 has a large differential gain, and the I_{SD} vs V_{SD} of M_5 (I_{DS} vs V_{DS} of M_7) also exhibits a large gain factor. Without some way of slowing the circuits response, oscillations occur. C_2 and R_{16} turn U_6 into an integrator. U_6 is a decompensated op-amp chosen at the recommendation of Vladimir Prodinov, an electronics professor at Cal Poly. His reasoning behind a decompensated op-amp is that stacking an integrator on top of a regular op-amp (which already acts as an integrator) is redundant. With a decompensated op-amp, fine control of the unity gain frequency is possible.

U_9 is present to prevent the integrator from drawing any current. D_1 and D_2 are clamping diodes that prevent the load voltage from exceeding more than 0.8V more than the limit voltage. The reason for two diodes and two MOSFETS is the bipolar output of the SMU. The load voltage can either be positive or negative. Thus, clamping in both directions is needed. Relays control which diode and FET is active.

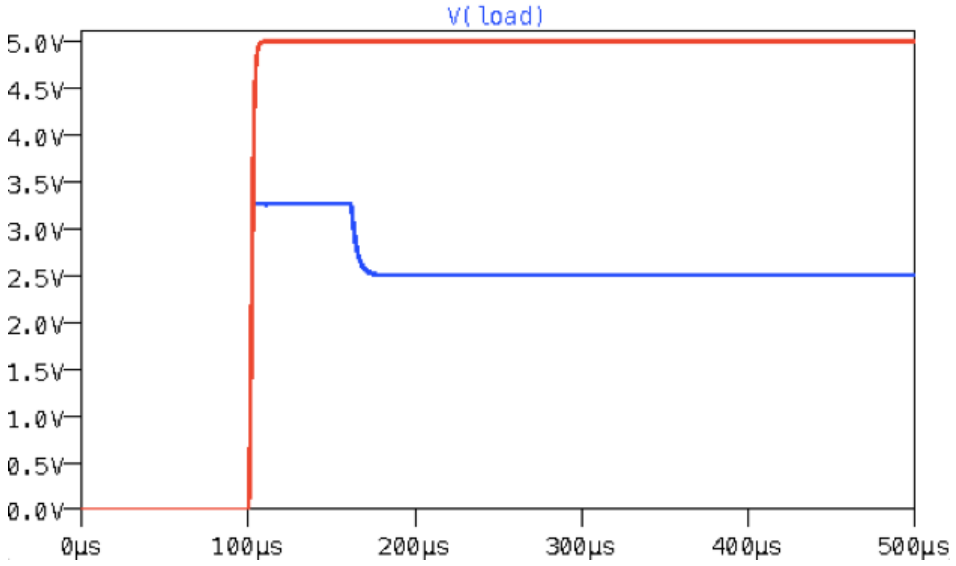


Figure 5.14. SMU Voltage Limiting Transient Simulation (Sourcing Current)

Figure 5.14 shows two waveforms. The red waveform is the load voltage without any voltage limiting, and the blue is with voltage limiting. This simulation is done with a load resistance of 50Ω, current output of 100mA, and voltage limit of 2.5V. The blue waveform shows a plateau-like shape from the diode clamping. After about 70µs, the control system activates and the load voltage decreases. The decrease is damped, exhibiting no oscillations or overshoot.

Figure 5.15 shows a similar scenario, with a load resistance of 50Ω, current output of -50mA, and voltage limit of -0.5V. Again, the blue waveform is load voltage with the limiting circuit, and red is without. The voltage limiting works for both positive and negative set points.

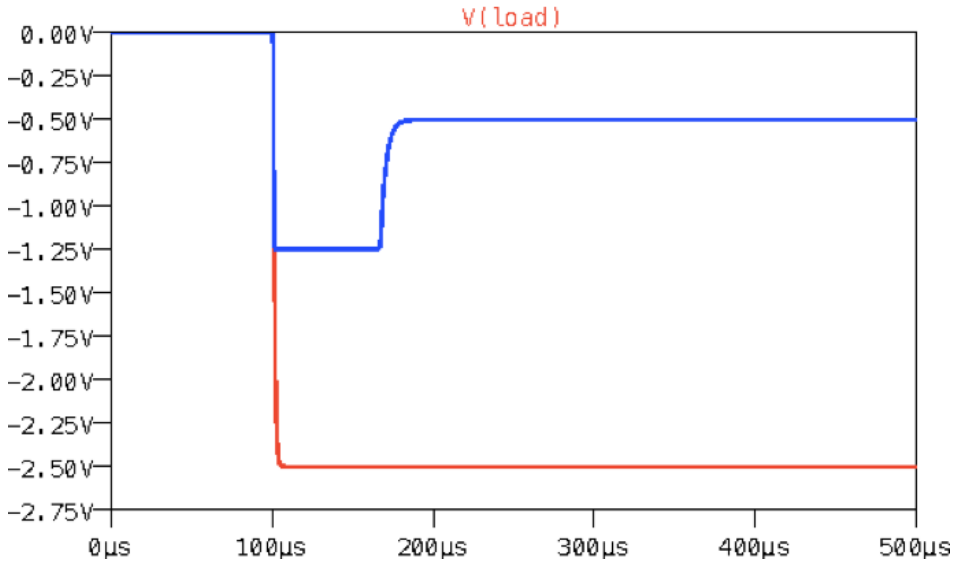


Figure 5.15. SMU Voltage Limiting Transient Simulation (Sinking Current)

5.2.2.2 Current Limiting

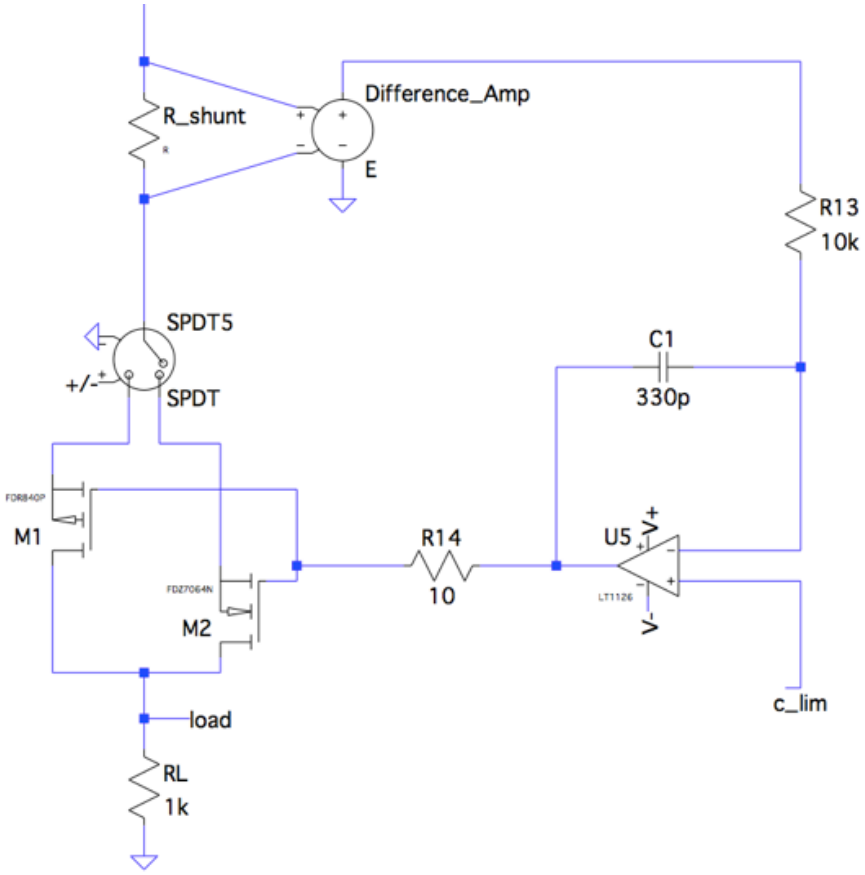


Figure 5.16. SMU Current Limiting Circuit

Figure 5.16 shows the control circuitry of the adjustable overcurrent protection. This protection circuit is active when the SMU is in voltage forcing mode. R_L is the load resistance, the protection circuit is seen in series between the load and normal voltage output. The difference amp (modeled as E) in figure 5.16, measures the voltage across R_{shunt}. This voltage signal carries the information about how much current the voltage supply is sourcing/sinking. M_1 and M_2 are series pass transistors that during normal operation are completely on. When either FET is on, it acts as a short. U_5 is the error amp that saturates at a rail during normal operation. When the measured output current is greater than the current limit threshold (C_{lim}), U_5 starts to slew its voltage. This begins to turn off M_1/M_2, increasing their on resistance. The M_1/M_2 drain to source resistance is seen in series with the load. A larger combination resistance of R_L and M_1/M_2 r_{DS} draws less current when a constant voltage is applied. Like the voltage limiting circuit, when the system is stable the op-amp terminals have equal voltage and converge the output current to that of the current limit.

C_1 and R_{13} stabilize the system. A relay controls which FET is in series with the load. Without the relay the normally disconnected MOSFET parasitic body diode turns on and disrupts the output voltage.

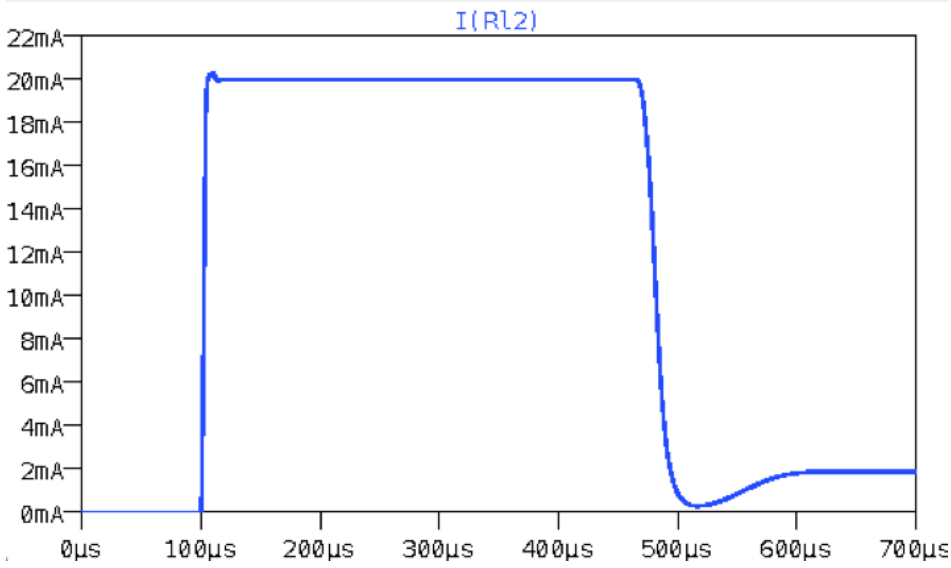


Figure 5.17. SMU Voltage Limiting Circuit (Positive Voltage Output)

Figure 5.17 shows the load current transient waveform with a load of 500Ω, voltage output of 10V, and current limit of 2mA. Initially the load draws 20mA, as expected. A painfully long 400µs later, the current limiting circuit activates. After some minor overshoot (10%) it limits the currents to the specified 2mA. Even though this system is about 10 times slower than the voltage limiting system, it shows potential stability concerns.

Figure 5.18 below shows an even more frightening scenario. With a load of 500Ω, voltage output of -10V, and current limit of -5mA, the output current noticeably oscillates about 3 times before settling. The 25% overshoot is quite the scary sight, as is the 550µs response time. Nevertheless, the show must go on. In the SMU PCB layout unpopulated pads are left in case additional stabilizing components are needed.

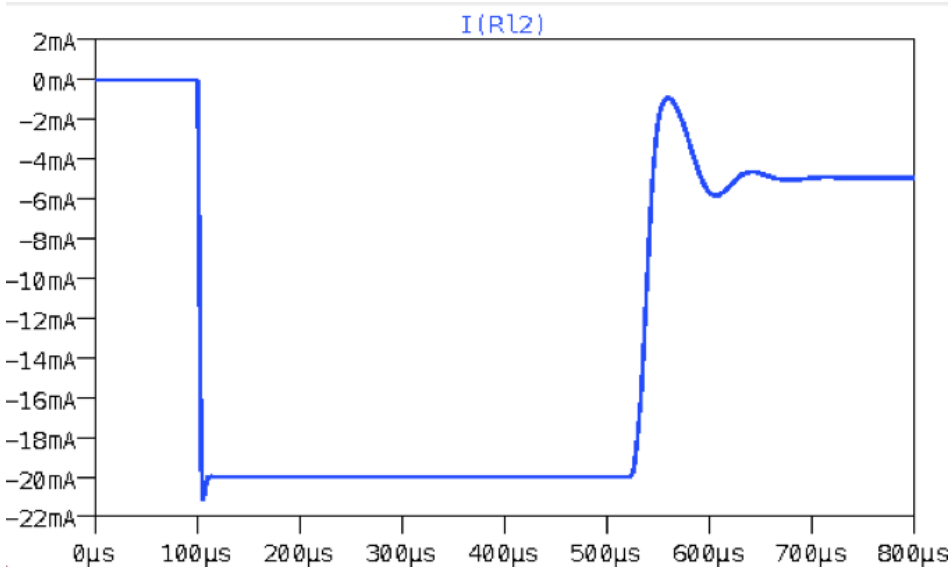


Figure 5.18. SMU Voltage Limiting Circuit (Negative Voltage Output)

5.2.3 Revision C

The (hopefully)[1] final revision of the SMU made a few changes to the output of the voltage source mode. In REV A, there is a 50Ω shunt resistance in series with the load. This resistance sets the current output when in current mode, but is useless in voltage mode. This resistance forms a voltage divider with the load leading to a decrease in the load voltage. Additionally, the 50Ω resistance burns 5W of power when the load draws a current of 100mA. The voltage drop nulling feedback loop discussed in REV A fixes the voltage drop problem, but is complicated and requires an additional relay. A solution for fixing both output impedance and power consumption problems is simply lowering the shunt resistance. A shunt resistance of 1Ω dissipate only 100mW at max current and alters the output voltage roughly 50 times less.

The problem with decreasing the shunt resistance is that it directly impacts the current output transfer function. The current output is given by equation 3.

$$I_{out} = \frac{V_1 - V_2}{R_{shunt}} \tag{3}$$

With the new R_{shunt} of 1Ω and previous differential voltage of ±5V, the current output is now ±5A. The output buffer cannot supply this much current. The differential voltage must decrease to ±0.1V for a proper max output of ±100mA.

To reiterate, when in voltage mode, V_1 varies from 0-10V, V_2 is a constant 10V, which produces a -10V – 10V output. In current mode, V_1 varies from V_{ref} ± 0.1V, V_2 is a constant VRef, which produces a -100mA – 100mA output when Rshunt is 1Ω.

The voltage at V_2 is 10V when the SMU operates in voltage mode. If the differential voltage in current mode is 9.9V – 10.1V, the 10V reference doesn't need adjustment. In REV A, a relay changed V_2 to 5V when in current mode. Revision C removes this relay, and uses fine and coarse control for the current/voltage adjustment. Two DACs have their voltages scaled and summed.

One DAC has its voltage (V_{coarse}) produce an output of 0V – 10V, whilst the other produces DAC an output voltage (V_{fine}) of -0.1V – 0.1V. These voltages sum and input to the voltage/current control input V_1. When in voltage mode V_{fine}'s output contribution set to 0V and V_{coarse} causes the output to vary between 0V – 10V, producing a total output of 0 – 10V. When in current mode V_{coarse} sets to the output to 10V and V_{fine} contributes between -0.1V – 0.1V, producing a combined output of 9.9V – 10.1V.

[1] See SMU revision D in Errata

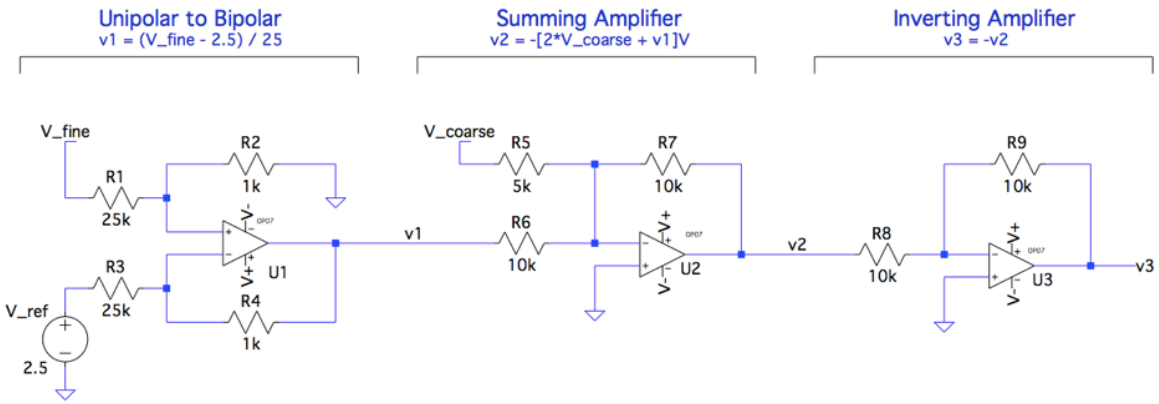


Figure 5.19. Fine and Coarse Control Hardware Realization

Figure 5.19 shows the implementation of the functionality described above. The first block consisting of U_1, R_1-R_4, and V_{ref} scales and shifts the V_{fine} voltage. The U_2 and R_5-R_7 block sums the conditioned V_{fine} and V_{coarse} times 2. The U_3, R_8, R_9 inverts the voltage for an end result shown in equation 4.

$$V_3 = 2 * V_{coarse} + \frac{V_{fine} - 2.5}{25} \tag{4}$$

When V_{fine} and V_{coarse} vary from 0 – 5V, the appropriate voltages for control are produced.

An improvement to this design allows for the removal of an additional op-amp. Figure 5.20 shows a modified version with the same output voltage characteristics but with fewer components. This design was made after the SMU circuit board was ordered and is not on the Revision C schematic. The author recommends this improved design.

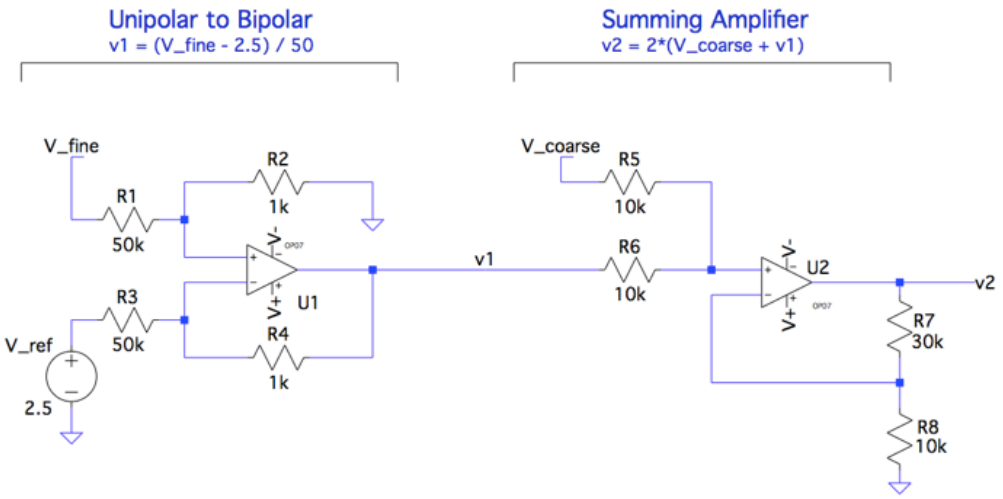


Figure 5.20. Fine and Coarse Control Hardware Realization With One Less Op-Amp

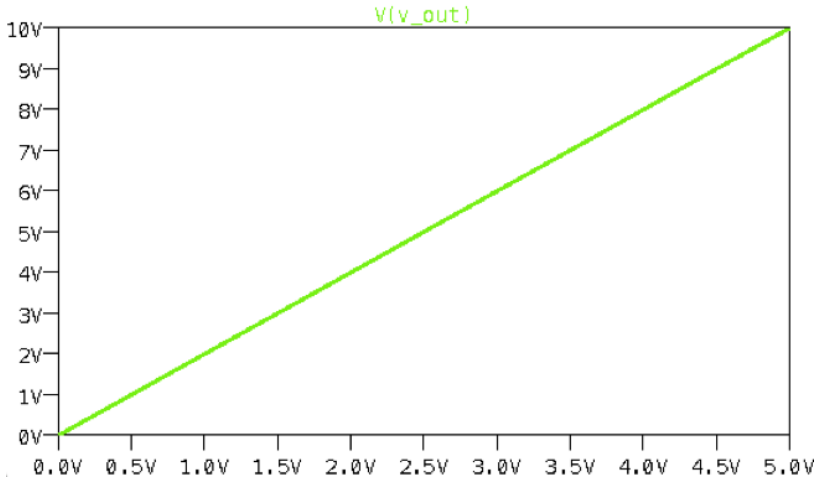


Figure 5.21. Output of Fine/Coarse Control for Voltage Mode

Figure 5.21 shows the output voltage when V_{fine} is a constant 2.5V and V_{coarse} varies from 0-5V. The output varies from 0-10V.

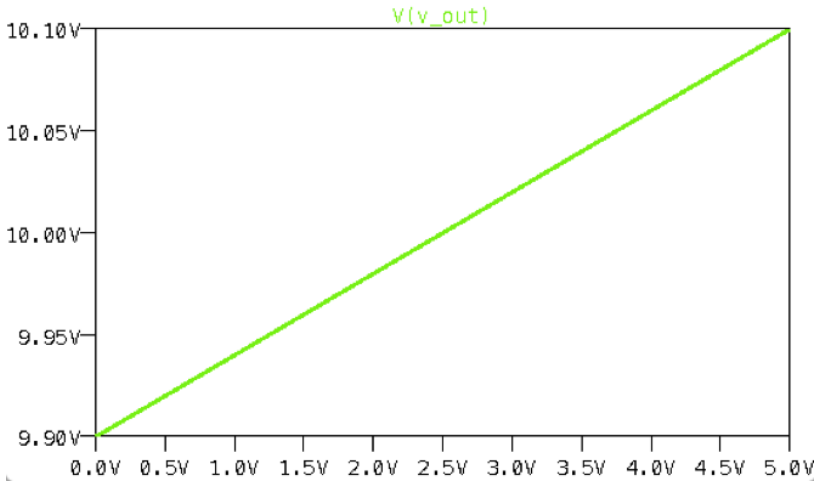


Figure 5.22. Output of Fine/Coarse Control for Current Mode

Figure 5.22 shows the output voltage when V_{coarse} is a constant 5V and V_{fine} varies from 0-5V. The output varies from 9.9-10.1V.

With the Fine/Coarse Adjustment complete, the SMU system design concludes.

5.3 Analog Input Output

5.3.1 Analog Input

The Analog Input and Outputs (AIO) are constrained mostly by the resolution specifications. The target voltage resolution is 100µV. A full scale range of ±10V calls for an 18-bit ADC/DAC. These ADC/DACs are typically slow; not a concern, but have an input/output range of 0 – 5V, which is. Bipolar to unipolar and unipolar to bipolar conversion techniques are needed to interface the systems to the outside world.

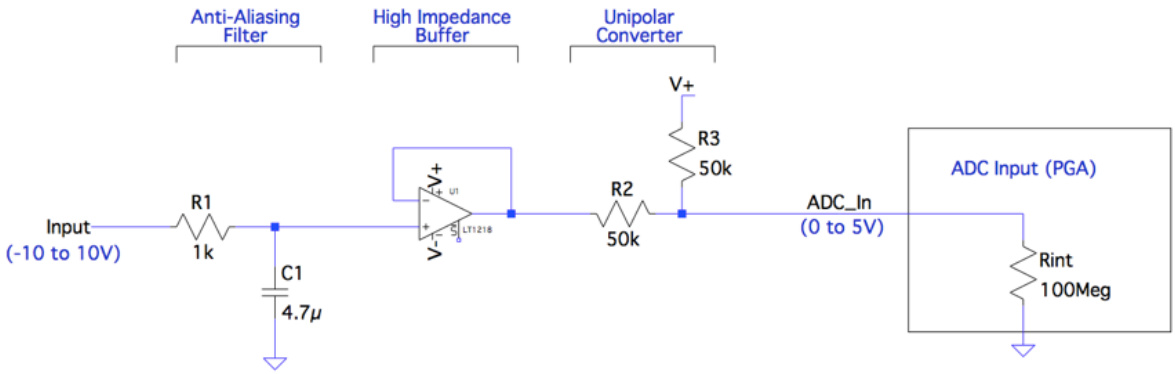


Figure 5.23. Input Circuity to the Analog to Digital Converter

The ADC chosen for the analog input is the ADS1220. This ADC is 24-bit, with up to 20 bits of effective resolution. This is more than the 18-bit needed for the target resolution. The ADS1220 has SPI communication and digital 50-60Hz rejection filters. For these reasons it is optimal for the analog input. The main drawback of the ADS1220 is that the input voltage range is 0 – 5V. The rest of the circuity shown in figure 5.23 is signal conditioning and protection.

R_1 and C_1 form a low-pass filter. The purpose of this filter is to reduce the effects of aliasing on the output data. The cutoff frequency of this antialiasing filter is 1/RC, set at roughly the sampling rate (20Hz).

The buffer U_1 (OPA4197) allows for a high impedance input. As a result, the analog input circuit does not draw a significant current. The input bias current of the OPA4197 is 5pA typical and 20pA maximum (at TA = 25°C) 17.

The Differential-Impedance of the OPA4197 is 100MΩ. The voltage between the inputs is the output voltage divided by the DC gain (120dB). Equations 5-7 the current drawn from the op-amp's differential loading is at most 0.1pA. This current is negligible compared to input bias current.

$$Gain = 120dB = 1E6V/V \tag{5}$$

$$V_+ - V_- = \frac{10V}{Gain} = 10\mu V \tag{6}$$

$$I_{in}^{DiffMode} = \frac{10\mu V}{100M\Omega} = 0.1pA \tag{7}$$

The Common-Mode Impedance is 10E12Ω. This impedance is seen toward ground. Equation 8 shows the maximum current draw from the common mode loading is 1pA, occurring at the maximum input voltage of 10V. This current is comparable to the typical input bias current.

$$\frac{10V}{10E12} = 1pA. \tag{8}$$

Therefore, the total input current draw is roughly 21pA at worst, and is expected to be in the single digit picoamps during normal operation. This current draw is magnitudes lower than what is necessary to not load a typical undergraduate circuit.

The OPA4197 also has internal EMI protection which prevents ESD strikes and other overvoltage events from damaging the ADC. The anti-aliasing filter also protects the circuit from such events.

R_2 and R_3 convert the bipolar signal (-10 – 10V) to a unipolar one (0 – 5V).[2] The simple resistive divider attenuates and DC offsets the oncoming signal. The resistor values are chosen to not load the buffer as well to not cause significant voltage error from the voltage divider with the ADC input. The ADC input is 100MΩ minimum 18. The potential error caused by the loading of the ADC is 0.05%. This error is linear and is calibrated out. The R_2, R_3 resistor tolerance also contribute linear error; nothing to worry over.

[2] Actually 0-10V, see errata

5.3.2 Analog Output

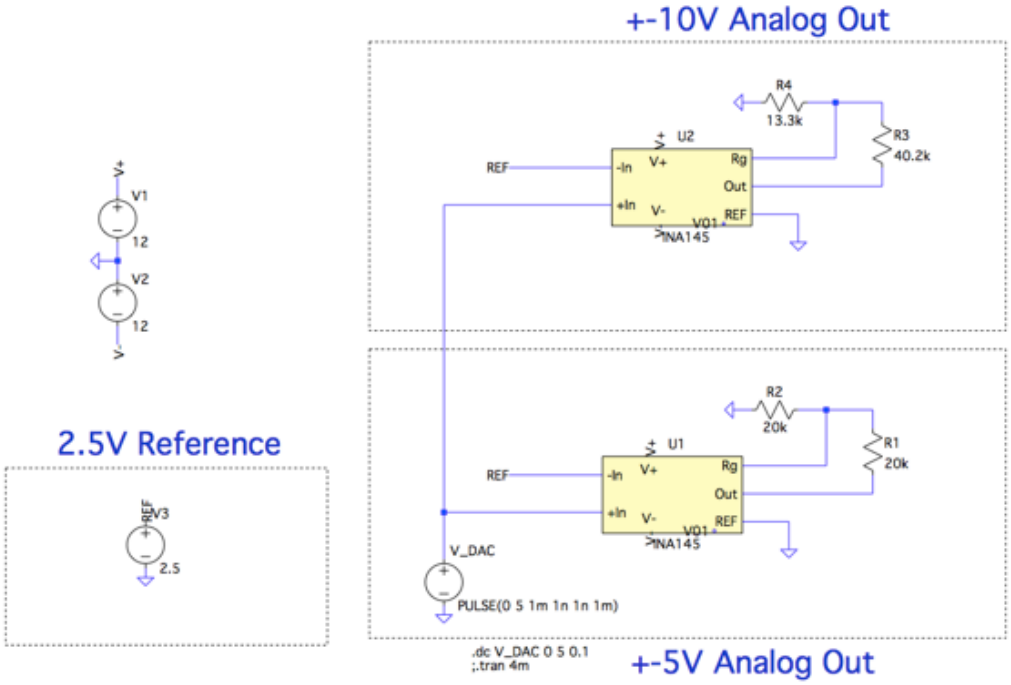
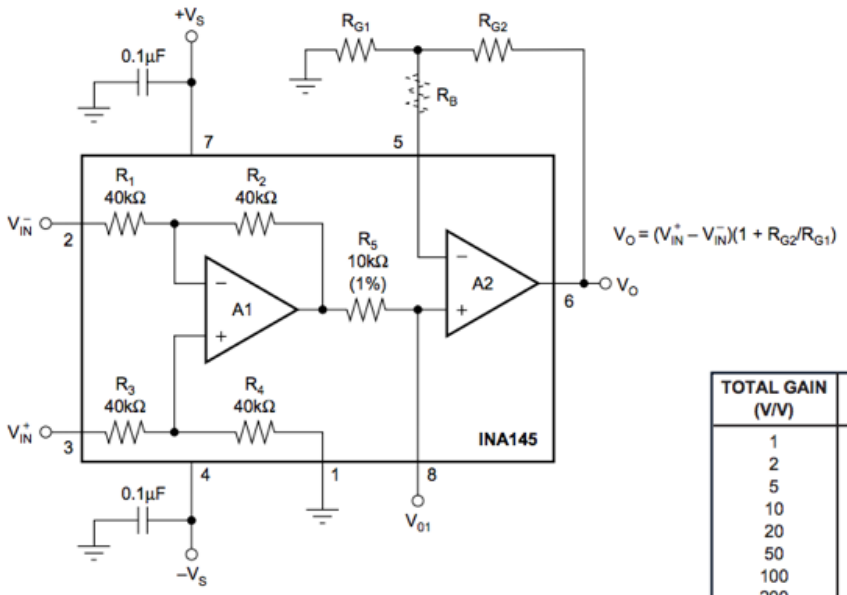


Figure 5.24. Output Circuity for the Digital to Analog Converter

The Digital to Analog Converter (DAC) used is the MAX5134AGUE+. The output range is 0 – 5V, which needs to modified to meet the -5 – 5V and -10 – 10V output requirements. A INA145 difference amplifier converts the voltages to these ranges. Equation 9 shows the output voltage equation for a difference amplifier.

$$V_{out} = (V_{in+} - V_{in-}) * Gain \tag{9}$$

A mid DAC output voltage reference of 2.5V provides a symmetrical positive and negative output. Gains of 2 and 4 are needed to produce ±5V and ±10V.



		STANDARD 1% RESISTORS		
TOTAL GAIN (V/V)	A2 GAIN (V/V)	R_{G1} (W)	R_{G2} (W)	R_B (W)
1	1	(None)	10k	—
2	2	20k	20k	—
5	5	12.4k	49.9k	—
10	10	11.0k	100k	—
20	20	10.5k	200k	—
50	50	10.2k	499k	—
100	100	10.2k	1M	—
200	200	499	100k	9.53k
500	500	100	49.9k	10k
1000	1000	100	100k	10k

Figure 5.25. INA145 Adjustable Gain Difference Amplifier Design Recommendations 20

Figure 5.25 shows an excerpt from the The INA145 datasheet. The excerpt shows the gain equation and recommended resistor values. The datasheet also recommends that the parallel impedance of the gain setting resistors is equivalent to the R_5 impedance (10kΩ). For a gain of 2, R_{G1} and R_{G2} values of 20kΩ are used. For a gain of 5, R_{G2} is 40.2kΩ and R_{G1} is 13.3kΩ. This results in an equivalent resistance of 9.99kΩ, and a gain of 4.02. The author is very proud of this.

5.4 Digital Input Output

5.4.1 Digital Input

The Digital Input Output (DIO) specifications are fairly lax in comparison to the rest of the subsystems. To accommodate various logic families, adjustable V_{IL}, V_{IH}, V_{OL}, V_{OH} levels are needed. Despite the digital signal having an analog range of values, a full-fledged ADC is not necessary for the input. The digital inputs are built with a comparator and adjustable voltage threshold. The non-inverting terminal of the comparator is the input, and the inverting terminal is a variable threshold voltage. The threshold voltage would be the average of the V_{IL} and V_{IH} levels. Figure 5.26 shows an example of this.

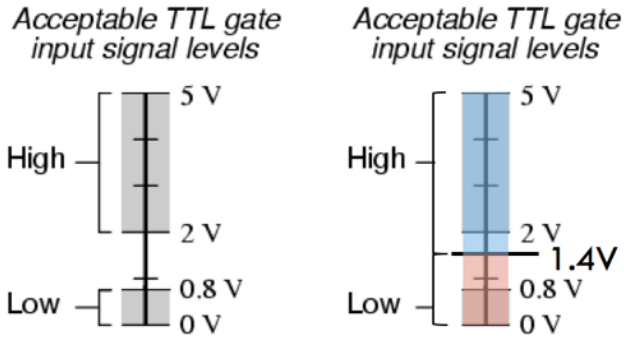


Figure 5.26. Graph Showing Threshold Voltage Set From Average of TTL Voltage Levels

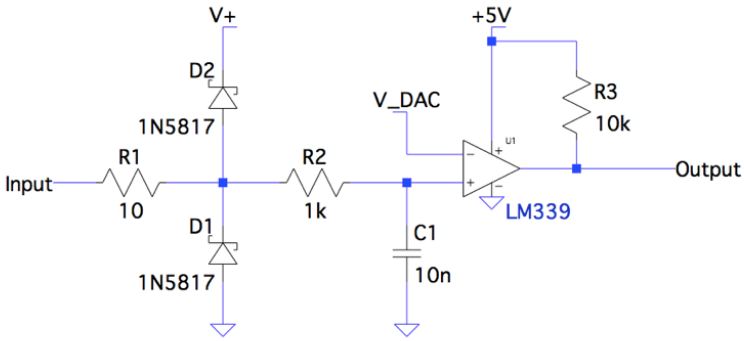


Figure 5.27. Digital Input Structure with ESD/Overvoltage Protection

Figure 5.27 shows the digital input circuit. D_1 and D_2 clamp the input voltage from roughly 0–5V. R_1 limits the current flowing through the diodes. This prevents from any potential transient voltage spikes from reaching any internal circuity. R_2 and C_1 form a low-pass filter, reducing noise sensitivity and further protecting from voltage spikes. The LM339 (U_1)is a cheap comparator.

The DAC used is the DAC084S085. The DAC084S085 is a quad channel, 8-bit DAC. The digital input does not require high resolution. Differences in V_{IL} and V_{IH} are typically in the hundreds of millivolts. A 8-bit DAC with an full scale range of has a voltage resolution of roughly 20mV. The DAC used can adequately distinguish between digital input voltages.

5.4.2 Digital Output

Figure 5.28 shows the digital ouput circuit. The circuit is simply a voltage follower with an isolation resistor. The voltage follower boosts the maximum output current of the circuit. The resistor improves stability when driving capacitive loads. Again, DAC084S085 is used, for the same reasons as stated previously.

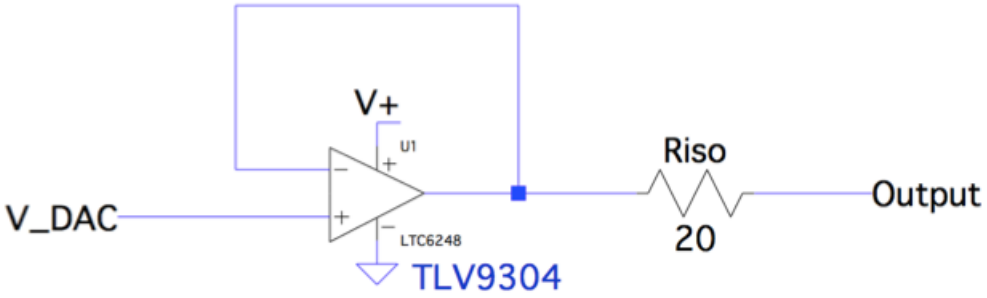


Figure 5.28. Digital Output Structure

6 Testing

> The proper method for inquiring after the properties of things is to deduce them from experiments.
>
> *Isaac Newton*

6.1 Power Supply

The Power Supply was the first subsystem tested, as such was approached with a very cautious optimism. It came as no surprise when the board didn't work when first powered up. The current draw of the board was large, drawing over 500mA at 15V. A measurement of the REF5050 reference voltage showed a reading of 2V, indicating that the DAC was drawing substantial current. For testing purposes, a 5V power supply temporarily replaced the REF5050. When the DAC outputs are set to output 2.5V (mid-scale), pin 9 (AO6) remained at 5V. Coincidentally, pin 9 is next to the 5V power rail of the DAC. A continuity test confirmed that the two pins are shorted. After a quick solder cleanup, the DAC draws less than 10mA and has all outputs fully functioning.

The first test of a power supply is to characterize the voltage output under loading conditions. Each output is connected to a 330Ω resistive load, and had the output voltage monitored as a function of input code sent to the DAC. Table 6.1 and figure 6.1 show the relative error.

Table 6.1. Output Voltage of Each Supply From a Given Hexadecimal Code

		Output 1		Output 2		Output 3		All Outputs
Code (h)	Set Voltage	Load Voltage 1	% vary	Load Voltage 2	% vary	Load Voltage 3	% vary	Total Power (mW)
0	0	0.0056	-	0.0065	-	-0.0049	-	0.0
22	0.5	0.507	1.400	0.503	0.600	-0.505	1.000	0.8
44	1	1.007	0.700	1	0.000	-0.999	-0.100	3.1
88	2	2.005	0.250	1.998	-0.100	-1.999	-0.050	12.2
CD	3	3.02	0.667	3.009	0.300	-3.006	0.200	27.7
111	4	4.015	0.375	4.001	0.025	-4	0.000	48.9
155	5	5.009	0.180	4.994	-0.120	-4.99	-0.200	76.2
199	6	6.004	0.067	5.987	-0.217	-5.98	-0.333	109.5
1DD	7	6.997	-0.043	6.982	-0.257	-6.971	-0.414	148.8
222	8	8.004	0.050	7.99	-0.125	-7.976	-0.300	194.8
266	9	8.997	-0.033	8.982	-0.200	-8.966	-0.378	246.2
2AA	10	9.992	-0.080	9.975	-0.250	-9.957	-0.430	303.6
2EE	11	10.984	-0.145	10.967	-0.300	-10.947	-0.482	366.9
332	12	11.967	-0.275	11.959	-0.342	-11.938	-0.517	435.5

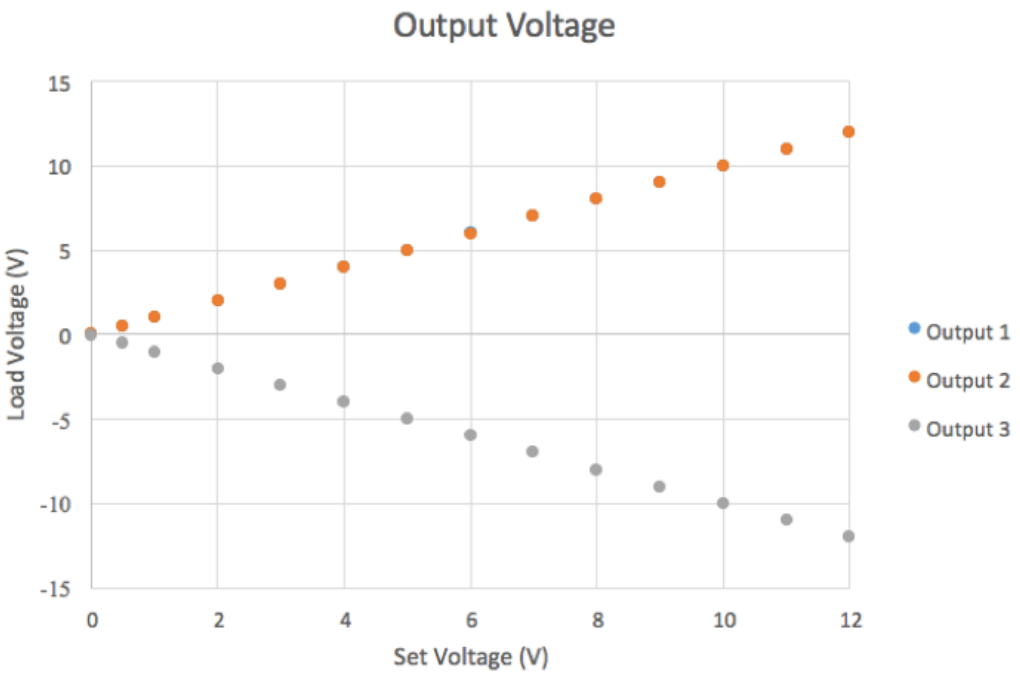


Figure 6.1. Power Supply Output vs Input Voltage

6.1.1 Line Regulation

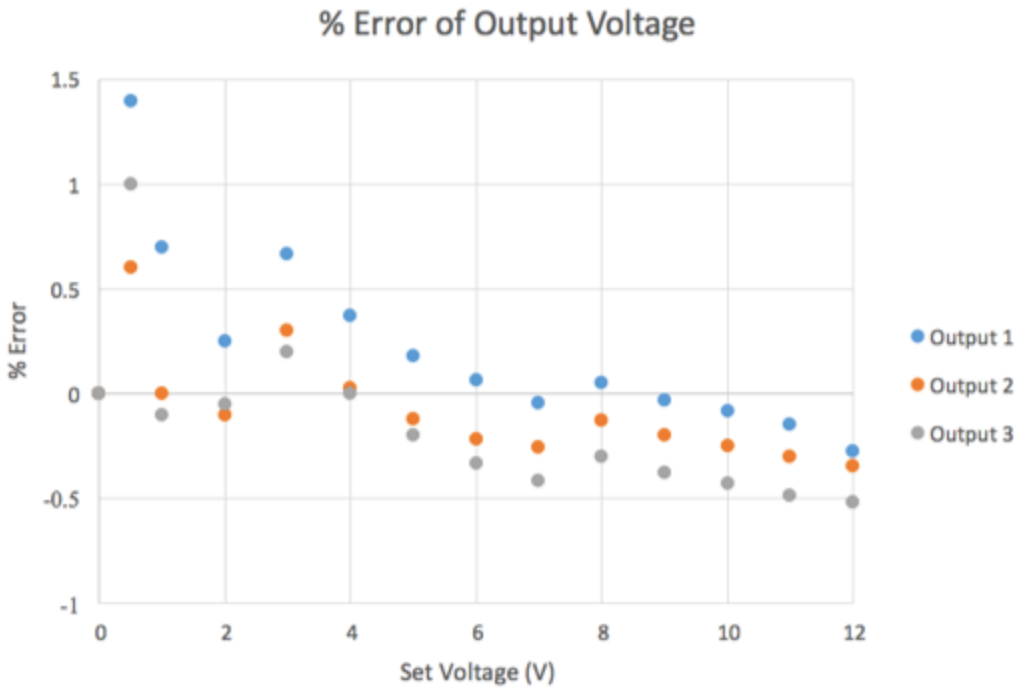
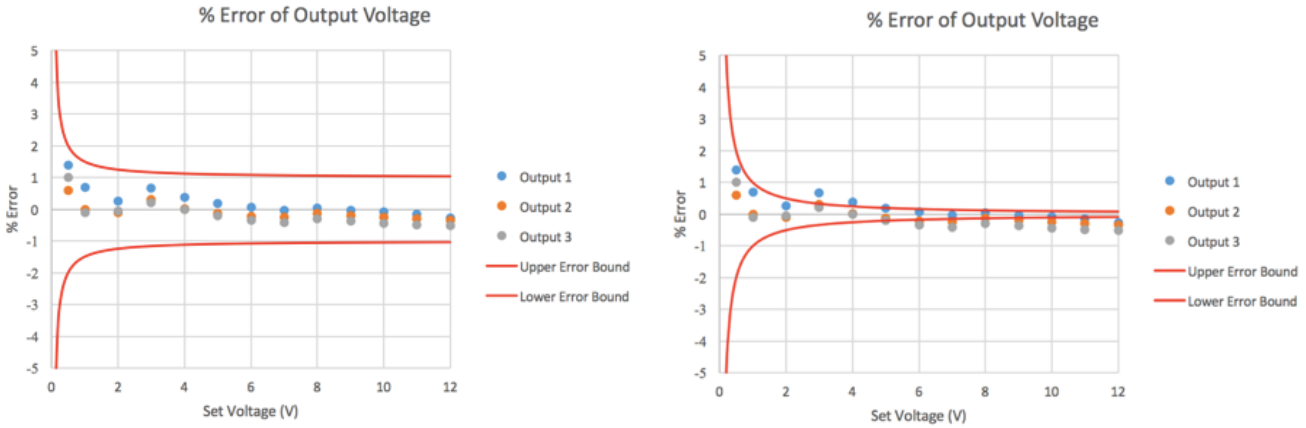


Figure 6.2. Voltage % Error at Selected Set Voltages

Figure 6.1 shows the output voltages of each power supply vary linearly as a function of input code (set voltage). More interestingly, figure 6.2 shows the % voltage error at each output. After roughly 1V, the % error mainly resides in the ±0.5% range. This % error is a better specification than the original ±10mV spec. A ±10mV at a 12V output level is a relative % error of 0.083%, too stringent for the purpose of this project.

For reference, the Agilent E3631A has an output accuracy of ±(0.1% +5mV) on the 6V output 3. As this project likely has a much lower budget than that of Agilent's, the power supply output accuracy specification is changed to ±(1.0% +5mV). The error bounds of the original and new specification are shown in figure 6.3.



(a) New ±(1.0% +5mV) Accuracy Specification

(b) Former ±10mV Accuracy Specification

Figure 6.3. Measured % Error plotted on same axis of Error Specifications

All the measured data points fall in between the new specification bounds while only 50% of the measured points fit in the original ±10mV bound.

6.1.2 Load Regulation

The load regulation of the power supply is measured at an output voltage of 5V. The output voltage is monitored for a set of loads. Figure 6.4 shows the variation in load voltage for a range of resistive loads.

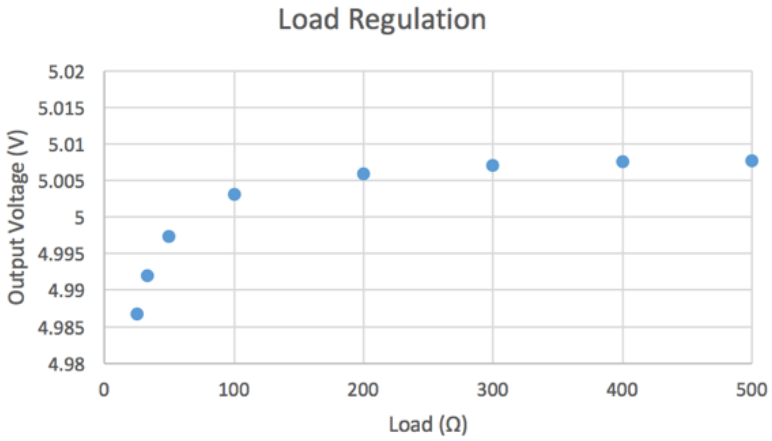


Figure 6.4. Variation in Output Voltage for Different Loads

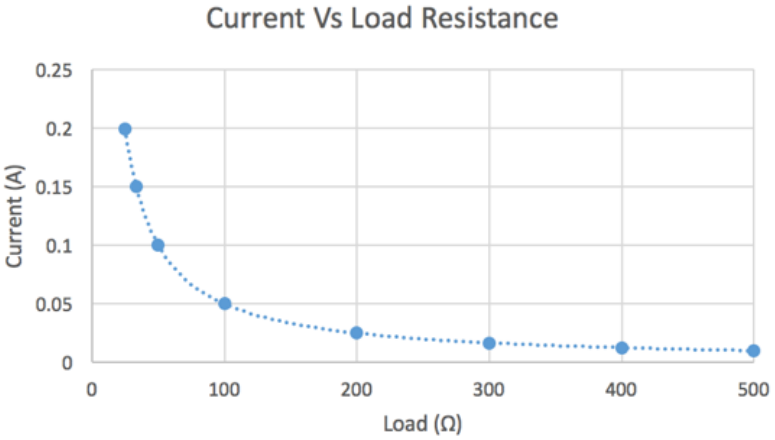


Figure 6.5. Current Demand of Different Loads

The heaviest load draws 200mA, and the lightest drew 1mA. The open circuit voltage is 5.0088V, and the 200mA current draw load voltage is 4.9867V. Measurements are done with an Agilent 34401A Multimeter. Equations 10 and 11 show the load regulation in percentage.

$$LoadRegulation(\%) = \frac{V_{max-load} - V_{min-load}}{V_{nom}} * 100 \tag{10}$$

$$0.422\% = \frac{5.0088 - 4.9867}{5} * 100 \tag{11}$$

6.1.3 Current Limiting

To the dismay of the author, each current shunt monitor needed calibration to accurately reflect the actual current delivered to the load. Figure 6.6 shows this calibration process test setup.

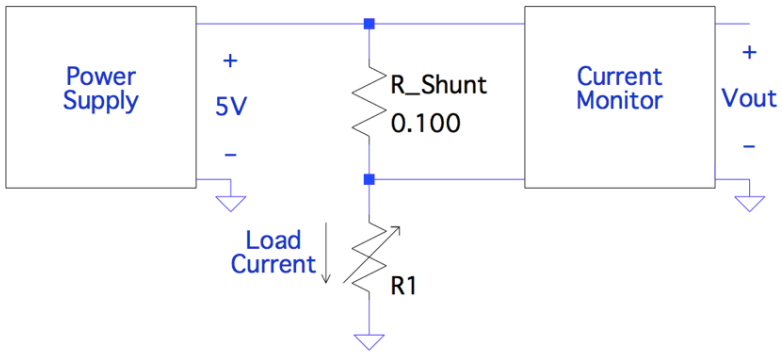


Figure 6.6. Current Limit Calibration Setup

R_1 is a potentiometer used to obtain different load currents. The load current is measured with an ammeter and the current monitor is measured with a voltmeter. The output of the current monitor is fit to the measured load current. Figure 6.7 shows the curve fit is linear, suggesting a simple gain and offset error.

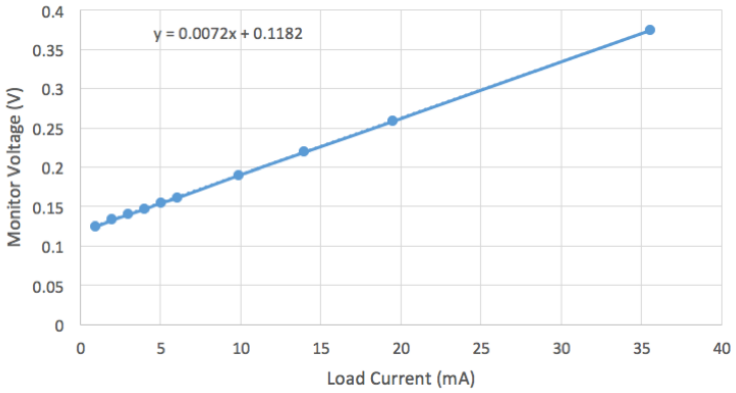


Figure 6.7. Current Shunt Amp Output 2 For Selected Load Currents

A 1st order linear equation adequately interpolates and extrapolates for other load currents. This trend equation models each current monitor. The code shown below implements the curve fit.

```
value = ((current_lim_1 * 0.0072 + 0.118) * MAX) / (REF); // current monitor scaling equation 1
output_BU257FV(value, PS_A04);                            // output 1 comparator channel

value = ((current_lim_2 * 0.0092 + 0.104) * MAX) / (REF); // current monitor scaling equation 2
output_BU257FV(value, PS_A05);                            // output 2 comparator channel

value = ((current_lim_3 * 0.0083 + 0.067) * MAX) / (REF); // current monitor scaling equation 3
output_BU257FV(value, PS_A03);                            // output 3 comparator channel
```

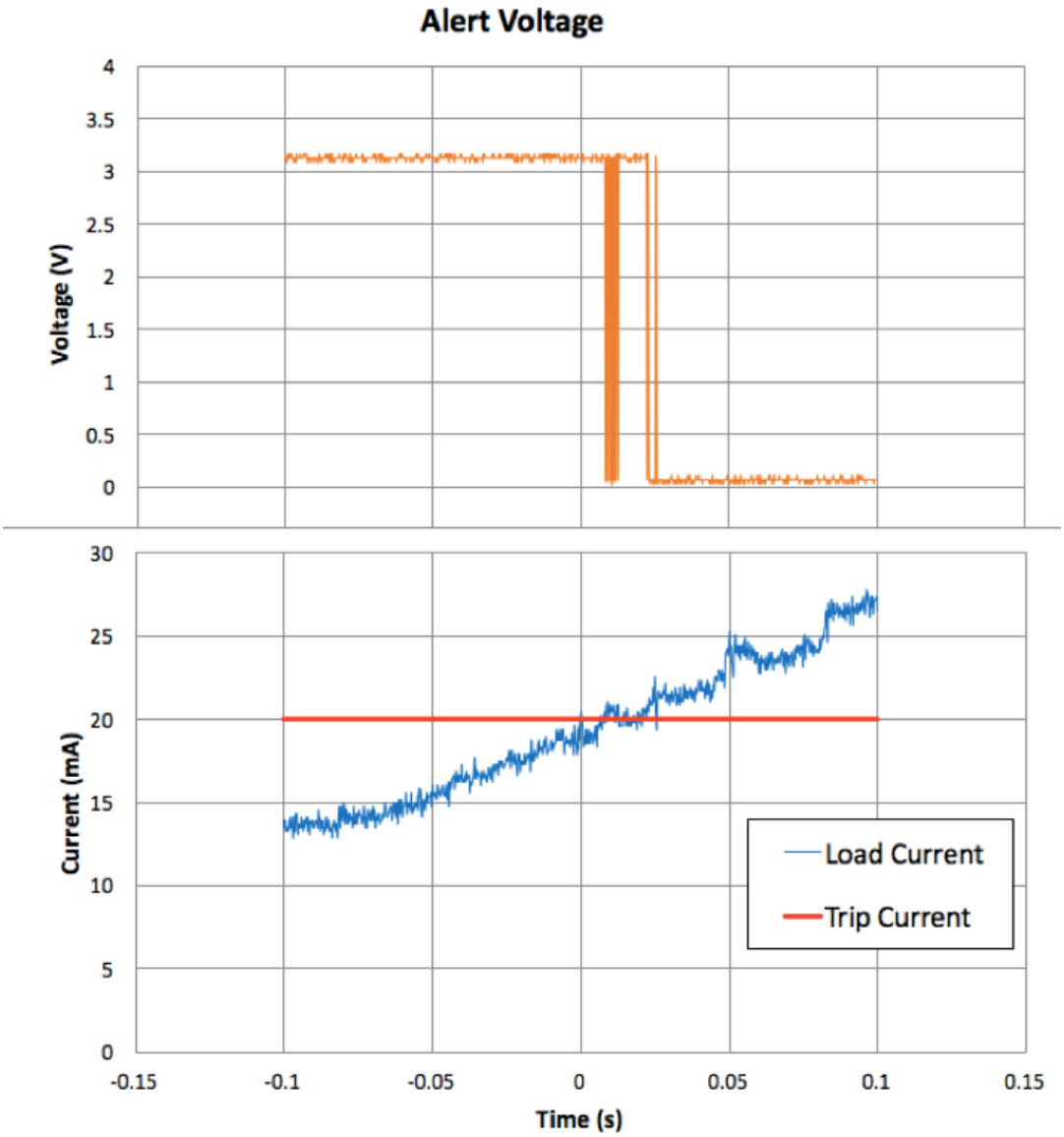


Figure 6.8. Alert Voltage Triggering on Overcurrent Event

Figure 6.8 shows an alert signal tripping when the load current exceeds a threshold. Although the 2000 data point scope data doesn't show the initial trip, the alert signal first toggled at 0 seconds. The scope single-shot triggered on the falling edge of the alert signal. The noise on the load current waveform is due to the hand turning of the mechanical potentiometer. The chatter on the alert voltage is not an issue, as the instant the alert voltage toggles, the microcontroller turns off the power supply, preventing further toggling and protecting the load.

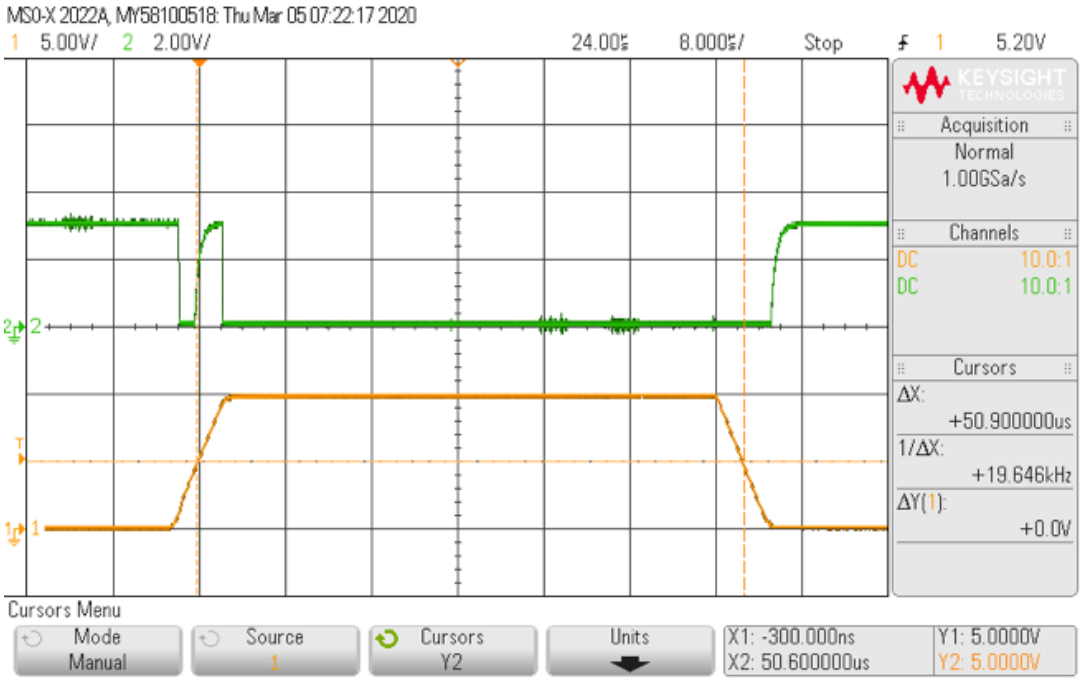


Figure 6.9. 100Ω Load with a 0–10V Step and 50mA Current Limit Load Voltage (Orange) and Alert (Green)

Figure 6.9 shows the current limit response time with a 100Ω load on the output. When a 0–10V step is applied, the load draws 100mA. A current limit of 50mA is at set. The response time is measured from the time that the load voltage is at 5V (load draws 50mA) to the time the load voltage decreases back to 5V. The response time in this case is 50.9µs. While no current limit time specification is defined, a fast response time is desirable to prevent damage to circuity.

Upon close inspection, two distinct noise pulses are seen on the alert waveform at t = 32 and 40µs. These pulses are caused by the EMI generated from the SPI communication from the microcontroller writing to the DAC to reset its output. The pulses are absent from the load voltage as the PCB power planes are well bypassed.

The pulses are of interest because they show the relative timings of the current limiting process. From the alert negative edge to the SPI communication initiation is 34µs. This 34µs is the time it takes for the microcontroller to interrupt on the falling edge of the alert, clear the interrupt flag, and call a SPI function. The SPI communication takes roughly 8µs, during which 16 bits are transmitted. After the SPI communication ends, the DAC takes another 8µs to change its output. The datasheet value for the BU2507FV output settling time (7µs typical) verifies this value 26.

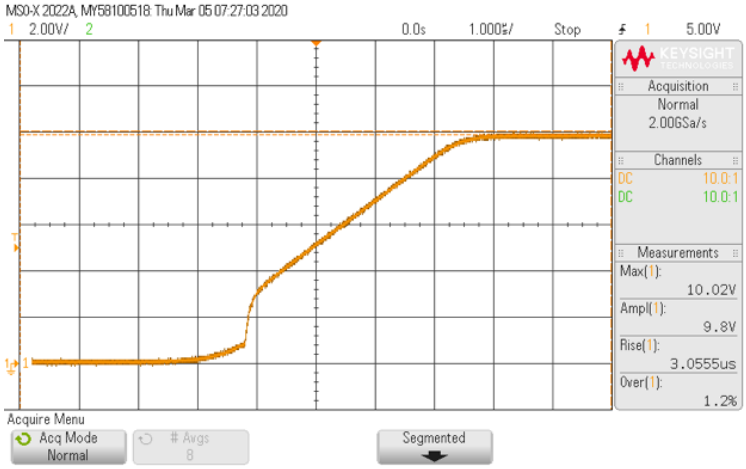
From the relative timings, the largest time sink is the microcontroller interrupt overhead. Faster clock frequencies result in faster response times. For the MSP432, the mere 3MHz execution speed used in testing can increase up to 48MHz with no external components.

Shown in the code below, the interrupt handler is minimalistic and free of erroneous activity. The code handling the interrupt and initiating SPI communication can not speed up in a meaningful way without increasing execution frequency.

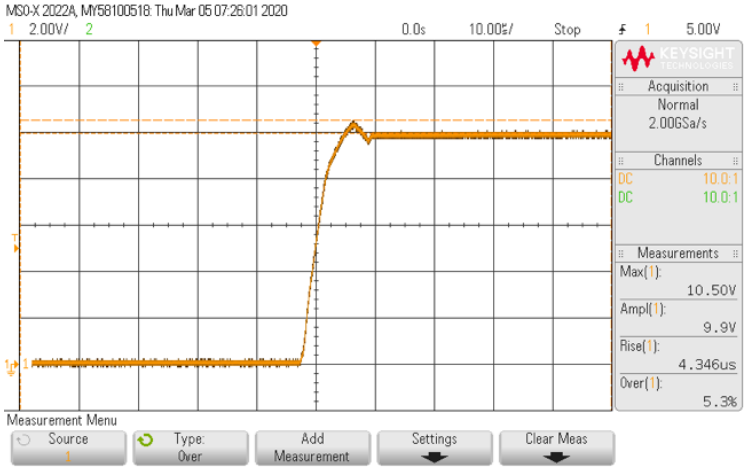
```
// Overcurrent Interrupt Handler

void PORT5_IRQHandler(void)
{
    if(P5->IFG & BIT0) // Supply 1
    {
        P5->IFG &= ~(BIT0);         // clear interrupt flag
        output_BU257FV(0, PS_A06); // output 0V
    }
    else if(P5->IFG & BIT1) // Supply 2
    {
        P5->IFG &= ~(BIT1);         // clear interrupt flag
        output_BU257FV(0, PS_A01); // output 0V
    }
    else if(P5->IFG & BIT2) // Supply 3
    {
        P5->IFG &= ~(BIT2);         // clear interrupt flag
        output_BU257FV(0, PS_A02); // output 0V
    }
}
```

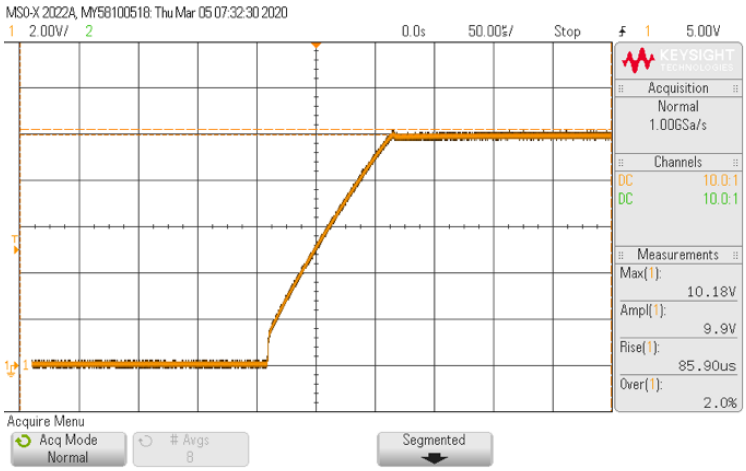
6.1.4 Transients



(a) 100Ω Load with a 0–10V Step



(b) 100Ω || 1µF Load with a 0–10V Step



(c) 100Ω || 10µF Load with a 0–10V Step

Figure 6.10. Step Response of Positive Power Supply Under Various Loading conditions

The power supply is subjected to a 0–10V input step under a set of loading conditions. Figure 6.10 shows the transient responses. Different load voltage slew rate and overshoots are seen based on the load capacitances. The slew rate of the power supply varied from 4V/µs to 0.08V/µs based on the capacitance present. The overshoot present suggests a damped response and therefore no stability concerns. All capacitors used were electrolytic, which have ESR values ranging from 1 – 100Ω at the capacitances and voltages tested 29.

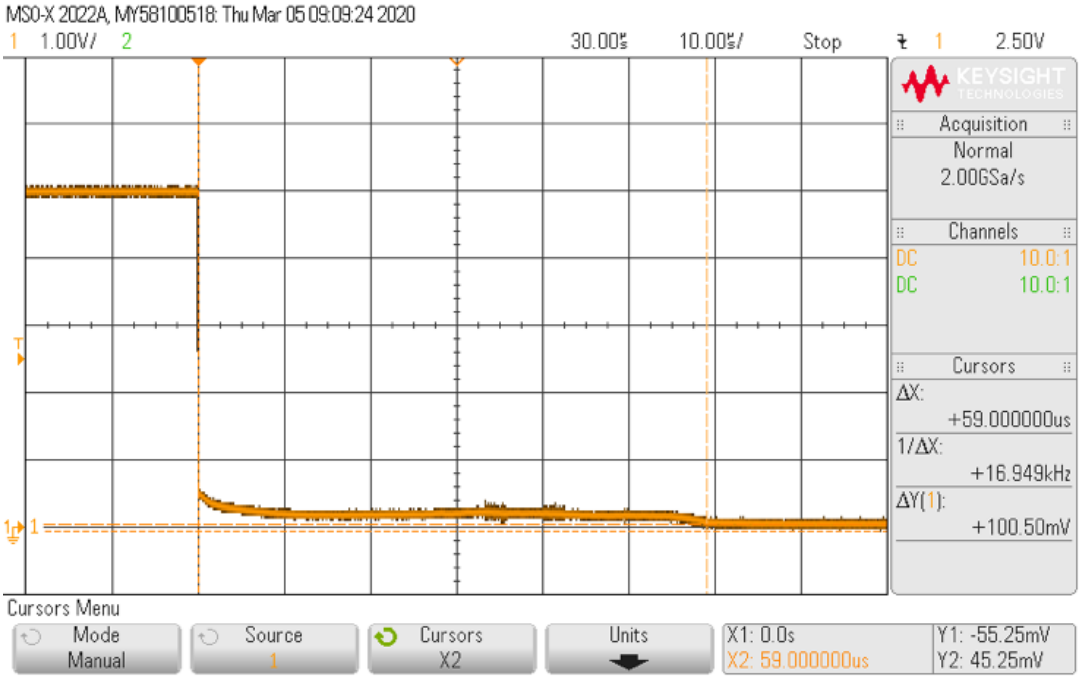


Figure 6.11. Power Supply Terminals Directly Shorted Transient

Figure 6.11 shows the final and most frightening transient test; the power supply terminals are shorted when outputting 5V. The terminal voltage instantly drops to 0.2V. The instantaneous current is likely in the amp range. However, after 59µs, the overcurrent protection activates and the output turns off. The power supply lives to see another day.

6.2 SMU

6.2.1 Early Prototype

As the first revision of the SMU showed promise, an early prototype is made. The prototype does not contain any relays; all connections are made manually. Figure 6.12 shows the bread-boarded prototype. This is the first circuit constructed during the course of the project.

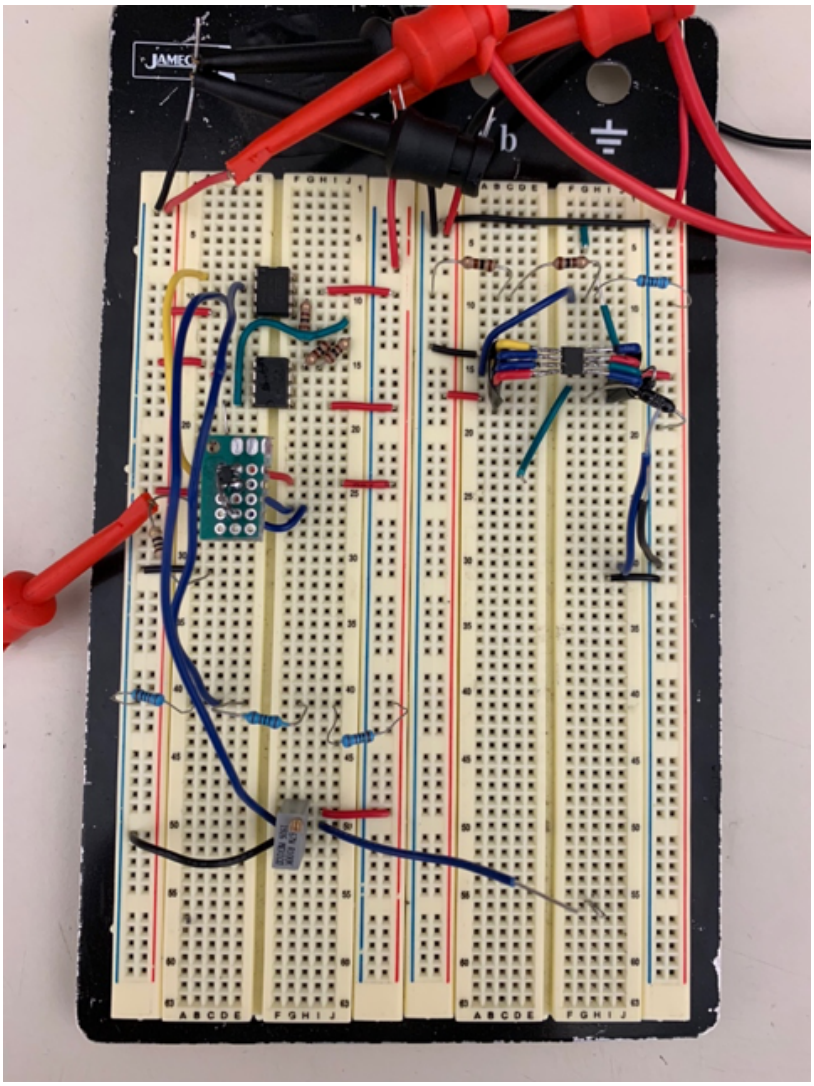
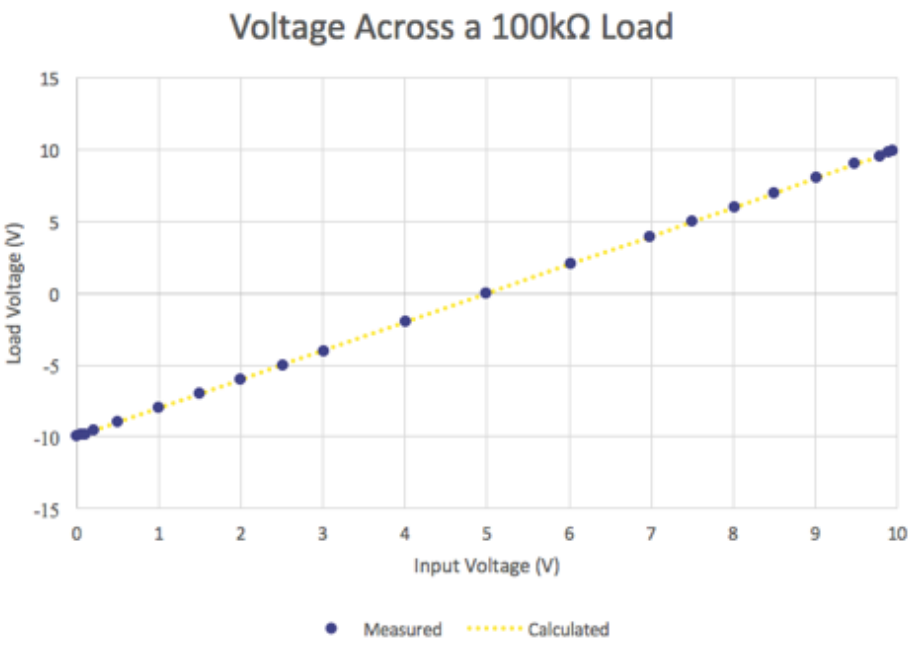
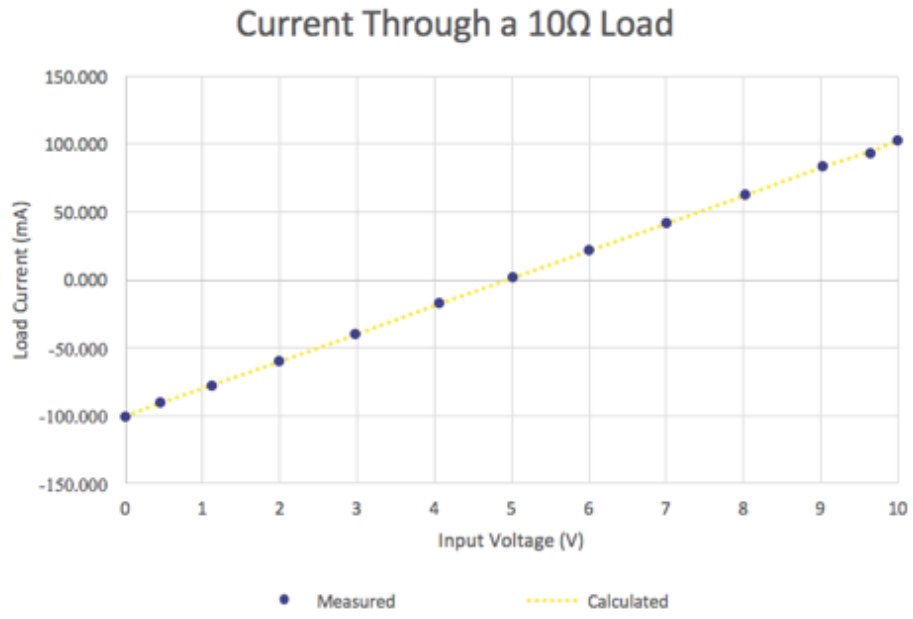


Figure 6.12. SMU Early Prototype on Breadboard

The circuit is crude: the reference voltages are generated from resistive dividers, and potentiometers mimic the DAC output voltages. Nevertheless, the circuit works as intended and proves its viability. Figure 6.13 shows the output voltage and current transfer characteristic of the prototype.



(a) Voltage Output



(b) Current Output

Figure 6.13. Voltage and Current Transfer Characteristics of Proto-SMU

Even without calibration nor proper voltage references, the voltage percent error is generally within 0.5% (for light loads) and the current percent error is generally within 1.0%. The prototype is deemed a success and development continued.

6.2.2 Voltage Mode

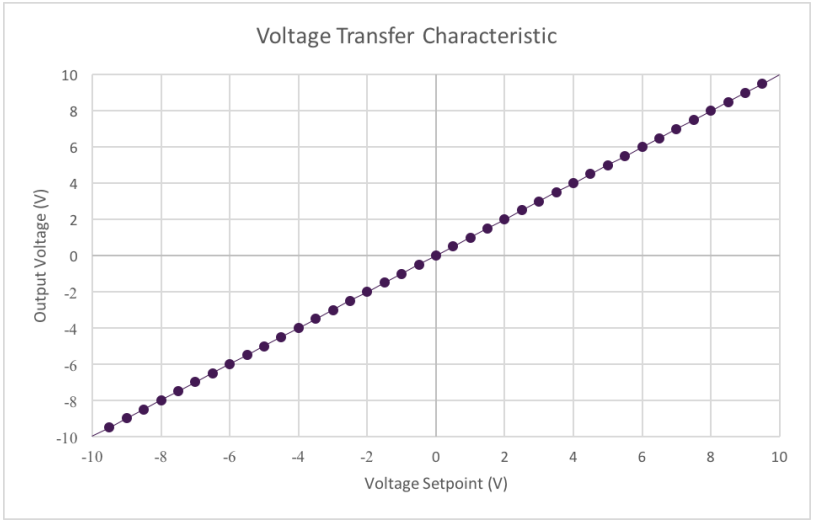
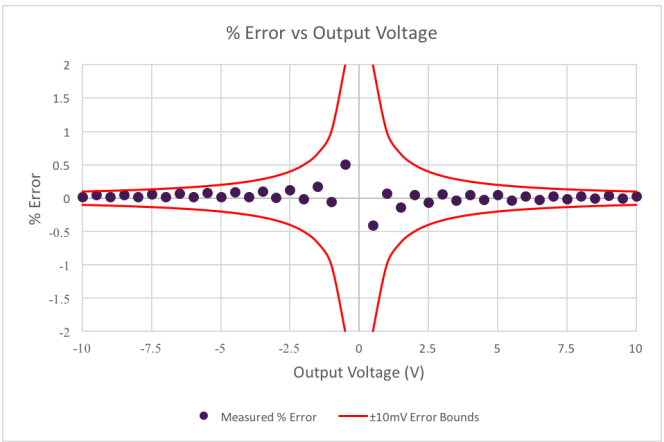


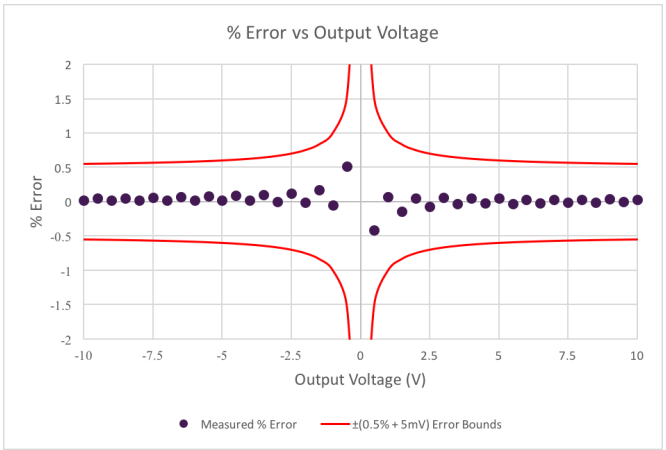
Figure 6.14. SMU Voltage Transfer Characteristic

Figure 6.14 shows the input vs no-load output voltage. Figure 6.15 shows the % error of the voltage output. The SMU voltage output meets the original specification of ±10mV. Nevertheless, an updated specification is preferred for some margin. Equation 12 shows the new specification. Figure 6.15a shows the original specification. Figure 6.15b shows the new error bounds.

$$\% \text{ Error Bounds} = \pm(0.5\% + 5mV) \tag{12}$$

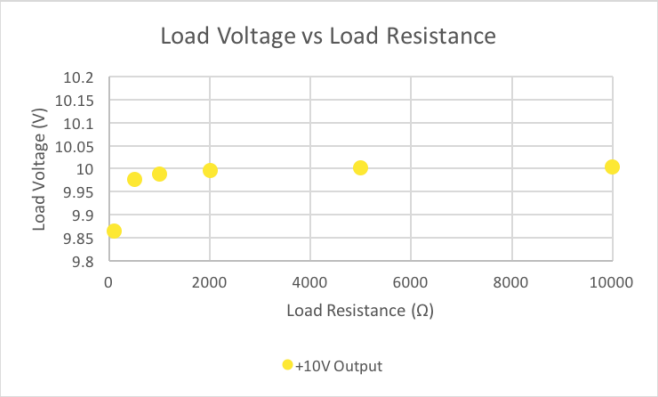


(a) Original Error Specification

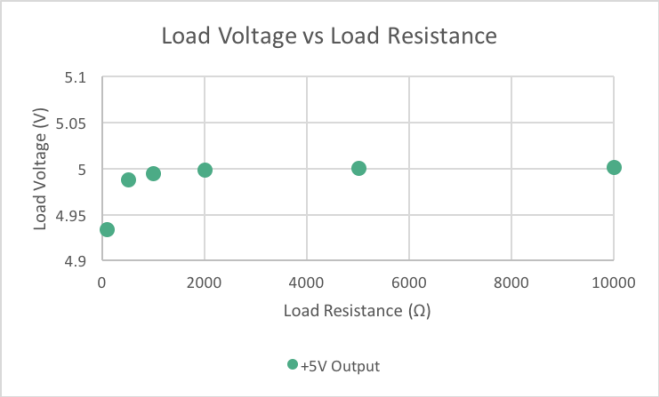


(b) Updated Error Specification

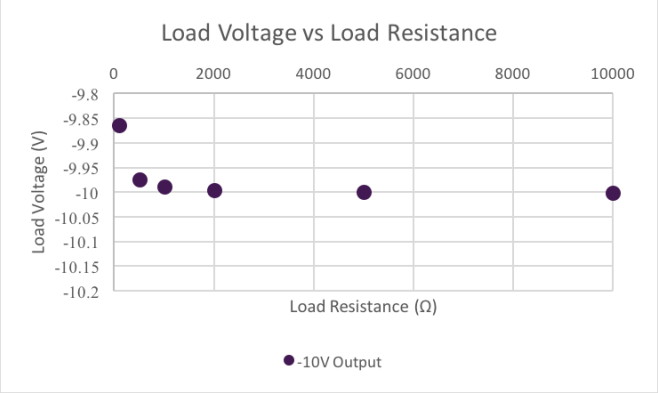
Figure 6.15. Measured Output Error with Original and Updated Specifications



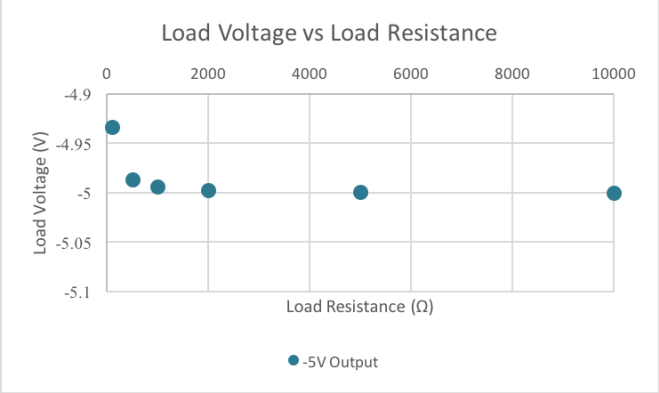
(a) +10V Output Load Regulation



(b) +5V Output Load Regulation



(c) -10V Output Load Regulation



(d) -5V Output Load Regulation

Figure 6.16. Load Regulations for Selected Output Voltages

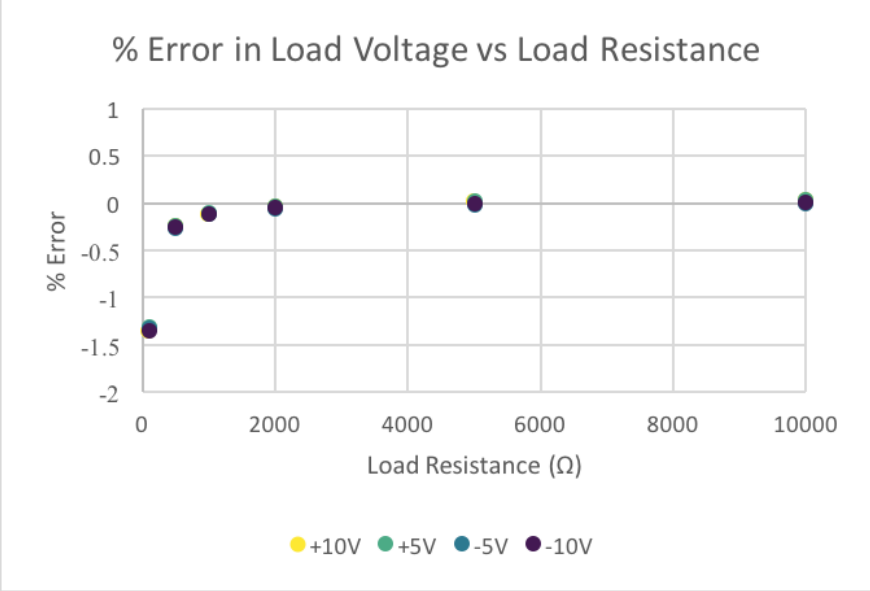


Figure 6.17. % Error of Load Voltages

Figure 6.16 show the SMU's load regulation for four output voltages. A load of 100Ω is the heaviest load tested. This load draws 100mA when attached to the ±10V outputs and 50mA for the ±5V outputs. Figure 6.17 show the % error of the outputs. Each of the four output voltages follow the same % error trend, indicating a constant output impedance. Equation 13 shows the formula used to calculate output impedance.

$$\text{Output Impedance} = \frac{V_{open-circuit} * \text{Load Resistance}}{V_{loaded}} - \text{Load Resistance} \tag{13}$$

From equation 13, the output impedance of the SMU averages to 1.36Ω. Figure 6.18 shows the main potential sources of output resistances.

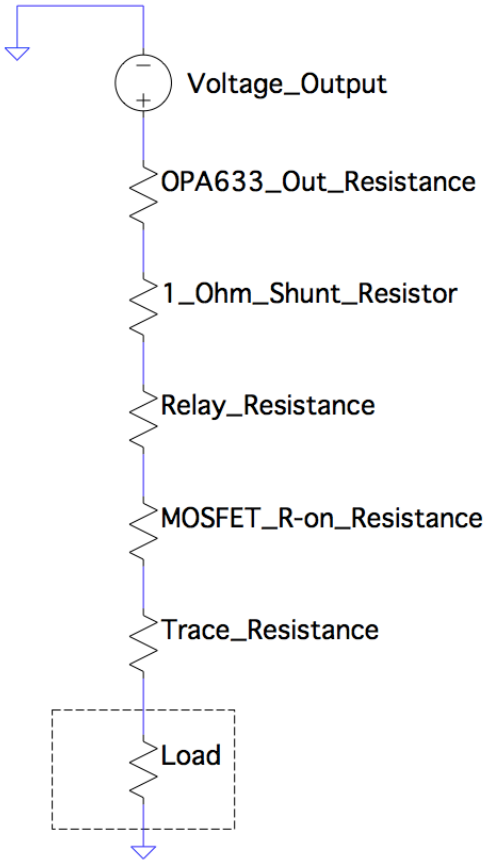


Figure 6.18. Resistors in Output Signal Path

Because the shunt resistor is 1Ω, the rest of the resistances sum to 360mΩ. The trace resistance is estimated to be roughly 10mΩ. This estimate comes from the trace width (7.62mm), trace thickness (2.8 mil), and trace length (30mm). The output resistance of the OPA633 is 5Ω typical 27. However, the output resistance is seen in a feedback path and is nullified as a result. The relay resistance is 150mΩ max. This leaves 200mΩ likely present from the MOSFETS. The MOSFETs are chosen for their low R_{DS-on} 24, 25.

6.2.3 Current Mode

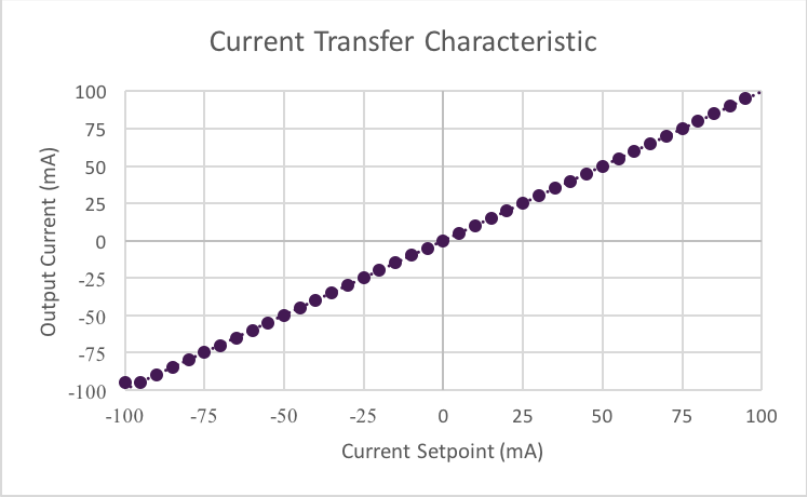
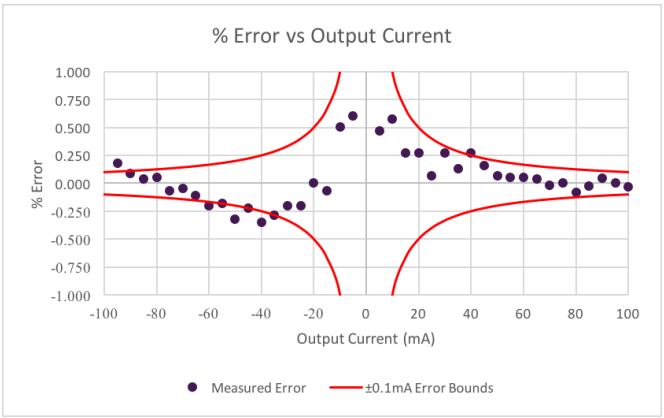


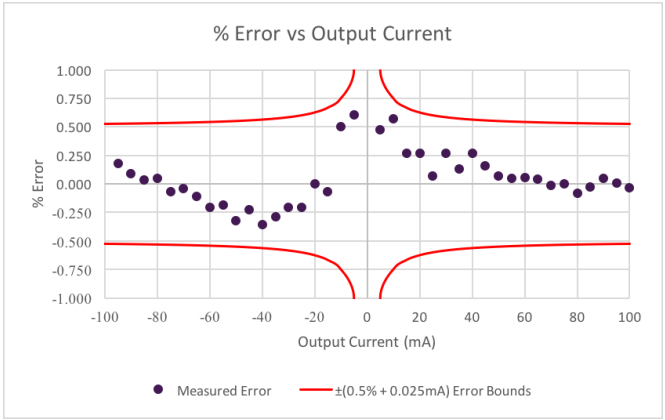
Figure 6.19. SMU Current Transfer Characteristic

Figure 6.19 shows the input vs output current. Figure 6.20 shows the % error of the voltage output. The SMU current output is close, but does not meet the original specification of ±0.1mA. Equation 14 shows an updated specification. Figure 6.20a shows the original specification. Figure 6.20b shows the new error bounds.

$$\% \text{ Error Bounds} = \pm(0.5\% + 25A) \tag{14}$$



(a) Original Error Specification



(b) Updated Error Specification

Figure 6.20. Measured Output Error with Original and Updated Specifications

An astute reader may notice that the bottom left most datapoint in figure 6.19 doesn't follow the trendline. This is because the calibrated code sent to the DAC is less than zero. The solution to this problem is to simply adjust the V_{coarse} DAC output upward by a few codes. This shifts the current transfer characteristic downward, allowing for the utilization of the full range. Figure 6.21 shows the zoomed out % error plots containing the erroneous datapoint.

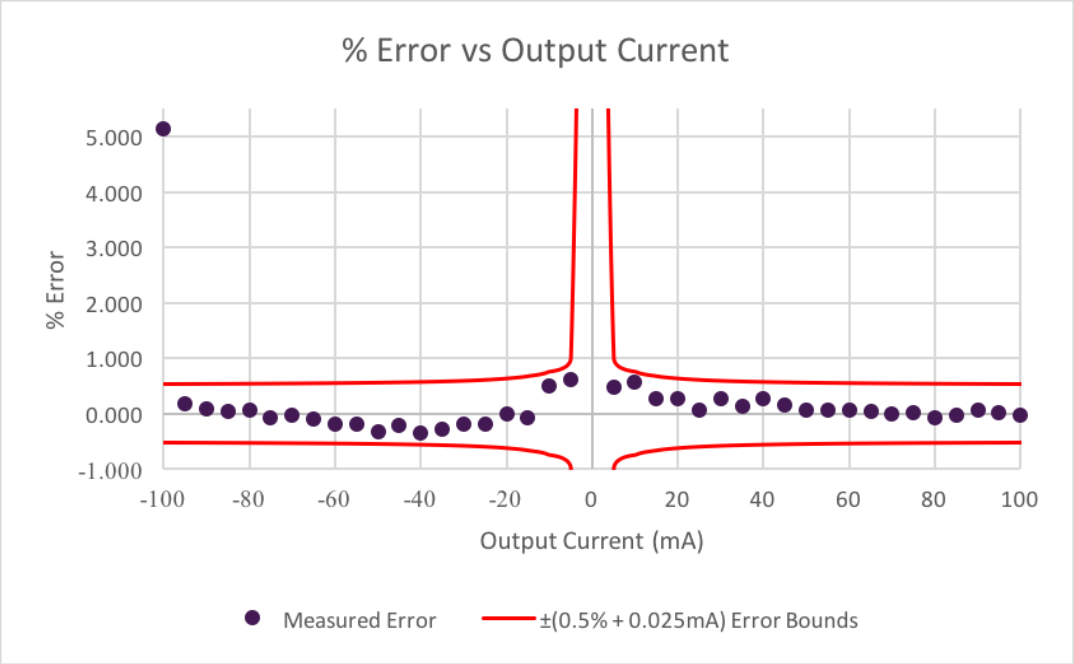


Figure 6.21. % Error of Current Mode (Zoomed Out View)

6.3 AIO

6.3.1 Analog Output

The analog output circuit has 4 different channels. Two channels output voltage from -10–10V, and the other two output -5–5V. Each channel needs calibration to account for various error sources in the system. Among these error sources are DAC offset and gain error, op-amp offset voltage, and gain setting resistor tolerance. Nullification of these errors is done with equations or look-up tables.

The main error sources affect either offset or gain of the output transfer function. These error terms are linear and are calibrated with a simple y = mx + b equation. A look-up table are used if more complicated errors are present (DAC integral non-linearity, for example).

Figure 6.22 shows the output error before and after calibration of analog output channel 3 as a function of full scale range percentage.

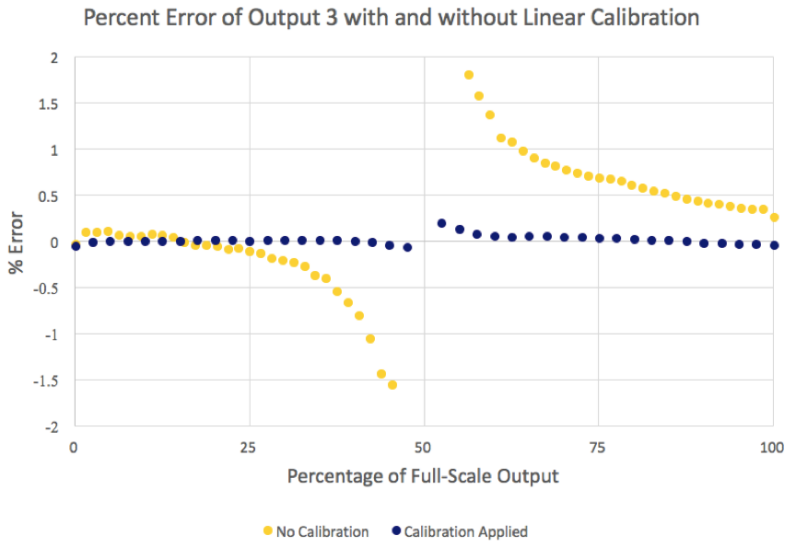


Figure 6.22. % Error Before and After Calibration (Output Channel 3)

After calibration the average magnitude of the error improved by a factor of 22.79. Additionally, the calibrated error now fits within error bounds of $\pm(0.1\% + 1\text{mV})$. The author deems this percent error impressive for a system with no feedback or other control circuity. The advantage of reaching such low error without feedback is that there are no stability concerns. Additionally, control circuity increases cost and board complexity.

Not all calibrations resulted in such a drastic improvement. Figure 6.23 shows the output error before and after calibration of analog output channel 0 as a function of full scale range percentage.

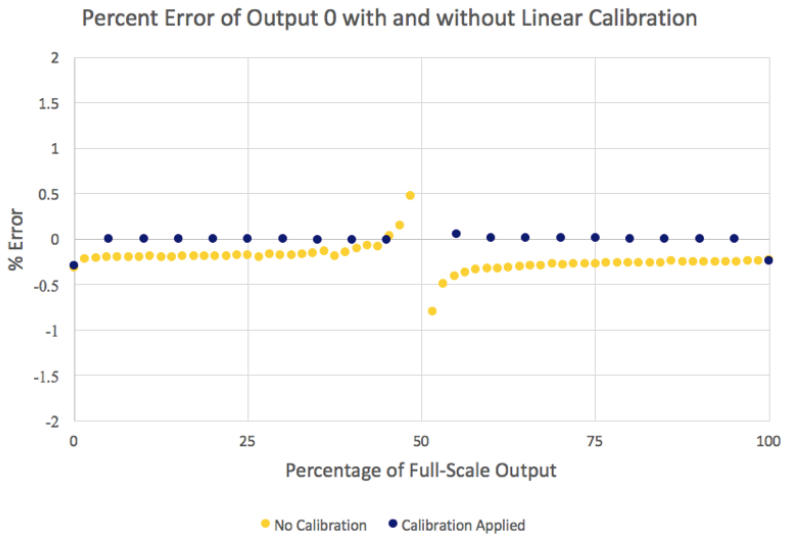


Figure 6.23. % Error Before and After Calibration (Output Channel 0)

The output percent error of output 0 is small even before calibration. While calibration reduces error even further, the two endpoints (output equal to 0% or 100% full scale range) show no improvement. Even

with a minimum or maximum code input, the output voltage did not reach the desired output voltage. This is because the ideal gain of the ±5V outputs is exactly 2. If any variation due to resistor tolerance decreases the gain, the output voltage can not reach the full scale output endpoints. As a result no improvement can be made to these values.[3]

[3]See errata for in-depth analysis and recommendations

6.3.2 Analog Input

The calibration process for the analog input is arduous. The ADC has 24 output bits, which correspond to a resolution of 1.192µV. Special measurement conditions are made when dealing with such a small voltage resolution. The Agilent 34401A 6½ digit multimeter has its terminals shorted for nulling out any offset. Multimeter measurements are averaged after given roughly 20 seconds to settle. The measurements the analog input takes are also averaged. The analog input takes the 8 most recent readings for its average. With these simple techniques, precise measurements are made.

The project's analog output feed into the analog input and the multimeter probe. At some points in time, this project has the capability to test itself. The author of this project shed a single tear of pride at the mere thought of this.

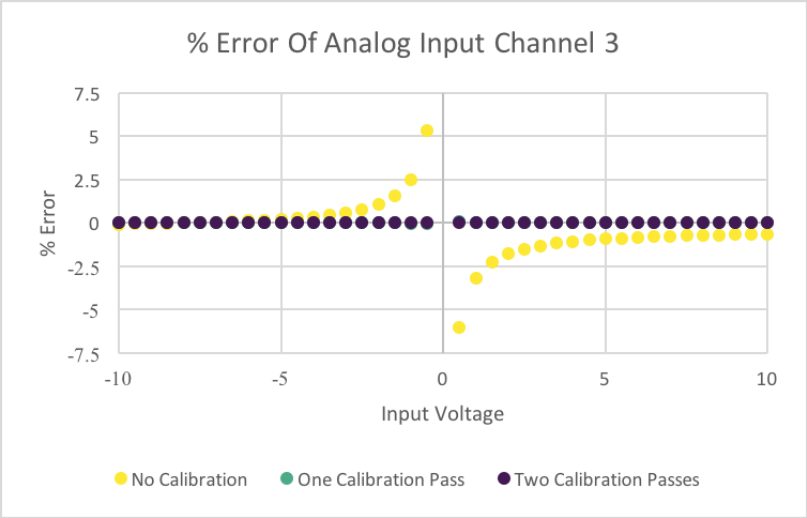


Figure 6.24. % Error with Zero, One, and Two Calibration Passes (Input Channel 3)

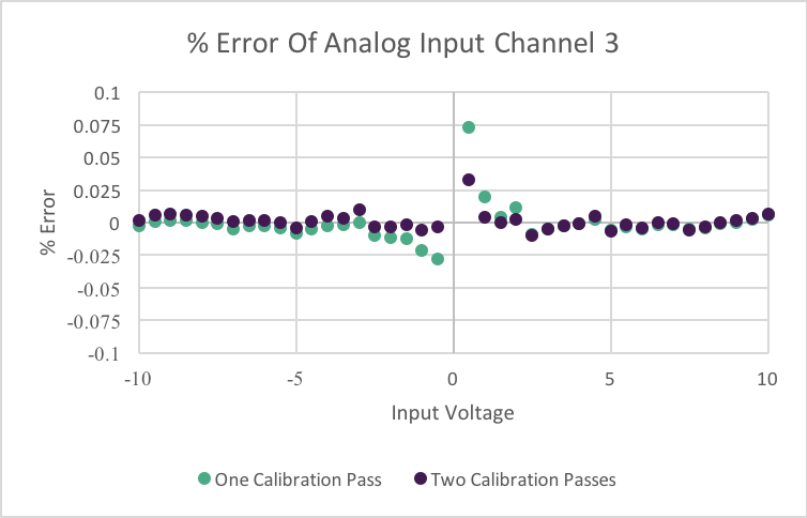


Figure 6.25. % Error One and Two Calibration Passes (Input Channel 3)

The analog input requires about 2-3 linear calibrations passes before acceptable results are seen. Eventually no notable improvement results from repeated calibrations. Figures 6.24 and 6.25 show the improvement calibration made. For reference, equation 15 shows the gain/offset correction equation for analog input channel 3.

$$voltage = reading * 1.00368548 + 0.0285495; \tag{15}$$

Each of the significant figures in equation 15 is relevant. A change in the last figure of the offset term results in hundreds of nanovolts of error. A change in the last figure of the linear term results in microvolts of error when at the maximum input voltages. Figure 6.26 show the happy consequences of such a tight calibration.

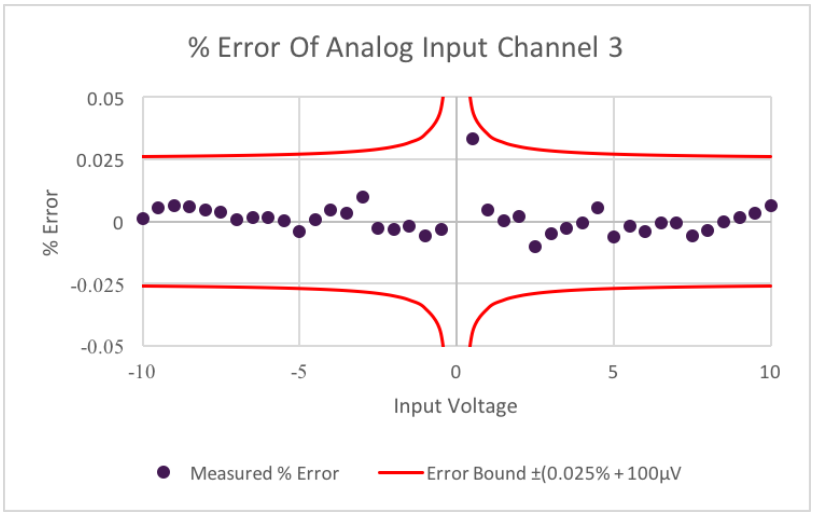


Figure 6.26. % Error After Two Calibrations with Error Bounds (Input Channel 3)

Equation 16 shows the error specification of the Analog input.

$$\%\ \text{Error Bounds} = \pm(0.025\% + 100\mu V) \tag{16}$$

6.4 DIO

6.4.1 Digital Output

The digital outputs did not require strenuous testing. Calibration even is forgone in pursuit of testing other subsystems. Nevertheless, some data is collected.

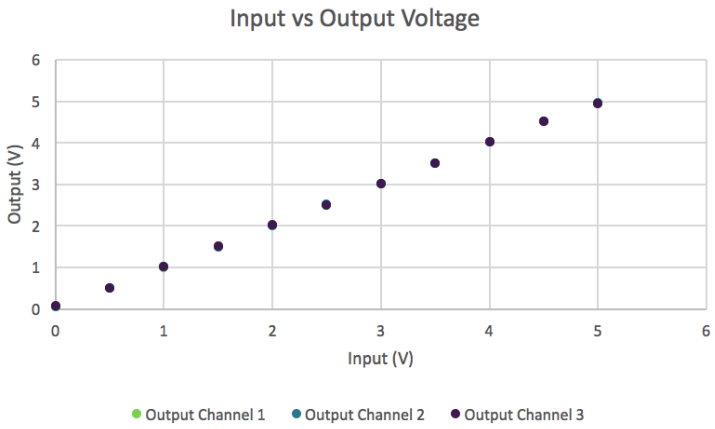


Figure 6.27. Output Voltage Transfer Characteristics of Digital Outputs

Figure 6.27 shows the output voltage transfer characteristic of three of the four digital outputs. Unfortunately digital output channel 0 burned out after it was shorted to 5V in a soldering mishap.

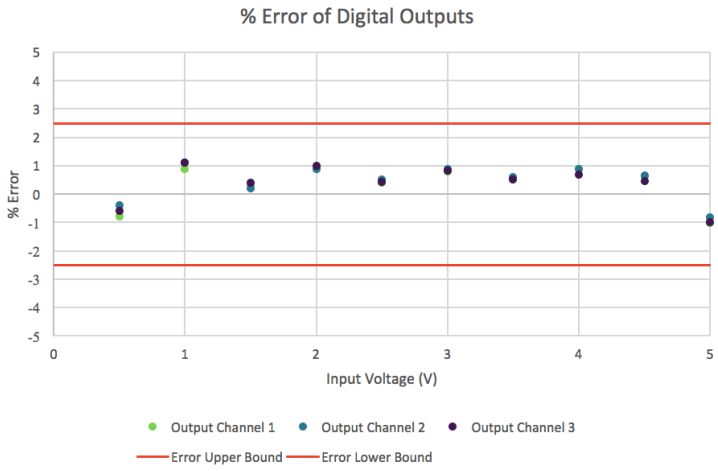


Figure 6.28. % Error of Digital Outputs

Figure 6.28 shows the percent error of the three channel across the output range. While the error is relatively large, this is without calibration. Additionally, the accuracy of the digital outputs isn't a concern.

Figure 6.29 shows the 90%-10% fall time of digital output channel 1. Unfortunately, the specified fall time of 1µs isn't met. Although this isn't a primary concern, a potential fix is identified and detailed in the errata section of the report.

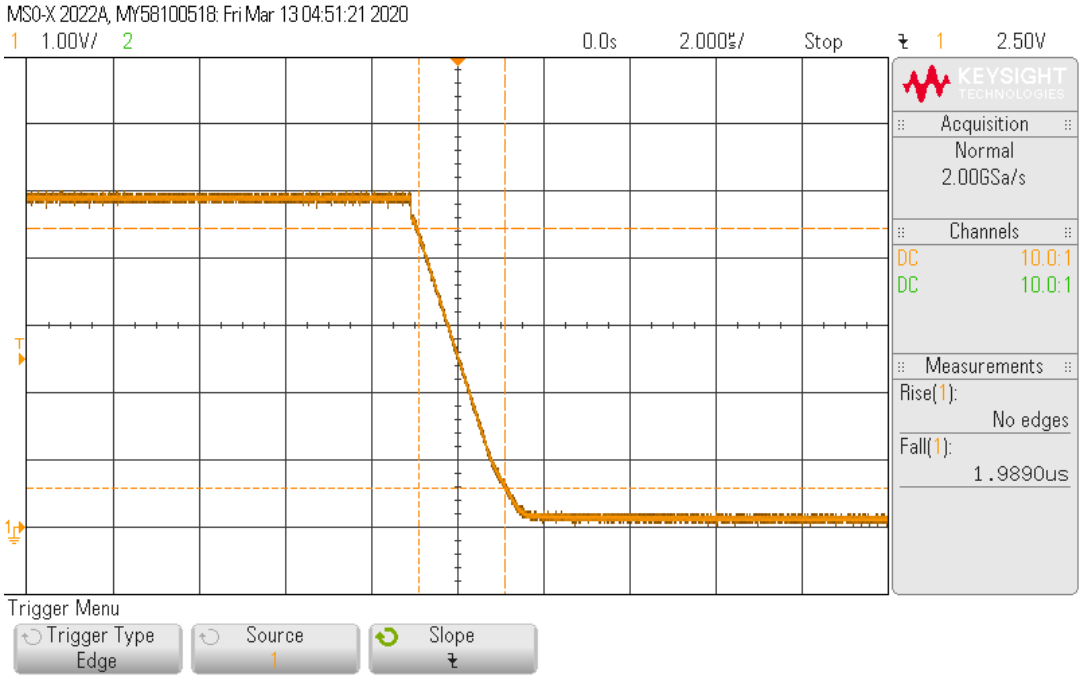


Figure 6.29. Fall time of Digital Output with a load of 2kΩ || 1000pF

6.4.2 Digital Input

Testing the digital inputs is a simple task. A 10kHz $1V_{pp}$ sine wave with a 2.5V is input into a digital input channel. The V_{IL} and V_{IH} are configured to achieve a trip voltage of 2.5V. Figure 6.30 shows the sine wave input and square wave output. The square wave output has roughly 50% duty cycle as expected. Propagation delays of about 7-10µs are seen. These delays are from the filter on the input and the innate propagation delay of the comparator.

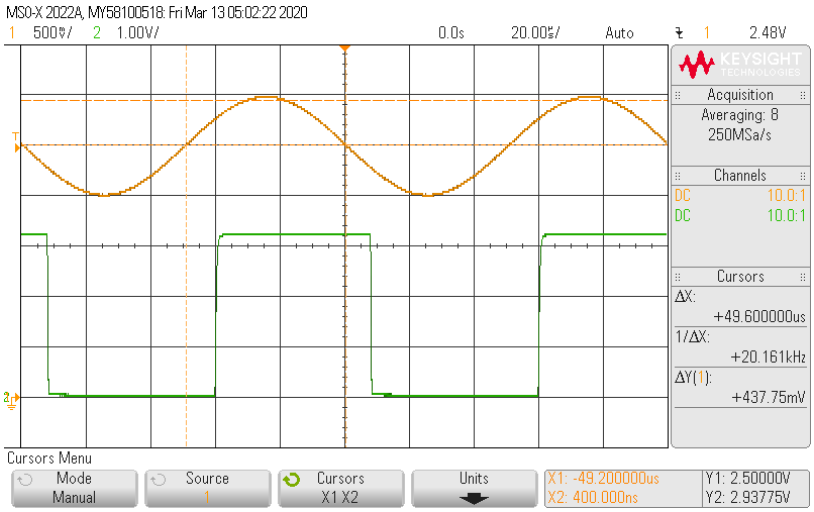


Figure 6.30. Input (Orange) and Output (Green) of Digital Input with V_{trip} set to 2.5V

Figure 6.31 shows the effect of the RC input filter on the digital input. A 5kHz 0-5V square wave input results in a rounded output. The main purpose of the RC filter is to help protect the input from high frequency noise.

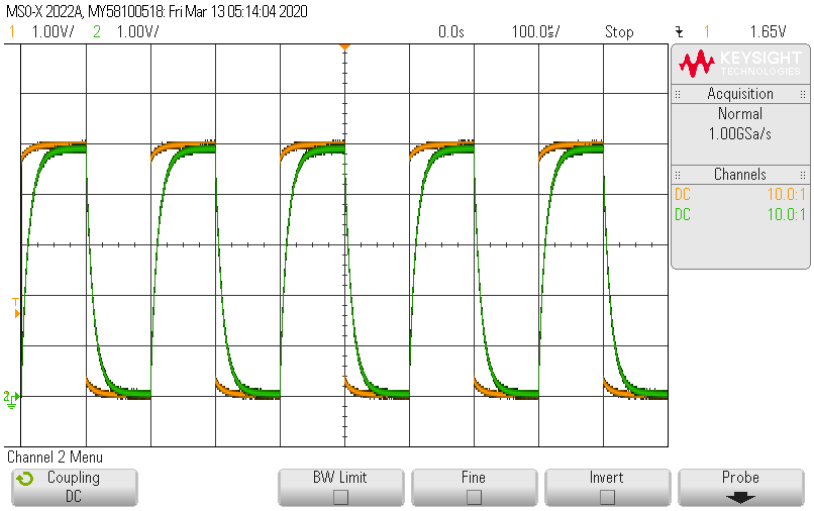


Figure 6.31. Input (Orange) and Output (Green) of Digital Input Filter

Figure 6.32 shows the effect of the overvoltage protection circuit. A 500Hz $10V_{pp}$ sine wave with a 2.5V offset is fed into the digital input. The voltage measured at the comparator input is clamped at -0.8V and 5.8V.

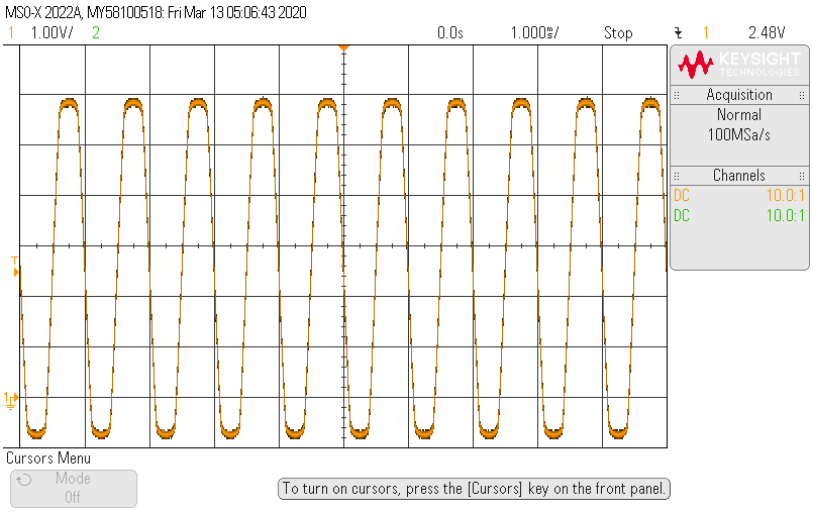


Figure 6.32. Clamped Input

7 Conclusion

> I am somewhat exhausted; I wonder how a battery feels when it pours electricity into a non-conductor?
>
> *Arthur Conan Doyle*

The author (from here on out referred to in the first person) believes this project was a success. Initially I had no clue how I was going to get any of the subsystems working. Through a lot of research, I slowly started to get an idea for the analog inputs and outputs. I went though many revisions based on of the fact that most DACs and ADCs don't interface with the voltages I wanted to allow. I was most afraid of the SMU. The SMU was broken down into different sections. First the current mode worked, and then the voltage mode worked. I built a prototype just to make sure my simulations were working correctly. Once that was verified, the voltage/current limiting was added. This took a painfully long time. I remember seeing a square wave, triangle wave, and sine wave at different nodes of the SMU circuit (after a step input was applied).

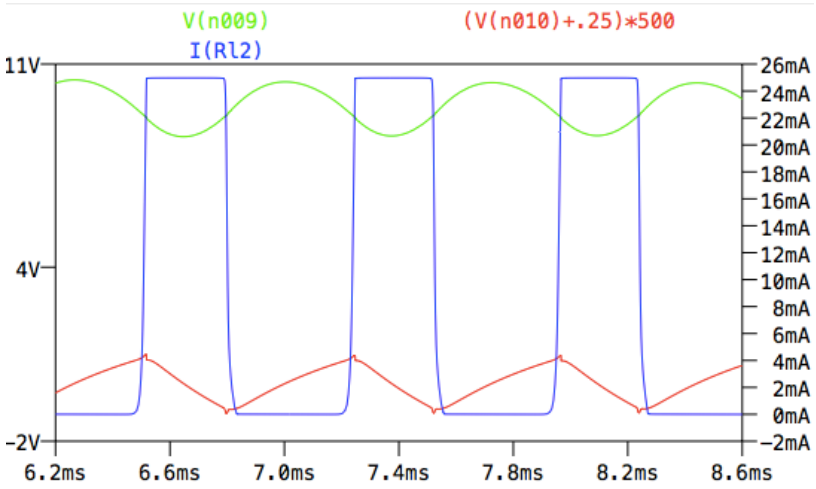


Figure 7.1. How is this even possible

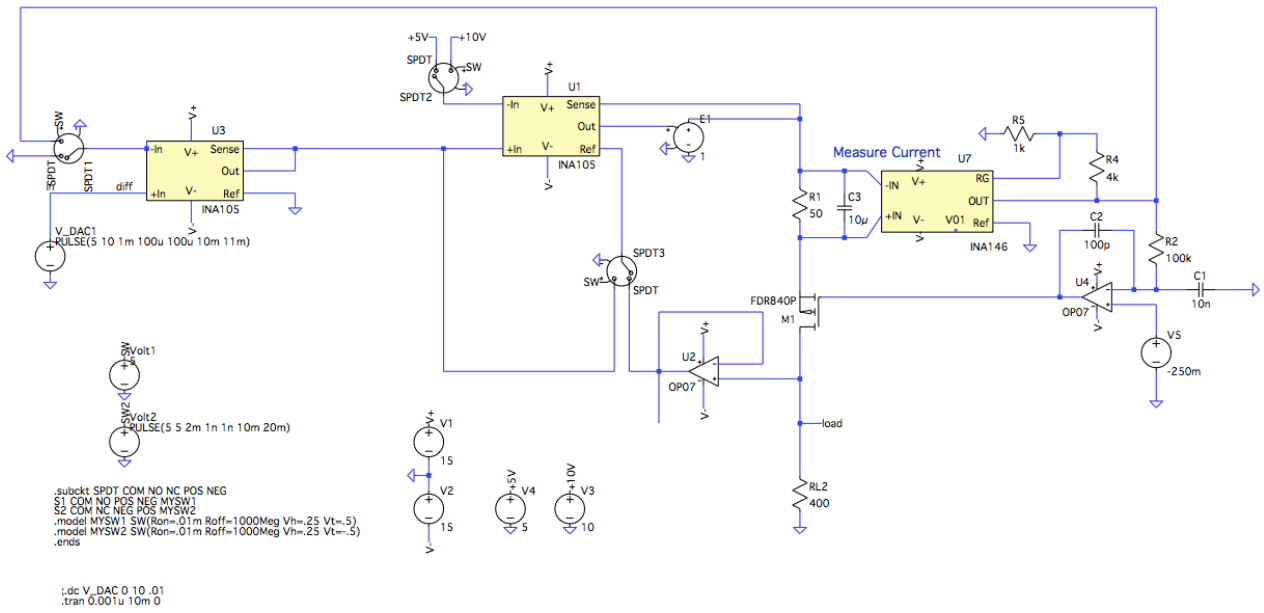


Figure 7.2. Lest anyone want to attempt to tame the Hell Circuit

Fortunately, the power supply was a pleasure to make after the SMU insanity. The board designs were fun to do, as was collecting quotes for the PCB/report. Testing the power supply was the most fun I had with circuits for a long time. Once it was working (which was not trivial in the slightest) I was burning resistors and LEDs just to see the magic smoke pop out without me freaking out for once. I tested the overcurrent protection by licking the leads.

The analog input and outputs were a massive pain to calibrate without automation, but once I did I couldn't believe the accuracy. I remember my phone died so I asked a random person to take a picture of the bench multimeter and my input and output reporting the same voltage down to the 100s of microvolt and better. The AIO section of the AIO/DIO board is what I am most proud of.

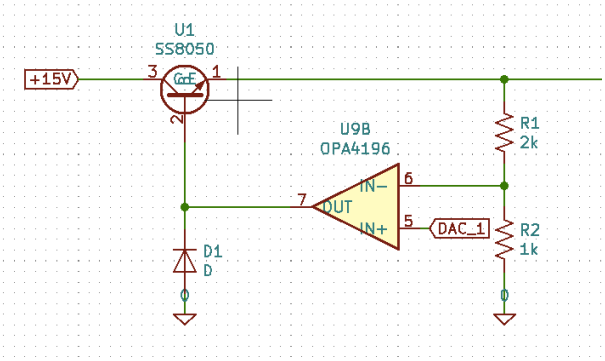
The next big accomplishment was when I finally characterized a BJT diode IV curve. That was a major personal goal of mine. The ECL sweep using the SMU as a constant current source was also a highlight for me. I have the audio recording where I realized it was working and started to freak out. And then I saw one of the output voltages start to increase and my heart drop, that is until I realized it was supposed to do that (see figure 9.7).

8 Errata

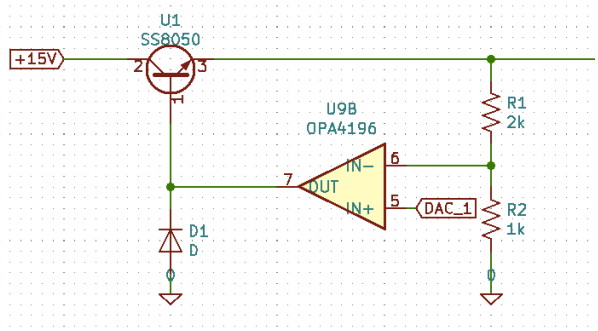
> Look, what do mistakes do but just extend the pleasure of building?
>
> *Adam Savage*

8.1 Power Supply

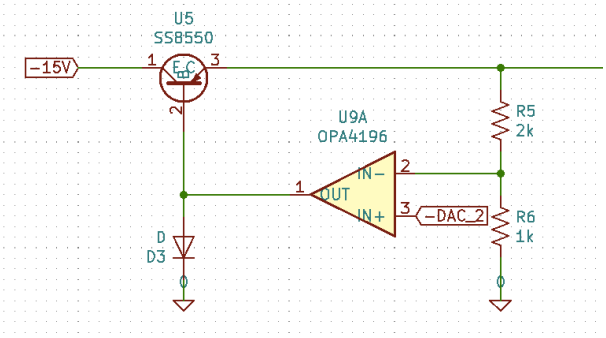
The power supply has one (known) mistake. The pin-out of the NPN/PNP is incorrect. The library symbol had a pinout commonly used by the TO-92 package. The actual package used is the TO-220, chosen for better power dissipation. The TO-92 symbol used had a pinout of E-B-C (C-B-E for PNP), while the TO-220 part ordered has a pinout of B-C-E. Figure 8.1 shows the incorrect schematic in 8.1a and 8.1c and the corrected version in 8.1b and 8.1d.



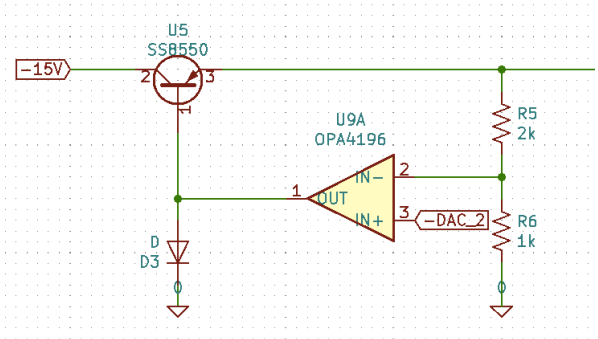
(a) Incorrect Pinout for NPN Transistor



(b) Correct Pinout for NPN Transistor



(c) Incorrect Pinout for PNP Transistor



(d) Correct Pinout for PNP Transistor

Figure 8.1. Schematic of Power Supply Showing Error and Correction

Power Supply Revision B corrects the issue. The author opts to bend the transistor leads to the correct orientation over ordering a entirely new PCB. Figure 8.2 shows the bent leads. The author refers to this shape as an aesthetically pleasing coalescence of the old (Romans) and the new (Transistors). The Museum of Modern Art has not returned the author's calls.

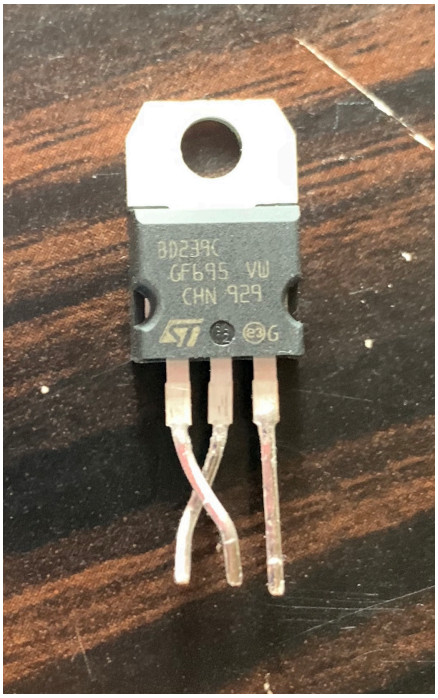


Figure 8.2. Roman Numeral Realization in Hardware

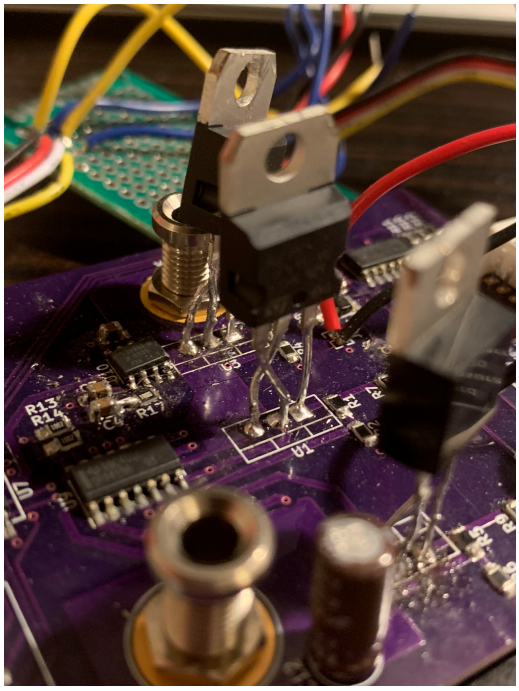


Figure 8.3. Corrected Pinout with Bent Leads

8.2 SMU

The SMU revision C schematic contains (quite) a few errors. The DAC used for the voltage control is powered with a 5V reference voltage. However, the internal 2.5V reference is used as it's reference. The author forgot that this would limit the DAC output to 2.5V. A simple fix is to double the gain/half the attenuation in the voltage conditioning circuits. Table **??** shows resistors with changed values.

Another issue with the SMU is with the coarse fine control. As the maximum voltage produced from the coarse control is 10V, any resistor tolerances/DAC max output error may reduce the actual voltage. The SMU in current mode is relatively sensitive to voltage errors; with an offset of just 10mV results in a current error of 10mA. To remedy this, the resistors are modified slightly in order to allow for some slack. This slack means that the fine/coarse outputs produces larger voltage swings than needed. This, along with calibration, compensates for any tolerance/DAC errors. Table 8.1 shows resistors modifications made during testing. Figure 8.4 shows the DAC voltage conditioning circuits in Revision D.

Table 8.1. Resistor Changes Made to SMU Rev C

Resistor	Previous Value	New Value
R9	10kΩ	5kΩ
R12	20kΩ	10kΩ
R13	20kΩ	15kΩ
R16	10kΩ	5kΩ
R20	50kΩ	10kΩ

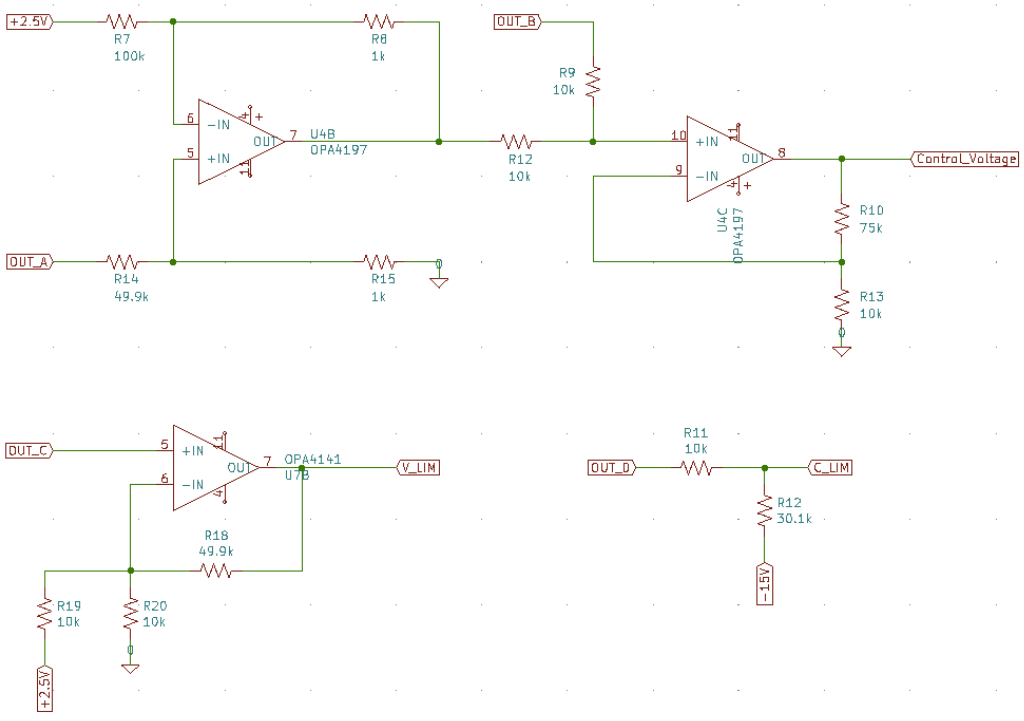
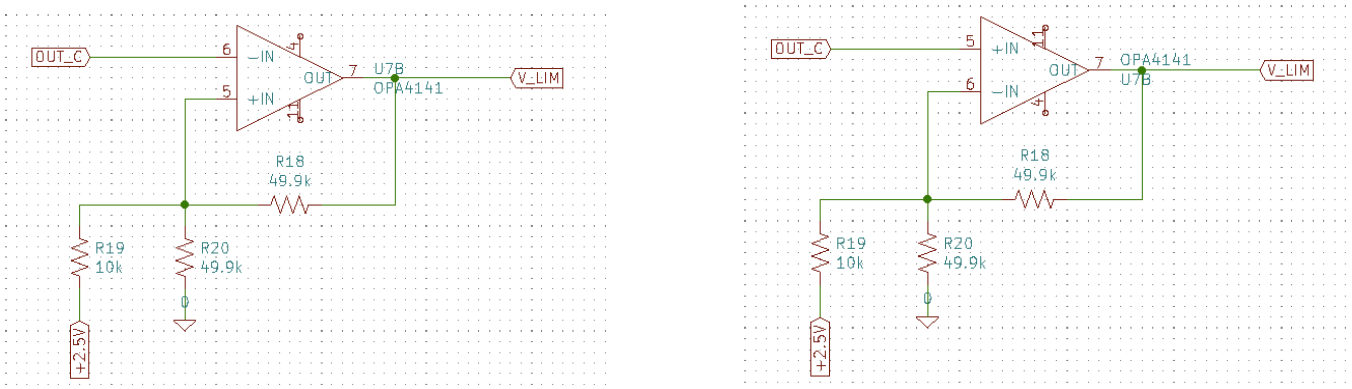


Figure 8.4. Modified Fine/Coarse Control and Voltage Conditioning Circuits

The op-amp used for the voltage limit has it's input terminals swapped. Figure 8.5 show the incorrect and correct configurations.

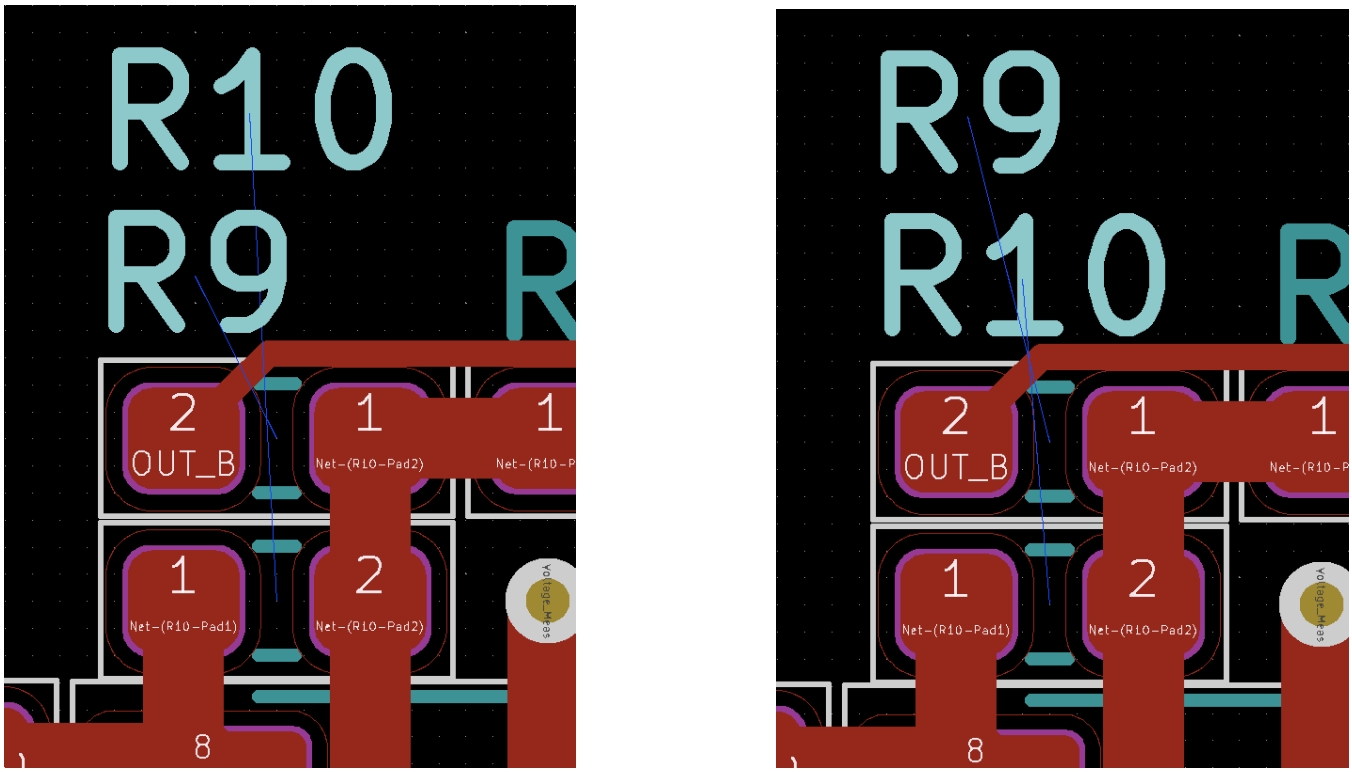


(a) Incorrect Input Terminals

(b) Correct Input Terminals

Figure 8.5. A Fun Game of Spot the Difference

There are a few silkscreen mistakes throughout the project. However, most of the mistakes are minor; only affecting the legibility of the designator. Figure 8.6a shows the one instance of an incorrect designator. The R9 and R10 silkscreen locations are swapped. In figure 8.6b the R9 designator correctly refers to the upper resistor.



(a) Incorrect Reference Designator

(b) Correct Reference Designator

Figure 8.6. Switcharoo Attended To

From the OPA633 datasheet:

"Pin 6 connects to the substrate of the integrated circuit and should be connected to ground. In principle it could also be connected to +VS or –VS, but ground is preferable." 27

In revision C, pin 6 of the OPA633 is connected to $-V_S$. In revision D, this connection is changed to GND.

8.3 AIO

Due to resistor tolerance, the output voltage can not reach the full scale output endpoints. The gain of the analog output is too low. A fix to this problem is to use resistor values that give gain above 2. Another more involved fix is measuring the exact resistor values and placing them to ensure the gain is greater than 2. The probability of a gain less than 2 occurring is 50%. This would be devastating in a production environment and revisal is imperative. This problem is less likely to occur in the ±10V outputs as the resistors set the ideal gain to 4.02. When worst case tolerances are taken into account, the gain of the output is 3.96, less than 4. A MATLAB script finds the probability of the actual gain is less than 4 when 1% tolerance resistors are used.

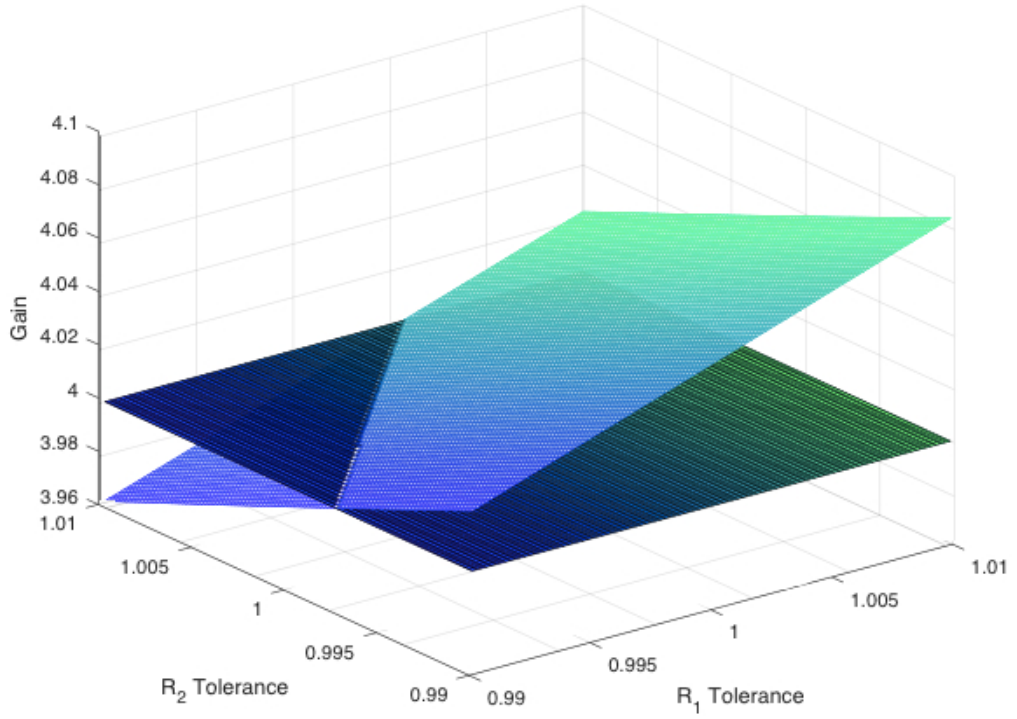


Figure 8.7. Gain as a Function of 2 Resistor Tolerance Ranges

Figure 8.7 shows two intersecting planes. The darker flat plane is a constant gain of 4. The lighter tilted plane is the gain achieved for two given resistors anywhere from ±1% tolerance. The top right corner, for example, is the gain if the value of R_1 is 1% higher than nomnial and the value of R_2 is 1% lower than nominal. This point results in the largest gain. If the lighter plane passes beneath the darker plane, a gain less than 4 results. The MATLAB code below calculates the probability of a less than 4 gain if resistor tolerances are uniformly distributed

```
% 1% tolerance resistors used
tol = meshgrid(linspace(0.99, 1.01), linspace(0.99, 1.01));

% generate grid of all resistance combinations
R1 = 40.2 .* tol;
R2 = 13.3 .* tol;

% find gain of each resistor combo
gain = (1 + R1./R2');

% generate grid equal to 4
cutoff(1:100,1:100) = 4;

% plot surfaces
mesh(gain, tol)
hold on
surf(cutoff, tol)

% find gains less than 4
L = logical(gain < 4);

% add up gains less than 4 and find occurrence probability
(sum(sum(L)) / (length(L))^2) * 100
```

The probability of a gain less than 4 occurring under uniform distribution is 19.74%. If the resistor values follow a gaussian distribution with = 2.5, there is only an 8.4% chance. If anyone emulates this project, the author recommends adjusting the resistor sizing, which prevents these issues. The culprit resistors are R1 though R8 on the AIO/DIO Board.

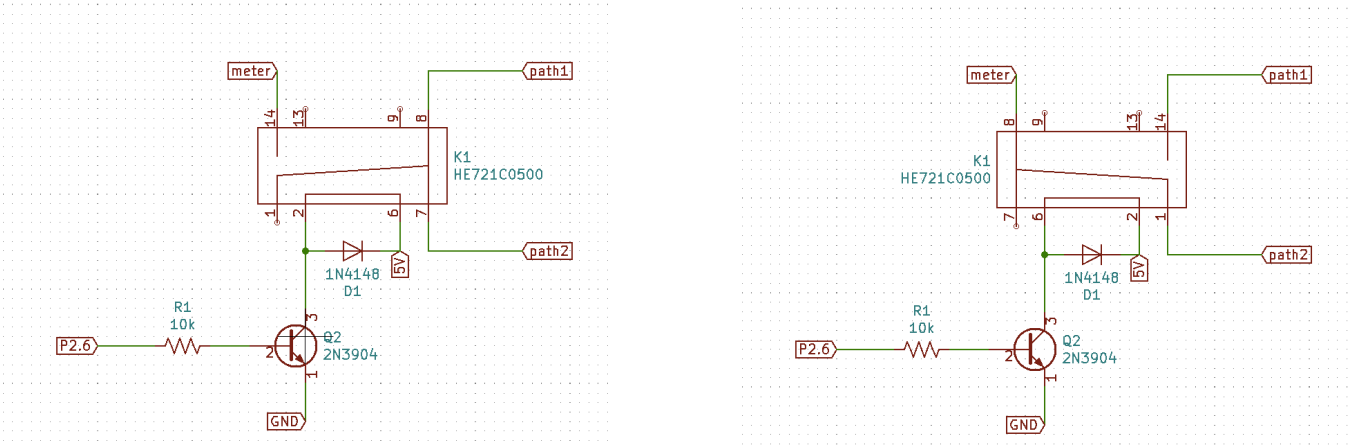
8.4 DIO

The digital output circuit did not meet the spec'd rise/fall time of 1µs (with load of 2000kΩ || 1000pF). While this doesn't concern the author in the slightest, the problem is analyzed.

The TLC3544 has a 11ns typical rise/fall time when configured with unity gain for a 2V input step 28. The isolation resistor of 20Ω forms a low-pass circuit with the load capacitance. However the time constant set by the RC values is 20ns. These factors should result in rise/fall times of less than 100ns. The author is not sure why the rise/fall times are an order of magnitude too slow.

8.5 µC Board

The linear regulator ordered is incorrect. An adjustable output component was ordered instead of a 5V variant. feedback resistors set the output voltage to approximately 5V.



(a) Incorrect Orientation

(b) Correct Orientation

Figure 8.8. The Results of Two Hours of Soldering

The relays on the µC board are flipped. Figure 8.8 shows the schematic fix.

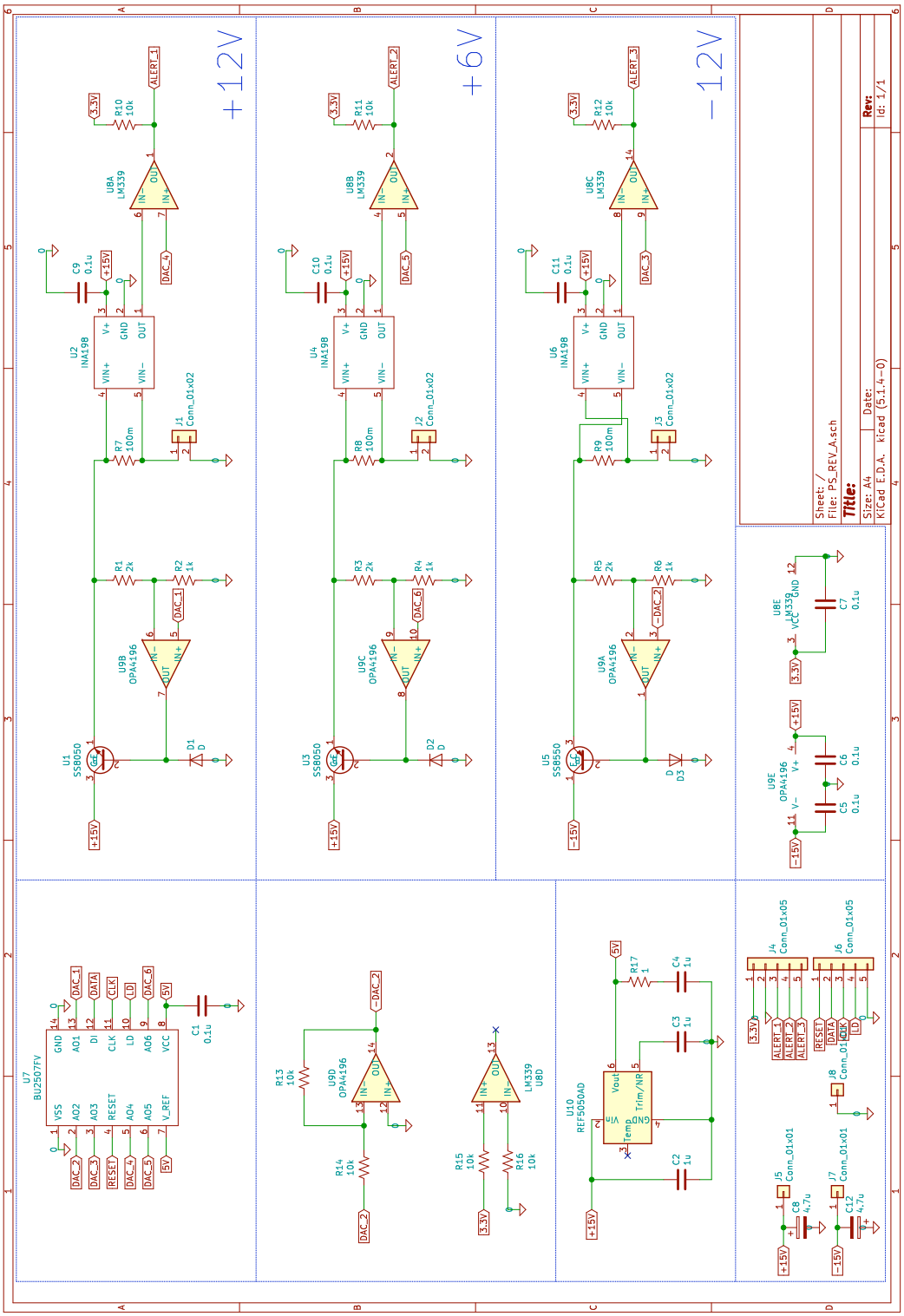
Pin 3.6 instead of Pin 3.7 is supposed to connect to the power supply TX. Revision B fixes this.

9 Appendices

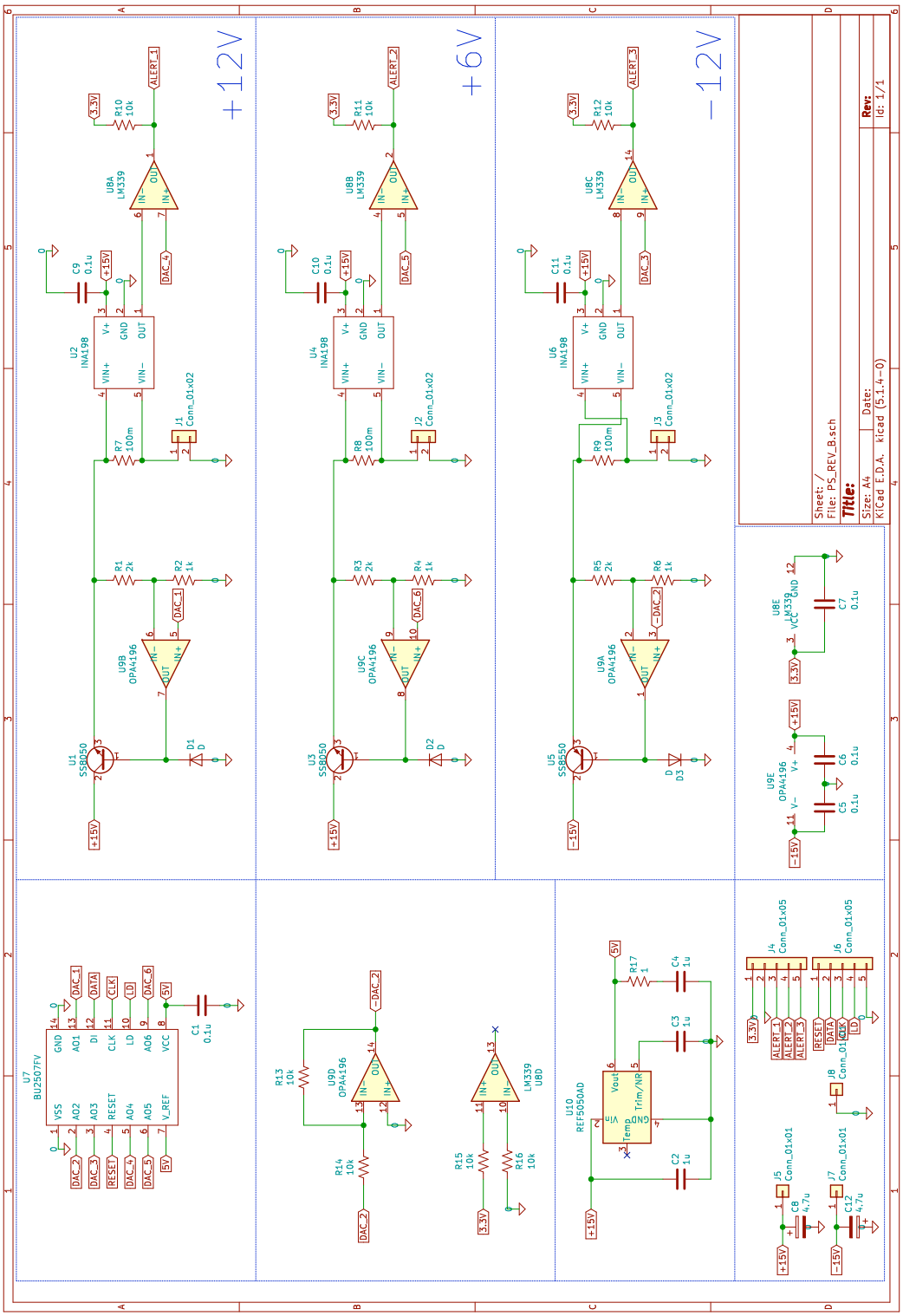
> People think that mathematics is complicated. Mathematics is the simple bit, it's the stuff we CAN understand.
> It's cats that are complicated.
>
> *John Conway*

9.1 Schematics

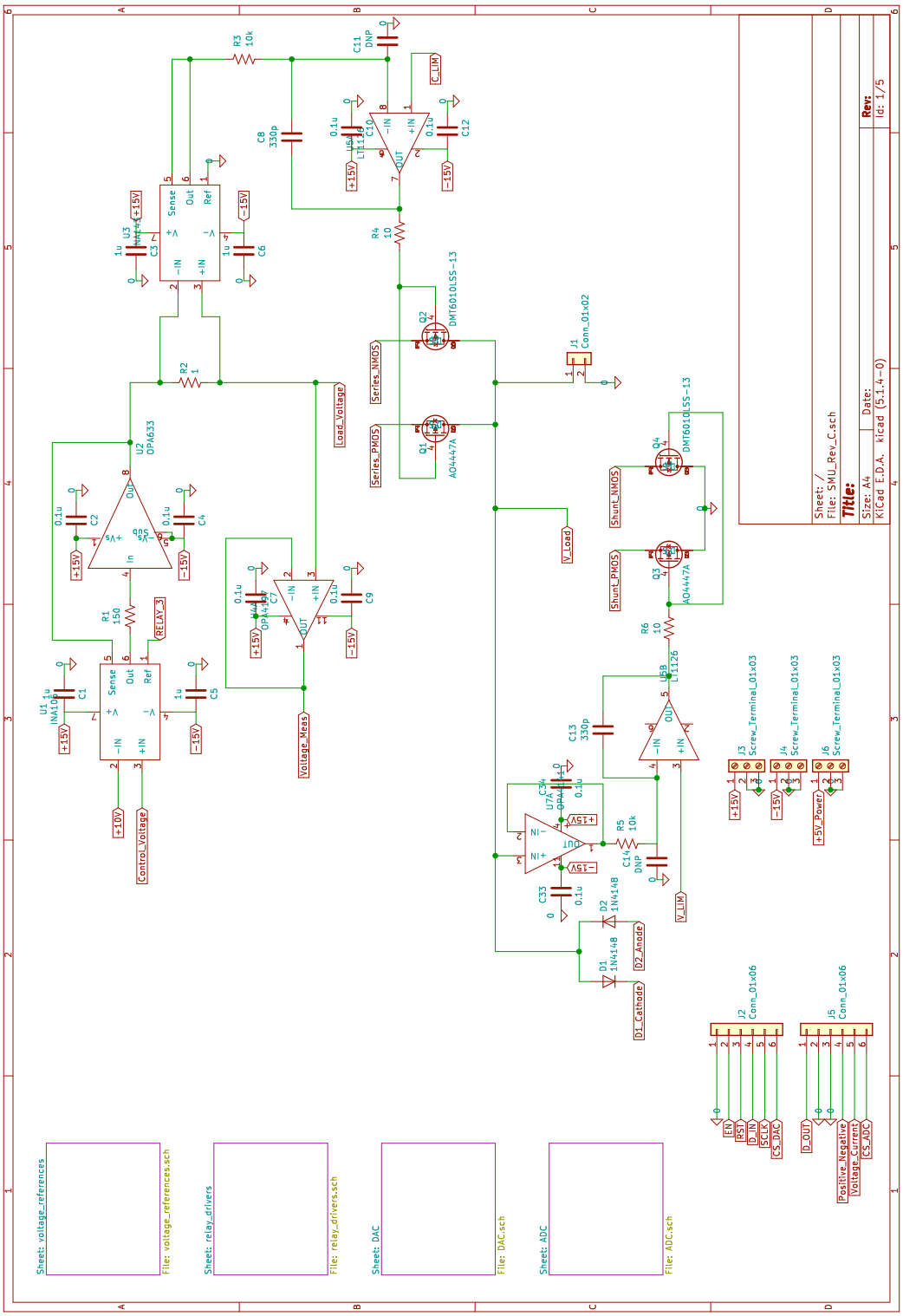
9.1.1 Power Supply Revision A

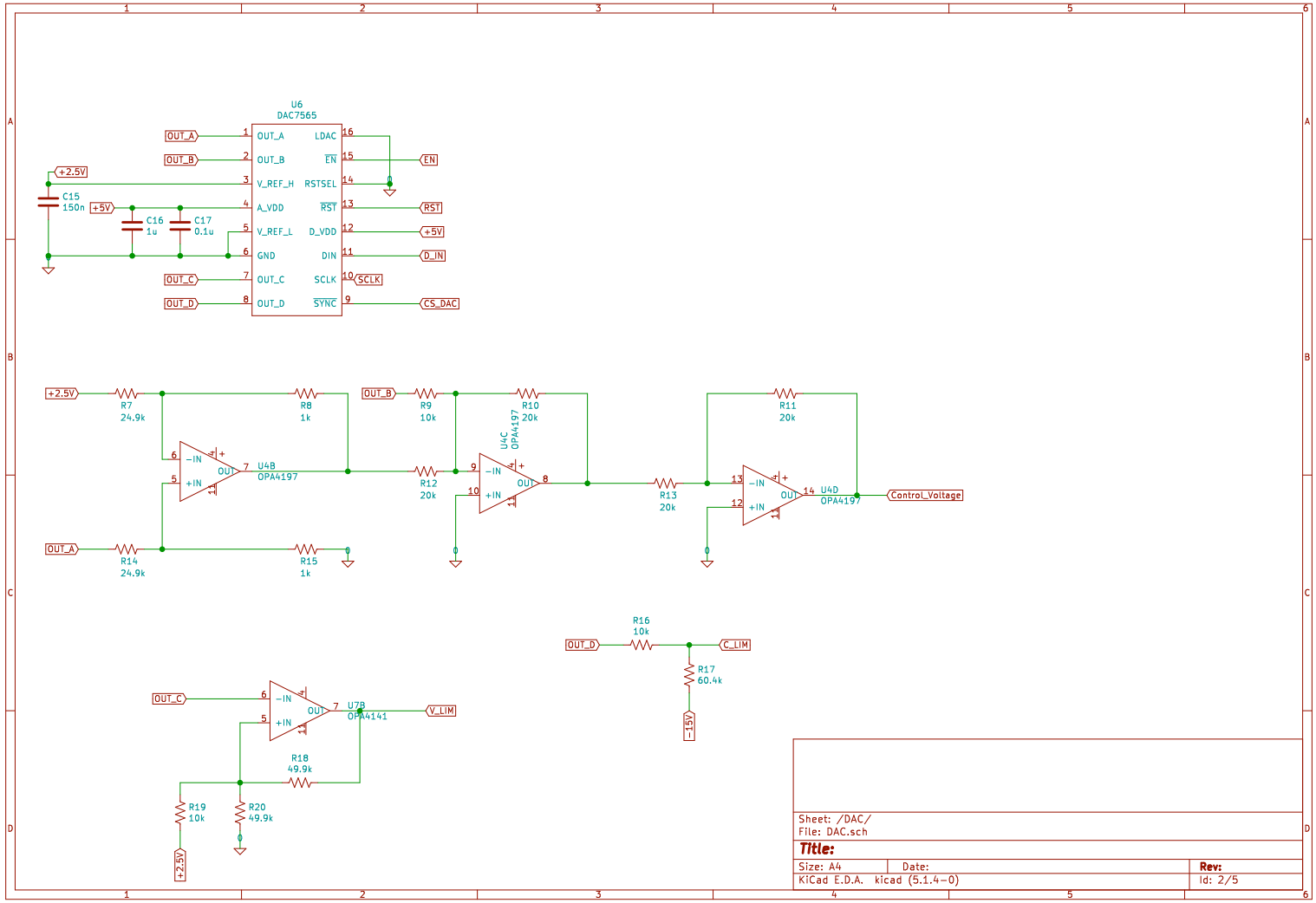


9.1.2 Power Supply Revision B



9.1.3 SMU Revision C

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OUT_B
V_REF_H
A_VDD
V_REF_L
GND
OUT_C
OUT_D
LDAC
EN
RSTSEL
RST
D_VDD
DIN
SCLK
SYNC
+2.5V
+5V
C15
150n
C16
1u
C17
0.1u
EN
RST
+5V
D_IN
SCLK
CS_DAC
R7
24.9k
R8
1k
U4B
OPA4197
R9
10k
R10
20k
U4C
OPA4197
R11
20k
R12
20k
R13
20k
U4D
OPA4197
Control_Voltage
R14
24.9k
R15
1k
R16
10k
C_LIM
R17
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-15V
U7B
OPA4141
V_LIM
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R19
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R20
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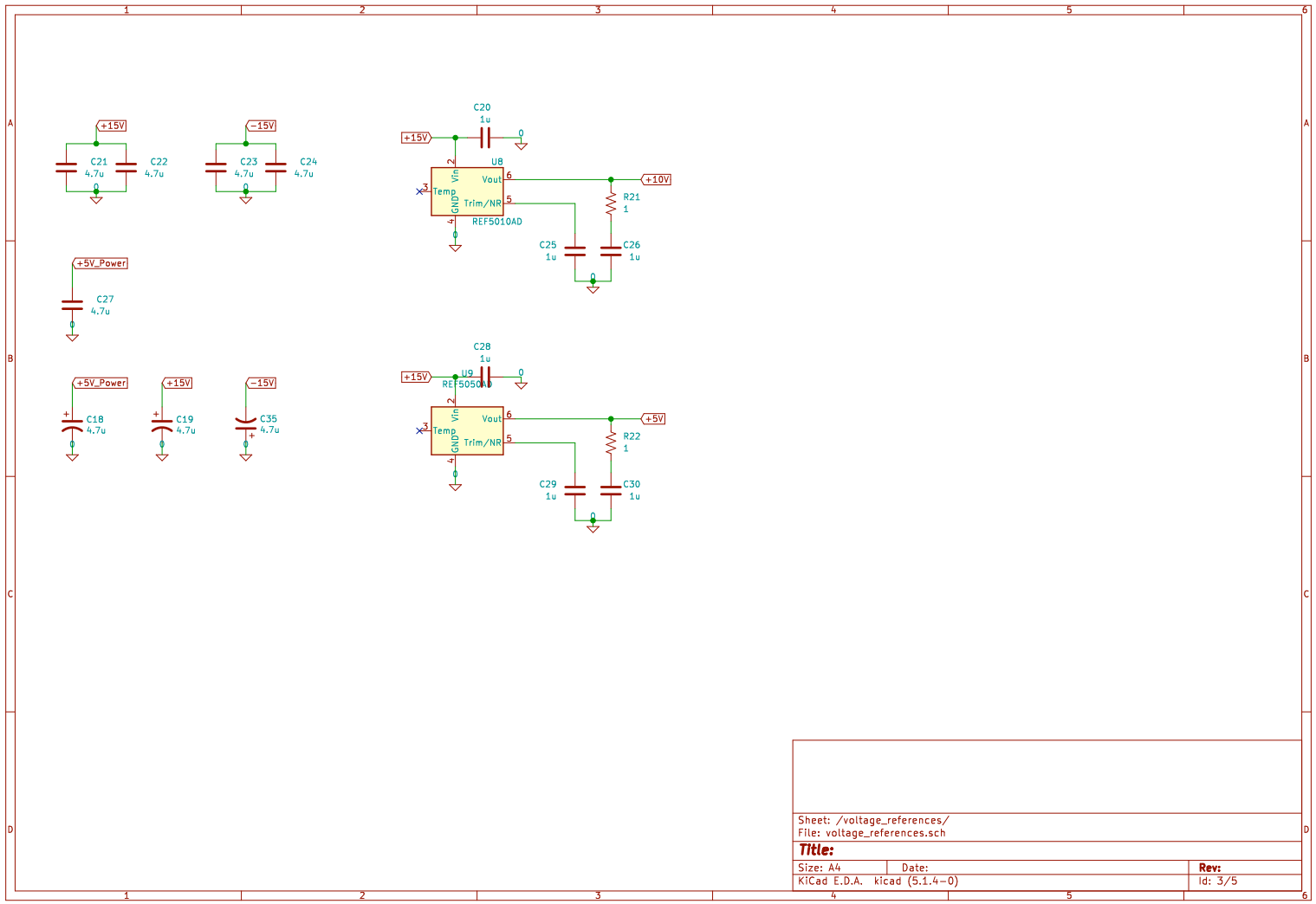
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C22
4.7u
-15V
C23
4.7u
C24
4.7u
C20
1u
U8
Vin
Temp
GND
Vout
Trim/NR
REF5010AD
+10V
R21
1
C25
1u
C26
1u
+5V_Power
C27
4.7u
C28
1u
U9
REF5050AD
+5V
R22
1
C29
1u
C30
1u
C18
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C19
4.7u
C35
4.7u
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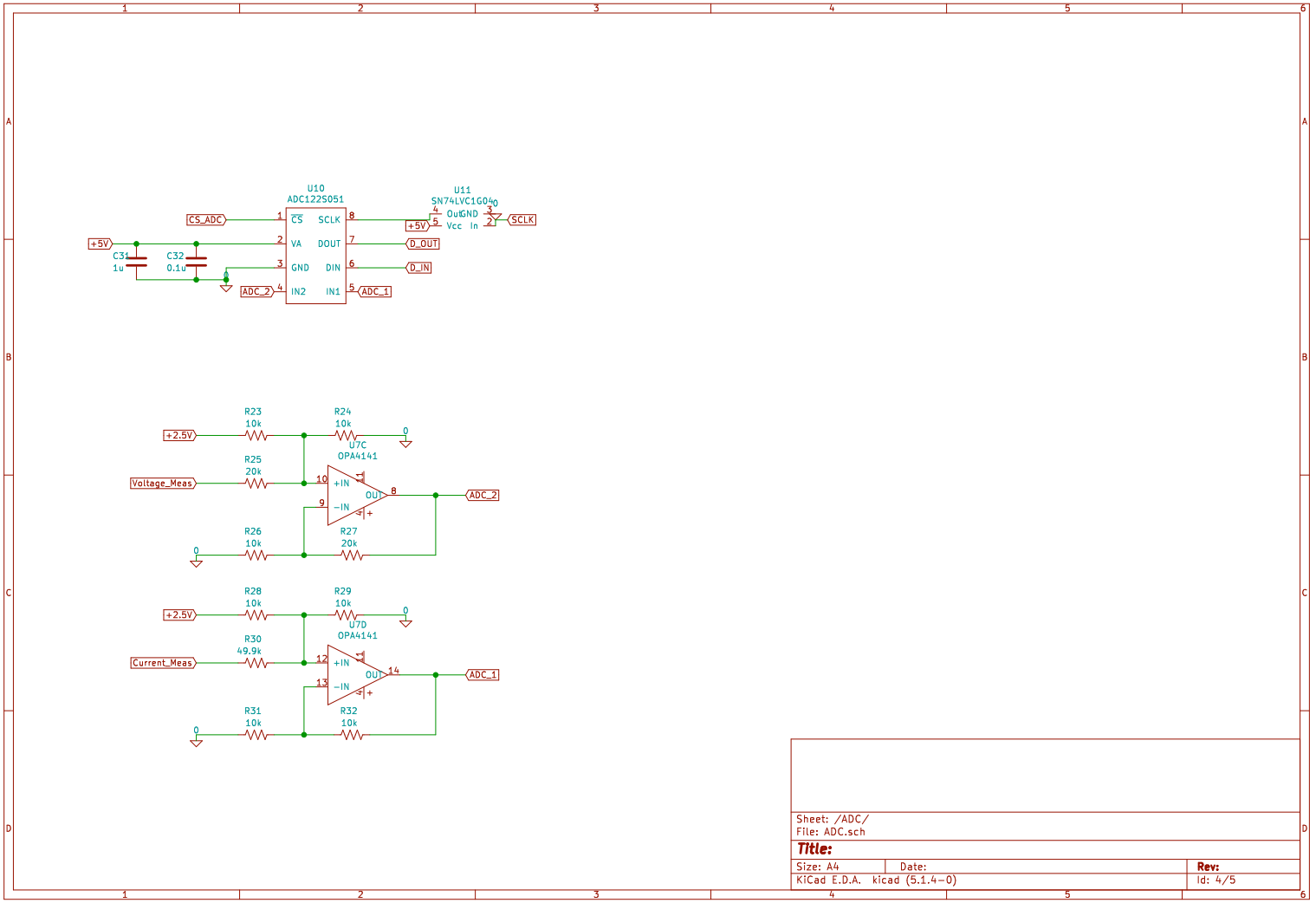
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U11
SN74LVC1G04
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SCLK
D_OUT
D_IN
ADC_2
ADC_1
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C32
0.1u
R23
10k
R24
10k
U7C
OPA4141
+2.5V
R25
20k
Voltage_Meas
R26
10k
R27
20k
R28
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R29
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U7D
OPA4141
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R32
10k
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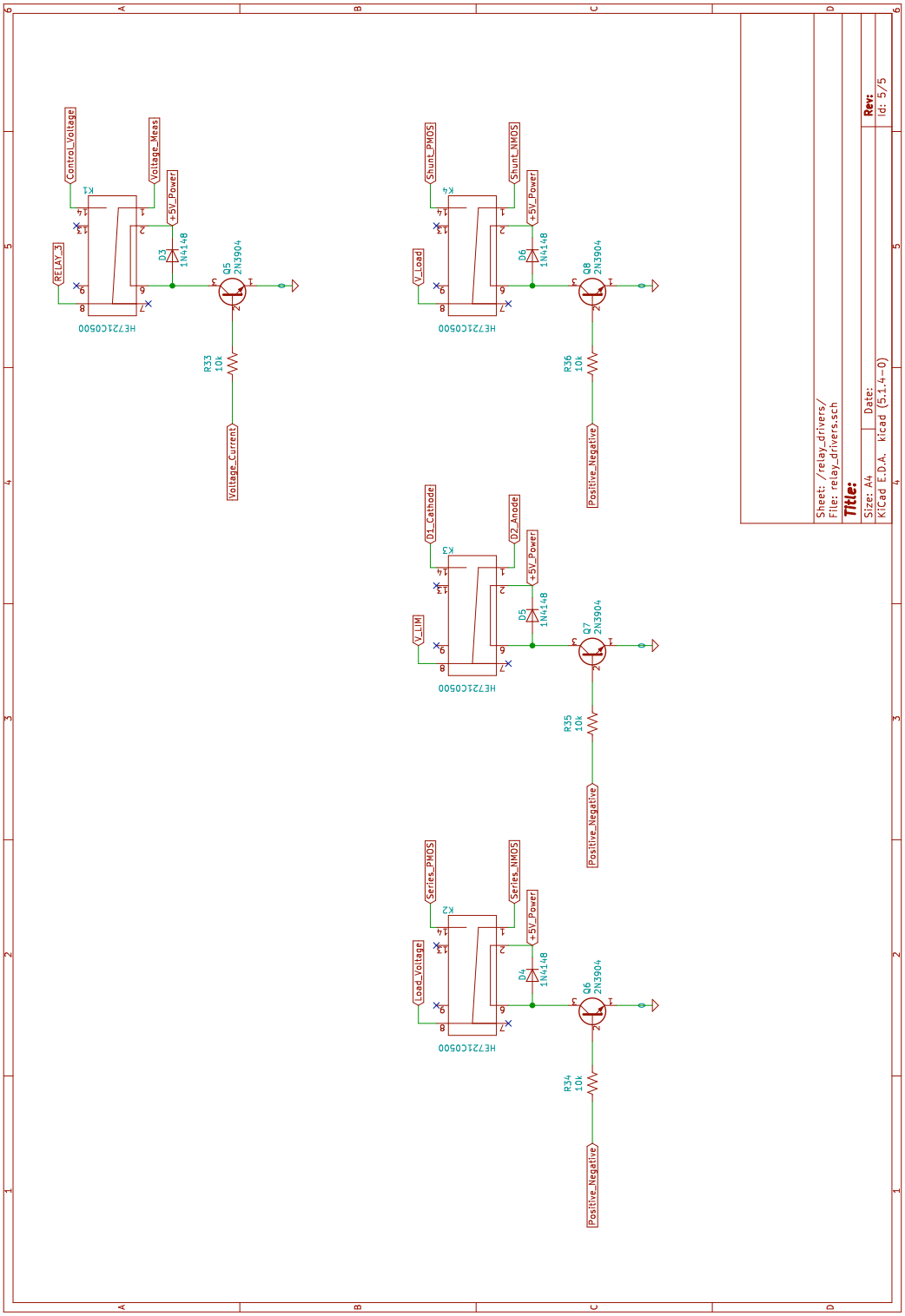
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Q5
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Voltage_Current
Shunt_PMOS
Shunt_NMOS
V_Load
D6
Q8
R36
10k
Positive_Negative
D1_Cathode
D2_Anode
V_LIM
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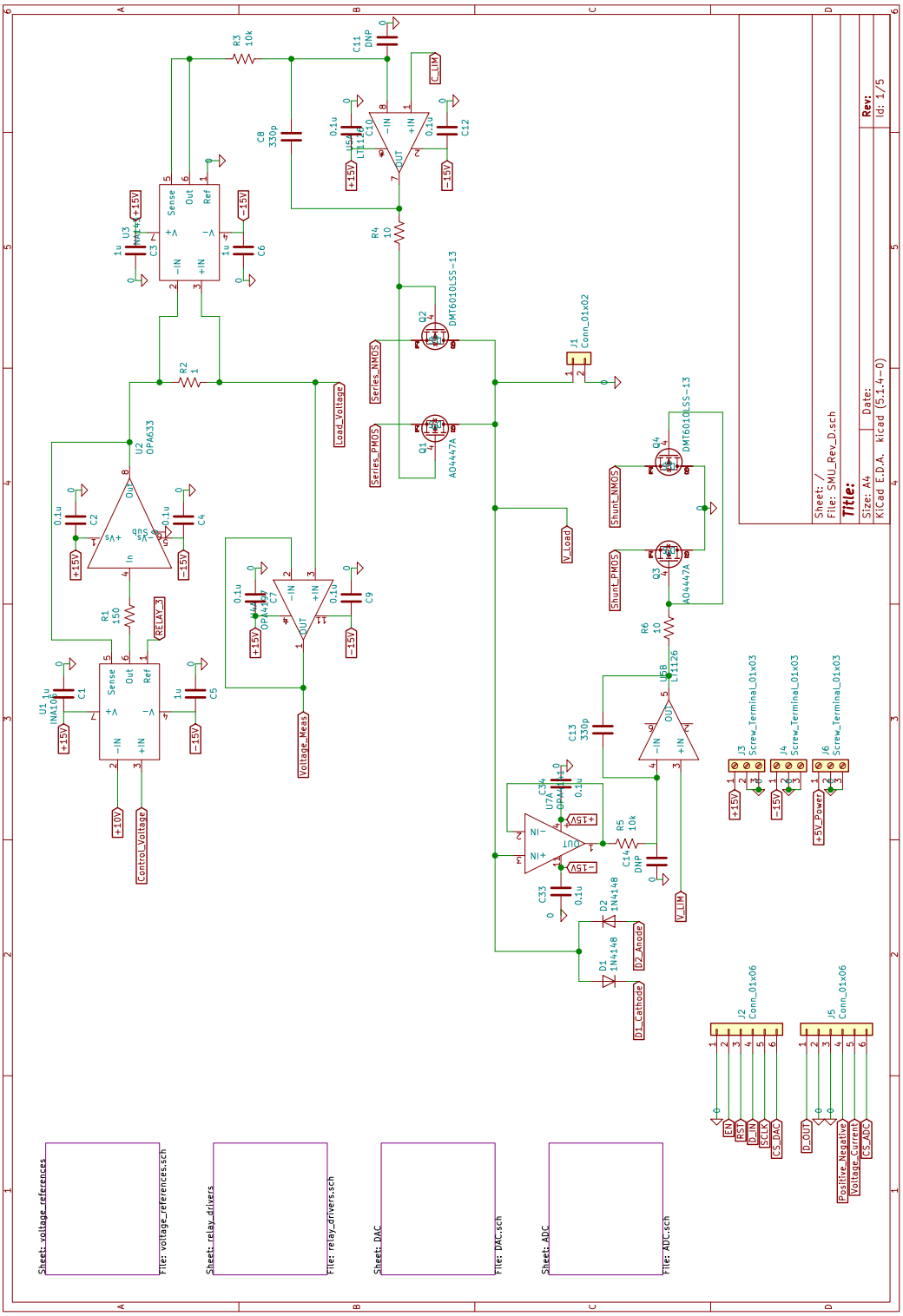
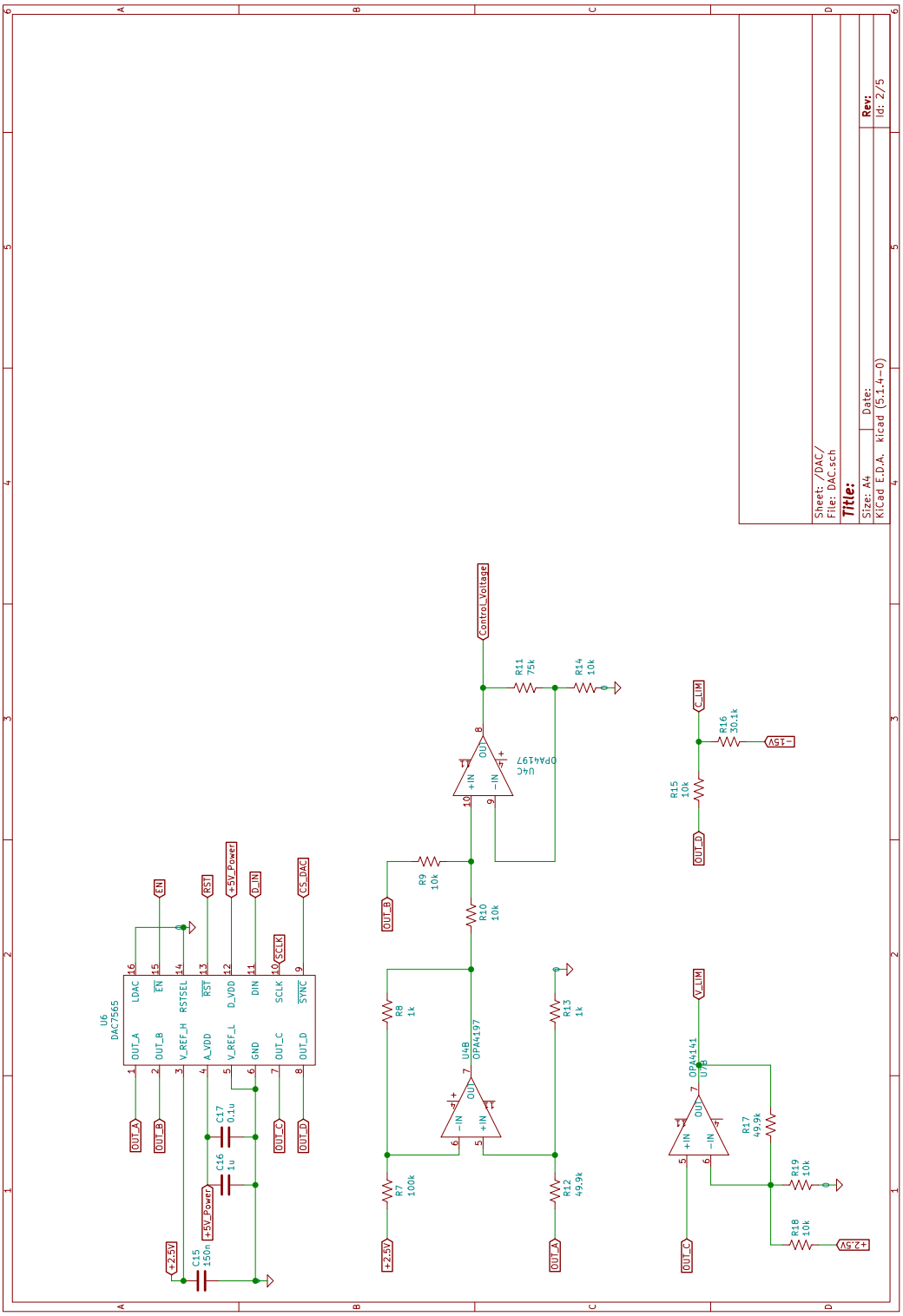
9.1.4 SMU Revision D

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RSTSEL
RST
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DIN
SCLK
SYNC
OUT_A
OUT_B
V_REF_H
A_VDD
V_REF_L
GND
OUT_C
OUT_D
EN
RST
+5V_Power
D_IN
SCLK
CS_DAC
C17
0.1u
C16
1u
C15
150n
+2.5V
+5V_Power
Control_Voltage
R11
75k
R14
10k
U4C
OPA4197
R9
10k
R10
10k
R8
1k
U4B
OPA4197
R13
1k
R7
100k
R12
49.9k
OUT_B
OUT_A
C_LIM
R16
30.1k
-15V
R15
10k
OUT_D
V_LIM
U7B
OPA4141
R17
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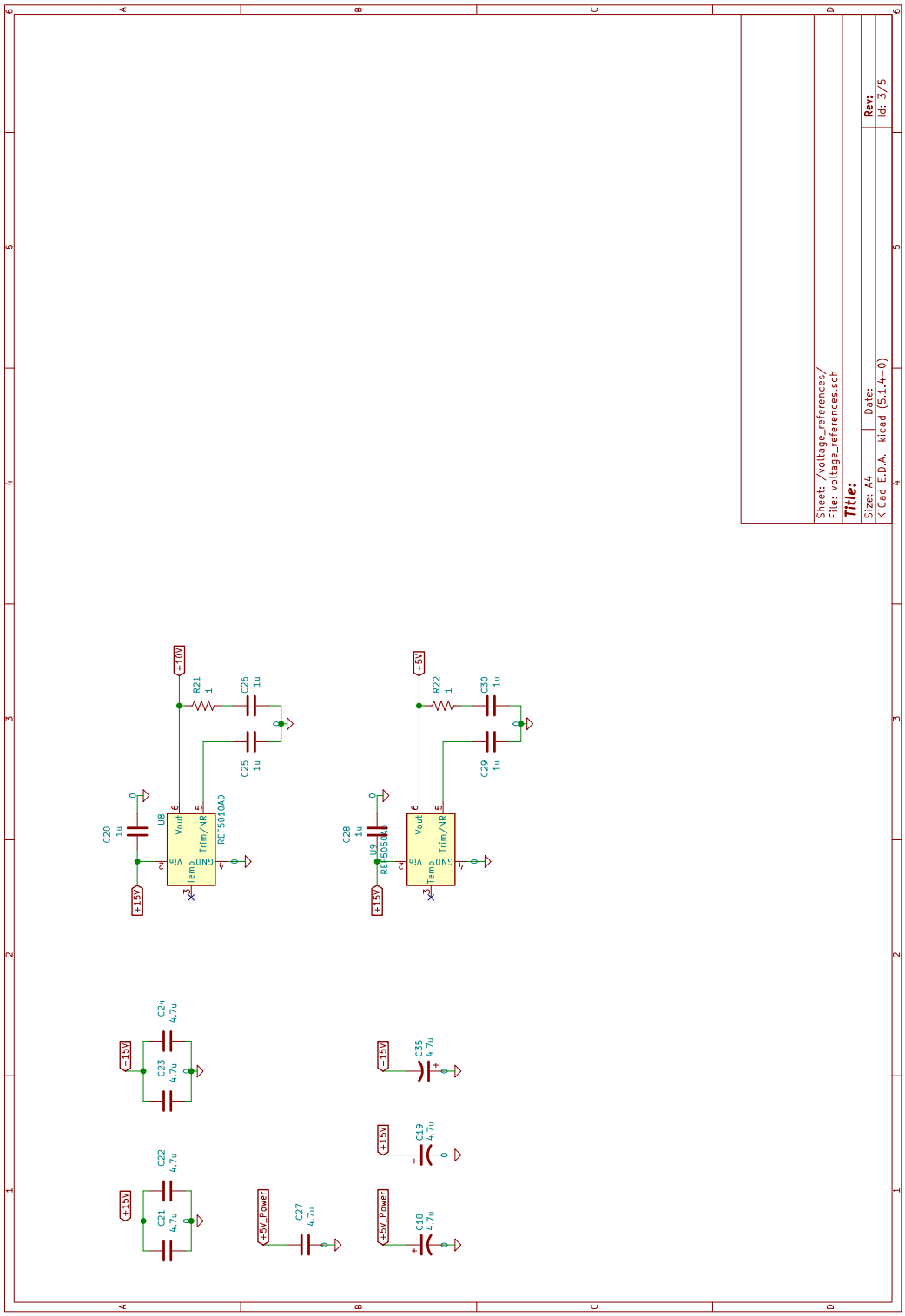
R19
10k
R18
10k
+2.5V
OUT_C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C26
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C25
1u
C20
1u
U8
Vout
Trim/NR
Vin
Temp
GND
REF5010AD
+15V
+5V
R22
1
C30
1u
C29
1u
C28
1u
U9
REF5050AD
C24
4,7u
C23
4,7u
C22
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4,7u
C18
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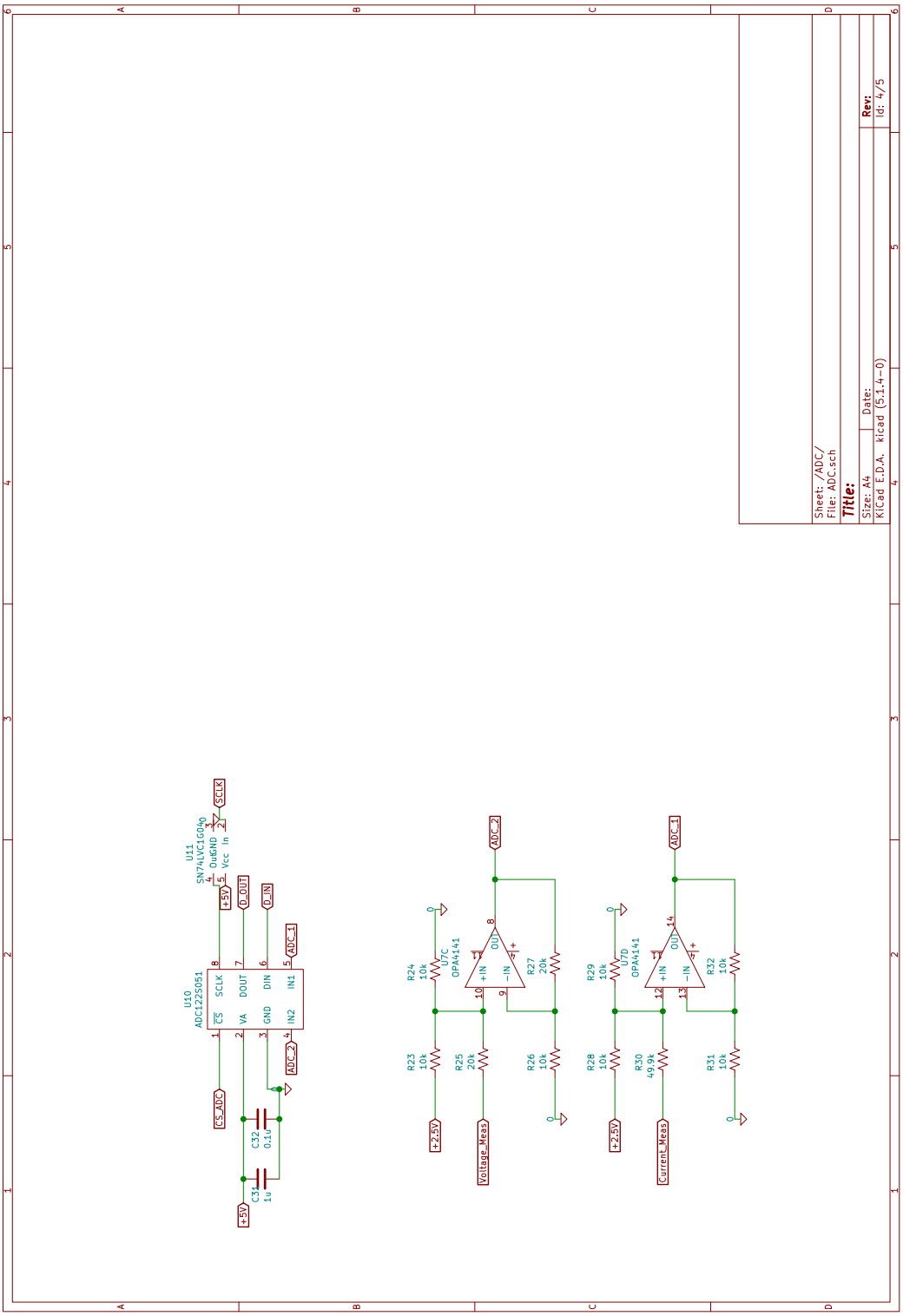
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SN74LVC1G04
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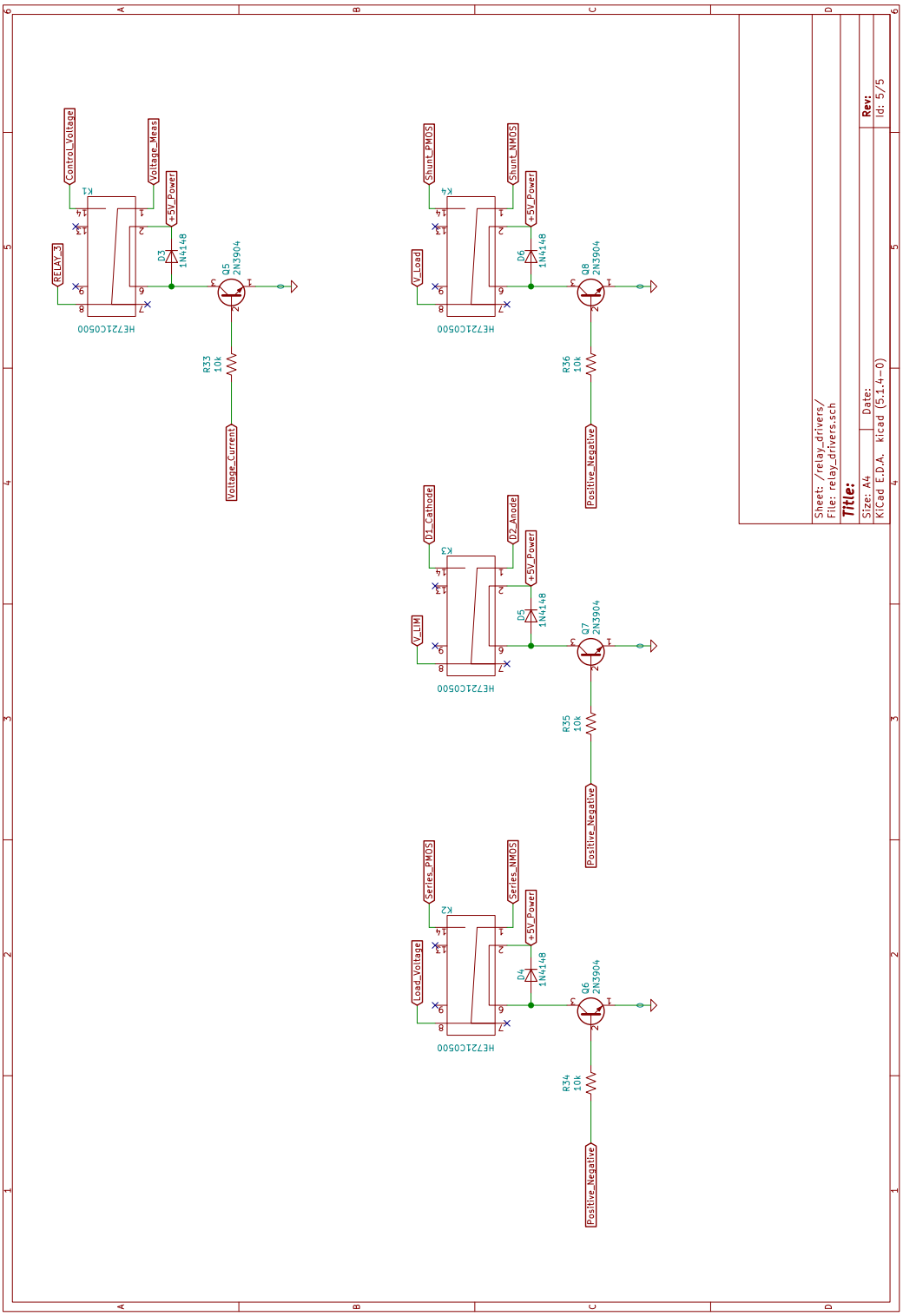
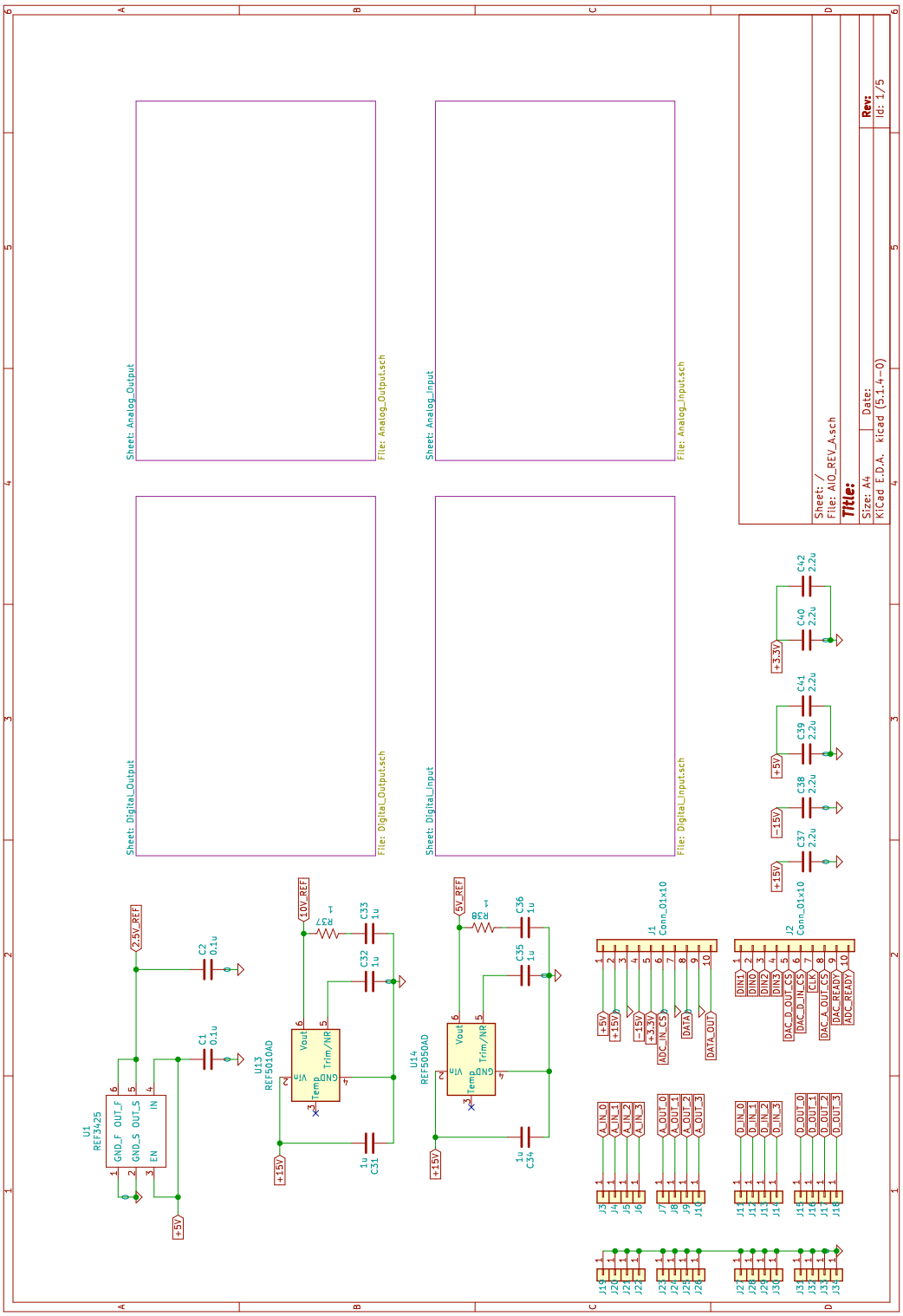
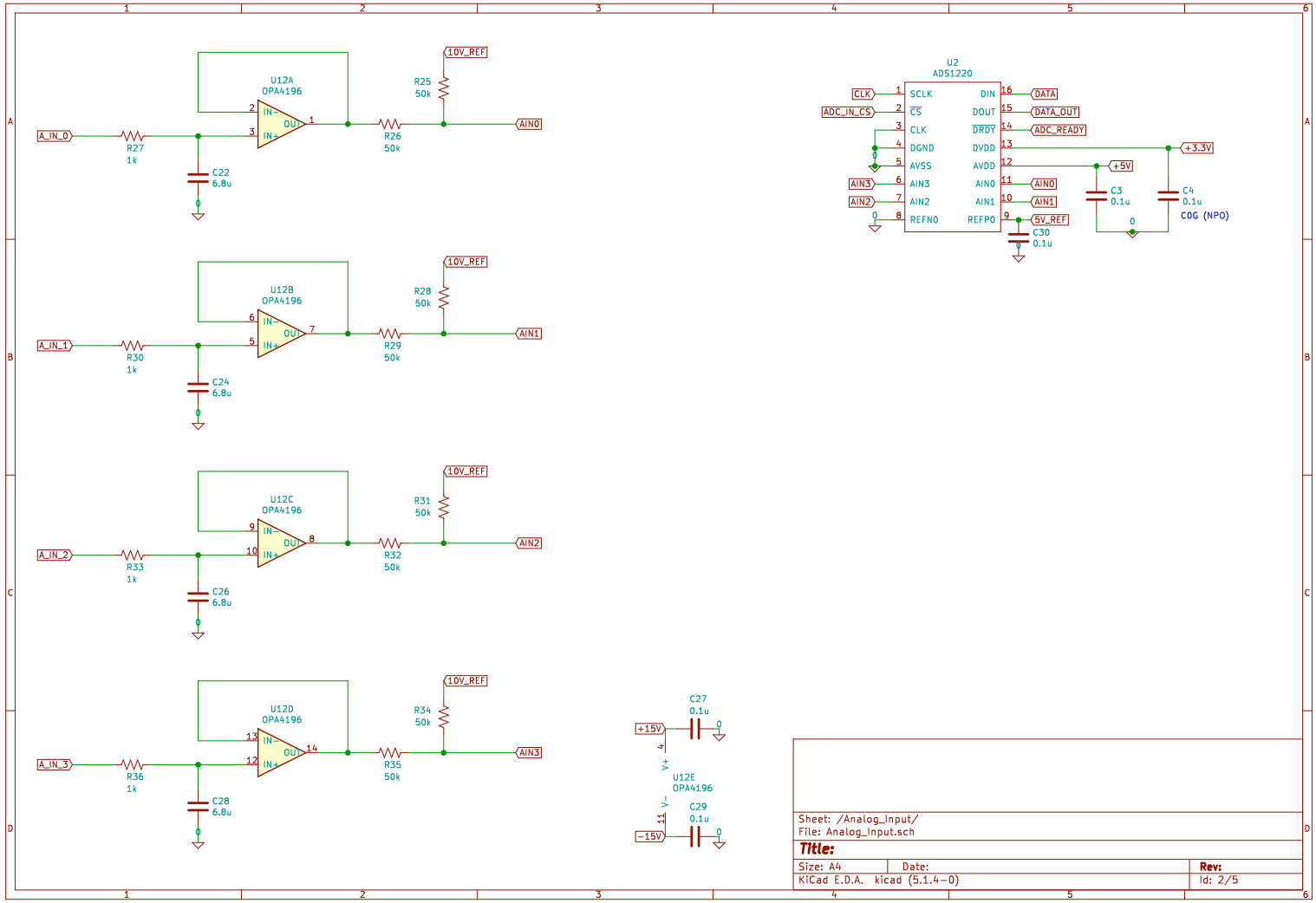
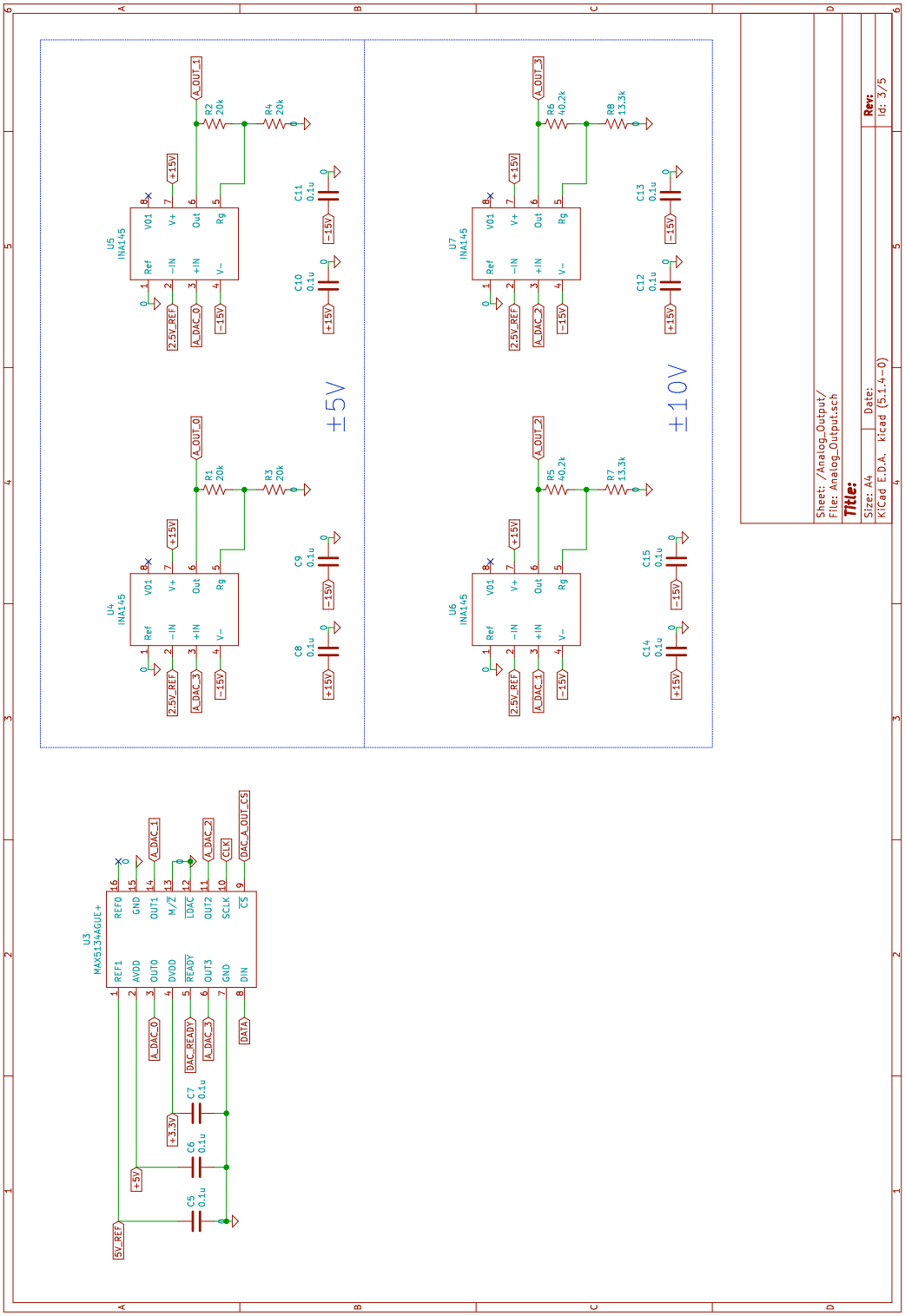
Vcc
In
Out
SCLK
+5V
D_OUT
D_IN
U10
ADC122S051
SCLK
DOUT
DIN
VA
GND
IN1
IN2
ADC_1
ADC_2
CS_ADC
C32
0.1u
C33
1u
R24
10k
R23
10k
R25
20k
R26
10k
R27
20k
U7C
OPA4141
+2.5V
Voltage_Meas
R29
10k
R28
10k
R30
49.9k
R31
10k
R32
10k
U7D
Current_Meas

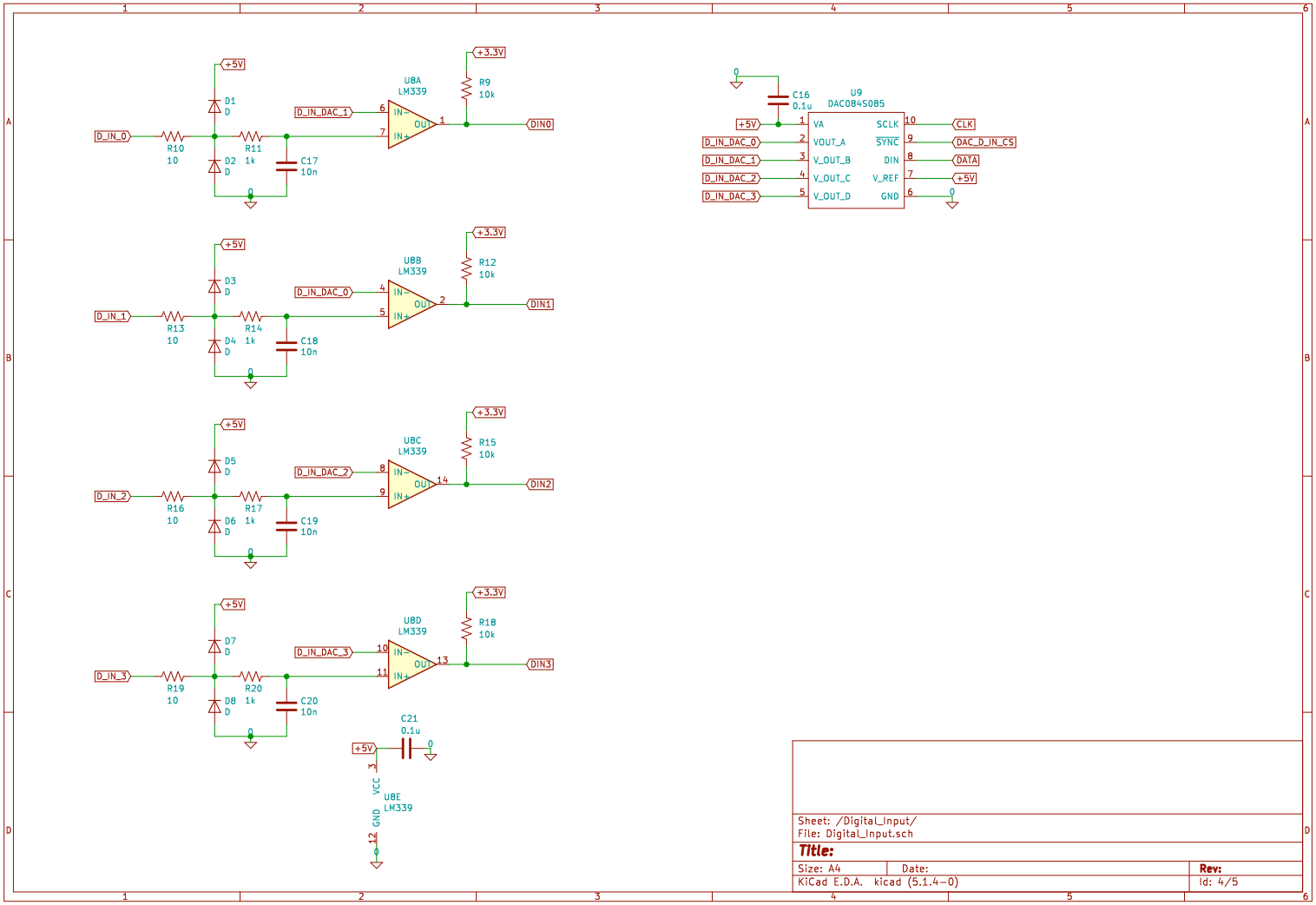

Control_Voltage
Voltage_Meas
+5V_Power
RELAY_3
D3
1N4148
Q5
2N3904
R33
10k
Voltage_Current
HE721C0500
Shunt_PMOS
Shunt_NMOS
V_Load
D6
Q8
R36
Positive_Negative
D1_Cathode
D2_Anode
V_LIM
D5
Q7
R35
Series_PMOS
Series_NMOS
Load_Voltage
D4
Q6
R34
Sheet: /relay_drivers/
File: relay_drivers.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4-0)
Id: 5/5

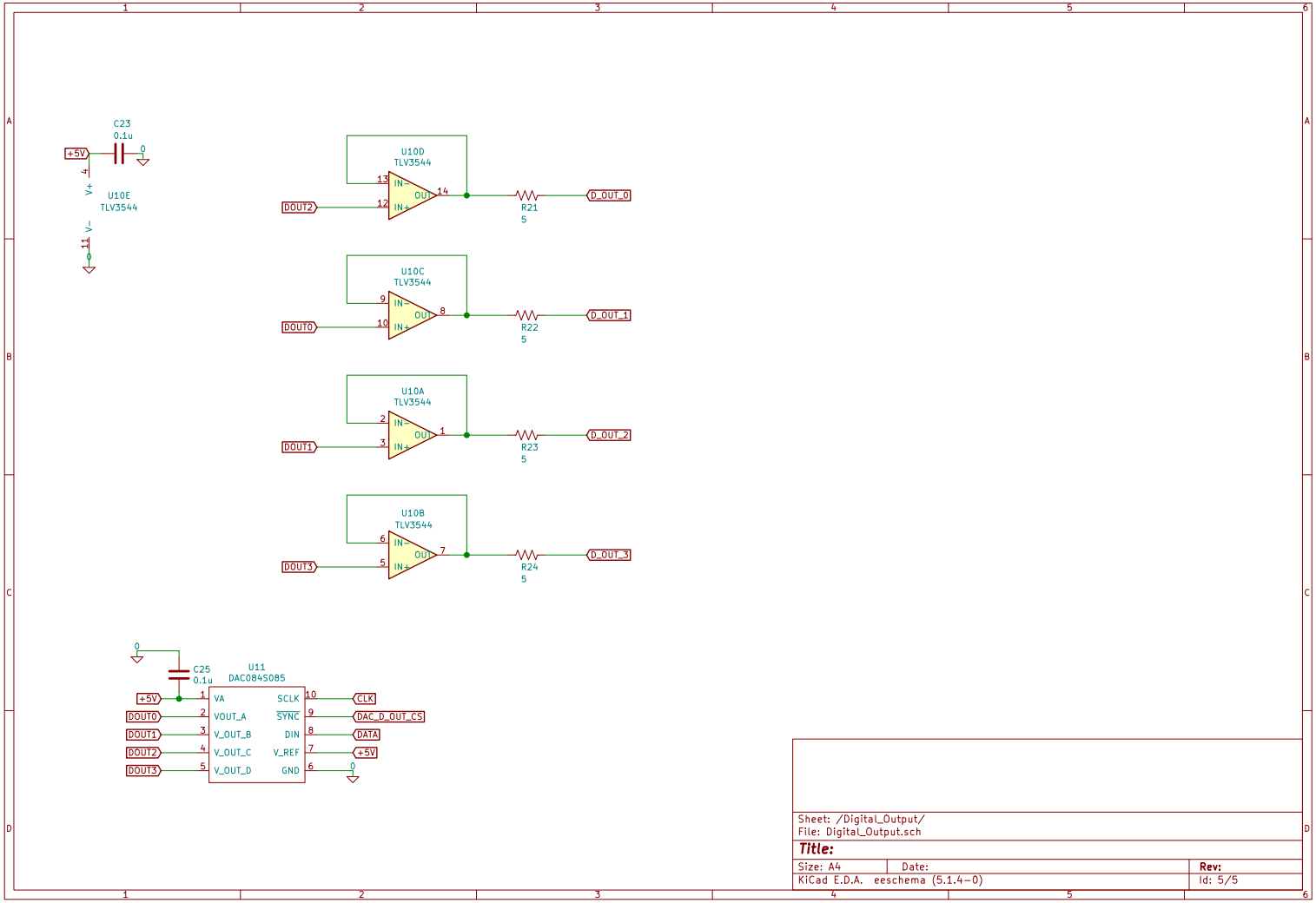
9.1.5 Analog/Digital Input/Output Revision A



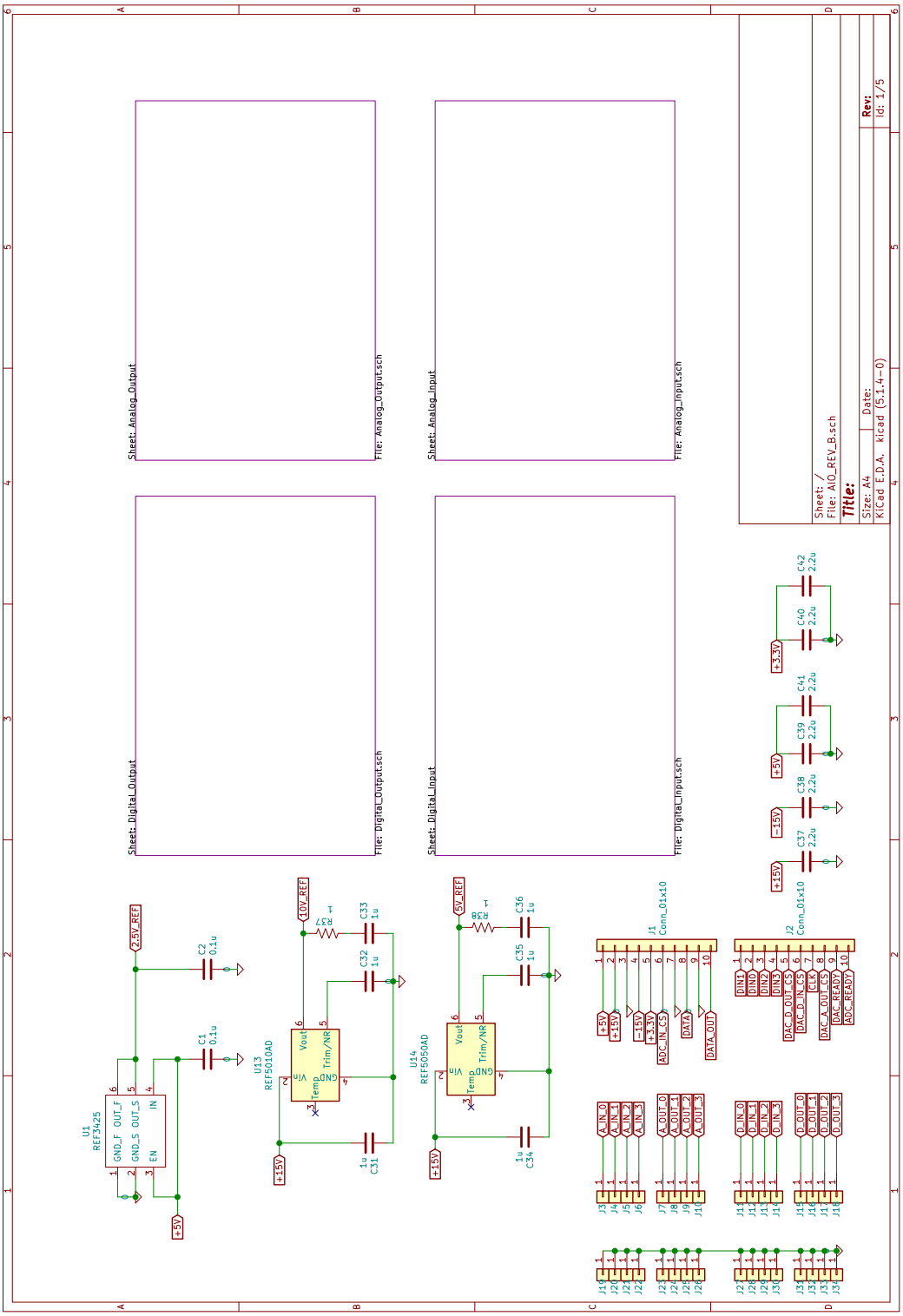

U12A
OPA4196
A_IN_0
R27
1k
C22
6.8u
R25
50k
R26
50k
10V_REF
AIN0
U12B
OPA4196
A_IN_1
R30
1k
C24
6.8u
R28
50k
R29
50k
10V_REF
AIN1
U12C
OPA4196
A_IN_2
R33
1k
C26
6.8u
R31
50k
R32
50k
10V_REF
AIN2
U12D
OPA4196
A_IN_3
R36
1k
C28
6.8u
R34
50k
R35
50k
10V_REF
AIN3
U12E
OPA4196
+15V
-15V
C27
0.1u
C29
0.1u
U2
ADS1220
SCLK
DOUT
CLK
DGND
AVSS
AIN3
AIN2
REFN0
DIN
DRDY
DVDD
AVDD
AIN0
AIN1
REFP0
CLK
ADC_IN_CS
DATA
DATA_OUT
ADC_READY
+3.3V
+5V
5V_REF
C3
0.1u
C4
0.1u
C0G (NPO)
C30
0.1u
Sheet: /Analog_Input/
File: Analog_Input.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4-0)
Id: 2/5

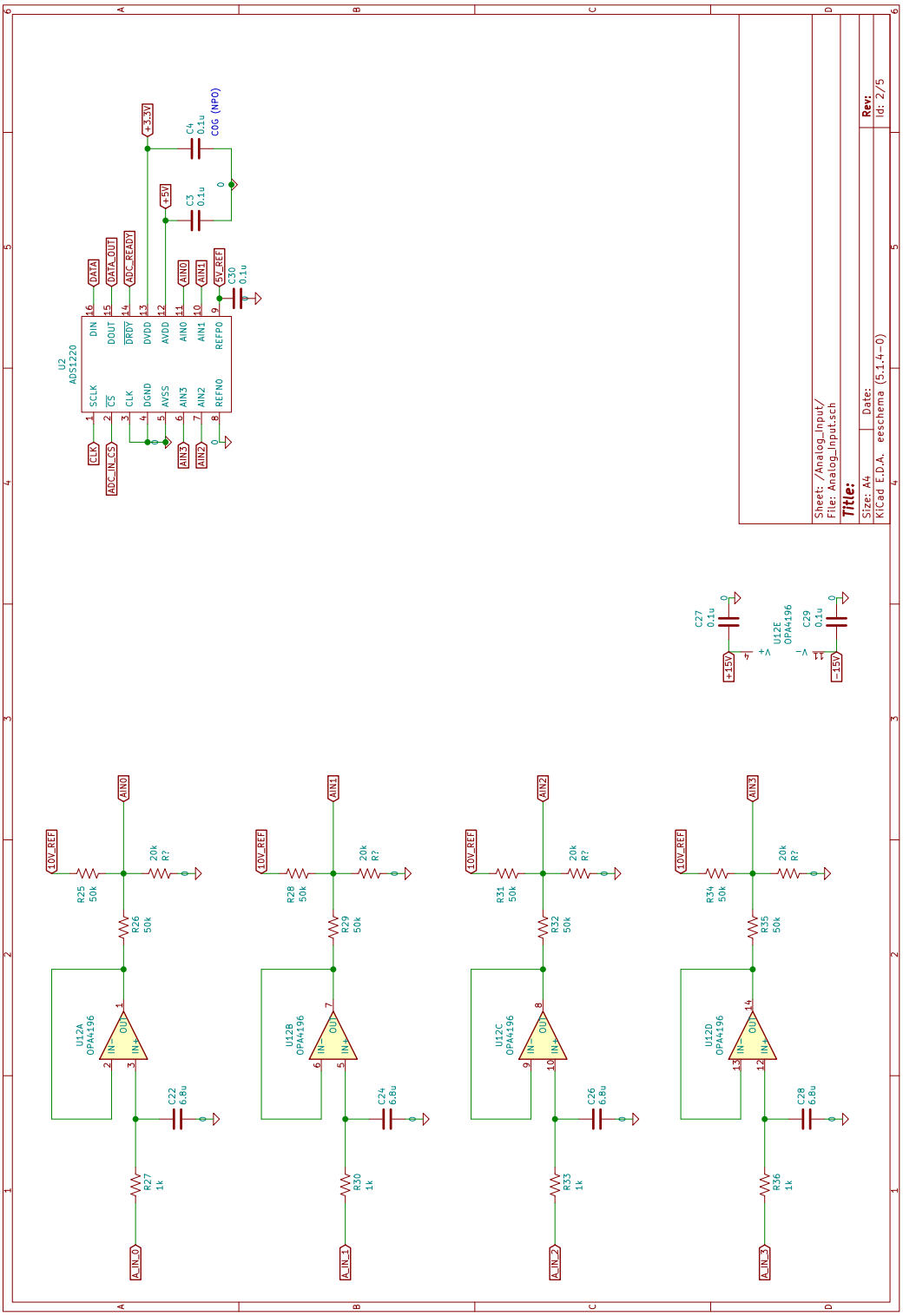

U3
MAX5134AGUE+
REF1
AVDD
OUT0
DVDD
READY
OUT3
GND
DIN
REF0
GND
OUT1
M/Z
LDAC
OUT2
SCLK
CS
5V_REF
+5V
+3.3V
A_DAC_0
A_DAC_3
DAC_READY
DATA
A_DAC_1
A_DAC_2
CLK
DAC_A_OUT_CS
C5 0.1u
C6 0.1u
C7 0.1u
U4
INA145
U5
INA145
U6
INA145
U7
INA145
Ref
VO1
V+
-IN
+IN
Out
Rg
V-
2.5V_REF
A_DAC_3
A_DAC_0
A_DAC_1
A_DAC_2
+15V
-15V
R1 20k
R2 20k
R3 20k
R4 20k
R5 40.2k
R6 40.2k
R7 13.3k
R8 13.3k
A_OUT_0
A_OUT_1
A_OUT_2
A_OUT_3
C8 0.1u
C9 0.1u
C10 0.1u
C11 0.1u
C12 0.1u
C13 0.1u
C14 0.1u
C15 0.1u
±5V
±10V
Sheet: /Analog_Output/
File: Analog_Output.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4-0)
Id: 3/5

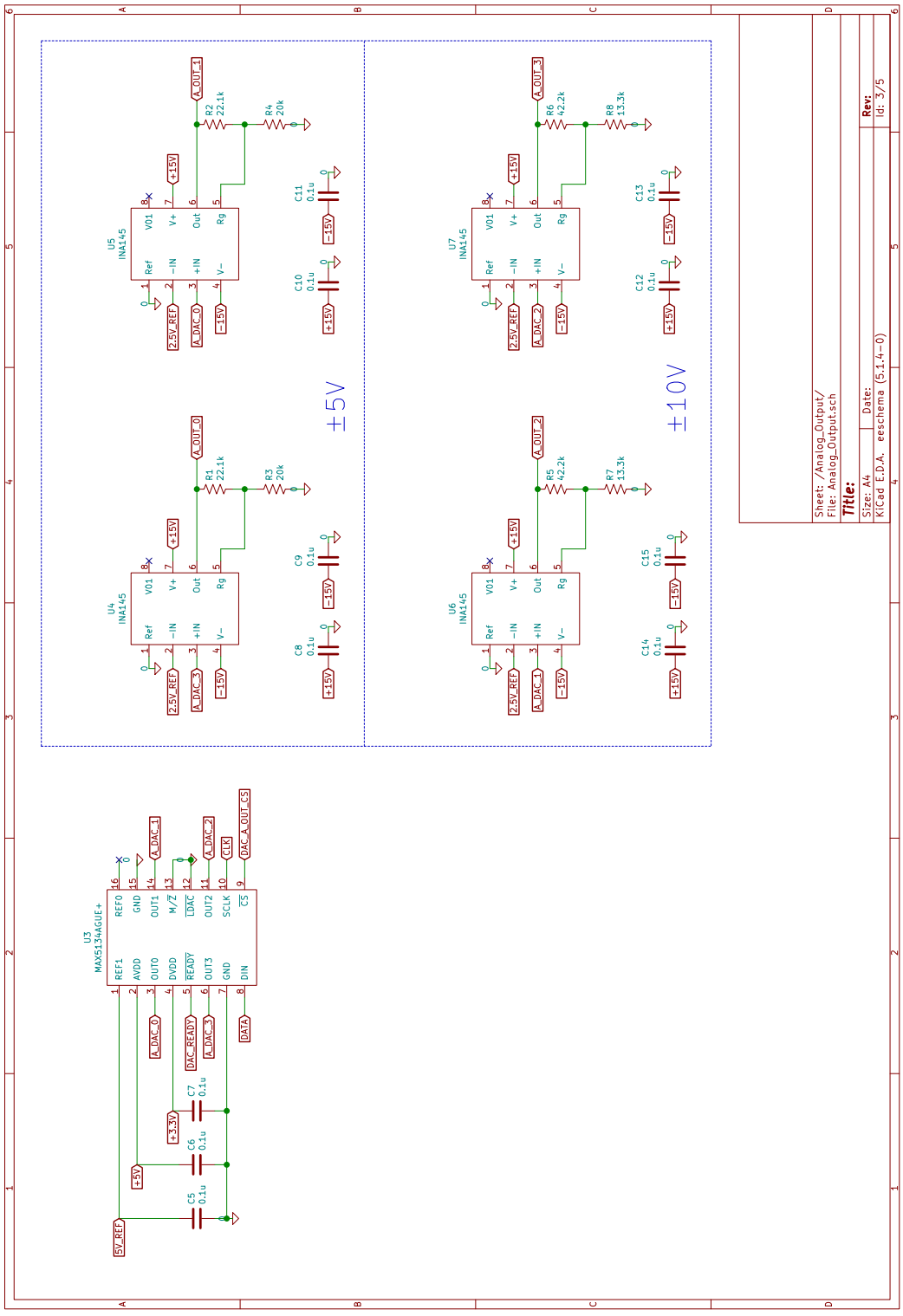

U8A
LM339
U8B
LM339
U8C
LM339
U8D
LM339
U8E
LM339
U9
DAC084S085
D_IN_0
D_IN_1
D_IN_2
D_IN_3
D_IN_DAC_0
D_IN_DAC_1
D_IN_DAC_2
D_IN_DAC_3
DIN0
DIN1
DIN2
DIN3
+5V
+3.3V
CLK
DAC_D_IN_CS
DATA
Sheet: /Digital_Input/
File: Digital_Input.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4-0)
Id: 4/5

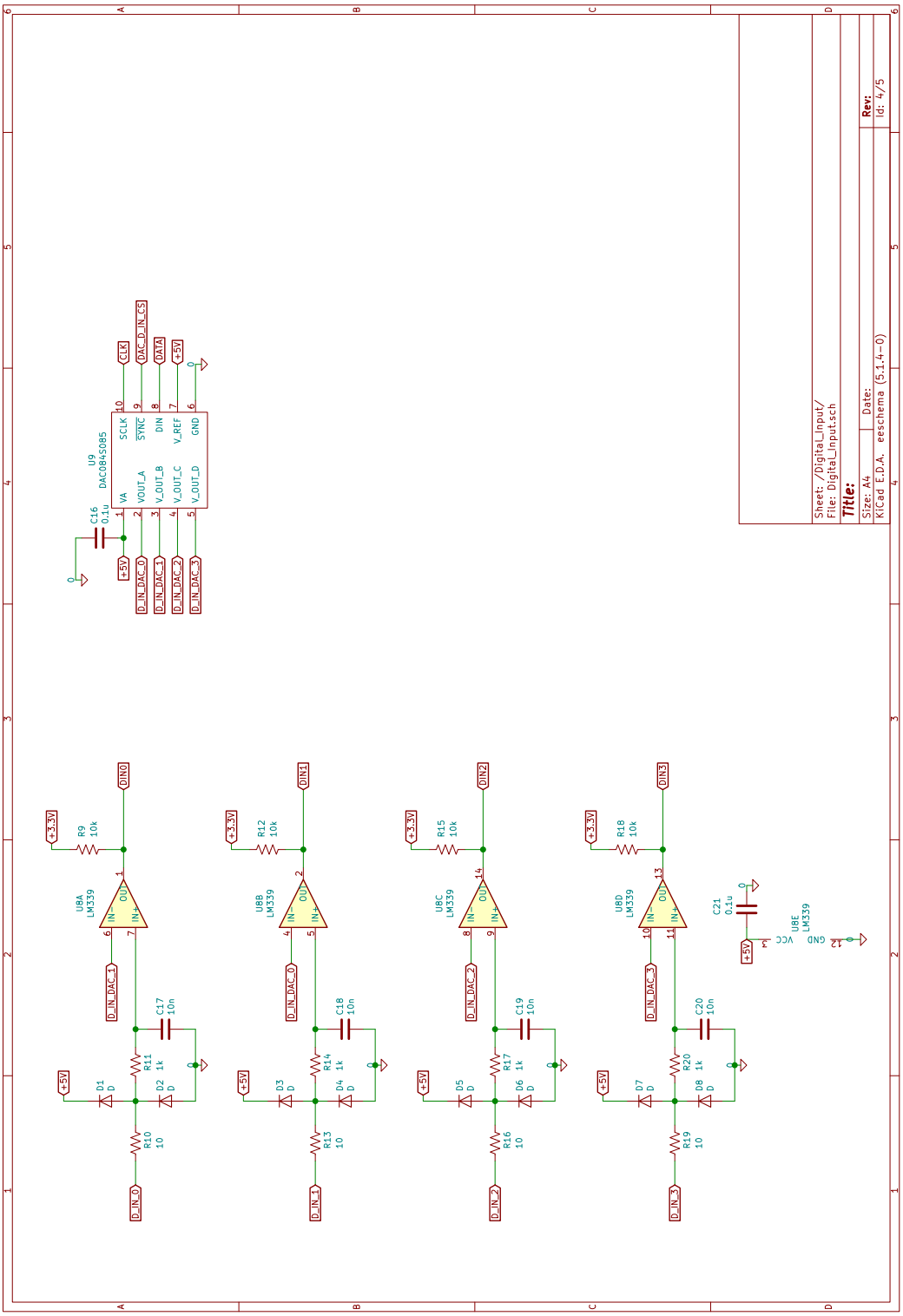

C23
0.1u
+5V
0
4
V+
U10E
TLV3544
11
V-
U10D
TLV3544
13
IN-
12
IN+
14
OUT
DOUT2
R21
5
D_OUT_0
U10C
TLV3544
9
IN-
10
IN+
8
OUT
DOUT0
R22
5
D_OUT_1
U10A
TLV3544
2
IN-
3
IN+
1
OUT
DOUT1
R23
5
D_OUT_2
U10B
TLV3544
6
IN-
5
IN+
7
OUT
DOUT3
R24
5
D_OUT_3
0
C25
0.1u
U11
DAC0845085
+5V
1
VA
DOUT0
2
VOUT_A
DOUT1
3
V_OUT_B
DOUT2
4
V_OUT_C
DOUT3
5
V_OUT_D
SCLK
10
CLK
SYNC
9
DAC_D_OUT_CS
DIN
8
DATA
V_REF
7
+5V
GND
6
0
Sheet: /Digital_Output/
File: Digital_Output.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema (5.1.4-0)
Id: 5/5

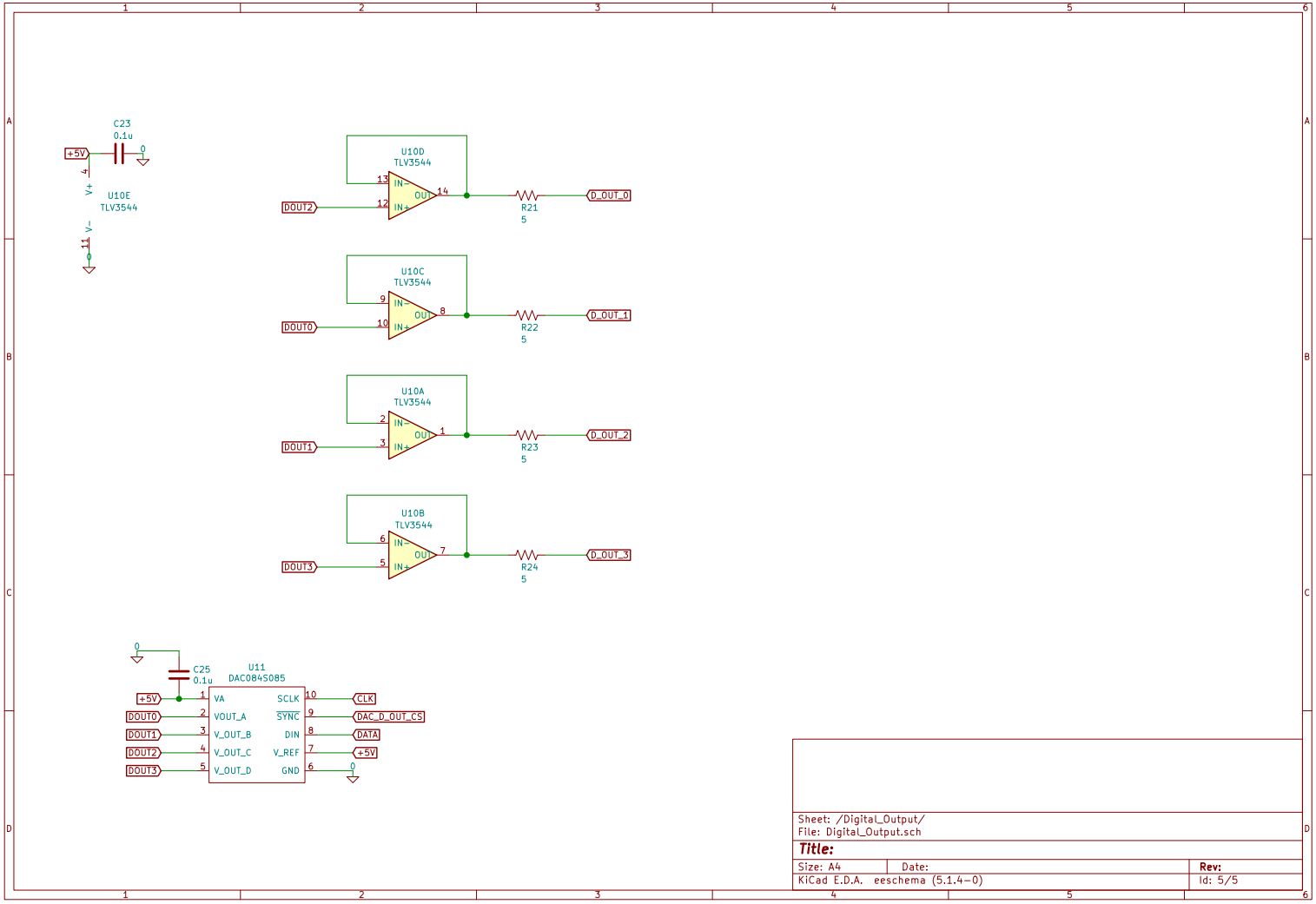
9.1.6 Analog/Digital Input/Output Revision B



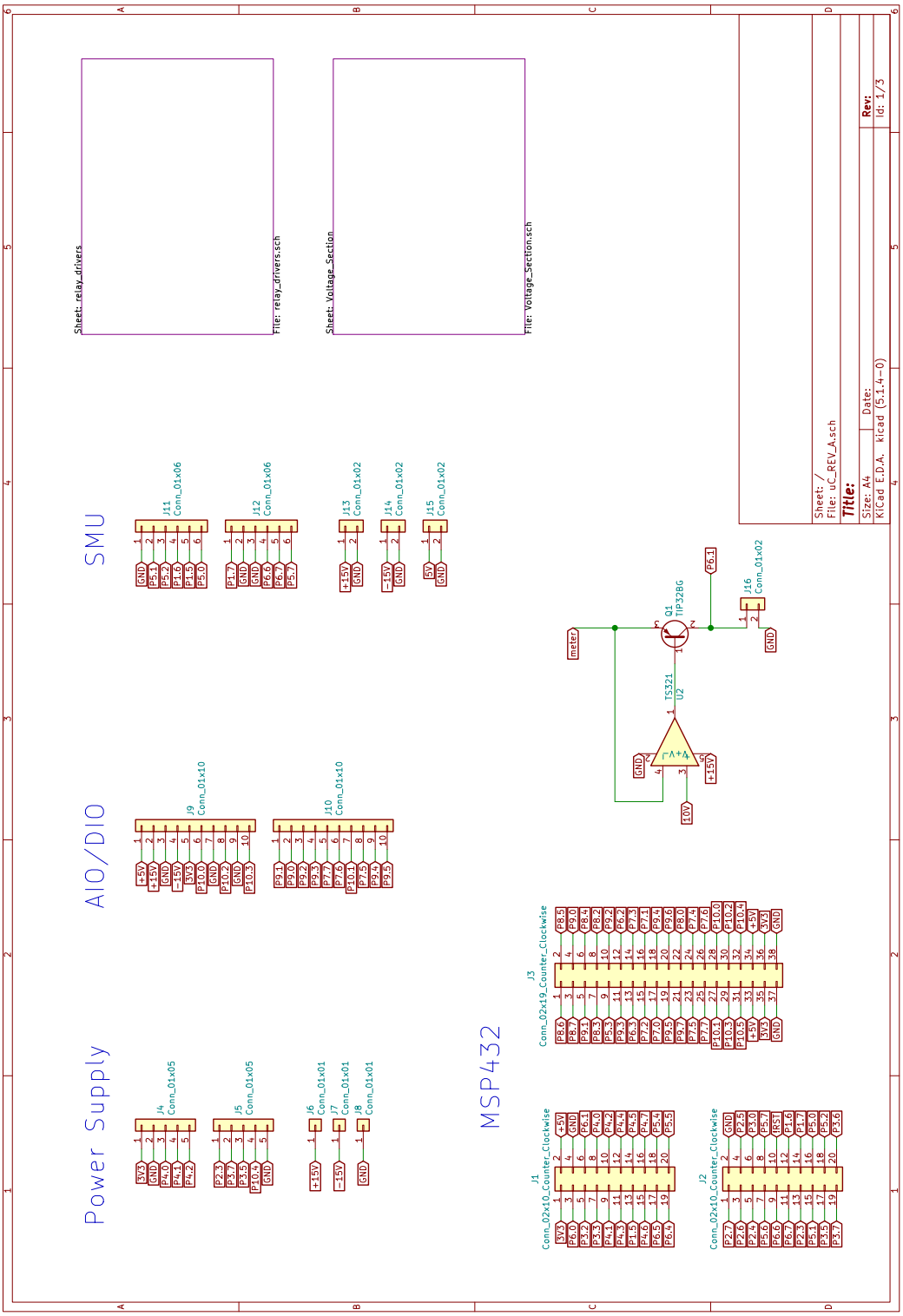

U2
ADS1220
SCLK
CS
CLK
DGND
AVSS
AIN3
AIN2
REFN0
DIN
DOUT
DRDY
DVDD
AVDD
AIN0
AIN1
REFP0
CLK
ADC_IN_CS
DATA
DATA_OUT
ADC_READY
AIN0
AIN1
5V_REF
+3.3V
+5V
C4
0.1u
C0G (NPO)
C3
0.1u
C30
0.1u
Sheet: /Analog_Input/
File: Analog_Input.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema (5.1.4-0)
Id: 2/5
U12A
OPA4196
U12B
OPA4196
U12C
OPA4196
U12D
OPA4196
U12E
OPA4196
C27
0.1u
C29
0.1u
+15V
-15V
10V_REF
R25
50k
R26
50k
20k
R?
R27
1k
C22
6.8u
A_IN_0
R28
50k
R29
50k
R30
1k
C24
6.8u
A_IN_1
R31
50k
R32
50k
R33
1k
C26
6.8u
A_IN_2
R34
50k
R35
50k
R36
1k
C28
6.8u
A_IN_3

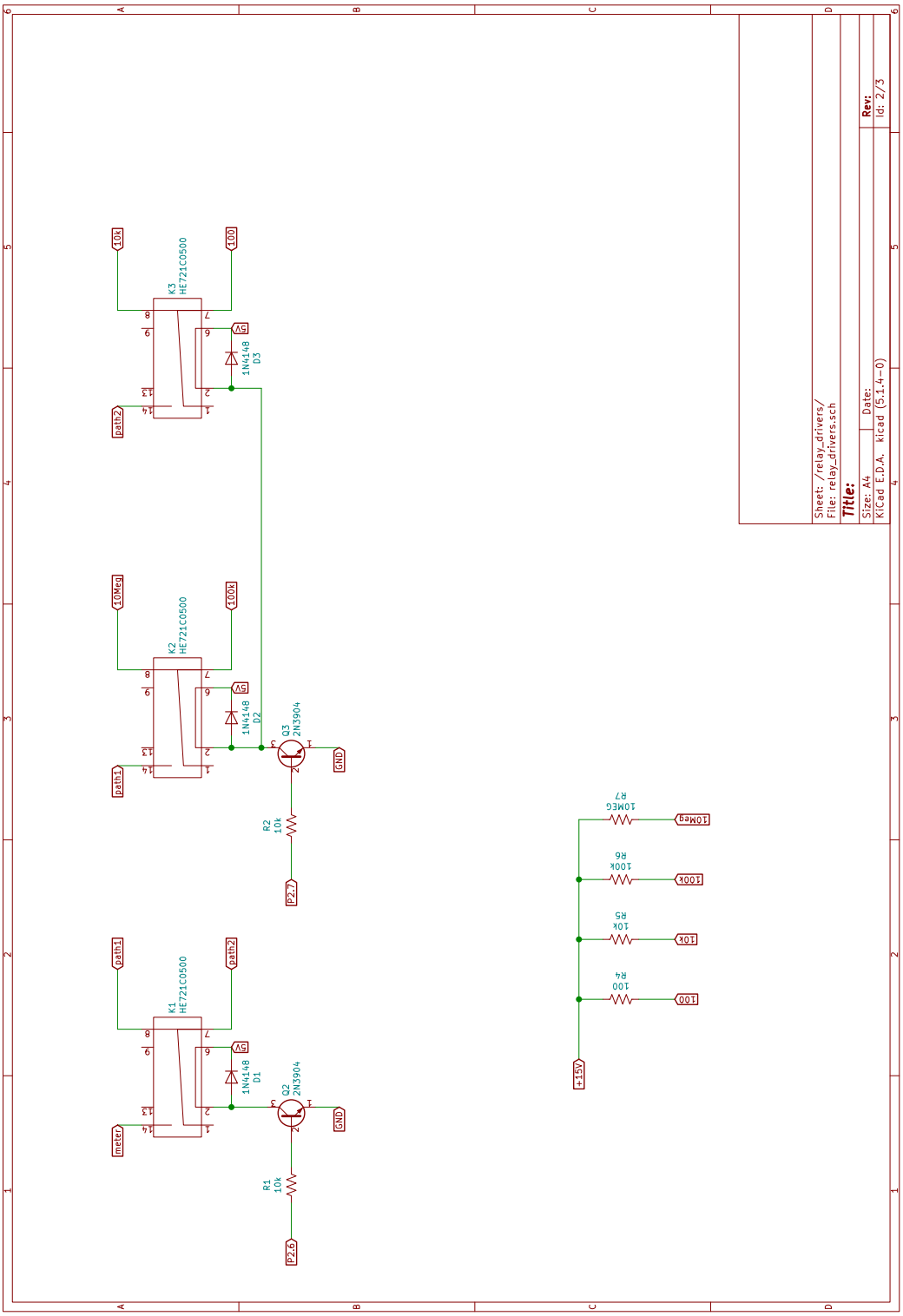

U3
MAX5134AGUE+
REF1
AVDD
OUT0
DVDD
READY
OUT3
GND
DIN
REF0
GND
OUT1
M/Z
LDAC
OUT2
SCLK
CS
5V_REF
+5V
+3.3V
A_DAC_0
DAC_READY
A_DAC_3
DATA
A_DAC_1
A_DAC_2
CLK
DAC_A_OUT_CS
C5 0.1u
C6 0.1u
C7 0.1u
U4
INA145
U5
INA145
U6
INA145
U7
INA145
Ref
-IN
+IN
V-
VO1
V+
Out
Rg
2.5V_REF
A_DAC_3
A_DAC_0
A_DAC_1
A_DAC_2
+15V
-15V
A_OUT_0
A_OUT_1
A_OUT_2
A_OUT_3
R1 22.1k
R2 22.1k
R3 20k
R4 20k
R5 42.2k
R6 42.2k
R7 13.3k
R8 13.3k
C8 0.1u
C9 0.1u
C10 0.1u
C11 0.1u
C12 0.1u
C13 0.1u
C14 0.1u
C15 0.1u
±5V
±10V
Sheet: /Analog_Output/
File: Analog_Output.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema (5.1.4-0)
Id: 3/5

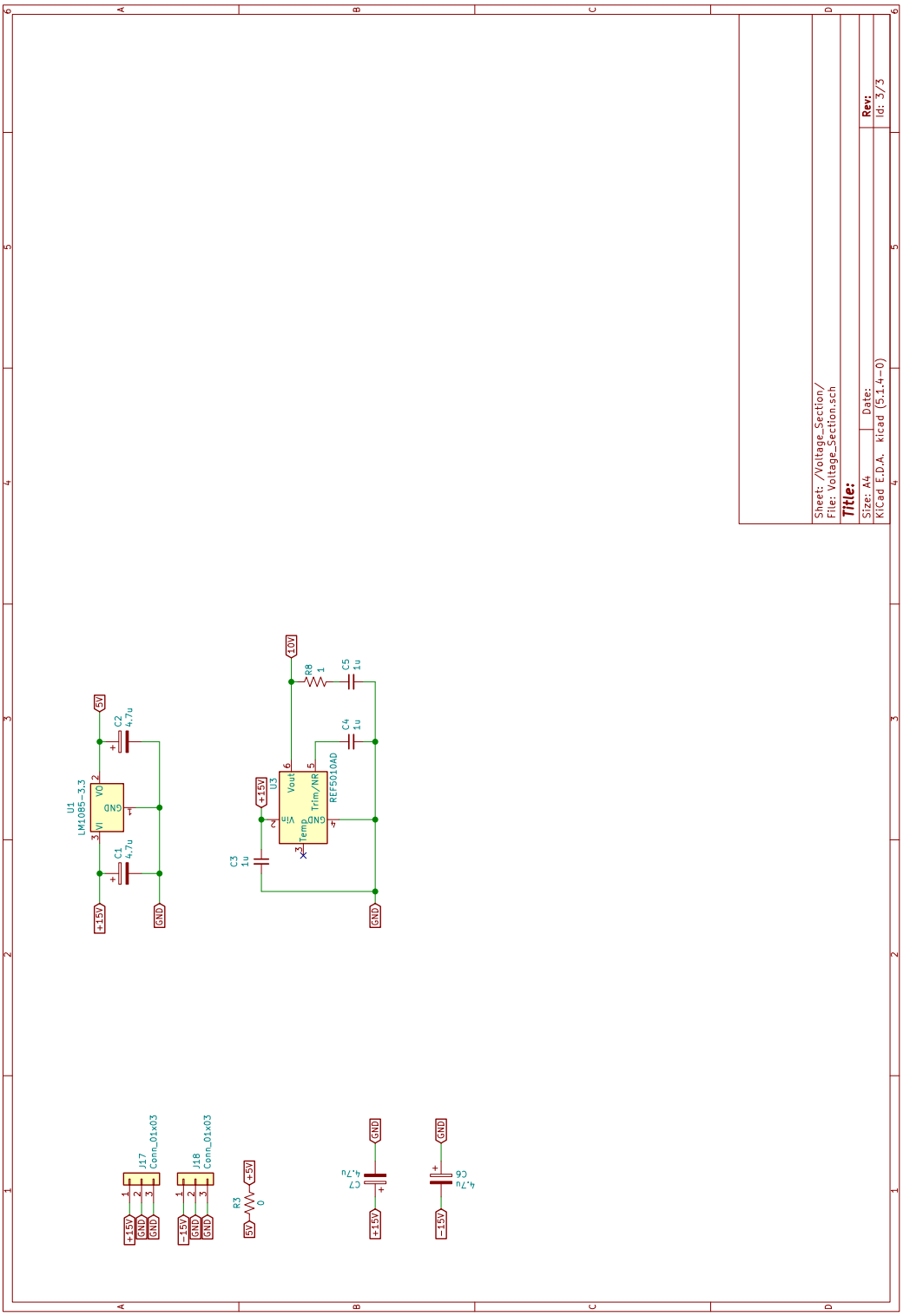

Sheet: /Digital_Input/
File: Digital_Input.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema (5.1.4-0)
Id: 4/5
U9
DAC084S085
C16
0.1u
U8A
LM339
U8B
LM339
U8C
LM339
U8D
LM339
U8E
LM339
C17
10n
C18
10n
C19
10n
C20
10n
C21
0.1u
R9
10k
R10
10
R11
1k
R12
10k
R13
10
R14
1k
R15
10k
R16
10
R17
1k
R18
10k
R19
10
R20
1k
D1
D2
D3
D4
D5
D6
D7
D8
+5V
+3.3V
0
DIN0
DIN1
DIN2
DIN3
D_IN_0
D_IN_1
D_IN_2
D_IN_3
D_IN_DAC_0
D_IN_DAC_1
D_IN_DAC_2
D_IN_DAC_3
CLK
DAC_D_IN_CS
DATA
V_OUT_A
V_OUT_B
V_OUT_C
V_OUT_D
V_REF
VA
SCLK
SYNC
DIN
GND


C23
0.1u
+5V
0
4
V+
U10E
TLV3544
11
V-
U10D
TLV3544
13
IN-
12
IN+
14
OUT
DOUT2
R21
5
D_OUT_0
U10C
TLV3544
9
IN-
10
IN+
8
OUT
DOUT0
R22
5
D_OUT_1
U10A
TLV3544
2
IN-
3
IN+
1
OUT
DOUT1
R23
5
D_OUT_2
U10B
TLV3544
6
IN-
5
IN+
7
OUT
DOUT3
R24
5
D_OUT_3
0
C25
0.1u
U11
DAC0845085
+5V
1
VA
DOUT0
2
VOUT_A
DOUT1
3
V_OUT_B
DOUT2
4
V_OUT_C
DOUT3
5
V_OUT_D
SCLK
10
CLK
SYNC
9
DAC_D_OUT_CS
DIN
8
DATA
V_REF
7
+5V
GND
6
0
Sheet: /Digital_Output/
File: Digital_Output.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema (5.1.4-0)
Id: 5/5

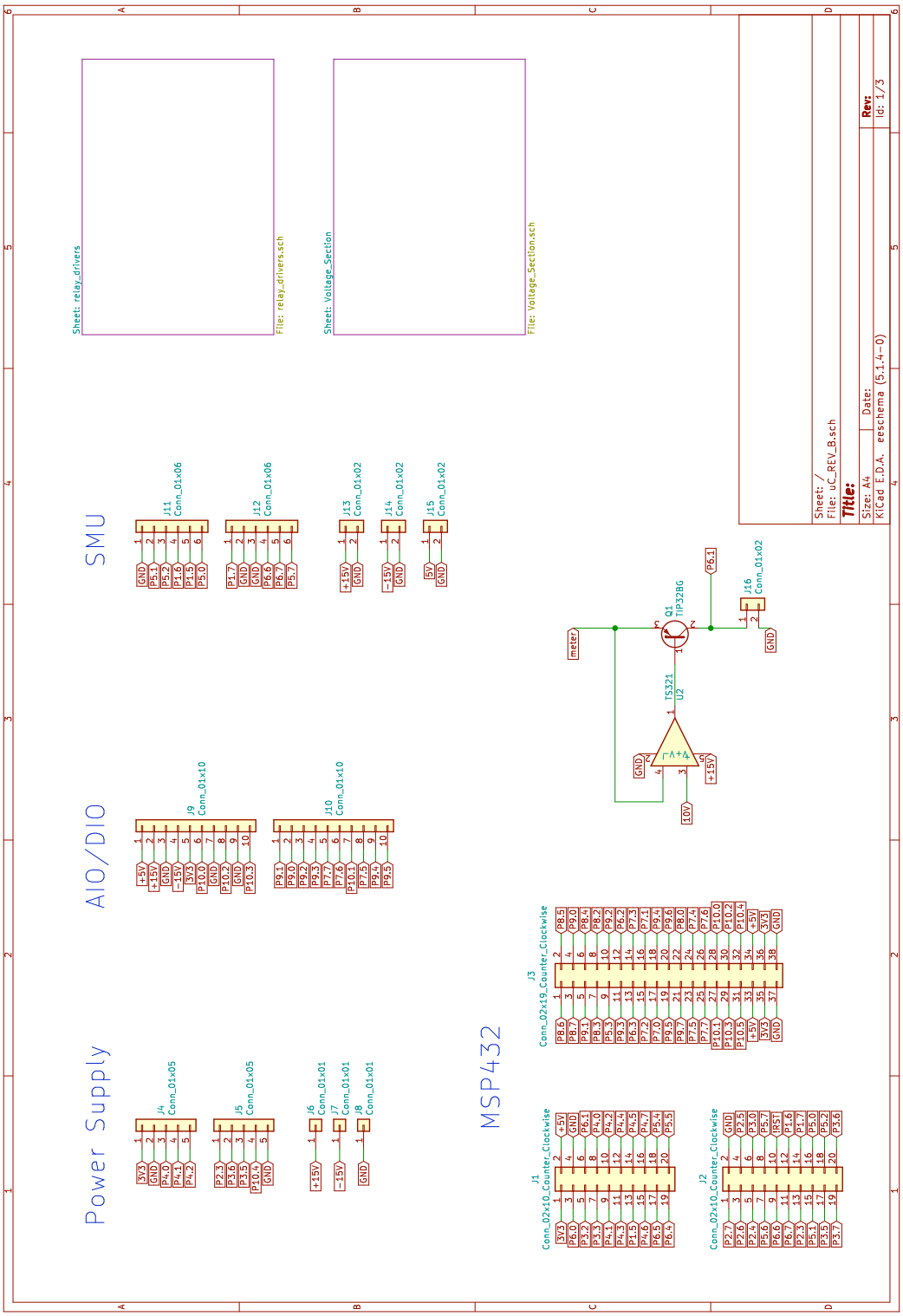
9.1.7 µC Revision A

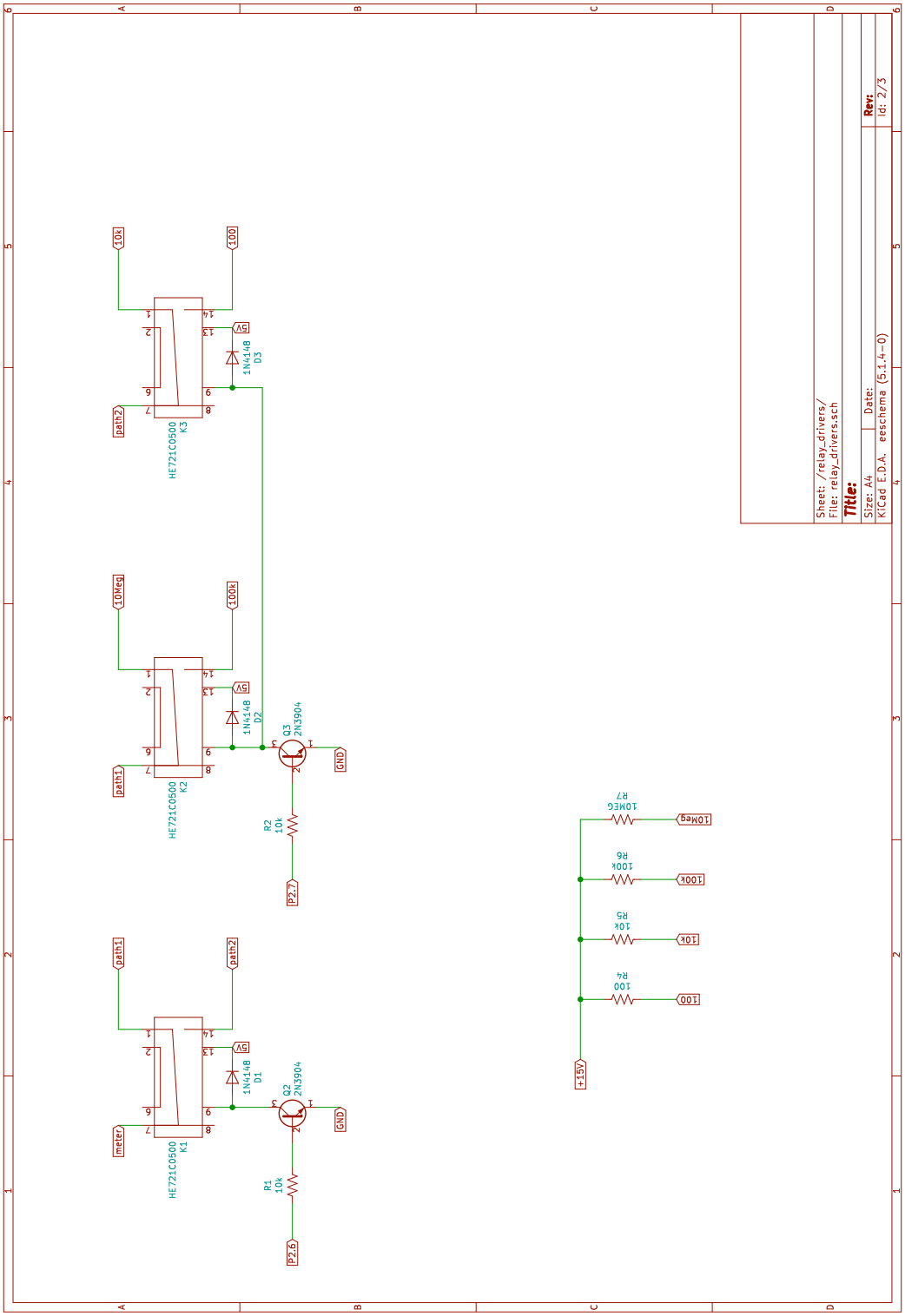


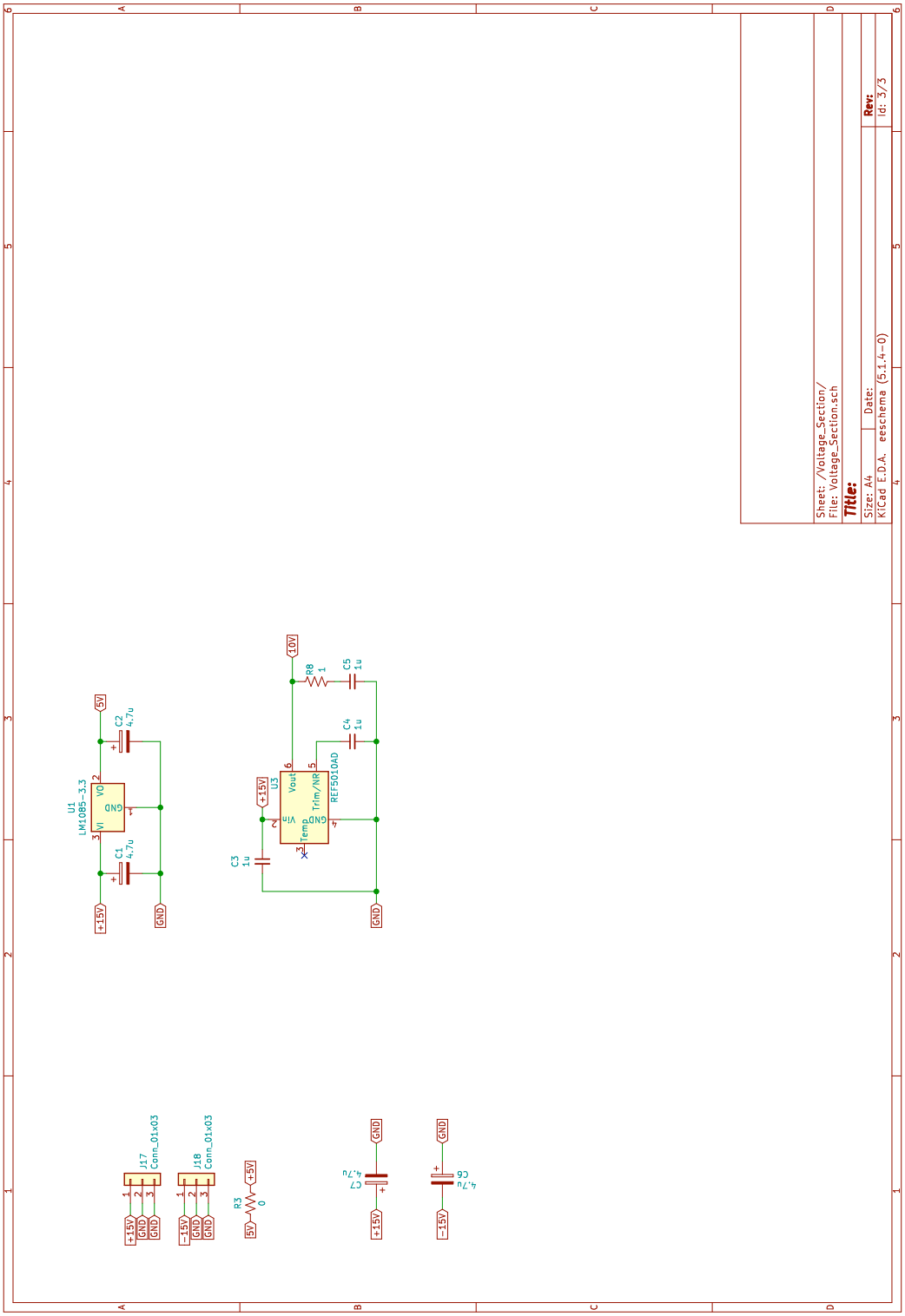

Sheet: /relay_drivers/
File: relay_drivers.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4-0)
Id: 2/3
K3
HE721C0500
K2
HE721C0500
K1
HE721C0500
1N4148
D3
1N4148
D2
1N4148
D1
Q3
2N3904
Q2
2N3904
10k
100
10Meg
100k
path2
path1
meter
5V
GND
R2
10k
R1
10k
P2.7
P2.6
R7
10MEG
R6
100K
R5
10K
R4
100
+15V


Sheet: /Voltage_Section/
File: Voltage_Section.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.4-0)
Id: 3/3
U1
LM1085-3.3
VI
VO
GND
C1
4.7u
C2
4.7u
+5V
+15V
GND
U3
REF5010AD
Vout
Trim/NR
Temp
C3
1u
C4
1u
C5
1u
R8
1
+10V
J17
Conn_01x03
J18
Conn_01x03
R3
0
C7
4.7u
C6
4.7u
-15V

9.1.8 µC Revision B

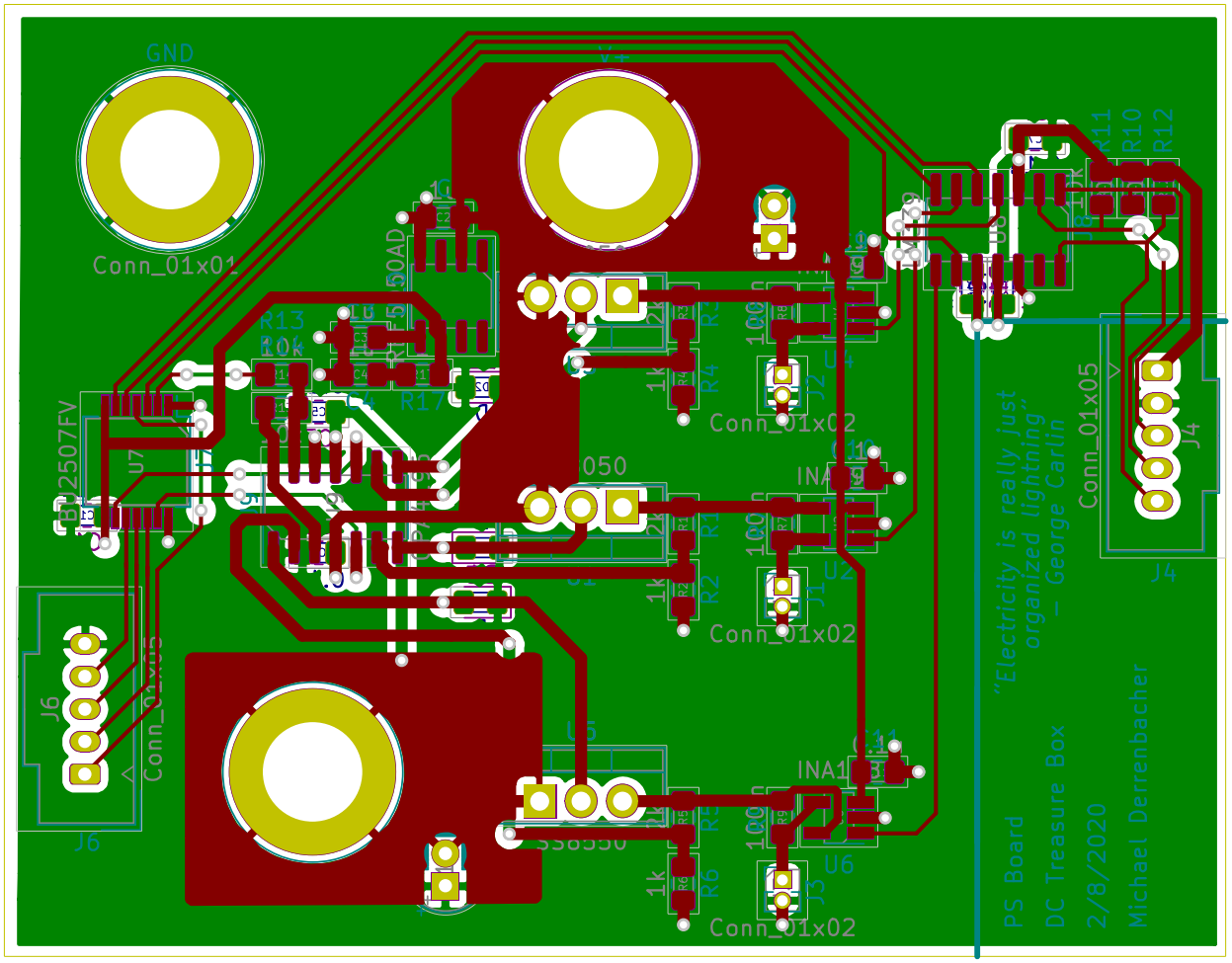



10k
100
5V
1N4148
D3
path2
HE721C0500
K3
10Meg
100k
5V
1N4148
D2
Q3
2N3904
path1
HE721C0500
K2
R2
10k
P2.7
GND
path1
path2
5V
1N4148
D1
Q2
2N3904
meter
HE721C0500
K1
R1
10k
P2.6
GND
10MEG
R7
100k
R6
10k
R5
100
R4
10Meg
100k
10k
100
+15V
Sheet: /relay_drivers/
File: relay_drivers.sch
Title:
Size: A4
Date:
KiCad E.D.A. eeschema (5.1.4-0)
Rev:
Id: 2/3

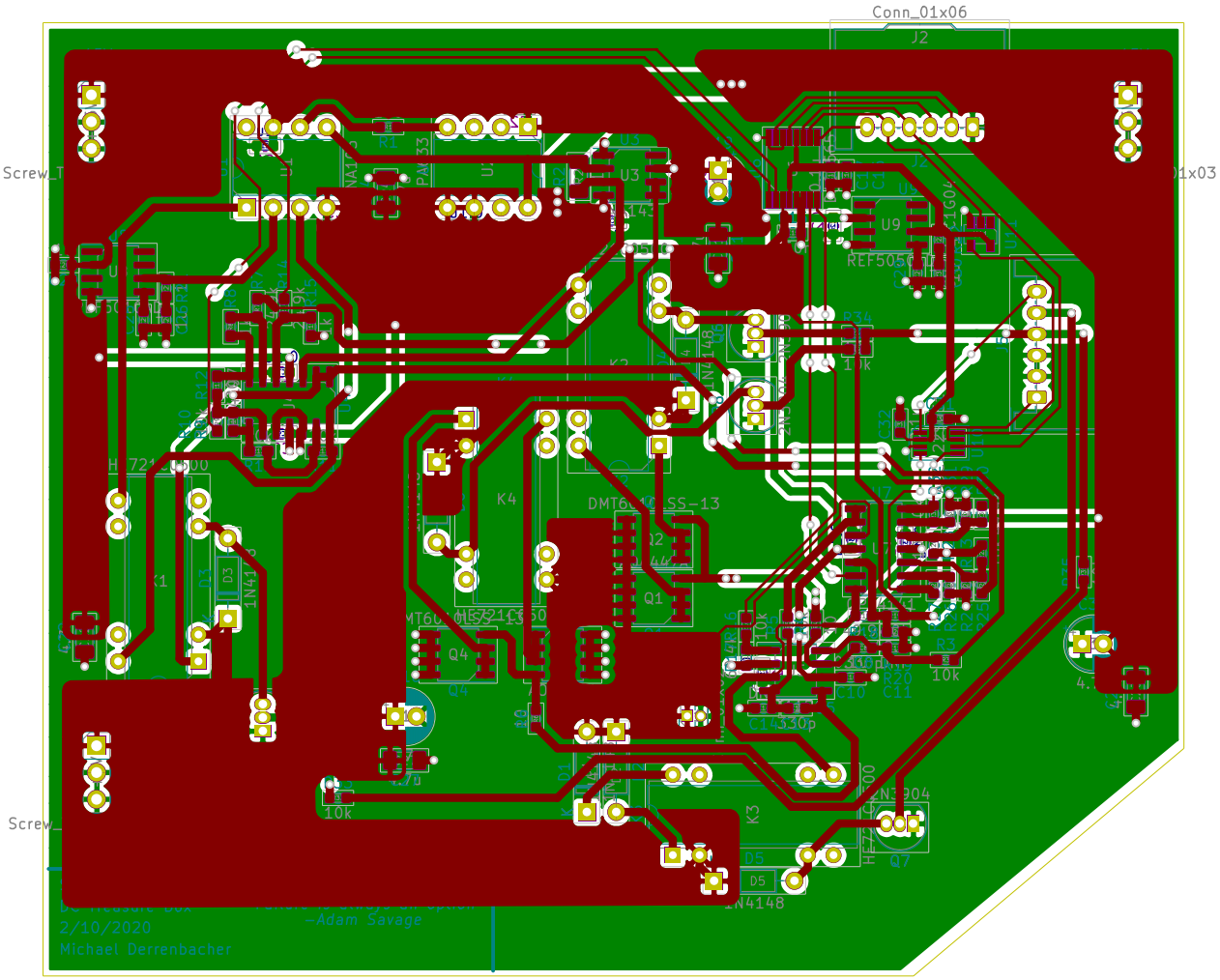

Sheet: /Voltage_Section/
File: Voltage_Section.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. eeschema (5.1.4-0)
Id: 3/3
U1
LM1085-3.3
VI
VO
GND
C1
4.7u
C2
4.7u
+15V
5V
GND
U3
REF5010AD
Vout
Trim/NR
Temp
C3
1u
C4
1u
C5
1u
R8
1
10V
J17
Conn_01x03
J18
Conn_01x03
R3
0
C7
4.7u
C6
4.7u
-15V

9.2 Layouts

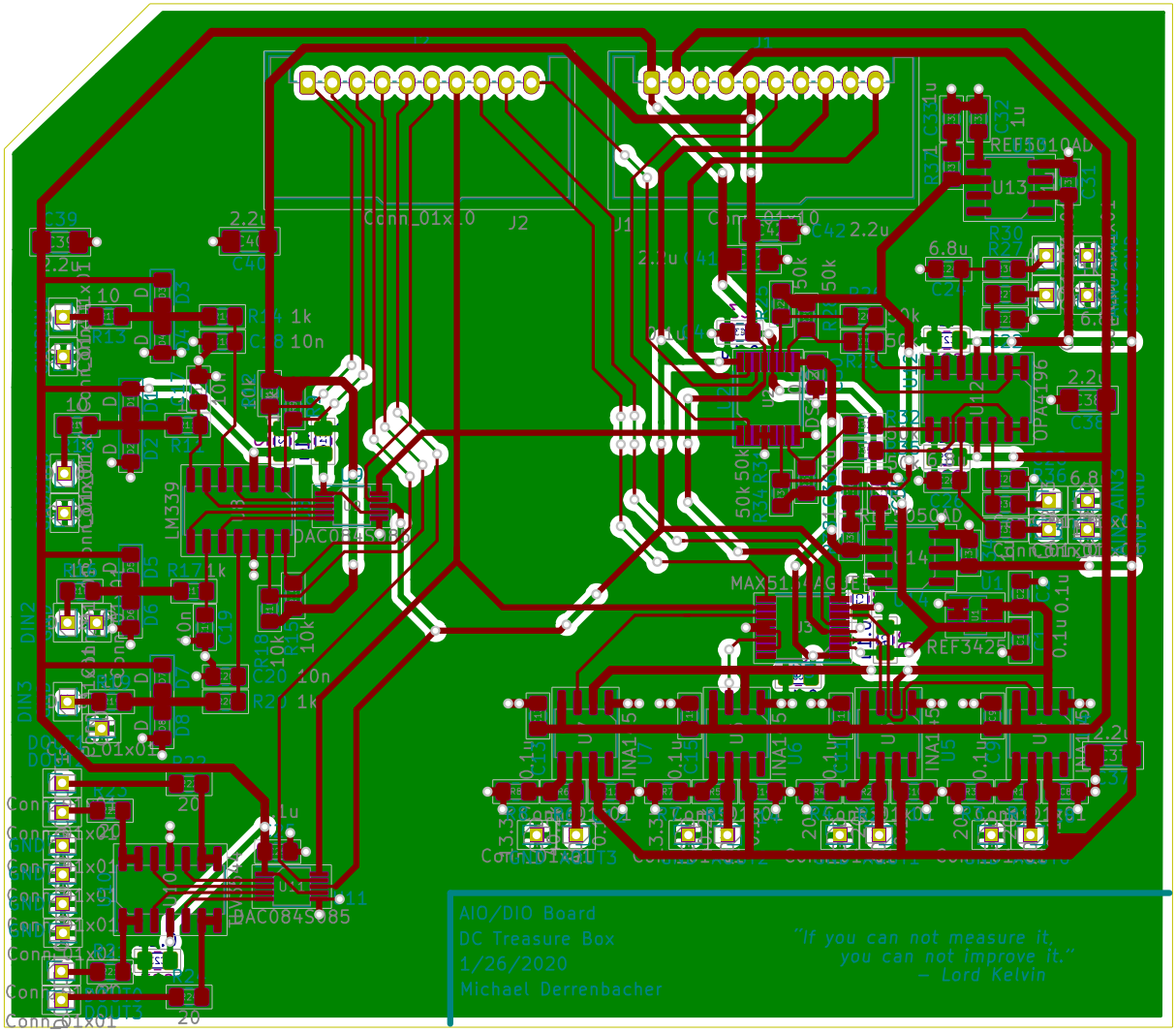
9.2.1 Power Supply Revision A



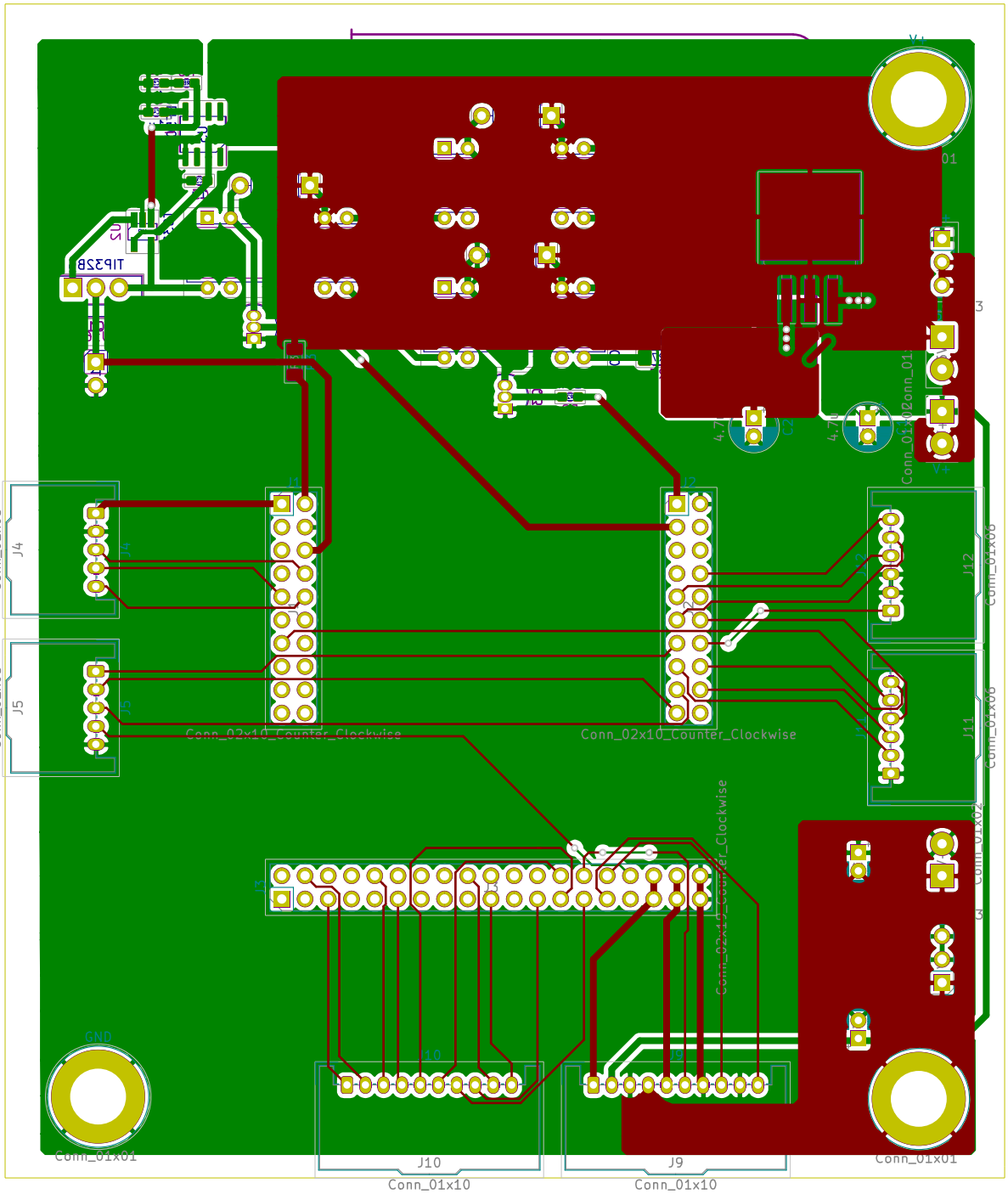
9.2.2 SMU Revision C



9.2.3 Analog/Digital Input/Output Revision A

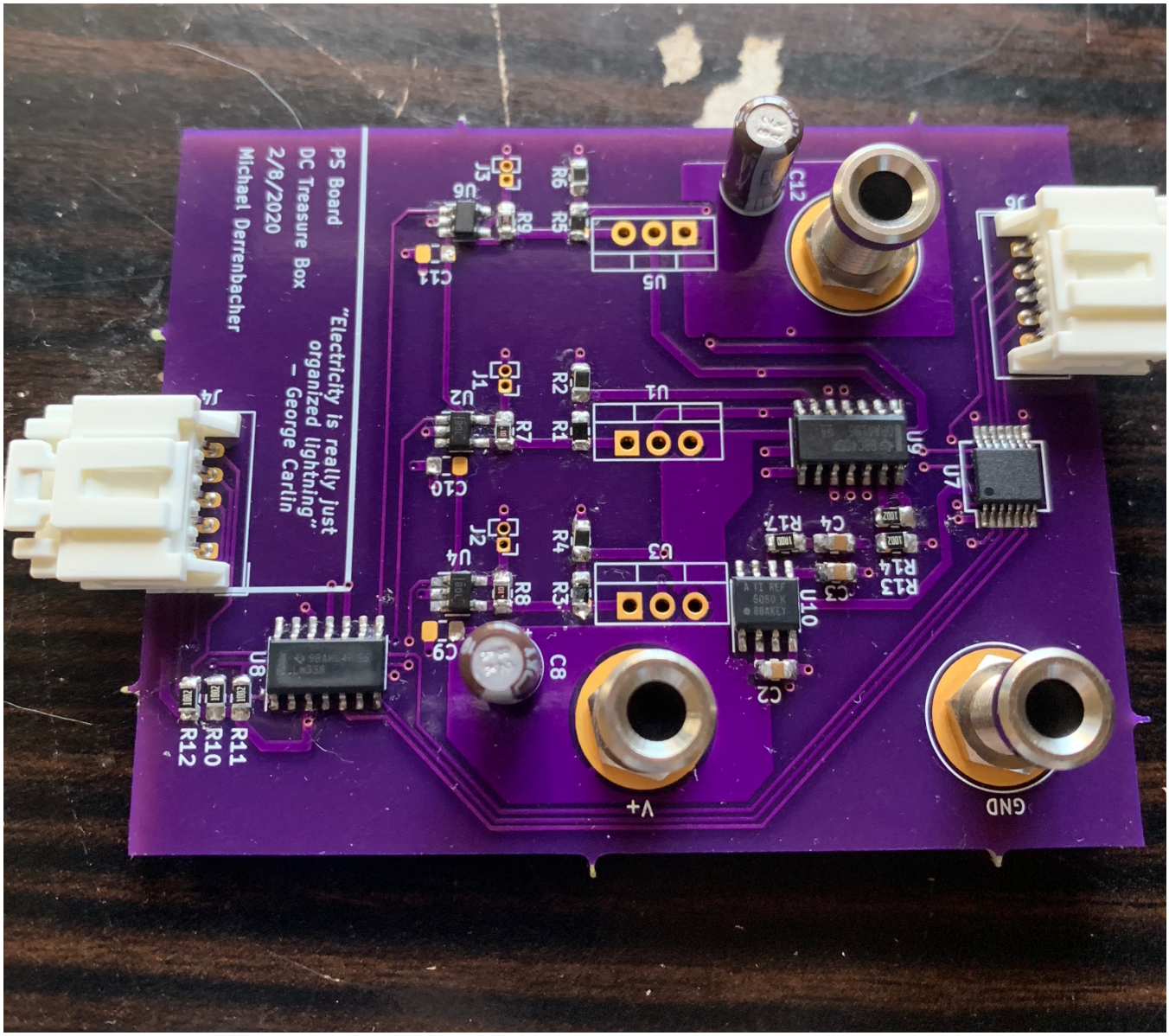


9.2.4 µC Revision A

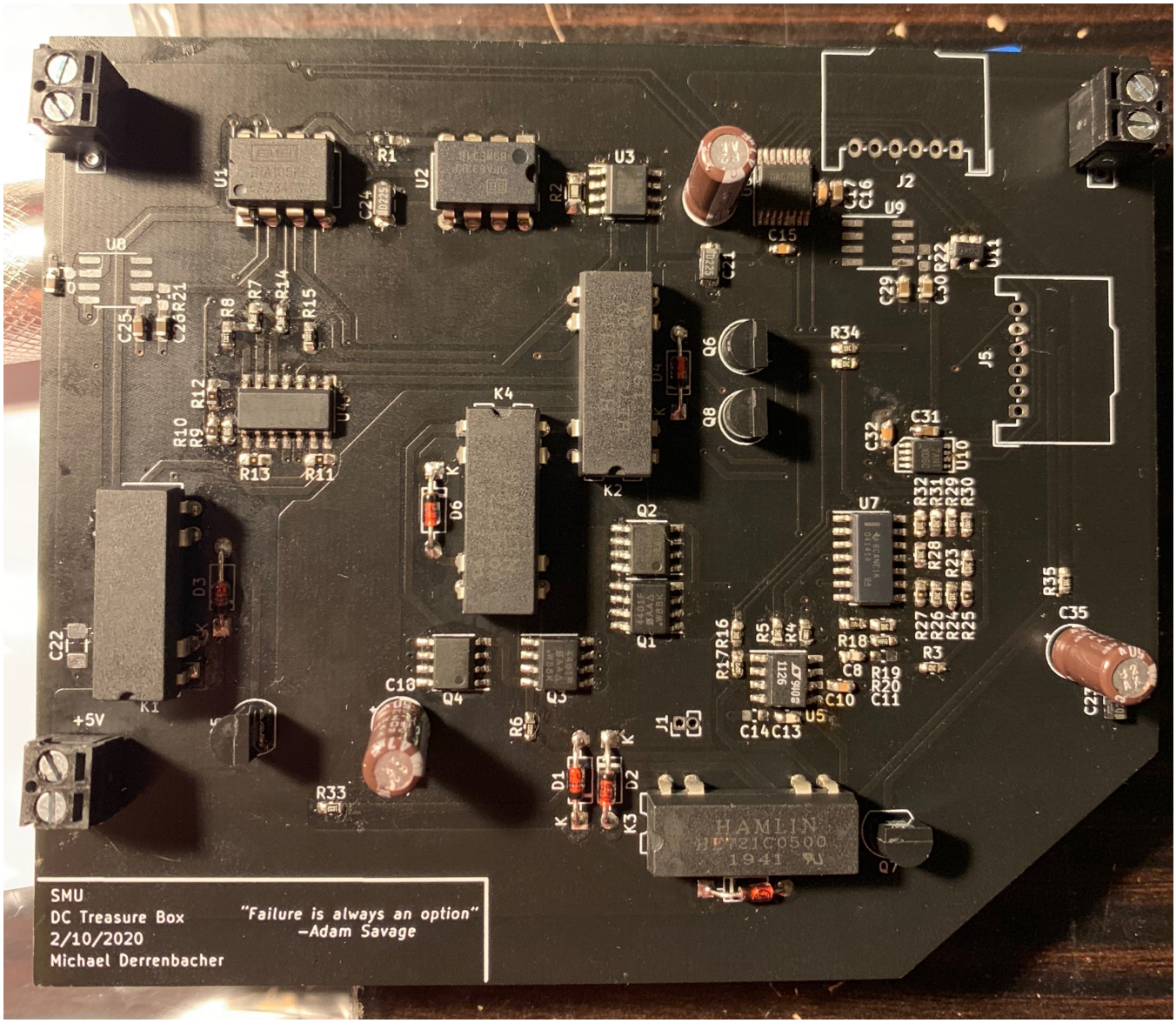


9.3 Fabricated Boards

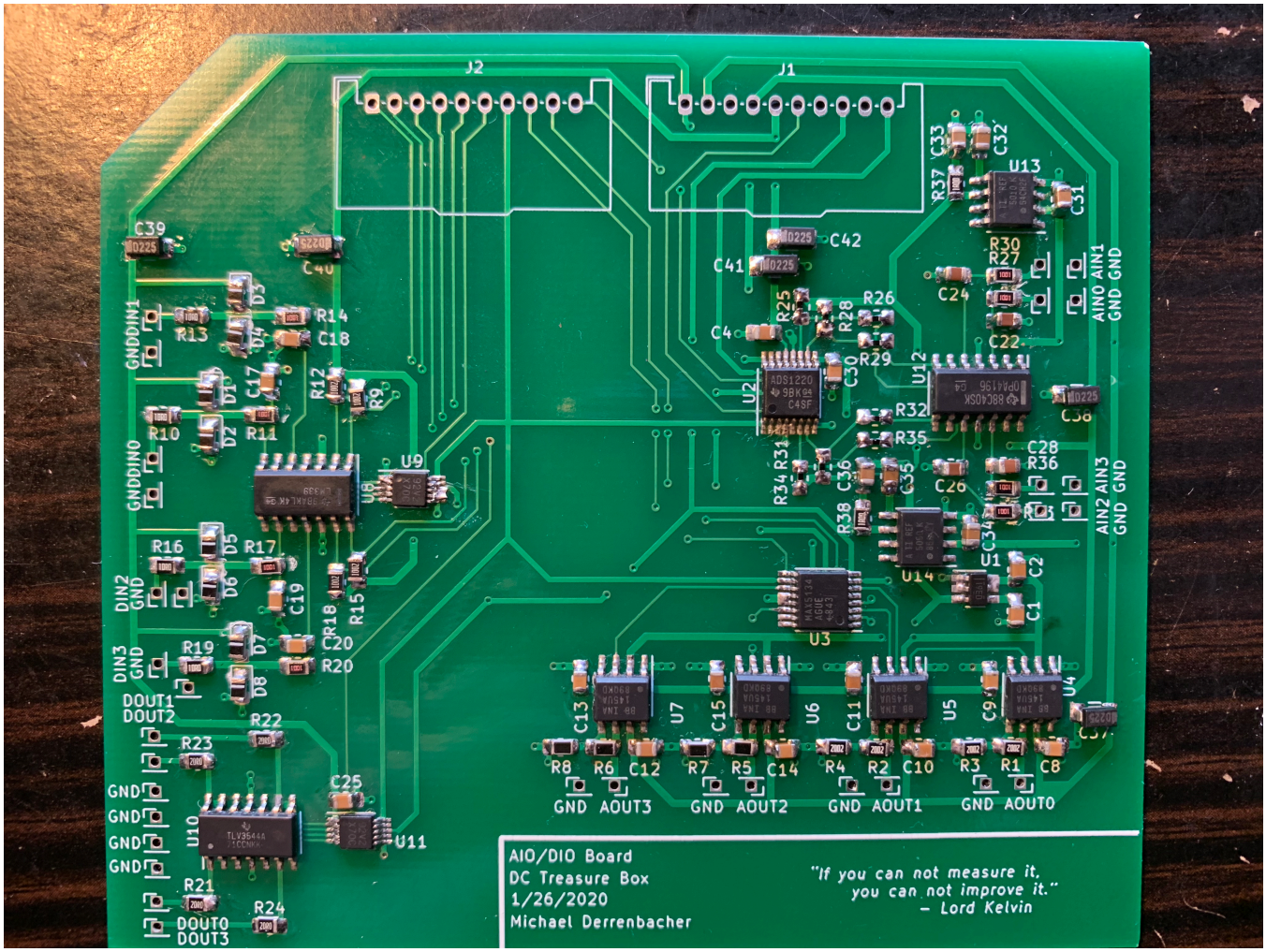
9.3.1 Power Supply Board



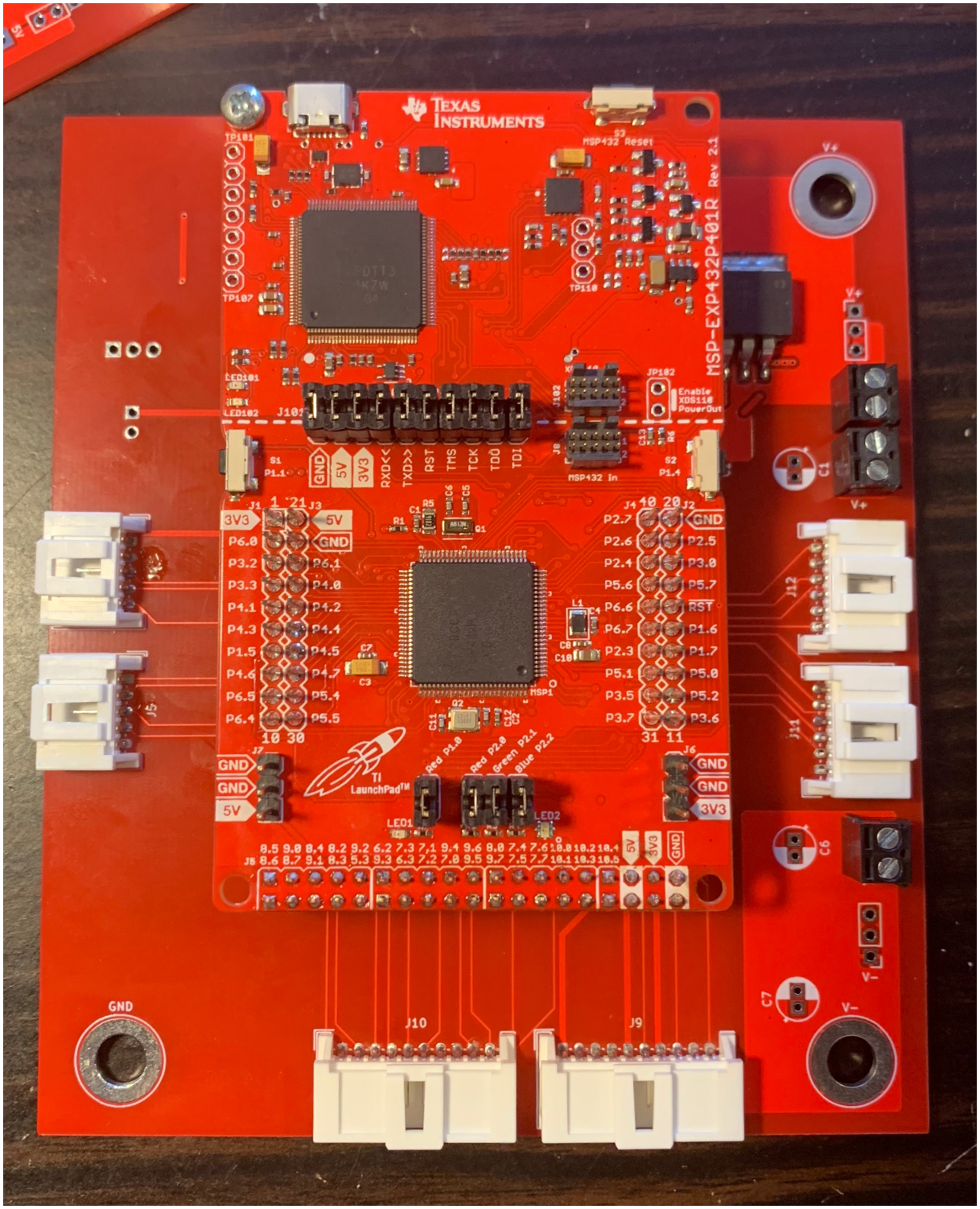
9.3.2 SMU Board



9.3.3 Analog/Digital Input/Output Board



9.3.4 µC Board


TEXAS INSTRUMENTS
MSP-EXP432P401R Rev 2.1
MSP432 Reset
MSP432 In
Enable XDS110 PowerOut
GND
5V
3V3
RXD<<
TXD>>
RST
TMS
TCK
TDO
TDI
P1.1
P1.4
P6.0
P3.2
P3.3
P4.1
P4.3
P1.5
P4.6
P6.5
P6.4
P6.1
P4.0
P4.2
P4.4
P4.5
P4.7
P5.4
P5.5
P2.7
P2.6
P2.4
P5.6
P6.6
P6.7
P2.3
P5.1
P3.5
P3.7
P2.5
P3.0
P5.7
P1.6
P1.7
P5.0
P5.2
P3.6
Red P1.0
Red P2.0
Green P2.1
Blue P2.2
LED1
LED2
TI LaunchPad™
V+
V-
J10
J9

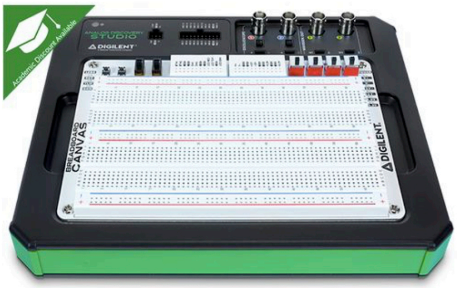
9.4 Survey

A survey was given out to 30 upper division EE and CPE students at Cal Poly SLO to gauge project interest and desired requirements. The survey was administered on 9/28/19 to 9/30/19. The following pages show the blank survey questions. The pages after that show the results.

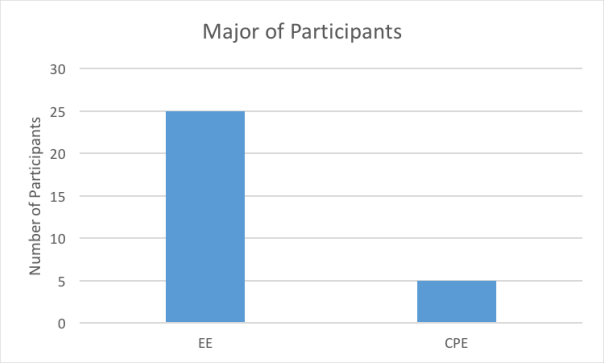
Major: _____	**Year:** _____

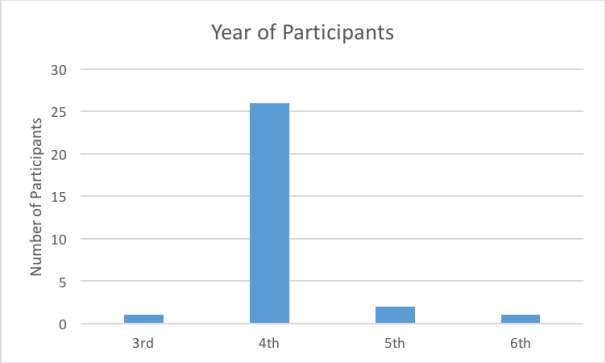
1a)	**Do you own a power supply?**	Yes	No
1b)	**If not, have you considered buying a power supply in the past?**	Yes	No
1c)	**If yes, what is the voltage range of it?** _____		
2)	**Do you own a multimeter?**	Yes	No
3)	**Do you own a breadboard?**	Yes	No
4a)	**Do you own an SMU (Source Measure Unit)?**	Yes	No
4b)	**Are you familiar with the practical usage of an SMU?**	Yes	No
5a)	**Have you ever been unable to access a power supply/multimeter/SMU for any reason(s)?**	Yes	No
5b)	**If yes, what were the reason(s)?** _____		
6)	**Do you set the current limit when using power supplies/SMUs?**	Yes	No
7)	**Is having an ohmmeter in the lab important to you?**	Yes	No

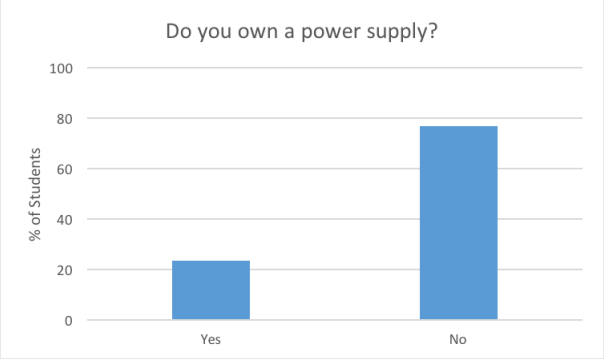
8)	**What is the *minimum* voltage range you would want from a power supply?** (circle one)	0V to +5V	-5V to +5V	-12V to +12V	-20V to +20V	Don't Know/ Care
9)	**What is the *lowest maximum* current you would want from a power supply?** **That is, what kind of currents would you want a power supply to be capable of outputting.** (circle one)	<50 mA	100 mA	500 mA	>1A	Don't Know/ Care
10)	**What is the minimum voltage resolution you would want from a multimeter?** (circle one)	<10 µV	50 µV	200 µV	>1mV	Don't Know/ Care
11)	**What percent error would you want on an ohmmeter?** (circle one)	<1%	5%	10%	>20%	Don't Care

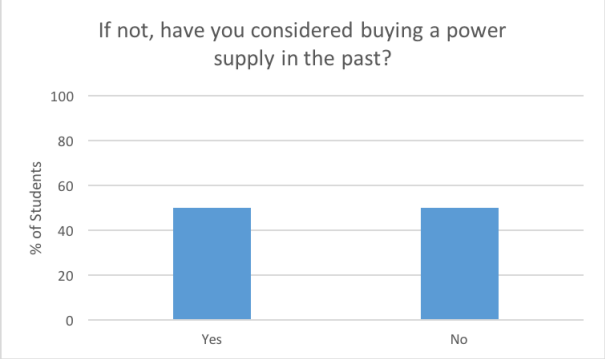
12)	What would you say you spent the majority of time in upper division electronics labs doing? **(Debugging, building circuits, taking measurements, ect)**		
13)	If you were to buy a box with **Power Supplies, SMU, Multimeter, and Sweep and Go-esqe Measurement functionality**, what would you consider paying for it? Consider that a typical ±12V 5A power supply costs **~$40-$80** and a cheap multimeter costs **~$30-50.**		
14)	**Are you familiar with either of these devices?** **(choose one option)**  	The top one only	Both of them
		The bottom one only	Neither of them
15)	If I were to tell you that both of those devices could comfortably replace an entire lab bench **(Power supply, Oscilloscope, Function Generator, Spectrum Analyzer, Logic Analyzer, ...),** how much would you say each one costs? (The bottom one has much better performance and built in breadboard)	Top: $_____	Bottom: $_____

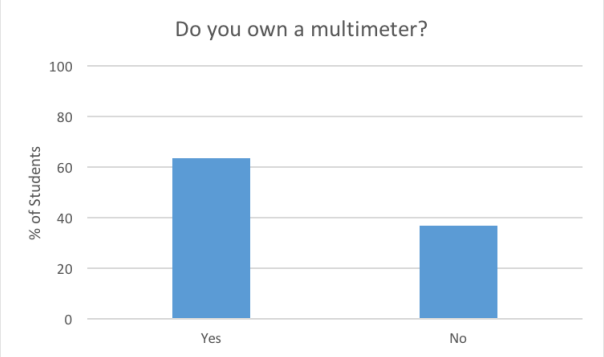
Was any part of this survey confusing?	
Write any miscellaneous comments here.	

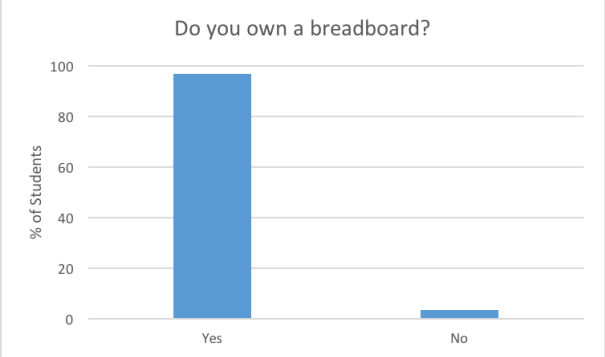

Major of Participants
Number of Participants
30
25
20
15
10
5
0
EE
CPE

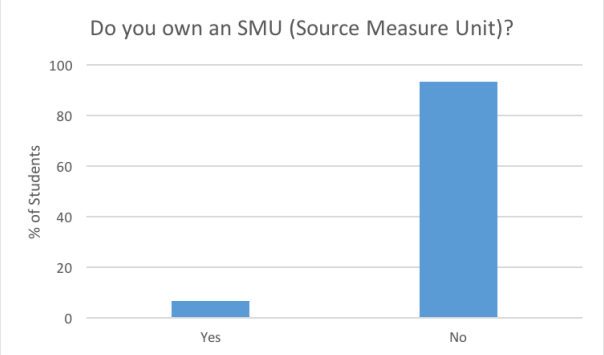

Year of Participants
Number of Participants
30
25
20
15
10
5
0
3rd
4th
5th
6th

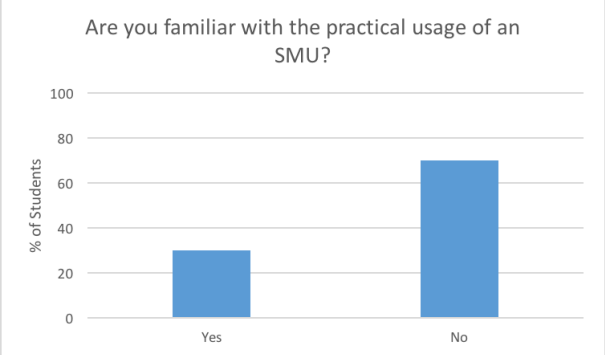

Do you own a power supply?
% of Students
100
80
60
40
20
0
Yes
No

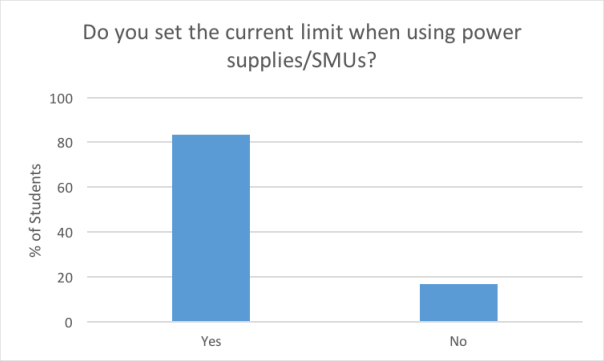

If not, have you considered buying a power supply in the past?
% of Students
100
80
60
40
20
0
Yes
No

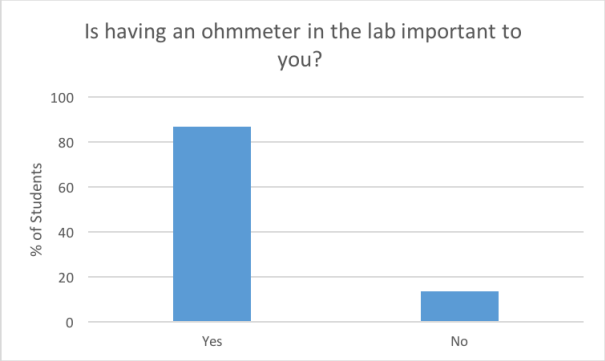

Do you own a multimeter?
% of Students
100
80
60
40
20
0
Yes
No

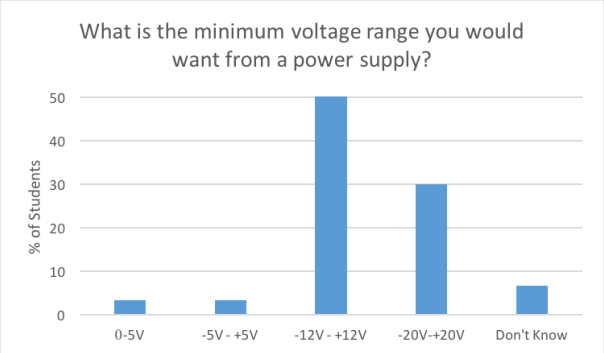

Do you own a breadboard?
% of Students
100
80
60
40
20
0
Yes
No

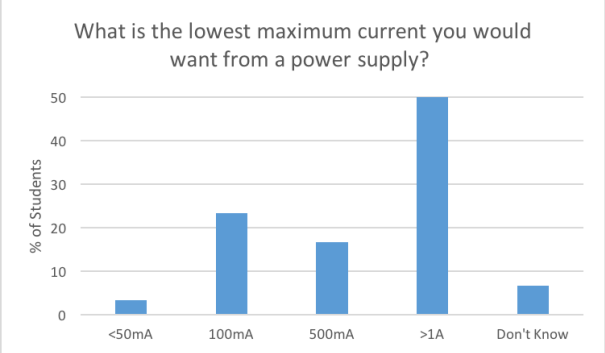

Do you own an SMU (Source Measure Unit)?
% of Students
100
80
60
40
20
0
Yes
No

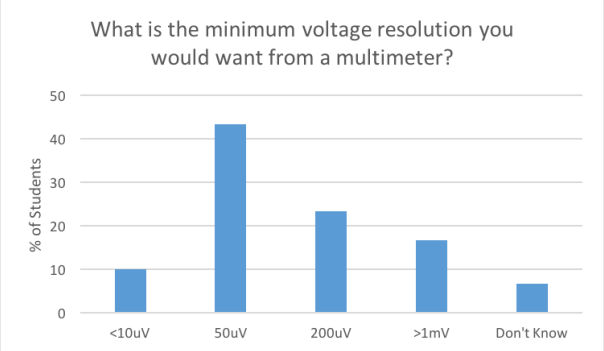

Are you familiar with the practical usage of an SMU?
% of Students
100
80
60
40
20
0
Yes
No

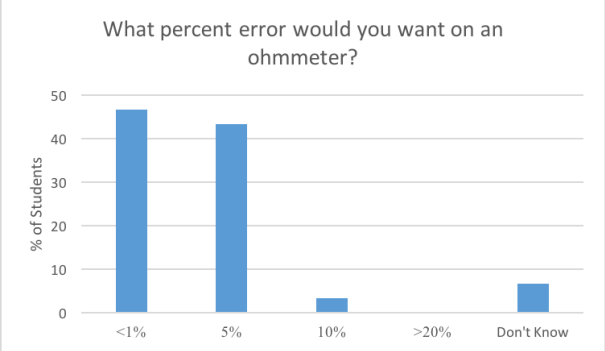

Do you set the current limit when using power supplies/SMUs?
% of Students
100
80
60
40
20
0
Yes
No


Is having an ohmmeter in the lab important to you?
% of Students
100
80
60
40
20
0
Yes
No


What is the minimum voltage range you would want from a power supply?
% of Students
50
40
30
20
10
0
0-5V
-5V - +5V
-12V - +12V
-20V-+20V
Don't Know


What is the lowest maximum current you would want from a power supply?
% of Students
50
40
30
20
10
0
<50mA
100mA
500mA
>1A
Don't Know

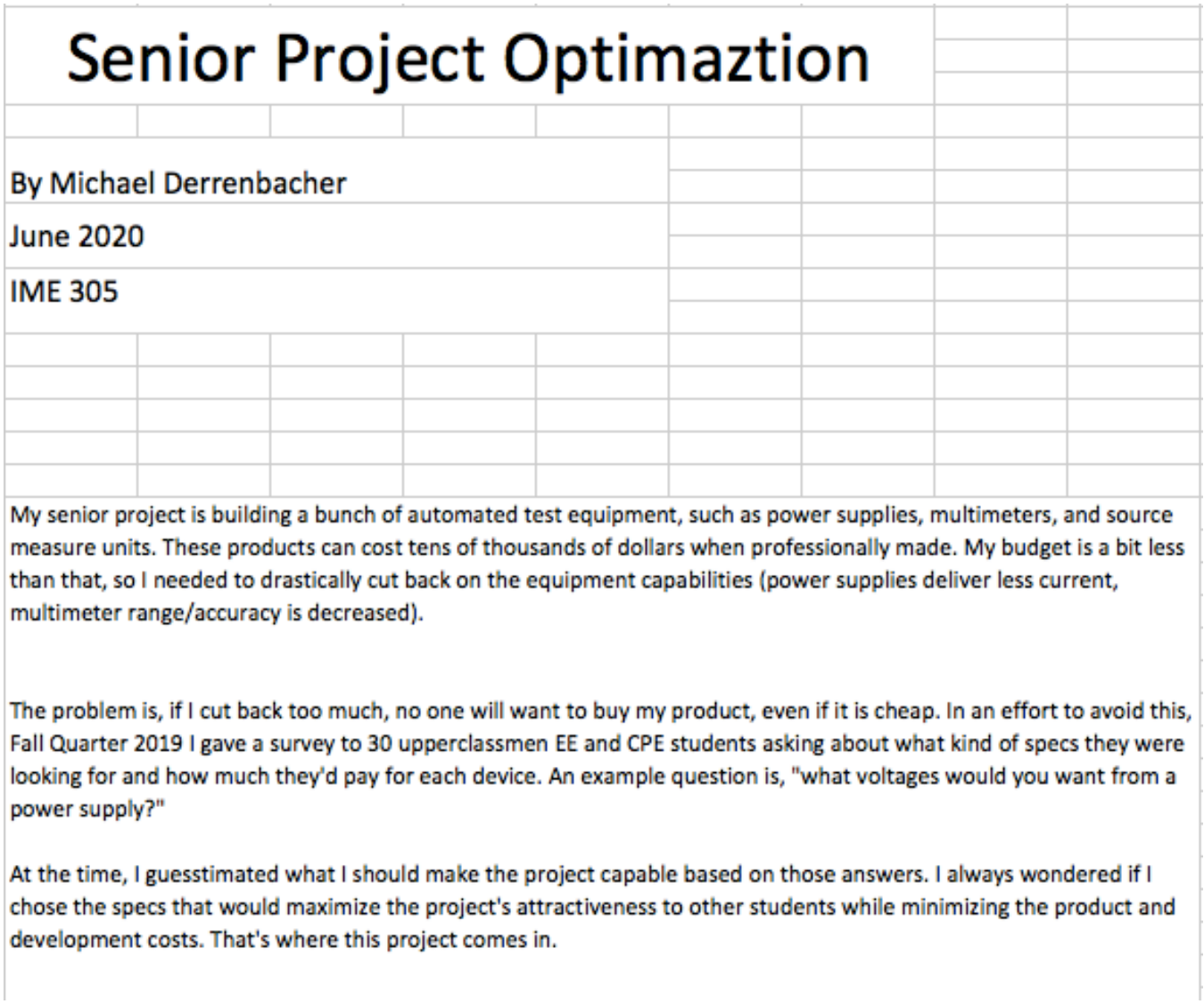

What is the minimum voltage resolution you would want from a multimeter?
% of Students
50
40
30
20
10
0
<10uV
50uV
200uV
>1mV
Don't Know


What percent error would you want on an ohmmeter?
% of Students
50
40
30
20
10
0
<1%
5%
10%
>20%
Don't Know


Desired Price for Product
% of Students
50
45
40
35
30
25
20
15
10
5
0
$0-$25
$25-$50
$50-$75
$75-$100
$100-$125
$125-$150
$150-$175
$175-$200
$200-$225
$225-$250
$250-$275
$275-$300
$300-$325

9.5 Survey Optimization and Analysis

For a Operations Research II project, the author themed it after his senior project survey. The following images show the excel workbook with text commentary.



Senior Project Optimaztion

By Michael Derrenbacher

June 2020

IME 305

My senior project is building a bunch of automated test equipment, such as power supplies, multimeters, and source measure units. These products can cost tens of thousands of dollars when professionally made. My budget is a bit less than that, so I needed to drastically cut back on the equipment capabilities (power supplies deliver less current, multimeter range/accuracy is decreased).

The problem is, if I cut back too much, no one will want to buy my product, even if it is cheap. In an effort to avoid this, Fall Quarter 2019 I gave a survey to 30 upperclassmen EE and CPE students asking about what kind of specs they were looking for and how much they'd pay for each device. An example question is, "what voltages would you want from a power supply?"

At the time, I guesstimated what I should make the project capable based on those answers. I always wondered if I chose the specs that would maximize the project's attractiveness to other students while minimizing the product and development costs. That's where this project comes in.

For this model I assigned each answer a time cost, fiscal cost, and value number.

The time cost is a number that estimates how many hours it'd take to design and verify a given spec.

Fiscal cost is how expensive it would be to implement.

Value number is the percentage of people that would like to see that spec implemented.

For example, making the power supply source only low currents would have a small time cost, small fiscal cost, and a small value number. A power supply that sources high currents would have a medium time cost, high fiscal cost, and a value number of 100%.

I will have to guesstimate the time and fiscal costs, but as I already built the project I can make decent educated guesses based on my current costs. The fixed costs come from a standard PCB order from JLCPCB.

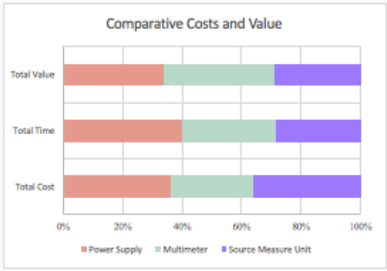
Equation to optimize:
Value * 1000 - (Time + Cost)
(Value * 1000 to get on same order as time/cost for easy comparison)

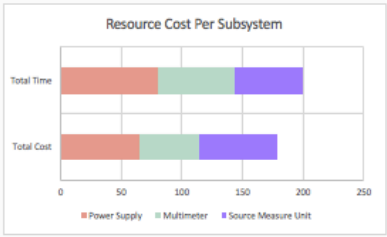
Subsytem	Spec	Range	Time Cost (hours)	Fiscal Cost ($)	Value Number (%)
Power Supply	Fixed Cost	Make	20	25	0.333
		Don't Make	0	0	0.000
	Output Voltage	0 — 5V	4	3	0.036
		-5 — +5V	10	6	0.071
		-12 — +12V	15	15	0.678
		-20 — +20V	25	30	1.000
	Output Current	<50mA	2	3	0.036
		<100mA	10	10	0.286
		<500mA	20	20	0.464
		>1A	30	40	1.000
Multimeter	Fixed Cost	Make	30	25	0.333
		Don't Make	0	2	0.000
	Number of Output Channels	1	5	4	0.631
		2	6	8	0.865
		3	6	12	0.950
		4	6	16	1.000
	Number of Input Channels	1	5	7	0.631
		2	6	9	0.865
		3	6	17	0.950
		4	7	18	1.000
	Voltage Resolution	>1mV	5	5	0.179
		200µV	7	7	0.429
		50µV	10	13	0.893
		<10µV	25	35	1.000
Source Measure Unit	Fixed Cost	Make	40	30	0.334
		Don't Make	0	0	0.000
	Output Voltage	0 — 5V	4	3	0.036
		-5 — +5V	10	6	0.071
		-12 — +12V	15	15	0.678
		-20 — +20V	30	32	1.000
	Output Current	<50mA	2	3	0.500
		<100mA	10	12	0.750
		>500mA	25	34	1.000

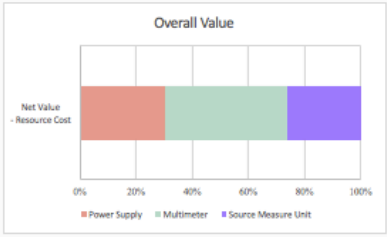
Goals	
Maximum Hours to Work:	200
Maximum Budget in Dollars:	200
Must Make Power Supply (1/0)	0
Must Make Multimeter (1/0)	0
Must Make Source Measure Unit (1/0)	0
Must Satisfy at least x Percent of Power Supply Wants	0
Must Satisfy at least x Percent of Multimeter Wants	0
Must Satisfy at least x Percent of Source Measure Unit Wants	0

Solve

Results	Money Spent Time Spent	$200 179 Hours
Power Supply	Output Voltage	-12 — +12V
	Output Current	>1A
Multimeter	Number of Outputs	4
	Number of Inputs	3
	Voltage Resolution	200µV
Source Measure Unit	Output Voltage	-12 — +12V
	Output Current	<100mA







Variables				Time			Money			Value		
Make PS	V Range	C Range		Make PS	V Range	C Range	Make PS	V Range	C Range	Make PS	V Range	C Range
1	0	0		20	4	2	25	3	3	0.333	0.03567	0.03567
	0	0			10	10		6	10		0.071357	0.285678
	1	0			15	20		15	20		0.678492	0.464249
	0	1			25	30		30	40		1	1

					Time Cost	Fiscal Cost	Value
1	<=	1	Choose 1 V range		65	80	0.279469
1	<=	1	Choose 1 C range				
0	=	0	All or nothing				
					134.468918		

VLOOKUP Stuff		
0	0 — 5V	-12 — +12V
0	-5 — +5V	
1	-12 — +12V	
0	-20 — +20V	
0	N/A	
0	<50mA	>1A
0	<100mA	
0	<500mA	
1	>1A	
0	N/A	

Variables				Time				Money				Value			
fake Multimeter	Output	Input	Res	Make	Output	Input	Res	Make	Output	Input	Res	Make	Output	Input	Res
1	0	0	0	30	5	5	5	25	4	7	5	0.333	0.631	0.631	0.17857
	0	0	1		6	6	7		8	9	7		0.8646	0.865	0.42857
	0	1	0		6	6	10		12	17	13		0.95	0.95	0.89285
	1	0	0		6	7	25		16	18	35		1	1	1

					Time Cost	Fiscal Cost	Value
1	<=	1	Chose 1 Output		49	63	0.306121
1	<=	1	Choose 1 Input				
1	<=	1	Choose 1 Res				
0	=	0	All or nothing				
					194.12135		

VLOOKUP Stuff		
0	1	4
0	2	
0	3	
1	4	
0	N/A	
0	1	3
0	2	
1	3	
0	4	
0	N/A	
0	>1mV	200μV
1	200μV	
0	50μV	
0	<10μV	
0	N/A	

Variables				Time			Money			Value		
Make SMU	V Range	C Range		Make	V Range	C Range	Make	V Range	C Range	Make	V Range	C Range
1	0	0		40	4	2	30	3	3	0.334	0.03567	0.5
	0	1			10	10		6	12		0.071357	0.75
	1	0			15	25		15	34		0.678492	1
	0				30			32			1	

					Time Cost	Fiscal Cost	Value
1	<=	1	Choose 1 V range		65	57	0.238558
1	<=	1	Choose 1 C range				
0	=	0	All or nothing				
					116.558164		

VLOOKUP Stuff		
0	0 — 5V	-12 — +12V
0	-5 — +5V	
1	-12 — +12V	
0	-20 — +20V	
0	N/A	
0	<50mA	<100mA
1	<100mA	
0	>500mA	
0	N/A	

179	<=	200	**Total Time**	445.1484
200	<=	200	**Total Cost**	
82.415	>=	0	**Total Value**	
83.925	>=	0	**PS Value**	
91.928	>=	0	**Multi Value**	
71.425	>=	0	**SMU Value**	
1	>=	0	**Force PS**	
1	>=	0	**Force Multi**	
1	>=	0	**Force SMU**	

Results	Money Spent Time Spent	$200 179 Hours	Actual	
Power Supply	Output Voltage	-12 — +12V	-12 — +12V	On Target
	Output Current	>1A	200mA	Below
Multimeter	Number of Outputs	4	4	On Target
	Number of Inputs	3	4	Above
	Voltage Resolution	200µV	50µV	Above
Source Measure Unit	Output Voltage	-12 — +12V	-10 — +10V	~On Target
	Output Current	<100mA	100mA	On Target

For the most part, the actual specifications were fairly close to the 'optimized' variants. I tried to ensure that I was meeting demand during the design phase.

For the Output Current spec, I mostly ignored the survey results. I framed the question poorly. I should have asked what the most current a student needed for a undergraduate lab experiment. The electronics lab experiments don't need that much current. If someone wanted a general use power supply however, they might need all that current (motor control, heating elements, powering larger boards, ...). Overall the survey responses were skewed disproptionally high. That is why I settled on a much lower value of 200mA.

For the number of inputs, I agree with the optimization, very few circuits will need more than 3 voltage readings at once. Adding an additional input is likely not worth the cost. However, lots of components come with powers of two channels (1 channel, 2 channels, 4 channels, 8 channels, ...). While it might be optimal to only have 3 channels, it would be clunkier to set up.

The voltage resolution whas the the final discrepant spec. Again, this was mainly from me ignoring the survey. I wanted to have a really good multimeter, so I made one. Maybe it wasn't the most efficient use of reasources but it was still something I personally wanted to do.

9.6 Code

In a feeble attempt to prevent this report from being too long, all project code is hosted on a public repository.

https://github.com/MichaelDerrenbacher/DC_Treasure_Box

9.7 Demo Video

A short video explaining and demonstrating the project's capabilities:

https://www.youtube.com/watch?v=YxIDweSyTQg&feature=youtu.be

Make sure to rate, like, follow, donate, comment, and subscribe.

9.8 Experiments

9.8.1 BJT Thermometer Viability

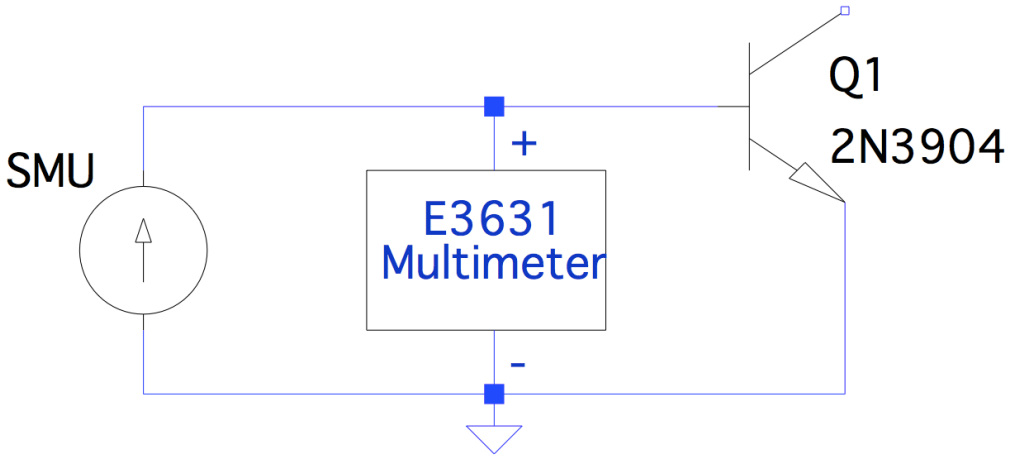


Figure 9.1. Test Setup for Generating I-V Curve

One of the main goals of project is to characterize semiconductors. The SMU in constant current mode is a perfect way to measure the current/voltage characterize of a diode connected BJT. Figure 9.1 shows the test setup. The SMU sweeps current from 0.2445mA to 10.0245mA, with a step size of 0.2445mA. This step is the smallest change in current value the SMU can output without quantization error. V_{BE} is recorded at each step.

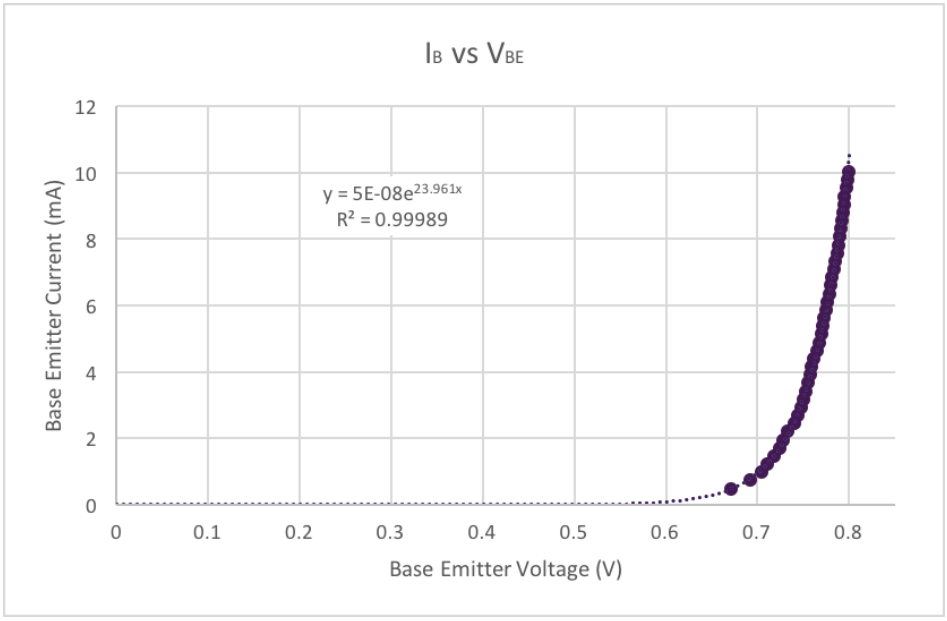


Figure 9.2. I-V Curve (Zoomed Out)

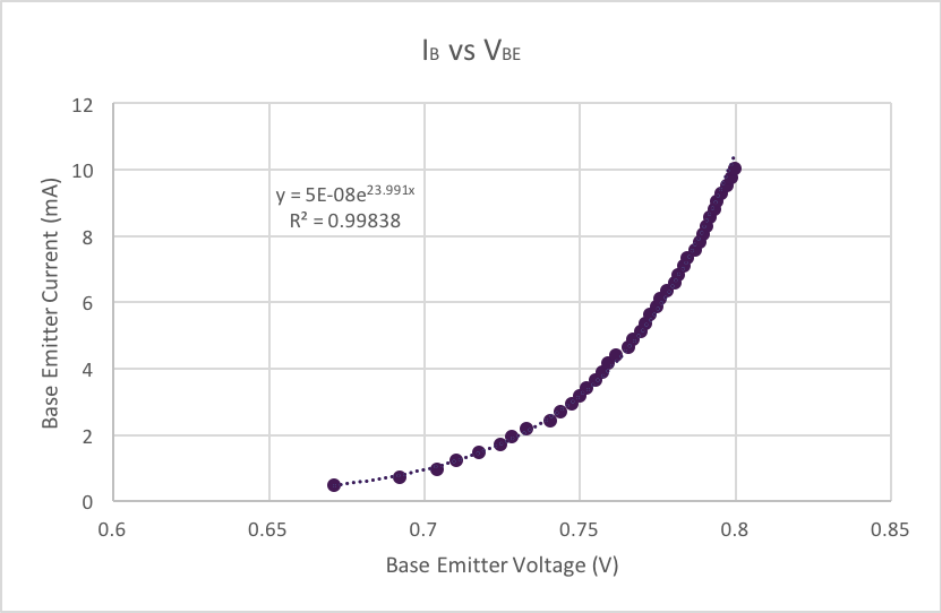


Figure 9.3. I-V Curve (Zoomed In)

Figures 9.2 and 9.3 show the plotted data along with an exponential trendline fit. The SMU proves to be a viable way of generating IV curves. Out of curiousity, the author wanted to know if the trendline equation could be used to figure out the temperature of his room. Equation 17 shows the ideal diode equation.

$$I_D = I_O(e^{\frac{qV_{BE}}{nkT}} - 1) \tag{17}$$

Where:

I_D is Diode Current
I_O is Reverse Saturation Current
V_{BE} is Base-Emitter Voltage
V_{BE} is Base-Emitter Voltage ($\sim 1.602 * 10^{19} Coulombs$)
k is Boltzmann's Constant ($\sim 1.381 * 10^{23} J/K$)
n is Ideality Factor (Ranges from 1 — 2)
T is Temperature in Kelvin

From figure 9.3 and equation 17, the measured reverse saturation current is 50nA. Equation 18 shows the exponential parts of the ideal diode equation and the trendline. Because only n and T are variables, setting n equal to 1 and 2 will show the upper and lower bounds of T. This will be the range of temperatures the room will fall under.

$$23.991 = \frac{q}{nkT} \tag{18}$$

$$T = \frac{1.602 * 10^{19}}{1.381 * 10^{23} * 23.991 * n} \tag{19}$$

$$T = \frac{483.527}{n} \tag{20}$$

From equation 20, the temperature range can be solved for by plugging in the edge cases of n, 1 and 2.

$n = 1$: $T = 483.527$ K

$n = 2$: $T = 241.763$ K

Therefore it can be said with near certain confidence that the temperature of the author's room was between -24.5 and 410.7 °F. A guesstimate of 65°F falls nicely within these bounds. This method successfully archives thermometer functionality. The author sheds a single tear of pride.

9.8.2 Output Voltage Limitations Sweep

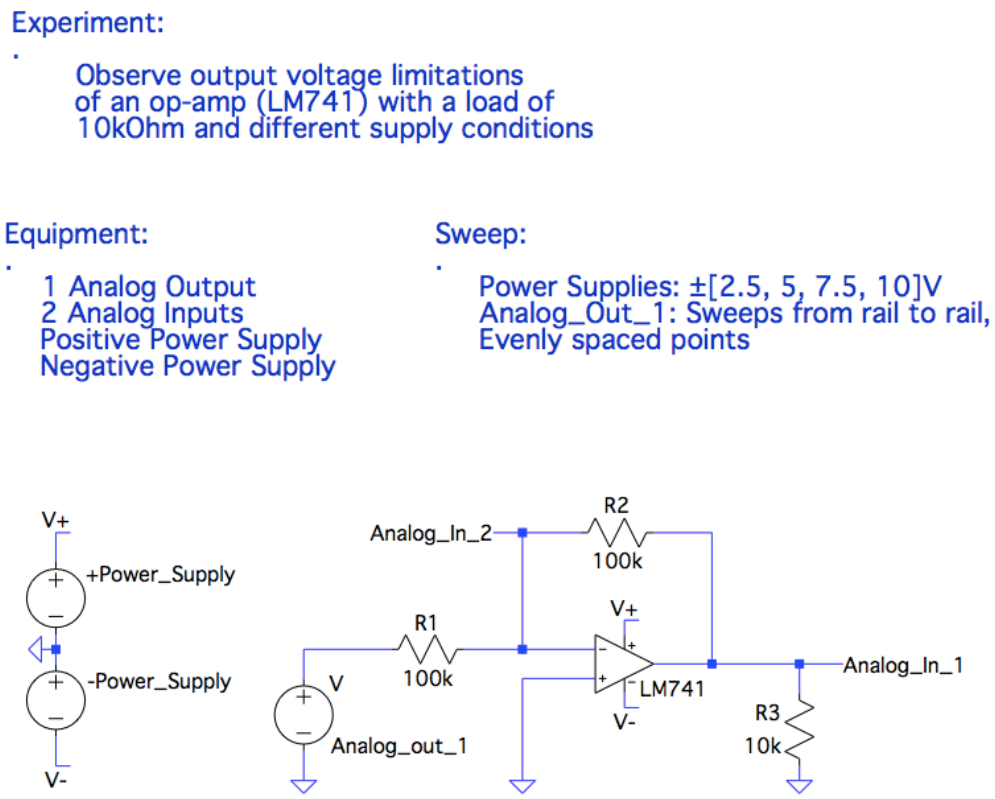


Figure 9.4. Test Setup for Measuring Output Voltage Swing

To test the sweeping functionality, a simple unity gain inverting amplifier is built. Figure 9.4 shows the circuit in question. The power supplies are set at: ±2.5V, ±5V, ±7.5V, and ±10V. The analog output sweeps values from the negative to positive supply rails. Theoretically, this results in the output voltage of the op-amp under test to slew from one power supply voltage to the other. However, in practice some op-amps saturate before reaching the power rails. The LM741 is an ancient op-amp that can not achieve rail-to-rail output. The measurement sweeps determine the valid output voltage range for the LM741 under different supply conditions. The load resistance of 10kΩ is kept constant, but can vary to further characterize the op-amp.

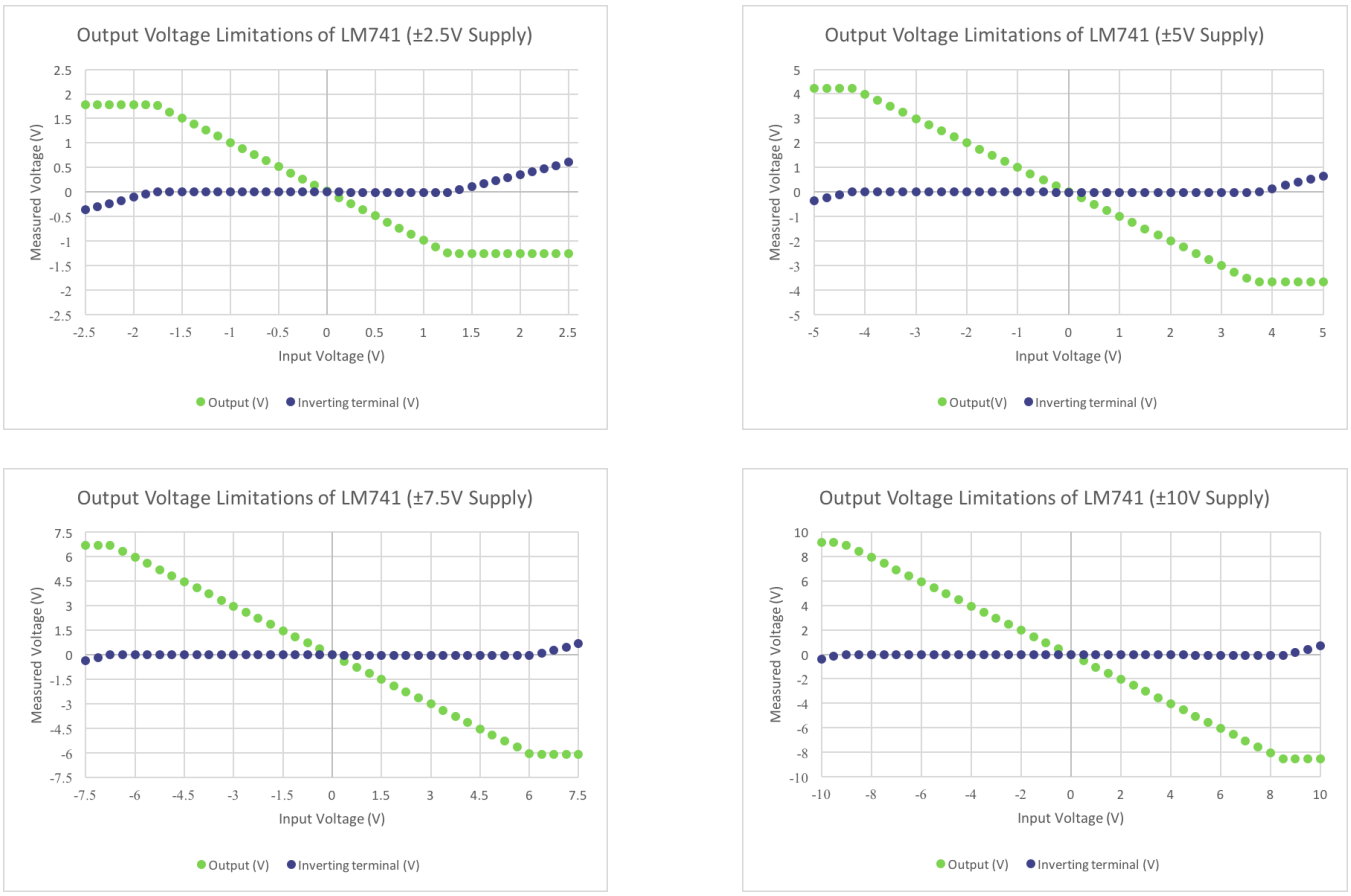


Figure 9.5. Op Amp Sweeps

Figure 9.5 shows how the LM741 op-amp can not output voltages close to its supply rails.

9.8.3 Diff-Pair Voltage Sweep

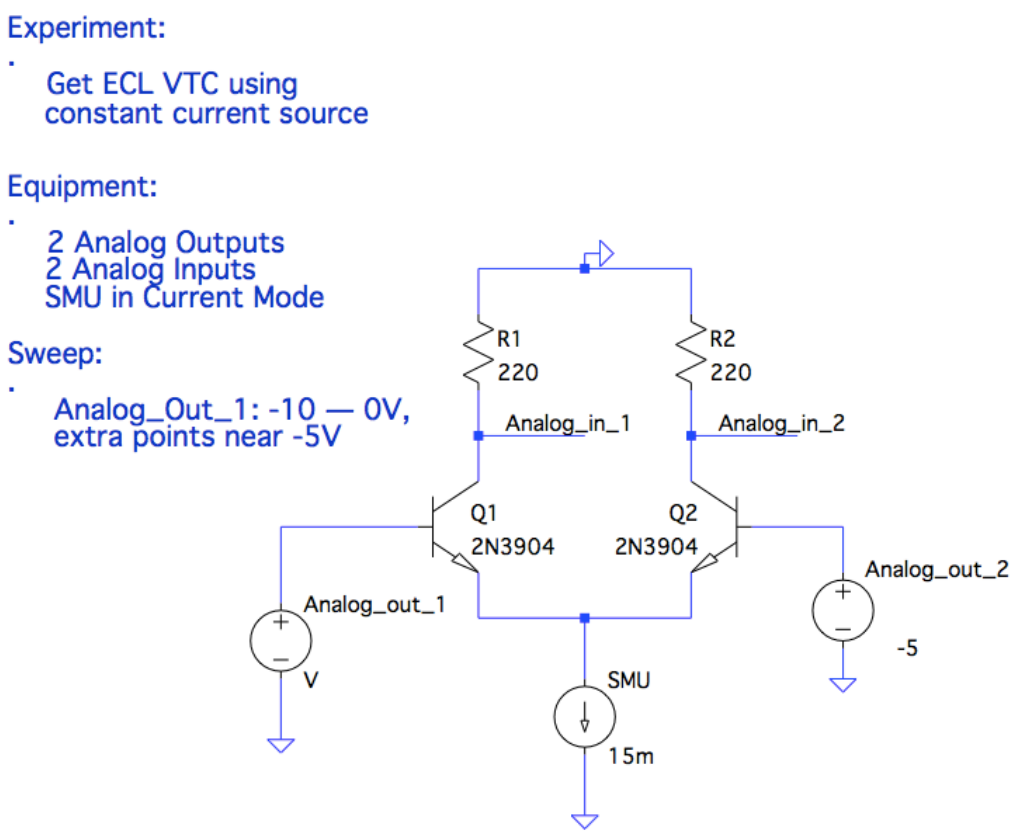


Figure 9.6. Test Setup for Measuring Differential Pair Transfer Characteristics

Another experiment to test the full-system integration is to measure the transfer characteristics of a Differential Pair. The power supply, analog input/output, and SMU are all necessary to test this the circuit in figure 9.6. This diff-pair represents a possible input stage of an ECL (Emitter Coupled Logic) Gate.

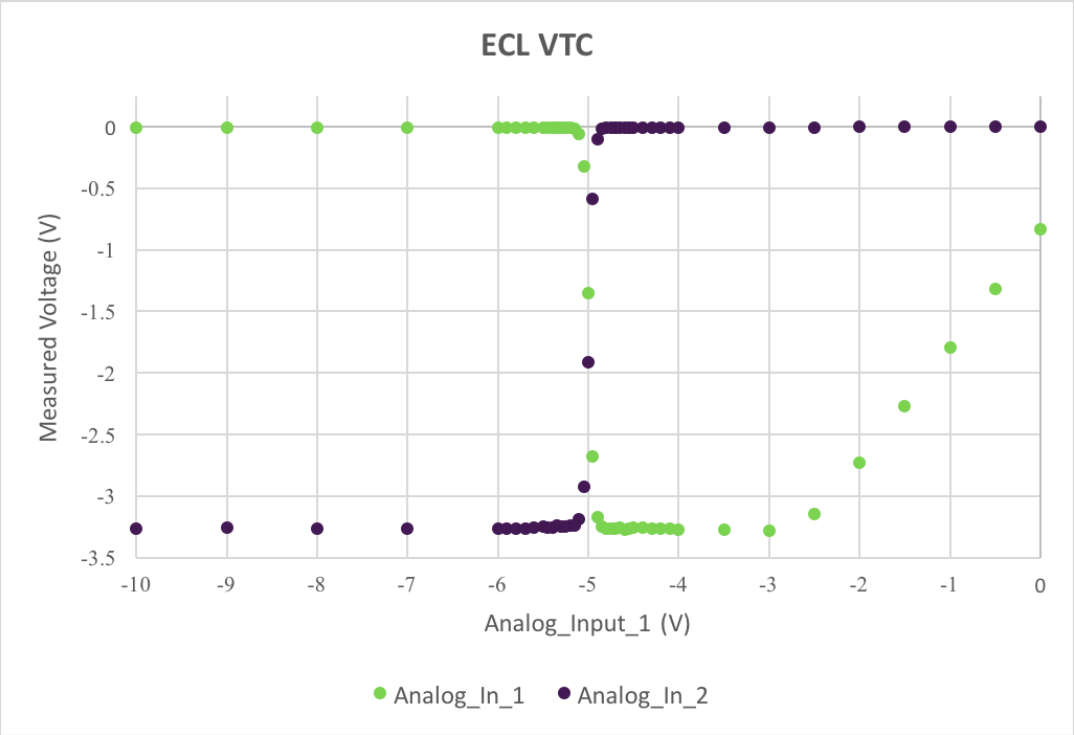


Figure 9.7. ECL Voltage Transfer Characteristic

Figure 9.7 shows the two logic levels of the ECL gate, the narrow transition region, and the effect of Q_1 saturating at higher input voltages.

9.8.4 Common Emitter Sweep

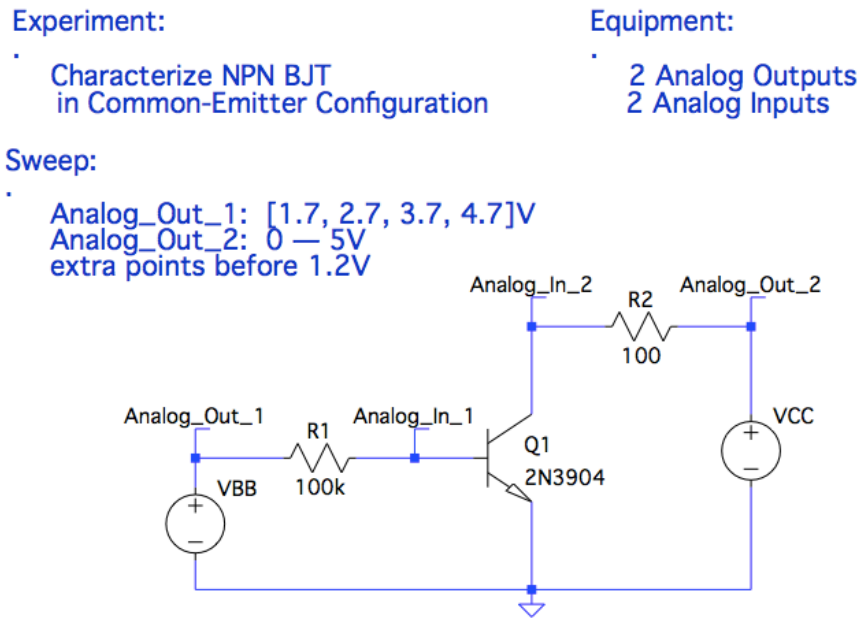


Figure 9.8. Test Setup for Measuring Common Emitter Characteristics with Different Base Currents

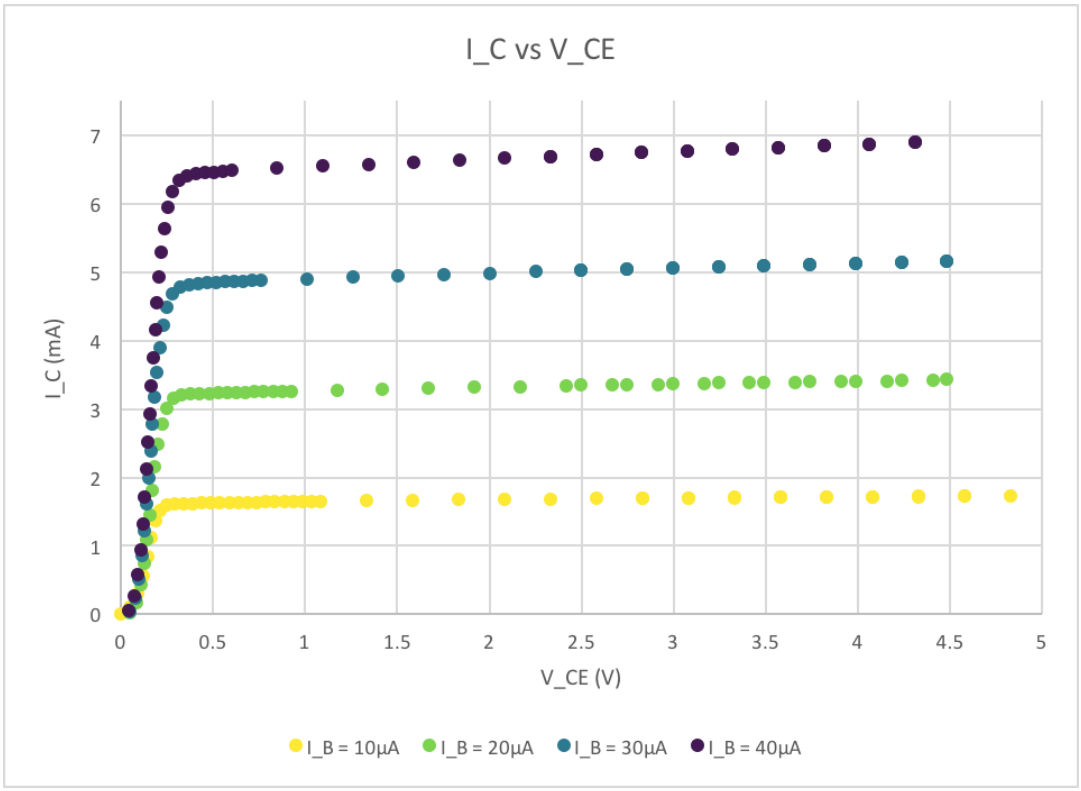


Figure 9.9. Test Setup for Measuring Common Emitter Characteristics with Different Base Currents

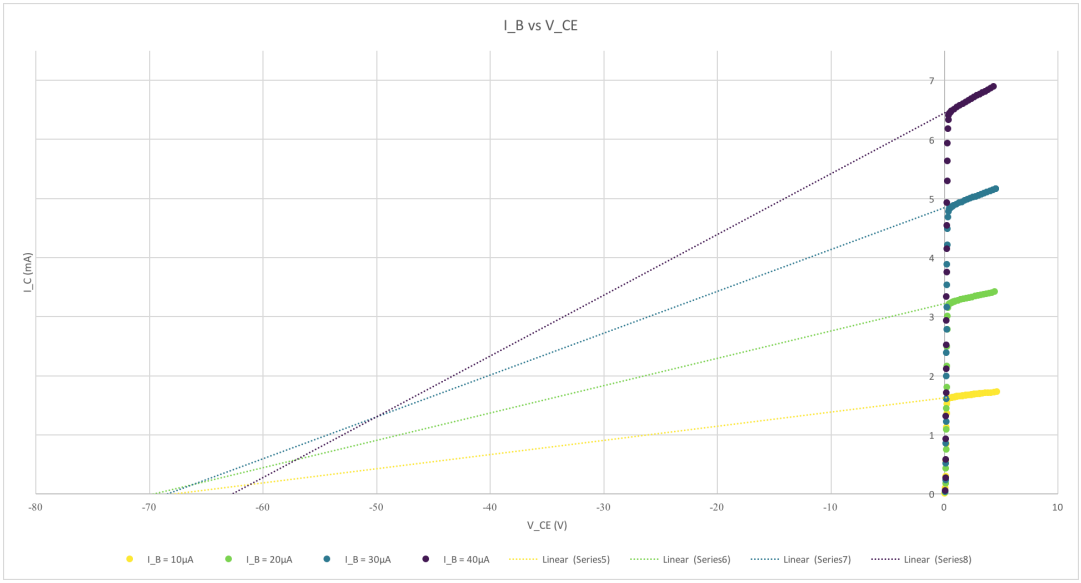


Figure 9.10. Using Effective-Base-Width Modulation to Extrapolate Early Voltage

9.8.5 Current Mirror Sweep

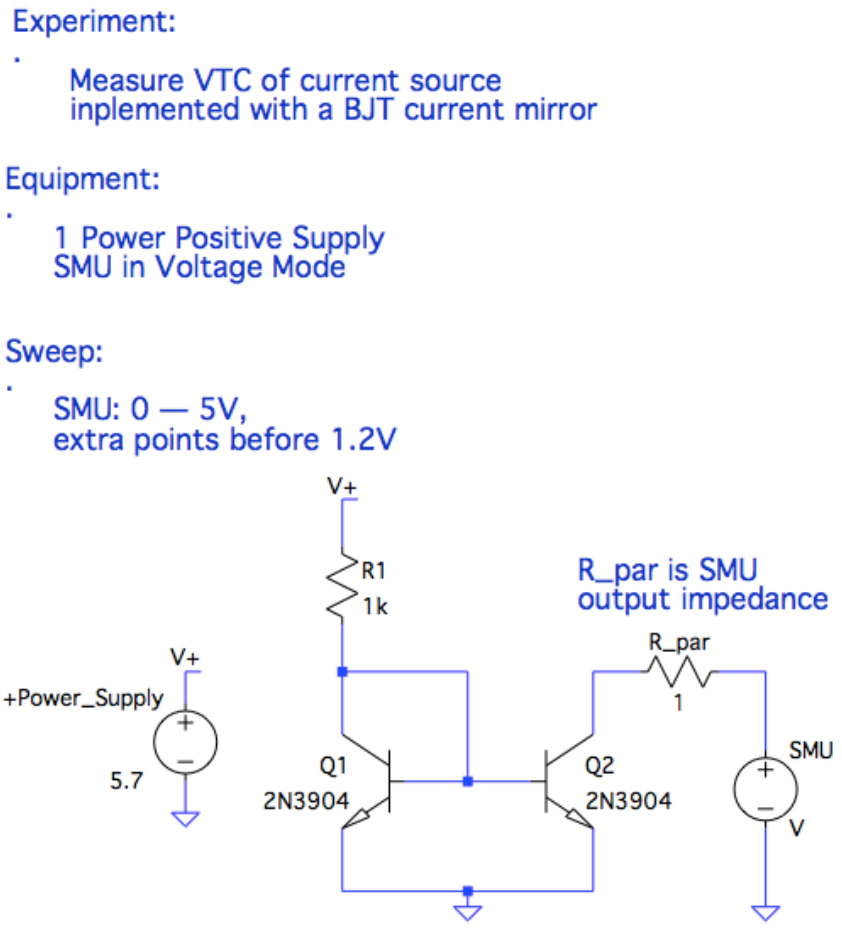


Figure 9.11. Test Setup for Measuring Current Mirror Characteristics

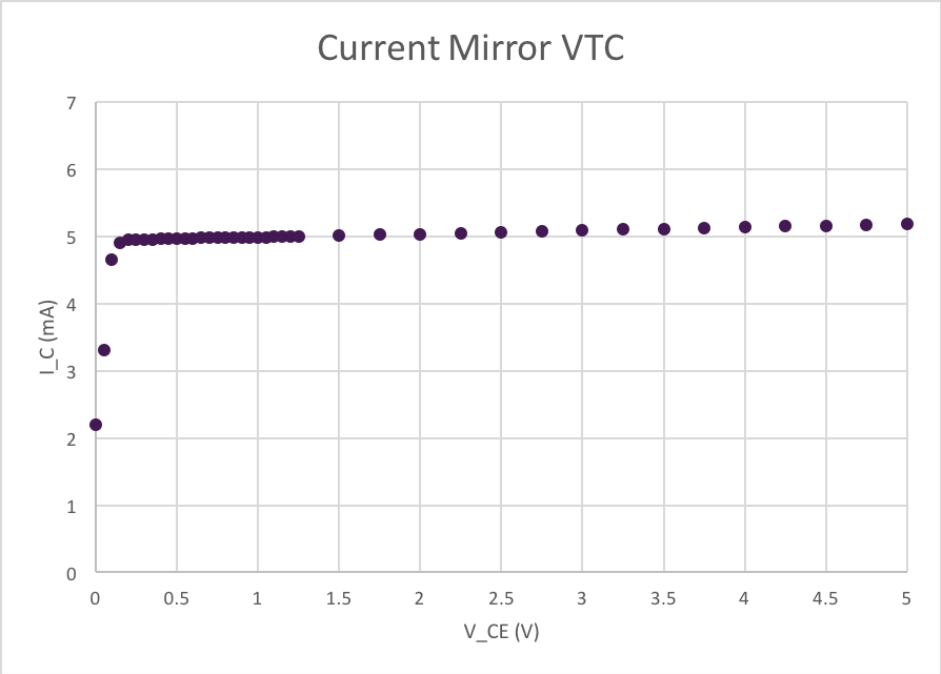


Figure 9.12. Measured Current Mirror Current vs Input Voltage

9.9 ABET Analysis

9.9.1 Summary of Functional Requirements

The project has 4 main subsystems: power supplies, analog input/outputs (AIO), digital input/outputs (DIO), and a source measure unit (SMU). Each subsystem is autonomous and can coordinate measurement sweeps. For example, a program can set the power supplies to ±5V, sweep a analog output from 0-5V in 0.1V increments, measure up to four node voltages, and repeat at a different supply voltage.

The power supply subsystem has 3 output channels. Two channels are 0 – 12V, and the other is -12 – 0V. Each channel can supply up-to 200mA. Each channel has adjustable over current protection.

The SMU subsystem has one output channel. The SMU can source current and measure voltage, and can force voltage and measure current. The SMU supplies up to ±10V and ±100mA. It has overvoltage and overcurrent protection. These protections put the SMU into either constant voltage or constant current current mode.

The analog input output subsystem has 4 inputs and 4 outputs. Each input accepts -10 – 10V. Two outputs are -5 – 5V, and 2 are -10 – 10V. The outputs can comfortably source 20mA without significant voltage error.

The digital input output subsystem has 4 inputs and 4 outputs. Each input accepts 0 – 5V. The input digitization threshold is adjustable. Each output can emitter 0 – 5V. The output rise fall time is 2µs. The output voltage levels are adjustable.

9.9.2 Primary Constraints

Reducing costs as much as possible is the most difficult part of the project. In order to be desirable to the market, the product can not cost more than a few hundred dollars. For all of the functionality planned, achieving this goal is difficult.

Tables 2.2 - 2.5 show the specifications and marketing justification for each subsystem. These specifications are based on other lab equipment on the market.

The SMU is a complicated circuit that has many control loops and compensators integrated into it. Stabilizing the output while achieving the desired accuracy is a difficult task.

Interfacing to 6 different ADCs and DACs (analog to digital converter, digital to analog converter) is time consuming. Similar interface protocols are needed.

9.9.3 Economic

This product is manufactured capital. The value is inherent in the product itself, and is determined by the user. The material cost of the project is about $220, but the total value derives from the usefulness the project provides. A person that wants lab equipment will value this project.

The estimated time the project took to complete is 500 hours. Over the 8-month working period this equates to 15.625 hours per week, or 2.23 hours per day. If the author is paid a hourly salary of $40 per hour, he would need to pay himself $20k in compensation.

Additional costs accrue from software licensing fees. Other fixed costs come from lab equipment needed for project testing and verification.

Before the project is released, it needs testing for the most recent revision. This testing would delay the release date to roughly late 2020. The project is built to last at least four years; the entire time a student takes to complete an undergraduate degree. For continued accuracy, the project may require intermittent calibration.

"The project is estimated to take at least 300 hours to complete. This time factors in any learning done whilst researching viable relevant techniques and topologies. The largest time sink is the design and testing of the various subsystems. Many design considerations and though testing is needed to ensure that specifications are met." - the previous, naive version of the author.

The project has drained at least 500 hours of the author's life. The exact number isn't known as to avoid giving the author an existential crisis. The report writing, subsystem design, and component search were the major time sinks. - the current, jaded version of the author.

After the project ends the author gets his very own programmable portable lab box. The author plans to bring the box to bars around town in an attempt to pick up dates by telling them about the analog input accuracy specifications.

9.9.4 If manufactured on a commercial basis

The the actual project cost of $220 exceeded the original target cost of $200 by 10%. The author profits $30 per unit sold if the project sells for $250. After 667 units sell, the project sees overall profit.

At Cal Poly, there are roughly 710 EE students and 550 CPE students. Assuming one-forth of those students are freshman, 315 potential buyers enter the school each year. If only 2% of those students buy this project, it takes (only) about 105 years before profit occurs. If the selling price increases to $300, the estimated time till profit is 40 years.

Figures 9.13 and 9.14 show a plausible selling optimization. Figure 9.13 shows the likelihood that any one given person will buy the product. This curve is merely an estimate, if real data is sought, a year or two of actual data will generate numbers with some weight behind them. Figure 9.14 shows the optimal price to sell at given the buying likelihood data from figure 9.13.

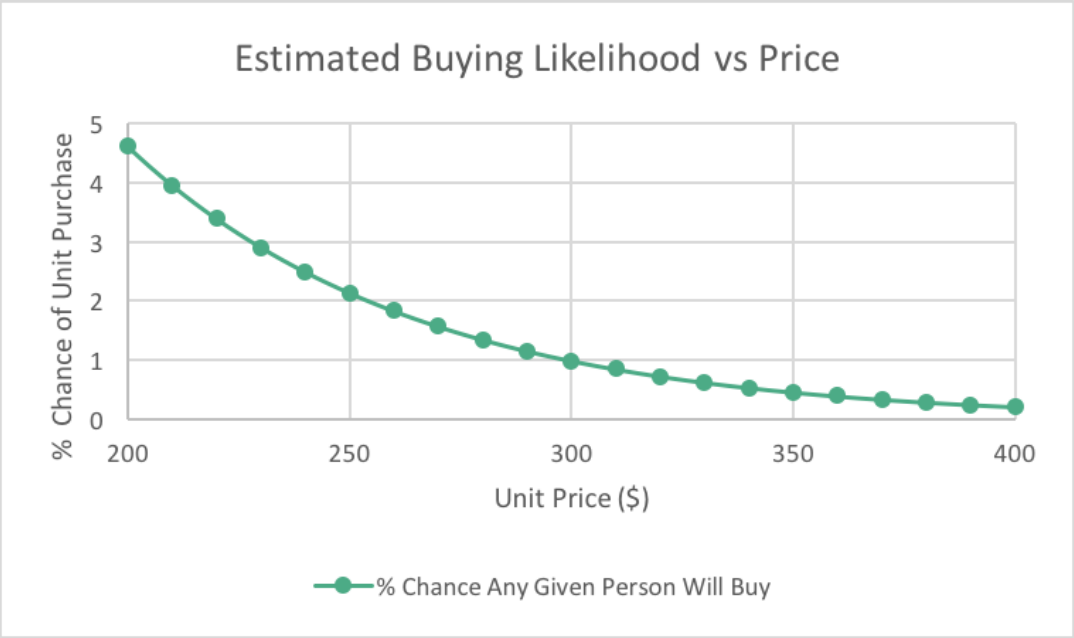


Figure 9.13. Estimated Likelihood Curve

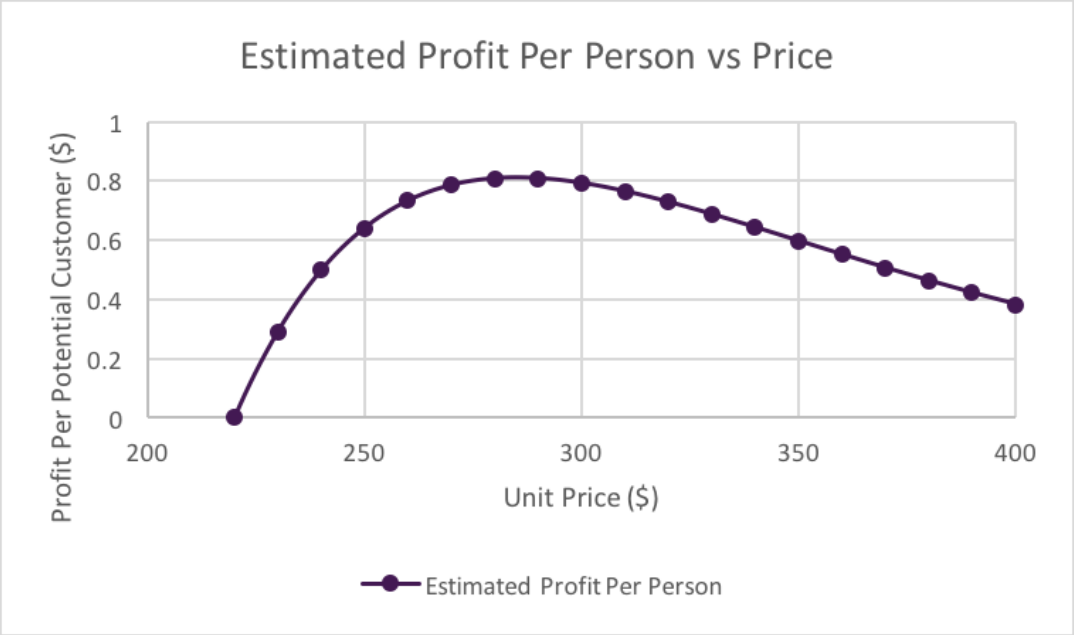


Figure 9.14. Optimization Curve

From figure 9.14, the best price to sell at is \$290, resulting in an average profit per person of \$0.808 per year. From these values the population needed to start to generate a net profit after 10 years is about 2500 people, Assuming Cal Poly is a normal sized school, the product requires marketing at about 8 college campuses of students to meet this population number.

9.9.5 Environmental

The construction of this product requires PCB boards fabrication, integrated circuit manufacturing, and mineral/metal mining. To minimize these potentially harmful actions, RoHS compliant parts are sought. This ensures that environmental laws are met in accordance when constructing this product.

The product directly requires mining of metal resources. These resources are used for the construction of the components and boards used in the product. The mining processes may cause considerable pollution and waste. The mining industry is responsible for the use of land, which may displace different species of animals. Pollution emitted as a result because of this product may be harmful to sea life and bird species.

The project also indirectly requires transportation of materials. This transportation likely uses fossil fuels which can negatively affect the environment.

The product does not directly influence natural resources or ecosystem services. When unloaded, the product dissipates about 2 Watts of power. This amount of consumption pales in comparison to other household devices. For reference, a typical television consumes roughly 90-110 Watts.

9.9.6 Manufacturability

The project generates heat as it dissipates power. The enclosure requires proper air ventilation. Without ventilation, the boards will get hotter, which may affect the accuracy of the project.

The project required calibration before it reached the desired accuracy. An automated calibration suite is necessary for large scale production.

The output wires on the PCBs do not have strain relief. Overtime the wire connections will degrade and inhibit performance. Better connectors are needed before production.

9.9.7 Sustainability

No foreseen maintenance costs are associated with the product. The product is designed to be self-contained, and does not need servicing. Calibration may be required to continually achieve accuracy specifications.

Future additions toward this project include AC capabilities (oscilloscope, function generator). AC capabilities would greatly increase the attractiveness of the product to the target market. These functionalities would turn the product into a full-fledged portable lab bench. Other points of improvements are beefier power supplies and SMU output. Because the project is fully modular, so long as a board communicates with SPI and can take any combination of +3.3V, +5V, +15V, and -15V as power, it can freely replace any of the base boards. This expandability makes further work simple and isolated.

If someone (that means you, person reading this) wants to inherit this project, the author has some recommendations for future work. For AC functionality, The product would need to either speed up the microcontroller (currently runs at a lackadaisical 3MHz) or use a faster one. A dedicated board with fast ADCs and potentially EEPROM for waveform memory is a starting point. Some sort of non-terminal

display is also required. As far as other improvements are concerned, the errata section of this report details mistakes the author encountered. One idea the author had for the power supply was to have an adjustable switching mode supply followed by an adjustable linear regulator. This would be much more efficient than the current implementation of just the linear regulator. Temperature control is another avenue of improvement, especially for the SMU.

9.9.8 Ethical

"to be honest and realistic in stating claims or estimates based on available data;" -IEEE Code of Ethics

The primary ethical concern stemming from this project is the validity of the data reported. The author attests that all data and experimentation is done without modification. No skewing or fudging of any data occurred during the duration of the project. The author believes that simulation of subsystems working give some credibility to the overall design. Video evidence of data sweeps also contribute toward the overall validity.

A few product specifications changed over the course of the project. The author's inexperience with complete engineering projects necessitated these modifications. These changes are articulated in the design and testing sections of the report. Notable changes include the accuracy of power supplies, analog inputs/outputs, and SMU; as well as the rise/fall times of the digital output.

9.9.9 Health and Safety

The project does not have any open voltage differentials of greater than 40V, which would classify it as a high voltage system. Additionally, all of the outputs of the project are low power (roughly 1W each). Circuit protection devices techniques such as transient voltage suppression and over current protection are implemented in the final design. The damage done from user error or misuse is minimized as a result.

When manufacturing the product hot solder is used to fuse together connections. Hand-soldering presents burn risk to the manufacturer (me). This risk is minimized when working with a clear workspace and moving at a slow, consistent pace (the author admits that he did not always move at a slow, consistent pace and most definitely did not have a clear workspace at any point in time).

9.9.10 Social and Political

An unavoidable social issue is the inherent inequity this product causes. Because the price of $200-300, not every student can afford the product. This presents an advantage towards the students that can afford it and thus have a convent lab in their home. So long the product costs money, this impact can not be totally eliminated. The author has worked extensively to reduce cost as much as possible. The benefit of such a product is that if more and more students acquire it, the demand for on campus lab equipment falls allowing for other students to use it.

The only stakeholders identified are the author, the buyer, and Professor Braun. The author stakes his pride on this product, and dedicated extensive time and money toward development. If the product is actually sold, Professor Braun is likely to be the point of contact for debugging purposes.

9.9.11 Development

Many different programs aid with electronic design.

kicad is the schematic and PCB layout editor. See Section 9.1.

LTSpice simulated proposed circuits, verifying their working order.

Code Composer Studio is the software development environment that aids in programming the MSP432 microcontroller.

Microsoft Excel organizes and formats data into graphs and trends for visualization.

MATLAB does computational analysis. See Figure 8.7.

Overleaf is for report and LaTeX formatting.

Parametric component searches narrowed down components based on required specifications.

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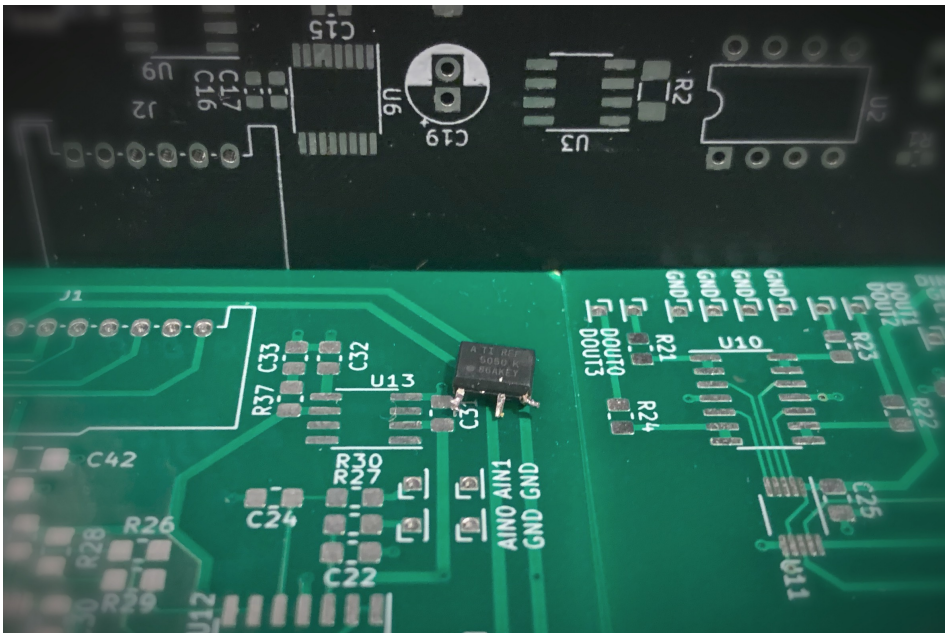
9.10 Special Thanks

9.10.1 Component Graveyard

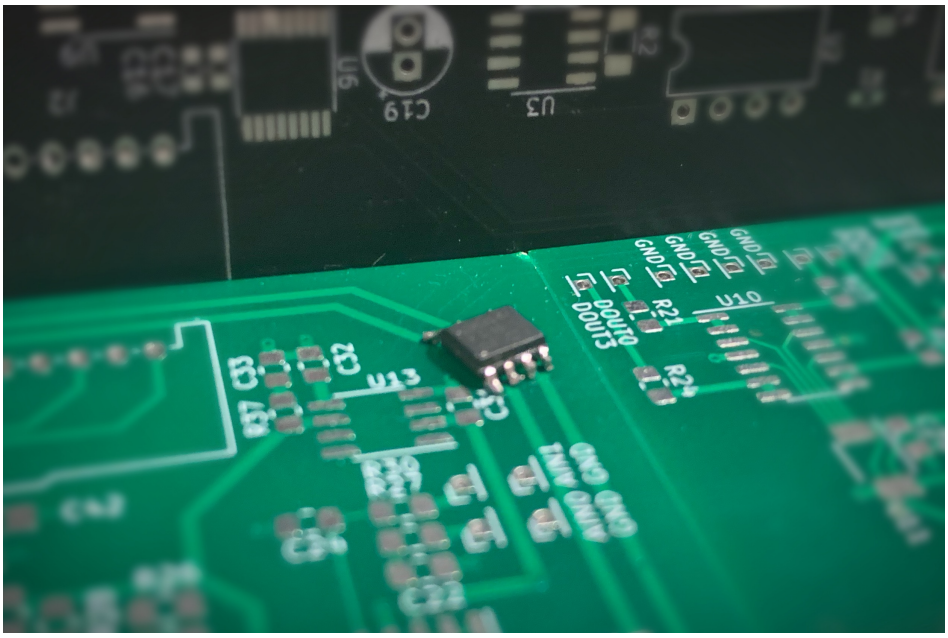
Designers design, testers test, but do components compon? Do they ever come home? No, not if the author accidentally slaughters them with his sheer incompetence they don't. All ramblings aside, components have it rough. They are expected to work 24/7 every week for decades at a time. Not to mention they work in high stress environments with massive temperature fluctuations, cramped quarters, and even have to burden the freshman (and senior) EE students accidentally swapping VDD and GND. All this brutal work for what? Pennies? Dollars? The truth of the matter is that this whole project is built out of components, and without them, the project would be absolutely nowhere. The author would like to take some precious megabytes out of his report in order to thank the fallen components that (un)willingly gave their lives for a greater good.

Table 9.1. R.I.P.



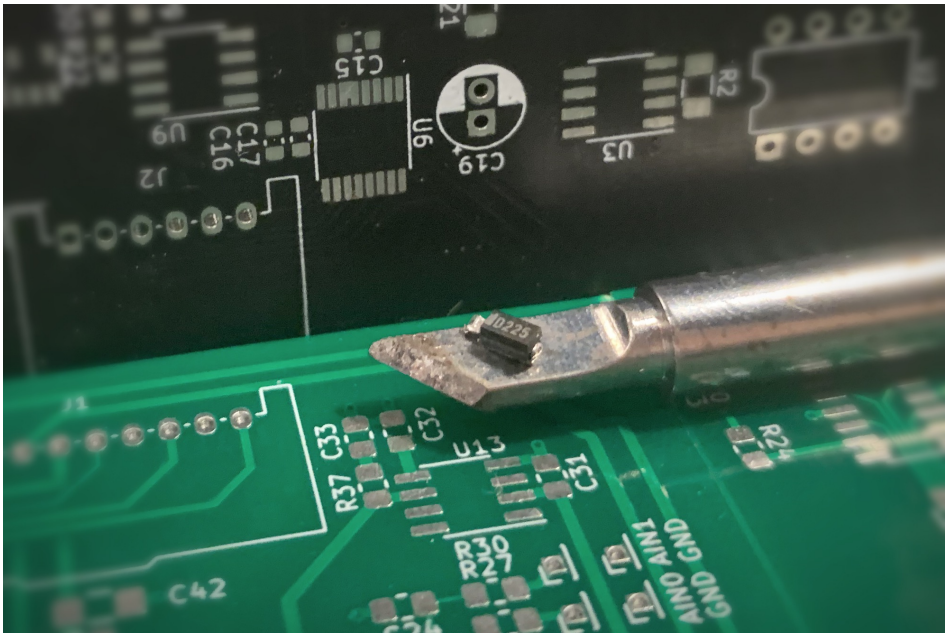
Part Name: REF5050
Time of Death:
Cause of Death: 15V applied to output with V_{DD} disconnected

Table 9.2. Beloved Wife and Mother



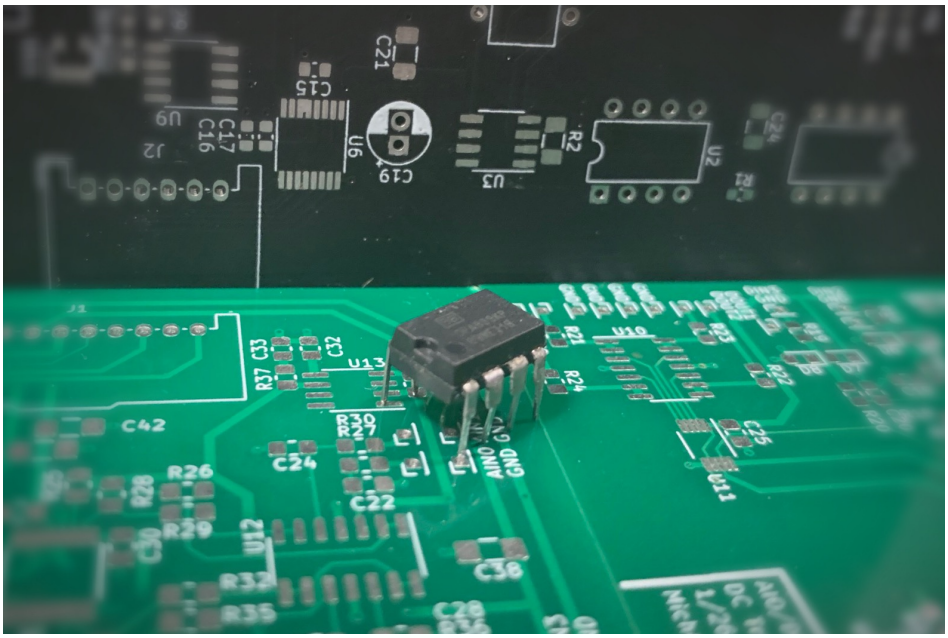
Part Name: INA145
Time of Death: 11:13AM, 2/16/2020
Cause of Death: 15V applied to output with V_{DD} disconnected

Table 9.3. F



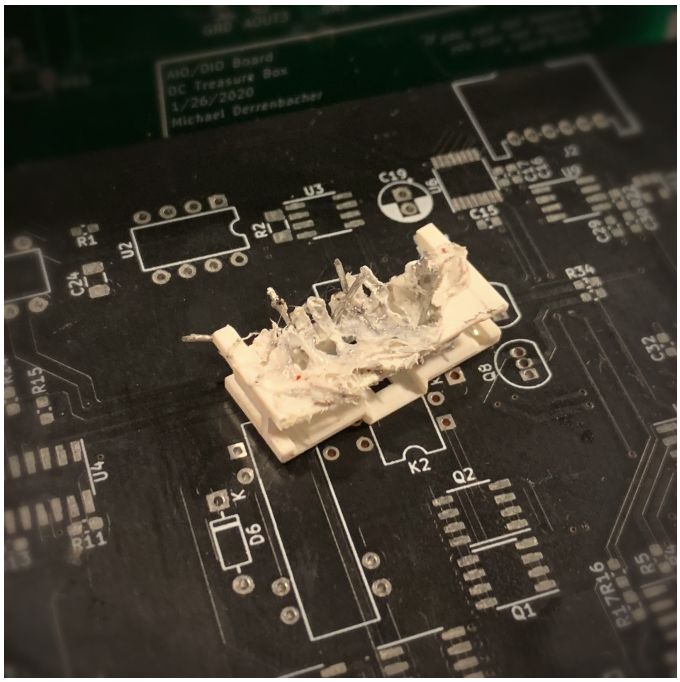
Part Name: Tantalum Capacitor
Time of Death: 1:07PM, 4/14/2020
Cause of Death: Reverse polarity

Table 9.4. Gone but not Forgotten



Part Name:	OPA633
Time of Death:	9:33PM, 4/22/2020
Cause of Death:	Prolonged overcurrent conditions

Table 9.5. RIP in Peace



Part Name:	MicroClasp Connector
Time of Death:	12:47 PM 5/7/2020
Cause of Death:	Author Lost Patience While Desoldering

Table 9.6. Wounded in Battle, in Stable Condition

Part Name: MSP432P401R Launchpad (Pin 1.5)
Time of Death: 6:56 PM 3/26/2020
Cause of Death: Scope Prope Shorted SPI Output and GND

Table 9.7. A Beautiful Soul

Part Name: MSP432P401R Launchpad
Time of Death: 5:30 PM 5/11/2020
Cause of Death: Code Composer Studio Crashed During Code Upload and Bricked Board

9.10.2 Other Thanks

David Braun - for reining me in and making sure I wrote my ABET analysis. This sentence was written in passive voice by me just to annoy you with my grammar one last time.

Paul Hummel - for emergency airdropping me a MSP and saying "That's a good question" whenever I asked him a question.

Vladimir Prodonov - for helping me get the Hell Circuit working.

My Mom - for proofreading my report and writing "Is this an EE term?" everytime I made a spelling mistake.

My Cat - for not ESD zapping any of my circuits and for being the best lab assistant I could ask for.

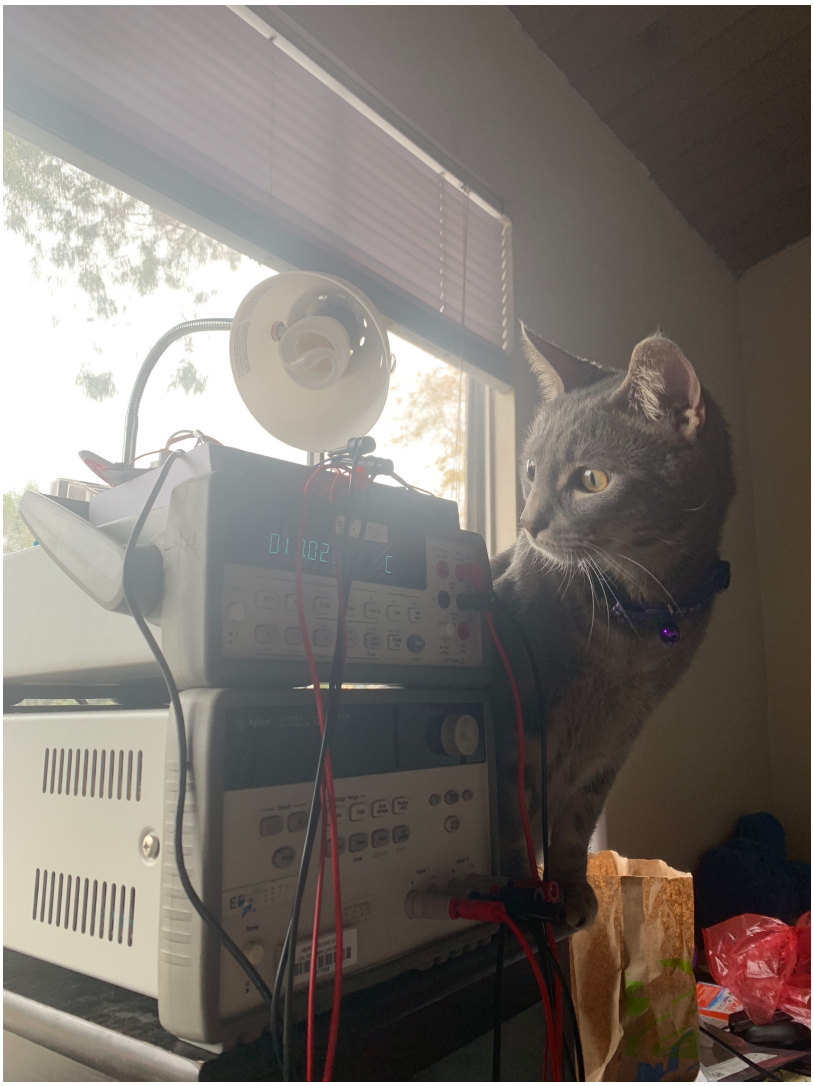


Figure 9.15. Navi Heir-Stokes reading off important voltages

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Thanks for reading!
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