HIGH EFFICIENCY RF AMPLIFIER DESIGN

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Abstract

High efficiency RF power amplifiers are key to the operation of modern wireless systems. From reducing power consumption at base stations to increasing battery life in handsets, high efficiency amplifiers help system designers to meet key performance criteria for their customers. The advent of the Internet of Things and 5G will lead to mass proliferation of battery operated wireless devices, increasing demand for high efficiency systems. In this project, a high efficiency 4W narrowband PA operating at 1GHz is designed, built and tested for the IMS2020 high efficiency power amplifier (HEPA) design competition. Emphasis is placed on achieving maximum power-added efficiency. The resulting amplifier provides 81.5% power added efficiency while delivering 4.8W to a 50Ω load with 0.25W input power.

Acknowledgments

I'd like to begin by acknowledging the individuals who contributed to this project, providing technical resources, equipment, time, and support. Without you, this project could not have been successfully completed.

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I'd like to thank Kent Johnson and KJ Microwave for giving me machine shop access to fabricate the design and equipment to test it. Without your help, this project could never have come as far as it did.

To my parents, I wouldn't be here without you. Your constant advice, expertise, support, and yes, money, got me through college. For everything you have given me, I owe you a debt I could never repay.

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Chapter 1

Introduction

The International Microwave Symposium (IMS) holds student design competitions at its annual conference to stimulate innovation in key technological areas and allow students to tackle some of the industry's biggest challenges.

For 14 consecutive years, MTT-5 (High Power Amplifier Components and Techniques Committee) has held the high efficiency RF power amplifier student design competition (SDC). [1] This competition focuses on achieving maximum power added efficiency (PAE) while meeting other specific performance parameters. Power added efficiency is defined in equation 1.1.

$$PAE(\%) = \frac{P_{out} - P_{in}}{P_{dc}} \times 100 \tag{1.1}$$

PAE is a measure of how efficiently an amplifier converts DC bias current into RF power. Contest entries are scored according to the figure of merit (FOM) defined in equation 1.2. [1]

$$FOM = PAE(\%) \times [Freq(GHz)]^{0.25} \tag{1.2}$$

Therefore, the goal of the project is to achieve the highest possible figure of merit while meeting the ground rules to be eligible for the competition (see requirements and specifications).

A variety of device types, amplifier classes, and circuit formats exist. A key part of the design process is selecting the appropriate amplifier class and circuit format. Input and output networks and DC biasing circuitry must also be designed and optimized.

The following chapters lay out the specifications, design process, fabrication, testing, and conclusions for the project.

Chapter 2

Requirements and Specifications

The groundrules and baseline requirements for eligibility in the competition are listed below, as provided by the contest organizers. rules

1. The power amplifier (PA) design may use any type of technology, but must be the result of new effort, both in the amplifier design and fabrication.

2. The PA mechanical design should allow for internal inspection of all relevant components and circuit elements. The RF ports should be SMA female connectors. Bias connections should be banana plugs.

3. The PA should require a maximum of two dc supply voltages for operation.

4. The PA must operate at a frequency in the range of 1 GHz to 10 GHz and have an output power level when excited by a single carrier of at least 4 watts, but no more than 40 watts at the frequency of test.

5. All PAs should require less than 24 dBm of input power to reach the minimum 4 watt output power when excited with a single carrier.

6. Measurements will be made by the judges only. A team representative must be present at testing to provide information on connections, design frequency, and expected output power level.

7. All linearity measurements will be performed under CW two-tone operation with two equal amplitude carriers spaced 20 MHz apart at room ambient conditions into a 50 ohm load. Only the power at the two fundamental carrier frequencies will be included in the measurement of output.

8. Linearity measurements will be conducted with a maximum of 21 dBm input power per tone. The tone power will be swept from 0 dBm to 21 dBm and the C/I ratio measured.

9. The winner will be based on the amplifier's PAE measured during official testing at the lowest power level for which the C/I ratio* equals 30 dB. If the C/I ratio is better than 30 dB over the entire testing range, the measurement at 21 dBm input power per tone will be used. The

figure of merit for scoring will be the PAE multiplied by a frequency weighting factor having the form $(GHz)^{0.25}$.

10. The team will be allowed a maximum of 10 minutes to set up their PA and familiarize with the test equipment before testing.

11. The official measurements will be performed by the committee with the chosen device biasing point from the students.

12. The decision of the judges will be final. Awards from IMS and industry will be presented at the Student Awards Luncheon.

The marketing requirements shown in table 2.1 were chosen in EE460 to serve as overarching principles ensuring success of the project and customer satisfaction. The engineering specifications shown in table 2.2 were developed from the marketing requirements in EE460 and revised in EE461 after updated rules were provided by the IMS contest organizers. The marketing requirements and engineering specifications together serve to ensure that the final product meets all competition rules and is well-positioned to win the competition.

Table 2.1: RF Amplifier Marketing Requirements

Marketing Requirements

1. Simple DC biasing scheme

2. High linearity

3. Standard connections

4. Design allows for easy internal inspection

5. High efficiency

6. Easiest design frequency

Table 2.2: RF Amplifier Specifications

Marketing Requirements	Engineering Specifications	Justification
1	The PA shall have no more than two (2) DC supply voltages.	Complex DC biasing schemes require additional power supply circuitry, which increases complexity and cost. Two DC bias voltages is typically the minimum for this type of amplifier.
2	Carrier-to-intermodulation ratio (C/I) shall be greater than 30dBc when excited by two tones spaced 20MHz apart at the input power level of test.	The C/I ratio is a common way to measure RF amplifier linearity. In this case, this specification is provided by the contest rules.
3	RF ports shall use SMA female connectors.	Very common RF connectors, also contest rules.
3	DC bias ports shall use banana plugs.	Very common connectors, also contest rules.
4	The PA enclosure shall have a cover removable with a Philips screwdriver.	Judges must be able to inspect the final product, so the amplifier must be inspect-able with simple tools.
5	The PA shall have at least 50% PAE (Power Added Efficiency) with less than 0.25W input power	50% is a baseline achieved by most amplifiers in past competitions. [2]
6	The PA shall have a center frequency of 1 GHz.	Lowest allowed frequency makes design simpler.

Table 2.3 shows key deliverables for the project, as well as their approximate completion dates. This represents a preliminary schedule, subject to change without notice.

Table 2.3: RF Amplifier Deliverables

Delivery Date	Deliverable Description
Dec. 9th, 2019	Design Review
Mar. 13th, 2020	EE 461 Demo
Dec. 20th, 2020	EE 461 Report
Apr. 1st, 2020	Enter IMS Contest
May. 25th, 2020	EE 462 Demo
May. 25th, 2020	Sr. Project Expo Poster
Jun. 5th, 2020	EE 462 Report

Chapter 3

RF Amplifier Theory

This chapter describes the main amplifier classes, along with their advantages and disadvantages, before selecting the most appropriate type for the project and examining its operational theory in detail.

RF amplifiers can be divided into two classes. The first is the conduction angle amplifiers, which can be described by their conduction angle or the portion (in radians) of one complete cycle (2π) during which the device conducts current. The second is the switch-mode amplifiers, in which the active device operates as a switch, residing in either the 'on' or 'off' state, but not in between. [3]

3.1   Conduction Angle Amplifiers

Figures 3.1 through 3.4 show the ideal transfer characteristics for the conduction angle amplifiers. For each amplifier, the main characteristics, advantages, and disadvantages are also listed. Information is taken from [3], [4], and [5].

Class A
Conduction Angle: 2π
Maximum Theoretical Efficiency: 50%
Advantages: Highly linear, easy to design and build.
Disadvantages: The least efficient amplifier. Typical real-world efficiency can be as low as 25%.
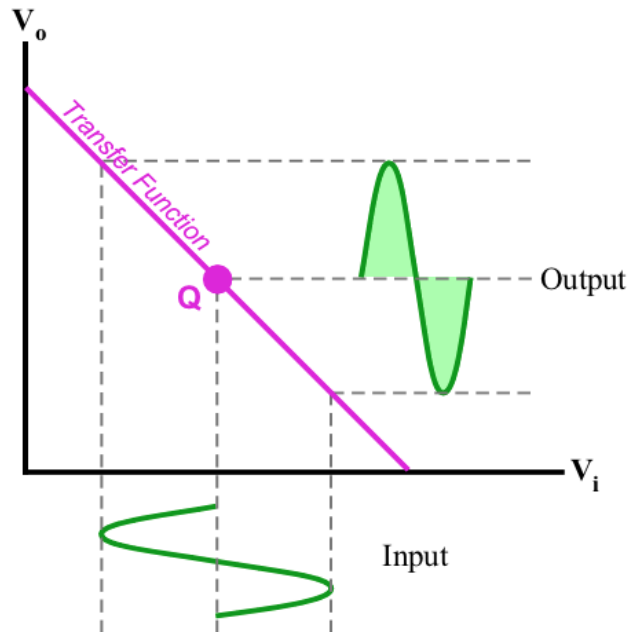
Figure 3.1: Class A Transfer Characteristic

Class B
Conduction Angle: π
Maximum Theoretical Efficiency: 78.5%
Advantages: Zero quiescent current, so no power is consumed while amplifier is idle. Lower bias point dramatically increases efficiency.
Disadvantages: Degraded linearity since device only conducts for half the cycle.
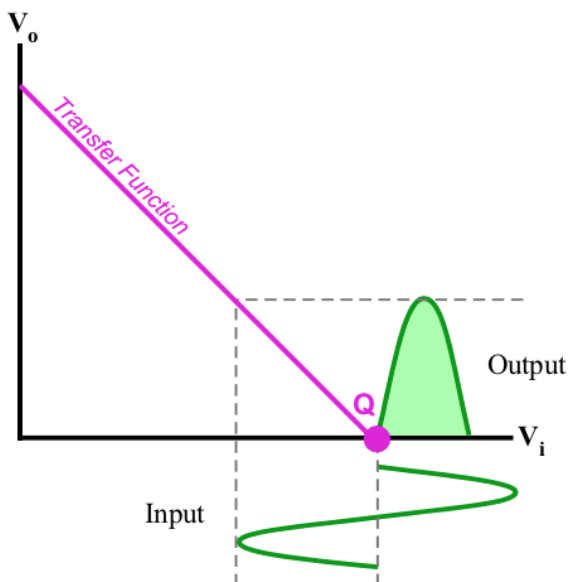
Figure 3.2: Class B Transfer Characteristic
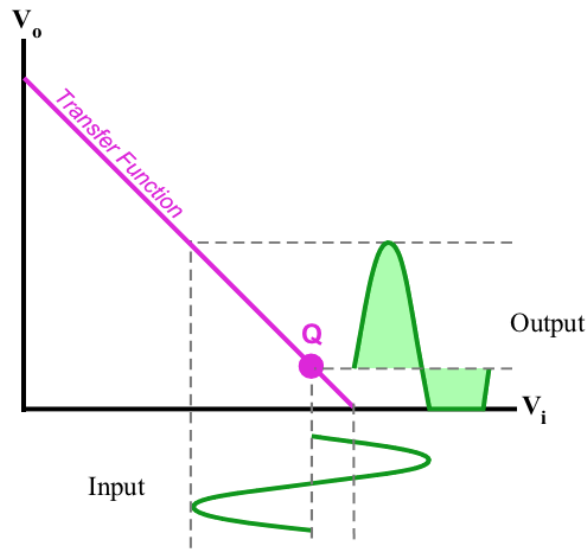
Figure 3.3: Class AB Transfer Characteristic

Class AB
Conduction Angle: $\pi < \theta < 2\pi$
Maximum Theoretical Efficiency: 78.5%
Advantages: Better efficiency than class A and better linearity than class B.
Disadvantages: Neither linearity nor efficiency is outstanding. This amplifier is a cross between class A and class B, hence the name.
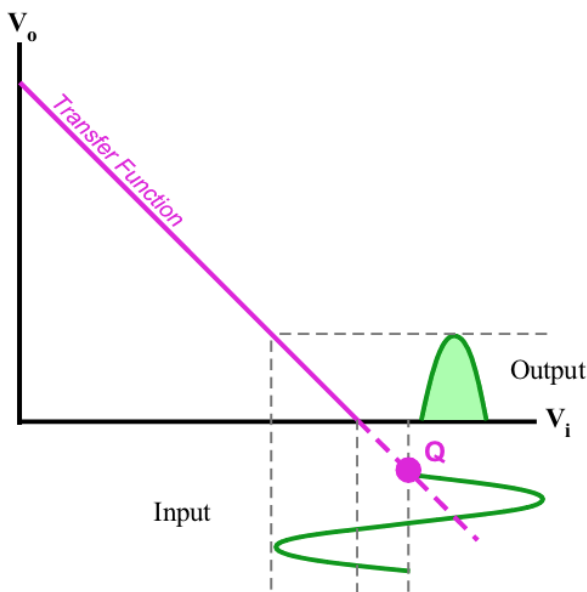
Figure 3.4: Class C Transfer Characteristic

Class C
Conduction Angle: $\theta < \pi$
Maximum Theoretical Efficiency: $\approx 90\%$
Advantages: High efficiency due to excellent bias current utilization.
Disadvantages: Bias point is even lower than class B, giving this amplifier the worst linearity.

3.2   Switch-Mode Amplifiers

The active device in a switching amplifier always operates in either the 'on' or 'off' state, much like a switch. These amplifiers rely on tuned admittances presented at the device output to shape and control the output waveforms. [4] Switching amplifiers are thus best defined by their output

waveform shapes.

Figures 3.5 through 3.7 show the output waveforms for the most common switch mode amplifiers. [4], [3], [6]
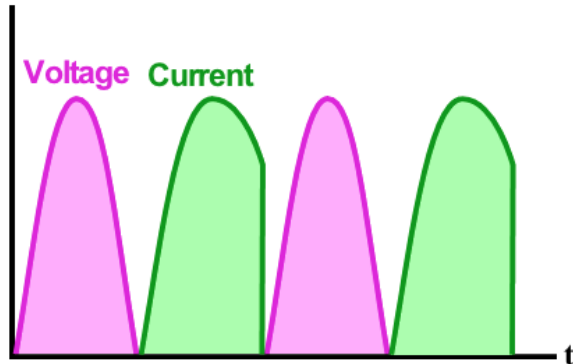
Figure 3.5: Class E Output Waveforms

Class E
Maximum Theoretical Efficiency: 100%
Advantages: Very high theoretical efficiency.
Disadvantages: Device parasitics make successful class E implementations difficult at high frequencies. Requires fast switching input to acheive high efficiency. Poor linearity due to switching action
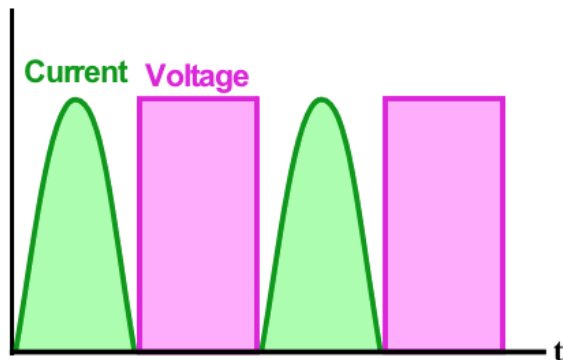
Figure 3.6: Class F Output Waveforms

Class F
Maximum Theoretical Efficiency: 100%
Advantages: High theoretical efficiency, easier to implement than class E.
Disadvantages: Poor linearity due to switching action.
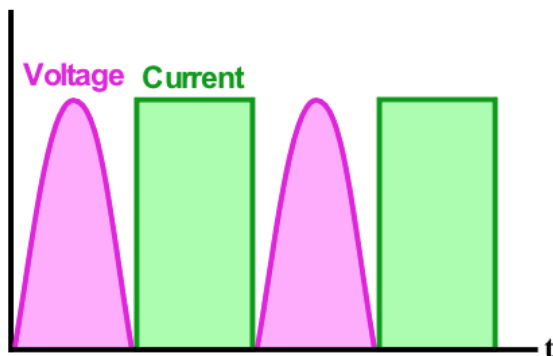
Figure 3.7: Class F^{-1} Output Waveforms

Class F^{-1}
Any switching amplifier can be converted to its inverse by presenting a reciprocal admittance to the device output. The F^{-1} amplifier has similar characteristics to the regular class F, except the voltage and current waveforms are swapped.

3.3   The Doherty Amplifier

The Doherty amplifier has received significant attention from engineers for its ability to provide high efficiency over a wide range of input powers. Invented in the 1930s by William Doherty, the Doherty amplifier uses two active devices. The first is the "carrier amplifier," which is biased as a class AB. The second is the "peaking amplifier," biased as a class C. For low power inputs, the carrier amplifier does all the work, and the peaking amplifier remains off. For high power operation, the peaking amplifier also turns on to assist the carrier amplifier. [7]

Doherty amplifiers are useful in applications where high efficiency is desired, but signal power varies with time (for example, an AM system). Doherty amplifiers are not used in systems that always operate at full power, such as FM transmitters and radars. [7]

3.4   Amplifier Class Selection

For this project, the main goal is to build an amplifier that is able to provide high power added efficiency (PAE) while meeting the linearity specification of the IMS contest.

After examining the advantages and disadvantages of each amplifier, the class F and Doherty amplifiers emerge as the main contendors for the project.

A Doherty amplifier would require at least three supply voltages, and the IMS contest allows a maximum of two DC supply voltages (see competition rules, page 4). Constructing a custom circuit to generate the necessary supply voltages would expand the scope of the project well beyond the recommended 150 hours for senior projects.

The class F amplifier is thus the amplifier of choice for this project.

3.5   Class F Amplifier Operation

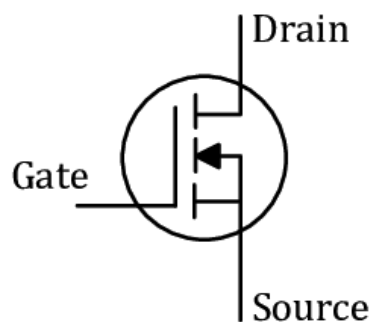Consider the device shown in figure 3.8:

Figure 3.8: A Basic FET

The power dissipated in the device is given by equation 3.1.

$$P_{dis} = V_{DS} \cdot I_D \tag{3.1}$$

For maximum efficiency, the power dissipated in the device should be minimized. Equation 3.1 indicates that to minimize P_{dis}, V_{DS} and I_D should never be large at the same time.

The ideal V_{DS} and I_D waveforms of a class F amplifier are shown in figure 3.9.
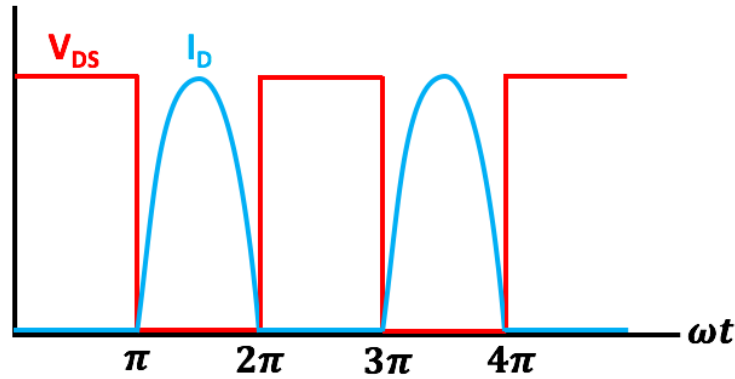
Figure 3.9: Class F Amplifier Waveforms

Figure 3.9 shows that when V_{DS} is non-zero, I_D is zero, and vice-versa. Therefore, for the ideal class F amplifier, $P_{dis} = 0$, and efficiency = 100%.

To understand how to create these waveforms, re-write them using Fourier Series:

The Fourier Series expansion of the square voltage wave shown in figure 3.9 is shown in equation 3.2, where A represents the maximum V_{DS}, n represents the harmonic number, and ω_0 represents the fundamental frequency in rad/s.

$$V_{DS}(t) = \frac{A}{2} + \frac{4A}{\pi} \sum_{n=1}^{\infty} \frac{sin((2n-1)\omega_0 t)}{2n-1} \tag{3.2}$$

Equation 3.2 shows that the square wave is composed of odd voltage harmonics of the fundamental frequency.

Equation 3.3 contains the corresponding Fourier Series expansion for the half-sine current waveform, where B represents the maximum drain current.

$$I_D(t) = \frac{B}{\pi} + \frac{B}{2} sin\omega_0 t - \frac{2B}{\pi} \sum_{n=1}^{\infty} \frac{cos(2n\omega_0 t)}{4n^2-1} \tag{3.3}$$

Equation 3.3 shows that the half-sine wave is composed of even current harmonics.

Therefore, the drain network should preserve odd voltage harmonics and even current harmonics. The transistor drain should see a load impedance at harmonic frequency nf_0 of $Z_L = \infty$ for $n = 3, 5, 7...$ and $Z_L = 0$ for $n = 2, 4, 6....$ Presenting the same harmonic impedances at the gate of the device has been shown to further improve efficiency, so this technique will be applied for this design. [5]

To achieve the theoretical maximum 100% efficiency for class F, all harmonics (an infinite number) must be controlled. In practice, this is impossible, and it is generally not worth controlling high order harmonics, because the corresponding efficiency gain is small and may be counteracted by extra loss and parasitic elements from excessively complicated circuitry. This project controls the second and third harmonics only. [5]

Chapter 4

Design

This section details the design process for the final amplifier, including DC biasing, harmonic traps, matching networks, and physical implementation. The Cree/Wolfspeed CG2H40010F GaN HEMT device was used throughout this design due to its high drain efficiency, 10W power capability, the recommendation of Dr. Derickson, and the availability of free samples from Cree. Keysight ADS is used for simulation with the device model provided by Cree.

4.1 DC Biasing

The first step in designing the amplifier is establishing the DC bias point and circuitry. The CG2H4001F datasheet recommends operating with a drain voltage of 28V. [8] The bias point of a class F amplifier is typically between a class B and a class AB, and must be near cutoff to generate the harmonics necessary to build class F waveforms. [5]

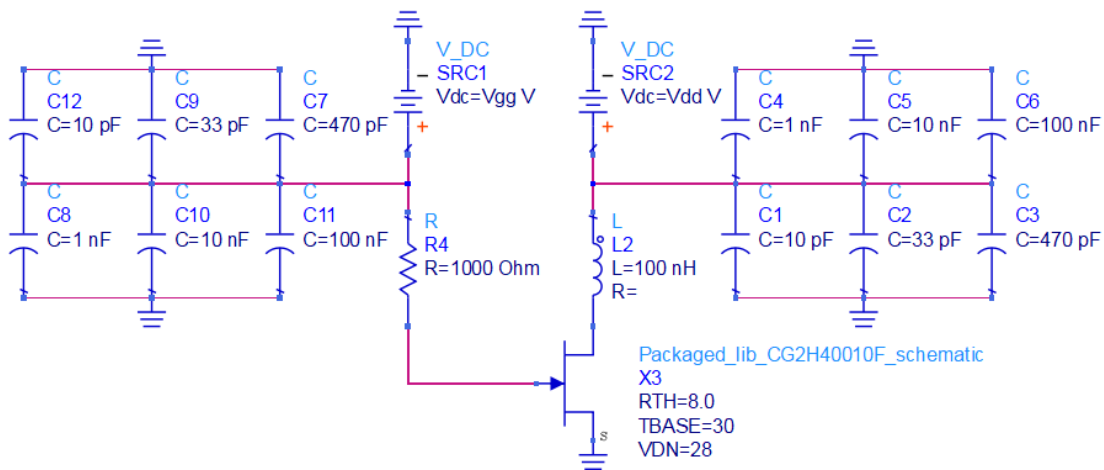Figure 4.1 shows the device bias circuitry.

Figure 4.1: DC Biasing Circuit

The drain is biased with a 100nH RF choke to ensure a high impedance at 1GHz. 6 parallel decoupling capacitors were selected from on-hand components (10pF, 33pF, 470pF, 1nF, 10nF, 100nF) to ensure broadband decoupling.

Since this is a FET device, gate current is zero and the gate can be biased with a large value resistor, in this case $1k\Omega$. This is preferable to using another RFC because it avoids H-field coupling between the gate and drain chokes, which may lead to oscillations. Another set of 6 decoupling capacitors is placed at the gate.

An ADS gate voltage sweep from -3.5V to -2.5V shows drain current I_D as a function of V_{GS}. Figure 4.2 shows the resulting plot.
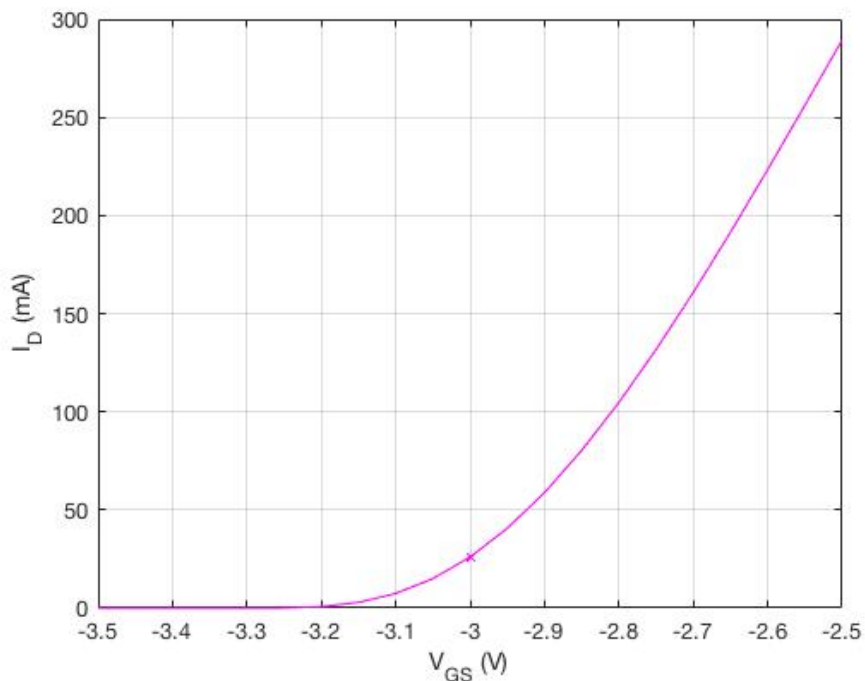
Figure 4.2: Simulated I_D vs V_{GS} for CG2H40010F

The 'x' in figure 4.2 indicates a drain current I_D of approximately 25mA for a gate voltage V_{GS} of -3.0V. This bias point should allow the device to create the harmonics necessary for class F operation, and will be used throughout simulation. Gate bias voltage can be easily optimized during hardware testing, so this value simply acts as a starting point.

A note on quarter-wave bias stubs: Use of a quarter-wave biasing stub for this project was specifically avoided. For class F design, impedances at harmonic frequencies of the fundamental are critical. The quarter wave stub presents an open circuit at the fundamental frequency, but depending on its placement in the circuit may disrupt the harmonic impedances. For this design, use of the quarter wave stub restricts the number of possible circuit configurations and needlessly complicates the design process.

4.2 Source/Load Pull Analysis

The class F harmonic impedances listed on page 13 are nominal impedances for an ideal device. Non-ideal devices have parasitic components at the gate and drain, which may shift the optimal harmonic impedances from their nominal values. Source and load pull simulations allow the designer to determine optimal source and load impedances for efficiency and delivered power at fundamental and harmonic frequencies.

Keysight ADS sweeps the designated harmonic impedance over a range of values, calculating efficiency and delivered power at each, then plotting constant efficiency and power contours on the Smith Chart. This allows the designer to easily examine the simulation data and select the desired impedance value.

For this project, an iterative approach to source/load pull analysis is used to optimize the harmonic impedances. The load pull simulation block is shown in figure 4.3
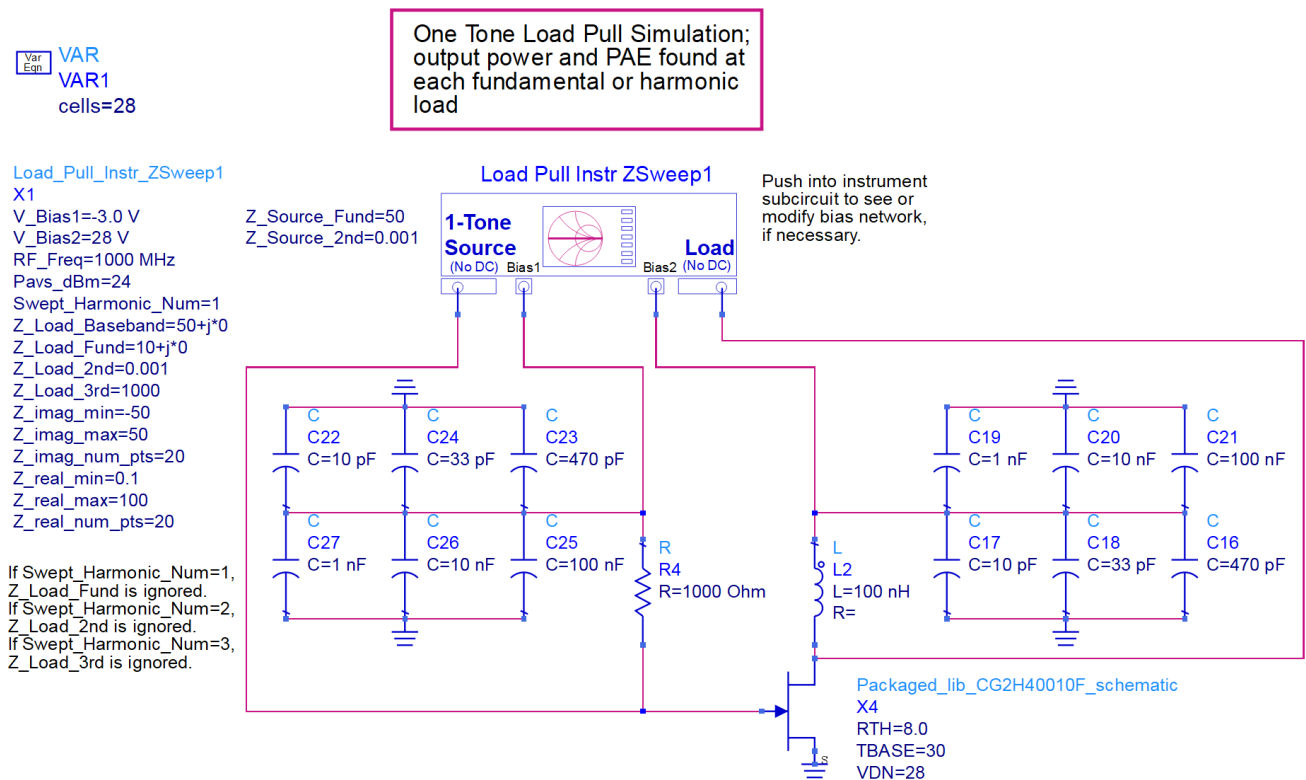
Figure 4.3: Load Pull Simulation Circuit

The source pull simulation circuit is shown in figure 4.4. Both simulations may be found under the DesignGuide menu in ADS.
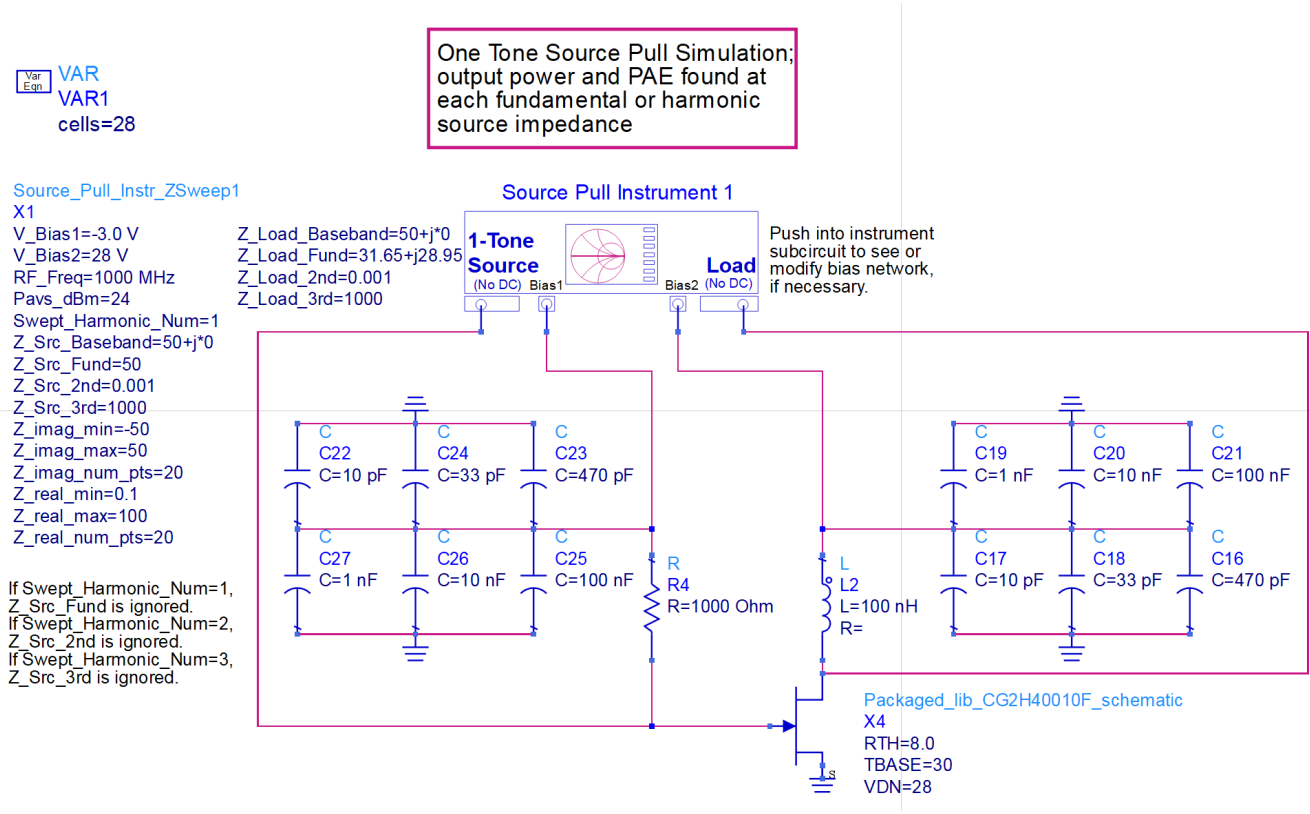
Figure 4.4: Source Pull Simulation Circuit

Initially, set the source and load second and third harmonic impedances the nominal values determined on page 13. Set all other impedances to 50Ω. Note that ADS does not allow impedances of 0 or ∞, so use 0.001Ω and 1000Ω, respectively. Set the bias voltages for the gate and drain to -3.0V and 28V, respectively. Set the available source power to +24dBm or 0.25W, the maximum drive level allowed in contest rules (see page 4).

The following subsections show ADS simulation results for the first three steps of the optimization process in order to demonstrate the workflow. The corresponding tables list the impedance value settings for that step, as well as the impedance sweep ranges used.

4.2.1   Load Pull Analysis, Fundamental

Table 4.1 lists the impedance settings for the first load pull simulation. Table 4.2 lists the sweep range for the first load pull simulation. Figure 4.5 shows the simulation data plotted on a smith chart.

Table 4.1: Z_{L1} Impedances

Impedance	Value (Ω)
Z_{L1}	Swept
Z_{L2}	0.001+j0
Z_{L3}	1000+j0
Z_{S1}	50+j0
Z_{S2}	0.001+j0
Z_{S3}	1000+j0
Others	50+j0

Table 4.2: Z_{L1} Sweep Values

Parameter	Value (Ω)
R_L^{min}	0.1
R_L^{max}	100
X_L^{min}	-50
X_L^{max}	+50
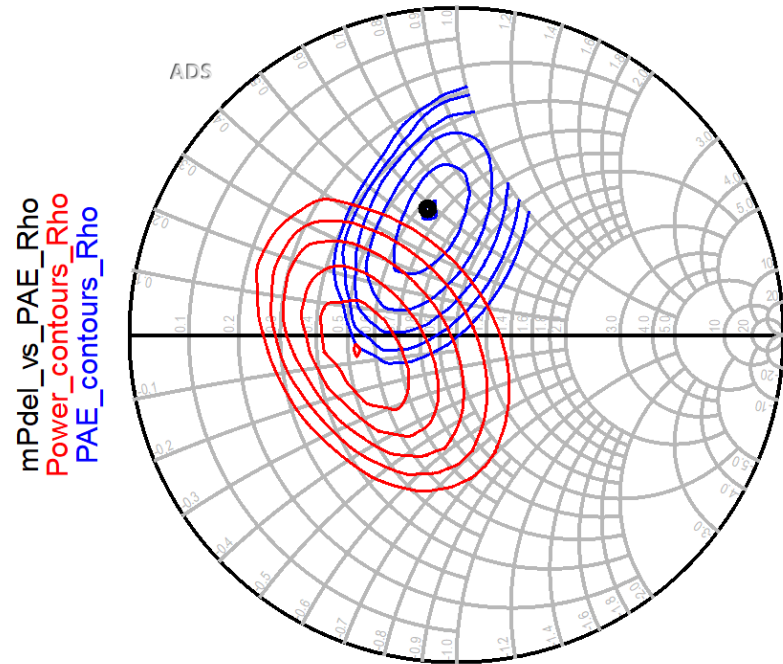
Figure 4.5: Load Fundamental Smith Chart

The black dot in figure 4.5 represents the fundamental load impedance providing maximum PAE. To ensure that the amplifier meets the 4W output requirement for the competition (see contest rules, page 4), ensure that the point of maximum PAE also provides at least +36dBm of delivered power. Simulation indicates **38.3dBm** at this point. Since the amplifier provides sufficient power, use this new fundamental load impedance of **31.65+j28.95**Ω and continue to the next step.

4.2.2   Source Pull Analysis, Fundamental

Table 4.3 lists the impedance settings for the fundamental source pull simulation. Table 4.4 lists the sweep range for the source pull simulation. Figure 4.6 shows the simulation data plotted on a smith chart.

Table 4.3: Z_{S1} Impedances

Impedance	Value (Ω)
Z_{L1}	31.65+j28.95
Z_{L2}	0.001+j0
Z_{L3}	1000+j0
Z_{S1}	Swept
Z_{S2}	0.001+j0
Z_{S3}	1000+j0
Others	50+j0

Table 4.4: Z_{S1} Sweep Values

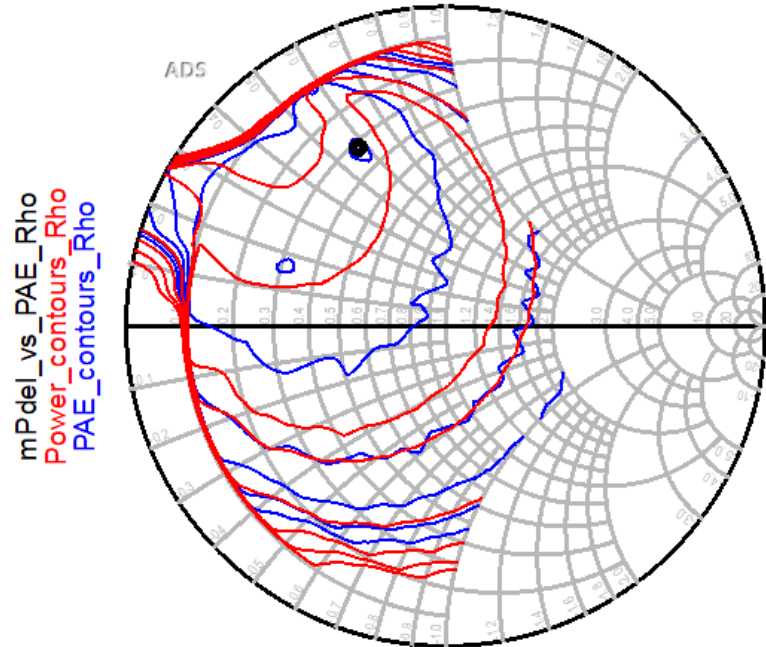| Parameter	Value (Ω)
R_L^{min}	0.1
R_L^{max}	100
X_L^{min}	-50
X_L^{max}	+50

Figure 4.6: Source Fundamental Smith Chart

The black dot in figure 4.6 represents the fundamental source impedance providing maximum PAE. Again verifying sufficient output power, simulation indicates **38.2dBm** at this point. Since the amplifier provides sufficient power, use this new fundamental source impedance of **15.87+j28.94**Ω and continue to the next step.

4.2.3   Load Pull Analysis, Second Harmonic

Table 4.5 lists the impedance settings for the second harmonic load pull simulation. Table 4.6 lists the sweep range for the simulation. Figure 4.7 shows the simulation data plotted on a smith chart.

Table 4.5: Z_{L2} Impedances

Impedance	Value (Ω)
Z_{L1}	31.65+j28.95
Z_{L2}	Swept
Z_{L3}	1000+j0
Z_{S1}	15.87+j28.94
Z_{S2}	0.001+j0
Z_{S3}	1000+j0
Others	50+j0

Table 4.6: Z_{L2} Sweep Values

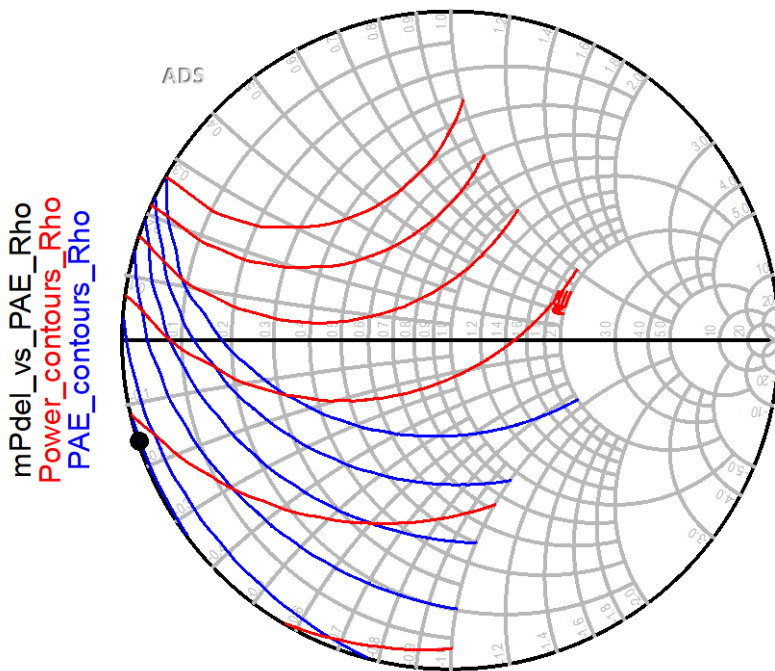| Parameter	Value (Ω)
R_L^{min}	0.1
R_L^{max}	100
X_L^{min}	-50
X_L^{max}	+50

Figure 4.7: Load 2nd Harmonic Smith Chart

The black dot in figure 4.7 represents the fundamental source impedance providing maximum PAE.

Figure 4.7 illustrates the effect of device parasitics. The optimum second harmonic load impedance is nominally a short circuit, but simulation indicates a maximum PAE point that is capacitive. This is likely due to output inductance of the device.

Continuing the same procedure of optimizing, checking power, and updating impedance values in the simulation for the remaining impedances results in the three charts shown in figure 4.8, representing Z_{S2}, Z_{L3}, and Z_{S3}.

Note that the impedance sweep values should be adjusted to cover the high-resistance portion of the Smith Chart for the third harmonic, since the optimal impedance is nominally an open circuit.

(a) Source 2nd Harmonic Smith Chart

(b) Load 3nd Harmonic Smith Chart
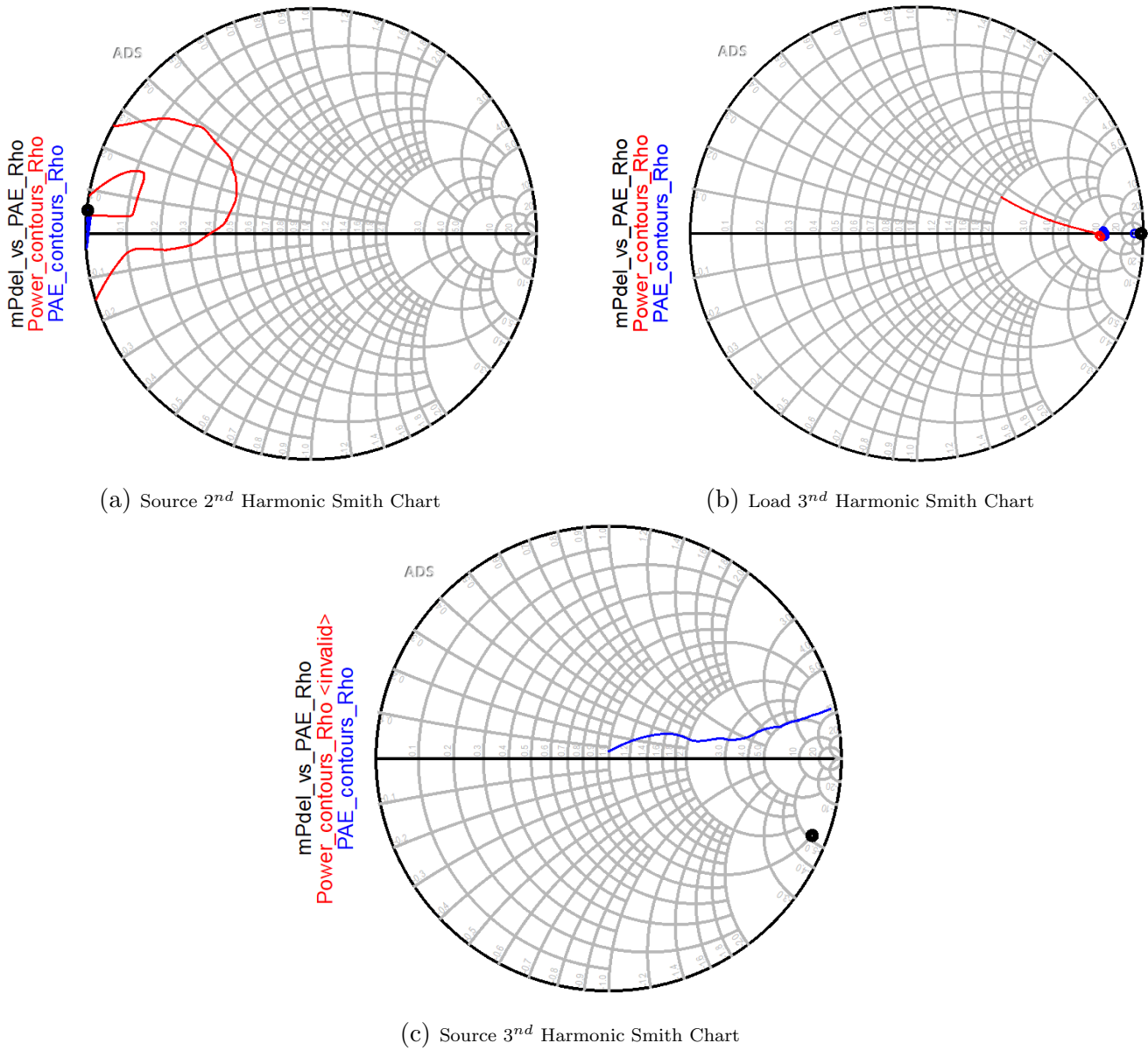

(c) Source 3nd Harmonic Smith Chart

Figure 4.8: Remaining Simulation Smith Charts

The optimal second and third harmonic source impedances (Figure 4.8(a) and (c)) are also shifted from their nominal values by the device parasitics. Running the simulation with optimal values yields **91.5% PAE**, while running with nominal values yields **89.8% PAE**. Since simulation verifies this is an efficiency difference of only 1.7%, *it is decided to use the nominal values for all harmonics* to simplify the design process. While it is possible to develop a circuit topology that allows all of the harmonic impedances to be optimized, it requires a more complex layout not within the time budget of this project.

4.3   Harmonic Traps

With the harmonic impedances established, the next step is designing the 'Harmonic Traps' to provide the correct impedances to the transistor's gate and drain. Many circuits exist for this purpose. One such circuit is shown in figure 4.9.
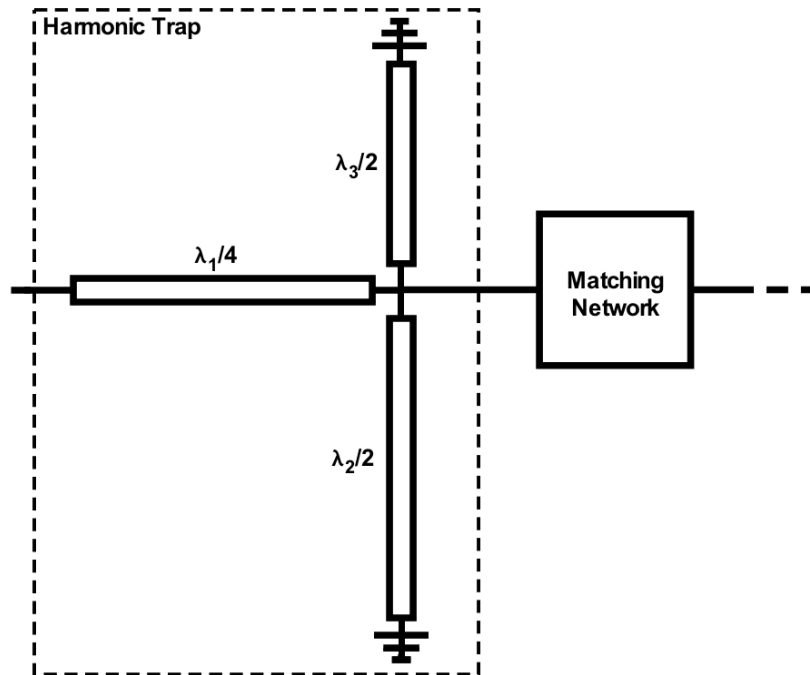

Figure 4.9: Harmonic Trap Circuit

The half-wave short circuit stubs create second and third harmonic shorts at the cross junction. When these short circuits are translated to the left (drain) side of the quarter wave line, a short is created at the second harmonic (2GHz) and an open at the third harmonic (3GHz). A matching network follows the harmonic trap to create the optimum fundamental impedance for power transfer and efficiency.

Short circuit stubs were selected over open circuit stubs because they do not suffer from the same fringing capacitance and radiation losses.

Figure 4.10 shows the ADS re-creation of the harmonic trap circuit using ideal transmission lines.
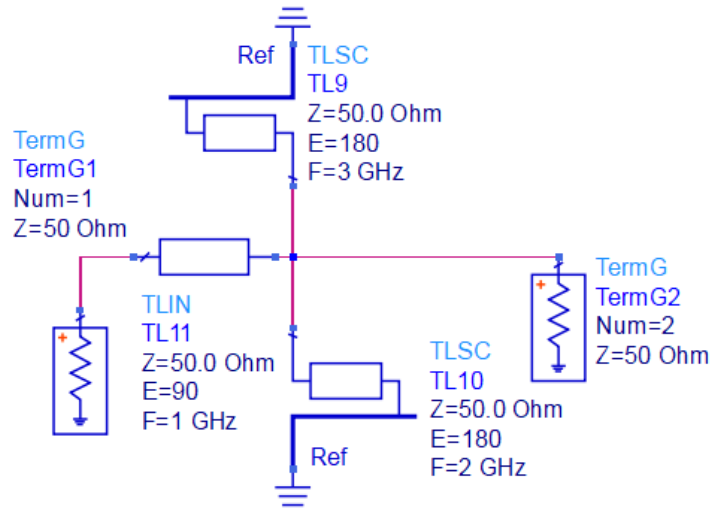
Figure 4.10: Harmonic Trap ADS Circuit

Figure 4.11 shows the simulated input impedance of the harmonic trap from the left (drain) side. Markers m1 and m2 indicate a short circuit at 2GHz and an open circuit at 3GHz, as expected.
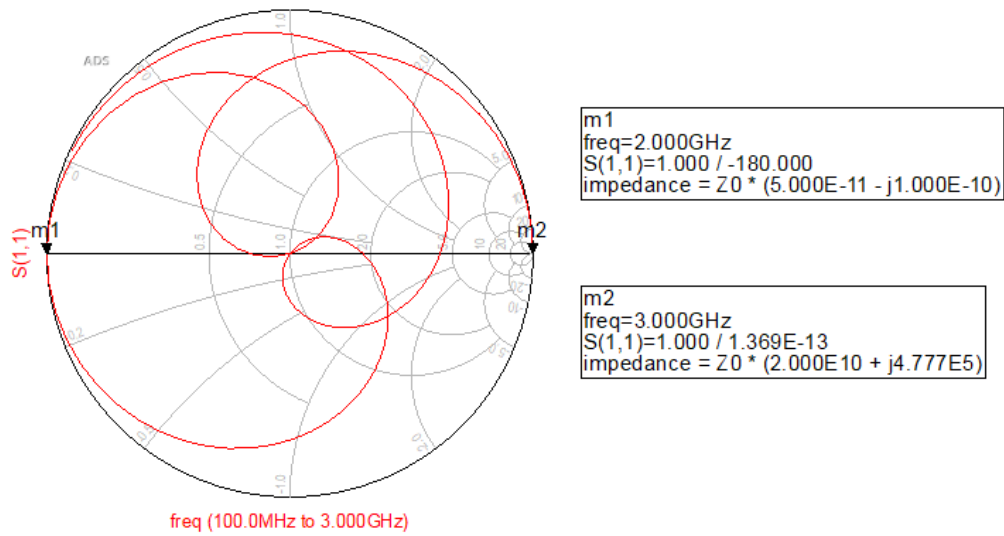

Figure 4.11: Harmonic Trap Simulation

The harmonic traps can now be integrated with the FET and biasing circuitry, as shown in figure 4.12.
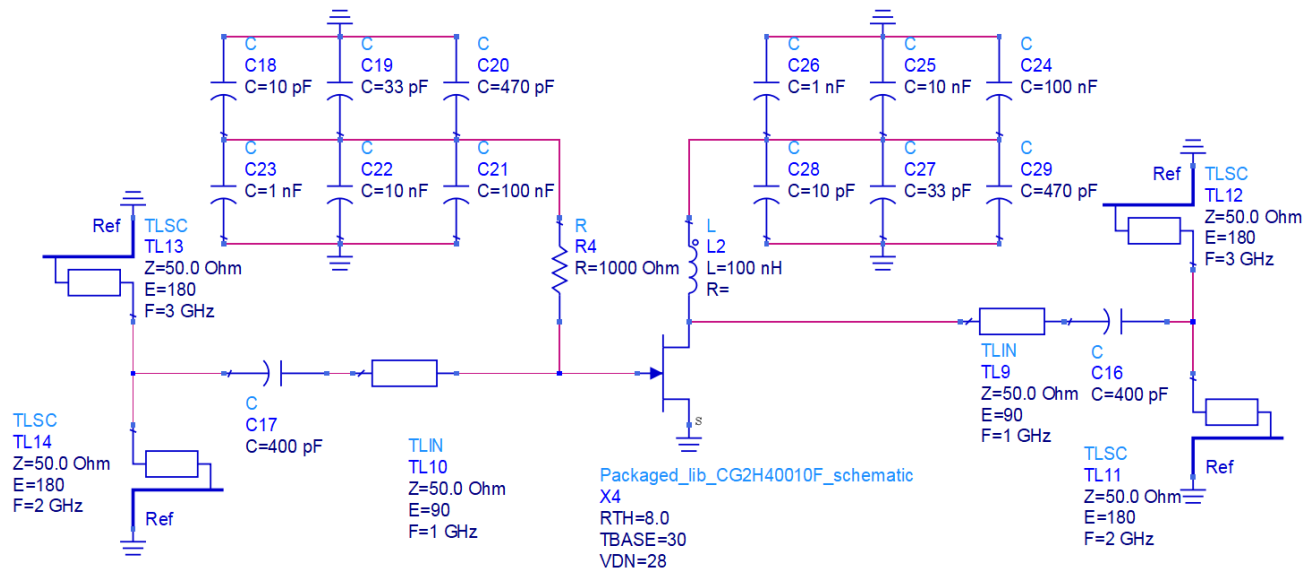
Figure 4.12: FET with Biasing and Harmonic Traps

Coupling capacitors are added to isolate the input, output, and short circuit stubs from DC bias. A value of 400pF is chosen, having an impedance at the fundamental frequency of 1GHz $Z_C = 1/\omega C = 1/2\pi(1GHz)400pF = 0.398\Omega$, which is sufficiently low to ensure adequate RF coupling. The 400pF capacitor is formed by four 100pF capacitors in parallel. The smaller value capacitors ensure a high resonant frequency and low equivalent series resistance (ESR).

4.4   Matching Networks

The next step is designing the matching networks that set the drain and gate impedances at the fundamental frequency. Since the matching networks are connected after the harmonic traps, their impedances at the gate and drain will be modified by the short circuit stubs and quarter-wave line. The simplest way to account for this and determine the correct matching impedance is to perform load and source pull simulations at the fundamental frequency again, this time with all impedances set to 50Ω and the harmonic traps included in the circuit (perform source and load pull analysis for the entire circuit of figure 4.12).

The resulting load pull simulation is shown in figure 4.13(a). The optimized fundamental load impedance is entered into the source pull simulator and source pull is performed. The resulting source pull simulation is shown in figure 4.13(b).
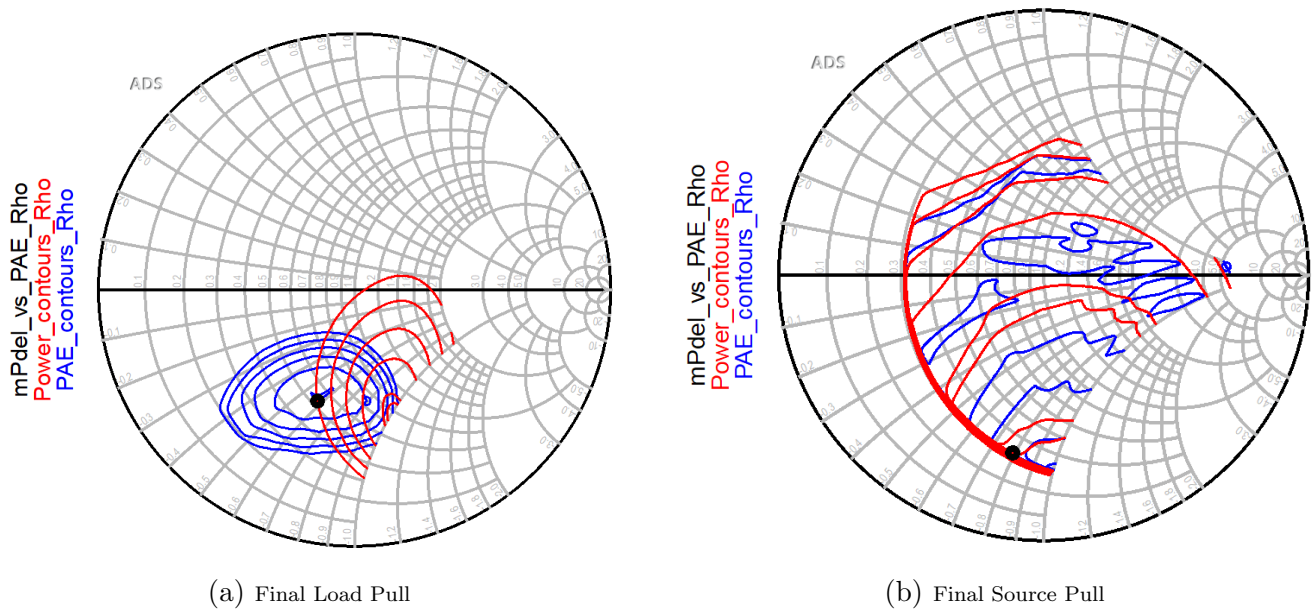
(a) Final Load Pull

(b) Final Source Pull

Figure 4.13: Final Source and Load Pull

The optimized load impedance (load matching network impedance) is **26.39-j28.95**Ω. The optimized source matching network impedance is **15.88-j46.8**Ω. The final optimized PAE is **85.51%**, and the final output power is $+39.3dBm$, easily satisfying the 4W requirement.

Further investigation reveals that if the source matching network is eliminated (50Ω is presented directly to the harmonic trap), the resulting PAE is only reduced by 2.5% to **82.9%**. To simplify the design and save time, the source matching network is eliminated.

The Smith Chart matching network utility in ADS allows the designer to insert different circuit elements and drag the network impedance to different locations on the chart. A simple single-stub tuner will suffice for this design. Figure 4.14 shows the Smith Chart matching utility.
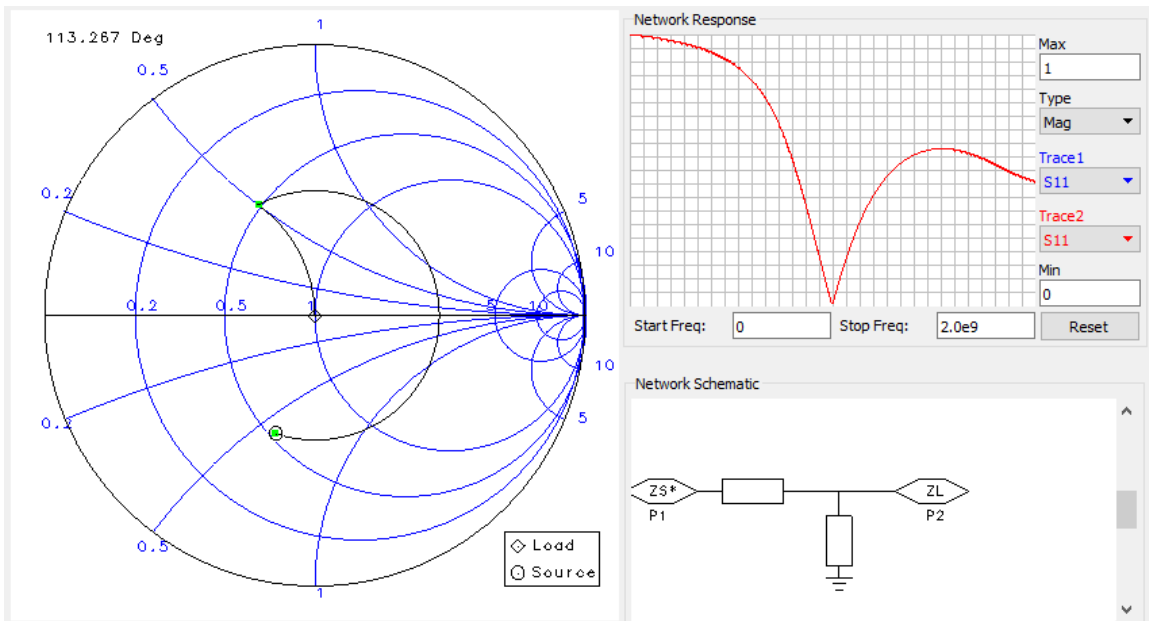
Figure 4.14: Smith Chart Matching Utility

Figure 4.15 shows the final amplifier circuit with output matching network, harmonic traps, and DC biasing.
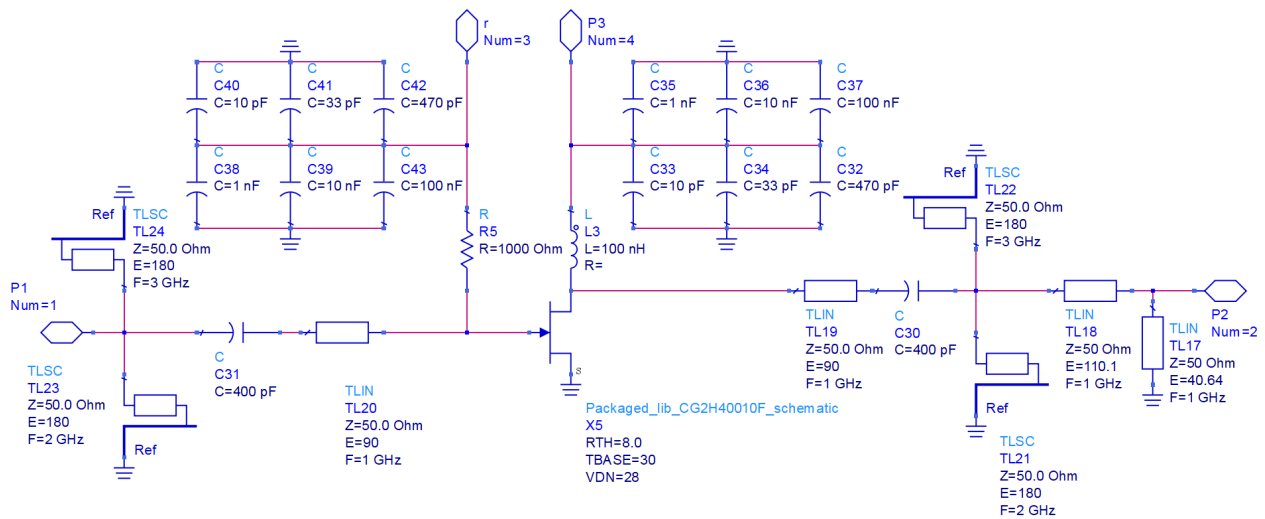

Figure 4.15: Final Amplifier Circuit

Load pull simulation is run one more time to verify the PAE with the output matching network included. Figure 4.16(a) shows that the optimum fundamental load impedance has now been shifted to near 50Ω. Figure 4.16(b) shows final delivered power vs PAE curves. The final optimized metrics are shown in table 4.7.
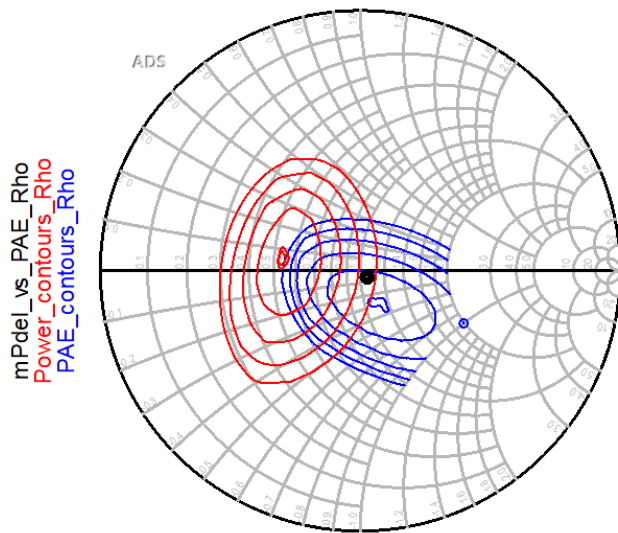
(a) Overall Load Pull
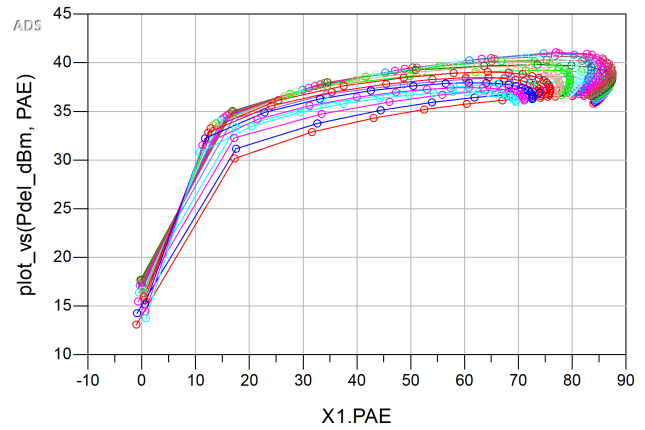
(b) PAE vs Delivered Power Curves

Figure 4.16: Final Simulated Data

Parameter	Value
PAE	86.4%
Output Power	+39.1dBm

Table 4.7: Final Optimized Metrics

Chapter 5

Fabrication

This chapter gives an overview of the physical implementation and fabrication of the device designed in the last chapter.

Three different formats were primarily considered before settling on the final implementation approach.

1. Microstrip - Microstrip is easy to work with and cheap to purchase. However, it suffers from dielectric losses. The equipment necessary to fabricate a microstrip board was unavailable due to the COVID-19 pandemic.

2. Suspended Substrate Stripline - Suspended Substrate Stripline (SSS) consists of a circuit suspended between two ground planes, using an air dielectric. Dielectric losses are much lower than microstrip. However, the physical size of the design makes SSS cumbersome and difficult.

3. Coaxial - Coaxial circuits, while time-consuming to fabricate, have several advantages: Electrically sealed structure reduces radiation losses; Large conductor area provides lower conductor loss than microstrip or SSS; Air dielectric can be used, providing lower dielectric losses than Microstrip.

Due to the COVID-19 pandemic, the tooling available to the designer was best suited for fabricating a coaxial design, so this topology was selected.

The design was fabricated from low oxygen 101 copper, which has higher conductivity than standard copper, minimizing losses. Inner and outer conductors were selected from off the shelf sizes using equation 5.1, where D is the outer conductor diameter and d is the inner conductor diameter, to create a characteristic impedance near 50Ω.

$$Z_o(\Omega) = \frac{138 \times log_{10}(D/d)}{\sqrt{\epsilon_r}} \tag{5.1}$$

A 0.179" outer conductor and 0.062" inner conductor were conveniently available, for a characteristic impedance of 63.54Ω, which is near enough to 50Ω.

Cross pieces were fabricated from half-inch square bar. A clamshell design allows the cross pieces to clamp down on the outer conductors using 2-56 screws, as shown in figure 5.1.

Figure 5.1: Transmission Line Cross Pieces

The device mount was also fabricated from copper bar. A 3D model of the mount is shown in figure 5.2. Two holes allow the device flange to be screwed into the mounting block with 2-56 screws.
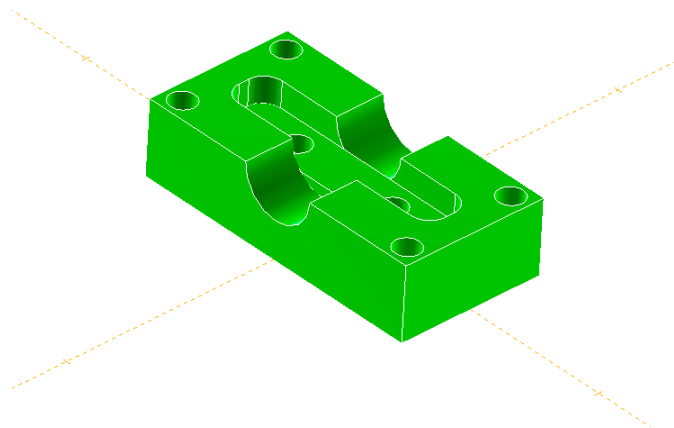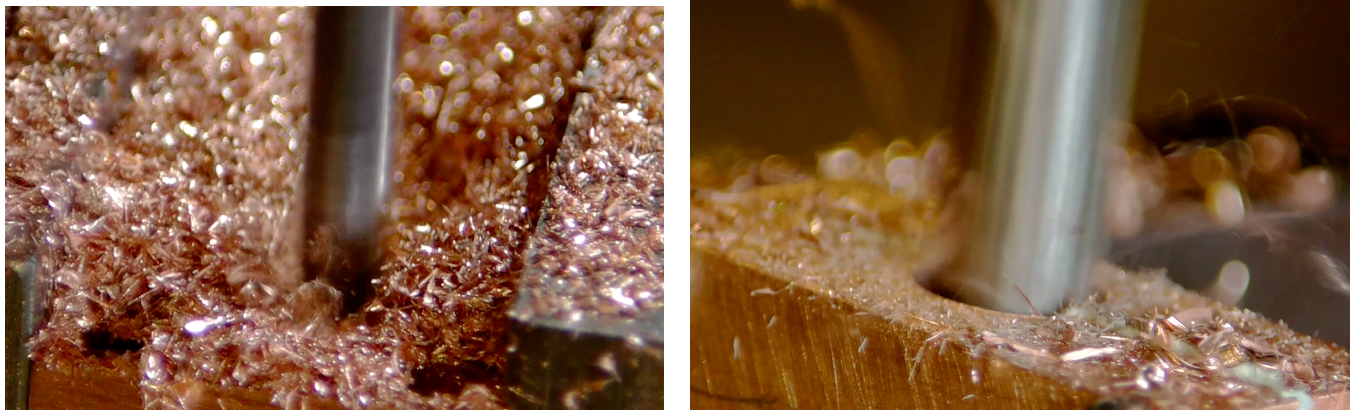

Figure 5.2: Device Mounting Block

The center of the block is milled down so the gate and drain leads sit at the same vertical level as the center conductor, and each side of the block is milled to allow the coaxial transmission lines to connect. Figure 5.3 shows these machining processes.

(a) Machining the Device Pocket   (b) Counter-Boring for Gate and Drain Connections

Figure 5.3: Machining the Device Mounting Block

The top half of the device mount clamps down on the transmission lines in the same way as the cross pieces. 4-40 filtered feedthroughs are inserted to supply DC bias to the device, as shown in figure 5.4.
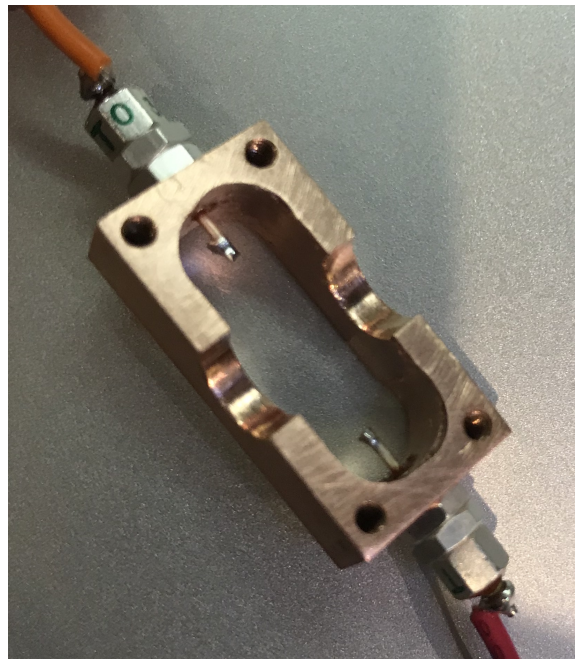

Figure 5.4: Top Half of Device Mounting Block

The lathe turns shorting plugs for the ends of the stubs as shown in Figure 5.5 and cuts the inner and outer conductors to length.

Figure 5.5: Turning a Shorting Plug

Final assembly takes place once all parts have been fabricated, and the entire amplifier is mounted on a 0.062" thick aluminum plate for mechanical stability and heat sinking. Internal connections are made with solder paste and a heat gun, as shown in figure 5.6. Shorting plugs are soldered into the ends of the stubs. Small plastic shims support the inner conductors to maintain concentricity during the assembly process.
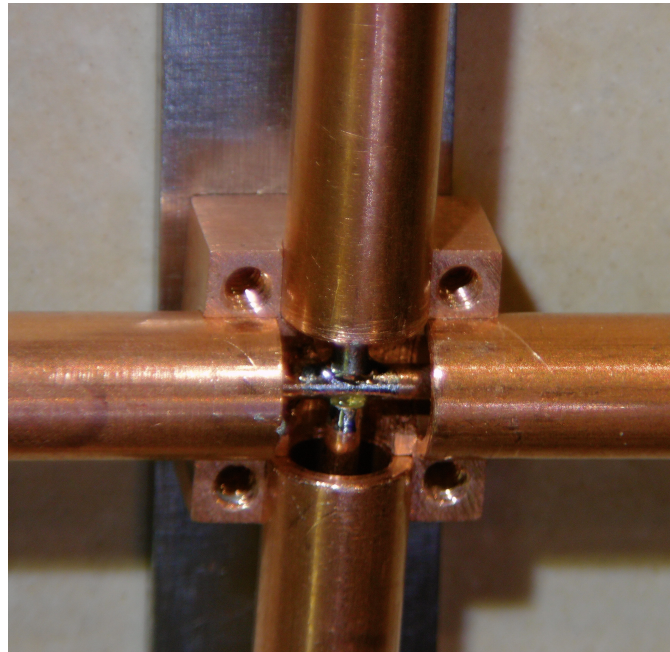

Figure 5.6: Soldering a Coaxial Cross Member

A 100nH RFC biases the drain. A 0.08" diameter mandrel was convenient for winding. Equation 5.2 gives the approximate inductance of an air core choke, where d is the diameter of the coil in inches, n is the number of turns, and l is the length of the coil in inches.

$$L(\mu H) = \frac{d^2 \times n^2}{18d + 40l} \tag{5.2}$$

A 14 turn coil provides approximately 100nH. Figure 5.7 shows the RFC after winding.
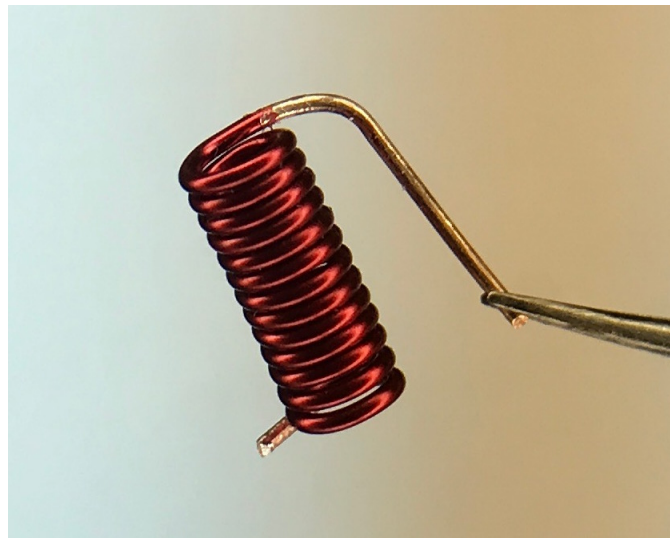

Figure 5.7: A Small, Very Cute Inductor

Figure 5.8 contains a detailed technical drawing of the entire amplifier. Figure 5.9 shows the entire amplifier after fabrication and assembly.
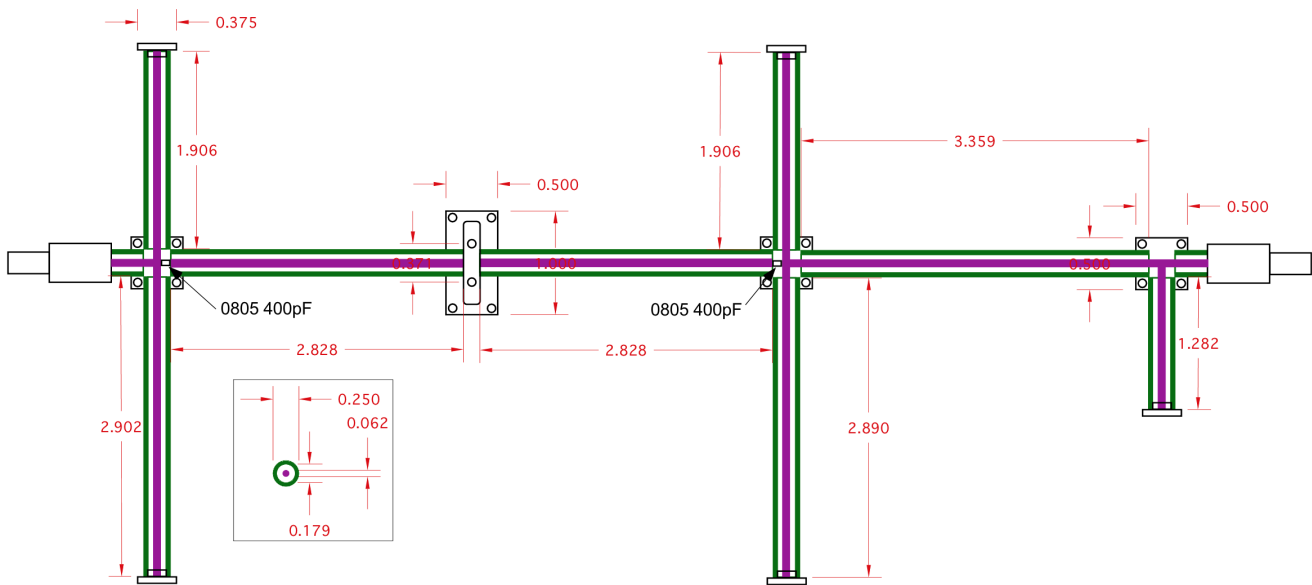
Figure 5.8: Amplifier Technical Drawing
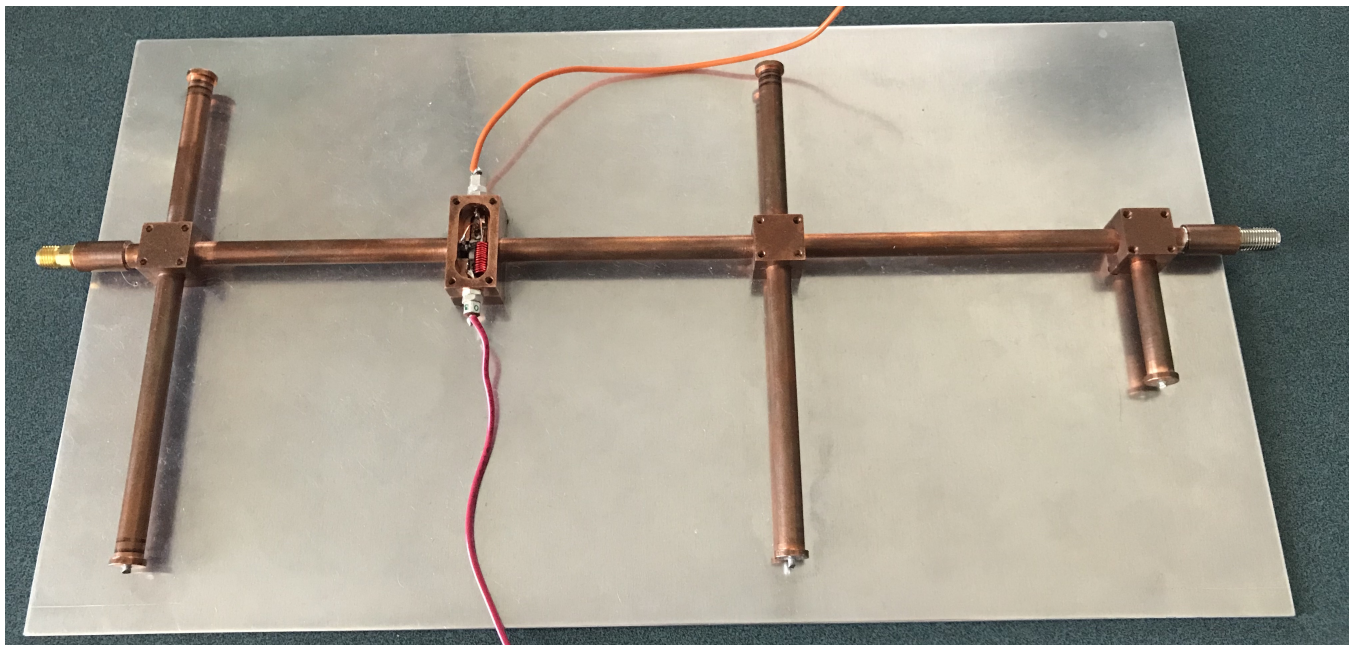
Figure 5.9: Complete Assembled Amplifier

Chapter 6

Testing

This chapter covers testing and experimental measurement of the amplifier. Testing is divided into four phases: attenuator / cable characterization, stability testing, one-tone testing, and two-tone testing.

6.1   Attenuator Characterization

A Narda 20dB, 20W resistive attenuator and a Minicircuits 10dB attenuator are placed at the output of the amplifier to protect test equipment during measurements. The attenuators are shown in figure 6.1.

Figure 6.1: Test Attenuators

For accurate output power measurements, the precise attenuation of the attenuator combination, adapters, and test cables at the amplifier output needs to be measured. A handheld NanoVNA-F was used for this measurement. Experimentation revealed that the attenuation is not perfectly constant over temperature. A heat gun was used to warm the attenuator, and its S-Parameters were measured at elevated temperature. Figure 6.2 shows the resulting S21 data.
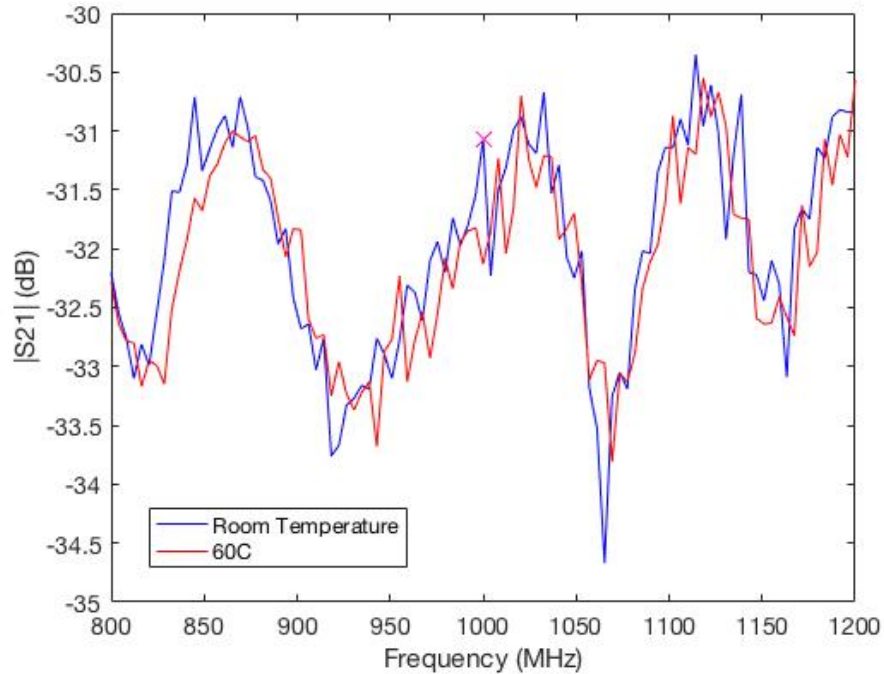
Figure 6.2: Attenuator S-Parameters over Temperature

Several watts of power will be dissipated in the attenuator during testing, so a small fan added to the attenuator ensures that it remains at a constant low temperature. Figure 6.2 shows that at room temperature, the attenuation is **31.07dB**, marked by the 'x'. This offset can be entered into the Spectrum Analyzer during later testing.

6.2   Stability Testing

The goal of this phase is to bias the amplifier and ensure that no oscillations are present before continuing testing. The input of the amplifier is terminated in a 50Ω load and the output is connected to the HP 8590A spectrum analyzer through the test attenuator. Drain bias is set to 28V and gate bias is set to -3.0V, the simulation condition. Figure 6.3 shows the resulting output.
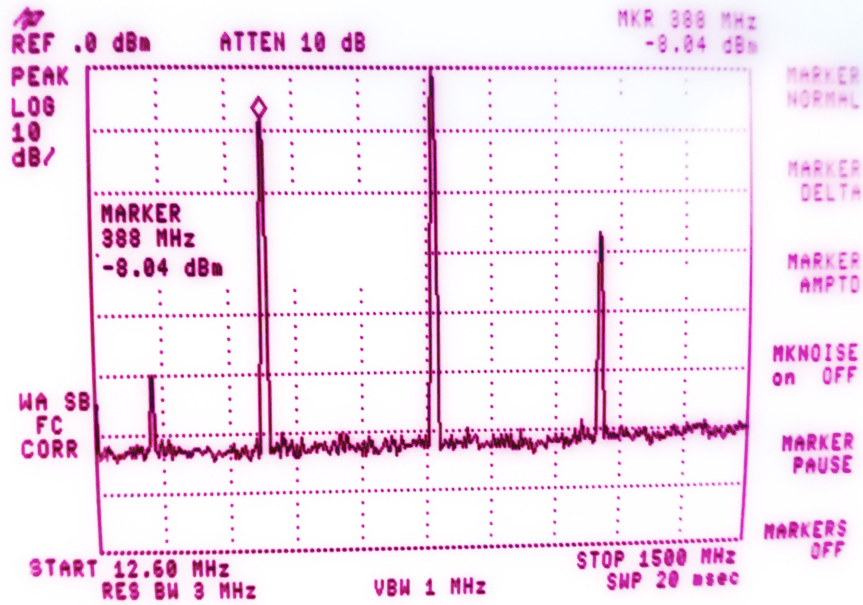
Figure 6.3: Initial Unstable Amplifier Output

The amplifier is unstable, oscillating at 388MHz. The amplifier stability can be determined by plotting the 'k' factor and its phase. 'k' and its phase are defined in equations 6.1 and 6.2. [9]

$$|k| = |\Gamma_{out}||\Gamma_L| \tag{6.1}$$

$$\angle k = \angle \Gamma_{out} + \angle \Gamma_L \tag{6.2}$$

Γ_{out} and Γ_L are defined in figure 6.4
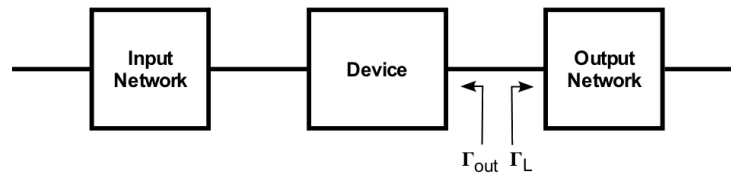
Figure 6.4: Γ Definition

The amplifier is unstable if $k \geq 1$ and $\angle k = \pm 0, 360, 720....$ [9] ADS S-Parameter simulation measures Γ_{out} and Γ_L and plots $|k|$ and $\angle k$. Figure 6.5 shows the results.

(a) Magnitude k

(b) Phase k
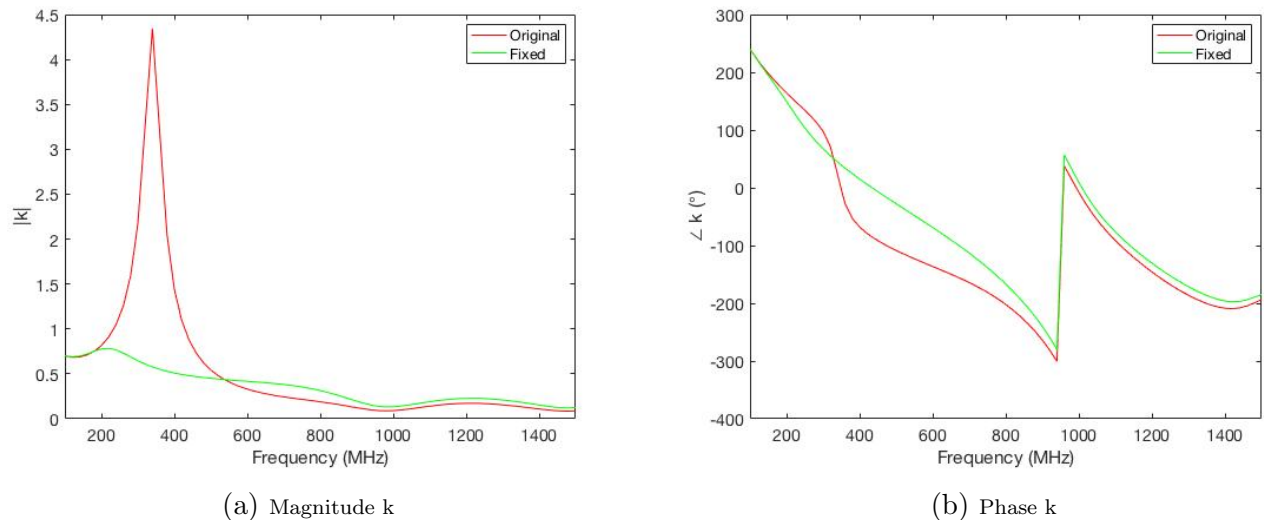
Figure 6.5: Stability 'k' Factor

Figure 6.5(a) shows that the magnitude of k is much greater than 1 near 388MHz, while 6.5(b) shows the phase is near zero. A shunt 33Ω resistor placed at the gate of the FET shifts the source impedance out of the unstable region and brings k below 1, as shown by the green trace in figure 6.5(a). The resistor is AC coupled with a 30pF capacitor to avoid drawing current through the $1k\Omega$ gate bias resistor, disrupting the gate bias voltage. Figure 6.6 shows the FET with the stabilizing resistor.
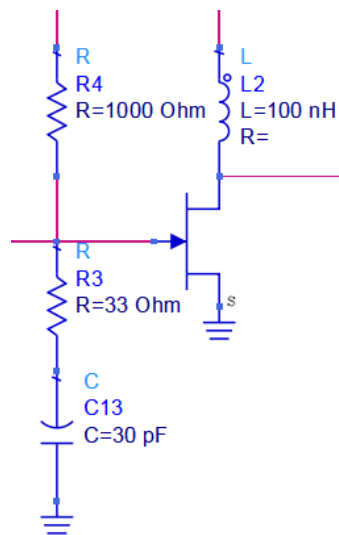
Figure 6.6: FET and Stabilizing Circuit

Re-running the ADS load pull simulation indicates an efficiency penalty of approximately 3.7% for this modification, for a new PAE of 82.7%. It is possible that a more optimal set of component values exists to stabilize the amplifier with less efficiency penalty, but the designer was not able to source new component values quickly and had to work with on-hand supplies. After implementing the stabilizing circuit, the FET was biased and no oscillations appeared on the spectrum analyzer.

6.3   One-Tone Testing

The goal of the one-tone test is to verify the output power of the amplifier is at least 4W with 0.25W input and measure the maximum PAE for the device. The complete test setup is shown in figure 6.7.
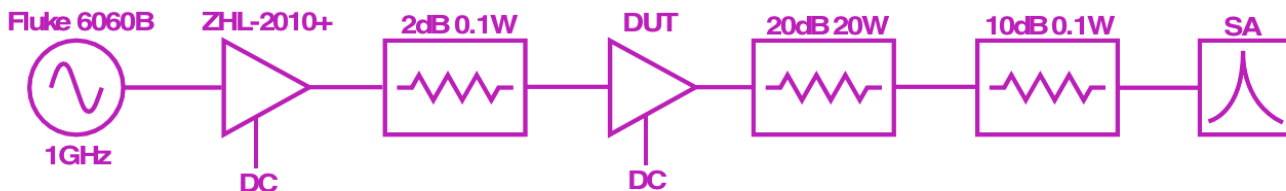
Figure 6.7: Test Setup for One-Tone Testing

A Minicircuits ZHL 2010+ amplifier is used as a driver for the DUT to provide sufficient input power. A 2dB attenuator is placed between the driver amplifier and the DUT to improve the input return loss for testing. An isolator would be the ideal solution, but was unavailable. The signal source power was increased while monitoring the driver output power until it reached +24dBm, the maximum drive level allowed by the competition. The driver amplifier was then connected to the DUT and the DUT bias was turned on. The output was measured on the spectrum analyzer, and is shown in figure 6.8.
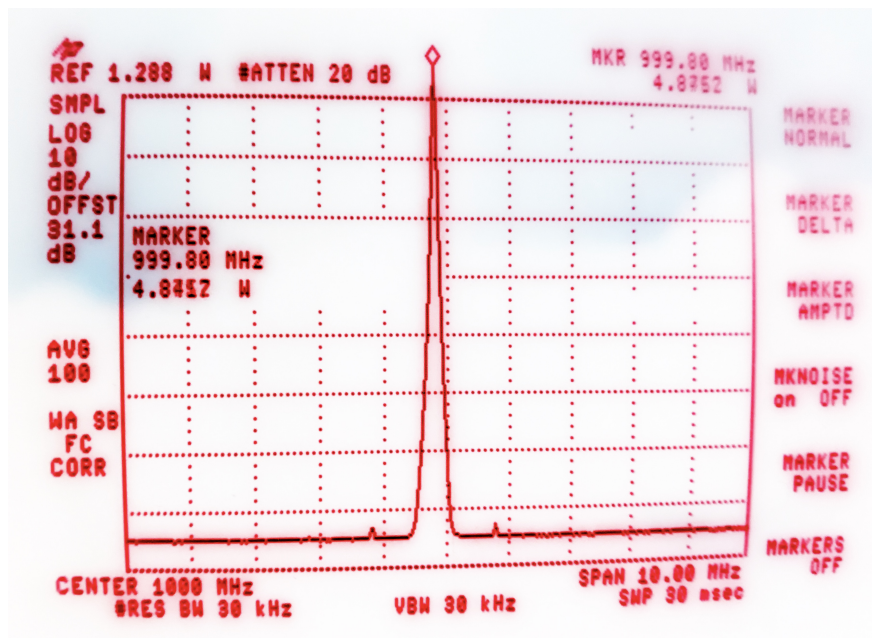
Figure 6.8: Single Tone Amplifier Output

Table 6.1: One-Tone Data

Parameter	Value	Units
V_{GS}	-3.0	V
V_{DS}	28	V
I_D	200	mA
P_{DC}	5.6	W
P_{IN}	0.25	W
P_{OUT}	4.84	W
PAE	81.9	%

Table 6.1 summarizes the measured data for the single-tone test. The amplifier delivers 4.84W (meeting contest requirements) with a PAE of 81.9%.

6.4 Two-Tone Testing

The goal of the two-tone test is to measure the amplifier's efficiency while meeting the contest linearity specification. Two tones spaced 20MHz apart are applied to the DUT. The input power is reduced until third order spurs are 30dBc below the carrier. The amplifier's PAE is then measured at this drive level. Figure 6.9 shows the two-tone test setup.
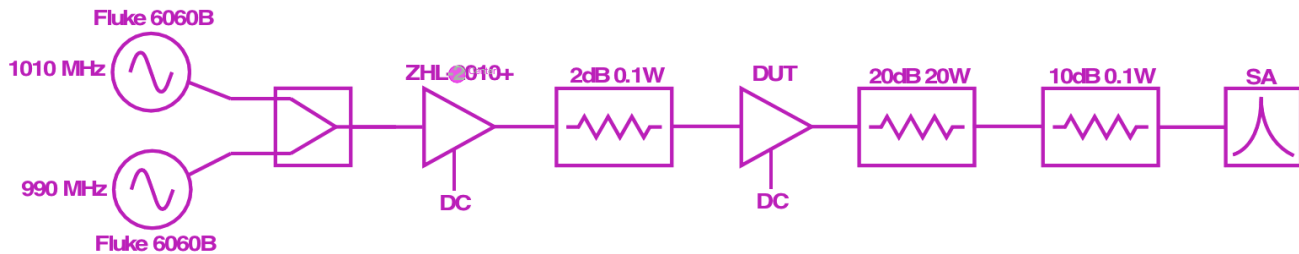
Figure 6.9: Test Setup for Two-Tone Testing

Figure 6.10 shows the amplifier's output spectrum for the two tone test.
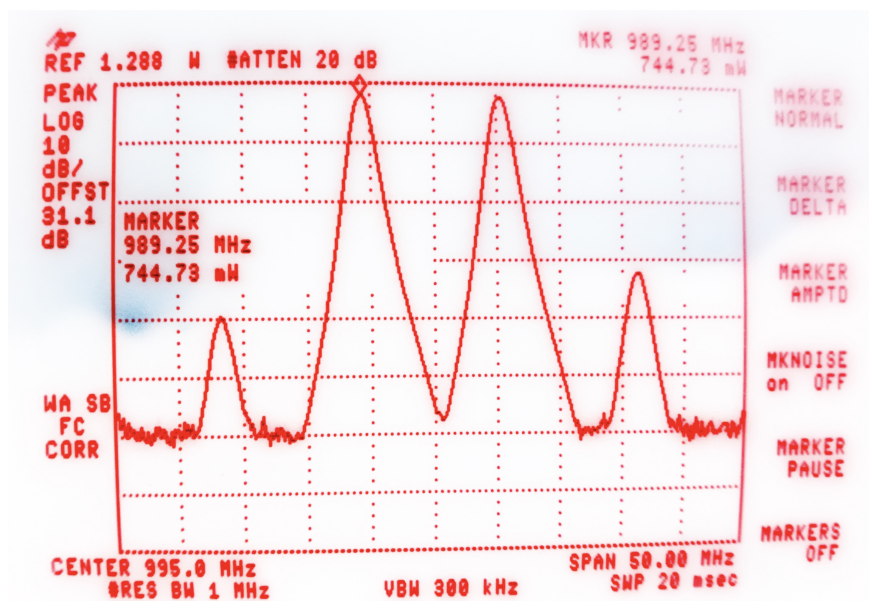
Figure 6.10: Two Tone Amplifier Output

Table 6.2: Two-Tone Data

Parameter	Value	Units
V_{GS}	-3.0	V
V_{DS}	28	V
I_D	130	mA
P_{DC}	3.64	W
P_{IN}	38.1	mW
P_{OUT}	2×744.73	mW
PAE	38.7	%

Figure 6.11 verifies the input power for the two tone test, and ensures that the 3rd order products of the driver amplifier are negligibly small and may be ignored. Figure 6.12 verifies that the 3rd order products of the DUT are 30dB below the carrier, as specified in contest rules.
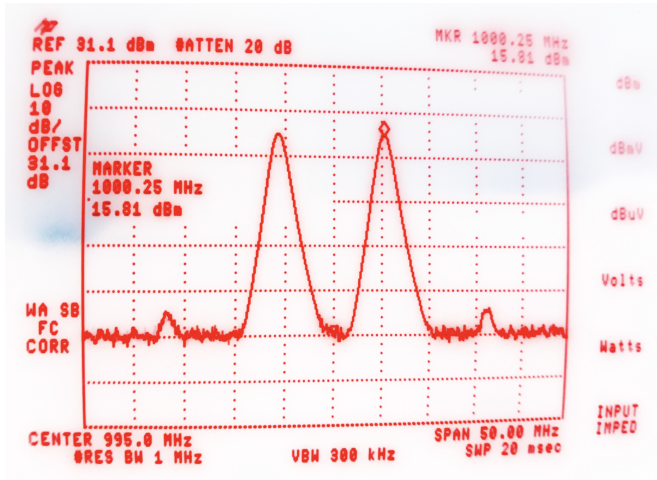
Figure 6.11: Two Tone Test Input Signal
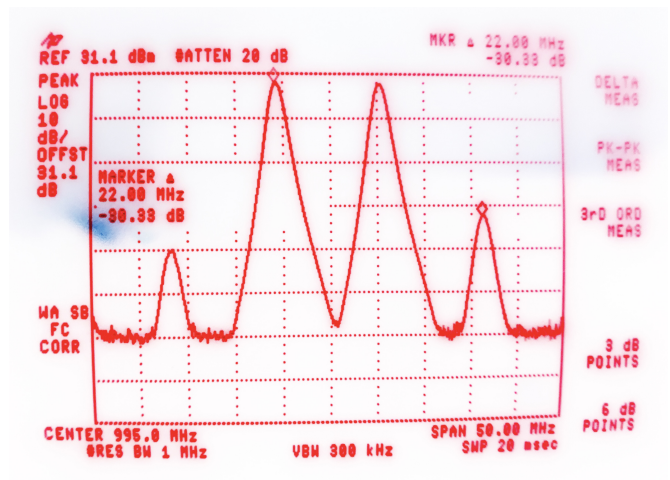
Figure 6.12: Two Tone Test IMD Measurement

6.5   Thermal Testing

Inspecting the amplifier with a thermal camera during operation can reveal where efficiency losses occur by visually identifying hot regions of the circuit and suggesting areas to improve heat-sinking. Figure 6.13 shows a thermal image of the amplifier during operation.
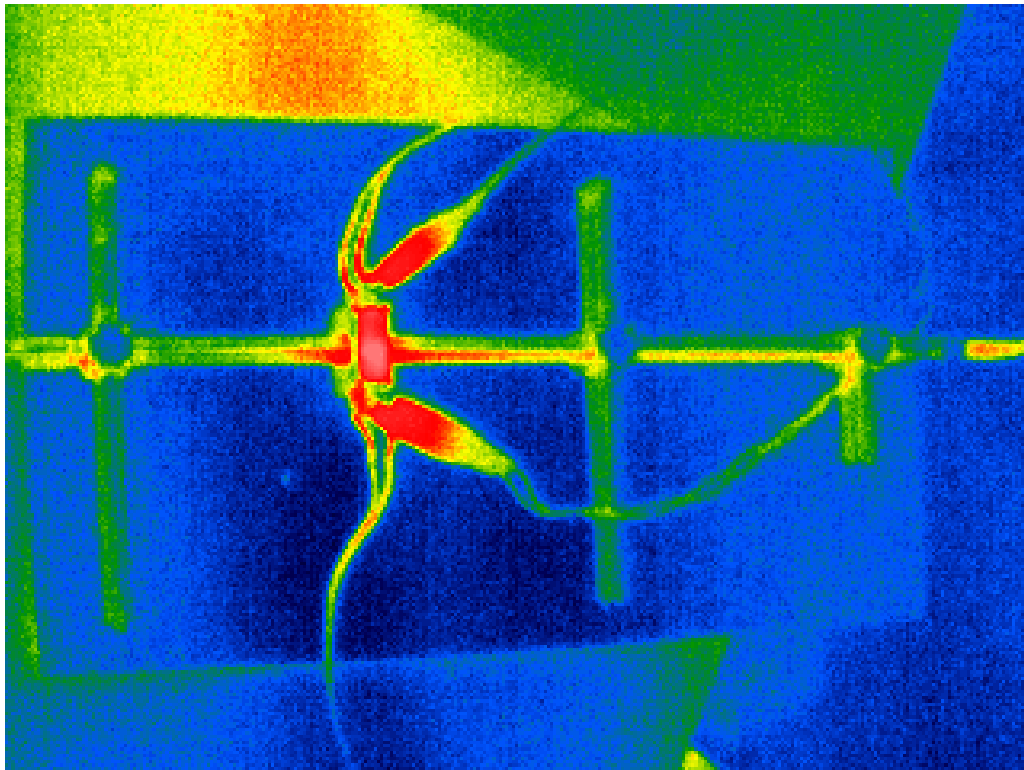
Figure 6.13: Thermal Image of the Amplifier

This image shows that the majority of heat is produced at the device mount, which is expected.

The output cable (right side) also has an elevated temperature and appears to be dissipating power. The bias connections at the top and bottom of the device mount are also hot due to the flow of current.

Figure 6.14 shows a closeup of the device mount.
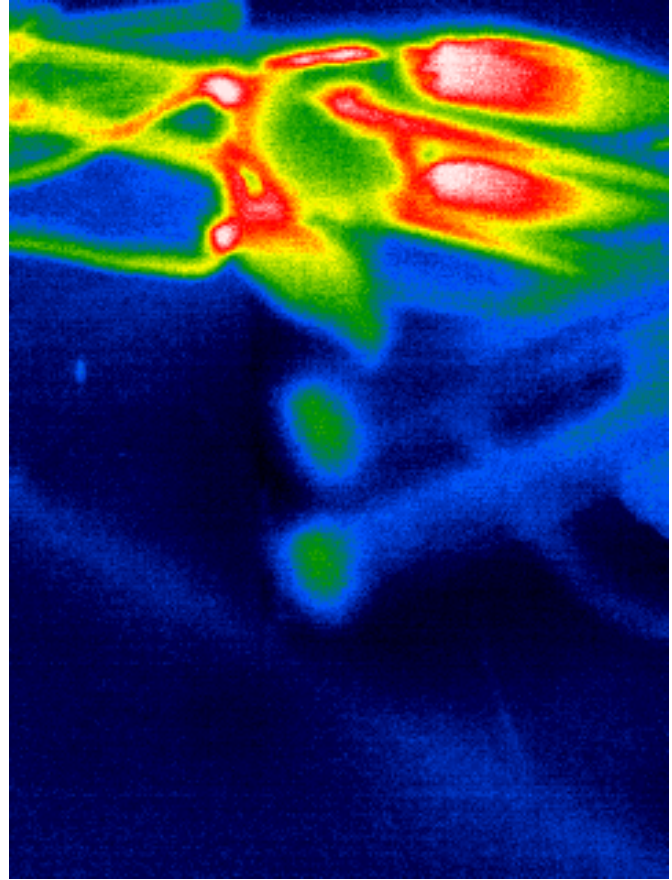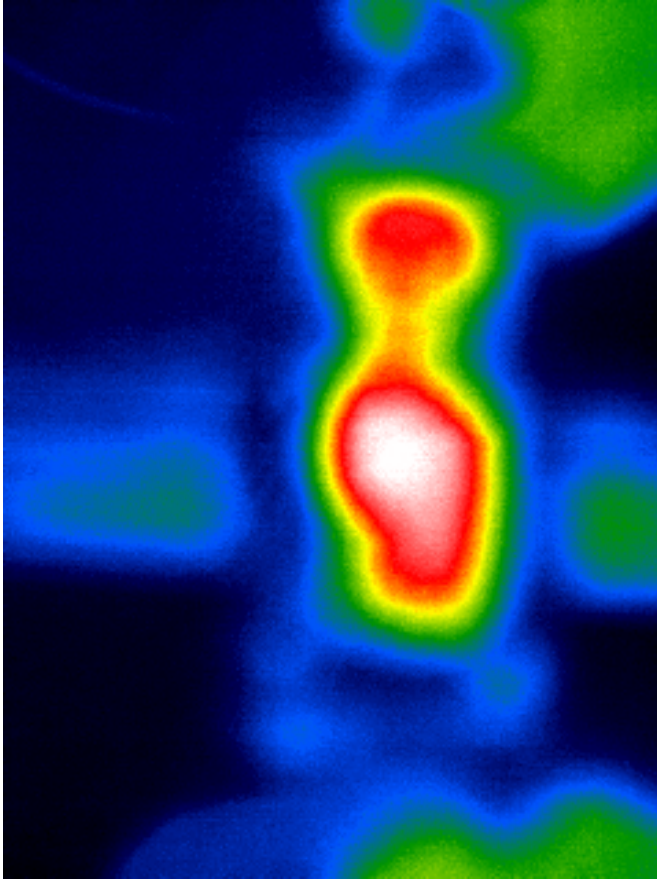
Figure 6.14: Thermal Image of the Device Mount   Figure 6.15: Thermal Image of a Shorting Plug

The large hot area is in the vicinity of the drain bias choke. The choke is uncomfortably hot to the touch during operation. A thicker wire gauge should have been used for the choke to decrease resistance. The current choke appears to dissipate substantial power.

Figure 6.15 shows a closeup of one of the shorting plugs at the ends of the short circuit stubs. The shorting plug (center, reflection is off the mounting plate) has an elevated temperature due to high surface currents at the short circuit. Heat is generated at the short circuit due to electrical resistance of the copper. This suggests that a more conductive material (like silver) might be able to reduce loss at the ends of the stubs. Alternatively, open circuit stubs could be tested, since they do not have high surface currents at their ends.

Chapter 7

Conclusion

7.1   Results Summary

The class F amplifier satisfied the IMS competition requirement of 4W output power by producing 4.84W while providing 81.9% PAE. During two-tone testing, the amplifier produced 1.49W while providing 38.7% PAE. This dramatic reduction in PAE is due to the reduction in input drive level required to meet the specified -30dBc IMD_3. With insufficient input drive, the amplifier does not produce strong enough harmonics to build the class F waveforms.

The competition rules, requiring efficiency while meeting a linearity specification, highlight a key trade off in engineering design. There is no free lunch. More power is required to obtain better linearity and signal fidelity. The competition is all about finding the "sweet spot" between the two that results in the highest figure of merit possible.

In the introduction section, the figure of merit was defined as $FOM = PAE(\%) \times [Freq(GHz)]^{0.25}$. Since the amplifier operates at 1GHz, no frequency weighting bonus is applied. The final amplifier then has a FOM of **38.7**.

7.2   Future Work

Several future improvements could be made to the amplifier to boost its performance and make the design more robust.

1. Input Matching Network - Excluding the input matching network did not significantly decrease the PAE, but it did destroy the input return loss. S-Parameter simulation in ADS showed an input return loss of about 1dB at 1GHz, which necessitated the 2dB attenuator between the driver amplifier and the DUT to absorb reflections. An input matching network would eliminate the need for an attenuator, and could boost PAE by 1-2%.

2. Stability improvements - While the shunt gate resistor stabilized the amplifier, it is still

possible to induce oscillations by starting the drain bias too quickly or powering on with an input signal present. The nature of these oscillations is unknown because they seem to be above the 1.5GHz top frequency of the spectrum analyzer used in testing. Stabilizing the amplifier at higher frequencies would make it more robust and easier to work with.

3. Bias Choke - The drain bias choke seems to dissipate significant power. Winding a new bias choke with thicker gauge wire would eliminate this problem, and might improve efficiency and output power. If the choke has too much resistance, it will not only dissipate power, reducing efficiency, but also reduce the drain voltage of the FET, limiting output power. This might be why simulation predicted an output power of +39dBm, but the measured output was only +36.8dBm.

4. Bias Connectors - Bannana plugs for bias connections have not been obtained as of the time of this report, and are required to make the amplifier eligible to compete in the IMS competition. They will be added before the competition.

5. Device Enclosure - The device mount currently has no top cover, and is free to radiate power. Adding a metal cover will reduce radiation losses.

6. Conductor Surface Finish - Further polishing of the inner and outer conductors could reduce electrical losses, and may improve amplifier efficiency.

7. Test Equipment - A spectrum analyzer and power meter were used to measure the amplifier's output power. While reasonable agreement was obtained between the two, neither instrument has been calibrated within 20 years. Test equipment drifts over time, so to obtain the most accurate results, a freshly calibrated instrument should be used for testing.

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Appendix A

Project BOM

Qty	Item	Supplier	Part Number	Unit Price	Total Price
1	0.5"x0.5"x12" Super-Conductive 101 Copper Bar	McMaster-Carr	3350K221	$33.94	$33.94
1	0.5"x0.25"x12" Super-Conductive 101 Copper Bar	McMaster-Carr	3350K211	$17.28	$17.28
1	3/8" 12"lg Round Super-Conductive 101 Copper Bar	McMaster-Carr	8965K14	$15.01	$15.01
3	0.25" OD 0.18" ID 12" lg Super-Conductive 101 Copper Tube	McMaster-Carr	8965K24	$4.45	$13.35
3	0.062" OD 0.035" ID 12" lg Super-Conductive 101 Copper Tube	McMaster-Carr	7190K51	$2.93	$8.79
1	Cree GaN HEMT FET (Free Sample)	Cree	CG2H40010F	$0.00	$0.00
-	Various SMT Capacitors	Cal Poly	n.a.	$0.00	$0.00
-	Assorted Wire	Cal Poly	n.a.	$0.00	$0.00
2	SMA Jack-Jack Connector	DigiKey	ACX1242-ND	$5.48	$10.96
					$99.33

Appendix B

Prototype Amplifier

In Winter quarter, a prototype amplifier operating at 2GHz was built to become familiar with design and test procedures for class F amplifiers. While the process is not covered in detail here, an overview is provided.

B.1 Construction

With the design complete, the class F amplifier was constructed in hardware. Semi-rigid coax was used for all transmission lines and stubs. $1\mu F$ 0603 chip capacitors were used to short circuit the wave shaping stubs and biasing stubs, as well as to provide input and output AC coupling. RF chokes (for biasing) were constructed by winding 20 turns of magnet wire using a piece of semi-rigid coax as a mandrel.

Two pieces of circuit board material (single-sided) were cut to 4" x 6" and used as ground planes on which to build the circuit. The FET was mounted on a 0.062" brass shim for proper height. Each circuit board was soldered at the edge to the brass shim to ensure ground plane continuity. The entire assembly was mounted to a piece of 2" wide 0.125" thick aluminum plate to act as a heat sink. 6-32 machine screws were used to mount the circuit board material to the plate, and 4-40 machine screws were used to mount the FET to the shim. Finally, SMA connectors were added at the input and output for easy testing. The completed assembly is shown in figure B.1.
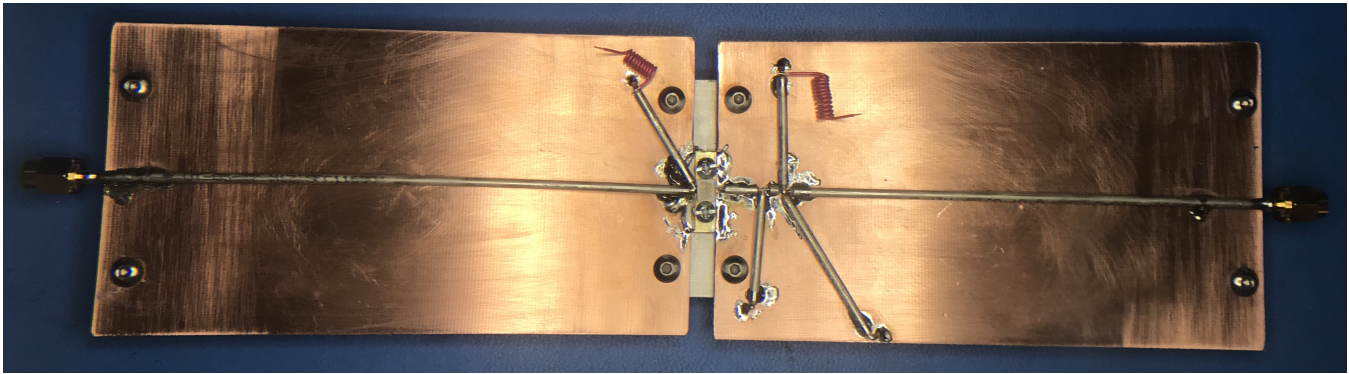
Figure B.1: Completed Class F Amplifier Prototype

B.2   Testing

After construction, the Class F amplifier was tested. The drain was biased at 28V (per datasheet recommendation). In order for the amplifier to operate as class F, the drain bias current must be small enough for the transistor to operate as a switch, rather than a linear amplifier. This is necessary to create harmonic content for the wave shaping network. A drain current of approximately 20mA is chosen as a good starting point. The FET's gate is biased at -3.0V, yielding approximately 20mA drain current.

A 2GHz, 0dBm signal was applied to the amplifier input. Figure B.2 shows the amplifier's output on the spectrum analyzer. Note that a 20W, 20dB pad was placed on the amplifier's output to protect the spectrum analyzer from excessive power.
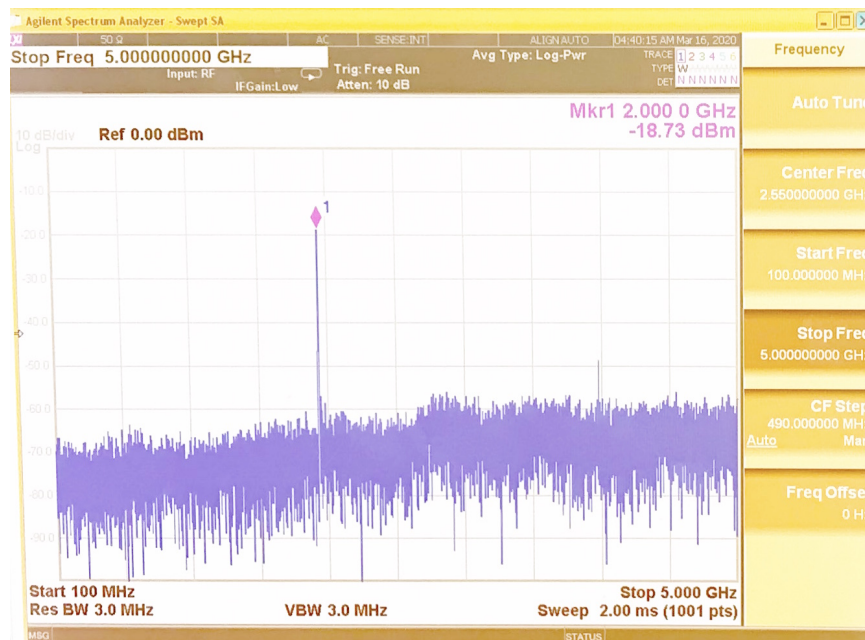

Figure B.2: Class F Amplifier Prototype Output

Compensating for the 20dB pad, the amplifier has an output power of 2.73dBm. This translates to a gain of 2.73dB. Both the output power and the gain are insufficient for the requirements of this project. With no matching networks at the input or output, significant power may be lost due to reflections, leading to reduced gain.

Figure B.3 shows the amplifier's output for the same input conditions but 50mA drain bias current.

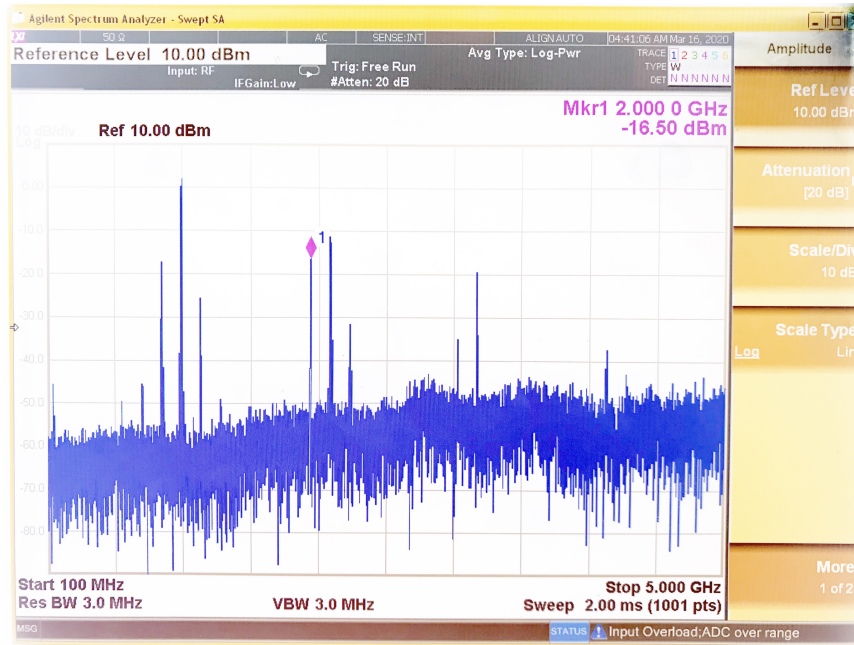Figure B.3: Class F Amplifier Prototype Output (unstable)

At this increased bias current, the amplifier becomes unstable and oscillates at approximately 1GHz. This is due to excess positive feedback in the circuit, which causes oscillations to become self-reinforcing.

Overall, this amplifier was not sufficient to meet the needs of the project, but provided a good starting point for the final design.

Appendix C

ABET Senior Project Analysis

Summary of Functional Requirements

This project serves as a general-purpose high-efficiency RF power amplifier with a center frequency of 1.0 GHz. Its purpose is to make weak signals stronger for processing, conditioning, or transmission. Typical applications for similar products include wireless operators such as WLAN and cellular devices. These devices often operate with battery power, making high-efficiency essential. This amplifier also has high linearity to ensure good signal fidelity over a broad range of input power levels.

Primary Constraints

The primary challenge anticipated is achieving high-enough power added efficiency to win the IMS 2020 design competition. Designing input and output matching networks and ensuring stability will also be challenging. High frequency circuits are very sensitive in general, so any design involving RF circuitry is typically challenging.

Economic Impacts

Human This project will have minimal impact on human capital, especially during the development phase. This amplifier likely would not be produced in high enough volume to significantly affect overall human capital.

Financial The financial impacts of this project are not well known, but sales would likely profit the designer. The capital required for development is minimal, given that my labor is free.

Manufactured or Real This amplifier requires physical manufacturing (obviously), and thus requires labor for construction.

Natural Capital This amplifier does consume non-renewable natural resources (those used in semi-conductor production), but the quantities are so small that it would not significantly affect the environment overall.

When and Where Costs and Benefits Accrue The costs of this project accrue primarily during the development phase, when capital and labor are required to design, test, and build prototypes. The benefits come in the form of sales after development.

Project Cost and Who Pays This project will cost approximately $10,588, including paid labor. The developer is covering the cost of the project, and labor is will be free.

If Manufactured on a Commercial Basis

If manufactured on a commercial basis, estimated amplifier sales would be 100 devices per year. The estimated manufacturing cost of each device is $20.00. The estimated purchase price of each device is $200.00. The estimated profit per year is $18,000.00. It is impossible to estimate the per-year operation cost for a device of this type, because it is entirely dependent on the usage rate, the cost of electrical power for the customer, and a multitude of other factors that remain unknown.

Environmental Impacts

This project uses non-renewable elements for semiconductor production. However, the usage rate is statistically insignificant, and does not present a threat to the environment. This amplifier shall be produced following proper hazardous waste disposal procedures, so no ecosystems should be damaged. Assuming any hazardous waste is properly disposed of and project materials are sourced from environmentally responsible suppliers, this project should not harm any other species.

Manufacturability

This device must be manufactured in an electrostatic discharge safe environment. This makes it more difficult to build these devices. It also requires substantial RF test equipment to properly verify performance, and a lot of this equipment would be needed for manufacturing, which might be expensive. In the development phase, equipment will be sourced from the Cal Poly EE Microwave lab as needed.

Sustainability

This project uses non-renewable elements for semi-conductor production, leading to potential sustainability issues. However, the usage rate is so slow that it is insignificant. There are also no viable alternatives that currently exist to manufacture a device of this type renewably. The completed device requires no maintenance and can theoretically operate forever if not damaged.

Ethical

Ethical issues with this project are limited. The project itself does not carry inherent ethical issues, but the customer's use of the product could be for unethical purposes e.g. espionage, electronic warfare, etc. It is impossible to know or control how customers will use a product, so there is no way to mitigate this problem. For example, manufacturing cellular equipment may lead to more texting and driving deaths, but we do not hold cellular operators responsible for accidents when they happen. Similarly, it is impossible for me to know how customers might use or misuse this amplifier, so there is no way I can be responsible for what they do with it.

Health and Safety

This project may emit RF radiation, which can be harmful in large enough doses. However, proper precautions, such as using terminations during operation, can successfully mitigate this danger. This project will also contain lead from solder. Assuming proper handling procedures (such as using a fume extractor and washing hands after working) are followed, the risk of lead poisoning should be minimal.

Social and Political

The social and political aspects of this project are not well known. Few similar products exist on the market, and it remains unknown to what uses this amplifier might be put. Ultimately, if this component is used successfully in a larger design, it may have significant social and political impacts, but they cannot be predicted at this time. I have no stakeholders in this case (I am developing the project alone).

Development

New tools used in the development of this project include Keysight's ADS simulation software, as well as Spectrum Analyzers and VNAs.