



**Electrical Engineering Department  
California Polytechnic State University**

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**Senior Project Final Report**

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**Efficiency Optimization of MISO Converter**

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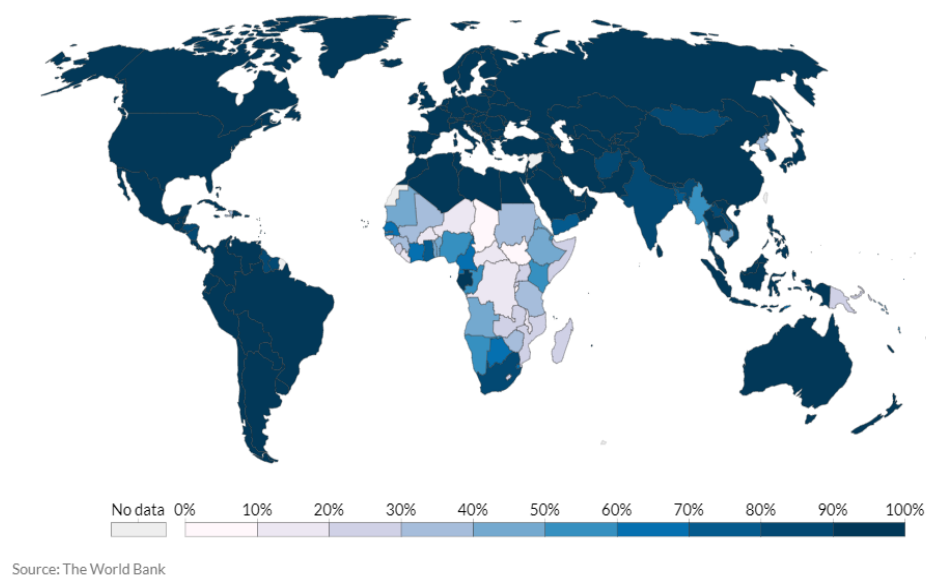
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## **Abstract**

In recent years, there has been a rapidly growing need for sustainable energy sources. This need comes from the increasing threat of climate change, significant population growth, as well as the effort to bring electricity to rural and underdeveloped areas across the world. The DC House project at Cal Poly aims to address these issues. The Multiple Input Single Output (MISO) converter is an integral part of the DC House project. The MISO converter is a system that connects multiple power sources to a DC bus. This allows the DC House to be powered by multiple types of renewable energy sources, including solar power, wind power, hydro power, and human power. The MISO converter has a nominal input of 24V and a nominal output of 48V with a maximum power rating of 150W. Improvements can be made to the current low-cost MISO to increase efficiency and decrease costs. Several considerations that can be implemented include but are not limited to component selections, board size and layout, and more relaxed design constraints especially for those requirements that were met with significant margin. This project entails the second revision of the low-cost MISO Boost converter incorporating improvements as previously mentioned. Simulation results of the proposed design show that the proposed design meet all design requirements including reduced cost and physical size. Hardware implementation unfortunately did not take place due to the COVID-19 pandemic which caused campus shutdown and thus our inability to access the power electronics lab.

## Chapter 1: Introduction

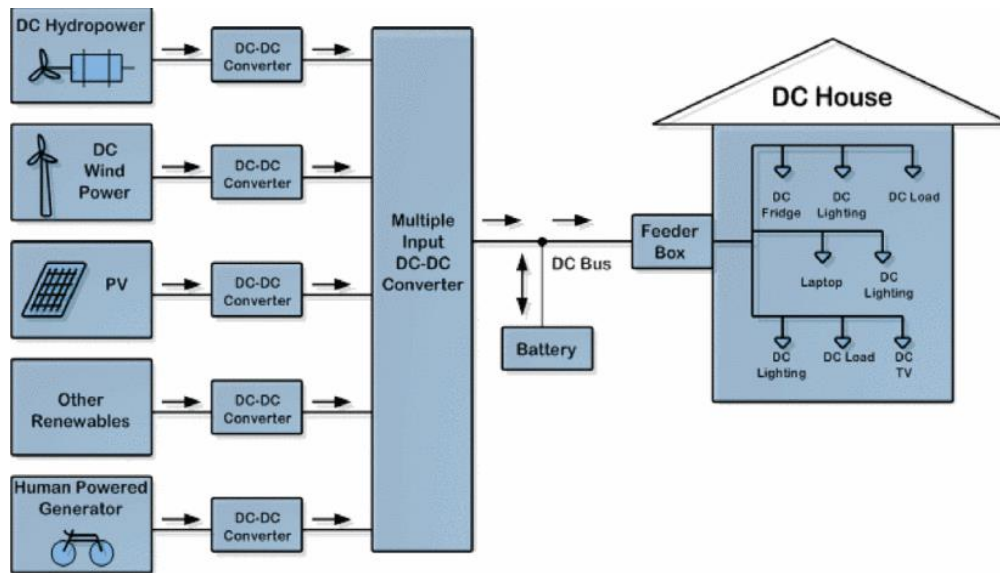
According to Our World in Data [1], 13% of the world was without electricity in 2016. While great growth has been made since the turn of the century, there are still some countries at less than a 75% electrification rate, such as Chad, which is currently around 9%. Access to this resource gives those less fortunate a better chance at improving their communities. Providing everyone with access to such a vital resource is a goal that we should all strive for. Our lives revolve around electricity. It is the resource that allows us to be more productive throughout the day; we have more time to work, maintain the household, and study for academics, among other things. The advancement of electricity has improved drastically over recent decades, with power electronics allowing access to new types of energy from renewable sources. By utilizing these renewable sources, electricity is used much more efficiently.



**Figure 1-1: Map of World Electrification Rates [1]**

The DC House Project at Cal Poly was created with the goal of providing electricity to underdeveloped or rural areas. The benefit of the DC House is that it can operate on a small scale, even at a single household level. This allows deployment of the DC House to not require a large undertaking, which could prove costly. The exclusion of AC power within the DC House eliminates the need to convert between both forms of electricity. This eliminates unnecessary power losses since some electrical power is lost when converting between AC and DC power. With most electrical appliances running on DC power, it would be inefficient to convert the DC inputs to AC power, only to convert them back to a DC output.

The DC House Project started up in September of 2010 with the goal of designing a system that runs DC loads sourced directly by low-power, low-voltage renewable energy DC sources [2]. Despite the benefit of the sustainability of these renewable energy sources, one issue with using these types of sources is that we cannot rely on them to constantly supply power. The reliability of renewable sources is escalated by being able to connect multiple variations of renewable energy to reliably power a single load. The Multiple Input Single Output (MISO) converter was therefore developed as an efficient and cost-effective way to allow multiple sustainable energy sources to power a single load. In addition to connection to the load, the MISO converter is also connected to a battery so that energy can be stored in the event that there is no power being supplied by any of the input sources and the sources are producing more energy than what the load demands.



**Figure 1-2: Block Diagram of the DC House project at Cal Poly [2]**

Since its inception, the DC House has been advancing through different stages of growth and improvement. Along with this, the MISO converter for the DC House has also been going through revisions and refinements with more work is still in progress to yield a MISO technology with improved performance while keeping the cost minimum.

## Chapter 2: Background

Our project hopes to address the previously mentioned issue of limited access to electricity in rural communities. Along with the DC House project, we aim to help provide these people with a resource that has become a necessity to survive in the modern world. It is imperative that we strive to create the most efficient converter possible because underutilizing energy in an area where that resource is scarce is wasteful and causes unnecessary financial strain on its citizens. Since the aim of the DC House is to be the main (or only) source of power supply for its users, it is imperative to create a reliable system. An important consideration for this project involves the fact that multiple generation sources could be used to charge batteries within the DC House. As such, providing a means to have multiple sources of power generation is key to the design of the converter.

Single sources of energy are not ideal for the problem we are attempting to solve due to the reliability of the sources. Our project will harness solar energy as one source to power the house. The popularity of solar energy is growing as society moves further away from coal towards cleaner, greener energy. Solar energy is also an obvious answer to moving away from nonrenewable energies such as fossil fuels because it is an inexhaustible energy. Although photovoltaic (PV) cells, which are used to harness solar energy, might not absorb sunlight all hours of the day, or most efficiently, sunlight is an energy we will not exhaust for the foreseeable future, unlike fossil fuels. Another important reason to look towards photovoltaic cells for the harnessing of solar energy is their improved efficiency. The most recent increase in efficiency for PV cells is a “record-breaking 26.3 percent efficiency—a 0.7 percent increase over the previous record” [3]. This improvement is significant as the efficiency is that much closer to approaching the max



efficiency of 29 percent for silicon PV cells. Although the PV cells are not currently the most efficient, they are slowly but surely heading in the right direction

However, solar energy on its own is not as reliable as we would like. When compared to coal, the traditional source of energy in the US, solar energy has a much smaller capacity factor. Capacity factor is a measure of the actual output power over a period of time compared to the maximum output power over the same amount of time. Solar energy has a capacity factor of 20% for photovoltaic power plants, while a coal plant has a capacity factor of 65-70% [4]. The discrepancy in the capacity factors is due to the limited amount of sunlight the solar panels can harness. Daytime amounts to about 12 hours a day, with even less sunlight on a cloudy day. The discontinuous production of energy using solar energy makes it an unreliable source on its own.

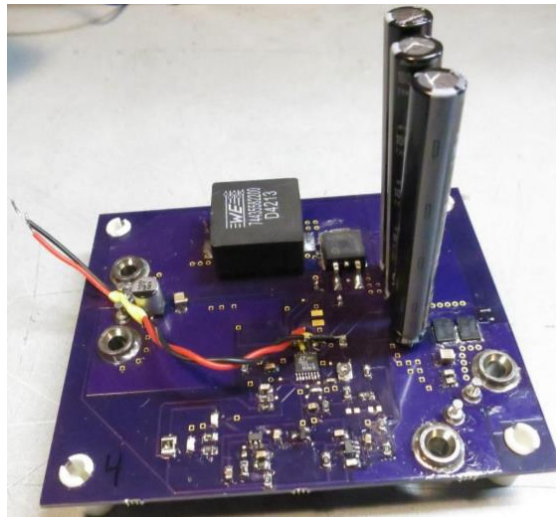
Another technology talked about on the topic of renewable energies are wind turbines. Harnessing wind energy is also a relatively new approach to move away from fossil fuels. Wind energy is natural and allows us to reduce our carbon footprint. Like solar energy, wind is also an inexhaustible energy produced by the earth harnessable by us. Once the wind turbines and infrastructure for converting the energy is installed, the turbines would simply need to be maintained. Another assuring trend in the use of wind turbines is the increase in efficiency the technology has had over the years. Pre-1988, wind turbines were almost as inefficient as solar PV cells with a capacity factor of 20 percent. However, as early as 2004, the capacity factor for wind turbines rose to 36 percent [5]. The increase in efficiency of wind turbines demonstrates that although this technology is young and inefficient, it is slowly improving and proving itself to be a viable option for our energy needs.

Like solar energy, wind energy is also not entirely reliable. Wind turbines capacity factor is approximately 25 to 30 percent, which is much lower than the coal's power factor [2]. The

reason for the low reliability is the intermittency of wind over time. One way the industry has attempted to rectify the issue of reliability is connecting multiple turbines in parallel over vast areas to guarantee more consistent output power [6].

Alone, these renewable technologies are not reliable. Both are subject to the intermittency and fickleness of the atmosphere that affects how much wind and solar energy can be harnessed. Together, however, the reliability of the overall system increases. Multiple sources to a system will allow a diversification of our energy, so when one source falters, another might possibly provide energy to the system [7]. The multiple-input single-output (MISO) converter of the DC House accomplishes just that; a system with multiple, parallelable inputs for an increase in reliability for power conversion over a single input source.

The MISO converter is a specialized component for the Cal Poly DC House project, and there have been many previously proposed designs for it. The direct comparison of our final product will be to the prior designs. Our project aims to be the preferable design in terms of cost and performance. Some past designs utilized flyback or full-bridge converters to step-up the input voltage. Both the flyback and full-bridge converters offer the ability to step up DC voltages; however, there were problems encountered with each of these designs in previous iterations. These topologies also require the use of more components which would result in a loss of efficiency and an increase in cost. Our design will utilize a boost converter topology based of a previous iteration of the MISO converter designed presented in [8] and attempt to reduce its overall cost, as shown in Figure 2-1. Reaching this goal will allow the use of a low-cost DC House system in rural areas across the world.



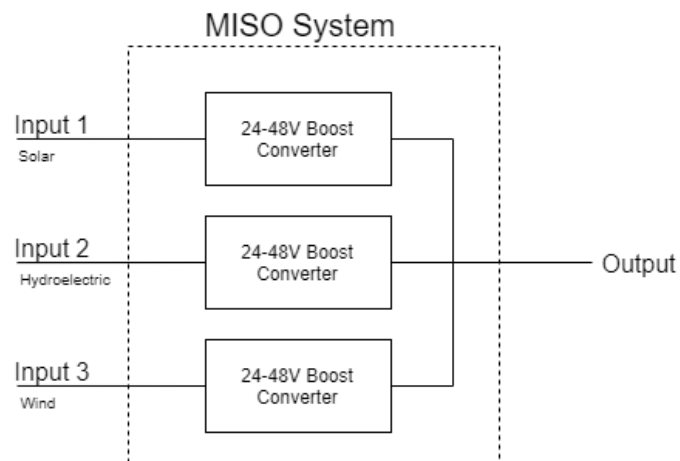
**Figure 2-1: Previous Boost MISO converter [8]**

In this project, we will design and build the low-cost MISO converter based on the previous design presented in [8]. Besides lowering the cost, another objective of this project is to decrease the size of the MISO board and its components. This will also allow us to lower the cost of production per board.

In summary, this project will modify the most recent MISO converter design for the DC House project to reduce the overall cost of the MISO converter. Computer simulation will be used to verify the modified design followed by hardware construction and test to evaluate its operation and performance. Cost analysis of the modified will also be conducted to determine the final cost of the MISO board and the amount of cost saving compared to the previous design.

## Chapter 3: Requirements

By definition, the MISO will take multiple DC inputs and connect them to a single DC output. We are working with a low-cost version of the MISO; thus, our design will implement an identical boost converter for each stage. As each input will be handled by its own separate converter, it is crucial that the outputs of these boards be parallelable so that they may run a single load. Figure 3-1 shows a level 0 block diagram of the MISO converter for a case with three different inputs. Each 24-48V Boost converter will have an identical design and be connected at the output. The MISO converter should be able to operate with any number of the inputs supplying power at a given point in time. This creates a more reliable system for our user, where their access power will not be limited by changing conditions. However, due to cost constraint this project will design and construct a total of 4 MISO converters, all paralleled to a single output.



**Figure 3-1: Level 0 Block Diagram**

To reduce the cost to our customers, it is necessary to maintain a low production cost for the MISO converter. The price of manufacturing should not exceed \$50 per board. One way to help reduce the price per board is to improve the board layout so that we may decrease the overall

size of the board. The final design for each converter should be within the dimension of 3"x3"x0.75". This will also allow us to meet the physical requirement of a compact and stackable design. Multiple MISO converter boards should be able to be stacked and stored in a neat wall-mounted fixture. This will not only create a more aesthetically pleasing product for our customers, but also make it more well-organized and easily accessible. This will make it easier for users to manage and upkeep the converter.

Each board will have a nominal input voltage of 24V. Each converter should maintain ideal operations when the source voltage is within +/-2V of the nominal input voltage. The nominal DC output voltage of each board will be 48V. To preserve the DC output characteristics, the peak-to-peak ripple of the output voltage waveform should remain below 5% of the average output voltage. Because we are working with a boost converter design, the input voltage to each board should not exceed 48V. The maximum power rating of the converter will be 150W, leading to an approximate output current of 3.125A at full load conditions.

To maintain minimum loss within each converter, the efficiency of the converter should larger than 85% at full load. This is important as high efficiency means low power will be consumed by the converter which further minimize the cooling requirement of the converter, thus reducing the overall cost. Since the minimum input voltage is 22V, the 85% efficiency requirement will result in a maximum input current of approximately 8A.

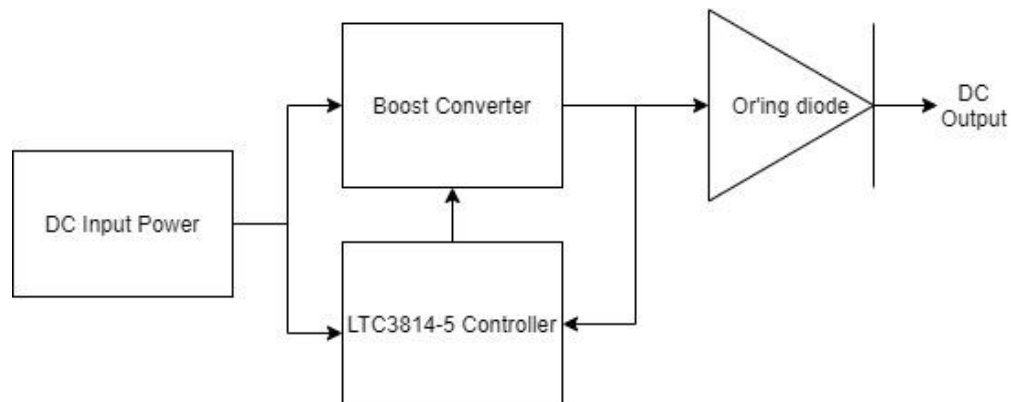
Table 3-1 summarizes all the design requirements for this project. The main strategy to achieve these requirements is through improving the board layout and resizing of components.

**Table 3-1: Summary of Requirements**

<b>Parameter</b>	<b>Requirement</b>
Board Dimension	3"x3"x0.75"
Price per Board	<\$50
Nominal Input Voltage	24V $\pm$ 2V
Average Output Voltage	48V
Maximum Output Power	150W
Input Current Rating	< 8A
Output Current Rating	3.125A
Peak-to-Peak Ripple	<5% Output Voltage
Line Regulation	<5%
Load Regulation	<5%
Efficiency at Full Load	>85%

## Chapter 4: Design

This MISO converter is designed so that each input goes through an identical conversion circuit and is paralleled at the output. A level 1 block diagram of a single stage is shown in Figure 4-1. Each DC power supply is input to a boost converter and it is also used to power the controller. This controller monitors the feedback of the boost converter and outputs the signal to the switches accordingly. An OR-ing diode is placed between the output of each DC converter and the overall DC output of the MISO so that no current can flow back into any stage when its power supply is off. It is important that the feedback is taken before the OR-ing diode to prevent the separate stages from interrupting the operations of each other when coming on and off. For the voltage conversion stage, a boost converter topology was decided upon. This allows for a simpler design which lowers the price for this low-cost design. The LTC3814-5 controller was chosen based on price, efficiency, and operating voltages.



**Figure 4-1: Level 1 Block Diagram of MISO**

The duty cycle for a boost converter is found using the input and output voltages to determine the transfer function of the converter. The transfer function can be found using the Volt-Second Balance (VSB) Method as shown in Equation 4-1. This method uses the fact that there is an approximate conservation of energy in an inductor as it charges and discharges. As shown in Equation 4-2, the minimum input voltage,  $V_{in-minimum}$ , is used to find the maximum duty cycle,  $D_{max}$ . Additionally, to calculate a more realistic value for the duty cycle, efficiency  $\eta$ , is included in the duty cycle equation to account for the losses in the non-ideal converter. The maximum duty cycle is found using Equation 4-3.

$$VSB = v_{Lon}t_{on} + v_{Loft}t_{off} = 0 \quad \text{Eq. 4-1}$$

$$v_{Lon}TD + v_{Loft}T(1 - D) = 0$$

$$V_{in}DT + (V_{in} - V_o)(1 - D)T = 0$$

$$V_{in}D + V_{in} - V_o - V_{in}D + V_oD = 0$$

$$V_{in} - V_o + V_oD = 0$$

$$V_{in} - V_o(1 - D) = 0$$

$$V_o = \frac{V_{in}}{(1-D)}$$

$$V_o = \frac{V_{in-minimum}*\eta}{(1-D_{max})} \quad \text{Eq. 4-2}$$



$$V_o(1 - D_{max}) = V_{in-minimum} * \eta$$

$$V_o - V_o D_{max} = V_{in-minimum} * \eta$$

$$V_o D_{max} = V_o - V_{in-minimum} * \eta$$

$$D_{max} = 1 - \frac{V_{in-minimum} * \eta}{V_o} = 1 - \frac{22V * (0.85)}{48V} = 0.61 \quad \text{Eq. 4-3}$$

The average inductor current,  $I_L$ , can be found relating efficiency with the input current,  $I_{in}$ . In a boost converter, the inductor is connected to the input voltage, so the average inductor current is the same as the average input current. To find the input current, the input power,  $P_{in}$ , is used. The equation for efficiency is shown in Equation 4-4. Using the efficiency of 85% as shown in the product specifications, the average inductor current can be found using Equation 4-5.

$$\eta = \frac{P_o}{P_{in}} \quad \text{Eq. 4-4}$$

$$P_{in} = \frac{P_o}{\eta} = \frac{150W}{0.85} = 176.5W$$

$$P_{in} = V_{in} I_{in} = V_{in} I_L$$

$$\text{Eq. 4-5}$$

$$I_L = \frac{P_{in}}{V_{in}} = \frac{176.5W}{24V} = 7.35A$$

The inductor ripple,  $\Delta i_L$ , can be found using the inductance solved for previously and the desired percent inductor ripple. A typical inductor current ripple of 20% was chosen. Equation 4-6 shows the calculation of the inductor ripple current.

$$\Delta i_L = \%ripple * I_L = 0.2 * 7.35A = 1.47A \quad \text{Eq. 4-6}$$

The waveform of the inductor current is triangle wave, with the difference between minimum and maximum values of the waveform being the inductor ripple current, while the average inductor current is a value somewhere towards the middle of these two values. Using the inductor ripple current, the maximum inductor current,  $i_{Lmax}$ , is found by adding half the inductor ripple to the average inductor current as shown in Equation 4-7.

$$i_{Lmax} = I_L + \frac{\Delta i_L}{2} = 7.35 + \frac{1.47}{2} A = 8.09A \quad \text{Eq. 4-7}$$

The critical inductance is found by using the inductor voltage,  $V_L$ , and ripple current. Using Equation 4-8, the inductance can be related to the inductor's ripple current and the input voltage. The equation uses the variables when the inductor is charging to find the critical inductance.

$$L \frac{\Delta i_L}{dt} = V_{in} \quad \text{Eq. 4-8}$$

$$L_c = \frac{\Delta t_{on} V_{in}}{\Delta i_L} = \frac{V_{in} D T}{\Delta i_L} = \frac{V_{in} D}{\Delta i_L f} = \frac{24V * (0.61)}{1.47A * (320kHz)} = 3.11\mu H$$

When selecting the inductor for the boost converter, one should pick an inductor that is comfortably larger than the critical inductance to make sure the converter operates correctly. When attempting to select an inductor there were none readily available on electronic retailer sites that met the inductance and current requirements. The inductor size was gradually increased until finding an inductor meeting both inductance and maximum current requirements found on [www.digikey.com](http://www.digikey.com).

The switches are the next component sized. Our design uses synchronous switching, requiring a high-side (HS) MOSFET and a low-side (LS) MOSFET that replaces the diode in a traditional, nonsynchronous boost converter. The current ratings for the low-side and high-side

MOSFETs are calculated using equations 4-9 and 4-10, respectively. The low-side switch current,  $I_{LS-SW}$ , is derived from the inductor current, as the inductor is connected to the input while the low-side switch node is connected to the other end of the inductor. The switch receives current from the inductor when the switch is closed meaning the average switch current can be related to the average inductor current as shown in Equation 4-9.

$$I_{LS-SW} = I_L * D = 7.35 * (0.61) A = 4.48 A \quad \text{Eq. 4-9}$$

The high-side switch current,  $I_{HS-SW}$ , can be found in a similar fashion. As the inductor discharges, it sources current through the high-side switch to the output, complimenting the low-side switch current. The average high-side switch current is shown in Equation 4-10. Note that the high-side switch current is equal to the maximum output current.

$$I_{HS-SW} = I_o = I_L * (1 - D) = 7.35 * (1 - 0.61) A = 2.87 A \quad \text{Eq. 4-10}$$

The low-side switch voltage rating,  $V_{LS-SWmax}$ , can be found when the low-side switch is in its off state. When off, one side of the switch is shorted to ground while the other is shorted to the high-side switch. Since the high-side switch is on, there is virtually no loss across the high-side switch. With little loss across the high-side switch while on, the low-side switch node connected to the high-side switch has an effective voltage of  $V_o$ . Taking the desired output voltage ripple of 5% into account, the maximum low-side switch is calculated using Equation 4-11.

$$V_{LS-SWmax} = \underline{V_o} + \frac{\Delta V_o}{2} = 48 + \frac{2.4}{2} V = 49.1V \quad \text{Eq. 4-11}$$

Similarly, the high-side switch voltage rating,  $V_{HS-SWmax}$ , can be found when it is in its off state. In this state, the low-side switch node shorts the inductor to ground while the other side of the open created by the off high-side switch is connected directly to the output. Taking the output

voltage ripple into account, the maximum switch voltage for the high-side switch is calculated using Equation 4-12.

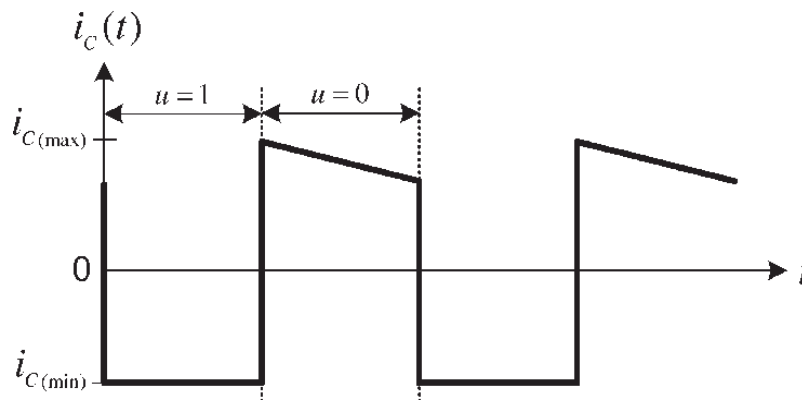
$$V_{HS-SWmax} = \underline{V_o} + \frac{\Delta V_o}{2} = 49.1V \quad \text{Eq. 4-12}$$

The next component sized is the output capacitor,  $C_{out}$ . The critical output capacitance can be found using the output capacitor current waveform. Through Kirchhoff's Current Law (KCL), one can find the relationship between the inductor, capacitor, and high-side switch currents using Equation 4-13.

$$i_{HS-SW}(t) = i_c(t) + i_o(t) \quad \text{Eq. 4-13}$$

$$i_c(t) = i_{HS-SW}(t) - i_o(t)$$

The resulting waveform is trapezoidal as depicted in Figure 4-2 [6]. Using Amp-Second Balance of a capacitor in DC steady-state, the sum of the negative and positive areas of the waveform are equal as energy must be conserved in ASB.



**Figure 4-2: Output Capacitor Current Waveform [9]**

The area of charge of the bottom waveform can be found using Equation 4-14, with the lower current being the average high-side switch current.

$$\text{Area of } q = C_o \Delta V_o \quad \text{Eq.4-14}$$

$$I_{HS-SW} * t_{on} = C_o \Delta V_o$$

$$C_o = \frac{I_{HS-SW} * DT}{\Delta V_o} = \frac{I_{omax} * D}{\Delta V_o f} = \frac{10A * (0.61)}{(2.4V) * 320kHz} = 7.9\mu F$$

The output capacitor is connected in parallel to the output, so the voltage rating can be found using the output voltage and output voltage ripple as shown in Equation 4-15.

$$V_{output-capmax} = V_o + \frac{\Delta V_o}{2} = 49.1V \quad \text{Eq. 4-15}$$

The RMS current of the output capacitor is found by utilizing both the AC and DC current of the high-side switch as seen in Figure 4-2. The equations for the AC and DC components were found in [10].

$$i_{co-rms} = i_{HS-SW-rms} = \sqrt{i_{HS-SW-ac}^2 - i_{HS-SW-avg}^2} \quad \text{Eq. 4-17}$$

$$i_{co-rms} = \sqrt{[I_L \sqrt{(1-D)} * \sqrt{1 + \frac{1}{3} [\frac{\Delta i_L}{2I_L}]^2}]^2 - [I_L (1-D)]^2}$$

$$i_{co-rms} = I_L \sqrt{[\sqrt{(1-D)} * \sqrt{1 + \frac{1}{3} [\frac{\Delta i_L}{2I_L}]^2}]^2 - [(1-D)]^2}$$

$$i_{co-rms} = I_L \sqrt{[(1 - D) * (1 + \frac{1}{3} [\frac{\Delta i_L}{2I_L}]^2)] - [(1 - D)]^2}$$

$$i_{co-rms} = 7.35A * \sqrt{[(1 - 0.61) * (1 + \frac{1}{3} [\frac{1.47A}{2 * 7.35A}]^2)] - [(1 - 0.61)]^2}$$

$$i_{co-rms} = 3.6A$$

For the input capacitor, an input voltage ripple was not specified as a parameter the converter should meet, so the team decided on a value of 5%. Since the input capacitor is connected in parallel to the input, the voltage across the capacitor can be related to the input voltage and input voltage ripple as shown in Equation 4-18.

$$V_{in-capmax} = V_{in} + \frac{\Delta V_{in}}{2} = 24 + \frac{1.2}{2} V = 24.6V \quad \text{Eq.4-18}$$

The critical capacitance can be found in a similar fashion to the output capacitance. The average capacitor current is equal to zero when adhering to Amp Second Balance, meaning the capacitor current is solely the triangular portion of the inductor current since it is connected to the input in parallel. Equation 4-19 uses the area under the triangular waveform of the input capacitor to relate the charge of the capacitor to its capacitance.

$$\text{Area of } q = C_{in} \Delta V_{in} \quad \text{Eq.4-19}$$

$$\frac{1}{2} * \frac{\Delta I_L}{2} * \frac{T}{2} = C_{in} \Delta V_{in}$$

$$C_{in} = \frac{\Delta I_L * T}{8 \Delta V_{in}} = \frac{\Delta I_L}{8f \Delta V_{in}} = \frac{1.47A}{8 * 320kHz * 0.6V} = 957nF$$

The input capacitor RMS current is found using its current waveform. Using the equations for common waveforms found in [10], the RMS current can be found as shown in Equation 4-20.

$$i_{cin-rms} = \frac{i_{cin}(t)}{\sqrt{3}} = \frac{(\Delta i_L/2)}{\sqrt{3}} = \frac{\Delta i_L}{2\sqrt{3}} = \frac{1.47A}{2\sqrt{3}} = 0.43A \quad \text{Eq. 4-20}$$

A summary of the design equations and calculated values can be found at the end of this chapter in Table 4-2.

One aspect when deciding what components to use is price. Because the scope of our project is a low-cost converter, it is imperative to find components that meet the requirements while still maintaining a reasonable price for our customers. When updating the component selections from the previous design, the main components contributing to the price were the transistors, and PCB. Although the price difference between newer components and the older ones might not be significant, small reductions in price across multiple components will reduce the overall price greatly.

The two main transistors in the previous converter design priced at \$3.90 each, contributing to \$7.80 to the cost of the converter. Cheaper transistors for the high-side and low-side transistors were found at prices of \$1.21 and \$1.79, costing \$3.00. The newer transistors reduced the contribution of the switches to the cost by \$4.80, or 7.8% of the total board cost.

Although low price is a desired characteristic for the converter, another characteristic to consider is compactness of the MISO. Since the converter uses multiple inputs, multiple boost converters are used with outputs that are parallelable. To further reduce size of the overall system, the converters were chosen to be stacked rather than laid out. The previous output capacitors used were excessively large, protruding almost 2.5 inches above the surface of the board. The team

searched for more compact capacitors that still met the requirements for capacitance, voltage and current rating, and effective series resistance (ESR). Many capacitors were found that met most of these criteria, however, the EKZN101ELL121MK16S was selected. This capacitor has a similar equivalent ESR, similar voltage and current ratings, and is much smaller than the capacitors used previously. Another benefit of picking this particular capacitor is the price; the new capacitor is \$0.90 each. This price leads to a price difference of \$1.83 or 3% of the total board cost.

Due to the cost constraints of this design as well as the unavailability of our labs and test equipment due to COVID-19, we were unable to create a new output connector method compared to the previous design. As it stands currently, there are two holes in the PCB for banana connectors for both input and output of the board. To connect the outputs of multiple boards, banana cables must be used to connect each board. This should function correctly based on the test results from the previous design, but it does not achieve the idea of “small form factor” that this design should have.

PCB price was reduced as well from \$12.40 to \$0.40, as a different company would be used compared to the first iteration of the converter. The original PCB was manufactured by OSHPark, which is much more expensive compared to our chosen manufacturer. With the new manufacturer, JLCPCB, we saved \$12 from the original design at the cost of having a slightly lower quality PCB. We determined that this drop will hardly affect the efficiency of the circuit if at all and would be a fine adjustment given the \$12 savings. PCB layout design factors greatly into how compact we are able to make the MISO converter. The new design of the PCB will decrease the size from 3.5”x4” to 3”x3”.

Overall, with the savings introduced by the new components, the removal of other components such as Q1, and the switch from OSH Park to JLCPCB for circuit manufacturing, the



total cost comes out to \$41.78, which is below our goal of \$50. The total cost savings from the previous design is \$19.11.

**Table 4-2: Summary of Design Equations**

Component	Design Equation	Value
Maximum Duty Cycle ( $D_{Max}$ )	$1 - \frac{V_{in-minimum} * \eta}{V_o}$	0.61
Average Inductor Current ( $I_L$ )	$\frac{P_{in}}{V_{in}}$	7.35A
Inductor Current Ripple ( $\Delta i_L$ )	$\%ripple * I_L$	1.47A
Maximum Inductor Current ( $i_{Lmax}$ )	$i_{Lmax} = I_L + \frac{\Delta i_L}{2}$	8.09A
Critical Inductance ( $L_c$ )	$\frac{V_{in}D}{\Delta i_L f}$	3.11 $\mu$ F
Average Low-Side Switch Current ( $I_{LS-sw}$ )	$I_L * D$	4.48A
Average High-Side Switch Current ( $I_{HS-sw}$ )	$I_L * (1 - D)$	2.87A
Maximum High-Side Switch Voltage ( $V_{HS-sw}$ )	$\frac{V_o}{2} + \frac{\Delta V_o}{2}$	49.1V
Maximum Low-Side Switch Voltage ( $V_{LS-sw}$ )	$\frac{V_o}{2} + \frac{\Delta V_o}{2}$	49.1V

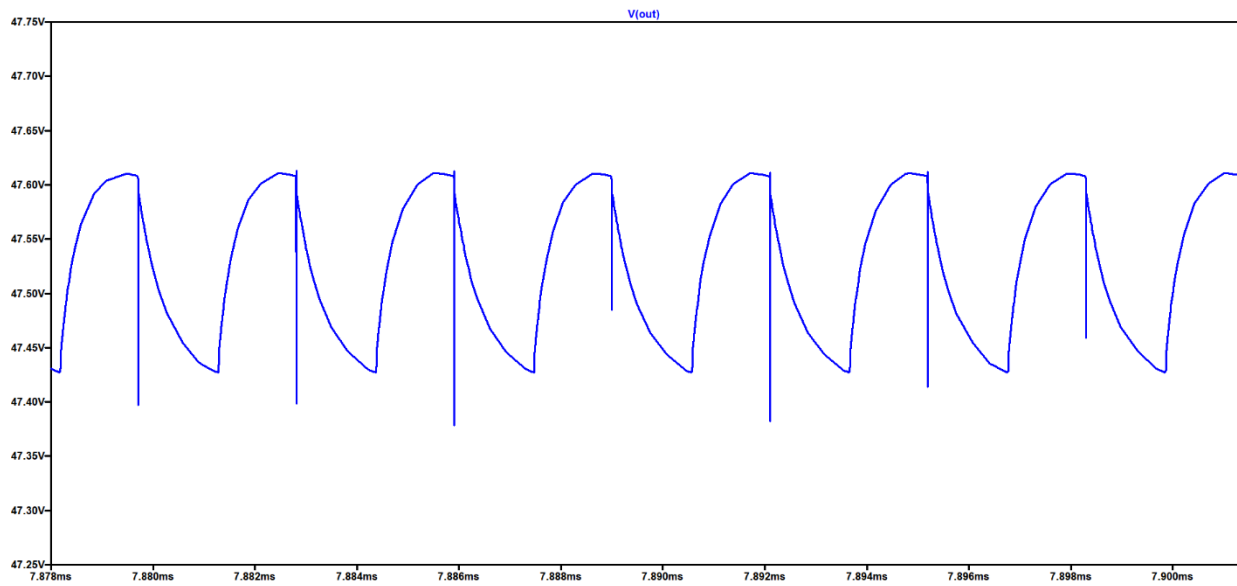
Critical Output Capacitance ( $C_o$ )	$\frac{I_{omax} * D}{\Delta V_o f}$	7.9 $\mu$ F
Maximum Output Capacitor Voltage ( $V_{output-capmax}$ )	$V_o + \frac{\Delta V_o}{2}$	49.1V
Output Capacitor RMS Current ( $i_{co-rms}$ )	$I_L \sqrt{[(1 - D) * (1 + \frac{1}{3} [\frac{\Delta i_L}{2I_L}]^2)] - [(1 - D)]^2}$	3.6A
Maximum Input Capacitor Voltage ( $V_{in-capmax}$ )	$V_{in} + \frac{\Delta V_{in}}{2}$	24.6V
Critical Input Capacitance ( $C_{in}$ )	$\frac{\Delta I_L}{8f \Delta V_{in}}$	957nF
Input Capacitor RMS Current ( $i_{cin-rms}$ )	$\frac{\Delta i_L}{2\sqrt{3}}$	0.43A

## Chapter 5: Simulation

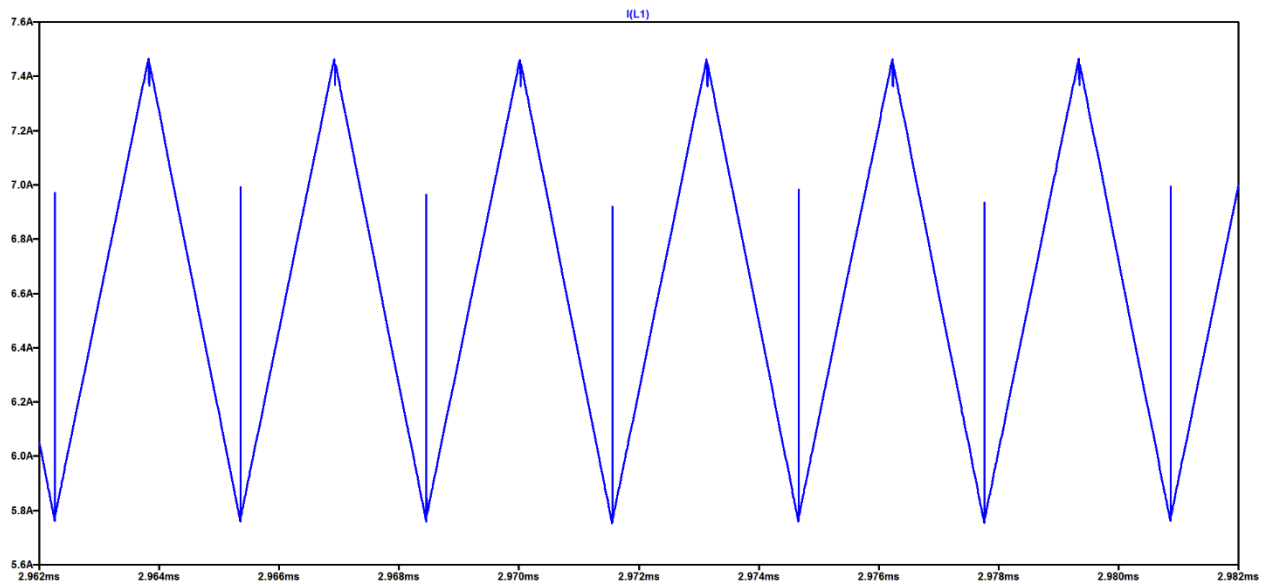
To ensure the proper operation of the updated design, the converter was simulated to verify the design. To perform these simulations, we used LTSpice® software, using the readily available model for the LTC3814-5 boost controller. Before beginning our simulations, we updated the schematic file for the MISO converter to match all component values that were changed. To save on cost, some of the new components that were chosen are more lossy than the components used in the previous design. With these higher losses, it is necessary to simulate to ensure that we will still meet design requirements such as efficiency, line regulation, and load regulation.

The transistors initially chosen for the synchronous boost converter, however, were not readily available in LTSpice®, so the Spice models for the transistors were downloaded and added to the library. When simulating the converter with the updated transistors, the results were not as expected. The output voltage was much higher than before, also being unstable and preventing the simulation from reaching steady state. The transistors were both replaced with two different transistors manufactured by Infineon and readily available in the Spice library; these changes are reflected in the Bill of Materials. With these new transistor models, the results were much better, all while maintaining a lower cost than the previous iteration of the converter.

First, a single converter stage was simulated to certify proper operation before connecting and testing multiple stages in parallel. The waveforms of inductor current and output voltage were observed at steady state to verify the peak-to-peak values of the two ripples. These waveforms can be seen in Figure 5-1 and Figure 5-2.



**Figure 5-1: Output Voltage Ripple of Single Converter (183.02mV)**



**Figure 5-2: Inductor Current Ripple (1.74A)**

The inductor current ripple shown in Figure 5-2, 1.74A, exceeded the calculated value of 1.47A. One possible reason for a larger ripple current than expected is due to the use of a small inductor. When determining the size of an inductor, the LTC3814-5 datasheet suggests a typical

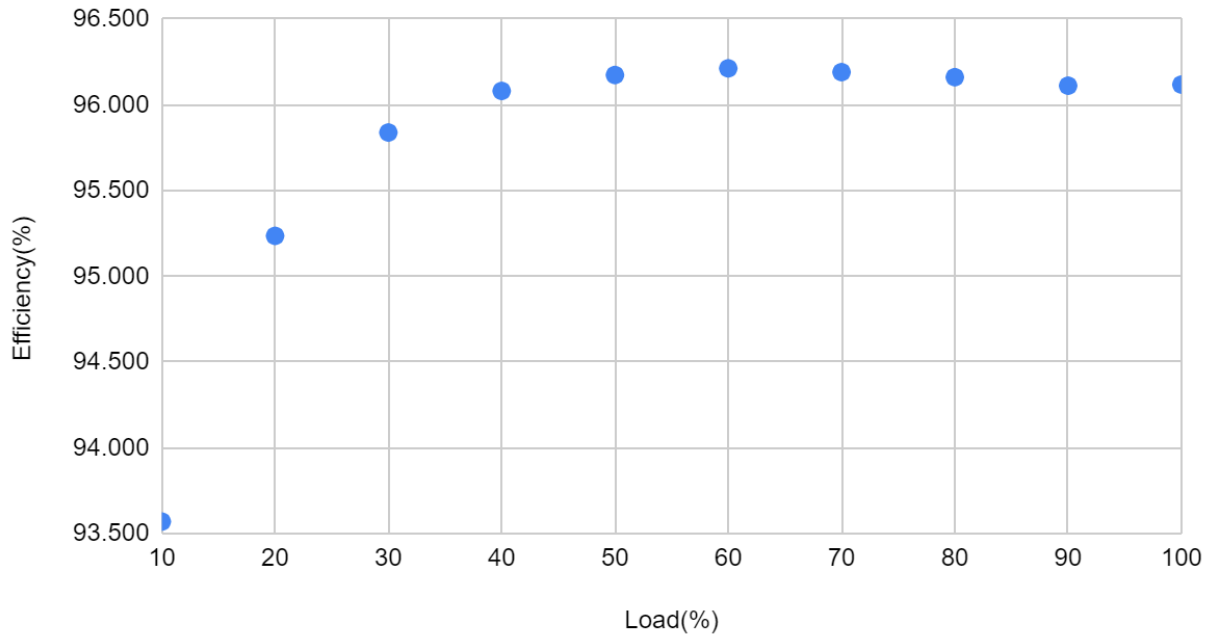
value of 30-40% for the inductor ripple, a sentiment expressed in Dr. Taufik's textbook on power electronics. However, the team chose a much smaller inductor ripple of 20%. This value is half as much as the higher spectrum of typical inductor values and could possibly have caused problems with meeting such a low ripple. When calculating the inductor current ripple with 30%, the current ripple is 2.21A of which the simulated inductor current ripple falls well below. Changing the inductor current ripple, however, changes other values as well. The critical inductance would change from  $3.11\mu\text{H}$  to  $15.6\mu\text{H}$ . The current inductor chosen does meet this specification, as the value was increased to meet the current rating.

The simulations were used to check that the efficiency, load regulation, and line regulation requirements were met. The load regulation is a measure of the converter's ability to keep a constant output voltage with variations in the input voltage. Load regulation is the converter's ability to maintain a constant output voltage with variations in the output load conditions. Both parameters can be expressed in percentages, and our converter must meet line and load regulation specifications of 5% for both parameters.

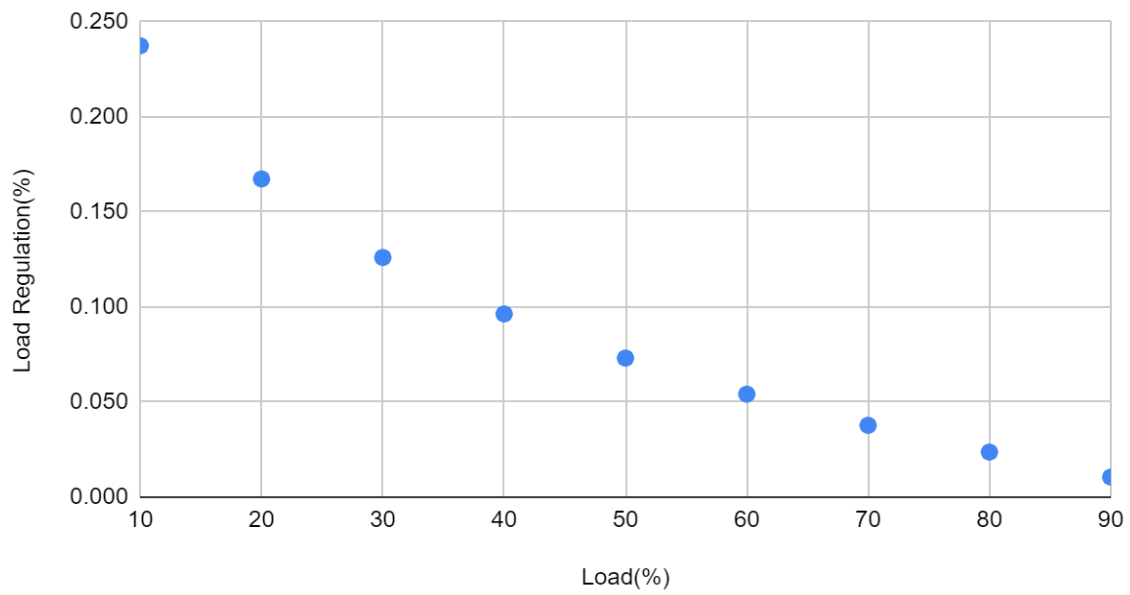
To verify the efficiency and load regulation, the converter was simulated with loads varying from 10-100% full load current in steps of 10% with nominal input voltage. For each of the loads, average input power, output power, and output voltage measurements were taken at steady state. The results of these measurements are summarized in Table 5-1. A plot of the efficiency as the load is increased is shown in Figure 5-3. As seen from the plot, the individual converter meets the efficiency parameter comfortably, with no values being close to the 85% efficiency specification. Figure 5-4 shows a plot of the load regulation across a variety of loads, with the load regulation meeting the specification of 5% for each condition.

**Table 5-1: Results of Single Converter Simulation with Varying Load**

Load (%)	Output Voltage (V)	Input Power (W)	Output Power (W)	Efficiency (%)	Load Regulation (%)
10	47.639	16.292	15.245	93.569	0.237
20	47.606	31.992	30.468	95.235	0.167
30	47.586	47.667	45.683	95.838	0.126
40	47.572	63.376	60.892	96.080	0.096
50	47.561	79.126	76.098	96.173	0.073
60	47.552	94.894	91.300	96.212	0.054
70	47.544	110.717	106.499	96.190	0.038
80	47.538	126.555	121.696	96.161	0.024
90	47.531	142.430	136.890	96.111	0.011
100	47.526	158.227	152.084	96.117	Nominal



**Figure 5-3: Single Converter Efficiency vs. Load %**



**Figure 5-4: Single Converter Load Regulation vs. Load %**

To calculate the line regulation of the converter, the converter was simulated with +/-2V of the nominal 24 input voltage at full load yielding output voltages of 47.556V and 47.527, respectively. Using these values along with the nominal values for the output and input voltages and Equation 5-1, the line regulation was found to be 1.5% and 0.05% for the maximum and minimum input voltage, respectively. These values are within the specified design requirement of less than 5%. The results of the line regulation can be found in Table 5-2

$$\text{Line regulation} = \frac{V_{Out\ nominal} - V_{Out}}{V_{In\ nominal} - V_{In}} \times 100$$

Eq. 5-1

**Table 5-2: Line Regulation of Single Converter**

$V_{in}$ (V)	$V_{out}$ (V)	Line Regulation (%)
24	47.526	Nominal
26	47.556	1.500
22	47.527	0.050

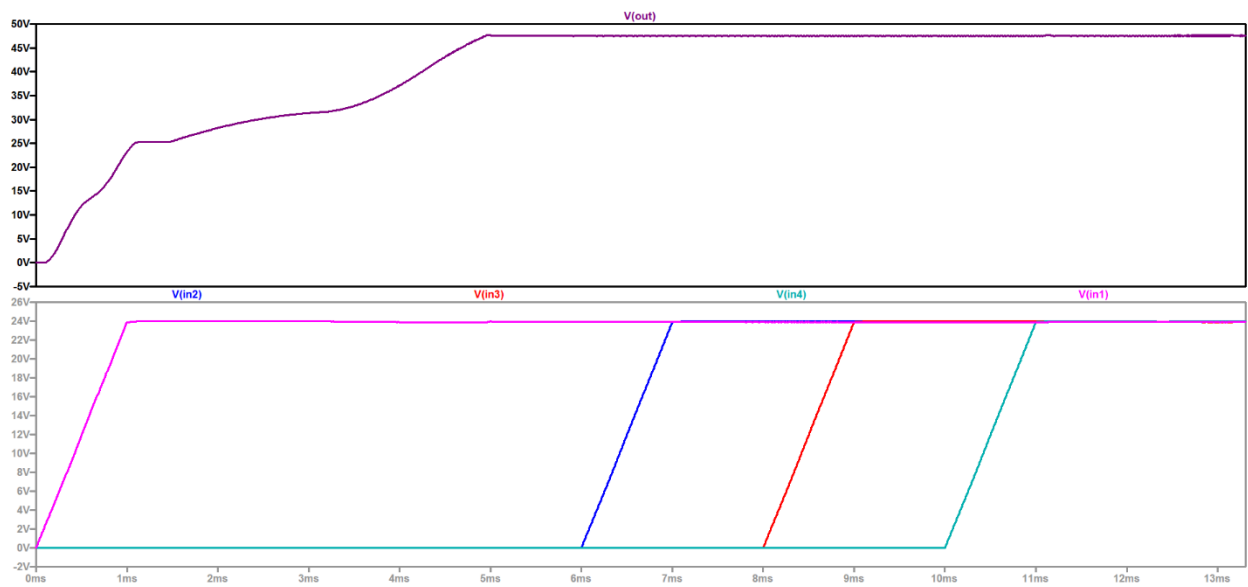
Once successful operation of a single boost converter was verified, the MISO converter system was then simulated with all four boost converters paralleled together.

The results of simulating the MISO converter at nominal input voltage and full load are shown in Figure 5-5. The converter was simulated with all four individual boost converters paralleled together on the output after the OR-ing diodes. The waveforms for the input voltages are included in the lower plot plane of the simulation. As seen from these waveforms, the inputs

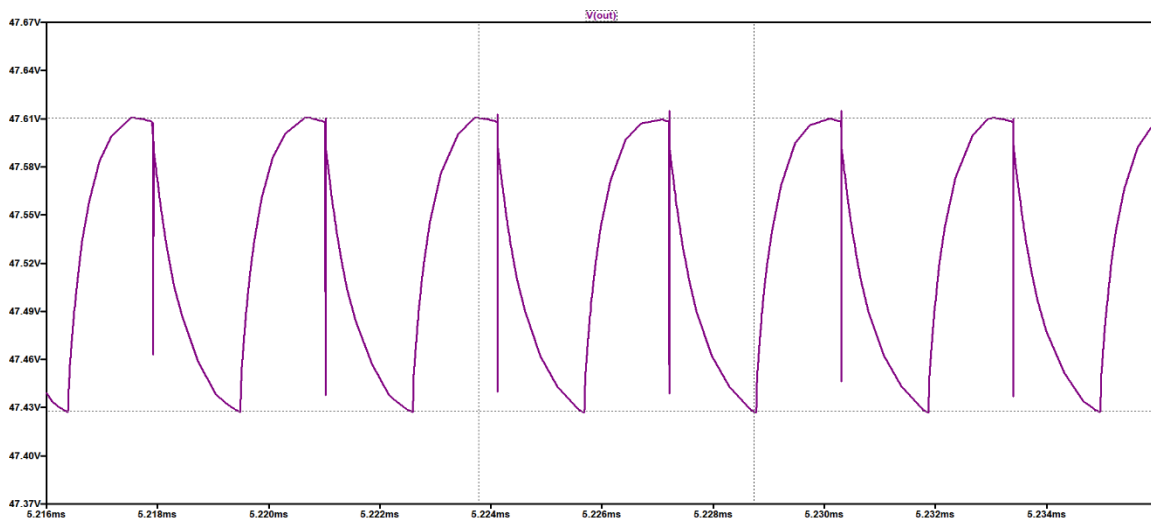


were turned on one at a time. This was done to verify that the converter would operate ideally while any number of the boards is supplying power.

Figure 5-6 is a close-up of the output voltage waveform at steady state, which details the output voltage ripple. The MISO converter was found to have an output voltage ripple of 182.97mV, or about 0.38% of the output voltage. This is well within the specified design requirement of less than 5%.

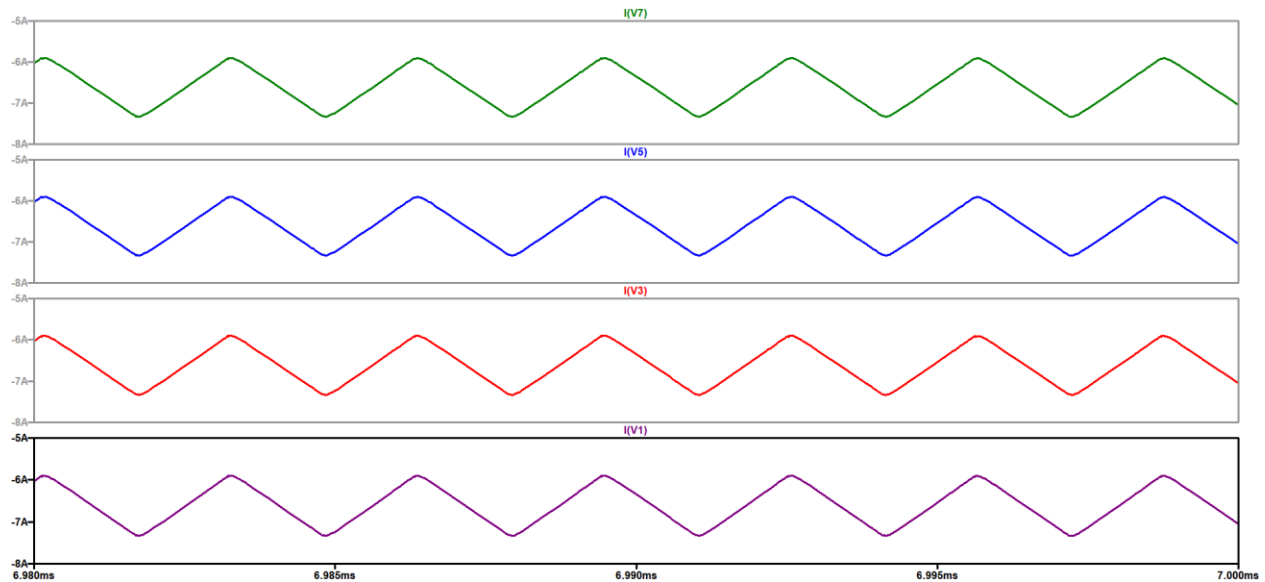


**Figure 5-5: Simulation of MISO converter**



**Figure 5-6: Output Voltage Ripple of MISO Converter (182.97mV)**

It is important that each converter in the MISO system share output current equally. This is to ensure that one board does not have to handle too much of the load at one time, which would stress that circuit more than the others. Figure 5-7 illustrates that each output current is identical to one another in simulation.



**Figure 5-7: Input Current Waveforms Showing Equal Current Sharing**

The converter was then simulated to determine the line regulation. The converter was first simulated with the minimum input voltage of 22V, yielding an output voltage of 47.527V. Next, the input voltage was changed to the maximum input voltage of 26V, yielding an output voltage of 47.556V. Using these values along with the nominal values for the output and input voltages and Equation 5-1, the line regulation was calculated for both cases. The data for the line regulation is shown in Table 5-3, which shows the line regulation requirement of 5% is met.

**Table 5-3: Line Regulation of Single Converter from LTSpice® Simulation**

$V_{in}$ (V)	$V_{out}$ (V)	Line Regulation (%)
24	47.526	Nominal
26	47.525	0.050
22	47.509	0.850

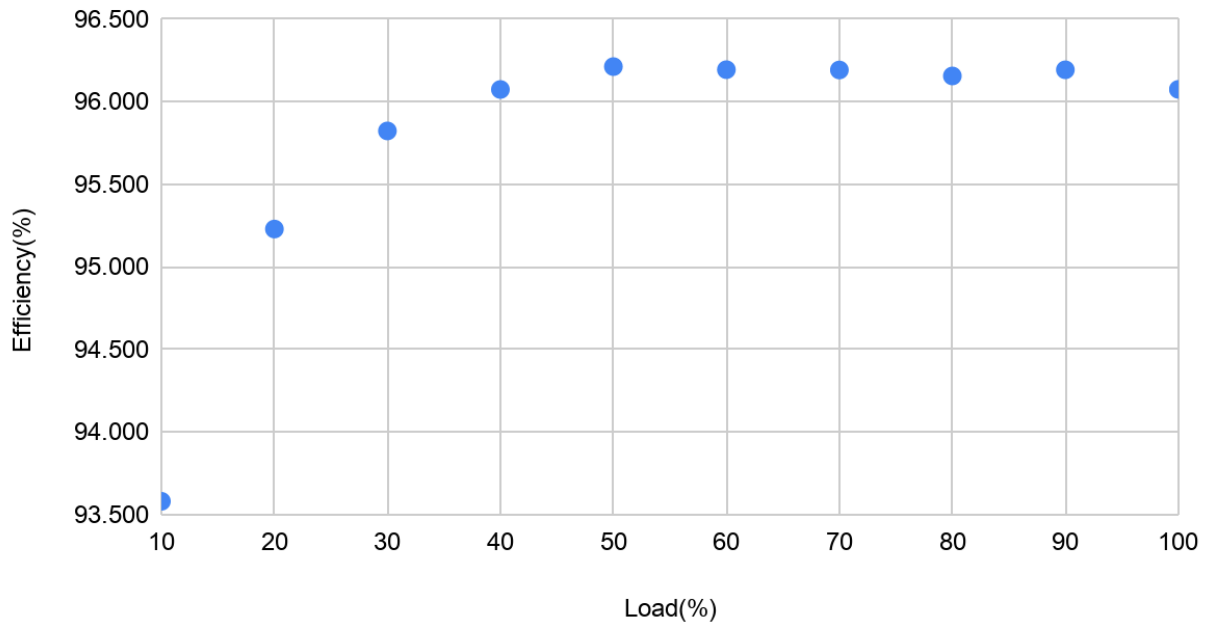
The converter was also simulated to verify the load regulation requirement using a no load set up. The steady state output voltage under no load condition and nominal input voltage was 48.03V. Using the steady state value of 47.526V at full load and nominal input voltage, the load regulation was found to be 1.05% using Equation 5-2. This value is well within the design requirement of less than 5% The data for the load regulation is shown in Table 5-4.

$$Load\ regulation = \frac{V_{Out\ No\ load} - V_{Out\ Full\ load}}{V_{Out\ Full\ load}} \times 100 \quad Eq. 5-2$$

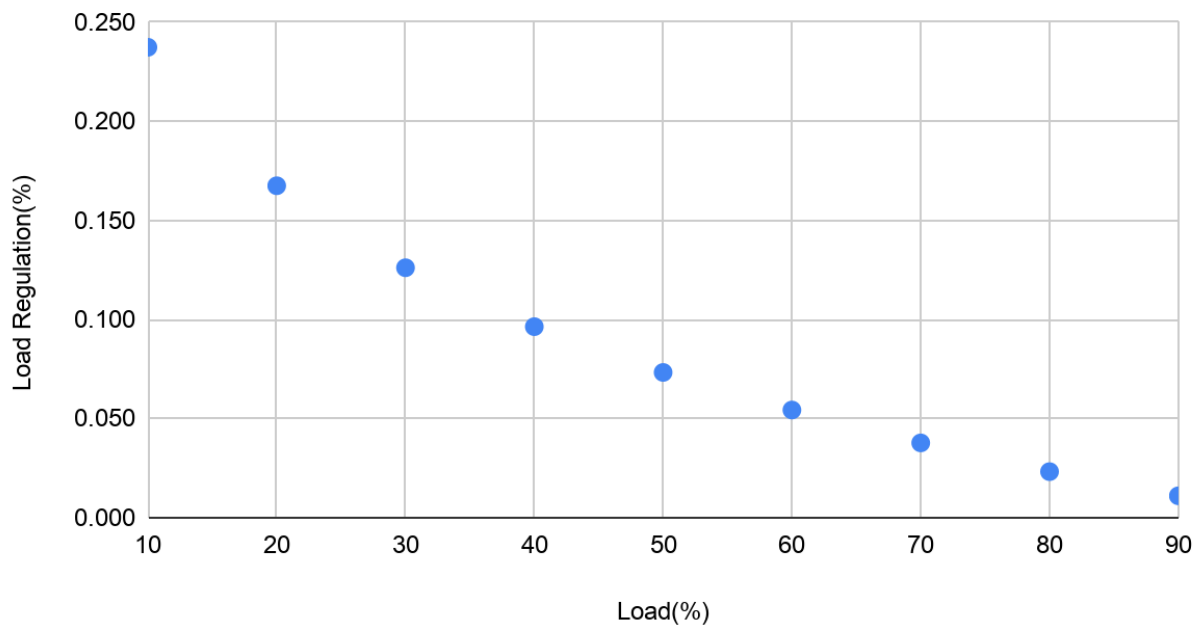
**Table 5-4: Results of MISO Converter Simulation with Varying Load**

Load (%)	Output Voltage (V)	Input Power (W)	Output Power (W)	Efficiency (%)	Load Regulation (%)
10	47.639	65.160	60.978	93.581	0.237
20	47.606	127.976	121.871	95.230	0.168
30	47.586	190.695	182.731	95.824	0.126
40	47.572	253.521	243.569	96.075	0.096
50	47.561	316.371	304.391	96.213	0.073
60	47.552	379.647	365.200	96.195	0.054
70	47.544	442.856	425.996	96.193	0.038
80	47.537	506.240	486.782	96.157	0.023
90	47.532	569.228	547.563	96.194	0.011
100	47.526	633.184	608.336	96.075	Nominal

The results from the previous tables for efficiency and load regulation for the MISO system can be seen in Figure 5-8 and 5-9. It is evident that the simulated efficiencies are around 95%, which is well above our goal of 85%.



**Figure 5-8: MISO Efficiency vs. Load %**



**Figure 5-9: MISO Load Regulation vs. Load %**

After verifying our design through simulation, we developed an improved board design utilizing our new components. We were able to save space by choosing some components with smaller footprints. However, a few other components in our iteration are larger than the ones that they replaced. Because of this, we had to compact the components on the board to make up for this size increase. Compacting the board proved worthwhile though, resulting in a board area of 2.99" x 2.99". Both sides of the board layout can be seen in Appendix C

Most of the underlying design principles from the first design remain in our layout. Many current paths on this board are simply planes, to account for large currents traveling through these paths. For paths that will have smaller currents running through them, small, 10-20 mil traces are used. Generally speaking, these small traces are used for signal paths, and the planes are used for power paths. For signal paths, 90-degree turns are eliminated in favor of two 45 degree turns. The purpose of this is to eliminate any possibility of high frequency effects on our switching signal. While the frequency at which our circuit switches is not in the GHz range, where EMI emissions are possible, it is still good practice to avoid any 90-degree trace turns.

This two-layer design has two distinct ground planes: one for the power path, and one for the signal path. This is to reduce the effects of the high frequency, high power switching signal along the power path against the signal path. Planes that are on opposite sides of the board are connected through various vias to ensure both ground planes still have the same voltage. The utilization of various vias to do this remained from the original design. A few components, including a small NMOS transistor named Q1 in the original design, were removed because they were not critical to the function of the circuit. Lastly, the standoff holes in the corners were changed from a perfect square orientation to having a single skewed corner. The purpose of this was to force each board's orientation to be the same when stacking multiple circuits.

## Chapter 6: Conclusion

With 13% of the world's inhabitants living without electricity, it is imperative to work towards minimizing this statistic to improve the quality of life for those who make up this demographic. One remedy for this issue is the Cal Poly DC House Project, which provides people with a DC power source for those who do not have access to AC power grids. The aim of the project was a low-cost MISO converter that could be used in conjunction with a DC House in remote areas of countries such as Indonesia, the Philippines, and others. This converter would make use of the abundant renewable energy sources such as hydroelectric, photovoltaic, and wind turbines to provide people without access to AC power grids a stable power source. The MISO functionality of our converter allows a single household to harvest power from multiple different energy sources to charge a single 48V battery. Effectively, this prevents a DC House from being limited by a single power generator.

The original goal of the project was to design and build a circuit board that could be hardware tested. Due to the effects of COVID-19 on accessibility of labs and equipment, the project was revised so that the only testing that could be done was through simulation using LTSpice® software. Although it was not possible for the board to be built and tested in hardware, an updated PCB design was developed that can be verified in hardware by future senior project groups. This further testing is necessary before the design can be confirmed to corroborate the results received from simulation. There are also some losses that cannot be accounted for in simulation, which will be seen in hardware testing. These losses could influence the efficiency and other characteristics of the converter. These features are requirements that must be met by the physical MISO converter once it is built.

Another important goal of the project was to develop a cheap, compact method for connecting the outputs of multiple converters. This would effectively create a multiple input, single output system to charge the single 48V battery in the DC House. The previous design of this converter connected the circuits via banana cables, which was intended to be eliminated. Due to the lack of readily available banana connectors that could interface the different boards, the high costs of a single banana connector, and the unavailability of testing equipment due to COVID-19, a solution could not be designed and tested. As a result, the method of output connectors remained unchanged. However, the placement of said connectors did change due to the board becoming more compact. Any designers for future iterations of this project would find it desirable to develop a new method for this function.

Another possible improvement for the future would be component selection. The component sizing revealed many of the components were oversized, the inductor for example. An inductor of a similar inductance was found for almost half the price, only lacking with a current rating slightly less than the maximum inductor current rating. The inductor also had a smaller footprint which would help reduce the size of the board. The reason for this oversight was in the filtering of components on the retail sites. Searching for a broader range of values relative to the calculated ratings and nominal value would increase the likelihood of finding cheap components with similar ratings.

Although assembling and testing the MISO converter was not possible due to factors outside of our control, the design is likely to work in practice. The single boost converter was simulated individually and met the design specifications outlined in Chapter 3. The MISO converter was also simulated, four converters being paralleled together at the output to verify the operation of multiple sources working together to provide power to the DC house. The MISO



converter is capable of powering the DC House while meeting the parameters of using four 24V nominal input sources with an efficiency greater than 85%, tight load regulation, minimal output voltage ripple and a combined output power of 600W all while maintaining a low cost. Compared to the previous design, the updated MISO converter uses readily available components rated with looser loss restrictions as before to provide a cheaper converter design.

The goal of the design for the converter regarding price was \$50 per board in this four board MISO converter. The cost of the previous iteration of the board was \$61.68, meaning the new price goal would have a savings of about 19%. With removing some components, switching PCB suppliers, and finding cheaper alternatives, the team was able to design a converter for the low-cost of \$41.78, a savings of 32% from the previous design. Not only was the design cheaper, but more compact as well. This compactness reduces space of the overall MISO system and makes it less intrusive for those who would have them in their homes.

The design of the converter was successful overall as we were able to reduce the cost by almost a third of the original price while not compromising quality of operation. The physical implementation and testing of the board would be the next step for future groups in order to verify the operation of the board for commercial use. As previously mentioned, a method for stacking the boards to create the MISO system would be another desirable step for future groups.

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## Appendices

### Appendix A – Bill of Materials

Part	Value	Mfg. Part#	Mfg.	Quantity Per Board	Unit Price	Price Per Board
STAND1, STAND2, STAND3, STAND4	Board Support Snap Fit	8842	Keystone	4	\$0.28	\$1.12
L1	22uH	74435582200	Würth Elektronik	1	\$6.89	\$6.89
C3, C9, C14	120uF	EKZN101ELL121MK16S	United Chemi-Con	3	\$0.90	\$2.70
V_IN	1.9V Red LED	150080SS75000	Würth Elektronik	1	\$0.18	\$0.18
IN_GOOD	1.9V Red LED	150080VS75000	Würth Elektronik	1	\$0.18	\$0.18
R23	1 MOhm	RC0805FR-071ML	Yageo	1	\$0.10	\$0.10
Q1	150V NMOSFET	IPD530N15N3GATMA1	Infineon	1	\$1.21	\$1.21
R2	30.9 kOhm	P20762CT-ND	Panasonic	1	\$0.36	\$0.36
PAD1, PAD2, PAD3, PAD4	Female Banana Jack	575-4	Keystone	4	\$0.84	\$3.36
D6, D7	100V Schottky Diode	BAT46ZFILM	STMicroelectronics	2	\$0.12	\$0.24
C4	5600pF	CC0402KRX7R7BB562	Yageo	1	\$0.01	\$0.01
C11	100uF	860010674014	Würth Elektronik	1	\$0.26	\$0.26
C1, C7, C36, C37	0.1uF	CL21B104KCFNNNE	Samsung	4	\$0.03	\$0.12
C8	100pF	GRM1885C1H101JA01D	Murata Electronics	1	\$0.04	\$0.04
C5	150pF	GRM1885C1H151JA01D	Murata Electronics	1	\$0.04	\$0.04

C6	330pF	GRM1885C1H331JA01D	Murata Electronics	1	\$0.04	\$0.04
C2, C19, C33	1uF	GMK212B7105KG-T	Taiyo Yuden	3	\$0.09	\$0.27
C15, C16, C17, C18, C20, C21, C34, C35	10000pF	C0805C103K1RAC7210	KEMET	8	\$0.03	\$0.24
C10, C12, C22, C23, C24, C29, C30	0.1uF	12101C104K4T2A	AVX Corporation	7	\$0.32	\$2.24
PAD5, PAD6, PAD7, PAD8	Terminal Turret	H9004-01	Harwin	4	\$0.39	\$1.56
Q2	120V NMOSFET	IPP114N12N3 G	Infineon	1	\$1.79	\$1.79
D9	Shunt Voltage Reference	LM4040CYM3-2.5-TR	Microchip Technology	1	\$0.32	\$0.32
U2, U4	Comparator	LT1716CS5#TRMPBF	Analog Devices	2	\$2.49	\$4.98
U1	Boost Controller	LTC3814IFE	Linear Technology	1	\$8.73	\$8.73
R7	300kOhms	RK73B1JTDD304J	KOA Speer	1	\$0.01	\$0.01
R16, R22	0Ohms	RC0603JR-070RL	Yageo	2	\$0.02	\$0.04
R15	1kOhms	RC0805JR-071KL	Yageo	1	\$0.02	\$0.02
R18, R21	10kOhms	RC0805FR-0710KL	Yageo	2	\$0.02	\$0.04
R8, R19	100kOhm	RC0805FR-07100KL	Yageo	2	\$0.02	\$0.04
R3	499Ohms	RC0805FR-07499RL	Yageo	1	\$0.02	\$0.02
R9, R14	4.99kOhms	RK73H2ATTD4991F	KOA Speer	2	\$0.02	\$0.04
R25	49.9Ohms	ERJ-6ENF49R9V	Panasonic	1	\$0.03	\$0.03
R5	6.49kOhms	ERJ-6ENF6491V	Panasonic	1	\$0.03	\$0.03
R4, R17, R20	78.7kOhms	RC0805FR-0778K7L	Yageo	3	\$0.02	\$0.06

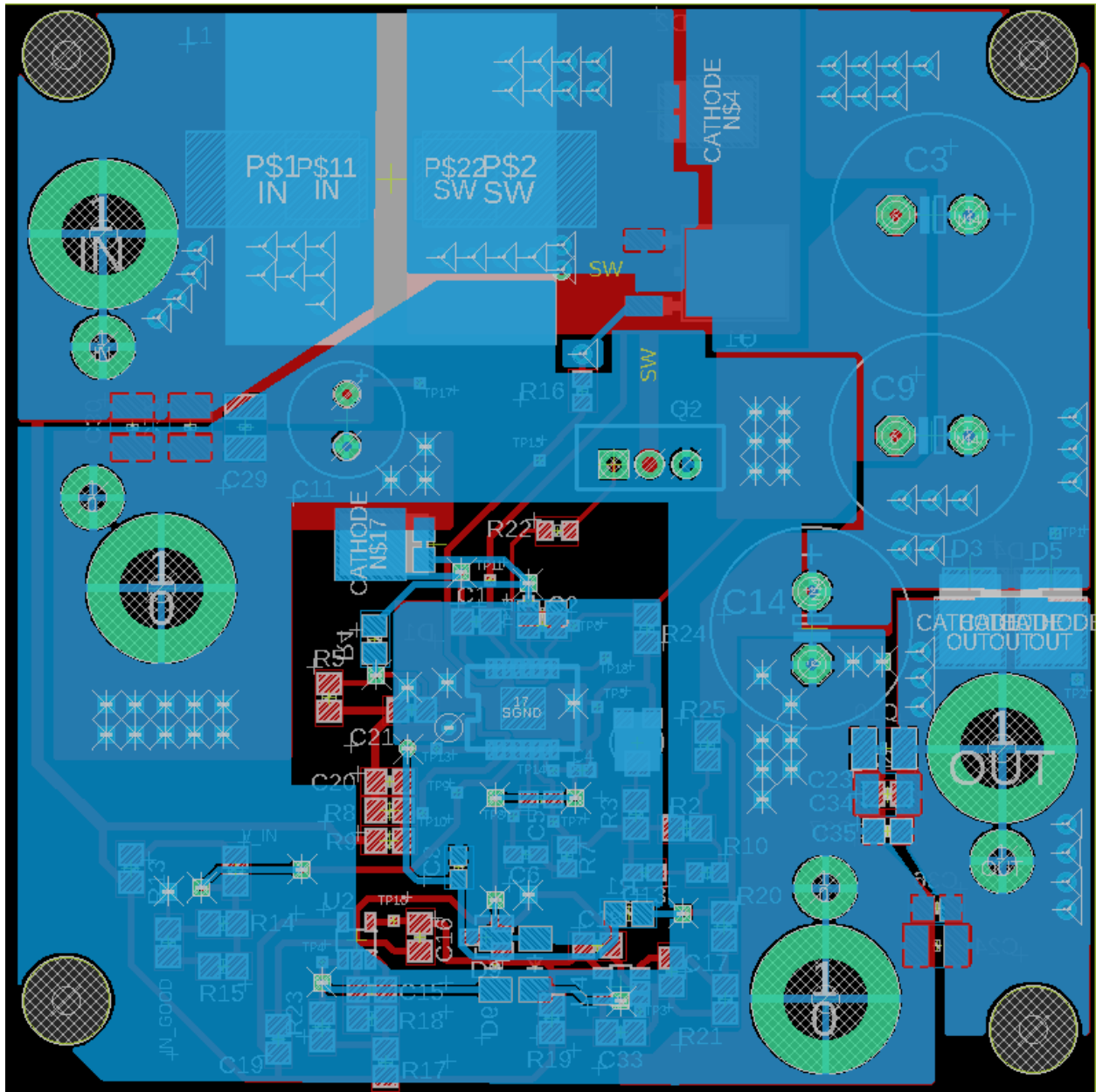
R1	806kOhms	RC0805FR-07806KL	Yageo	1	\$0.02	\$0.02
R24	0Ohms	RMCF0805ZT0R00	Stackpole	2	\$0.01	\$0.02
R6	100kOhms	RC1206FR-07100KL	Yageo	1	\$0.10	\$0.10
R13	4.99kOhms	RK73H2ATTD4991F	KOA Speer	1	\$0.10	\$0.10
RPOT	100Ohms	TC33X-2-101E	Bourns	1	\$0.28	\$0.28
D1, D2, D3, D4, D5	100V Schottky Diode	V10P10-M3/86A	Vishay	5	\$0.86	\$4.30
PCB			JLPCB	1	\$0.40	\$0.40

**Total: \$41.78**

**Cost Difference from Previous Design: -\$19.11**









## **Appendix D – Analysis of Senior Project Design**

### **1. Summary of Functional Requirements**

The work of this project details the redesign of a previously built DC-DC Boost Converter. This converter was designed with a MISO capability in mind. This was implemented by having the output be “parallelable.” This would allow multiple copies of the design output to a single battery, where each circuit handles a different power source. A single converter will convert 24 V to 48 V, DC. A key component of this new design is for it to be cheap. Specifically, the production cost must be below \$50 for a single unit. The converter must maintain a 48 VDC output over changes in input voltage and output load.

### **2. Primary Constraints**

The main limiting factors that we were challenged with were the cost and the output quality of the system. The materials cost of the original design was about \$64, and the main challenge was to reduce the cost while maintaining the quality of the output signal. To do so, Dr. Taufik allowed us to relax some of the constraints. The output voltage variation over input changes can be relaxed to 5% (as opposed to 3%) and the overall efficiency can be lower than 90%, but no lower than 85%.

### **3. Economic**

The primary purpose of this project is to provide a cheap means for converting power provided by sustainable energy generation solutions. The DC House Project at Cal Poly involves building an overall affordable, livable house for those in rural areas who do not have access to power from a grid. As such, the cost of our final design is something to be considered.

The time that each of us put into this project is the human capital invested into the project. Apart from that, there will most likely be some effort involved in setting our product up for home usage.

The materials used in our design are made from the Earth's natural resources. Copper and Gold for conductors, Silicon or possibly Gallium Arsenide for semiconductors, and polymers and glass for the fiberglass on our PCB. These resources are not scarce, but they are finite. As such, our design clearly contributes to the usage of these ever-dwindling resources.

#### **4. If manufactured on a commercial basis:**

There is no clear estimate for the number of devices per DC House. In mass production, each device might take between \$20 and \$35 to manufacture, depending on the price of some of the components in mass production. Since the efficiency of the device is lower than 100%, some power will be wasted. Since the user will not be paying for power (and will be generating the power themselves via solar panels), this does not necessarily equate to costing the user money.

#### **5. Environmental**

The power generation methods that will power the DC House are meant to be sustainable. Ideally, this would reduce the overall reliance of unsustainable energy generation methods. Therefore, the world will be using less of our finite resources while benefitting from the usage of electricity.

The environmental impacts of production are a different story. It is more than likely that the fabrication factories for circuits are run on a nonzero amount of nonrenewable energy. As such, the production of our design makes use of nonrenewable energy resources.

Some of the Earth's natural resources are used in this product. As mentioned earlier, this means that our design contributes to the usage of our ever-dwindling amount of precious metals and materials. These materials include copper, gallium arsenide, glass (sand), or various polymers.

As for other species, constructing the DC Houses in rural areas can always have a chance of disrupting ecosystems. If land needs to be cleared for the house to be built, then homes of animals could be possibly destroyed.

## **6. Manufacturability**

There should not be any issues with manufacturing this product. Since the design that we are improving on has already been built previously, the design is at the very least, functional. As of this project's completion, there are no custom parts in the design. As such, manufacturing should not be very difficult.

## **7. Sustainability**

As the components of our device are meant to be cheap, they most likely will not be very robust. As a result, the longevity of our device may not be very long. It is difficult to estimate how long our device can last, but one could hypothesize that if it only lasts 10 years, then the user would have to purchase a new device for every power generator they own. This could prove costly not only to the user, but to the environment, as more materials would need to be used to build more of our products.

This project could make use of any upgrades. Many changes could be made to improve efficiency, as the final design could have an efficiency as low as 80%. However, improving the efficiency of this design would most likely involve increasing the price of our product, the

opposite of our goal. In the same vein (but in the other direction), the device could be made cheaper if we sacrifice the overall performance of the product.

## **8. Ethical**

As previously mentioned, this project contributes to the Cal Poly DC House Project. This project is designed to provide electrically powered houses to areas of developing countries that do not already have access to such commodities. This goal would seem ethically and morally “correct.” However, many ethical issues exist that one may not initially realize.

Externalities are always associated with the design and production of a product intended to be distributed to others. Some are direct while others are indirect. In our project, one may not initially consider the downsides to providing these developing areas with cheap electrical housing. By providing an area with houses that can sustain themselves electrically, they do not depend on any outside power distribution system. If this area’s government had a plan to implement a power grid in the future, such plans would be dashed. While one could argue that this would end up saving this government’s money, another could argue that the lack of infrastructure on the government’s part contributes to its potential weakness, therefore reducing the country’s means of having a stable, centralized power to strengthen the country’s economy and wellbeing.

The immediate benefit of implementing the DC House is that those without power, get power. Electricity, while not a recent discovery, is unfortunately not a basic commodity for everyone around the world. Electricity brings many conveniences and necessities to any human. Namely, electric light, electric heating (and cooling), and electric appliances are all examples of the benefits of electricity. Without these things, much less room for societal and

political development exists, as the humans in these areas do not have access to the technology that others do. The lack of electricity holds these groups back from progressing as societies.

By adopting the Utilitarian framework of approaching ethics, one would try to consider both the costs and benefits of their actions. The cost of implementing these off-grid electrically powered houses would be a potential weakening of the overall economy of a developing country, due to missing the opportunity to implement infrastructure as a centralized power grid. The benefits of the off-grid houses are that everyone gets electricity, immediately. The latter of these two is the stronger one.

As previously mentioned, getting everyone access to electricity will open opportunities for them to progress their neighborhoods/villages/towns with their newfound use of electricity. As such, these societies can form small governments of their own, or strengthen their own centralized governments, or otherwise just improve the general quality of life in their areas. When the general quality of life increases in multiple areas of a country, that country has a better overall wellbeing. Regardless of the specific outcome, increasing the welfare of the people is the intended goal of the DC House Project. Furthermore, the Utilitarian goal of “greatest good for the greatest number” is satisfied, therefore justifying this project as ethically correct.

## **9. Health and Safety**

Electrical devices pose a risk of getting shocked. While the input voltage might not be sufficient to kill, the resistance of the body always varies. The output of our circuit has a potential difference of 48 V. If the user happens to be wet and bridges the two leads on the end of the circuit, they could hypothetically feel about 10 - 40 mA of current. Again, while not

sufficient to kill, this could hypothetically damage any critical biomedical devices, such as a pacemaker.

Apart from the electrical standpoint, the materials used in production of our device are inedible, and most likely toxic. If a small child were to break off a piece of our design and ingest it, negative health effects may occur.

For the manufacturing process, one could hypothesize that the emissions generated by the fabrication factories producing our product produce negative health effects on the Earth's ecosystem. Apart from this, our design has no immediate negative effects on health.

## **10. Social and Political**

Our design contributes to the DC House Project. Ideally, the DC House will provide a means for people in developing countries and/or rural areas to have an affordable house that makes use of electricity. The results and effects of this will be discussed below.

Firstly, the ones who benefit the most from this project are those that would be given access to these DC Houses. Hypothetically, if a philanthropic company were to supply rural areas in developing countries with these houses, free of monetary cost to the residents of said places, then the residents would essentially get free use of electricity in their own homes. One could also hypothesize that those who profit off the use of nonrenewable energy sources and/or use of power grids would be against the implementation of off-grid, self-sustainable housing solutions.

However, this is only the hypothetical result of the entire DC House. Our project only contributes to this. In more direct terms, the existence of a single DC-DC power converter makes a small difference in the sociopolitical climate of developing countries, much less so in rural areas of more wealthy countries such as the U.S.

It is also worth mentioning that the use of these products requires some knowledge of electricity, and a functional understanding of why a house could need multiple supply voltages. As such, those without education could struggle with the use of our product and could create some inequities between those who do have a functional understanding of our product, and those who do not.

## **11. Development**

The process of creating the PCB layout of our design entailed the usage of PCB layout software, namely EAGLE. Also, the actual design process of a boost converter was something that we had to familiarize ourselves with. We had to learn the nuances of boost converter design such as separating the ground planes for the signal and power paths.

## Appendix E – Schedule

### Winter 2020

	Week 1		Week 2		Week 3		Week 4		Week 5		Week 6		Week 7		Week 8		Week 9		Week 10		Finals																													
	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F
	8		15		22		29		5		12		19		26		5		12		19																													
<b>Review &amp; Literature Survey</b>																																																		
Research Any Previous Work																																																		
List References																																																		
Finalize Design Goals																																																		
<b>Design</b>																																																		
Level 0, 1, 2, Block Diagrams																																																		
Design, Calculations, Component Selections																																																		
Schematics and Simulation (if applicable)																																																		
<b>Component Selections and Purchase</b>																																																		
Search for Components																																																		
Bill of Materials and Board Layout (if applicable)																																																		
Order and Acquire Components																																																		
<b>Report Writeup</b>																																																		
Chapter 1																																																		
Chapter 2																																																		
Chapter 3																																																		

▲ Assignment Due      🗓️ Advisor Feedback

Continue to Spring

Spring 2020	APRIL										MAY										JUNE																							
	Week 1		Week 2		Week 3		Week 4		Week 5		Week 6		Week 7		Week 8		Week 9		Week 10																									
	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R	F	M	T	W	R
<b>Design (For Chapter 4)</b>																																												
Design Equations																																												
Component Selections																																												
Circuit or System Design																																												
<b>Computer Simulation (For Chapter 5)</b>																																												
Simulation Setup																																												
Simulation Results																																												
Data Results Analysis																																												
PCB Layout (if applicable)																																												
<b>Report Writeup</b>																																												
Chapter 4																																												
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Chapter 6																																												
Final Report Submission																																												

▲ Assignment Due

FINALS WEEK