Characterisation of the cascode gate drive of power MOSFETs in clamped inductive switching applications

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Statement of Original Authorship

The work contained in this thesis has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the thesis contains no material previously published or written by another person except where due reference is made.

QUT Verified Signature

Mark Broadmeadow

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Abstract

Power MOSFETs in switching applications are conventionally driven through an external gate resistance. The gate resistance is adjusted to provide controlled rate of change of load current and voltage. This method of drive introduces long switching delays, due to the time required to charge the gate-source capacitance of the power MOSFET, described by the RC time constant of the gate resistor and gate-source capacitance. The delays in charging the gate of the power MOSFET result in increased switching losses and conduction losses. The high driving impedance also makes the MOSFET susceptible to failure modes invoked by the MOSFET parasitic capacitance during switching transitions.

To overcome the limitations of existing gate drive topologies, a novel gate drive concept is proposed to provide fast, controlled switching of power MOSFETs. The proposed topology exploits the cascode configuration with the inclusion of an active gate clamp to ensure that the driven MOSFET may be driven and held off under all load conditions. The circuit is composed of two low-voltage, n-channel power MOSFETs which drive the source of a high-voltage power MOSFET. In contrast to a conventional gate drive, gate current is not sourced through a resistor, allowing high peak currents to be delivered to the gate during turn-on; long charging delays and the Miller plateau are eliminated. Alternative implementations are also proposed, including substitution of a p-channel device for the clamp MOSFET to simplify implementation.

This work explores the operation of the proposed cascode gate drive topology in the context of clamped inductive switching applications. Mechanisms to enable control of the switching process via cascode gate drive are elucidated via simulation and validated experimentally. Unique analysis tools and techniques are developed and employed to demonstrate the application of cascode gate drive for switching performance optimisation.

The simplified turn-on waveforms for cascode gate drive of power MOSFETs are derived. Mechanisms that control the switching process are identified and discussed. Additionally, the action of the clamp MOSFET in the switching process is described, with the natural and forced turn-off mechanisms identified. Advantages and limitations of the proposed cascode gate drive topology are discussed.

The switching performance characteristic of MOSFETs under cascode gate drive are explored via simulation. Typical switching waveforms for the proposed cascode gate drive are presented and compared with the characteristic waveforms for a conventional gate drive. An exploration of the parameter space for the proposed cascode gate drive topology is conducted. The parameter space composed of the cascode MOSFET gate resistance (R_{gle}) and high-voltage MOSFET gate-source capacitance (C_{gshe}) is identified as a candidate for further investigation.

A detailed investigation of switching performance over the (R_{gle}, C_{gshe}) parameter space is conducted via simulation, including load current sensitivity. In general, increasing C_{gshe} is shown to reduce turn-on switching losses for a given value of R_{gle}, while the maximum $\mathrm{d}v/\mathrm{dt}$ during the switching transient is decreased and the maximum $\mathrm{d}i/\mathrm{dt}$ during the transition remains relatively constant. Switching optimisation is performed via application of a novel analysis technique featuring overlaid contour plots of multiple switching performance metric surfaces. Practical examples demonstrating switching loss optimisation in the presence of slew-rate constraints using cascode gate drive are formulated and presented.

An experimental prototype of the proposed cascode gate drive topology is developed. Operation of the prototype is successfully demonstrated in a clamped inductive switching application at 400 V and 10 A. The observed experimental gate-source voltage waveforms are distinctly different from that of a conventional gate drive, with RC charging delays and the Miller plateau eliminated. Switching performance of the prototype is characterised experimentally at 350 discrete operating points over the (R_{gle}, C_{gshe}) parameter space for load currents ranging from 1 A to 10 A. At the highest demonstrated switching speed, a turn-on switching loss of 74 µJ is achieved for a maximum $\mathrm{d}v/\mathrm{dt}$ of 59 V/ns and maximum $\mathrm{d}i/\mathrm{dt}$ of 560 A/µs.

The switching behaviour observed in simulation is validated experimentally: independent control of $\mathrm{d}i/\mathrm{dt}$ and $\mathrm{d}v/\mathrm{dt}$ switching metrics is demonstrated, enabling optimisation of switching performance unachievable via conventional gate drive. Mechanisms that control the switching process are identified and mapped to the observed gate-source voltage waveforms.

Finally, recommendations are made for future research pathways arising from this work. Application of the cascode gate drive topology to silicon carbide (SiC) MOSFETs is proposed, along with a number of modifications to the cascode gate drive topology, including use of highly integrated MOSFET-driver ICs and the inclusion of low-voltage series diodes for body-diode reverse recovery elimination. Investigation of the combined use of cascode and high-voltage MOSFET gate resistances for switching performance optimisation is also proposed.

Original contributions

1. **Cascode gate drive of power MOSFETs**

   A novel cascode gate drive configuration for power MOSFETs in switching applications is developed. The circuit is composed of two low-voltage n-channel power MOSFETs which drive the source of a high-voltage power MOSFET. In contrast to conventional gate drive, gate current is not sourced through a resistor, allowing high peak currents to be delivered to the gate during turn-on: long charging delays and the Miller plateau are eliminated.

   The second low-voltage MOSFET acts as an active gate clamp to ensure the high-voltage MOSFET may be driven off under all load conditions, and holds the MOSFET off with a low-impedance clamp. Alternative implementations are also proposed.

2. **Analysis of the switching process for cascode drive of power MOSFETs**

   The simplified turn-on waveforms are derived for the cascode gate drive of power MOSFETs . Mechanisms that control the switching process are identified and discussed, along with the advantages and limitations of the proposed cascode gate drive topology.

3. **Exploration of the $(\boldsymbol{R_{gle}, C_{gshe}})$ parameter space for switching performance optimisation**

   The cascode MOSFET gate-resistance (R_{gle}) and high-voltage MOSFET gate-source capacitance (C_{gshe}) are identified as the key parameters for controlling the switching behaviour of the driven high-voltage MOSFET. Switching behaviour across the (R_{gle}, C_{gshe}) parameter space is elucidated via simulation and validated experimentally over 350 operating points. Independent control of $\mathrm{d}i/\mathrm{dt}$ and $\mathrm{d}v/\mathrm{dt}$ switching metrics is demonstrated, enabling optimisation of switching performance unachievable via conventional gate drive.

   Switching optimisation is performed via application of a novel analysis technique featuring overlaid contour plots of multiple switching performance metric surfaces. Practical examples demonstrating switching loss optimi-

sation in the presence of slew-rate constraints using cascode gate drive are formulated and presented.

4. **Development of practical simulation and experimental analysis tools for switching performance characterisation**

   New analysis tools for the characterisation of the switching performance of power semiconductors are developed.

   In the simulation domain, practical methods and processes for extracting SPICE model parameters from power MOSFET and Schottky diode datasheets are developed. Simulation test circuits for the evaluation of extracted models, and comparison to documented device performance, are demonstrated.

   In the experimental domain, a post-processing technique for reconstruction of true current from $\mathrm{d}i/\mathrm{dt}$ polluted resistive current shunt measurements is developed. Reconstruction of switching current transients in a non-optimal layout using low-cost, surface-mount current sense resistors is demonstrated. A practical method for tuning the reconstruction filter using experimental data is also derived.

   Finally, a system for automated switching performance feature extraction from double-pulse waveform data is developed and implemented.

Publications

Resulting directly from this work

M. A. H. Broadmeadow, G. F. Ledwich, and G. R. Walker, "An improved gate driver for power MOSFETs using a cascode configuration," in *Proc. 7th IET Int. Conf. Power Electronics, Machines and Drives (PEMD 2014)*, Manchester, UK, 2014, pp. 1–6.

M. A. H. Broadmeadow, G. R. Walker, and G. F. Ledwich, "Comparison of the gate drive parameter space for driving power MOSFETs using conventional and cascode configurations," in *Proc. 2014 IEEE Energy Conversion Congr. and Expo. (ECCE'14)*, Pittsgurgh, PA, 2014, pp. 1–8, (in press).

M. A. H. Broadmeadow, G. F. Ledwich, and G. R. Walker, "Automated power semiconductor switching performance feature extraction from experimental double-pulse waveform data," in *Proc. 2014 Australasian Universities Power Engineering Conf. (AUPEC 2014)*, Perth, Australia, 2014, pp. 1–6, (in press).

Other related publications

G. R. Walker, M. A. H. Broadmeadow, and G. F. Ledwich, "A high frequency, low voltage stackable full bridge module for modular multilevel cascade converter (MMCC) research," in *Proc. 7th IET Int. Conf. Power Electronics, Machines and Drives (PEMD 2014)*, Manchester, UK, 2014, pp. 1–6.

G. R. Walker, N. Ghasemi, M. A. H. Broadmeadow, and G. F. Ledwich, "A high cell count cascade full bridge converter for wide bandwidth ultrasonic transducer excitation," in *Proc. 2014 IEEE Energy Conversion Congr. and Expo. (ECCE'14)*, Pittsgurgh, PA, 2014, pp. 1–7, (in press).

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Nomenclature

HV MOSFET	The high-voltage MOSFET being driven in cascode configuration; Q3 in Figure 2.1.
Cascode MOSFET	The low-voltage MOSFET placed in the source path of the high-voltage MOSFET being driven in cascode configuration; Q2 in Figure 2.1. Controls the turn-on process.
Clamp MOSFET	The low-voltage MOSFET placed across the gate-source of the high-voltage MOSFET in cascode configuration; Q1 in Figure 2.1.

Abbreviations

2D	Two-dimensional
3D	Three-dimensional
BJT	Bipolar junction transistor
CAD	Computer-aided design
DUT	Device under test
EMI	Electromagnetic interference
FEA	Finite element analysis
FET	Field effect transistor
IC	Integrated circuit
JFET	Junction field effect transistor
MOSFET	Metal-oxide semiconductor field effect transistor
PC	Personal computer
PCB	Printed circuit board
PDF	Portable document format
PFC	Power factor correction
PWM	Pulse width modulation
RC	Resistor-capacitor
SiC	Silicon carbide
SPICE	Simulation Program with Integrated Circuit Emphasis
TVS	Transient voltage suppressor
VDMOS	Vertical double diffused power MOSFET

Symbols

a		Non-linear gate-drain capacitance parameter.
$\mathbf{A}$	[Wb/m]	Vector magnetic potential.
c		Intercept of straight line.
C_{ds}	[F]	Drain-source capacitance.
C_{dshe}	[F]	Drain-source capacitance added externally to driven HV MOSFET in cascode configuration.
C_{dsle}	[F]	Drain-source capacitance added externally to cascode MOSFET in cascode configuration.
C_{gd}	[F]	Gate-drain capacitance.
$C_{gd,max}$	[F]	Maximum non-linear gate-drain capacitance.
$C_{gd,min}$	[F]	Minimum non-linear gate-drain capacitance.
C_{gd0}	[F]	Zero-bias gate-drain capacitance.
C_{gdhe}	[F]	Gate-drain capacitance added externally to driven HV MOSFET in cascode configuration.
C_{gdle}	[F]	Gate-drain capacitance added externally to cascode MOSFET in cascode configuration.
C_{gs}	[F]	Gate-source capacitance.
C_{gshe}	[F]	Gate-source capacitance added externally to driven HV MOSFET in cascode configuration.
C_{gsle}	[F]	Gate-source capacitance added externally to cascode MOSFET in cascode configuration.
C_{iss}	[F]	Input capacitance.
C_j	[F]	Junction capacitance.
C_{j0}	[F]	Zero-bias junction capacitance.
C_{oss}	[F]	Output capacitance.
C_p	[F]	Parasitic parallel capacitance.
C_{rss}	[F]	Reverse transfer capacitance.
$\mathrm{d}i/\mathrm{dt}$	[A/s]	Time rate of change of current, typically refers to drain current i_d.
$\mathrm{d}v/\mathrm{dt}$	[V/s]	Time rate of change of voltage, typically refers to drain-source voltage v_{ds}.
η_0	[F/m]	Permittivity of free space.
η_r		Relative permittivity.
E_{cond}	[J]	Conduction energy loss.
E_{off}	[J]	Turn-off switching energy loss.
E_{on}	[J]	Turn-on switching energy loss.
E_{rr}	[J]	Reverse recovery energy loss.

E_{tot}	[J]	Total energy loss.
f_{sw}	[Hz]	Switching frequency.
$GMIN$	[S]	Shunt conductance.
i_0	[A]	Current at time zero.
i_d	[A]	Drain current.
i_D	[A]	Diode forward current.
$i_{d,HV}$	[A]	Drain current of the HV MOSFET.
i_g	[A]	Gate current.
I_L	[A]	Inductor (load) current in a clamped inductive switching configuration (see Figure 1.4).
IS	[A]	Saturation current.
$\mathbf{J}$	[A/m^2]	Current density.
KP	[A/V^2]	Transconductance parameter.
λ	[1/V]	Channel-length modulation.
L		Channel length scaling.
L_f	[H]	Reconstruction filter inductance parameter.
L_{loop}	[H]	Loop inductance.
L_s	[H]	Parasitic series inductance.
μ_0	[H/m]	Permeability of free space.
m		Gradient of straight line.
M		Junction grading coefficient.
$mtriode$		Conductance multiplier in triode region.
N		Emission coefficient.
p_{loss}	[W]	Instantaneous power dissipation within a switching device.
R_d	[Ω]	Drain resistance.
$R_{ds,on}$	[Ω]	Resistance of the MOSFET channel when driven into the ohmic region.
R_g	[Ω]	Gate resistance.
R_{ghe}	[Ω]	Gate resistance added externally through which HV MOSFET is driven.
R_{gle}	[Ω]	Gate resistance added externally through which cascode MOSFET is driven.
R_s	[Ω]	Source resistance.
$subthres$	[A/V]	Sub-threshold conduction parameter.
t	[s]	Time.
t_f	[s]	Fall time.
t_{off}	[s]	Turn-off time.
t_{on}	[s]	Turn-on time.

t_r	[s]	Rise time.
t_{rr}	[s]	Reverse recovery time.
TT	[s]	Transit time.
V_{bus}	[V]	DC bus voltage applied across a half-bridge circuit.
v_D	[V]	Diode forward voltage.
V_{drh}	[V]	Drive voltage for the HV MOSFET used in LTspice simulations.
$V_{drive,HV}$	[V]	Drive voltage for the HV MOSFET.
$V_{drive,LV}$	[V]	Drive voltage for the cascode and clamp MOSFETs.
V_{drl}	[V]	Drive voltage for the cascode MOSFET used in LTspice simulations.
v_{ds}	[V]	Drain-source voltage.
$v_{ds,HV}$	[V]	Drain-source voltage of the HV MOSFET.
v_{gd}	[V]	Gate-drain voltage.
v_{gs}	[V]	Gate-source voltage.
$v_{gs,ca}$	[V]	Gate-source voltage of the cascode MOSFET.
$v_{gs,HV}$	[V]	Gate-source voltage of the HV MOSFET.
v'_{gs}	[V]	MOSFET gate-source terminal voltage.
$V_{gs(IL),ca}$	[V]	Gate-source voltage required for the cascode MOSFET to conduct the load current, I_L, in the active region.
$V_{gs(IL),HV}$	[V]	Gate-source voltage required for the HV MOSFET to conduct the load current, I_L, in the active region.
$V_{gs(th),ca}$	[V]	Threshold voltage of the cascode MOSFET.
$V_{gs(th),HV}$	[V]	Threshold voltage of the HV MOSFET.
V_j	[V]	Junction potential.
V_t	[V]	Thermal voltage.
V_{th}	[V]	Threshold voltage.
V_{trig}	[V]	Trigger voltage.
W		Channel width scaling.

Chapter 1

Introduction

Power MOSFETs in switching applications are conventionally driven through an external gate resistance [1]. The gate resistance is adjusted to provide controlled rate of change of load current and voltage. This method of drive introduces long switching delays due to the time required to charge the gate-source capacitance of the power MOSFET, described by the RC time constant of the gate resistor and gate-source capacitance. The high driving impedance also makes the MOSFET susceptible to failure modes invoked by the MOSFET parasitic capacitance during switching transitions. Alternatively, low gate resistances can be used in conventional gate drive to achieve very fast switching speeds [2], at the expense of high peak drive currents.

Current sourced [3, 4] and resonant [5, 6] gate drivers have also been developed, which utilise an inductive magnetic element to charge the gate of a power MOSFET. These drivers provide some advantages over voltage driven gate drive, such as recovery of gate drive energy and reduced turn on times, but exhibit limitations in performance (minimum duty cycle and circulating current losses) and practical implementation (complexity, size and cost).

To overcome the limitations of existing gate drive topologies a novel gate drive topology is proposed to provide fast, controlled switching of power MOSFETs. The proposed topology exploits the cascode configuration with the inclusion of an active gate clamp to ensure that the driven MOSFET may be driven and held off under all load conditions.

This work explores the operation of the proposed cascode gate drive topology in the context of clamped inductive switching applications. Mechanisms to enable control of the switching process via cascode gate drive are elucidated via simulation and validated experimentally. Unique analysis tools and techniques are developed and employed to demonstrate application of cascode gate drive for switching performance optimisation.

1.1 Methodology and organisation of this thesis

The conceptual structure and summary of the contents of this thesis are presented in Figure 1.1. This section discusses the overall methodology for this work and the supporting rationale. An overview of the content of this thesis is presented by chapter in the following subsections.

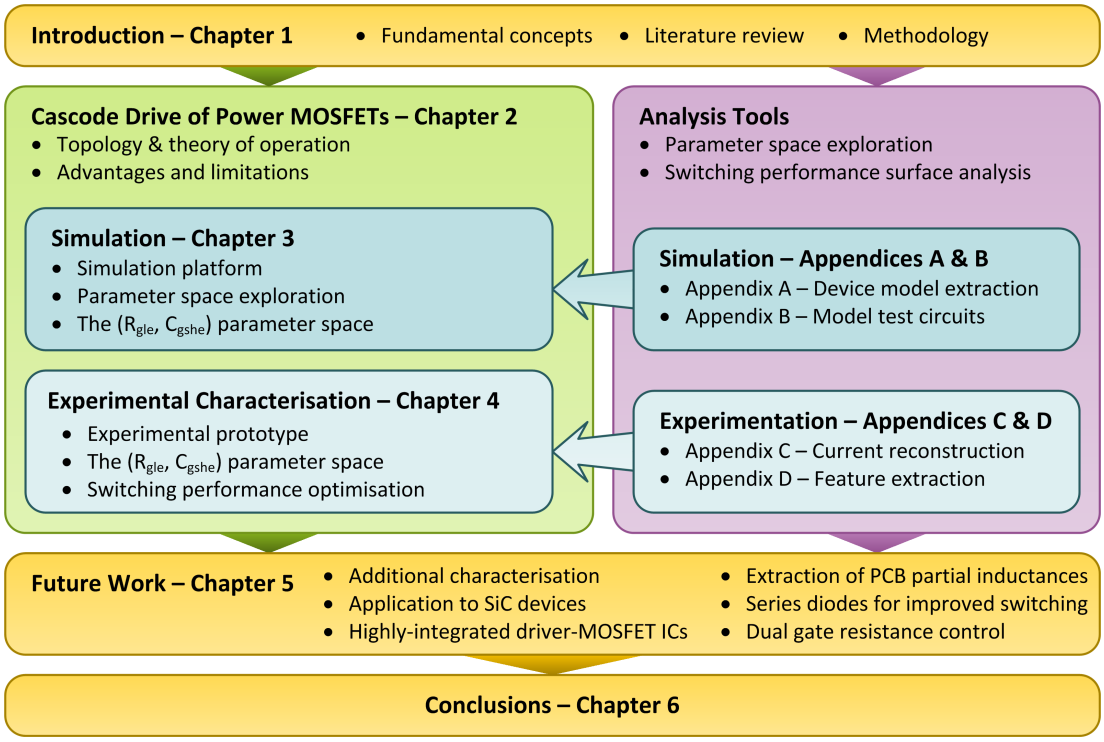


Figure 1.1: Conceptual structure and summary of the content of this thesis.

1.1.1 Chapter 1 – Introduction

Chapter 1 introduces the research problem and describes the fundamental concepts that form the foundation for this work. A literature review is presented highlighting the state of the art for the gate drive of power MOSFETs.

1.1.2 Chapter 2 – Cascode drive of power MOSFETs

A novel cascode gate drive configuration for power MOSFETs in switching applications is developed. The circuit is composed of two low-voltage n-channel power MOSFETs which drive the source of a high-voltage power MOSFET. In contrast to conventional gate drive, gate current is not sourced through a resistor, allowing high peak currents to be delivered to the gate during turn-on; long charging delays and the Miller plateau are eliminated.

In Chapter 2 the theoretical operating principles of cascode gate drive of power MOSFET are discussed. Simplified turn-on waveforms are described to aid in the understanding of the mechanisms that control the turn-on process. The action of the clamp MOSFET is also discussed. Finally, advantages and limitations of cascode gate drive are presented.

1.1.3 Chapter 3 – Simulation

Simulation is used in this work to explore the operating characteristics of the proposed cascode gate drive. Limitations of the simulation platform are explicitly acknowledged: specifically, the shortcomings of the available MOSFET models and limited ability to accurately capture circuit parasitics present in the practical circuit. Rather than attempting to address these issues via introducing substantial additional complexity to the simulation circuit, this work instead accepts that the behaviour of the simulated circuit will be of limited accuracy, but can instead be used as an effective tool for exploring the characteristic behaviour of the cascode gate drive over a broad parameter space. Findings based on the simulation work can then be validated by experimental characterisation of a prototype.

Chapter 3 presents the platform and methodology used to simulate the cascode gate drive of power MOSFETs. Comparisons between conventional and cascode gate drive switching waveforms are provided as an aid in understanding the fundamental difference in the switching process and underlying mechanisms. An exploration of the available cascode gate drive parameter space is performed in order to determine candidate parameters for control of the switching performance under cascode gate drive. The cascode MOSFET gate resistance, high-voltage MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space is subsequently identified as a candidate for further investigation. A detailed analysis of this parameter space is conducted and findings presented.

1.1.4 Chapter 4 – Experimental characterisation

Chapter 4 presents the experimental characterisation of the cascode gate drive topology applied to high-voltage power MOSFETs. Experimental characterisation of a cascode gate drive hardware prototype allows the behaviour of real power semiconductor devices and the effects of parasitic elements in a practical circuit to be captured.

Details of the implemented hardware prototype and test fixture are documented. The cascode gate drive is characterised in an inductive-clamped switching application using a double pulse test fixture. Sensitivity to the cascode MOSFET gate resistance, R_{gle}, high-voltage MOSFET gate-source capacitance,

C_{gshe}, and load current, I_L, is explored over 350 experimental operating points.

Switching performance of the cascode gate drive prototype over this parameter space is evaluated and compared with the behaviours elucidated via simulation. Opportunities for switching performance optimisation via cascode gate drive are identified.

1.1.5 Chapter 5 – Future work

Chapter 5 outlines future research opportunities that have been identified during the course of the research program summarised in this thesis. The identified research pathways fall outside the scope of this thesis.

Further characterisation of the proposed cascode gate drive topology is recommended, particularly to validate the elucidated behaviours across additional high-voltage MOSFET and cascode MOSFET devices/device combinations. Development of an analytical model is also proposed to permit better prediction of the cascode gate drive performance at design time. A methodology for the extraction of PCB partial inductances at design time is suggested.

Application of the cascode gate drive topology for driving silicon carbide (SiC) MOSFETs is proposed as a key potential application of this work. Cascode gate drive addresses some of the key limitations of SiC MOSFETs, included the requirement for higher gate drive voltage levels (typically $-2\,\mathrm{V}$ to $20\,\mathrm{V}$) and the lower transconductance of SiC devices (requiring higher gate drive currents for fast switching). The proposed cascode gate drive topology can also be trivially modified to accommodate a negative gate drive bias if required.

A number of modifications to the cascode gate drive topology are also proposed, including use of highly integrated MOSFET-driver ICs and the inclusion of low-voltage series diodes for body-diode reverse recovery elimination. Investigation of the combined use of cascode MOSFET and high-voltage MOSFET gate resistances for switching performance optimisation is also proposed.

1.1.6 Chapter 6 – Conclusions

Chapter 6 presents the key findings of this work. Key operating principles of the cascode gate drive of power MOSFETs are summarised, along with the switching performance characteristics elucidated via simulation and validated experimentally.

1.1.7 Appendices A, B, C & D – Analysis tools

A new suite of analysis tools was developed to conduct the research presented in this thesis. These tools and accompanying methodologies are captured in Appendices A through D. Other analysis tools are incorporated throughout the body of the work.

Firstly, a practical process for extraction of power semiconductor device models is developed and documented in Appendix A. A complementary collection of SPICE test circuits to evaluate the performance of extracted models is provided in Appendix B.

A post-processing methodology for reconstruction of true current from di/dt polluted current shunt measurements is developed and presented in Appendix C. A novel method for tuning the proposed reconstruction filter using experimental double-pulse switching waveforms is described.

A system for automated post-processing of experimental double-pulse waveform data to extract switching performance metrics is developed. Appendix D describes the methodology and feature extraction techniques developed and applied in this work. A MATLAB implementation of the post-processing techniques is provided.

Finally, a novel technique for the optimisation of switching performance utilising overlaid contour plots of multiple switching performance metric surfaces is demonstrated. This technique is first described in Chapter 3 and then subsequently demonstrated via application to simulated and experimental result surfaces throughout Chapters 3 and 4.

1.1.8 Appendices E & F – Results

Appendices E and F document simulation and experimental results, respectively, for which direct inclusion in the body of this thesis were not appropriate. Specifically, Appendix E presents the full collection of result surfaces from the coarse parameter sweeps conducted in Chapter 3. Appendix F indexes the full collection of attached feature extraction reports (see Section 1.1.9 below) and presents a summary of experimental turn-on waveforms for various trajectories across the (R_{gle}, C_{gshe}) parameter space.

1.1.9 Attached documentation

Attached documentation includes documents relevant to this work which were too verbose for inclusion in appendices, and/or unsuitable for hard-copy reproduction. Instead these documents are provided in soft-copy form with digital copies of this thesis.

Attached are the complete schematic diagrams for the hardware prototype, including the "MOSFET Module" and "Isolation Module" schematics.

Additionally, the feature extraction reports generated from each of the 350 experimental tests are included (each a 6-page PDF document). These reports provide complete and detailed analysis of the switching performance of the experimental prototype at each operating point; only a subset of this data is presented in the body of this work.

1.2 Fundamental concepts

1.2.1 Power MOSFETs for switching applications

When used in switching applications, power MOSFETs exhibit three characteristic regions during the turn-on (and turn-off) process [1]. These regions are commonly denoted the cut-off, active and ohmic regions respectively (see Figure 1.2). By traversing these three regions the flow of current through the MOSFET can be controlled. A MOSFET is in the cut-off region when the gate-source voltage is less than the threshold voltage. In this region the MOSFET will support its full rated drain-source breakdown voltage. As the gate-source voltage is increased above the threshold voltage the device enters the active region. In this region the drain-source current is dependent only on the gate-source voltage and is independent of the applied drain-source voltage. When the gate-source voltage is increased above the threshold voltage by more than the applied drain source voltage the MOSFET enters the ohmic region. In this region the power MOSFET transfer curve is effectively linear, and the MOSFET channel appears resistive, where increasing the gate-source voltage decreases the resistance of the channel.

In switching applications, power MOSFETs are driven into the ohmic region to achieve low conduction losses at high currents. It is the traversal of the active region, however, that largely controls the voltage-current characteristics of the device during turn-on. Two intrinsic elements of power MOSFETs that must be considered when analysing the turn-on process are the parasitic gate-source and drain-gate capacitances, as they greatly influence the turn on process. These capacitances are not constant but vary with the applied drain-source voltage. The

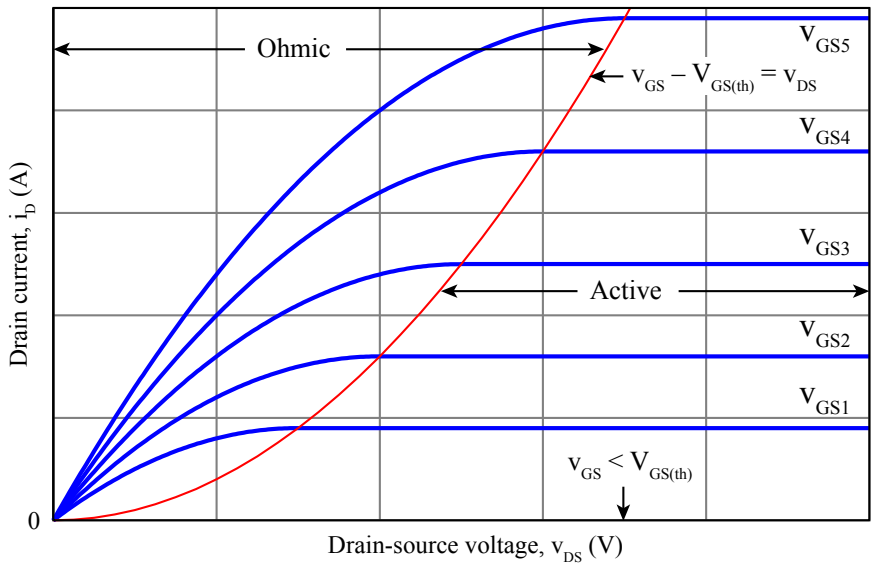


Figure 1.2: Current-voltage characteristics of a power MOSFET [7].

parasitic gate-source capacitance affects the turn-on process because to increase the gate-source voltage of the device, this parasitic capacitance must be charged. The parasitic drain-gate capacitance affects the turn-on process because as the drain-source voltage of the MOSFET decreases, a current is induced in the parasitic capacitance, drawing current out of the gate of the device. This results in the Miller phenomenon which will be discussed in subsequent sections.

Figure 1.3 shows a MOSFET model which can be used to model the switching characteristics of the device. It includes the parasitic elements that have the greatest effect on switching including parasitic capacitances, the body diode, internal gate resistance and package inductances.

1.2.2 Clamped inductive switching

A key concept in many half-bridge and full-bridge power converter topologies is clamped inductive switching. Inductive switching occurs when a half-bridge switching configuration is used to drive an inductive load. The switches in the half-bridge are modulated to regulate the load current. Thus a switching transition involves the turn-off of one switch and the turn-on of the other. A dead-time, in which neither switch is turned-on, is usually introduced to prevent excessive "shoot-through" current being conducted, as would occur if both switches were on simultaneously. Generally, it can be assumed that during a switching transition the load current is constant, as the time constant of the inductive load is very large compared with the transition time of the switches. Figure 1.4 shows a typical example of clamped inductive switching.

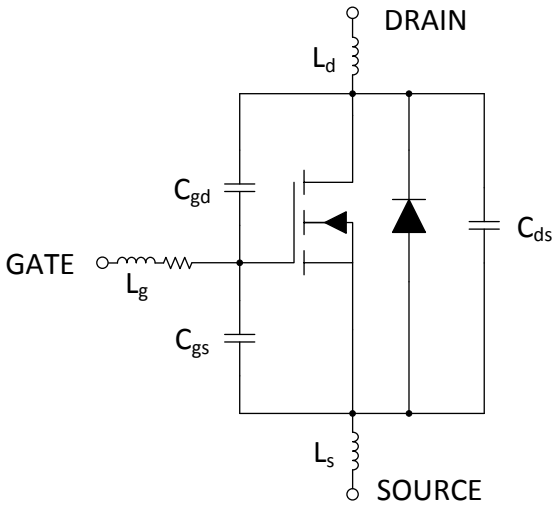


Figure 1.3: Power MOSFET switching model including parasitic elements.

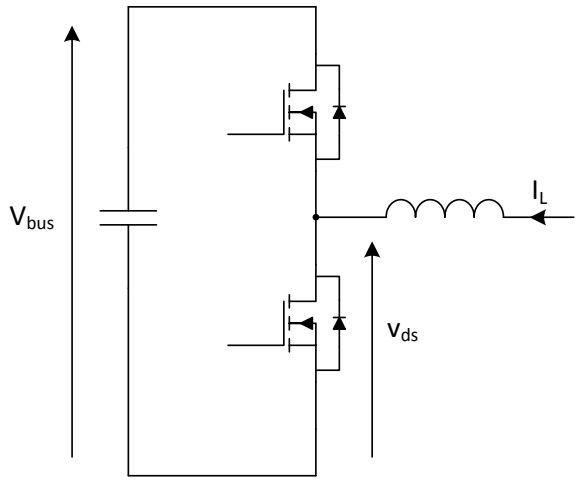


Figure 1.4: Half-bridge configuration showing clamped inductive switching.

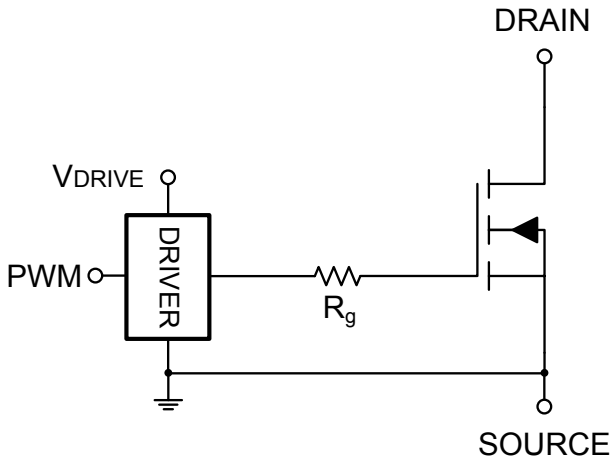


Figure 1.5: A conventional gate drive configuration.

1.2.3 Conventional voltage-driven gate drive

Conventional MOSFET gate drives are voltage driven through a gate resistor [8] (see Fig. 1.5). The gate-source capacitance is charged through the gate resistor to the supply voltage, at which time the MOSFET is fully enhanced. The gate resistor may be sized to control the switching transients of the power MOSFET, including the rate of change of drain-source voltage and current. A detailed analysis is required to fully understand the turn-on process and its effect on converter operation.

Commonly, power converters utilise inductive switching, as described previously. This is the case that will be considered when describing the turn-on process. Figure 1.6 shows the turn-on process for a power MOSFET in a clamped inductive switching application. Initially the power MOSFET is in the cut-off region with zero gate-source voltage and the load current is circulating via the upper device. The full input voltage of the supply is applied across the MOSFET drain-source and no current flows through the device.

A drive voltage is then applied to the gate resistor and the gate-source capacitance begins to charge at a rate defined by the RC time constant of the gate resistor and gate-source capacitance (the effective gate-source capacitance is relatively constant during this period due to constant drain-source voltage). Once the gate-source voltage reaches the threshold voltage, the MOSFET begins to conduct a current which increases linearly as the gate-source voltage is increased. The drain-source voltage remains unchanged while the conducted current is less than the load current. Once the full load current is established through the device, the drain-source voltage starts to transition towards zero. During the change in drain-source voltage, current is drawn out of the gate via the drain-gate capacitance. This results in the Miller plateau, in which the gate-source voltage remains constant during the change in drain-source voltage. At the end of the Miller period, when the drain-source voltage has reached its minimum, steady-state value, the gate-source voltage continues to increase towards the drive voltage, again following the RC time constant of the gate resistor and gate-source capacitance (the effective gate-source capacitance is now increased by the contribution of the gate-drain capacitance at zero drain-source voltage).

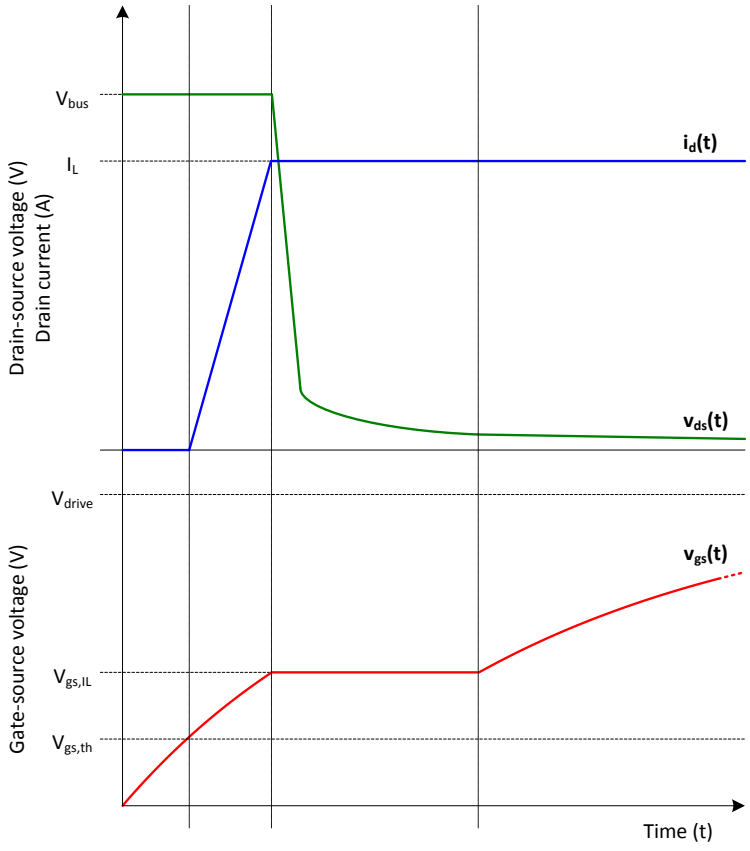


Figure 1.6: Turn-on process for a power MOSFET in a clamped inductive switching application under conventional gate drive.

1.2.4 Power MOSFET losses

Losses in power MOSFETs can be divided into two categories: switching losses and conduction losses. Switching losses occur due to the flow of current through the device during the switching transient when both drain-source current and drain-source voltage are non-zero (see Figure 1.7). Assuming linear changes in drain-source current and drain-source voltage, the switching losses may be approximated by [9]:

$$P_{loss,sw} = \frac{1}{2} I_L V_{bus} (t_{on} + t_{off}) f_{sw} \tag{1.2.4.1}$$

where $(t_{on} + t_{off})$ is the total time required, in one switching cycle, for both the current and voltage to transition, and f_{sw} is the switching frequency. It can be clearly seen that to decrease the switching losses, the transition time must be decreased. Similarly, for a specific device, the conduction losses may be minimised by reducing the time required to fully enhance the MOSFET after the Miller region. Using a voltage driven gate drive, the device will be conducting at a higher effective resistance for a period of time, related to the RC time constant involved in charging the gate-source capacitance.

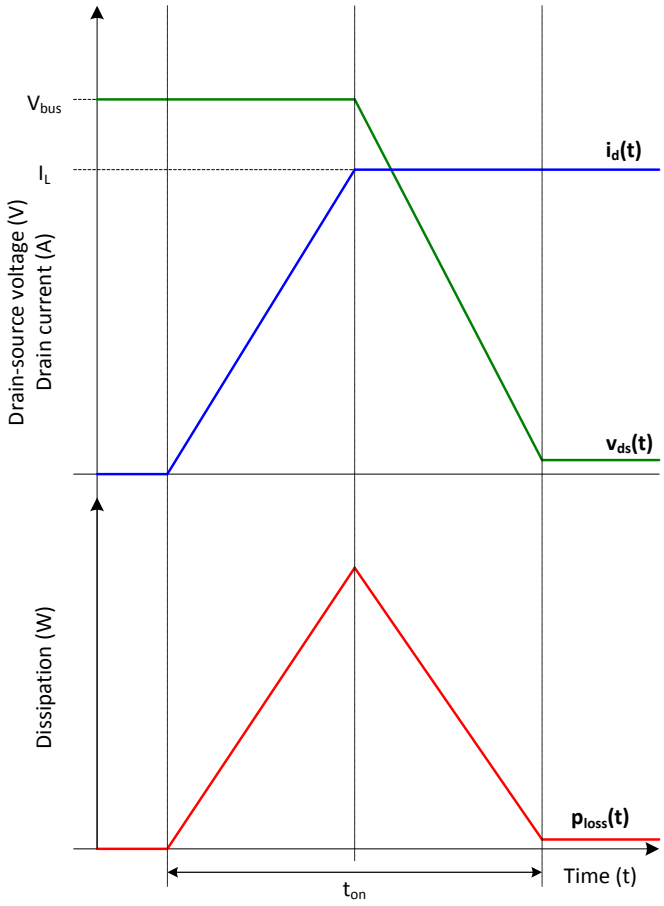


Figure 1.7: Simplified turn-on switching waveforms showing switching and conduction losses. The turn-off process is the mirror of the illustrated turn-on process.

1.2.5 Benefits of high switching frequency operation

Increasing the switching frequency of power electronic converters is attractive due to the reduced requirements for magnetic components when operating at high frequency. Magnetic components generally constitute a large component of the cost, size and weight of a power converter. Furthermore, the cost is largely irreducible at production volumes due to limiting material costs of iron and copper and the manufacturing costs of producing wound components. By increasing the switching frequency, smaller magnetic components may be used yielding high power density, lower losses and lower costs.

Increasing the switching frequency of a converter, however, has a number of implications. Firstly, switching and gate drive losses are directly proportional to the switching frequency. To maintain converter efficiency at a higher switching frequency it would therefore be necessary to decrease switching losses.

Secondly, as switching speeds are increased, the influence of parasitic circuit elements becomes more pronounced. These include device parasitics (parasitic capacitances and package inductances) and layout parasitics (primarily inductances). As switching speeds increase, rates of change of voltage and current must, by definition, increase, leading to higher voltages/currents being established across/through parasitic elements. Typically this is detrimental to the operation of the switching circuit, and ultimately may lead to unacceptable device stresses and failure of the switching devices.

Finally, the high slew rates associated with fast switching transitions can result in unacceptable levels of electromagnetic interference (EMI). This problem is exacerbated by the presence of parasitics which can lead to high-frequency "ringing" (up to hundreds of megahertz) at the leading and trailing edges of switching transients.

The maximum practical switching frequency is also limited by the minimum achievable pulse width. Turn on times for power MOSFETs driven by conventional gate drive circuits range from tens of nanoseconds to microseconds. For pulse width modulated (PWM) converters, the switching period should be much larger than the minimum pulse width to ensure low output distortion. Thus, for successful operation of PWM converters at high switching frequencies, the transition time of the power MOSFETs should be minimised.

1.3 Literature review

1.3.1 Power MOSFET failure modes

When designing any gate drive circuit for power MOSFETs, great care must be taken to address a number of common failure modes that have been identified. Furthermore, many potential reliability issues are exacerbated at high switching frequencies. A common failure mode for power MOSFETs is dv/dt induced turn on of the MOSFET due to parasitic capacitances in the MOSFET structure (see Figure 1.8) [10]. Modern power MOSFETs are practically immune to dv/dt induced turn on of the parasitic bipolar transistor [8], however, they are still prone to turn on due to current induced through the parasitic drain-gate capacitance [11]. Conventional techniques for dealing with this phenomenon have included MOSFET selection, reduced gate drive resistance and negative gate drive [12]. For higher switching frequencies, the dv/dt issue cannot be solved simply by good MOSFET selection due to limits in MOSFET technology.

Negative gate drive does not eliminate the spike in gate-source voltage, but simply offsets it below the turn-on threshold. This scenario is hardly ideal and is ineffective if the dv/dt induced voltage spike is of sufficient magnitude. It has also been demonstrated in the literature that a negative gate bias can introduce ringing on both the drain-source voltage as well as the gate-source voltage [13].

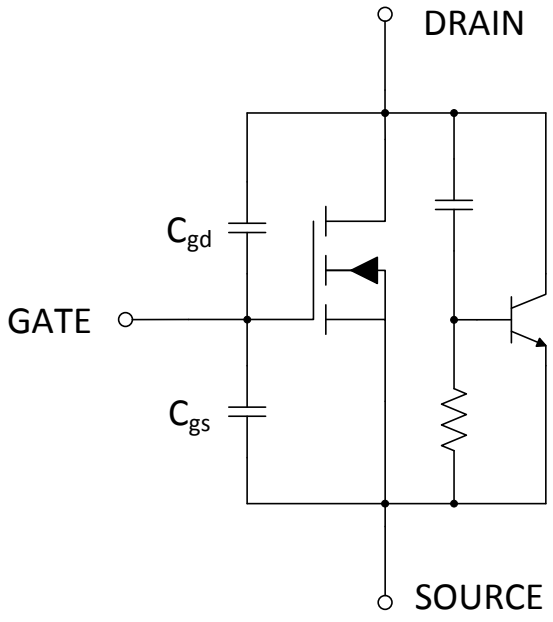


Figure 1.8: Equivalent circuit of a power MOSFET for modelling dv/dt induced failure modes.

The effectiveness of reducing the turn-off impedance is also limited, due to parasitic inductances in the power MOSFET package. Reducing the gate-source impedance may be achieved through the addition of external gate-source capacitors or a low impedance auxiliary clamp. For these methods to be exploited the MOSFET parasitic inductance should be minimised. This can be achieved through the use of advanced MOSFET packaging [14] or by mounting the MOSFET die directly. Reducing or eliminating the package inductance has added benefits for MOSFET switching times [15], which is essential for higher frequency operation. Using direct die-mounting techniques, switching times of 6 ns [16] have been successfully demonstrated for power MOSFETs compared to typical MOSFET switching speeds of 60 ns [8]. The use of coupled inductors on the half bridge, as presented in some topologies in literature [17], could also be used to limit $\mathrm{d}v/\mathrm{dt}$ induced turn-on, by reducing the voltage transients seen by the MOSFET during the off period. This topology has the additional benefit of requiring no dead-time between the upper and lower MOSFETs, which could be a distinct advantage at higher switching frequencies.

A second failure mechanism for power MOSFETs is the over-voltage transients on the gate-source voltage during the Miller period. These transients are usually as a result of oscillations of the gate-source voltage at the Miller plateau, caused by the body-diode reverse recovery phenomenon [18] or interaction between parallel MOSFETs [19, 20]. Interaction between parallel MOSFETs can be eliminated by ensuring sufficient impedance between the gate drive of independent MOSFETs. Recovery of the body diode, however, results in high-frequency ringing on the half-bridge during the Miller period. This ringing is coupled onto the gate by the parasitic (or externally added) gate-source capacitance or drain-gate capacitance for the high-side and low-side MOSFETs respectively. By reducing the rate of change of reverse recovery current available to the diode, this effect can be minimised.

Rate of change of reverse recovery current may be reduced with a conventional voltage driven gate driver by increasing the gate drive resistance, resulting in a consequential increase in turn-on delay and switching losses. A two-stage gate drive system is presented in the literature [21], which utilises two different gate resistances to control this phenomenon: a low drive current is delivered during the initial turn-on period, and subsequently, a higher gate current is delivered to quickly drive the device to full enhancement. This system showed distinct improvements in terms of oscillations due to diode reverse recovery.

1.3.2 Body diode reverse recovery

Once a power diode has been conducting in the forward state, it requires a finite time to switch to the blocking state [8], in which a reverse voltage may be supported. This is equally true of the power MOSFET parasitic body diode. Time and reverse current is required to remove the minority carriers from the drift region of the power diode before a reverse voltage can be established. This time is generally referred to as the reverse recovery time. The switching transients during reverse recovery, including the reverse recovery time and peak reverse recovery current, are dependent on the specific device and the rate of change of current through the diode during turn-off.

Certain power converter topologies require reverse current to flow through the switching devices. When MOSFETs are used, this generally results in the body diode conducting a portion, or all, of the load current. This has a number of detrimental effects on converter operation. Firstly, high reverse recovery currents result in increased switching losses as the peak reverse recovery current must be conducted during maximum drain-source voltage by the opposing MOSFET in the half-bridge. This can lead to operation of the MOSFET outside the safe operating area, resulting in failure of the device. A second failure mode exists, whereby reverse recovery of the body diode under light load conditions can result in the latch-up of parasitic bipolar transistor inherent in the MOSFET structure [22, 23]. Fast recovery of the body diode may also introduce high-frequency oscillations onto the half-bridge during a switching transition. These oscillations can be coupled onto the gate of the power MOSFET through the parasitic drain-gate and gate-source capacitances which may result in over-voltage failures or inadvertent turn-on of the power MOSFET. Finally, the finite reverse recovery time places a limit on the minimum achievable switch transition time which in turn limits the maximum achievable switching frequency.

A number of solutions have been proposed to reduce the effect of body diode reverse recovery on converter operation and reliability. One solution is to limit the rate of change of reverse current through the body diode by increasing the turn-on time of the switching devices [24]. This reduces the peak reverse recovery current and limits high-frequency oscillations caused by reverse recovery. Increasing the turn-on time on the MOSFETs, however, results in increased switching losses and reduces the achievable switching frequency.

Reverse conduction of the MOSFET channel may also be used to reduce the effect of reverse recovery on converter operation [25]. If the MOSFET is turned on before the body diode begins to conduct, then the reverse current will be diverted through the MOSFET channel. For this method to work the voltage

drop across the channel when conducting the peak load current must be less than the threshold voltage of the body diode, otherwise the body diode will conduct a proportion of the load current. Even this situation has benefits [26], however, as the current conducted by the diode is reduced, resulting in reduced reverse recovery charge. This method also requires that there exist a finite time in which a MOSFET may be turned on to divert the current before it commutates through the body diode. This is not always the case for clamped inductive switching. For example, when a power MOSFET that is conducting reverse current is turned off, the current will immediately commutate to the body diode; there is no delay in which the MOSFET could be turned on to support the current before the body diode conducts.

A method used to avoid reverse recovery completely is to place a diode in series with the MOSFET such that the body diode can never conduct [23, 27, 28]. An anti-parallel Schottky diode is then placed around the MOSFET-diode combination to support any reverse current. Schottky diodes are a majority-carrier device formed by placing a thin film of metal directly in contact with a semiconductor [1]. As no minority carriers exist in the device, these diodes do not undergo reverse recovery. The major disadvantage of this method is an increase in conduction losses due to the forward voltage drops of the series diode and reverse Schottky diode in forward conduction, and the anti-parallel Schottky diode in reverse conduction. This method also prevents savings in conduction losses by paralleling MOSFETs, as the forward voltage drop of the diodes is irreducible.

A final method proposed to avoid reverse recovery of the body diode is through the use of a series MOSFET [28]. A low voltage MOSFET may be placed in series with the power MOSFET such that their sources are common. A Schottky diode is then placed in anti-parallel with the series combination. When off, the low voltage MOSFET prevents reverse current from flowing into the body diode of the power MOSFET. Instead the current is conducted by the Schottky diode, which doesn't exhibit reverse recovery. When both the power MOSFET and low voltage MOSFET are turned on, current can flow in both the forward and reverse directions. There are no additional drive requirements for this configuration as the MOSFETs share a common source, so they may be driven by the same driver. The additional losses from adding the low-voltage MOSFET in the load current path is minimal given that the on-resistance of low voltage MOSFETs is generally two orders of magnitude lower than that of high-voltage MOSFETS.

1.3.3 Alternatives to voltage driven gate drive

The disadvantages of conventional voltage driven gate drives for high switching frequency operations has led to the development of alternative gate drive topologies. These can be loosely categorised as either current driven, or resonance driven [29]. In both cases, an inductive magnetic component is used to charge the gate-source capacitance of the power MOSFET. The magnetic component may take the form of an inductor [3–6, 30–37], coupled inductor [31] or transformer [31, 38], depending on the topology.

The use of an inductive component allows current to be delivered to the gate in a controlled and near-lossless manner, without the need for a gate resistor. Current driven topologies achieve this by establishing a constant drive current through an inductive element and switching this current into (or out of) the gate of the power MOSFET to charge (or discharge) the gate capacitance. When the current is not being used to drive the power MOSFET it is allowed to circulate. Resonant drive topologies utilise the resonance of the inductive element with the gate capacitance. These topologies may use full resonance, where the gate voltage approaches twice the supply voltage, or clamped resonance, where the gate voltage is clamped to the supply voltage and remaining current is recovered or dissipated [29]. The major advantage of these charging mechanisms is that drive energy may be partially or fully recovered, which is particularly important for loss savings at high switching frequencies.

A current driven gate drive may supply constant current to the gate of the power MOSFET, independent of the gate voltage, resulting in reduced turn-on times and hence, switching losses. The magnitude of the current may be regulated to achieve the required turn-on times. The disadvantage of this solution is that continuously circulating the drive current when it is not being utilised in a switching transition results in losses that may exceed any savings in recovered drive energy. The alternative is the use of a high-inductance, low-resistance inductor, resulting in poor energy density and high cost [29].

Current flow in resonance driven gate drivers is discontinuous, with all the energy in the inductor being delivered into the gate capacitance, or recovered. The resonant inductance must therefore be selected to achieve the required turn-on time. The disadvantage of resonance driven gate drive is that it is sensitive to series resistance, including the internal gate resistance, which can result in minimal energy recovery [29]. Also, if the gate voltage is not clamped, the drive inductor presents a high impedance to the gate which can result in $\mathrm{d}v/\mathrm{dt}$ induced turn on of the power MOSFET.

A commonly utilised topology, which can be used to implement either a current driven or clamped resonance driven gate driver, is a full bridge of low-voltage MOSFETs used to drive an inductor [5, 30, 32, 33, 36–38]. This topology provides low impedance clamping of the power MOSFET gate to provide immunity to dv/dt induced effects. The topology may also be modified to provide a negative gate bias. The major disadvantage of this topology is the additional complexity required to control the four active switches. When controlled to be current driven it also exhibits pulse width limitations due to the time required to reverse the current through the inductance.

1.3.4 Cascode configuration

A cascode configuration can be formed by the combination of two transistors: either bipolar junction transistors (BJTs), FETs or a combination of the two (see Figure 1.9) [39]. Commonly this configuration is used to form a cascode amplifier. The base (or gate) of the upper device is held at a constant DC voltage. The base (or gate) of the lower device is then driven, allowing the upper device to turn on. This configuration has significant advantages for fast (e.g. radio frequency) amplifiers, as it eliminates the Miller effect of the upper device.

The cascode configuration can also be used for switching applications [40–46]. As with the cascode amplifier, the cascode configuration can be used with two MOSFETs to achieve faster switching and improved efficiency by eliminating the Miller effect [40]. It has also been used to improve the switching performance of a BJT by adding a low voltage MOSFET in cascode configuration to realise a high-current, high-voltage switch [42, 43, 45]. The cascode configuration has also been used for driving normally-on silicon carbide junction FETs (JFETs) for high-voltage switching applications. This technique has been demonstrated for driving both single JFETs [46], as well as series connected JFETs for switching several kilovolts [41].

While the cascode driven switches have been used in bridge configurations, the switches have been limited to BJTs. The turn off mechanism for a BJT in a cascode configuration exists independent of load conditions, as a BJT is a current driven device. This is not the case for a MOSFET in a cascode configuration. In a low side switching application the gate-source capacitance of the MOSFET will be discharged through the drain-source resistance. When the MOSFET is conducting reverse current, however, this turn-off mechanism does not exist. Rather, due to the bias voltage applied to the gate, the gate of the driven MOSFET will remain enhanced so long as reverse current continues to flow.

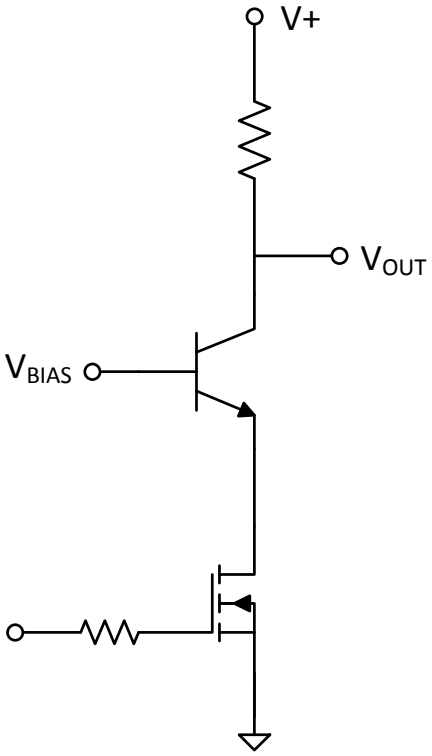


Figure 1.9: A typical cascode amplifier configuration composed of a BJT and MOSFET.

The MOSFET gate will only be discharged once the load current commutates out of the MOSFET into the opposing switching device in the half-bridge. Typically this would occur when the opposing device turns on. This may result in the MOSFET under cascode drive being exposed to substantially higher rates of change of current and voltage during turn-off (i.e. limited only by the turn-on speed of the opposing switching device). The cascode device cannot be used to control the turn-off process in this situation, potentially leading to unacceptably high switching stresses on the driven MOSFET.

1.3.5 Power MOSFET modelling

Simulation is often used for evaluating and designing power converters and gate drive circuits. For simulation to be valuable, however, the results must be valid and accurate. This relies on the underlying circuit models being valid for the mode of operation. The ability to accurately predict device behaviour during the design phase is also hampered by the limited information available on semiconductor device parasitics. Semiconductor datasheets generally describe parasitic circuit elements at a specific operating point, usually outside nominal operating condition [47]. Other elements, such as parasitic package inductances, are rarely included. There are methods available for extracting theses parameters experimentally [48–50], however, these methods are often complex and require

specialised equipment. This is also not an effective process for device selection at the design stage.

Classical MOSFET models are based on the assumption that the parasitic MOSFET capacitances completely describe the switching operation of the device [51]. Most classical models also only consider these capacitances to be dependant on one terminal voltage [47]. These models do not take into account the parasitic inductances [9, 52], which tend to limit the switching performance in practice, particularly for high switching frequency operation.

There has been much focus recently on developing accurate models for predicting MOSFET losses [9, 51–54]. While these models can accurately describe MOSFET switching losses they either rely on device characteristics that are not generally available to designers [9, 53] or are based on the assumption of specific drive scenarios [51, 52, 54], such as conventional voltage driven gate drive. These models may provide a useful tool for design engineers to estimate converter losses, but do not provide a meaningful insight into the switching process, or transients, which is critical for gate drive design.

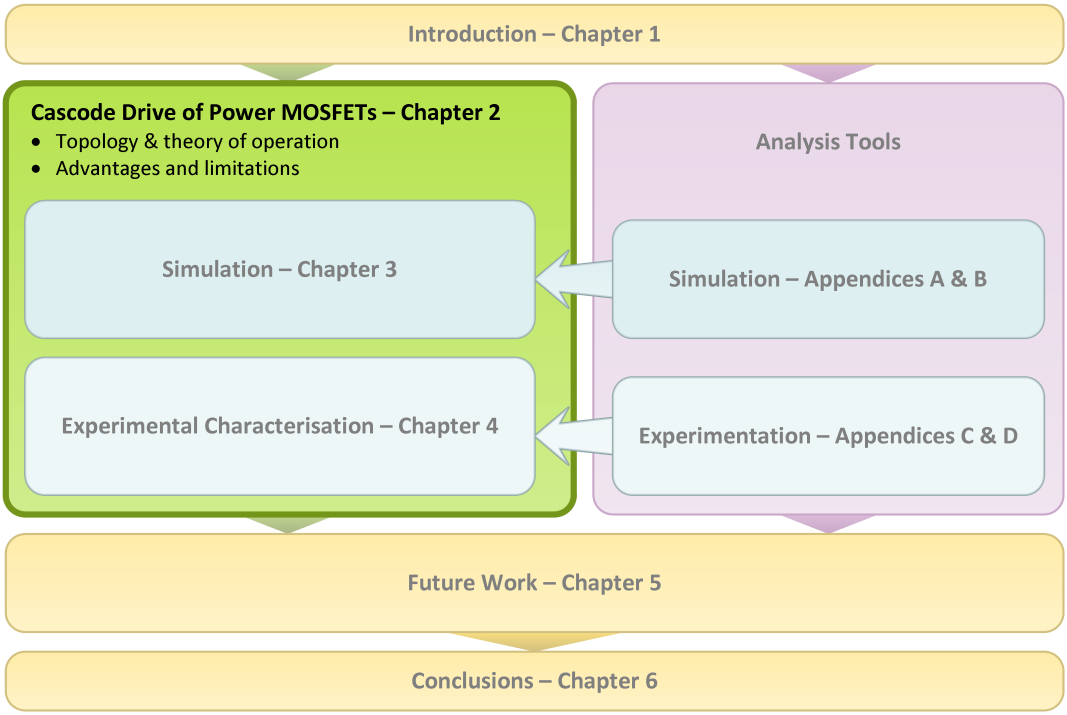
Analytical models are an alternative to complex physical based or complete MOSFET models. These models are usually based on certain simplifications, and so are less accurate [52]. Analytical models have the advantage, however, of providing insight into the switching process and mechanisms, allowing immediate comparison of different operating conditions or semiconductor devices.

There exists a gap in the literature for the modelling of MOSFET switching in the domain of high switching speeds and unconventional drivers. Advanced MOSFET driver design requires a MOSFET model that provides insight into the switching process and mechanisms, and that is not dependant on a specific domain of operating conditions. Existing MOSFET models do not address these requirements. Classical models exclude MOSFET characteristics and parasitics that are important at high switching speeds and are generally based on switching under conventional voltage fed gate drive. Physical based or complete MOSFET models can be used to accurately model specific devices, but provide limited insight into the switching process and generally require information on device characteristics that is unavailable to designers. Alternative methods, such as analytical models, may provide a more valid tool to evaluate the high speed switching of MOSFETs using unconventional drivers.

Chapter 2

Cascode gate drive of power MOSFETs

Presented in this chapter is a novel cascode gate drive configuration for power MOSFETs in switching applications. The theoretical operating principles of the proposed cascode gate drive circuit are discussed. Simplified turn-on waveforms are derived and a summary of the advantages and limitations of cascode gate drive is presented.



2.1 The proposed cascode gate drive topology

The proposed cascode gate drive circuit is shown in Figure 2.1. The circuit is composed of two low-voltage n-channel power MOSFETs, Q1 and Q2, which are used to drive high-voltage power MOSFET Q3. The cascode MOSFET, Q2, is connected from the source of Q3 to the effective source of the entire module. The clamp MOSFET, Q1, is connected between the gate and source of Q3.

A voltage source, $V_{drive,HV}$, capable of both sinking and sourcing current, is connected from the gate of the high-voltage MOSFET to the source of the cascode MOSFET. The magnitude of this voltage source should be equal to the maximum desired gate drive voltage for the high-voltage MOSFET. Bypass capacitors are connected in parallel with $V_{drive,HV}$.

A bootstrap driver is used to drive the clamp and cascode MOSFETs through gate resistors R1 and R2 respectively. The bootstrap driver may be supplied from a separate voltage source, $V_{drive,LV}$, to allow the use of low voltage clamp and cascode MOSFETs that are optimized for lower drive voltages. Diodes D1 and D2 may be optionally connected in anti-parallel with resistors R1 and R2 respectively to provide dead time between the clamp and cascode MOSFETs when switching.

The cascode driver circuit may be also implemented using a number of alternative configurations, while achieving the same operating characteristics. A p-channel MOSFET may be used for the clamp MOSFET, for example, to allow both the clamp and cascode MOSFETs to be driven from the same driver IC, and from the same drive voltage source as the high-voltage MOSFET, simplifying the circuit implementation.

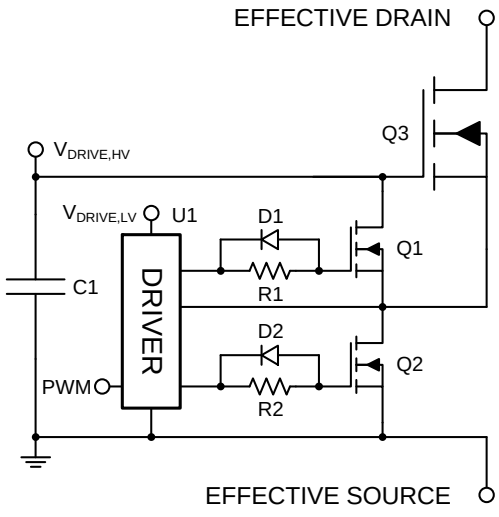


Figure 2.1: The proposed cascode gate drive topology.

2.2 Theory of operation

2.2.1 Action of the clamp MOSFET

In the presence of positive drain-source current the high-voltage MOSFET will turn off naturally when the cascode MOSFET is turned off. The load current will commutate from the cascode MOSFET to instead discharge the gate-source capacitance of the high voltage MOSFET. Any excess current flows through the external source-gate diode (or body-diode of the clamp MOSFET in the proposed topology) and is returned to the drive voltage source $V_{drive,HV}$ which clamps the gate voltage of the high-voltage MOSFET. $V_{drive,HV}$ must be capable of sinking current to ensure the drive voltage is not pumped-up over a number of turn-off cycles.

In the case of reverse channel conduction, however, natural turn-off of the high voltage MOSFET with the cascode MOSFET is not guaranteed. Additionally, as the natural turn-off is affected by the load current the natural turn-off process is load dependant.

To overcome these limitations the clamp MOSFET is included in the proposed topology to ensure that the high-voltage MOSFET can be turned off independent of load conditions. The clamp MOSFET can be turned on to discharge the gate-source capacitance of the high-voltage MOSFET through the low impedance of the channel of the clamp MOSFET. Dead time must be introduced between the turn-on of the clamp and cascode MOSFETs to avoid shoot-through currents from discharging the gate-drive supply. The clamp MOSFET may also be held-on during the off-period of the high-voltage MOSFET to provide a low-impedance clamp to ensure the high-voltage MOSFET is not unintentionally turned on by applied transients.

During turn-off, the drain-source characteristics of the high-voltage power MOSFET are not tightly coupled to the gate-source voltage profile. Rather, the half-bridge transition is dominated by either the charge/discharge of parasitic capacitances by the load current, or the turn-on transient of the opposing switching device. For these reasons, the primary focus of this work is on the control and optimisation of the turn-on process for the cascode gate drive topology.

Simulation of the natural and active-clamped turn-off processes are provided in Section 3.5, while experimental validation of the turn-off performance of the proposed topology is detailed in Section 4.5.4. Finally, a discussion of the reverse-conduction characteristics of the proposed topology and opportunities for future research is provided in Section 5.7.

2.2.2 Simplified turn-on process

The turn-on process for the cascode driver circuit is more complex than that of the conventional resistor-fed gate driver, as the cascode MOSFET conducts both the load current and the gate current of the high-voltage MOSFET. We examine the turn-on process for a cascode driven high-voltage MOSFET in a clamped inductive switching application. The simplified switching waveforms and corresponding current paths during turn-on are shown in Figures 2.2 and 2.3 respectively.

Prior to turn-on, the entire load current is circulating through the clamping diode to the bus and the voltage at the drain of the high-voltage MOSFET is clamped to the bus voltage (interval T_A). The clamp MOSFET, Q1, is turned off.

At t_0, the driver IC applies the drive voltage, $V_{drive,LV}$, to the cascode MOSFET drive resistor, R2. The gate-source capacitance of the cascode MOSFET then begins to charge through the gate resistor (see Fig. 2.3a). The gate of the cascode MOSFET continues to charge towards voltage $V_{drive,LV}$ during interval T_A (see Fig. 2.2), following an exponential relationship with a time-constant defined by the gate resistance and gate-source capacitance. Period T_A ends at t_1, when the gate-source voltage is equal to the threshold voltage of the cascode MOSFET, $V_{gs(th),ca}$.

At time t_1, the channel of the cascode MOSFET begins conducting. During interval T_B, current flows through the channel of the cascode MOSFET to charge the gate-source capacitance of the high-voltage MOSFET (see Fig. 2.3b). The gate-source voltage of the high-voltage MOSFET increases as the drain-source voltage of the cascode MOSFET decreases, due to the voltage $V_{drive,HV}$ being held constant. The rate of change of gate-source voltage of the high-voltage MOSFET is therefore controlled by the Miller effect of the cascode MOSFET.

During this interval the entire cascode gate current flows through the gate-drain (Miller) capacitance of the cascode MOSFET, as shown in Figure 2.3b. The gate current is controlled by the gate resistance, which subsequently controls the rate of change of gate-source voltage of the high-voltage MOSFET as the current flowing into the gate-drain capacitance is proportional to the rate of change of drain-source voltage on the cascode MOSFET. As all current flows through the gate-drain capacitance, no current is available to charge the gate-source capacitance such that the gate-source voltage of the cascode MOSFET remains constant during this interval. Interval T_B ends at t_2, once the gate-source voltage of the high-voltage MOSFET reaches the threshold voltage, $V_{gs(th),HV}$.

At time t_2, the channel of the high-voltage MOSFET begins conducting the

load current. As shown in Figure 2.3c, the load current must also be conducted by the cascode MOSFET. The gate-source voltage of both the cascode and high-voltage MOSFET must therefore increase during interval T_C to support the load current. The rate of change of drain current will be dependant on a number of factors, including the relative transconductances of the cascode and high-voltage MOSFETs. A low-voltage cascode MOSFET will usually have a transconductance orders of magnitude higher than that of the high-voltage MOSFET.

The cascode MOSFET must also conduct the current required to charge the gate of the high-voltage MOSFET. The current available to charge the gate of the high-voltage MOSFET is the difference between the drain current of the cascode MOSFET and the drain current of the high-voltage MOSFET. Typically the current required to charge the gate of the high-voltage MOSFET will be only a fraction of the load current. Combined with the difference in relative transconductances, this will typically result in the cascode MOSFET controlling the rate of change of load current during this interval.

As the drain current of the high-voltage MOSFET increases, current commutates from the high-side diode. Interval T_C ends at time t_3 when the entire load current, I_L, is supported by the high-voltage MOSFET. It should be noted that reverse recovery of the high-side diode is not considered in the simplified turn-on process, but would usually occur between intervals T_C and T_D.

At time t_3 the voltage at the drain of the high-voltage MOSFET begins to transition. During interval T_D, the drain-source voltage of the high-voltage MOSFET decreases. This results in a current flowing through the parasitic gate-drain capacitance which is proportional to rate-of-change of drain-source voltage and gate-drain capacitance. As there is no resistance in series with the gate of the high-voltage MOSFET, however, the gate current is not limited and the gate of the high-voltage MOSFET may be charged simultaneously.

As the gate of the high-voltage MOSFET is charged, the gate-source voltage of the high-voltage MOSFET increases and consequently the $\mathrm{d}v_{ds}/\mathrm{dt}$ also increases. The entire gate current of the high-voltage MOSFET must be conducted by the cascode MOSFET. The drain-source voltage of the cascode MOSFET decreases as the gate-source voltage of the high-voltage MOSFET increases, and hence, the time rate-of-change of gate-source voltage on the high-voltage MOSFET is controlled by the Miller effect of the cascode MOSFET, similar to interval T_B. As shown in Figure 2.2, the drain-source voltage of the high-voltage MOSFET decreases rapidly until it approaches the same magnitude as the gate-source voltage. At this time the gate-drain capacitance increases rapidly, due to the non-linear dependence of gate-drain capacitance on drain-source voltage.

The fall rate of drain-source voltage decreases significantly at this point due

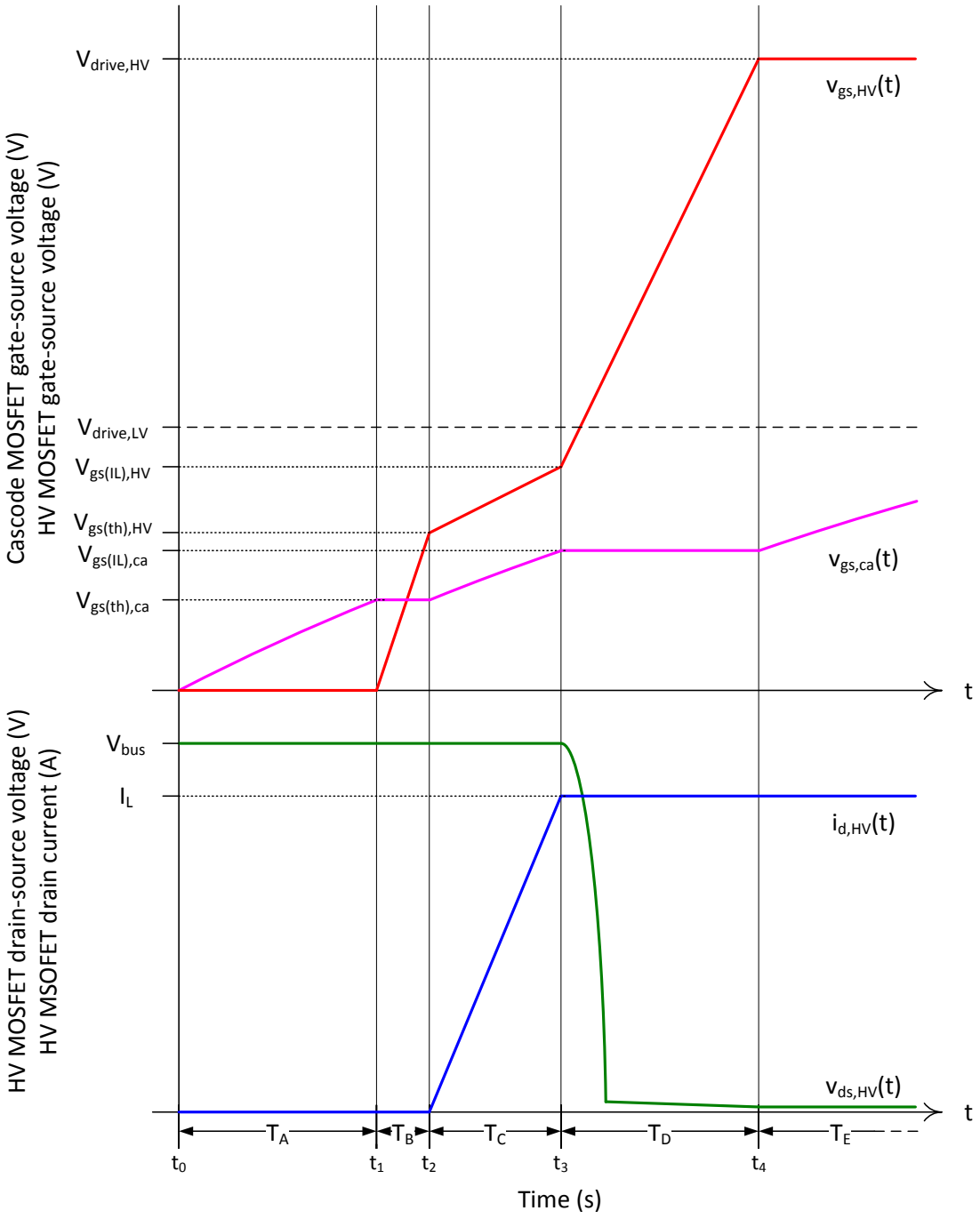


Figure 2.2: Simplified turn-on waveforms for the cascode gate drive circuit.

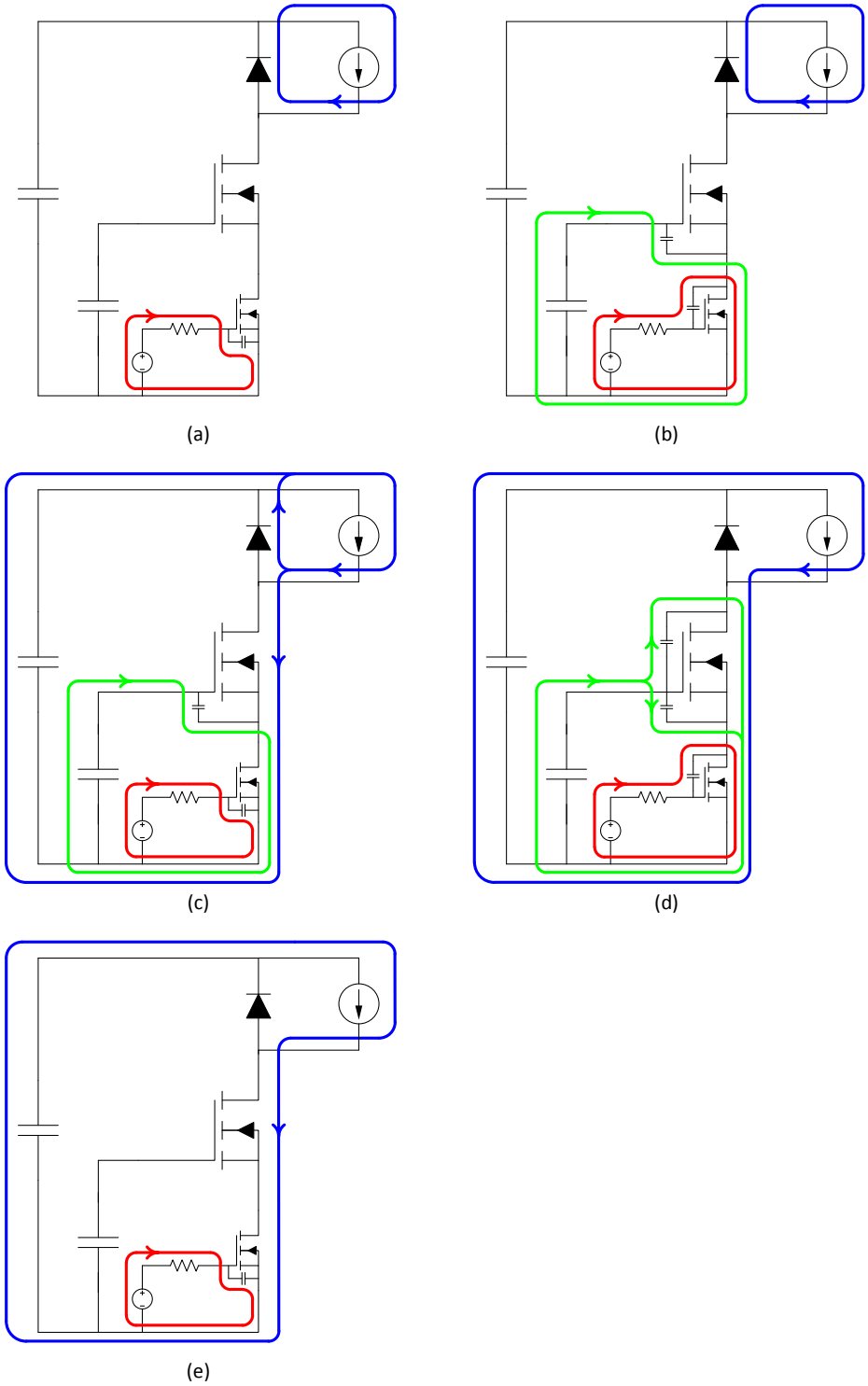


Figure 2.3: Current paths through the cascode gate drive circuit during turn-on. Subfigures correspond each discrete time interval identified in Figure 2.2: (a) Interval T_A. (b) Interval T_B. (c) Interval T_C. (d) Interval T_D. (e) Interval T_E.

to the increase in parasitic capacitance; higher gate and drain currents are transiently required to drive the MOSFET fully on. In the absence of a Miller plateau, however, the high voltage MOSFET is still able to be driven towards full enhancement during this interval, greatly reducing the turn-on time. Interval T_D ends at time t_4, once the gate-source voltage of the high-voltage MOSFET has increased to the supply voltage $V_{drive,HV}$.

Interval T_E extends from time t_4, until the gate of the cascode MOSFET is fully charged to the drive voltage, $V_{drive,ca}$. During this interval the load current is fully supported by the high-voltage MOSFET and the high-voltage MOSFET is fully enhanced, with the channel resistance having reached its minimum, steady-state value. The gate of the cascode MOSFET continues to charge through the gate resistor, however, given that the channel resistance of the cascode MOSFET is orders of magnitude lower than that of the high-voltage MOSFET, fully enhancing the gate of the cascode MOSFET is not critical; any reduction in the total resistance in the load path is negligible during this interval.

2.3 Advantages and limitations

2.3.1 Advantages

2.3.1.1 Higher drive current capability

In a conventional resistor-fed gate drive circuit, all current required to charge the gate of the power MOSFET must be sourced from the driver – typically a driver IC or transistor pair with limited current sourcing/sinking capability. The peak current that may be delivered to the MOSFET gate is also limited by the series resistance used to control the switching speed of the MOSFET.

The cascode driver allows high peak currents to be delivered to the MOSFET gate, regardless of the state of charge of the gate. As there is no series resistance present, the peak gate current is limited only by the cascode MOSFET.

2.3.1.2 Reduced gate charging time

In the conventional resistor-fed gate drive circuit, the charging of the MOSFET gate is constrained by the RC time constant of the gate resistor and parasitic gate-source capacitance of the power MOSFET, resulting in long turn-on delays. Instead the cascode MOSFET directly controls the rate of change of gate-source voltage of the high-voltage MOSFET. The rate of change of gate voltage is then largely linear which allows the gate-source voltage to be driven quickly to the threshold voltage and then the turn-on region to be traversed rapidly in a con-

trolled manner. The time to fully enhance the gate to the maximum drive voltage is greatly reduced as there is no RC time constant involved in charging the gate – the charging process is instead controlled by the characteristics and control of the cascode MOSFET.

2.3.1.3 Reduced gate drive power requirements

The cascode MOSFET drive requirements are significantly less than those of the high-voltage MOSFET. Further, the use of lower drive voltages and currents is possible due to the higher transconductance of low-voltage MOSFETs. In many cases it may be possible to use a logic-level output to drive the cascode MOSFET.

Due to the natural turn-off mechanism it is possible for the majority of the high-voltage MOSFET gate drive energy to be recovered into the gate drive supply from the high-voltage bus during turn off under forward channel conduction. This significantly reduces the gate drive power supply requirements.

2.3.1.4 Improved dv/dt immunity

In the cascode driver the gate of the high-voltage MOSFET is always connected to a low-impedance voltage source. Any currents which are injected into the gate via voltage transients applied to parasitic capacitances are bypassed by this supply, improving immunity to dv/dt inducted turn-on. Additionally, during the off-period the clamp MOSFET provides a very low-impedance shunt across the gate-source of the high-voltage MOSFET to hold the MOSFET off under all conditions.

2.3.1.5 Negative gate drive capability

The cascode driver is also ideally suited to provide a negative gate voltage bias during the off period. A simple modification to the topology whereby the drain of the clamp MOSFET is connected to a voltage source slightly higher than that of the drive voltage source would provide this functionality. The cascode driver would therefore be ideally suited to driving silicon carbide power MOSFETs which require a negative gate bias to hold them off and high drive current for fast switching times due to their significantly reduced transconductance compared with standard silicon power MOSFETs.

2.3.2 Limitations

2.3.2.1 Increased conduction losses

Introduction of the cascode MOSFET into the load current path results in additional conduction losses due to the channel resistance, $R_{ds,on}$, of the cascode MOSFET. Note, however, that as the cascode MOSFET is a low-voltage device it will typically have an $R_{ds,on}$ value orders of magnitude lower than that of the drive high-voltage MOSFET. Any increase in conduction losses is therefore largely negligible. As an example, the HV and cascode MOSFETs used in the experimental sections of this work have typical $R_{ds,on}$ values of 199 mΩ and 1.1 mΩ respectively: in this case we expect a less than 0.6 % increase in conduction losses.

2.3.2.2 Increased circuit complexity

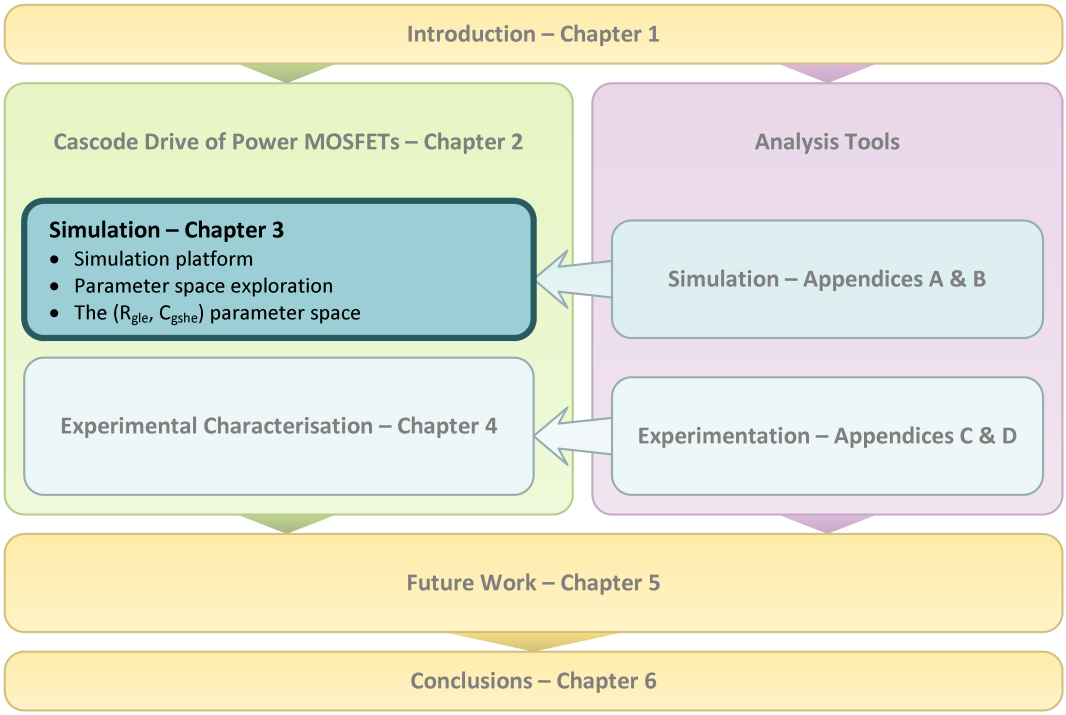
The proposed topology features two additional active devices (the cascode and clamp MOSFETs), and depending on the implementation, potentially an additional gate-drive supply voltage. The gate drive supply for the high-voltage MOSFET must also be capable of both sinking and sourcing current. As a result the gate drive footprint area may also be increased.

Increased circuit complexity is not of major concern given that the devices required to implement the proposed cascode topology are all low-voltage and typically available in space-optimised leadless packages. Highly integrated solutions are also available (low-voltage MOSFET half-bridges, with or without incorporated driver) allowing the proposed topology to be potentially implemented with a single additional IC.

Chapter 3

Simulation of the cascode gate drive of power MOSFETs

This chapter presents the platform and methodology used for simulation of the cascode gate drive of power MOSFETs. An exploration is conducted via simulation to determine candidate parameters for control of the switching performance of power MOSFETs under cascode gate drive. The cascode MOSFET gate resistance, high-voltage MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space is subsequently identified as a candidate for further investigation. A detailed analysis of this parameter space is performed and findings presented.



3.1 Introduction

Simulation is used in this work to explore the operating characteristics of the proposed cascode gate drive. Limitations of the simulation platform are explicitly acknowledged: specifically, the shortcomings of the available MOSFET models and limited ability to accurately capture circuit parasitics present in the practical circuit. Rather than attempting to address these issues via introducing substantial additional complexity to the simulation circuit, this work instead accepts that the behaviour of the simulated circuit will be of limited accuracy, but can instead be used as an effective tool for exploring the characteristic behaviour of the cascode gate drive over a broad parameter space. Findings based on the simulation work can then be validated by experimental characterisation of a prototype.

Discussed in this chapter is the simulation platform and methodology used to explore the performance of the cascode gate drive of power MOSFETs. Comparisons between conventional and cascode gate drive switching waveforms are provided as an aid in understanding the fundamental difference in the switching process and underlying mechanisms. Simulation is then used to explore the available parameter space for controlling the switching process of the proposed cascode gate drive topology. Candidate parameter spaces for switching performance optimisation are identified, and subsequently a detailed analysis is performed.

3.2 Modelling

A summary of the modelling decisions underpinning the simulation work in this thesis are presented below. Forward references are provided where more detailed explanation or justification of the modelling decisions is warranted.

1. The high-voltage MOSFET (IPL60R199CP) is modelled using the manufacturer published level-1 model [55].
2. The cascode MOSFET (CSD86350Q5D, “Sync” MOSFET) is modelled using an LTspice VDMOS model extracted from characteristics available in the manufacturer published datasheet.

   Semiconductor device model availability and selection is discussed in Section 3.3.2. Models were selected to correspond to devices used in the experimental prototype; device selection rationale is provided in Section 4.2.1.

3. The clamp MOSFET is not modelled (replaced by an idealised diode).

   The clamp MOSFET plays no role in the turn-on process when held off. It can be approximated as a diode connected from source-gate of the high-voltage power MOSFET (representing the intrinsic body-diode of the clamp

MOSFET). A discussion of the role of the clamp MOSFET in the turn-off process is provided in Section 3.5.

4. All other circuit elements are modelled as ideal. Parasitic package and layout inductances are not modelled.

   Detailed discussion and justification for this methodology are provided in Sections 3.1 & 3.3.4.

3.3 The simulation platform

3.3.1 Simulation package

LTspice IV was selected as the circuit simulation package of choice. LTspice is made freely available by Linear Technology and provides a SPICE simulator with schematic capture and waveform viewer. The salient feature of this package is the inclusion of a vertical double diffused power MOSFET (VDMOS) model. The LTspice VDMOS model is based on the level-1 monolithic MOSFET model with a number of modifications, particularly, the inclusion of an empirical function to model the non-linear gate-drain capacitance as a function of drain-source voltage. The VDMOS element allows simplified extraction of device models from datasheet parameters, reduced simulation time and more reliable convergence compared with MOSFET models based on complex subcircuits. A more detailed discussion of the LTspice VDMOS model is provided in Appendix A.

3.3.2 Device models

There are two major sources of device models: manufacturer published models and models developed by the user. Manufacturer published models typically use complex subcircuits to achieve well-matched behaviour of the model compared with the physical semiconductor device. Depending on the complexity of the model, this may lead to extended simulation times or, potentially, problems with convergence of the simulation. Semiconductor models published by device manufacturers also vary greatly in quality – users should always validate the performance of the model before use.

Additionally, manufacturers may encrypt their published device models for the purposes of protecting their Intellectual Property. Typically this has the consequence of locking the model to use with the simulation package with which it was developed.

Alternatively, users may implement their own models for devices using standard SPICE component models (or extensions available in the simulation pack-

age). At design time, most users will only have access to manufacturer published datasheets – the ability to implement models is then highly dependent on the quantity and quality of information available on the datasheet. Users may be able to augment datasheet characteristics via experimental characterisation, however this typically requires access to physical devices and specialised testing equipment.

As part of this work, methodologies for extracting semiconductor device models from information available on manufacturer published datasheets are developed and presented in Appendix A. Examples are provided which describe the extraction process and resulting models for the three key power semiconductors used in the simulation and experimental work that forms the basis of this thesis.

In this work a combination of manufacturer published and user-developed device models are utilised. For the high-voltage power MOSFET used in this work (Infineon IPL60R199CP [56]) the manufacturer published level-1 model is used [55]. This model showed good performance compared with the quoted datasheet characteristics, and, while there was a substantial overhead in simulation time due to the complexity of the model, simulation times were acceptable given the improved accuracy of the model (compared with a model for this device extracted from datasheet information, see Appendix A).

For the low-voltage power MOSFET used as the cascode MOSFET in this work (Texas Instruments CSD86350Q5D, "Sync" MOSFET [57]) the manufacturer published model was encrypted, and was unable to be used with LTspice. The performance of this model could, therefore, not be assessed. For this device, then, a simulation model was developed based on the characteristic data available in the published datasheet. The modelling process for this device is presented in Appendix A.

Finally, a SiC Schottky diode (Infineon IDD12SG60C [58]) was also required for use in simulation. Again, Infineon publishes a SPICE model for this device [59]. When the performance of this model was assessed (using the test circuits documented in Appendix B) excellent matching between the model and the characteristics published in the datasheet were observed. When operated in a clamped inductive switching configuration (switching opposing the IPL60R199CP MOSFET), however, the diode model prevented the simulation from converging. As an alternative, a model for the diode was extracted from the datasheet parameters, as described in Appendix A. This model exhibited comparable performance to the Infineon model, excluding a slight difference in the junction capacitance ($< 25\,\text{pF}$) for reverse voltages above 100 V, but allowed simulations to converge reliably, with no appreciable increase to the simulation time.

3.3.3 Performance metrics

A number of performance metrics are used to assess the simulation results obtained in this chapter. Outlined below is a brief description of each of these performance metrics including definition, measurement method and significance.

3.3.3.1 Total switching time

Total switching time for a turn-on transition is defined as the time from 10 % rise in drain current of the high-voltage MOSFET (using the load current as the 100 % reference value) to the fall in drain-source voltage to 10 % (using the bus voltage as the 100 % reference value) and is measured in seconds. The rise and fall of current and voltage respectively are reversed for measurements of a turn-off transition. Assuming voltage and current transitions remain relatively linear, switching losses are proportional to the total switching time. The total switching time also limits the maximum duty cycle that is achievable (due to the finite time required for a switching transition). In simulation this parameter can be measured programmatically using a measurement statement similar to the following:

```
.MEAS TRAN t_sw PP time
+ TRIG Id(MH) VAL=0.1*IL RISE=1
+ TARG V(DH) VAL=0.1*V(BUS) FALL=1
```

3.3.3.2 Switching loss

Switching loss is defined as the energy dissipated by the series combination of high-voltage and cascode power MOSFETs as seen from the drain-source terminals. For the cascode drive the voltage of interest is from the drain terminal of the high-voltage MOSFET to the source terminal of the cascode MOSFET and the current of interest is the drain current of the high-voltage MOSFET. The switching loss is calculated by taking the product of the drain-source voltage and drain-current and integrating over the turn-on (or turn-off) transition. The switching loss is measured in Joules. For simulations where the total switching time is of the same order of magnitude as the total simulation time the integration may be performed over the total simulation interval as the contribution of conduction and other losses to the calculated switching loss over this time scale will be negligible. In simulation this parameter can be measured programmatically using a measurement statement similar to the following:

```
.MEAS TRAN e_loss INTEG V(DH)*Id(MH)
```

3.3.3.3 Rise time

Rise time of voltage or current is defined as the time in which the measured quantity transitions from 10 % to 90 % of the steady state value. For voltage transitions the steady state value will be the bus voltage and for current transitions the steady state value will be the load (inductor) current. The rise time is proportional to the average rate of change of current or voltage during the transition. In simulation this parameter can be measured programmatically using a measurement statement similar to the following:

```
.MEAS TRAN t_rise PP time
+ TRIG Id(MH) VAL=0.1*IL RISE=1
+ TARG Id(MH) VAL=0.9*IL RISE=1
```

3.3.3.4 Fall time

Fall time of voltage or current is defined as the time in which the measured quantity transitions from 90 % to 10 % of the steady state value. For voltage transitions the steady state value will be the bus voltage and for current transitions the steady state value will be the load (inductor) current. The rise time is proportional to the average rate of change of current or voltage during the transition. In simulation this parameter can be measured programmatically using a measurement statement similar to the following:

```
.MEAS TRAN t_fall PP time
+ TRIG V(DH) VAL=0.9*V(BUS) FALL=1
+ TARG V(DH) VAL=0.1*V(BUS) FALL=1
```

3.3.3.5 Maximum di/dt

Maximum di/dt is defined as the maximum rate of change of current during a switching transition. Higher di/dt typically results in higher peak currents being carried by the switching device due to either reverse recovery of the opposing device in the bridge, or the higher rate of discharge of parasitic capacitances. High di/dt is also a source of EMI.

In simulation an auxiliary circuit is used to calculate the di/dt. A behavioural voltage source is used as a current-to-voltage converter, connected in parallel with a capacitor, which is used as a differentiator. The capacitor can be sized to provide an appropriate gain for the magnitudes of di/dt expected. The current through the capacitor, which is proportional to the di/dt, is measured. The following LTspice listing shows an example circuit used for this purpose:

```
Bdi DI 0 V=Id(MH)       ; I-to-V
Cdi DI 0 1n             ; Differentiation
```

A capacitance of 1 nF is selected; 1 A of current measured through the capacitor corresponds to 1 A/ns of di/dt. The maximum di/dt can be measured programmatically using a measurement statement similar to the following:

```
.MEAS TRAN didt_max MAX I(Cdi)
```

3.3.3.6 Maximum dv/dt

Maximum dv/dt is defined as the maximum rate of change of voltage during a switching transition. High dv/dt can result in unwanted turn-on of the opposing device in the half-bridge due to currents injected into the gate through parasitic capacitances. High dv/dt is also a source of EMI.

In simulation an auxiliary circuit is used to calculate the dv/dt. A behavioural current source is used as a voltage-to-current converter, connected in parallel with a inductor, which is used as a differentiator. The inductor can be sized to provide an appropriate gain for the magnitudes of dv/dt expected. The voltage across the inductor, which is proportional to the dv/dt, is measured. The following LTspice listing shows an example circuit used for this purpose:

```
Bdv 0 DV I=V(DH)        ; V-to-I
Ldv DV 0 1n Rser=0      ; Differentiation
```

An inductance of 1 nH is selected; 1 V measured across the inductor corresponds to 1 V/ns of dv/dt. The maximum dv/dt can be measured programmatically using a measurement statement similar to the following:

```
.MEAS TRAN dvdt_max MIN V(DV)
```

Note the use of the `MIN` measurement type; for a turn-on transition the voltage falls and therefore the dv/dt is negative. The maximum dv/dt is therefore given by the most negative value of dv/dt observed.

3.3.4 Layout and PCB parasitics

Practical implementation of a circuit introduces parasitic circuit elements. The PCB layout geometry and device packaging are the primary factors that contribute to these parasitics. In switching circuits, parasitic inductances tend to have the greatest impact on the performance of this circuit, with high transient voltages developed across these parasitic elements during periods of high rate-of-change of current. Parasitic capacitances may also lead to high transient currents

in the presence of fast voltage transients, however, parasitic capacitances are typically easier to eliminate by careful design.

Parasitic inductances are dependent on the geometry of the current paths in the circuit. Loop inductances can be estimated based on circuit geometries, however, in the case of complex multi-node circuits where there are multiple critical current loops with shared segments (such as in the case of the cascode drive configuration), loop inductances are not sufficient. Instead the loop inductance(s) should be decomposed into a number of partial inductances placed in the appropriate current segments. Using the proposed cascode circuit as an example, while there are only three critical current loops involved in the turn-on process there are over ten unique parasitic partial inductances that could contribute to the performance of the circuit.

Partial inductances are far more difficult to estimate compared with loop inductances, particularly in the context of PCBs layouts using wide, thin traces where the current paths are not only dependent on the copper geometry but are also frequency dependent. Additionally every current path segment potentially contributes to the partial inductance of every other segment.

Considering the aforementioned factors, the simulations in the following sections intentionally exclude the presence of PCB and device package parasitic inductances. The rational for this decision is summarised by the following points:

1. Parasitic inductances are a function of the physical implementation of the circuit, not the circuit topology. Simulation of the circuit excluding these parasitics provides an implementation-independent analysis of the topology.

2. While it may be possible to estimate typical loop inductances, the decomposition of these loop inductances into partial inductances would be a largely arbitrary decision which may not be a good representation of reality.

Instead a detailed experimental characterisation of a hardware prototype is conducted and presented in Chapter 4. By performing an experimental characterisation any effect of parasitic inductance will be captured in the results, allowing the results obtained by simulation to be validated. Additionally, a methodology for the extraction of partial PCB inductances at the design phase for informing SPICE simulations is proposed in Section 5.4 as an area of future work.

3.4 Gate drive topologies

The conventional resistor-fed gate drive is well documented and understood in the literature [1, 8]. Switching waveforms for the conventional driver presented in the literature, however, are typically idealised or simplified in some fashion to aid in the understanding of the switching process and mechanisms. The cascode switching process, while broadly understood in the literature [1], is not well documented, particularly in the context of the driving of power MOSFETs.

Presented in this section are a set of simulated switching waveforms for a power MOSFET driven by conventional and cascode gate drive configurations in a clamped inductive switching application. Waveforms are presented for three different opposing (high-side) devices: an ideal diode, a Schottky diode and a soft, ultrafast-recovery diode. These typical waveforms will be used to describe the typical features which can be observed in the switching waveforms. Finally, a comparison of the turn-on waveforms for the conventional and cascode drive configurations is presented, matched for equivalent turn-on losses.

3.4.1 Conventional resistor-fed gate drive

Figure 3.1 below shows the simulation circuit used to generate the typical waveforms for the conventional resistor-fed gate drive topology. A pulsed voltage source (V1) applies the drive voltage to the high-voltage power MOSFET (M1) through gate resistance (R1) at $t = 0$. The bus voltage is supplied by voltage source V2 and the load current is supplied by current source I1. D1 is the high-side clamping diode which circulates the load current during the MOSFET off period.

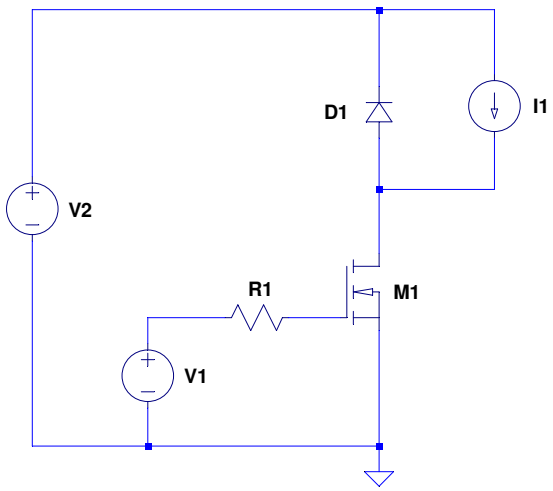


Figure 3.1: Circuit used to simulate the typical waveforms for the conventional gate drive topology.

3.4.1.1 Typical waveforms

The typical waveform simulations are performed with a bus voltage and load current of 400 V and 10 A respectively. The drive voltage for the high-voltage MOSFET is set to 12 V and the gate resistance is set to 100 Ω. The level-1 MOSFET model for the IPL60R199CP power MOSFET published by Infineon Technologies was again used for MH1 [55]. Transient waveforms were generated for three different diode models for D1: an ideal diode model, a model of the IDD12SG60C SiC Schottky diode (extracted from the datasheet parameters, see Appendix A) and a generic model for a soft, ultrafast-recovery silicon power diode.

Transient waveforms are presented on four sets of axes (see Fig. 3.2). The top pair of plots shows the full switching period from application of the gate-drive voltage to full enhancement of the MOSFET gate over a period of 1.4 µs. The bottom pair of plots is a time scaled version of the top plots showing only the 150 ns interval over which the load current and voltage transition. The upper plot in each pair shows the gate-source voltage of the MOSFET and the lower plot in each pair shows the drain current and drain source voltage. Traces numbered 1, 2 and 3 refer to the ideal, Schottky and soft recovery diode simulations respectively.

The first waveform feature of note is the characteristic shape of the gate-source voltage. An exponential charging curve is observed from time zero, through the threshold voltage up to the point where the drain-source voltage begins to transition. The Miller plateau is observed coincident with the fall of drain-source voltage and extending for around 120 ns to 150 ns. Following the Miller plateau the gate continues charging towards the drive voltage of 12 V, again following an exponential charging curve.

Note that the majority of the fall in drain-source voltage occurs at the beginning of the Miller plateau; the majority of the Miller plateau corresponds to only a relatively small additional decrease in the drain-source voltage (around 20 V, or 5 %, of the bus voltage). From the end of the Miller plateau to full enhancement the drain-source voltage decreases from 2.51 V to 1.75 V (a 30 % decrease) as the gate charges, however, the majority of this decrease occurs within the first 200 ns.

Consider now the interval over which the transition in drain current and drain-source voltage occurs. The MOSFET begins to conduct appreciable current for gate-source voltages above 3.6 V. The voltage of the Miller plateau corresponds to the gate voltage required for the MOSFET to conduct the full load current (in the active region). Note, however, that for all cases the gate voltage increase to approximately 5.7 V before the 10 A load current is fully supported by the MOSFET. This overshoot can be attributed to the additional internal impedances

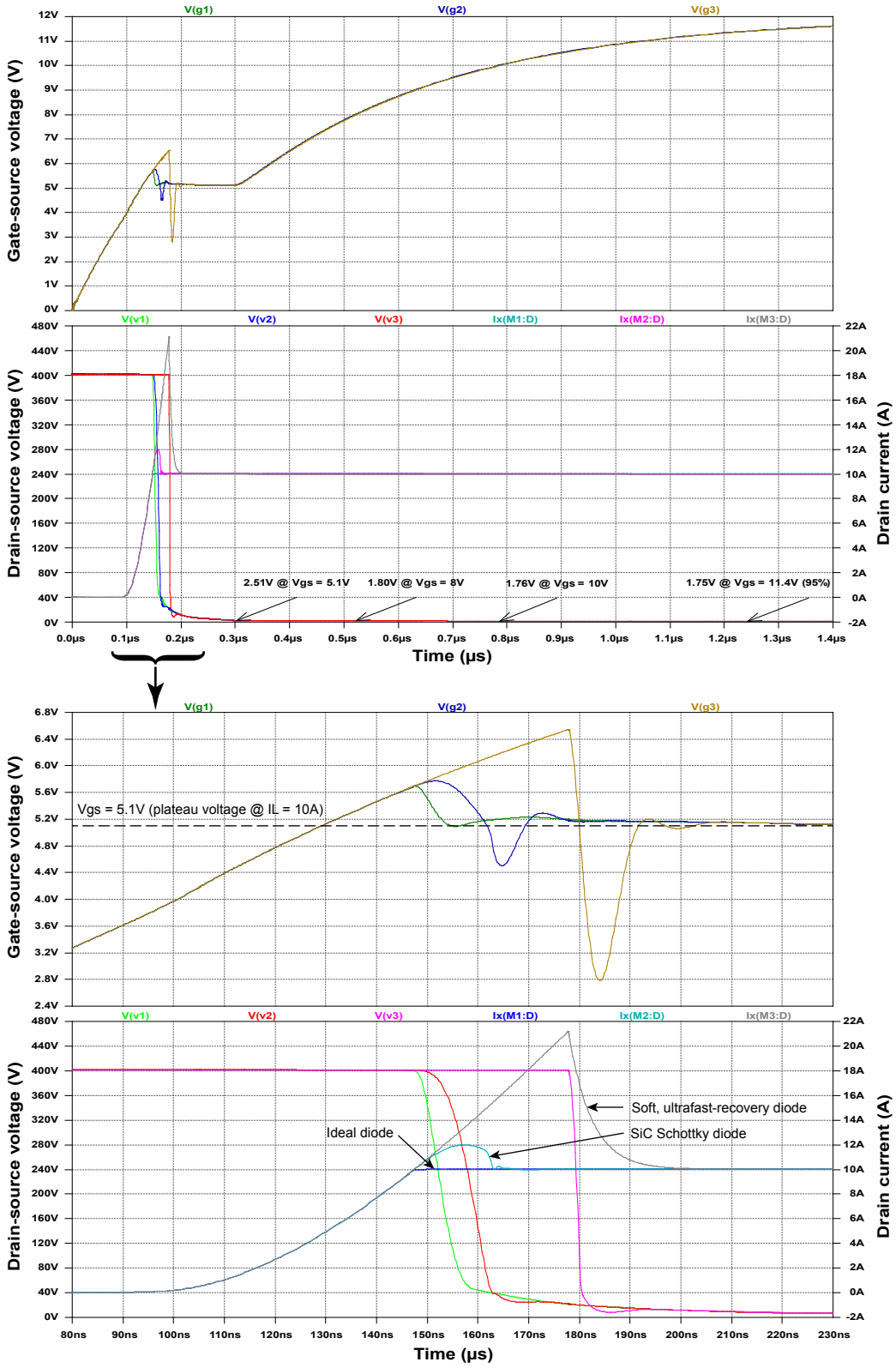


Figure 3.2: Typical turn-on transient waveforms for a conventional gate-drive in a clamped inductive switching application. Traces are provided for three diodes with different characteristics: (1) an ideal diode, (2) a SiC Schottky diode and (3) a soft, ultra-fast recovery diode. Traces can be matched to their corresponding colour by the number indices in the title of each plot. The bottom pair of axes shows the interval of current and voltage transition in greater detail.

present in the level-1 Infineon MOSFET model.

In the ideal diode case, the drain-source voltage on the MOSFET begins to fall as soon as the load current is fully supported by the MOSFET, and the gate voltage recovers to the Miller plateau voltage. For the Schottky diode case the drain-source voltage also begins to fall as soon as the load current is fully supported by the MOSFET, however, the drain current also increases beyond the load current. This additional current is the current required to charge the junction capacitance of the Schottky diode. Consequently, the gate-source voltage is also higher during this interval to support the additional current.

In the case of the soft recovery diode substantial additional current is conducted by the MOSFET before the drain-source voltage of the MOSFET begins to fall. This is the reverse recovery current of the soft recovery diode, which is required to sweep the minority carriers out of the junction before the diode is capable of reverse blocking. The reverse current peaks at approximately 21 A, just over double the load current. To support this additional current the gate-source voltage must also increase; as is shown, the gate-source voltage approaches 6.6 V during the peak current conduction.

Once the full load current plus the peak reverse recovery current of the soft-recovery diode is supported by the MOSFET, the drain-source voltage transitions. Note that the rate-of-change of voltage for the soft-recovery case is significantly higher than that of either the ideal diode or Schottky diode cases. This is due to the change in operating point at which the voltage transition occurs; in the soft recovery case the MOSFET is supporting 21 A of load current at the time at which the drain-source voltage begins to transition, compared with 10 A in the other cases. Up to 11 A of excess current is then available to discharge the drain-source capacitance of the MOSFET compared with the other cases, resulting in significantly higher $\mathrm{d}v/\mathrm{dt}$. This effect is somewhat mitigated by the soft-recovery characteristic of the diode; only a portion of the 11 A excess current is available during the high-$\mathrm{d}v/\mathrm{dt}$ portion of the transition. It should be noted, however, that a diode with a snappy recovery (such as the body diode of the modelled MOSFET) would exacerbate the situation.

3.4.2 Cascode gate drive

Figure 3.3 below shows the simulation circuit used to generate the typical waveforms for the cascode gate drive topology. A pulsed voltage source (V1) applies the drive voltage to the cascode MOSFET (ML1) through gate resistance (R1) at $t = 0$. Voltage source V2 is the gate drive supply for the high-voltage MOSFET (MH1). The bus voltage is supplied by voltage source V3 and the load current is supplied by current source I1. D1 is the high-side clamping diode which circulates the load current during the MOSFET off period. Diode D2 clamps the source voltage of the high-voltage MOSFET to the drive voltage during the off period.

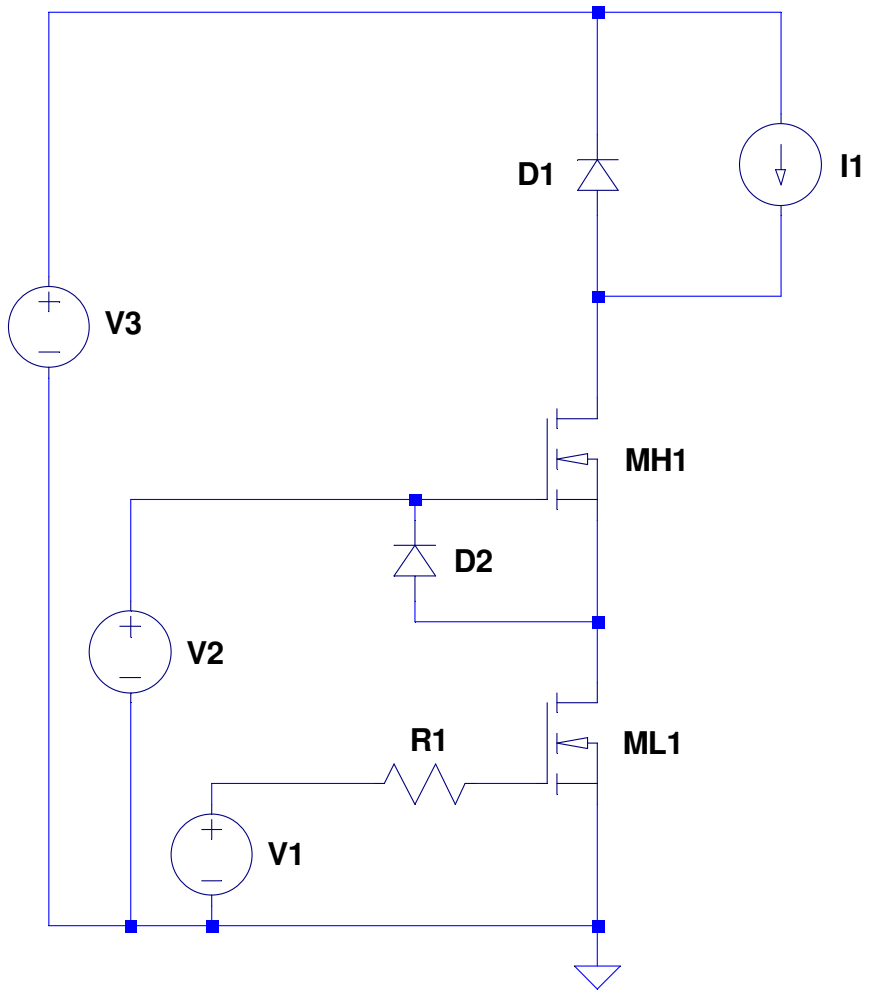


Figure 3.3: Circuit used to simulate the typical waveforms for the cascode gate drive topology.

3.4.2.1 Typical waveforms

The typical waveform simulations are performed with a bus voltage and load current of 400 V and 10 A respectively. The drive voltage for the high-voltage MOSFET is set to 12 V and the drive voltage for the cascode MOSFET is set to 5 V. The gate resistance of the cascode MOSFET is set to 220 Ω. The level-1 MOSFET model for the IPL60R199CP power MOSFET published by Infineon Technologies was used for M1. Transient waveforms were generated for three different diode models for D1: an ideal diode model, a model of the IDD12SG60C SiC Schottky diode (extracted from the datasheet parameters, see Appendix A) and a generic model for a soft, ultrafast-recovery silicon power diode.

Transient waveforms are presented on four sets of axes (see Fig. 3.4), as before. The top pair of plots shows the full switching period from application of the gate-drive voltage to full enhancement of the MOSFET gate over a period of 1.4 µs. The bottom pair of plots is a scaled version of the top plots showing only the 150 ns interval over which the load current and voltage transition. The upper plot in each pair shows the gate-source voltages of the MOSFETs (only the high-voltage MOSFET gate-source voltage is shown in the scaled plot) and the lower plot in each pair shows the drain current and drain source voltage. Traces numbered 1, 2 and 3 refer to the ideal, Schottky and soft recovery diode simulations respectively.

Inspecting firstly the gate-source voltage of the cascode MOSFET, the waveform shape is comparable with that of a conventional resistor-fed gate drive. This is expected given that the cascode MOSFET is driven in a conventional manner. A Miller plateau is clearly visible between 300 ns to 400 ns corresponding to the rise in gate-source voltage on the high voltage MOSFET (which is a fall in drain-source voltage on the cascode MOSFET). A very slight flattening of the charging curve of the cascode gate source voltage can also be observed at approximately 225 ns, however, the Miller effect at this point is far less pronounced.

The gate-source voltage waveform of the high-voltage MOSFET is distinctly different to that observed for a conventional resistor-fed gate drive. A fast rise to the threshold voltage over approximately 50 ns is observed. It should be noted that in the off state the gate-source voltage is held slightly negative due to the forward voltage drop of the clamping diode. At approximately 4 V gate-source voltage the high-voltage MOSFET begins conducting. As the high-voltage MOSFET begins conducting the gradient of the high-voltage MOSFET gate-source voltage waveform decreases. This is due to the requirement of the cascode MOSFET to also conduct the load current; consequently less current is available to charge the gate of the high-voltage MOSFET.

Note that no Miller plateau is evident in the gate-source waveform of the

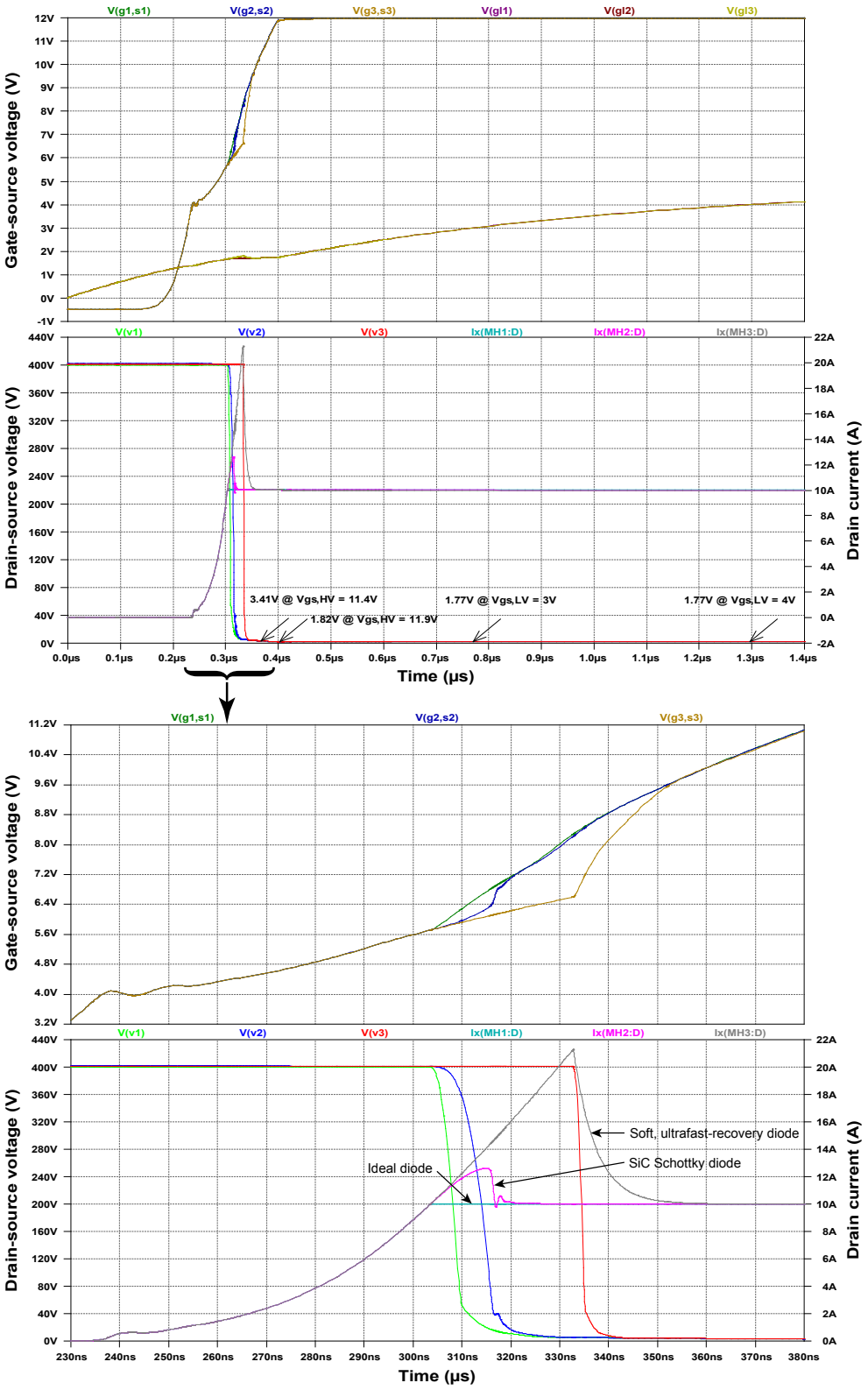


Figure 3.4: Typical turn-on transient waveforms for a cascode gate drive in a clamped inductive switching application. Traces are provided for three diodes with different characteristics: (1) an ideal diode, (2) a SiC Schottky diode and (3) a soft, ultra-fast recovery diode. Traces can be matched to their corresponding colour by the number indices in the title of each plot. The bottom pair of axes shows the interval of current and voltage transition in greater detail.

high-voltage MOSFET. The Miller plateau would typically be evident from the beginning of the drain-source voltage transition (approximately 300 ns). It can be seen that instead the gate of the high-voltage MOSFET continues to charge. The gate of the high-voltage MOSFET in fact reaches 95 % state of charge (11.4 V) less than 75 ns after the beginning of the drain-source voltage transition, compared with approximately 1.1 µs in the case of the resistor-fed gate drive.

The minimum on-state voltage is slightly higher for the cascode drive, 1.77 V compared with 1.75 V for the conventional driver. This is expected given the additional series resistance of the cascode MOSFET. It should be noted, however, that the minimum on-state voltage is reached much more quickly in the case of the cascode driver: less than 100 ns to 1.82 V compared with less than 500 ns to 1.80 V for the conventional drive topology.

Now considering the scaled plots, at approximately 305 ns the load current is fully supported by the high-voltage and cascode MOSFETs for the ideal and Schottky diode cases, and the drain-source voltage on the high-voltage MOSFET begins to transition. It should be noted that no Miller plateau is evident in the gate-source voltage waveform for the high-voltage MOSFET. Instead the gate-source voltage of the high-voltage MOSFET increases as excess current delivered by the cascode MOSFET continues to charge the gate during the drain-source voltage transition. Consequently an increase in the $\mathrm{d}v/\mathrm{dt}$ can be observed over the first 50 ns to 100 ns of the drain-source voltage transition.

In the case of the soft recovery diode the gate of the high-voltage MOSFET continues to charge (to approximately 6.6 V) until the load and reverse recovery currents are fully supported. After the peak reverse recovery current has been reached the drain source voltage transition occurs. As with the conventional gate drive, it should be noted that the $\mathrm{d}v/\mathrm{dt}$ is increased in the soft recovery case due to the different operating point at the instant of the drain-source voltage transition.

3.4.3 Comparison of conventional and cascode gate drives

To enable comparison of the typical waveforms of the conventional and cascode gate drive topologies, typical waveforms for the tun-on interval of both topologies are plotted on the same axes (see Fig. 3.5). Switching speeds were matched by setting the cascode MOSFET gate resistance to 220 Ω and adjusting the gate resistance in the conventional drive to provide comparable total turn-on switching losses. The turn-on instant was adjusted such that the transition in drain-source voltage of the high-voltage MOSFETs in both configurations occurred at the same instant. The Schottky diode model was chosen for these simulations.

Simulation results are plotted over three axes; from top to bottom: high-voltage MOSFET gate-source voltages, high-voltage MOSFET drain-source voltages and drain currents and finally, switching losses. It is worth noting from the drain-source voltage and drain current traces presented in Figure 3.5 that for the bulk of the switching transition the transient waveforms are closely matched; differences are apparent primarily at the leading and trailing ends of the switching transient. We consider then in detail the differences between the switching transients.

The first appreciable drain current is conducted once the gate reaches the threshold voltage of approximately 3.5 V. The cascode configuration drives the gate to this voltage more quickly. If we consider the interval bounded by $V_{gs} = (0\,\mathrm{V}, 3.5\,\mathrm{V})$ we can observe that the cascode configuration exhibits a reduced turn-on delay compared with the conventional gate drive – approximately 55 ns compared with 95 ns. Inspecting the gate-source waveforms at the instant of turn-on, however, it can be seen that the gate-source voltage gradient is comparably lower for the cascode configuration, resulting in a reduced $\mathrm{d}i/\mathrm{dt}$, as shown in the drain-source waveforms, particularly for the interval from 135 ns to 160 ns. This leads to increased switching losses for the cascode drive configuration in the leading edge.

During the transition of the drain-source voltage to approximately 50 V both the current and voltage transients are well matched. Below $V_{ds} = 50\,\mathrm{V}$ the cascode configuration results in a faster transition of the drain-source voltage to its minimum value, with a corresponding increase in the drain current during this period. For the conventional drive the time to reduce the drain-source voltage to its minimum value is significant, leading to appreciably higher switching losses for the interval from 220 ns to 360 ns. It should be noted that this interval corresponds to the Miller plateau interval evident in the gate voltage traces.

It can also be seen from the gate-source voltage traces that the cascode configuration leads to a significantly reduced time to full enhancement, with the gate

fully charged while the conventional drive has only partially traversed the Miller plateau region.

In both cases the total switching loss energy was just over 140 µJ (as a result of matching the switching speeds). The increased losses of the cascode configuration in the leading edge are offset by the increased losses of the conventional drive in the tail. This result indicates there is potentially an opportunity to reduce the switching loss for the cascode configuration by increasing the di/dt at the leading edge – without increasing the maximum di/dt for the switching transition.

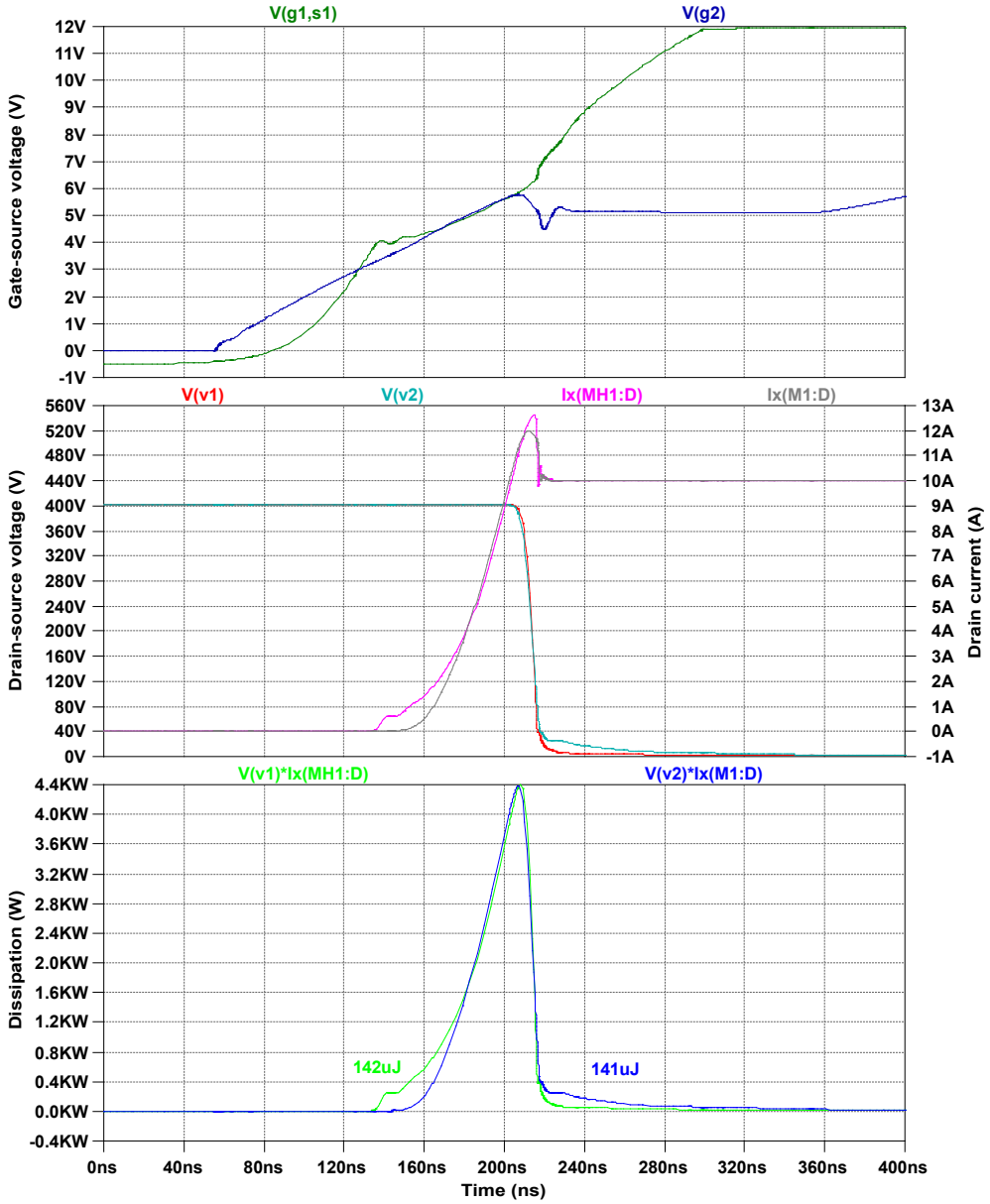


Figure 3.5: Comparison of typical turn-on transient waveforms for cascode and conventional gate drives in a clamped inductive switching application with a high-side SiC Schottky diode. Turn-on speeds are matched for equivalent total turn-on losses.

3.5 Turn-off switching characteristics

As discussed in Section 2.2.1, the detailed analysis of the turn-off process for the cascode gate drive topology is not the primary focus of this work. In this section, however, the switching characteristics of the two primary turn-off modes, namely natural and active-clamped turn-off, are identified and discussed. Of particular significance is the load-dependent nature of the turn-off process, and the effect of the active gate clamp on the switching process. Specifically, it is demonstrated that the high-voltage MOSFET drain-source switching characteristics are insensitive to the gate-source discharge profile, as the turn-off process is dominated by the interaction of load current with parasitic capacitances.

3.5.1 Simulation circuit

To investigate the turn-off process, the simulation circuit is adjusted as shown in Figure 3.6 to include the clamp MOSFET, denoted MCL. For the natural turn-off case the clamp MOSFET is held off by shorting its gate and source terminals, and can essentially be treated as a diode connected from source-drain of the high-voltage MOSFET (e.g D2 in Figure 3.3, the simulation circuit used for the turn-on process). For the purposes of this demonstration the same MOSFET model used for the cascode MOSFET (MCA) is used for the clamp MOSFET; note that in the experimental work presented in Section 4.5.4 the clamp MOSFET is a different low-voltage device and therefore has slightly different characteristics.

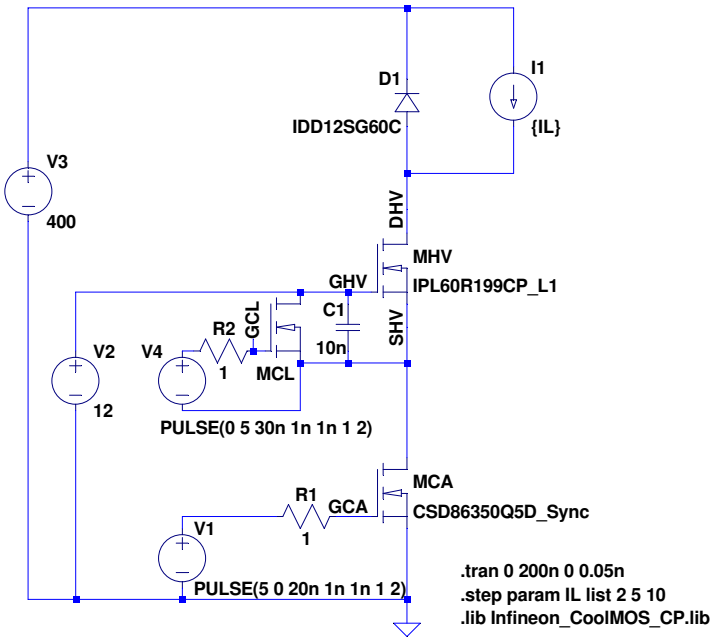


Figure 3.6: Circuit used to simulate the turn-off waveforms for the cascode gate drive topology.

3.5.2 Natural turn-off

In the natural turn-off case, the clamp MOSFET is held off, and turn-off is achieved by turning off the cascode MOSFET, interrupting the flow of load current and forcing the discharge of the high-voltage MOSFET gate. The turn-off process is then largely driven by the load current. The simulated natural turn-off process is illustrated in Figure 3.7 for three different load currents.

In the top plot of Figure 3.7, it can be seen that as the cascode MOSFET is turned-off, the gate-source voltage of the high-voltage MOSFET begins to decrease (as current commutates out of the channel on the cascode MOSFET to instead discharge the gate-source capacitance of the high-voltage MOSFET). As the load current is constant during the switching transition, and the gate-source capacitance remains almost constant, the drain-source voltage transition will be largely linear, with a gradient proportional to the load current. This effect can be clearly seen in Figure 3.7, with the gate-source voltage discharge time increasing with decreasing load current.

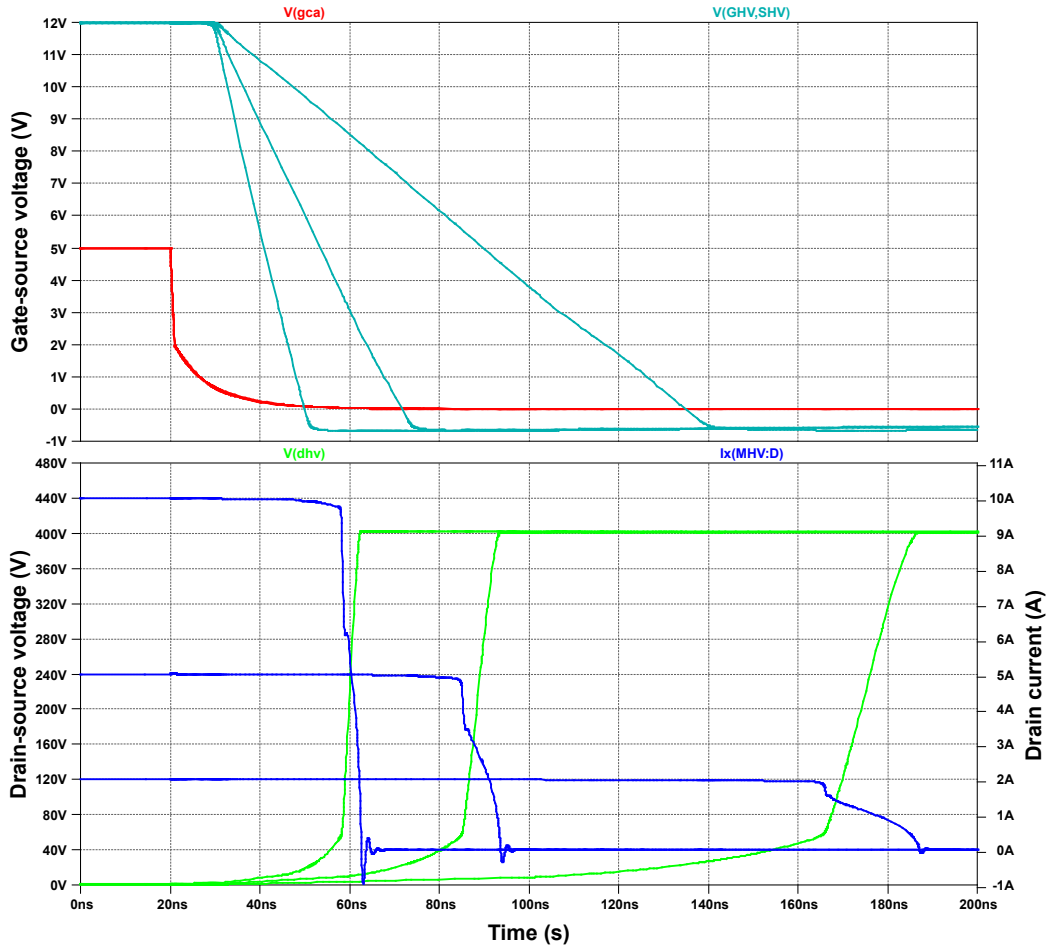


Figure 3.7: Simulated natural turn-off switching waveforms for the cascode gate drive topology operating with load currents of 2, 5 and 10 A.

Also note that the discharge profile of the cascode MOSFET gate plays practically no role in the high-voltage MOSFET drain-source turn-off characteristics. The turn-off process is dominated by the load current and parasitic capacitances. A fast turn-off circuit could be used to drive the cascode MOSFET instead of the 1 Ω gate resistor (e.g. an anti-parallel diode), to achieve faster turn-off of the cascode MOSFET with negligible impact to the natural turn-off process.

It is also worth noting that the discharge profile of the high-voltage MOSFET gate-source voltage also plays a limited roll in controlling the turn-off process. While the discharge rate of the gate does introduce turn-off delays, the bulk of the drain-source voltage transition, and the entirety of the drain current commutation occurs after the gate is fully discharged, and hence, are uncontrolled, driven solely by the load current.

3.5.3 Active-clamped turn-off

In the active-clamped turn-off case, following the turn-off the cascode MOSFET, the clamp MOSFET is driven on. This results in a fast discharge of the high-voltage MOSFET gate, independent of load conditions. Dead-time must be introduced between the drive signals of the cascode and clamp MOSFETs to avoid cross-conduction (shoot-through), which would discharge the high-voltage MOSFET gate drive supply. The simulated active-clamped turn-off process is illustrated in Figure 3.8 for three different load currents.

Comparing the waveforms in Figures 3.7 & 3.8 for the natural and active-clamped turn-off processes, the first major difference is in the discharge profile of the high-voltage MOSFET gate-source voltage. In the active-clamped case, a much faster discharge has been achieved, and the discharge time is independent of load current. In all cases the high-voltage MOSFET gate is fully discharged within 17 ns of the cascode MOSFET being driven off, and within 7 ns of the clamp MOSFET being driven on. Compare this with the natural turn-off case, where for the 2 A load case, 120 ns is required to fully discharge the gate.

The fast turn-off achieved through application of the clamp MOSFET substantially reduces the turn-off delay time compared with natural turn-off in all load cases. Note, however, that the high-voltage MOSFET drain-source turn-off characteristics are still load current dependent. This effect is highlighted in the active-clamped waveform as the drain-source waveforms are distinctly different in each load case, even though the high-voltage MOSFET gate-source voltage profiles are the same in all load cases.

Both the natural and active-clamped turn-off mechanisms for the cascode gate drive topology provide satisfactory switching performance. Importantly, in

both cases the high-voltage MOSFET drain-source turn-off switching characteristics are almost entirely decoupled from the discharge profile of the high-voltage MOSFET gate-source voltage. Instead, the turn-off process is dominated by the charge/discharge of parasitic capacitances by the load current.

The inclusion of the active-gate clamp provides some distinct advantages, however, in that fast discharge of the high-voltage MOSFET gate-source voltage can be achieved independent of load conditions. Consequently, turn-off switching delays can be greatly reduced. The clamp MOSFET provides the additional benefit of acting as a low-impedance gate clamp while the high-voltage MOSFET is held off.

The remainder of this work focuses on the optimisation of the cascode turn-on switching process, for which there is a direct relationship between the gate-drive and drain-source switching characteristics of the high-voltage MOSFET. The turn-off switching performance of the cascode gate-drive topology is, however, validated experimentally in Section 4.5.4.

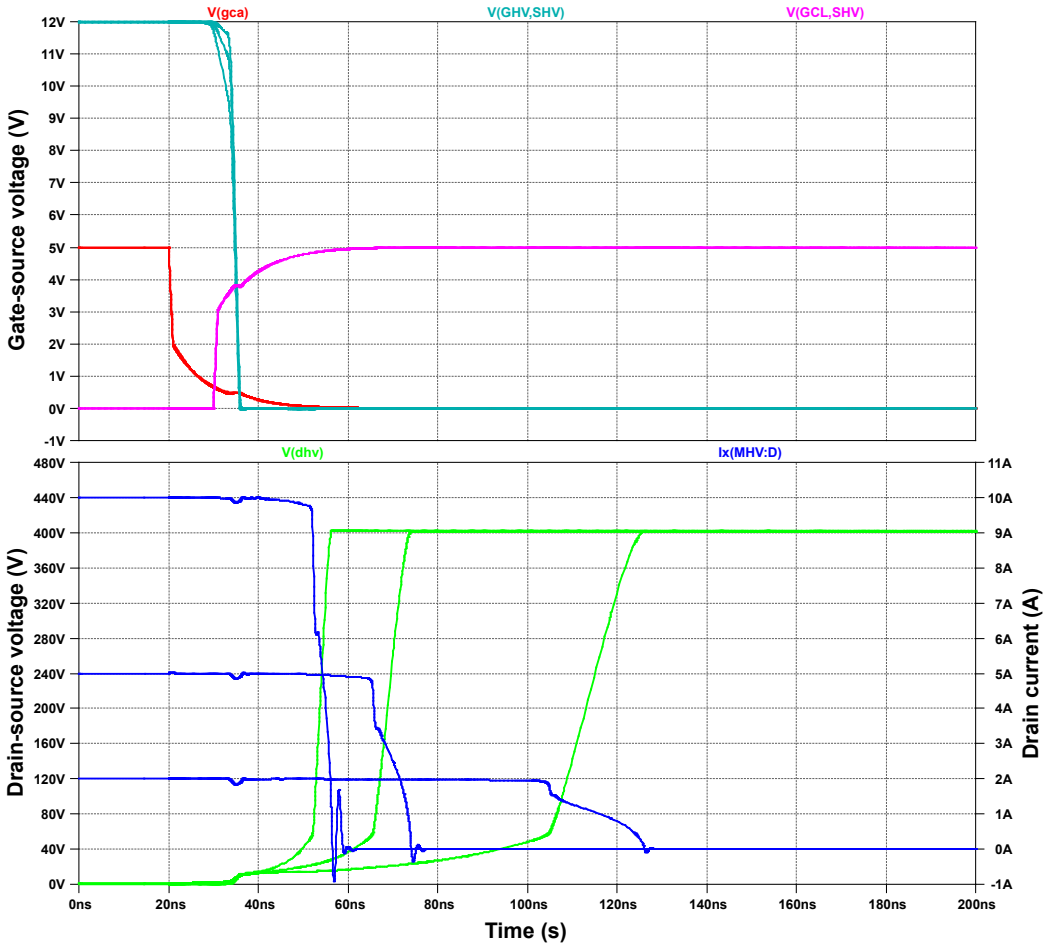


Figure 3.8: Simulated active-clamped turn-off switching waveforms for the cascode gate drive topology operating with load currents of 2, 5 and 10 A.

3.6 Exploration of the parameter space

3.6.1 Purpose & methodology

The cascode topology provides the opportunity to control the switching process via a number of controllable parameters. In most cases this involves the addition of external resistances of capacitances to the topology, but can also include the tuning of voltage supplies over a constrained range. This section aims to investigate the effect of these parameters on key switching performance metrics.

The primary control mechanism is the external gate resistance of the cascode MOSFET; this parameter can be considered to be considered to be continuously variable due to the availability of suitably rated resistors at practically any value. Other parameters that have been identified as potential mechanisms for controlling the switching process are given below in Table 3.1. External gate-drain capacitances were excluded from the parameter space for both the high-voltage and cascode MOSFETs due to the increased sensitivity to dv/dt induced turn-on that the addition of these capacitances would impose.

For the initial exploration of the parameters space, a 2D sweep is performed for each of the parameters identified in Table 3.1 against R_{gle}, the cascode MOSFET external gate resistance. Simulations are performed at a fixed load current for the initial investigation. Result surfaces are presented for three key performance metrics: average dv/dt, average di/dt and switching loss energy. This coarse parameter sweep is presented in Section 3.7 with all result surfaces presented in Appendix E.

Following this coarse investigation of the parameter space, the most promising candidate parameters are selected for a more detailed investigation, including analysis of the load current dependence and additional performance metrics. These details are presented in Section 3.8.

Parameter	Description	Min.	Max.	Default
R_{gle}	Cascode MOSFET external gate resistance	10 Ω	1 kΩ	N/A
R_{ghe}	HV MOSFET external gate resistance	0.1 Ω	1 kΩ	0 Ω
C_{gsle}	Cascode MOSFET external gate-source capacitance	100 pF	100 nF	0 pF
C_{gshe}	HV MOSFET external gate-source capacitance	1 nF	100 nF	0 pF
C_{dsle}	Cascode MOSFET external drain-source capacitance	1 nF	100 nF	0 pF
C_{dshe}	HV MOSFET external drain-source capacitance	1 pF	100 nF	0 pF
V_{drl}	Cascode MOSFET drive voltage	4 V	6 V	5 V
V_{drh}	HV MOSFET drive voltage	10 V	15 V	12 V

Table 3.1: Summary of the parameter space for the cascode topology.

3.6.2 Presentation of result surfaces

In exploring the parameter space, simulations are performed for sweeps of two independent variables. For each pair of values (the independent variables) the resulting performance metrics (listed in Section 3.3.3) are recorded. The result space is consequently a set of surfaces – one surface for each performance metric recorded. Often it is of interest to observe the corresponding changes of more than one performance metric as the parameter space is traversed. To accomplish this the result surfaces may be plotted as contours, allowing multiple performance metrics to be plotted simultaneously over the parameter space. Each contour line represents the path across the parameter space for which the corresponding performance metric is constant.

This method of visualisation is also particularly useful as a design tool. Limits of operation may be identified by the designer (for example, maximum allowable $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}i/\mathrm{dt}$) and masks applied to the result space with the aid of contour lines. Other performance metrics (for example, switching loss) may then be easily optimised visually by traversing the surface of the performance metric of interest within the allowable parameter space.

An example of such a plot is provided in Figure 3.9. The independent variables are plotted on the X and Y axes. These axes may be linearly or logarithmically scaled, typically depending on the range over which the independent variables were swept. Contours are plotted for each metric of interest. The legend indicates the performance metric and units for which each set of contours is plotted. If a plot is generated for a particular value of additional parameters (i.e. a constant value of other independent variables) then this value will be listed in the plot title.

Numbers on contour lines indicate the value of that contour. Not all contours may have their values explicitly stated, for readability. Contours will usually be uniformly spaced (in value), however, depending on the scale of the results space, contours may be instead logarithmically (or otherwise) spaced. In the case where not all contours are explicitly labelled with a value, then unlabelled contours will be uniformly distributed between contours for which values are defined.

Contour lines may be used to define boundaries of operation or as an aid in traversing the parameter and result spaces to achieve a particular result. Where contour lines are parallel to the vertical or horizontal axis it indicates that the performance metric in question is insensitive to changes in the parameter plotted on that axis (for a certain region in the parameter space). Where contours of different metrics run parallel it indicates that these metrics are tightly coupled and are difficult to control independently (when limited to the plotted parameter

space). Where contours of different metrics are orthogonal, these metrics can be independently controlled within the corresponding parameter space.

In certain cases it may be of interest to see the underlying transient simulation data for a certain point on the parameter space. In these cases the contour plot will be overlaid with indicators to show, for each transient simulation result, the corresponding location within the parameter space. These plots may also be annotated with arrows which indicate the trajectories that are followed when traversing the parameter and result spaces.

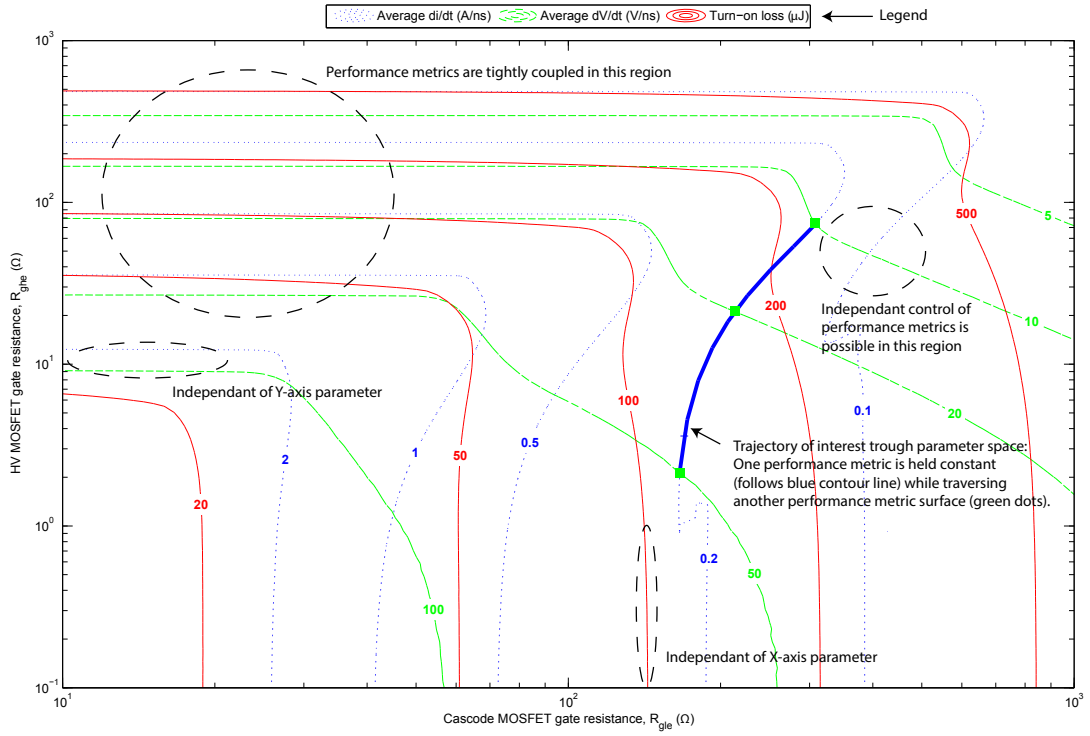


Figure 3.9: An example presentation of result surfaces generated from a 2D parameter sweep. Three performance metrics are plotted as indicated by the legend. Both axes are logarithmically scaled. The plot is annotated showing regions where the performance metrics are tightly coupled or where independent control of performance metrics is achievable. An example trajectory of interest is shown where the di/dt metric is held constant, following the 0.2 A/ns contour while the dv/dt metric surface is traversed from 50 V/ns to 20 V/ns.

3.6.3 Simulation circuit for parameter sweeps

The LTspice circuit used to conduct the parameter sweeps in the following sections is shown in Figure 3.10. The topology is that of the cascode drive configuration in a clamped inductive switching application. As only the turn-on process is of interest, an ideal diode is substituted in the place of the clamp MOSFET. Infineon's level-1 MOSFET model for the IPL60R199CP power MOSFET is used for the high-voltage MOSFET model [55], and the CSD86350Q5D "Sync" MOSFET model extracted from datasheet parameters [57], as described in Section A.4.2, is used for the cascode MOSFET model.

Component values have been substituted with SPICE parameters to allow the variables identified in Section 3.6, along with other circuit parameters such as the bus voltage and load current, to be controlled. SPICE parameters are modified programmatically via a MATLAB script to provide sweeps over the desired parameter spaces. Performance metrics are measured using the subcircuits and SPICE directives defined in Section 3.3.3. The aforementioned MATLAB script is used to collate the results of numerous transient simulation and to generate the corresponding result surfaces.

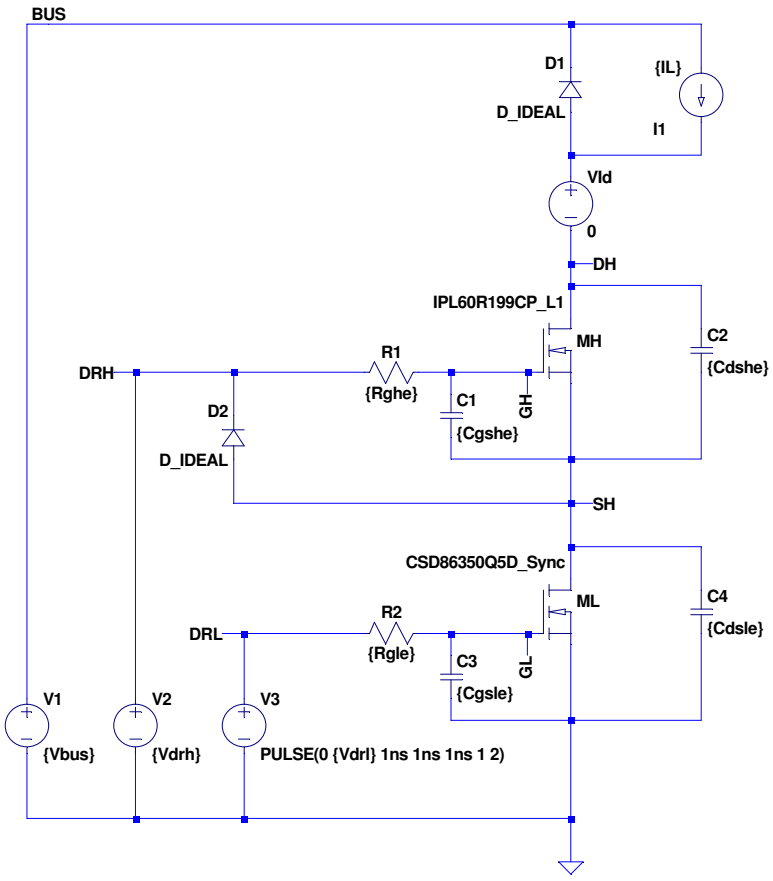


Figure 3.10: The LTspice simulation circuit used for the exploration of the parameter space.

3.7 Coarse parameter sweeps

Coarse parameter sweep were performed for the candidate parameters identified in the previous section. Three performance metrics were chosen to asses the suitability of each parameter space as a candidate for controlling the switching process of the cascode date drive topology: average di/dt, average dv/dt and turn-on loss. Turn-on loss was measured from the transient simulation directly as described in Section 3.3.3, average di/dt and dv/dt were calculated from the 10 % to 90 % current rise and voltage fall times respectively.

The seven result surfaces generated from these parameter sweeps are documented, along with a brief analysis and interpretation, in Appendix E. From a cursory analysis of the resulting surfaces it was possible to discard three of the parameter spaces, namely (R_{gle}, V_{drh}), (R_{gle}, V_{drl}) and (R_{gle}, C_{gsle}), as potential candidates for providing enhanced control of the switching process, due to the tightly coupled nature of the investigated performance metrics over these parameter spaces.

The result surfaces for the (R_{gle}, C_{dshe}) parameter space indicated that adding additional drain-source capacitance could be used as a method of achieving independent control of the di/dt and dv/dt performance metrics, but at the expense of significant additional losses. For this reason this parameter space was also discarded as a potential candidate.

The result surfaces for the (R_{gle}, R_{ghe}) parameter space indicated that this parameter space may provide good opportunities for independent control of the di/dt and dv/dt metrics. This approach, however, would reintroduce substantial impedance into the gate of the high-voltage MOSFET, potentially eliminating some of the advantages of the cascode configuration. For this reason it was decided that this approach fell outside the scope of this thesis. Instead, potential future research pathways arising from this finding are presented in Section 5.6.

Simulation of the (R_{gle}, C_{gshe}) and (R_{gle}, C_{dsle}) parameter spaces produced very similar result surfaces. From inspection of the cascode gate drive topology it can be seen that this is to be expected as charging or discharging respectively of these capacitances during turn-on would result in the same additional current being seen by the cascode MOSFET. While there may be advantages in introducing one capacitance over the other, or a combination of both, the difference in the effect on the investigated metrics was minimal. Further discussion will focus on the (R_{gle}, C_{gshe}) parameter space, but should also be applicable to the (R_{gle}, C_{dsle}) parameter space.

From inspection of the (R_{gle}, C_{gshe}) parameter space show in Figure 3.11 it can be seen that for small values of C_{gshe}, the average dv/dt and switching loss metrics

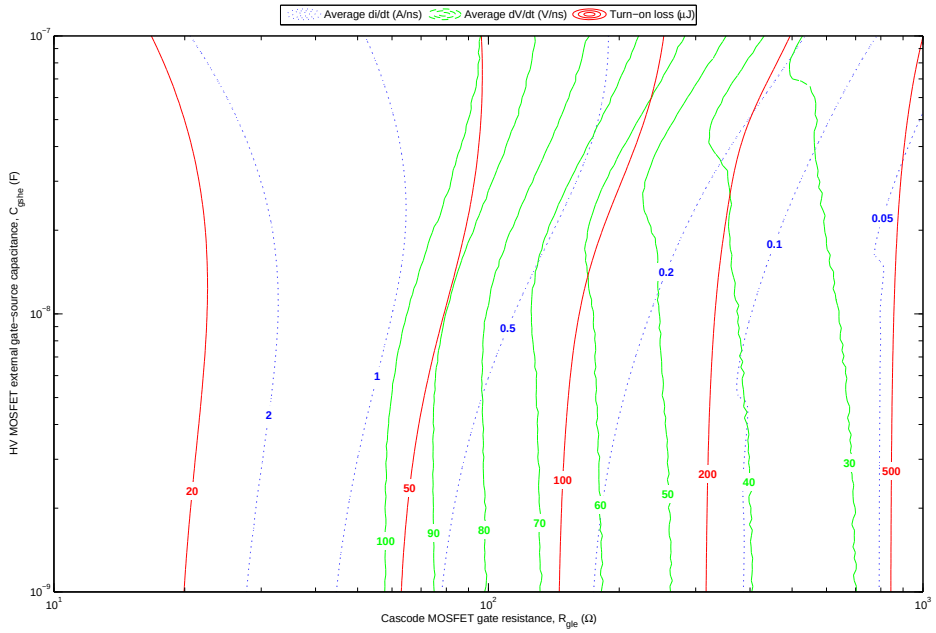


Figure 3.11: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, HV MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space.

are relatively insensitive to changes in this capacitance. As the C_{gshe} capacitance is increased, however, the average di/dt metric also increases. This provides the opportunity to traverse the dv/dt metric surface while holding the di/dt constant (or vice-versa). Consider, for example, the 0.2 A/ns di/dt contour: at approximately ($R_{gle} = 180\,\Omega, C_{gshe} = 2\,\text{nF}$) the 0.2 A/ns contour intersects with the 60 V/ns contour. By increasing both R_{gle} and C_{gshe} it is possible to follow the contour of di/dt = 0.2 A/ns to its intersection with the 40 V/ns contour at approximately ($R_{gle} = 330\,\Omega, C_{gshe} = 33\,\text{nF}$).

From the above cursory analysis it can be seen that this parameter space is a potential candidate to allow optimisation of the switching performance metrics. Adding additional gate-source capacitance to the high-voltage MOSFET is not expected to have unacceptable negative effects. While this additional capacitance will result in increased drive losses, the energy stored in a capacitance of the 1–100 nF required to observe an effect is small compared to the total turn-on losses due to the capacitance only being charged to the gate drive voltage (10 V to 20 V).

Based on this initial analysis the (R_{gle}, C_{gshe}) was selected as a candidate parameter space for further investigation. The following section provides a detailed analysis of the operation of the cascode drive topology over this parameter space including factors such as load current sensitivity and additional performance metrics such as maximum dv/dt and di/dt.

3.8 The (R_{gle}, C_{gshe}) parameter space

A detailed investigation of the (R_{gle}, C_{gshe}) parameter space for cascode drive of power MOSFETs was performed via simulation. A summary of the test conditions over which simulations were performed is provided in Table 3.2.

Parameter	Description	Value(s)
V_{bus}	Bus voltage	400 V
V_{drl}	Cascode MOSFET drive voltage	5 V
V_{drh}	HV MOSFET drive voltage	12 V
R_{gle}	Cascode MOSFET external gate resistance	100–1000 Ω
C_{gshe}	HV MOSFET external gate-source capacitance	100 pF–100 nF
I_L	Load current	0.1–10 A

Table 3.2: Test conditions for investigation of the (R_{gle}, C_{gshe}) parameter space by simulation.

This section presents the results from the exploration of the (R_{gle}, C_{gshe}) parameter space by simulation. Interpretation, analysis and discussion of the presented result surface are provided. Figures used to visualise the results have been grouped into Section 3.9 at the end of the chapter to aid the flow of text in the body and to permit easier figure-figure comparison by the reader.

3.8.1 Turn-on switching loss

We begin with an analysis of simulated turn-on switching loss result surfaces. For many applications switching loss will be one of the key, if not the primary, switching performance metric of interest.

Figure 3.12 presents the simulated turn-on switching loss surface, as a contour plot over the (R_{gle}, C_{gshe}) parameter space, for a load current of $I_L = 10$ A. Note that both axes are presented on a logarithmic scale. To aid in interpretation and discussion of these results the plot has been annotated with one characteristic region (region A) and two trajectories through the parameter space (trajectories B and C).

Firstly let us consider Trajectory B. Trajectory B represents the typical mechanism by which switching speed in a cascode drive configuration is controlled: changing the gate resistance of the cascode MOSFET, R_{gle}. Trajectory B shows a decrease in R_{gle} from 1000 Ω to 100 Ω. Note also that Trajectory B is positioned within the parameter space such that the effect of parameter C_{gshe} can be neglected (100 pF is negligible compared with the parasitic gate-source capacitance of the HV MOSFET, which is approximately 1.5 nF). Trajectory B, then, shows the switching performance achievable if R_{gle} is the only parameter varied to control the switching speed.

As an example consider point B1 on Trajectory B. With an R_{gle} value of 1000 Ω a turn-on switching loss of approximately 580 µJ is achieved. To decrease the switching loss it is possible to follow Trajectory B by decreasing R_{gle}, traversing the turn-on switching loss contours. At point B2, corresponding to $R_{gle} = 500\,\Omega$, turn-on losses are reduced to approximately 300 µJ. Turn-on switching loss can be further reduced by continuing along Trajectory B to point B3 ($R_{gle} = 100\,\Omega$) at which point losses are reduced to less than 80 µJ. Note that Trajectory B runs effectively perpendicular to the turn-on loss contour lines in Figure 3.12, indicating that, in terms of turn-on switching loss, this is the optimum control trajectory to reduce loss.

From the spacing of the turn-on loss contour lines it can also be seen that switching loss is more sensitive to changes in R_{gle} for higher values of R_{gle} (contour lines are closer together). R_{gle} then is an effective parameter for controlling the turn-on switching loss in a cascode gate drive configuration. This is the expected result given that *decreasing* the value of R_{gle} is expected to *increase* the turn-on speed, and hence, *reduce* turn-on switching losses.

Let us now introduce the high-voltage MOSFET gate-source capacitance, C_{gshe}, as a second degree of freedom. The C_{gshe} parameter offers the opportunity to traverse the parameter space presented in Figure 3.12 in the Y-axis direction.

Firstly consider Region A in Figure 3.12. Region A represents the portion of the parameter space for which there is very little sensitivity to changes in C_{gshe}, evidenced by the near-vertical contour lines over this region. This is expected given the value of C_{gshe} over this region is small compared with the parasitic gate-source capacitance of the high-voltage MOSFET (approximately 1.5 nF). For values of $C_{gshe} > 1\,\text{nF}$, however, there is an appreciable change in turn-on loss for increasing C_{gshe}.

Trajectory C shows a trajectory through the (R_{gle}, C_{gshe}) parameter space for increasing values of C_{gshe} with $R_{gle} = 500\,\Omega$. At point C1 (500 Ω, 1 nF) a turn-on loss of approximately 300 µJ is achieved. It is possible to traverse the loss contours, however, by following Trajectory C and increasing C_{gshe}. At point C3 (500 Ω, 100 nF), for example, turn-on losses are reduced to approximately 200 µJ, an approximate 33 % reduction.

This result is somewhat counter-intuitive given that an increase in gate-source capacitance would usually be associated with a *decrease* in switching speed, and hence, *increase* in switching losses. It should also be noted that increasing the gate-source capacitance of the high-voltage MOSFET will result in higher gate-drive losses; for a 100 nF increase in gate source capacitance and 12 V gate drive a conservative estimate of these additional losses would be on the order of 8 µJ.

The 100 µJ turn-on loss saving completely offsets the additional gate-drive loss, however, the gate drive loss does reduce the net energy saving somewhat.

Figure 3.13 provides a different visualisation of the data presented in Figure 3.12: turn-on switching loss is presented as a function of R_{gle} for different values of C_{gshe} (effectively constant C_{gshe} slices of the turn-on loss surface). Trajectories B and C from Figure 3.12 have been included on Figure 3.13 also.

Figure 3.13 shows clearly the relative change in turn-on loss that can be affected by changing the values of R_{gle} and C_{gshe} respectively. A 7–10 times reduction in losses is possible via the R_{gle} parameter over the 100–1000 Ω range. Comparatively, around a 15–35 % reduction in turn-on loss is possible by increasing C_{gshe} from 100 pF to 100 nF over the same R_{gle} range.

Equally, it is possible to affect the same loss reduction via any number of (R_{gle}, C_{gshe}) combinations. For example consider the C1–C3 trajectory which achieves a reduction in turn-on losses from 300 µJ to 200 µJ. The same effect could be achieved by decreasing R_{gle} from 500 Ω to 300 Ω. In order to determine which of these options is preferable, additional switching performance metrics need to be considered, as discussed in subsequent sections.

3.8.2 Maximum turn-on di/dt and dv/dt

In the coarse parameter sweeps (see Section 3.7) we focused on the average di/dt and dv/dt over the switching transition. These metrics are easier to extract from turn-on waveform data than instantaneous time-derivatives and are less sensitive to simulation artefacts (e.g. step changes). The averaged metrics were perfectly suitable for use in the coarse parameter sweeps, for which the key purpose was to conduct a broad exploration of the parameter space to select candidate parameters for more detailed investigation.

For practical applications, however, the maximum instantaneous di/dt and dv/dt metrics will be more relevant to operation of the circuit. For example, power MOSFET manufacturers usually specify a "maximum dv/dt ruggedness" for their devices (typically of the order of 50 V/ns); operation below this limit is recommended to avoid the risk of dv/dt induced turn-on of the device. Equally, converter EMI is a function of both dv/dt and di/dt – addressing the peak di/dt and dv/dt therefore makes more sense in the context of reducing EMI.

Figure 3.14 presents the maximum di/dt, maximum dv/dt and turn-on loss surfaces over the (R_{gle}, C_{gshe}) parameter space for $I_L = 10$ A. Trajectories B and C corresponding to Figure 3.12 are also included.

Again, we firstly consider Trajectory B: control of the switching speed by adjustment of R_{gle}. From Figure 3.14 it can be seen that as R_{gle} is decreased,

both the maximum di/dt and maximum dv/dt during the switching transition also increase. Figure 3.15 shows the simulated turn-on waveforms corresponding to points B1–B3 on Trajectory B. The traces have been time-synchronised at the point when $I_L = 10\,\mathrm{A}$.

From these waveforms the effect of decreasing R_{gle} can be clearly seen. There is a significant decrease in the rise time of the drain-current and also of the maximum di/dt. In each case the maximum di/dt occurs at $I_L = 10\,\mathrm{A}$ and the gradient of the drain-source current traces at this point increases substantially with decreasing R_{gle}. Note also that the change in the current rise time has a much larger impact on the turn-on switching losses (proportional to the area under the drain-current rise) than any change to the fall-time in drain-source voltage.

An appreciable change in drain-source voltage fall time, and hence, dv/dt is also observed for decreasing R_{gle}. Reducing the value of R_{gle} also results in the minimum on-state voltage being reached more quickly.

Next we consider the effect of changing C_{gshe} on the maximum di/dt and dv/dt metrics. From the contour plots in Figure 3.14 it can be seen that as C_{gshe} is increased there is relatively little change to the maximum di/dt up to Boundary D (evidenced by the near-vertical contour lines). Conversely, a *decrease* in the maximum dv/dt is observed over this region for increasing C_{gshe}.

Beyond Boundary D it is possible to observe a change in these trends: as C_{gshe} is further increased there is a significant increase is both maximum di/dt and dv/dt. Figure 3.14 has been annotated with Boundary D to delineate the approximate boundary in the parameter beyond which this change in the observed behaviour occurs.

Trajectory C can again be used to illustrate more clearly the behaviour captured by the contour plots. At point C1 (500 Ω, 1 nF) the maximum di/dt is 157 A/µs while the maximum dv/dt is 58 V/ns. We then follow Trajectory C to point C2 by increasing C_{gshe} to 40 nF. At point C2 (500 Ω, 40 nF) the maximum di/dt has increased marginally to 167 A/µs whilst the maximum dv/dt has decreased to 52 V/ns. Note that while maximum di/dt has remains relatively constant (6 % increase) and maximum dv/dt has *decreased* (10 %), a decrease in turn-on switching loss of more than 10 % is observed.

Further increases to C_{gshe} push operation into the region beyond Boundary D. At point C3 (500 Ω, 100 nF), for example, maximum di/dt increases substantially to 244 A/µs. Maximum dv/dt is unchanged at 52 V/ns at this point, though note that between points C2 and C3, Trajectory C traverses a valley in the maximum dv/dt surface and further increases to C_{gshe} would result in increases to maximum dv/dt.

Figure 3.16 presents the transient turn-on waveforms corresponding to points C1–C3. From these waveforms the effect of increasing C_{gshe} can be seen: the drain current rise time is substantially reduced. Note that for points C1 and C2 the drain current traces converge to approximately the same gradient at $I_L = 10\,\text{A}$, that is, they exhibit approximately the same maximum di/dt even though the rise time (and hence turn-on losses) at point C2 is substantially reduced. The drain-source voltage waveforms for all three points are difficult to discriminate – this is behaviour observed from the contour plot where there was only a minor decrease in maximum dv/dt over Trajectory C.

Figure 3.17 presents the data from Figure 3.14 as a set of constant C_{gshe} slices through the result surfaces. Average di/dt is additionally presented in this figure (a representation of the rise time). Figure 3.17 provides some insight into the mechanism by which turn-on losses are reduced while maximum di/dt stays relatively constant and maximum dv/dt decreases.

It can be seen that over the entire range of R_{gle} values, increases in C_{gshe} result in a decrease in switching losses. For the maximum dv/dt metric the behaviour is more complex. For $R_{gle} > 500\,\Omega$ an increase in C_{gshe} results in an decrease in maximum dv/dt. As R_{gle} is decreased, however, we see a transition in the behaviour such that increases beyond a certain value of C_{gshe} result in an increase in maximum dv/dt: this is the Boundary D, presented in Figure 3.14.

From the maximum di/dt curves we see that the curves converge for high values of R_{gle}, but then diverge at a certain point (dependent on the value of C_{gshe}) as R_{gle} is decreased. This means that there is a range over which C_{gshe} can be increased (dependent on the value of R_{gle}) without the maximum di/dt being affected.

When we compare the behaviour of the average di/dt metric, however, we see that for any increase in C_{gshe} above 1 nF there is a corresponding increase in the average di/dt. The implication of this behaviour is that it is possible to increase the average di/dt towards the maximum di/dt to effect a reduction in turn-on switching loss, without increasing the maximum di/dt during the switching transition.

For example, refer again to the points C1–C3 on Trajectory C which have been annotated on Figure 3.14. From point C1 (green) to C2 (magenta) there is relatively little change in maximum di/dt. Conversely, the average di/dt metric almost doubles, resulting in an appreciable reduction in turn-on loss. The maximum dv/dt actually reduces between points C1–C2.

To further explore the potential implications and possible applications of these findings the following section utilises the switching performance result surfaces presented above in two switching performance optimisation exercises.

3.8.3 Switching performance optimisation

The characteristics of the switching performance surfaces over the (R_{gle}, C_{gshe}) elucidated in the previous section provide the opportunity to utilise the cascode gate drive configuration to achieve optimised switching given a set of practical constraints. This section illustrates this process by presenting two different optimisation exercises.

3.8.3.1 Switching loss optimisation given a maximum dv/dt constraint

In this example we consider the process of turn-on switching loss optimisation given a maximum dv/dt constraint. Such a constraint would commonly be imposed based on the dv/dt ruggedness of MOSFETs used in a half-bridge configuration. The high-voltage power MOSFET in this work, for example, has a dv/dt ruggedness rating of 50 V/ns.

Figure 3.18 shows the maximum di/dt, maximum dv/dt and turn-on switching loss surfaces plotted over the (R_{gle}, C_{gshe}) parameter space. If the gate drive were controlled via the typical mechanism, cascode MOSFET gate resistance, R_{gle}, this exercise would be trivial: R_{gle} would be set to 680 Ω to achieve a maximum dv/dt of 50 V/ns realising a turn-on switching loss of approximately 400 µJ.

Based on the findings of this work, however, we have a second degree of freedom with which to control the switching process: adding external gate-source capacitance, C_{gshe}, to the high-voltage power MOSFET. This second parameter provides us with the opportunity to traverse the switching performance surfaces presented in Figure 3.18.

The optimisation process begins at point E1 (660 Ω, 1 nF), which achieves effectively the same performance as the base 680 Ω case described above. Recall from the previous section that it was observed that, in general, increasing C_{gshe} resulted in a decrease in both turn-on switching losses and maximum dv/dt. We expect, then, that increasing C_{gshe} should provide more optimal switching performance. Given that increasing C_{gshe} will affect a decrease in R_{gle}, however, we can simultaneously decrease R_{gle} to provided an additional decrease in switching losses whilst maintaining maximum dv/dt within the allowable 50 V/ns limit.

Trajectory E provides a graphical representation of this process. Given the imposed constraint of 50 V/ns maximum dv/dt, we will achieve the optimum result by following the 50 V/ns contour line to traverse the turn-on loss surface to the point of minimum loss (within the available parameter space). Points E2, E4 and E5 show increasingly optimised switching performance as C_{gshe} is increased to 20 nF, 40 nF and 100 nF respectively. E3 (540 Ω, 28 nF) shows the point at which turn-on switching losses are reduced from 400 µJ (base case) to

300 µJ (50 % reduction). Note that achieving this reduction in switching losses has resulted in a 25 % increase in maximum di/dt from 120 A/µs to 150 A/µs.

Further switching loss reductions can be achieved though further increases to C_{gshe} (and corresponding reductions to R_{gle}). At point E5 (510 Ω, 100 nF) a turn-on switching loss of 210 µJ is achieved, representing a loss reduction of almost 50 % compared with the base case. Maximum di/dt at this operating point is 237 A/µs, approximately double compared with the base case.

Figure 3.19 shows the simulated switching transient waveforms that correspond to points E1–E5 on Trajectory E. Note that for all cases the drain-source voltage transient (and hence maximum dv/dt are well matched). Conversely the rise in drain current is distinctly different in each case, and as Trajectory E is followed, a substantial reduction in the drain-current rise time is observed.

This simple example illustrates the potential benefits of using the (R_{gle}, C_{gshe}) parameter space to optimise the switching performance of power MOSFETs under cascode gate drive. For the 50 V/ns maximum dv/dt constraint used in this example, a reduction in turn-on switching losses of almost 50 % was achievable via appropriate application of the findings of this work, and through use of switching metric contour plots as a design tool.

3.8.3.2 Switching loss optimisation given a maximum di/dt constraint

In this second example we consider the process of turn-on switching loss optimisation given a maximum di/dt constraint. A maximum di/dt constrain may arise based on a number of considerations, including: EMI limits, diode reverse recovery considerations, transient overvoltage considerations (in the presence of parasitic inductances) or maximum device current commutation speed. For this example we select the maximum body diode commutation limit of 200 A/µs specified by the manufacturer for the MOSFET used in this work.

Figure 3.20 shows the maximum di/dt, maximum dv/dt and turn-on switching loss surfaces plotted over the (R_{gle}, C_{gshe}) parameter space. As in the previous example, if the gate drive were controlled via the typical mechanism, cascode MOSFET gate resistance, R_{gle}, this exercise would be trivial: R_{gle} would be set to 390 Ω to achieve a maximum di/dt of 200 A/µs realising a turn-on switching loss of approximately 240 µJ.

If we introduce C_{gshe} as a second degree of freedom, however, improved switching performance can be achieved. Consider Trajectory F which follows the constant maximum di/dt trajectory of 200 A/µs through the (R_{gle}, C_{gshe}) parameter space. In this case the optimum trajectory through the parameter space is effectively vertical, that is, a reduction in turn-on switching losses is achieved by increasing C_{gshe} while holding R_{gle} relatively constant. Points F1–F3 show op-

erating points along this trajectory for C_{gshe} values of 1 nF, 10 nF and 40 nF respectively. Note that point F3 sits in a valley in the maximum di/dt surface; following the 200 A/µs beyond point F3 does not achieve any further reduction in turn-on switching loss.

From points F1 to F3 a reduction in turn-on switching losses from 240 µJ to 216 µJ is achieved (10 % reduction). Note that while maximum di/dt has been held constant, Trajectory F traverses the average di/dt contour lines, increasing the average di/dt from 100 A/µs to > 150 A/µs (approaching the maximum di/dt of 200 A/µs); this is the primary mechanism by which turn-on switching losses are reduced.

Figure 3.21 shows the simulated transient turn-on waveforms corresponding to points F1–F3 on Trajectory F. Note that all three drain current waveforms converge to the same gradient at $I_L = 10$ A; this is the point of maximum di/dt (set to 200 A/µs by the optimisation exercise). The major difference between the presented drain current traces is the shape of the leading edge. As C_{gshe} is increased the drain current ramps-up more quickly to the maximum di/dt, resulting in a reduction of the drain-current rise time.

There is little observable change in the drain-source voltage waveform. From Figure 3.18, however, we expect a minor reduction in the maximum dv/dt over Trajectory F.

3.8.4 Load current sensitivity

Practical converters typically operate over a range of load currents. The analysis presented in the previous sections focuses on an arbitrary nominal load current of 10 A. For operation of a cascode gate drive in a practical application, however, the sensitivity of the switching performance to changing load current is of interest. Particularly it is of interest to identify the worst-case operating point (per metric). If the worst case point (or points) can be easily identified, the design process is simplified as details analysis can be conducted at the boundaries of operation, rather than over the entire operating range. A typical worst case operating point for a switching converter would usually be at peak load current.

Figure 3.22 presents the maximum di/dt, maximum dv/dt and switching loss surfaces over the (R_{gle}, I_L) parameter space for different values of C_{gshe}. Note that a load current trajectory in a practical application would be represented as a vertical line over this parameters space; an increase in load current moves the operating point in the positive Y direction, while a decrease in load current would move the operating point in the negative Y direction. Trajectory G plots a load current trajectory through the parameter space from a peak current of 10 A to a

minimum current of 100 mA.

Figure 3.22 is complemented by Figure 3.23 which shows the three switching metrics as a function of load current, I_L, for $R_{gle} = 400\,\Omega$ and various values of C_{gshe}. Note that Trajectory G is a decreasing load current trajectory through the parameter space, and therefore, applies to all curves presented in Figure 3.23, even though only two of the curves are explicitly annotated. The following analysis should be read with reference to both Figures 3.22 and 3.23 as appropriate.

Firstly we consider the effect of load current on turn-on switching losses. Based on a fundamental understanding of switching losses, we expect switching losses to be proportional to load current. This expectation is substantiated by the simulated loss surfaces presented in Figure 3.22: turn-on switching losses increase with increasing load-current and R_{gle}. Increasing C_{gshe} shifts the operating point slightly (reduces switching losses). This is more clearly seen in Figure 3.23 which shows that turn-on switching losses are monotonically increasing as a function of load current, regardless of the value of C_{gshe}. The maximum load current case can safely be taken as the worst-case turn-on switching loss operating point.

Next we consider the maximum di/dt surfaces presented in Figure 3.22. These surfaces exhibit some interesting features, particularly the regions where maximum di/dt is independent of load current (evidenced by vertical contour lines). This behaviour is showcased in Figure 3.23 where plateaus in the maximum di/dt are visible. While this behaviour is interesting to note, and may warrant further investigation in future work, the primary consideration of this analysis are the worst case operating points.

We note from Figures 3.22 and 3.23 that maximum di/dt is monotonically increasing across the parameter space for increasing load current, decreasing R_{gle} and increasing C_{gshe}. Worst case maximum di/dt, therefore, always occurs at peak load current.

Finally, we consider the maximum dv/dt surfaces presented in Figure 3.22. Of immediate concern is the valley present in the dv/dt surfaces. Note that this valley is clearly defined for lower values of C_{gshe} but shifts and becomes less defined as C_{gshe} is increased. This valley is of concern because in the circumstances that a peak current operating point is located within the valley, then as the load current is subsequently decreased towards zero, the maximum dv/dt will actually increase.

For example, consider Trajectory G as applied to the maximum dv/dt curves in Figure 3.23. For the $C_{gshe} = 100\,\text{nF}$ case consider the transition from G1 to G2: maximum dv/dt increases as load current decreases from 10 A to 6 A. in this case the increase in dv/dt is relatively modest, however alternatively consider the $C_{gshe} = 40\,\text{nF}$ case. From G1 to G2 there is a substantial decrease in maximum

dv/dt as load current is reduced from 10 A to 6 A; from G2 to G3, however, maximum dv/dt increases by almost 10 V/ns as load current is reduced to 2 A. This may not be a concern if the gate drive has been designed considering 10 A as the maximum load current, but could be an issue if 6 A was assumed to be the maximum load point.

Complicating matters further is that as C_{gshe} is increased the local minimum in the maximum dv/dt shifts position with respect to load current. For example, as C_{gshe} is increased from 100 pF to 40 nF the dv/dt local minimum shifts from approximately 0.2 A to 5.5 A.

The sensitivity of dv/dt to load current is unexpected and no obvious mechanism to support this behaviour is apparent. This result could be an artefact of simulation, particularly given that the exploration of the parameter space via simulation has been conducted using an ideal high-side diode with zero junction capacitance. This finding does highlight the need to conduct characterisation of the switching performance over a range of load currents.

Load current sensitivity will be explicitly investigated via experimentation in order to determine whether this load current sensitivity exists in a practical implementation.

3.9 Simulation result figures

To aid in the presentation of this chapter, figures used to describe the characteristics and simulated performance of the cascode MOSFET drive configuration have been collected into this section. Figures are not necessary presented in the order they appear in-text, but are instead optimally placed to allow convenient figure-to-figure comparison by the reader.

Where possible, figures are accompanied by a self-contained captions such that readers may browse the collection of simulated results without needing to refer to the body of the chapter in order to interpret the figures. Back-references to relevant sections of the chapter body are also provided such that readers may easily locate in-depth analyses of each figure.

3.9.1 Turn-on switching loss

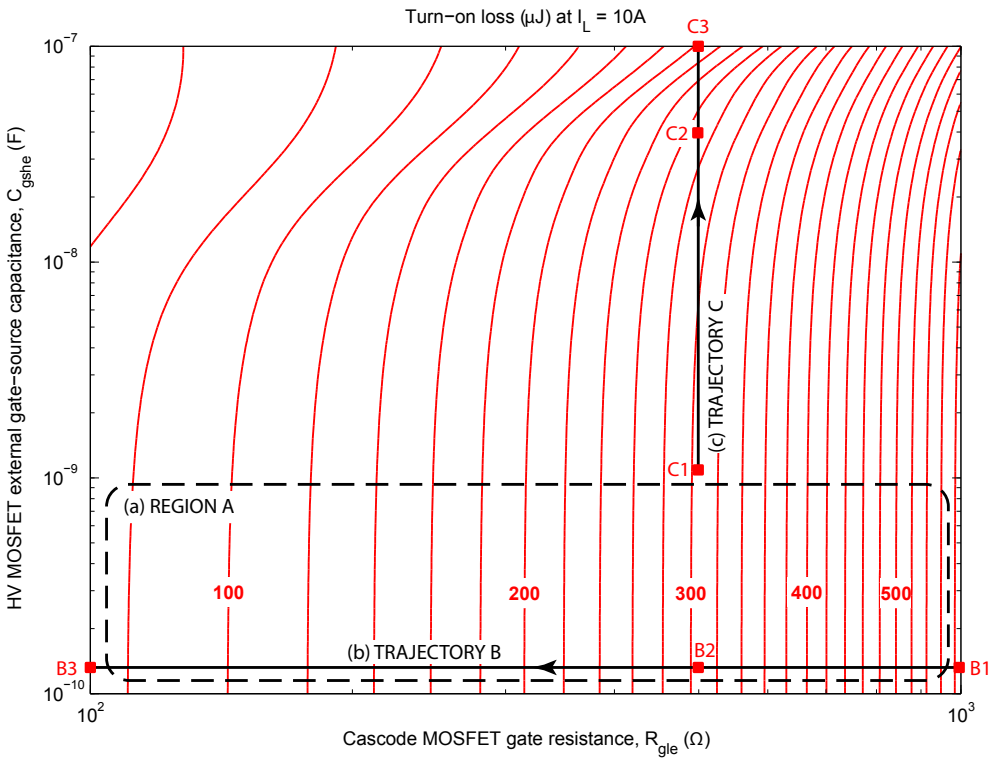


Figure 3.12: Turn-on loss (µJ, red) contours plotted over the cascode MOSFET gate resistance, HV MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space for a fixed load current of 10 A. (a) Region A – The region of the parameter space over which there is limited sensitivity of turn-on loss to changes in C_{gshe}. (b) Trajectory B – Trajectory through the parameter space reducing R_{gle} from 1000–100 Ω for negligible values of C_{gshe}. (c) Trajectory C – Trajectory through the parameter space increasing C_{gshe} from 1–100 nF for $R_{gle} = 500\,\Omega$. Referenced on pages 59 to 61.

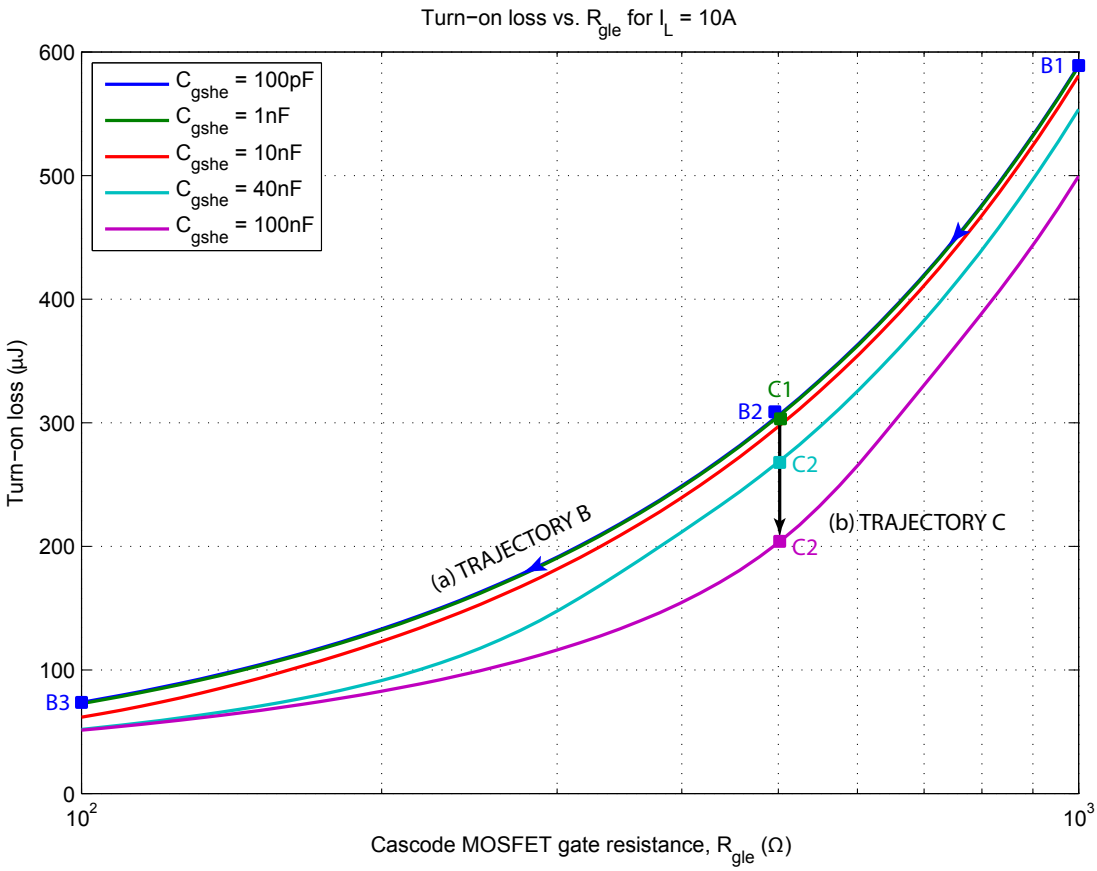


Figure 3.13: Turn-on loss plotted as a function of cascode MOSFET gate resistance for various values of HV MOSFET gate-source capacitance at a fixed load current of 10 A. (a) Trajectory B – Trajectory through the parameter space reducing R_{gle} from 1000–100 Ω for negligible values of C_{gshe}. (b) Trajectory C – Trajectory through the parameter space increasing C_{gshe} from 1–100 nF for $R_{gle} = 500\,\Omega$. Referenced on page 61.

3.9.2 Maximum dv/dt and di/dt sensitivity

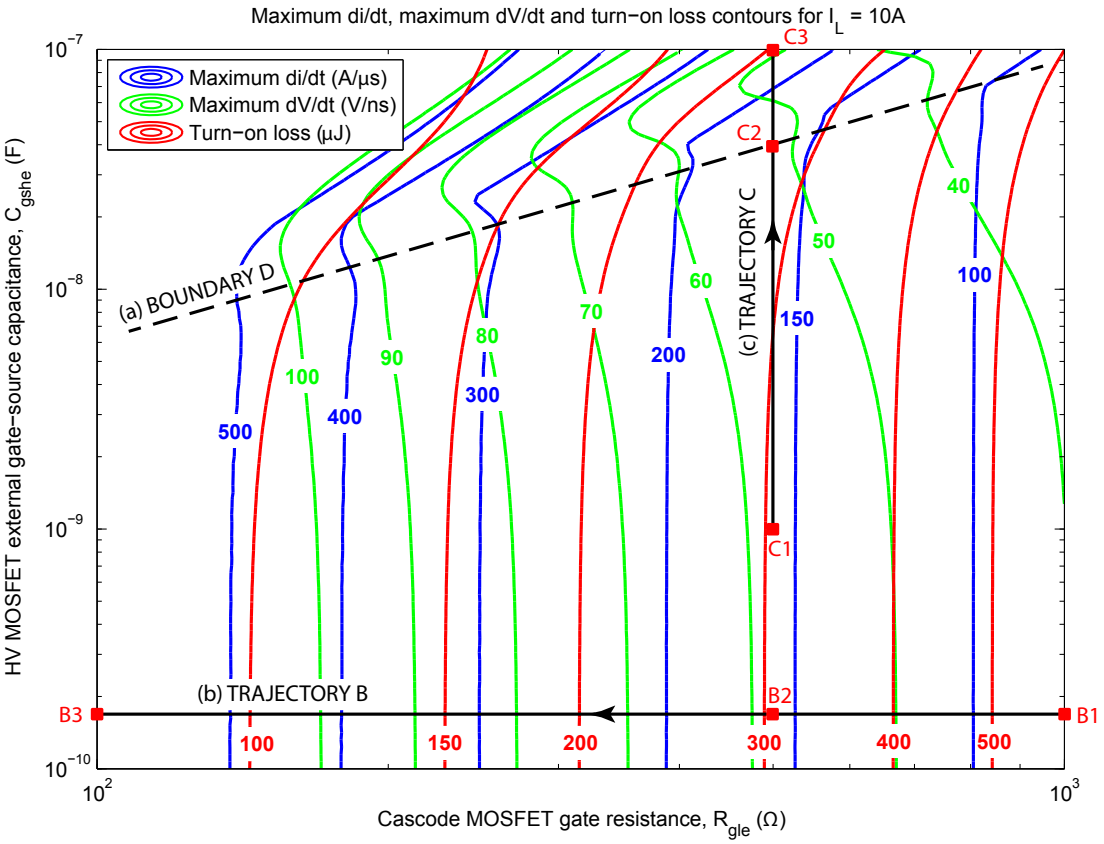


Figure 3.14: Maximum di/dt (A/µs, blue), maximum dv/dt (V/ns, green) and turn-on loss (µJ, red) contours plotted over the cascode MOSFET gate resistance, HV MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space for a fixed load current of 10 A. (a) Boundary D – Approximate boundary in the parameter space beyond which increases in C_{gshe} result in rapid increases in maximum di/dt and dv/dt. (b) Trajectory B – Trajectory through the parameter space reducing R_{gle} from 1000–100 Ω for negligible values of C_{gshe}. (c) Trajectory C – Trajectory through the parameter space increasing C_{gshe} from 1–100 nF for $R_{gle} = 500\,\Omega$. Referenced on pages 61 to 63 and 73.

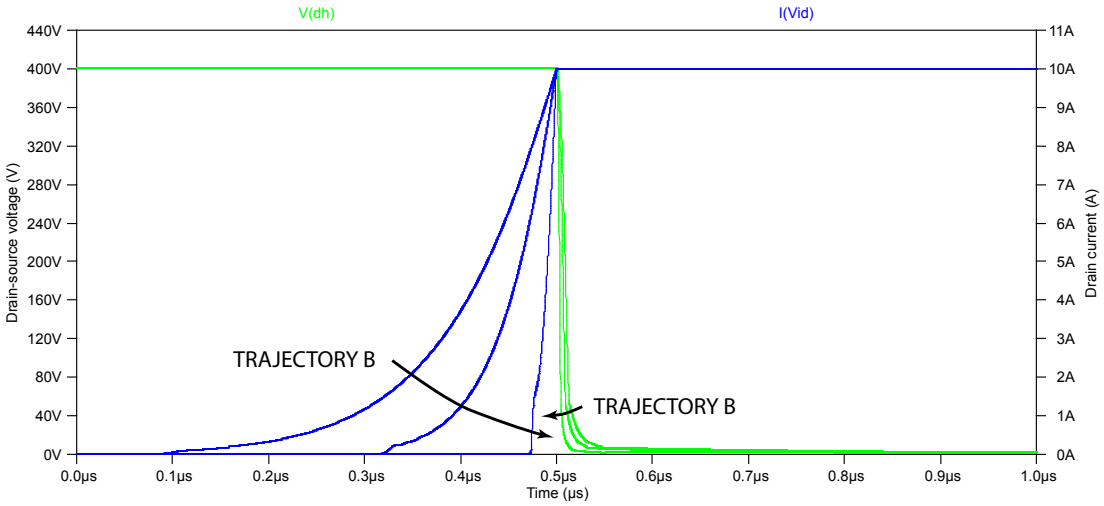


Figure 3.15: Transient turn-on simulation waveforms corresponding to operating points B1–B3 of Trajectory B, as illustrated in Figure 3.14. Referenced on page 62.

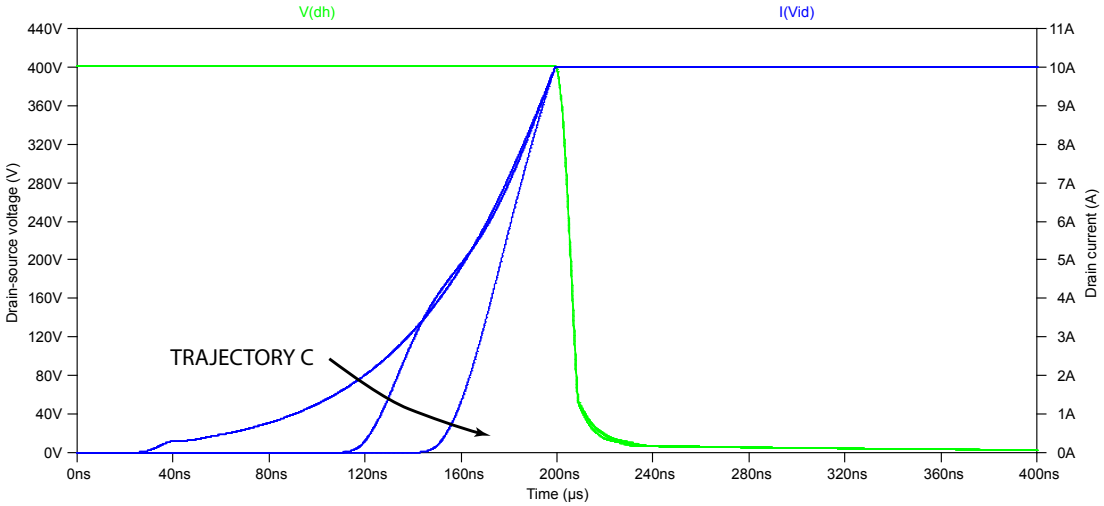


Figure 3.16: Transient turn-on simulation waveforms corresponding to operating points C1–C3 of Trajectory C, as illustrated in Figure 3.14. Referenced on page 63.

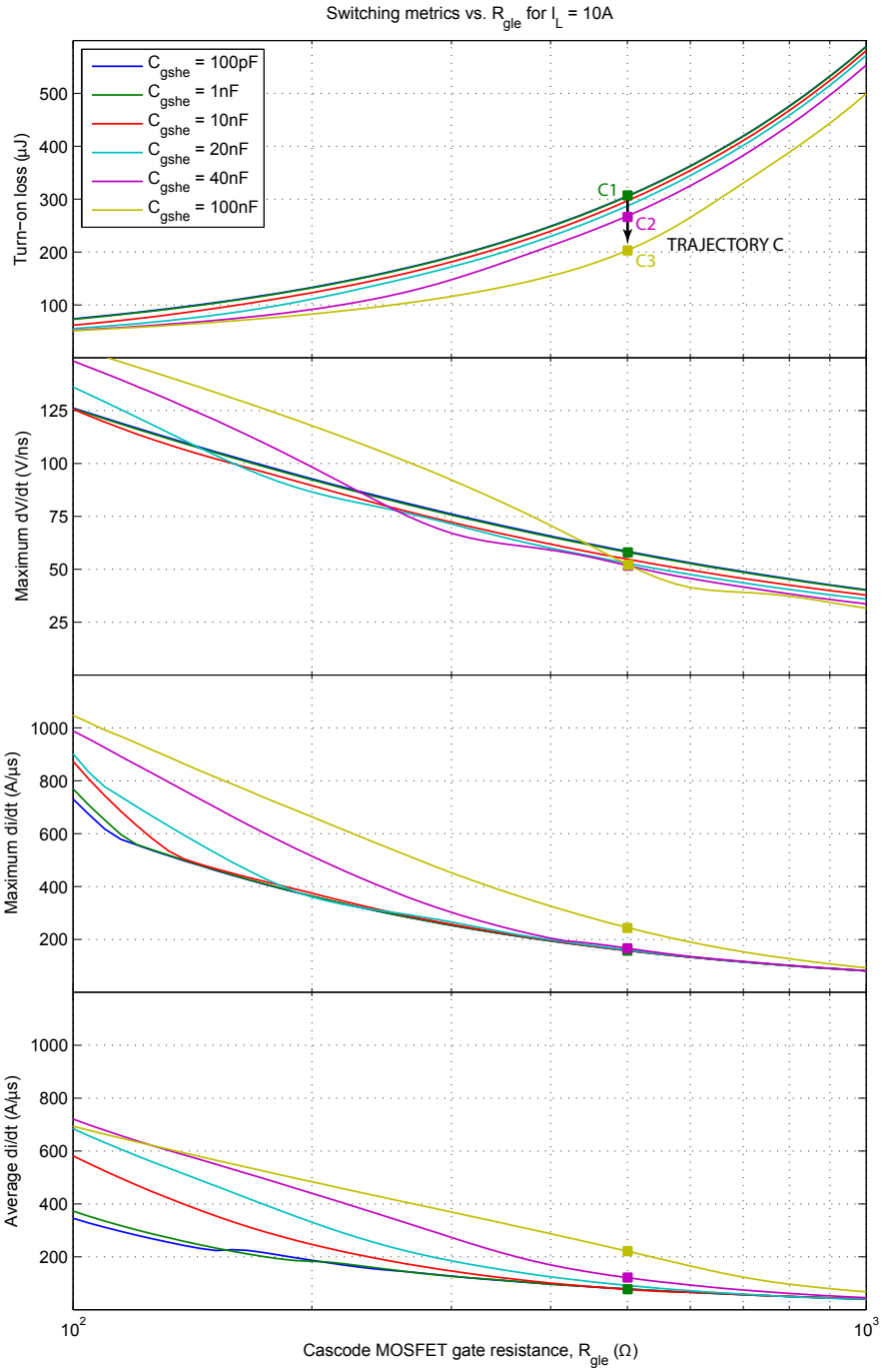


Figure 3.17: Switching metrics plotted as a function of cascode MOSFET gate resistance for various values of HV MOSFET gate-source capacitance at a fixed load current of 10 A. The turn-on loss plot is annotated with Trajectory C, a trajectory through the parameter space increasing C_{gshe} from 1–100 nF for $R_{gle} = 500\,\Omega$. The remaining plots are annotated with points C1–C3 which lie on this trajectory. Referenced on page 63.

3.9.3 Constant maximum dv/dt trajectory

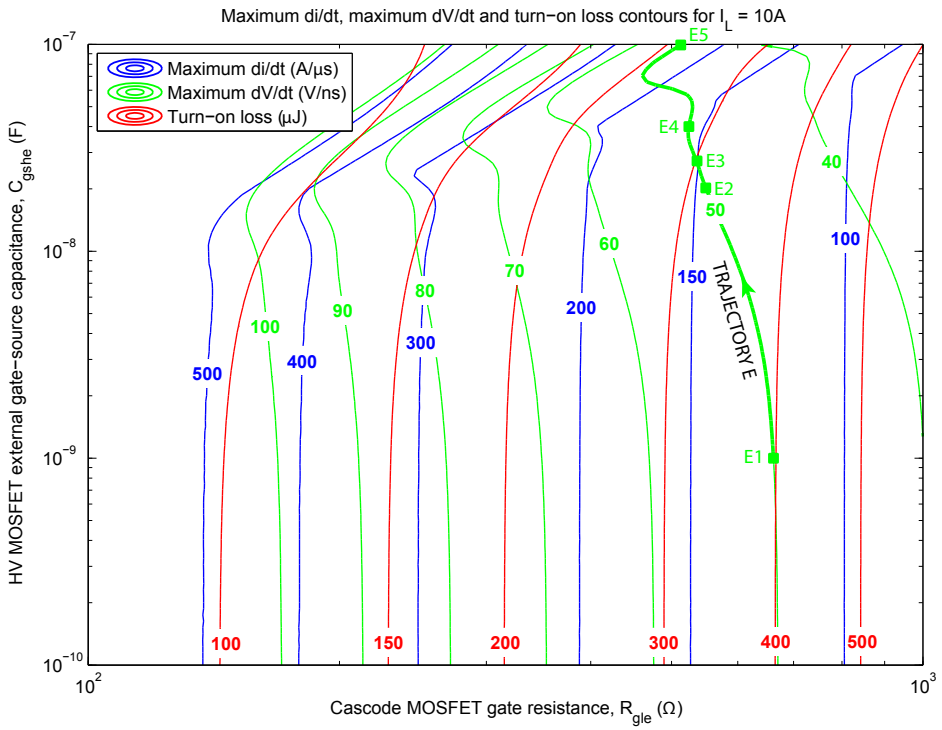


Figure 3.18: Maximum di/dt (A/µs, blue), maximum dv/dt (V/ns, green) and turn-on loss (µJ, red) contours plotted over the cascode MOSFET gate resistance, HV MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space for a fixed load current of 10 A. Additionally shown is Trajectory E, a constant maximum dv/dt trajectory trough the parameter space as C_{gshe} is increased from 1–100 nF. Referenced on pages 64, 66 and 76.

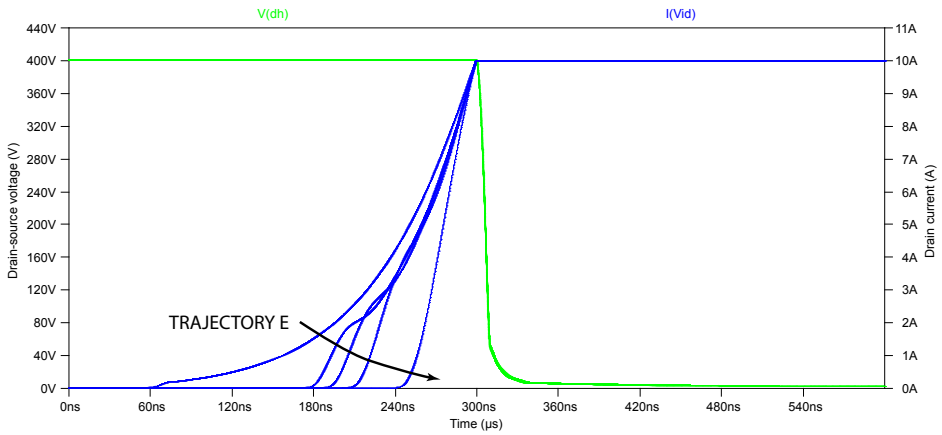


Figure 3.19: Transient turn-on simulation waveforms corresponding to operating points E1–E5 of Trajectory E, as illustrated in Figure 3.18. Referenced on page 65.

3.9.4 Constant maximum di/dt trajectory

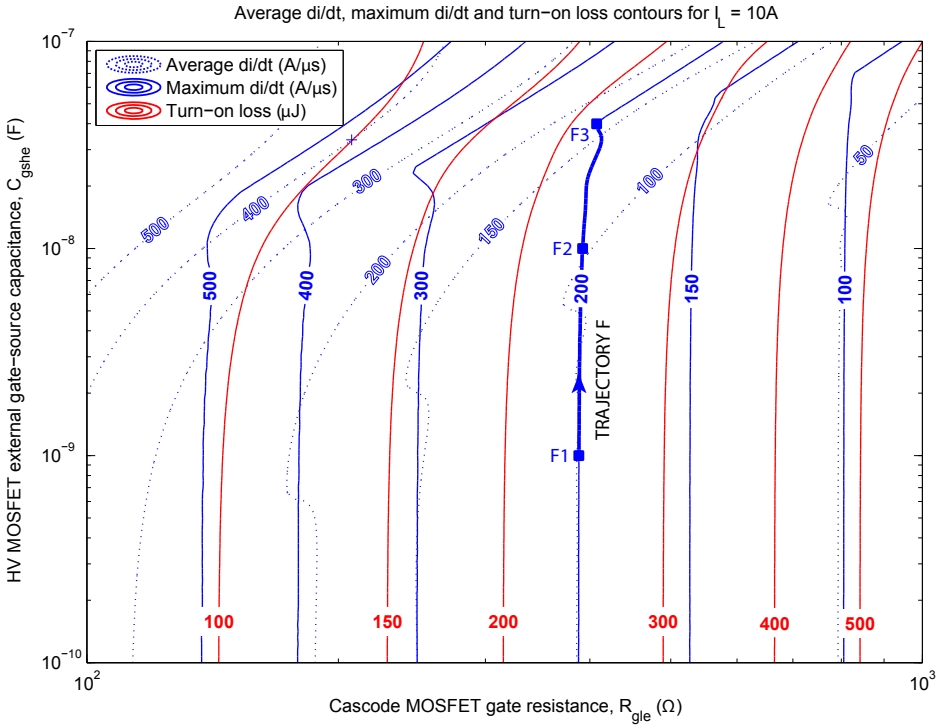


Figure 3.20: Average di/dt (A/µs, dotted blue), maximum di/dt (A/µs, solid blue) and turn-on loss (µJ, red) contours plotted over the cascode MOSFET gate resistance, HV MOSFET gate-source capacitance (R_{gle}, C_{gshe}) parameter space for a fixed load current of 10 A. Additionally shown is Trajectory F, a constant maximum di/dt trajectory trough the parameter space as C_{gshe} is increased from 1–40 nF. Referenced on pages 65 and 77.

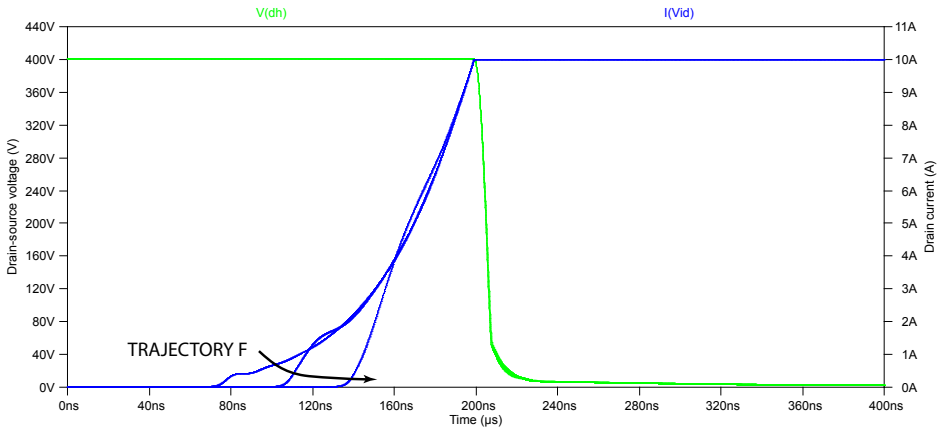


Figure 3.21: Transient turn-on simulation waveforms corresponding to operating points F1–F3 of Trajectory F, as illustrated in Figure 3.20. Referenced on page 66.

3.9.5 Load current sensitivity

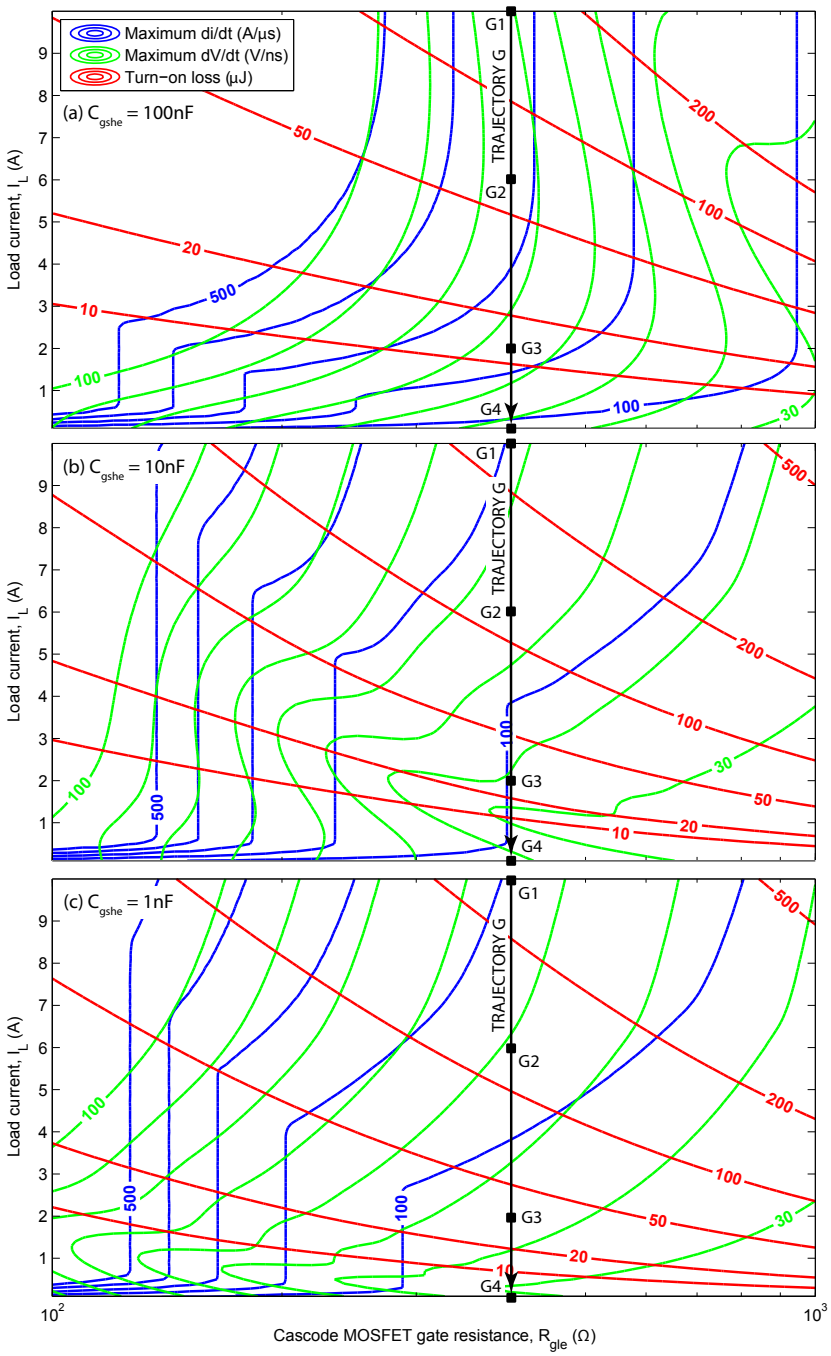


Figure 3.22: Maximum di/dt (A/µs, blue), maximum dv/dt (V/ns, green) and turn-on loss (µJ, red) contours plotted over the cascode MOSFET gate resistance, load current (R_{gle}, I_L) parameter space for a C_{gshe} values of 1 nF, 10 nF and 100 nF respectively. Additionally shown is Trajectory G, a decreasing load current (10–1 A) trajectory trough the parameter space for $R_{gle} = 500\,\Omega$. Referenced on pages 66 and 67.

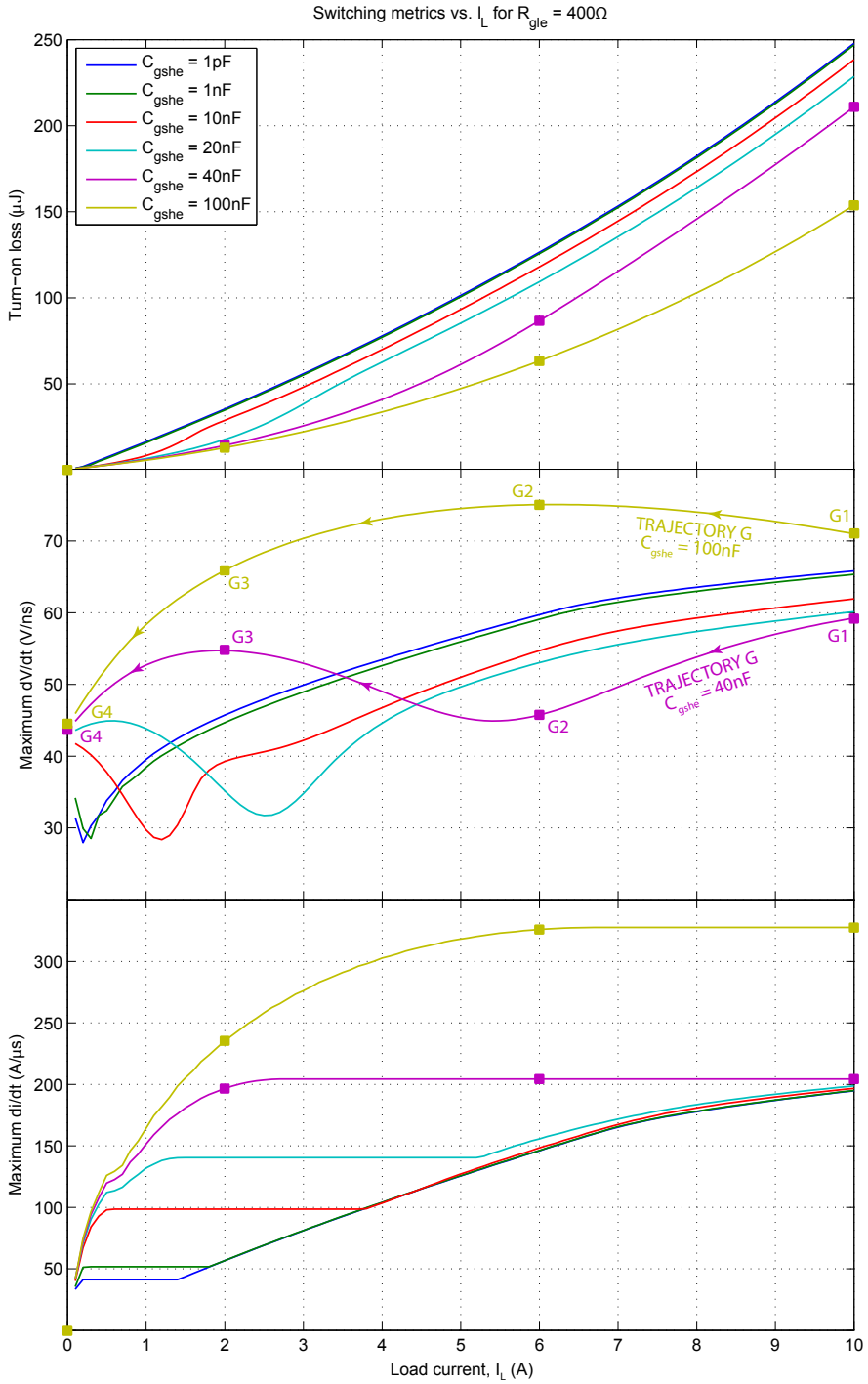
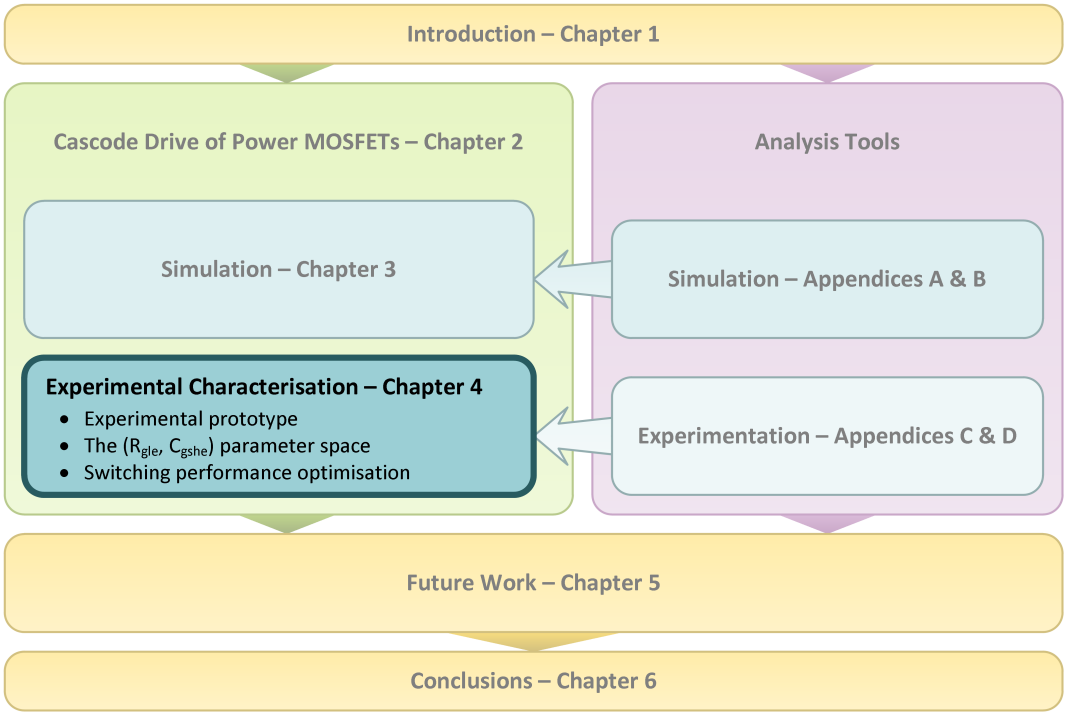


Figure 3.23: Switching metrics plotted as a function of load current for various values of HV MOSFET gate-source capacitance at a fixed cascode MOSFET gate resistance of 500 Ω. The maximum dv/dt plot is annotated with Trajectory G, a trajectory through the parameter space decreasing I_L from 10–1 A for $R_{gle} = 400\,\Omega$. The remaining plots are annotated with points G1–G4 which lie on this trajectory. Referenced on page 67.

Chapter 4

Experimental characterisation of the cascode gate drive of power MOSFETs

This chapter presents the experimental characterisation of cascode gate drive of power MOSFETs. Details of the implemented hardware prototype and test fixture are documented. The cascode gate drive is characterised in a clamped inductive switching application using a double-pulse test fixture. Sensitivity to the cascode MOSFET gate resistance, R_{gle}, high-voltage MOSFET gate-source capacitance, C_{gshe}, and load current, I_L, is explored over 350 experimental operating points.



4.1 Introduction

A hardware prototype was developed to experimentally validate the performance of the proposed cascode gate drive topology. The hardware prototype design and experimental double-pulse test fixture used in this work are described and documented in this chapter.

Additionally it was of interest to perform a detailed experimental characterisation of the performance of the cascode gate drive of power MOSFETs, for the purpose of validating the simulation results. A detailed experimental exploration of the (R_{gle}, C_{gshe}, I_L) parameter space was performed, with switching waveforms for the prototype recorded at over 350 discrete operating points.

A summary of the experimental performance of the prototype is provided along with a detailed analysis of the observed operating characteristics. Finally, opportunities for switching performance optimisation using the elucidated characteristics of the topology are identified, and an example optimisation process is presented using the experimental data.

4.2 Experimental prototype

4.2.1 MOSFET Module

The proposed cascode gate drive topology was implemented in hardware. A 650 V 9.9 A 199 mΩ silicon MOSFET was selected for the high-voltage MOSFET (Infineon IPL60R199CP). This device was selected as it was available in a low-inductance leadless package, and high-quality characteristic data and simulation models were available for this device. The selected device is representative of typical 650V superjuction silicon MOSFETs, but the advanced leadless packaging allows parasitic inductances to be minimised and high switching speeds to be targeted.

A stacked low-voltage n-channel MOSFET pair, also in a leadless package, was selected for the cascode and clamp MOSFETs (Texas Instruments CSD86350Q5D). These MOSFETs were rated at 30 V and 40 A with on-resistances of 1.1 mΩ and 5 mΩ for the cascode and clamp MOSFETs respectively. Similarly, these MOSFETs are representative of typical low-voltge silicon MOSFETs, but the stacked-die, leadless packaging allows parasitic and layout inductances to be minimised. The 1.1 mΩ on-state resistance of the cascode device also presents negligible additional resistance to the load current path (when considered against the 199 mΩ of the high-voltage MOSFET).

To drive the low-voltage MOSFET pair a bootstrap driver IC was selected

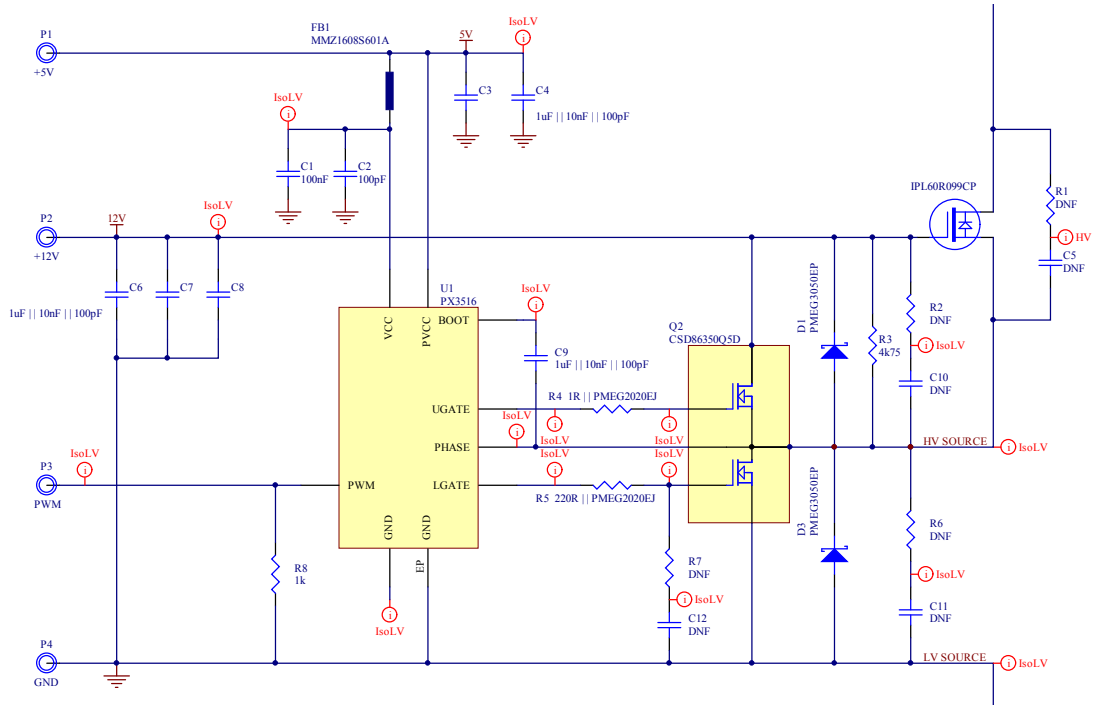


Figure 4.1: Circuit schematics for the experimental prototype of the cascode gate drive topology.

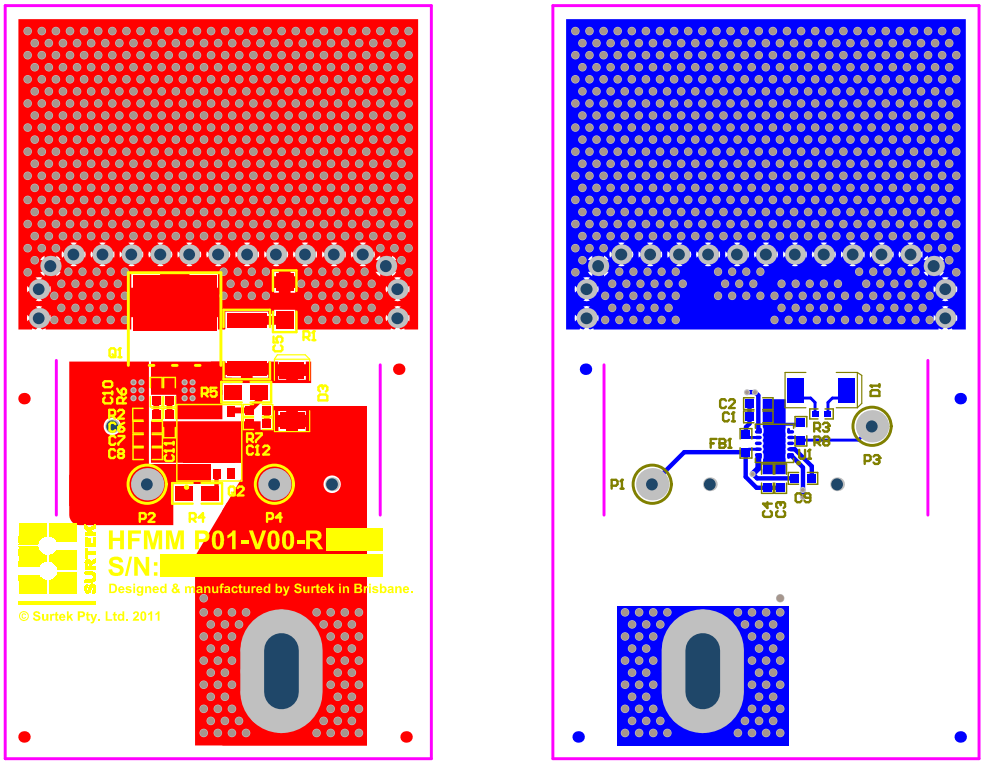


Figure 4.2: PCB layout for the experimental prototype of the cascode gate drive topology. Shown are the top (left) and bottom (right) sides of the implemented PCB.

(Infineon PX3516). Dead-time between the cascode and clamp MOSFETs was achieved through the inclusion of low voltage Schottky diodes in anti-parallel with the gate resistances to provide fast turn-off. The gate resistance for the clamp MOSFET was set to 1 Ω to provide fast turn-off of the high-voltage MOSFET.

The circuit was implemented on a PCB module which provided drain and source connections to the cascode circuit plus 5 V supply (for drive of the low-voltage MOSFETs), 12 V supply (for drive of the high-voltage MOSFET) and PWM signal connections. Detailed circuit schematics for the MOSFET Module are included as a PDF with the digital distribution of this thesis.

4.2.2 Isolation Module

The Isolation Module was implemented to provide an interface between the MOSFET Module (described above) and the switching controller. The module was designed to provided both power and signal isolation.

Power isolation was achieved though the use of 5 V to 15 V isolated DC-DC converters. The 12 V supply for the high-voltage MOSFET was derived from this unregulated, isolated 15 V supply through the use of a unity gain buffer (Linear Technology LT1010) and 12 V voltage reference. This arrangement was used to achieve a 12 V supply capable of both sourcing or sinking power. A low dropout regulator was used to supply the (meagre) power requirements of the low-voltage MOSFET gate drive.

Signal isolation was provided by a digital isolator (Silicon Labs Si8241).

Detailed circuit schematics for the Isolation Module are available in DR-S01-V00R00-IsolationModule.pdf, included with the digital distribution of this thesis.

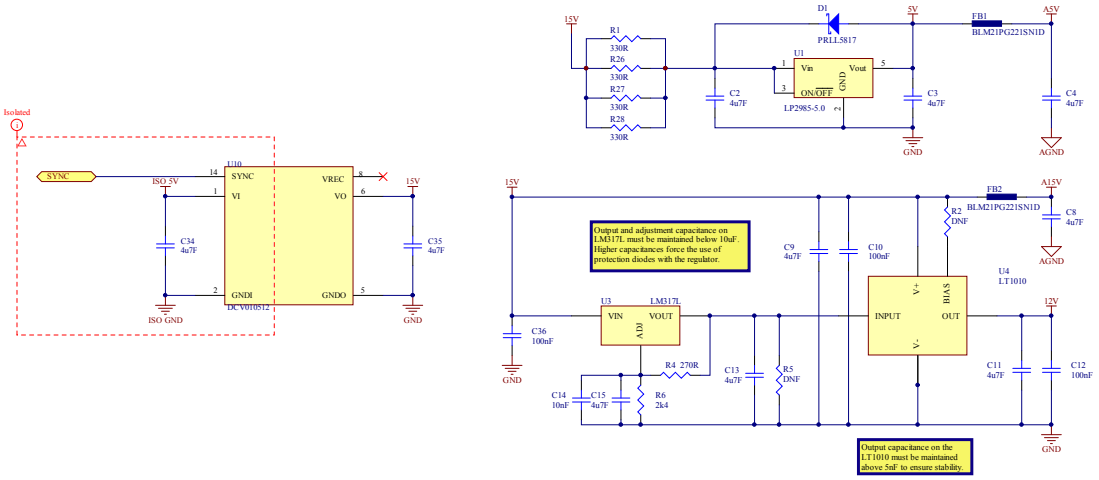


Figure 4.3: Extract of the circuit schematics for the Isolation Module of the experimental prototype. Shown is the isolated power supply and source/sink capable gate drive voltage supply.

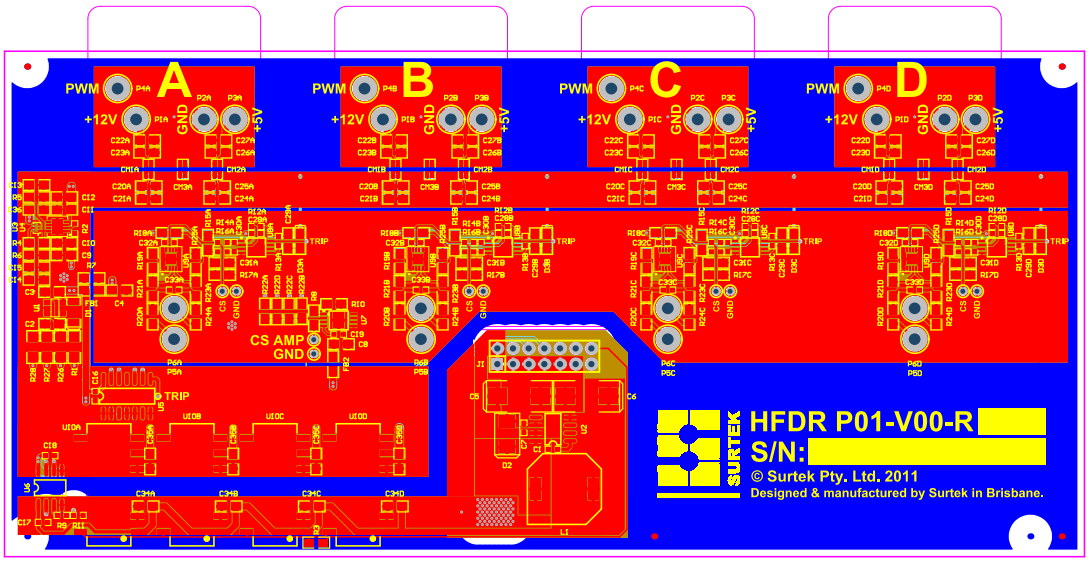


Figure 4.4: PCB layout for the Isolation Module of the experimental prototype.

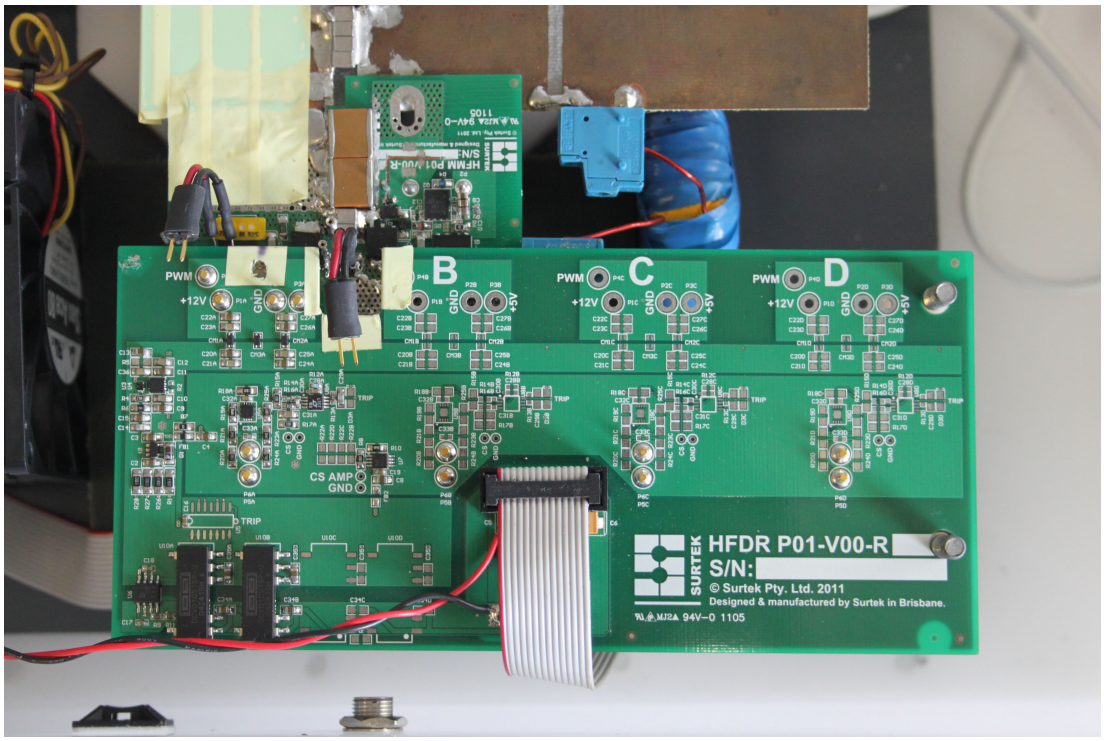


Figure 4.5: Photo of the assembled MOSFET Module and Isolation Module PCBs in the experimental test fixture.

4.3 Experimental test fixture

This section describes the experimental text fixture used to conduct testing of the experimental cascode gate-drive prototype. Figure 4.6 gives an overview of the experimental test fixture, including wiring, power supplies and instrumentation. Further details are provided in the relevant subsections.

4.3.1 Double-pulse configuration

The hardware prototype was configured for double-pulse testing as shown in Figure 4.7. Due to the need to achieve good DC-bus bypassing and to also include a current sense resistor in the switching commutation loop it was necessary to place the cascode gate drive prototype (device under test, DUT) in the high-side position. A SiC Schottky diode (Infineon IDD12SG60C) was placed in the low-side position as the free-wheeling diode. A 450 µH load inductor was then connected from the half-bridge point to the bottom of the bus.

Note that as the DUT was isolated and floating, it was possible to ground the half-bridge point, as shown, to allow ground-referenced voltage measurements to be taken via the oscilloscope.

4.3.2 Adjustment of R_{gle} and C_{gshe}

The value of the cascode MOSFET gate resistance (R_{gle}) was adjusted experimentally by replacing R5 (see Fig. 4.1) with a 500 Ω single-turn surface-mount potentiometer. This solution allowed any value of gate resistance up to 500 Ω to be selected.

A "spring-finger" was soldered to the gate terminal high-voltage MOSFET to allow the external gate-source capacitance (C_{gshe}) to be adjusted by adding surface mount capacitors of various values to the prototype.

4.3.3 Other modifications to the experimental prototype

In early testing of the prototype (in a different physical configuration to the version documented here) it was found that addition of two small RC snubbers across the drain-source of the high-voltage MOSFET (R1 and C5 in Figure 4.1) and opposing Schottky diode allowed the prototype to be operated over a wider operating range without device failures. This snubber (330 pF, 1.1 Ω) was subsequently included in the final experimental tests, but, with the improved physical configuration (i.e. reduced layout inductance), may no longer be necessary.

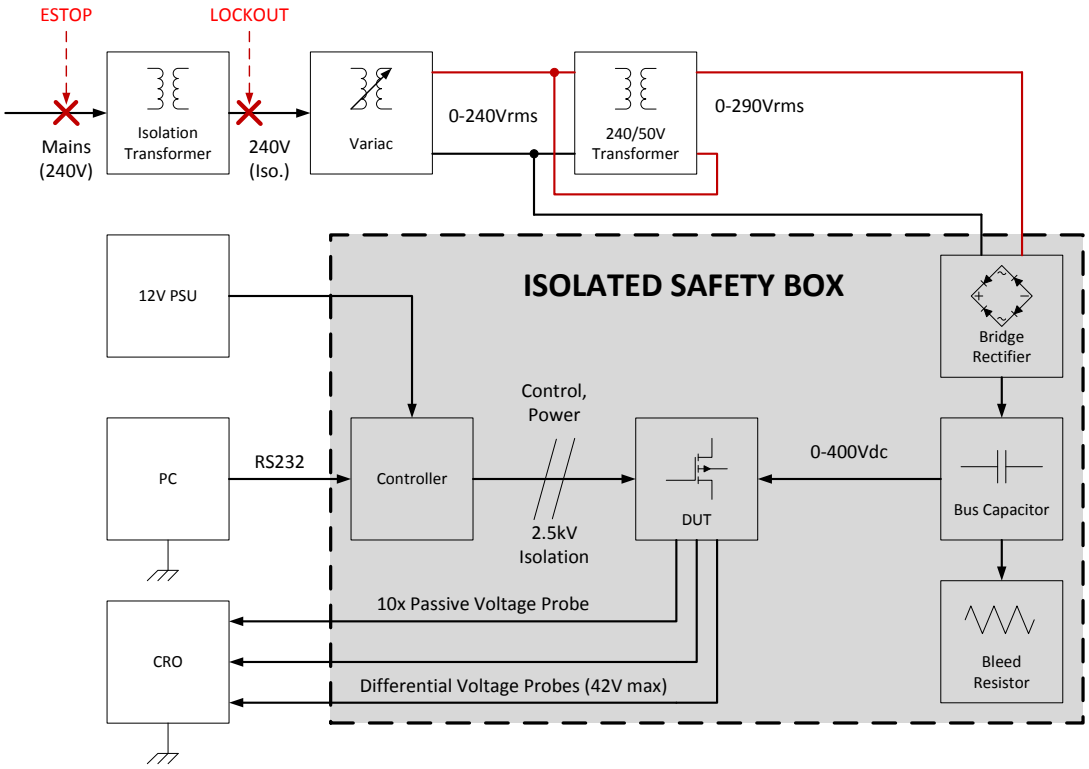


Figure 4.6: Single line diagram of the experimental test fixture and wiring.

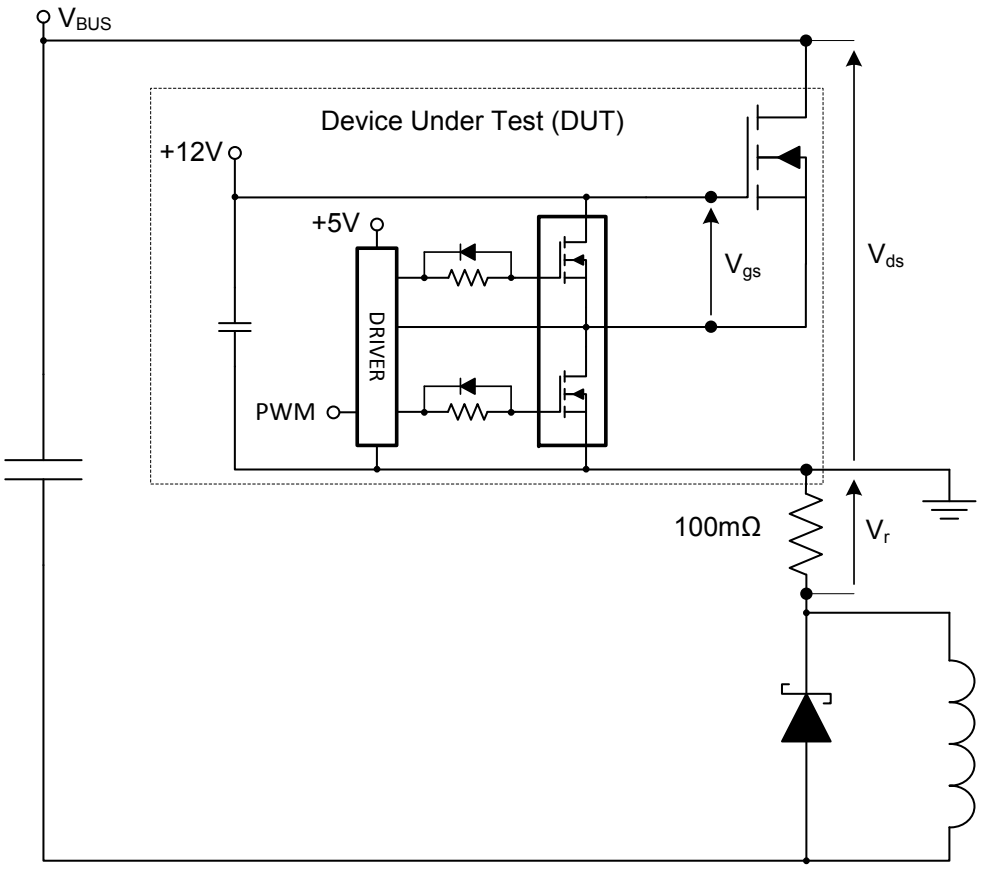


Figure 4.7: Circuit configuration used for experimental double pulse testing.

4.3.4 Power supply

The high-voltage DC (400 V nominal) bus power supply was derived from the rectified AC mains supply (240 V_{RMS} nominal). The input voltage to the bridge rectifier was controlled by an adjustable autotransformer. To achieve the required bus voltage of 400 V_{DC}, a 240/50 V transformer was connected to the output of the variable autotransformer with the primary winding in shunt and the secondary winding in series. This arrangement provided a maximum input voltage to the rectifier of 290 V_{RMS}, which was sufficient to achieve the 400 V DC bus voltage.

The output of the bridge rectifier was connected to a 2400 µF capacitor bus to provide filtering. A 4.4 kΩ resistance was permanently connected across the DC bus to ensure the bus capacitors were discharged to a safe voltage within one minute of the mains power supply being interrupted. The variable autotransformer was supplied through an isolation transformer such that the experimental prototype was floating with respect to ground. The source of the device under test was subsequently ground referenced via the oscilloscope. The specific configuration of the instrumentation is described in Section 4.3.5.

Power was supplied to the microcontroller used to control the switching of the device under test (DUT) via a bench-top power supply. Communication to the controller was achieved via an RS-232 connection to a PC (ground referenced). Galvanic isolation between the controller and DUT was implemented on the isolation module PCB, as described in Section 4.2.2.

4.3.5 Instrumentation

Switching waveforms were recoded using a Tektronix DPO3054 500 MHz oscilloscope with 2.5 GS/s sampling rate. Three voltage waveforms were recorded using the oscilloscope during experimental testing: the drain-source voltage of the DUT (measured from drain of the high-voltage MOSFET to source of the cascode MOSFET), the gate-source voltage of the high-voltage MOSFET and the voltage across the 100 mΩ current sense resistor. The measurement points for each of these measurements are shown in Figure 4.7.

The drain-source voltage was measured with a Tektronix P6139B 500 MHz 10× passive probe, while the gate-source and sense resistor voltages were measured using Tektronix TDP0500 500 MHz high-voltage differential probes. Measurement ranges of 42 V and 4.2 V were selected for the gate-source and sense resistor voltages respectively.

Waveforms were captured using a 16× averaging acquisition mode on the oscilloscope. A 100000 point sample length (40 µs at 2.5 GS/s) was selected to allow the entire double pulse waveform to be captured. A B-trigger was used to

centre the captured waveform at the switching instant of interest: the second fall in drain-source voltage (turn-on under load current).

The bus voltage and ambient temperature for each test were additionally recorded using an Agilent U1241A multimeter.

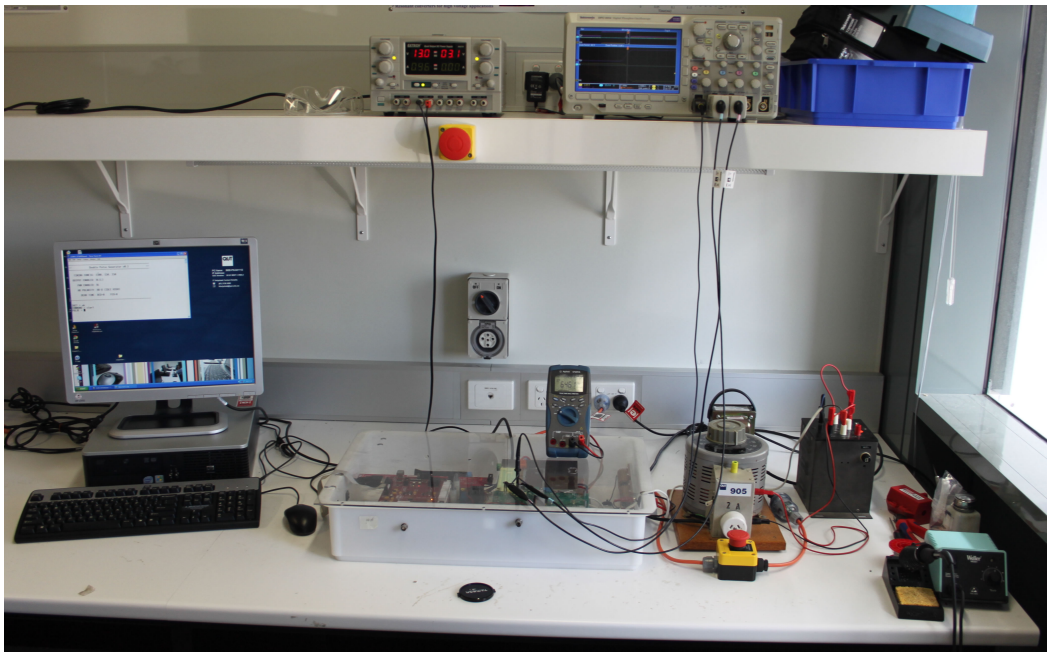


Figure 4.8: Photo of the experimental setup showing the test power supplies and instrumentation.

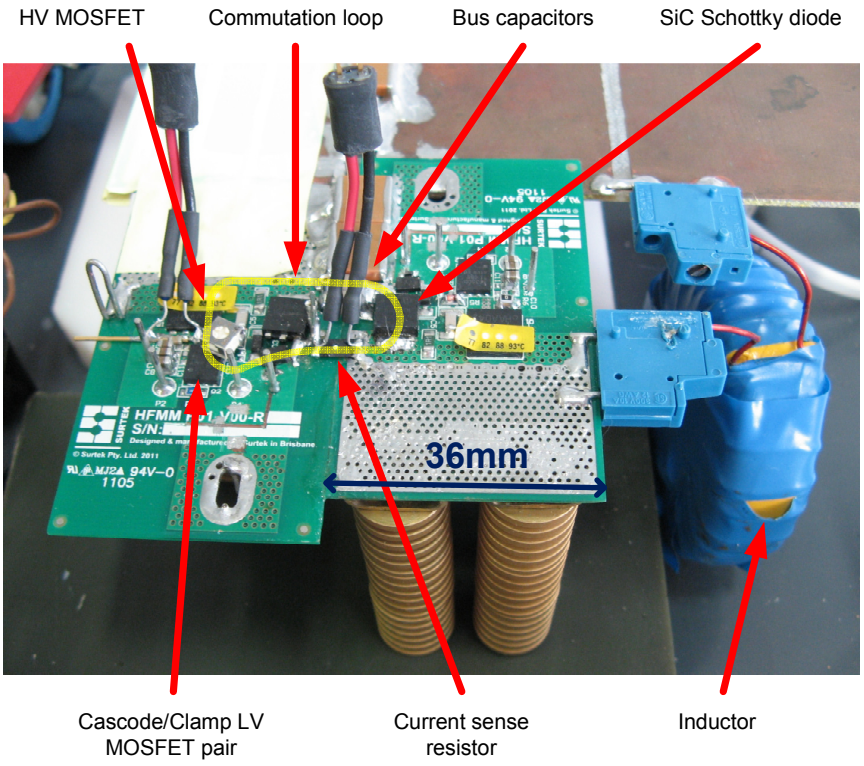


Figure 4.9: Photo of the experimental prototype showing key components.

4.4 Methodology

The cascode gate drive prototype was tested experimentally at 350 discrete operating points for various values of cascode MOSFET gate resistance (R_{gle}), high-voltage MOSFET gate-source capacitance (C_{gshe}) and load current (I_L). Table 4.1 below summarises the range of values over which each parameter was swept.

Parameter	**Values**
Cascode MOSFET gate resistance, R_{gle} (Ω)	100, 120, 150, 180 and 220
HV MOSFET gate-source capacitance, C_{gshe} (nF)	0.1, 1, 2, 4, 10, 20 and 40
Load current, I_L (A)	1, 2, 3, 4, 5, 6, 7, 8, 9 and 10

Table 4.1: Summary of experimental test parameter space.

For each combination of R_{gle} and C_{gshe} an initial calibration test was conducted at approximately 11 A load current; the results of this test were used to determine the double pulse timing (specifically the length of the first on pulse) to achieve the desired load currents for the subsequent tests.

A microcontroller (Texas Instruments TMS320F28355) was used to generate double-pulse switching signals with a 6.66 ns timing resolution. Double-pulse waveform timing was adjusted via a PC interface to the microcontroller over RS-232. While the timing of the first pulse was adjusted to set the load inductor current, the delay and second pulse timings were both fixed to 1 µs.

Tests were conducted at a bus voltage of 400 V_{DC}. For each test the switching waveforms (drain-source voltage, voltage across current sense resistor and gate-source voltage) were recorded via the oscilloscope. Post-processing of the waveforms was then conducted in MATLAB to reconstruct the true current from the current sense resistor voltage and to extract the desired switching performance metrics. These post-processing techniques are described in Appendices C and D respectively.

There were slight variations in the load currents achieved across all the experimental tests. Consequently, extracted experimental switching performance metrics across the (R_{gle}, C_{gshe}, I_L) parameter space were re-sampled onto a uniform grid composed of the parameter values given in Table 4.1, by linear interpolation. The goal of this process was to normalise the set experimental results to the same set of load currents. Experimental waveform data and extracted switching features for all tests are provided as an attachment with the digital copy of this thesis.

4.5 Results

4.5.1 Summary of the experimental prototype performance

4.5.1.1 Experimental result space

Summarised in Table 4.2 are the observed minimum and maximum for each switching performance metric across all experimental tests. The experimental tests performed cover a broad range of switching speeds and operating points, sufficient to describe the operation of the experimental prototype. Details of each individual test are available in the attached feature extraction reports which are indexed in Appendix F.

Switching performance metric	Units	Minimum	Maximum
Turn-on			
Switching loss	µJ	27	193
Maximum dv/dt	V/ns	23	59
Maximum di/dt	A/µs	97	563
Current rise time	ns	6	166
Voltage fall time	ns	8.4	20
Turn-on delay time	ns	38	192
Turn-on time	ns	49	206
Switching time	ns	27	207
Gate rise time	ns	70	281
Turn-off			
Switching loss	µJ	33	196
Maximum dv/dt	V/ns	2	25
Maximum di/dt	A/µs	7	192
Voltage rise time	ns	16	184
Current fall time	ns	107	408
Turn-off delay time	ns	26	116
Turn-off time	ns	42	299
Switching time	ns	110	307
Gate fall time	ns	11	32

Table 4.2: Summary of the bounds for each switching performance metric recorded over the experimental parameter space.

4.5.1.2 Fastest switching performance

The fastest switching speed was achieved with $R_{gle} = 100\,\Omega$ and $C_{gshe} = 40\,\text{nF}$. Table 4.3 summarises the observed switching performance metrics with these control parameters at a nominal load current of 10 A. For comparison the manufacturer reported performance characteristics are also presented (conventional gate drive, $I_L = 9.9\,\text{A}$, $R_g = 3.3\,\Omega$).

It should be noted that achieving very high switching speeds was not the primary focus of this work, but rather, investigation of the switching characteristics and control mechanisms of the cascode gate drive configuration. The maximum

switching speed at which the cascode gate drive was demonstrated was lower than the test condition presented by the manufacturer on the datasheet, however, it should be noted that for many practical applications, the datasheet test conditions do not represent the typical operating point. For this work, comparison with the manufacturer reported switching characteristics is not particularly useful.

The switching waveforms for this case are presented in Figure 4.10. Firstly, note the shape of the gate-source voltage trace: the Miller plateau has been entirely eliminated and the rate of change of gate-source voltage appears close to linear. The gate is charged to full enhancement over an interval of approximately 125 ns – full enhancement is achieved less than 50 ns after the fall in drain-source voltage. This behaviour is distinctly different to that of a conventional gate drive and ensures the MOSFET channel is driven quickly to its minimum on-state voltage.

Note also that as the low-voltage cascode MOSFET is being driven by the drive IC (to 5 V), the peak drive current requirement from the driver IC is only 50 mA. Compare this with a resistor fed gate drive (say 3.3 Ω at 12 V, the datasheet test condition) which would require the drive IC to source a peak current exceeding 3.6 A. High peak current is delivered to the gate of the high-voltage MOSFET under cascode drive, however, this current is sourced directly from the bypass capacitors and is therefore not limited by the capability of a driver IC.

The drain current and drain-source waveforms appear clean. Approximately 4 A of overshoot (40 %) is observed for the drain current, which can be attributed to the charging currents of the opposing Schottky diode and RC snubbers (see Section 4.3.3) present on the experimental prototype.

4.5.2 The (R_{gle}, C_{gshe}) parameter space

4.5.2.1 Turn-on switching losses

Firstly, the turn-on switching loss result surfaces over the (R_{gle}, C_{gshe}) parameter space are presented. Figure 4.14 shows the turn-on switching loss result surfaces from three different perspectives. The plot has been annotated with Trajectories H–K. Trajectories H and J are trajectories of changing R_{gle} for constant values of C_{gshe} of 100 pF and 40 nF respectively. Trajectories I and K are trajectories of changing C_{gshe} for constant values of R_{gle} of 220 Ω and 100 Ω respectively. The surface and trajectories shown in Figure 4.14 are traditionally shown as a contour plot in Figure 4.13.

Trajectory H represents the typical approach for controlling the switching speed of cascode gate drive: adjusting the cascode MOSFET gate-source re-

Switching performance metric	Units	Value	Datasheet Values
Turn-on			
Switching loss	µJ	74	–
Maximum dv/dt	V/ns	59	(>64)
Maximum di/dt	A/µs	563	(>990)
Current rise time	ns	19	–
Voltage fall time	ns	13	5
Turn-on delay time	ns	48	10
Turn-on time	ns	61	(15)
Switching time	ns	32	–
Gate rise time	ns	85	–
Turn-off			
Switching loss	µJ	178	–
Maximum dv/dt	V/ns	24	(>64)
Maximum di/dt	A/µs	167	–
Voltage rise time	ns	17	5
Current fall time	ns	118	–
Turn-off delay time	ns	34	50
Turn-off time	ns	51	55
Switching time	ns	122	–
Gate fall time	ns	21	–

Table 4.3: Summary of fastest switching performance of the experimental prototype. Manufacturer reported switching characteristics [56] for a conventional gate drive are provided for comparison; parentheses indicate a value was derived rather than directly reported on the datasheet by the manufacturer.

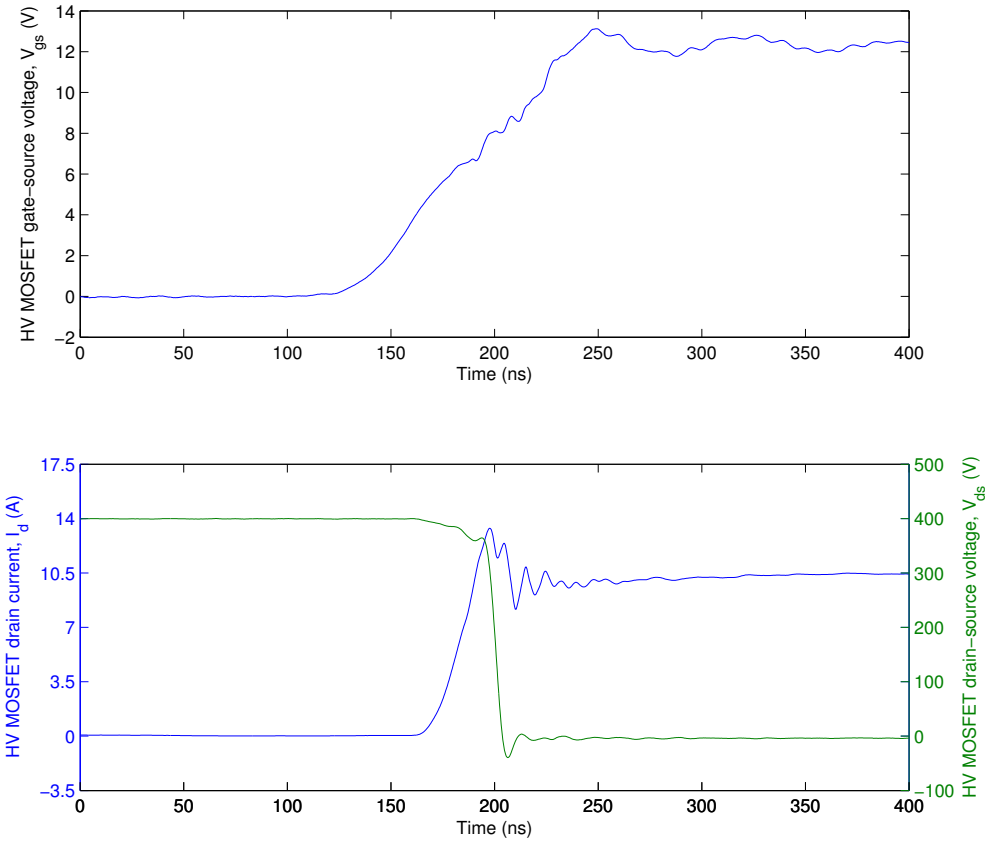


Figure 4.10: Turn-on switching waveforms for the experimental prototype operating at $I_L = 10\,\text{A}$ with $R_{gle} = 100\,\Omega$ and $C_{gshe} = 40\,\text{nF}$.

sistance with no additional gate-source capacitance added to the high-voltage MOSFET (100 pF is negligible compared with the parasitic gate-source capacitance of the device). It is clearly evident that decreasing values of R_{gle} result in reduced turn-on losses; for Trajectory H (see Fig. 4.14b) we see a reduction in switching losses from 191 µJ to 104 µJ (46 %) for a decrease in R_{gle} from 220 Ω to 100 Ω (55 %). This is the expected result given that reduced gate-resistance values should lead to increase turn-on switching speeds.

Next we consider the effect of the second parameter, C_{gshe}. Trajectory I shows the effect of increasing the value of C_{gshe} while holding R_{gle} constant at 100 Ω (see Fig. 4.14c). Relatively little change is observed of the 100 pF–10 nF range, however, between 10–40 nF a substantial reduction in the turn-on switching losses are observed. For a increase in C_{gshe} from 100 pF to 40 nF, a decrease in switching losses from 104 µJ to 73 µJ (30 %) is observed. It is worth noting that the additional gate drive losses resulting from the increase in C_{gshe} to 40 nF would be on the order of 3 µJ, that is, there is still a substantial net saving in total losses.

From Figure 4.14c it can be seen that across the entire range of R_{gle} values tested this behaviour was consistent: as the value of C_{gshe} was increased a reduction in turn-on switching losses was observed. The effect was smaller for higher values of R_{gle}. Considering Trajectory K ($R_{gle} = 220\,\Omega$), for example, a reduction in switching losses from 191 µJ to 169 µJ (12 %) was observed as C_{gshe} was increased to 40 nF.

The turn-on switching loss result surface is additionally presented as a contour plot in Figure 4.14, including Trajectories H–K corresponding to Figure 4.14. Figure 4.14 provides a good summary of the turn-on loss behaviour across the (R_{gle}, C_{gshe}) and will subsequently be used as a reference when investigating other switching metrics. It should also be noted that the characteristic shape of the experimental turn-on loss surface compares well with the simulated loss surfaces (see Fig. 3.12).

4.5.2.2 dv/dt sensitivity

Figure 4.15 shows the experimental maximum dv/dt result surface plotted over the (R_{gle}, C_{gshe}) parameter space for $I_L = 10$ A, with the corresponding turn-on loss contours. Firstly we note that the maximum dv/dt surface is relatively "noisy" compared with other experimental or simulated result surfaces, particularly for values of R_{gle} below 150 Ω. This can be attributed to the difficulty in extracting the maxima of the time derivative from experimental waveform data of limited resolution. Additional we note that the relative change in magnitude of the maximum dv/dt is quite small over the experimental parameter space (between 50–58 V/ns for $R_{gle} < 150\,\Omega$).

While the experimental data are relatively noisy, it is still possible to discern the characteristic shape of the maximum dv/dt result surface, particularly for higher values of R_{gle} and C_{gshe}. From Figure 4.15 we see that as R_{gle} is decreased the maximum observed dv/dt during the switching transient increases, as expected. This behaviour is clearly evident in the transient switching waveforms presented in Figure 4.17: with decreasing values of R_{gle} there is an appreciable change in the slope of fall in drain-source voltage. Additionally the maximum undershoot of the drain-source voltage increases.

Next let us consider the effect of changing C_{gshe}. For $R_{gle} > 150\,\Omega$, Figure 4.15 shows that as C_{gshe} is increased the maximum observed dv/dt actually decreases. The corresponding loss contours, however, indicate that the decrease in maximum dv/dt does not result in increased switching losses (as outlined in the previous section, switching losses decrease with increasing C_{gshe}).

For $R_{gle} < 150\,\Omega$ the effect of increasing C_{gshe} on maximum dv/dt is less apparent. Figure 4.16b provides a different visualisation of the maximum dv/dt result surface. For $R_{gle} \geq 150\,\Omega$ the trend outlined above is apparent. For R_{gle} $= 120\,\Omega$ there appears to be a change in behaviour. The trend of the 20 nF and 40 nF lines looks reasonable and indicates that for higher capacitances we may see an increase in dv/dt as we continue to decrease R_{gle} and increase C_{gshe}. The (120 Ω, 1 nF) data-point appears as though it may be an outlier, given the trends of the 100 pF and 10 nF lines. This outlier may potentially be an artefact of the feature extraction process.

The change in maximum dv/dt behaviour observed for lower values of R_{gle} and higher values of C_{gshe} is consistent with the results obtained by simulation (see Fig. 3.14), where a boundary in the parameter space was observed beyond which increases in C_{gshe} resulted in an increase in maximum dv/dt (rather than decease). Higher resolution experimental data would need to be collected to better define this boundary experimentally.

4.5.2.3 di/dt sensitivity

Figure 4.15 additionally shows the experimental maximum and average di/dt result surfaces plotted over the (R_{gle}, C_{gshe}) parameter space for $I_L = 10\,\text{A}$, with the corresponding turn-on loss contours. Again we firstly consider the effect of R_{gsle}. From Figure 4.15 we see that as R_{gle} is decreased the maximum di/dt during the switching transient also increases, as expected. This behaviour is observed in the transient switching waveforms presented in Figure 4.17: with decreasing values of R_{gle} there is an appreciable change in the maximum slope of the drain current, around the peak drain current. From the transient waveforms it is also evident that the change in the drain current transient is the primary

source of the switching loss reduction (the area under the drain current trace is representative of the energy dissipated in the switching device).

Next we consider the effect of changing C_{gshe} in the maximum di/dt. From Figure 4.15 it can be see that over a large proportion of the parameter space (typically $C_{gshe} \leq 10\,\text{nF}$), maximum d$i$/dt remains relatively constant/insensitive to increases in C_{gshe}. Within this region, then, is it possible to affect a change in maximum dv/dt or turn-on losses without affecting the maximum di/dt. The transient plots in Figure 4.18 provide a good illustration of this phenomenon: for increasing values of C_{gshe} these is no observable change in the maximum slope of the drain current but the leading edge of the drain current transient is "sharper" resulting in reduced switching losses.

This behaviour is captured by the average di/dt metric, also presented in Figure 4.15. Note that as C_{gshe} is increased it is possible to traverse the average di/dt contours while maximum di/dt is held constant. Figures 4.16c and 4.16d also provided a good visualisation of this behaviour. In Figure 4.16c it can be seen that the curves for $C_{gshe} \leq 20\,\text{nF}$ track closely (no change in maximum di/dt) while in Figure 4.16d the corresponding curves are separated, indicating an increase in average di/dt.

Figure 4.16c also provides a good visualisation of the change in behaviour for higher values of C_{gshe}. Note that for the 40 nF line the change in C_{gshe} (from 100 pF) results in *decreased* maximum di/dt for high values of R_{gle} but *increased* maximum di/dt for $R_{gle} \leq 150\,\Omega$. Again, this behaviour is consistent with the shape of the result surfaces observed in simulation.

4.5.2.4 Gate-source voltage characteristics

Figure 4.19 presents the gate-source voltage waveforms for the experimental prototype operating with $R_{gle} = 100\,\Omega$ with different values of C_{gshe}. Corresponding drain current and drain-source voltage waveforms are additionally presented.

Figure 4.19 shows the gate-source voltage waveform under operation with negligible additional gate-source capacitance (100 pF). The plot is annotated with four time intervals, T_A-T_D, which delineate the four key phases of the turn-on process. Interval T_A shows the initial charging of the HV MOSFET gate from 0 V to the threshold voltage. Interval T_B corresponds to the rise in drain current to the point at which the load inductor current is fully supported by the HV power MOSFET. Interval T_C corresponds to the fall in drain-source voltage. Finally, interval T_D extends from the end of the fall in drain-source voltage to the point at which the gate is charged to the drive voltage, and hence, the HV MOSFET channel is fully enhanced.

Firstly, note that the gate-source voltage waveform is distinctly different from

that of a conventional gate drive, and instead corresponds well to the gate-source voltage waveforms presented in Section 3.4.2. The gate is charged quickly to the threshold voltage over interval T_A, with the gradient of the gate-source voltage increasing across interval T_A (rather than decaying exponentially as would be expected for a conventional gate drive).

Note that for higher values of R_{gle} (for example, see Fig. 4.17), the charging of the gate over this interval is more linear as the charging rate is limited by the Miller effect on the cascode MOSFET. Higher values of C_{gshe} modify the operating point of the cascode MOSFET (i.e. higher cascode MOSFET drain currents are required to achieve the same $\mathrm{d}v/\mathrm{dt}$ of the HV MOSFET gate-source voltage) which has three effects: 1) The initial rate of change of the HV MOSFET gate-source voltage is lower, and takes longer to increase, 2) the Miller-limited maximum gate-source $\mathrm{d}v/\mathrm{dt}$ takes longer to reach (and it may *not* be reached before the threshold voltage) and 3) the maximum gate-source $\mathrm{d}v/\mathrm{dt}$ is reduced due to the higher cascode MOSFET drain current (and consequently higher gate-source voltage), which results in a reduced Miller current on the cascode MOSFET. These effects can be seen by comparing the transient experimental waveforms documented for various R_{gle} and C_{gshe} trajectories in Appendix F.

Interval T_A ends at the point at which the HV MOSFET gate-source voltage reaches the threshold voltage, and hence, the HV MOSFET begins conducting. A distinct change in the gradient of the gate-source voltage is observed at this point, extending throughout interval T_B. This can be attributed to the need of the cascode MOSFET to conduct the load current; as the HV MOSFET drain-current increases the net cascode MOSFET drain current available to continue the charging the gate of the HV MOSFET is reduced. Consequently the rate of change of gate-source voltage during the drain-current rise time is substantially reduced and is largely controlled by the value of R_{gle}. This can be clearly seen in Figures 4.17 and 4.18; in Figure 4.17 there is an increase in the gate-source $\mathrm{d}v/\mathrm{dt}$ during the drain current transition for decreasing values of R_{gle}. Conversely where R_{gle} is held constant, as in Figure 4.18, the gate-source voltage waveforms converge to the same trajectory during the drain current transition, regardless of the value of C_{gshe}.

This behaviour is effected to some extent by the value of C_{gshe}, in so much as the relative magnitudes of the gate charging current (higher for increasing values of C_{gshe}) and load currents will effect the trajectory of the gate-source voltage during the drain current transitions. Specifically, when the gate charging current is higher, the net current available to continue charging the gate once the HV MOSFET begins conducting is also higher, allowing the gate to be charged more rapidly. This additional charging current is available transiently, and hence, is

tightly coupled to the trajectory of the drain current transition. This mechanism is proposed as the cause for the increase in maximum $\mathrm{d}i/\mathrm{dt}$ that is observed for C_{gshe} values above a certain threshold (which is dependent on R_{gle}). This phenomenon can be observed in Figure F.8, where it can be seen that for increasing values of C_{gshe} the gate-source voltage overshoots the gate-source voltage trajectories for lower C_{gshe} values; the maximum $\mathrm{d}i/\mathrm{dt}$ metric, however, is only effected in the cases where the overshoot coincides with maximum $\mathrm{d}i/\mathrm{dt}$ point, around $C_{gshe} \geq 20\,\mathrm{nF}$ (typically at the instant that the load inductor current is fully supported by the HV MOSFET).

Interval T_C corresponds to the fall in drain-source voltage, which begins at the instant that the full inductor load current is supported by the HV MOSFET. Note that during this interval the drain current overshoots I_L. This should not be mistaken as reverse recovery current (which would occur *before* the fall in drain-source voltage, not concurrently), but is rather due to the charging of the opposing Schottky diode junction capacitance plus the RC snubber capacitance.

The gate-source voltage waveform during interval T_C is distinctly different from that of a conventional gate drive. For a conventional gate drive we would expect to see the Miller plateau over this interval, and extending well past the bulk-change in drain-source voltage. Additionally, we would expect to see a long decay time from lower drain-source voltages ($v_{ds} < 50\,\mathrm{V}$) to the minimum on-state voltage due to the non-linear nature of the gate-drain capacitance and the Miller effect. Instead, for the cascode gate drive there is no evidence of a Miller plateau and the gate-source voltage continues to increase during the fall in drain-source voltage. The drain-source voltage falls quickly to the minimum on-state voltage; there is no evidence that the Miller effect and non-linear gate-drain capacitance play a significant role in the fall of drain-source voltage for $v_{ds} < 50\,\mathrm{V}$. This behaviour is expected given that there is no gate resistor to limit the current delivered to the gate; the cascode MOSFET can supply both the Miller current plus gate charge current during drain-source voltage transition.

From Figure 4.17 it can be seen that the rate of change of the gate-source voltage during the drain-source voltage transition is dependent on the value of R_{gle}, with decreasing values of R_{gle} resulting in faster charging of the gate and hence, higher drain-source $\mathrm{d}v/\mathrm{dt}$. The effect of increasing C_{gshe} is less apparent; from the $\mathrm{d}v/\mathrm{dt}$ surfaces (see Fig. 4.15), however, for a substantial portion of the parameter space a decrease in the maximum $\mathrm{d}v/\mathrm{dt}$ is observed for increasing values of C_{gshe}. This behaviour is somewhat intuitive, given that we would expect the rate at which the gate is charged to be decreased though the addition of additional external gate-source capacitance. For high values of C_{gshe} an increase in maximum $\mathrm{d}v/\mathrm{dt}$ is observed. This phenomenon could be attributed to the

same mechanism described above for the di/dt characteristics: adding additional gate-source capacitance changes the operating point of the cascode MOSFET during interval T_C, resulting in higher net gate current being available to charge the gate more quickly.

Finally, we consider interval T_D, which corresponds to the charging of the HV MOSFET gate to the drive voltage, and hence, the minimisation of the on-state voltage drop across the MOSFET by fully enhancing the channel. Firstly it should be noted that this transition is extremely fast compared with a conventional gate drive, due to the absence of the exponential RC charging characteristic inherent in a conventional gate drive. For the drive case shown in Figure 4.19a, interval T_D extends for less than 50 ns. Bringing the gate-source voltage more quickly to its maximum has the added advantage of driving the MOSFET away from the active region, providing greater immunity to drain-voltage events (for which a potential positive feedback mechanism exists via the parasitic gate-drain capacitance).

From Figure 4.17 it can be see that reducing the value of R_{gle} results in the MOSFET gate being drive through interval T_D more rapidly. The effect of increasing C_{gshe} is less apparent, and given there is no drain current or drain-source voltage metric captured during this interval it is difficult to elucidate the sensitivity of the gate-source waveform to this parameter.

Figure 4.19b is included to demonstrate the changes to the characteristic shape of the gate-source waveform that can be affected by operation of the cascode gate drive across the (R_{gle}, C_{gshe}) parameter space. For the presented case the gate source waveform appears very close to linear over the turn-on switching transition, with the entire gate-charging process occurring within 125 ns.

4.5.3 Load current sensitivity

Some simulation-based evidence was presented in Section 3.8.4 that the worst-case switching performance in a cascode drive configuration may not always occur at the peak load current, particularly in terms of the maximum dv/dt metric. The implication of this finding was that the design process for a cascode gate drive in a practical application may be more complex if operating points across the entire load current range needed to be considered, rather than a few, identifiable worst-case operating points. A similar analysis is presented in this section to determine if the load current sensitivity present in the simulation data is also observable in the operation of the experimental prototype.

Figure 4.20 presents switching performance surfaces as a function of load current, I_L and cascode MOSFET gate resistance R_{gle} for two different values of C_{gshe}. Note that data for $I_L < 2$ A have been excluded as extracting switching

metrics from the experimental data was difficult at lower currents due to presence of transients in the load inductor current.

Figure 4.20b shows the result surfaces for negligible additional external gate-source capacitance (100 pF). For practical converter operation the trajectory of interest through the presented parameter space is a vertical line: changing load current for fixed R_{gle} and C_{gshe}. For any increasing load current trajectory through Figure 4.20b, the presented switching performance metrics are monotonically increasing, that is, maximum dv/dt, maximum di/dt and turn-on switching all increase with increasing load current. It can also be seen that each of these metrics is sensitive to load current for $C_{gshe} = 100\,\text{pF}$.

Alternatively consider Figure 4.20a. Firstly, it can be seen that increasing the value of C_{gshe} has substantially altered the shape of the switching performance surfaces. For these parameters maximum dv/dt is now largely insensitive to load current changes, evidenced by the near-vertical contour lines. Maximum di/dt is also less sensitive to load current changes, particularly at higher load currents and values of R_{gle}.

To investigate this behaviour the data from Figure 4.20 are presented as a set of slices through the result space in Figures 4.21 and 4.22. Figure 4.22 clearly shows the insensitivity of the maximum dv/dt metric to changes in load current. It can also be seen from this plot that, while maximum dv/dt is not strictly monotonically increasing with increasing load current, there are no substantial increases in maximum dv/dt as load current is decreased; the peak load current can be taken as a reasonable representation of the worst-case operating point.

It is also interesting to compare the maximum dv/dt characteristics presented in Figures 4.21 and 4.22. Note that for $C_{gshe} = 40\,\text{nF}$ the observed maximum dv/dt is typically lower than the $C_{gshe} = 100\,\text{pF}$ case for high load currents but higher in the $C_{gshe} = 100\,\text{pF}$ case for low load currents.

The maximum di/dt curves in both cases are strictly monotonic for increasing load current, and in the $C_{gshe} = 40\,\text{nF}$ case, for higher values of R_{gle}, an insensitivity to changes in load current can be observed.

It may be possible to leverage these load current dependent characteristics for improved converter operation in a particular application (e.g. increase C_{gshe} to reduce losses at the expense of higher maximum dv/dt at lower load currents), however, this analysis requires specific knowledge of the operating points/load cycles for an application and is therefore outside the scope of this work. The experimental results do show, however, that in the case of the maximum di/dt, maximum dv/dt and turn-on loss metrics, it is suitable to select the peak load current as representative of the worst-case operating point for the purposes of design.

4.5.4 Turn-off switching performance

This section documents the typical turn-off behaviour observed for the cascode gate drive hardware prototype. While the turn-off process of the cascode topology is not explored in detail in this work, experimental data were recorded for all turn-off transitions across the explored parameter space. The aim of this section is to present practical evidence of the operation of the active gate clamp, and its influence on the turn-off process. Readers should refer to the attached switching reports (see Section F.1) for detailed analysis of the turn-off switching performance.

Figure 4.11 shows the turn-off switching waveforms for load currents of 1–10 A with $R_{gle} = 220\,\Omega$ and $C_{gshe} = 10\,\text{nF}$. Note that due to the action of the active gate clamp, the discharge of the high-voltage MOSFET gate is independent of load current, with a fall-time of 12.8 ns across all load cases.

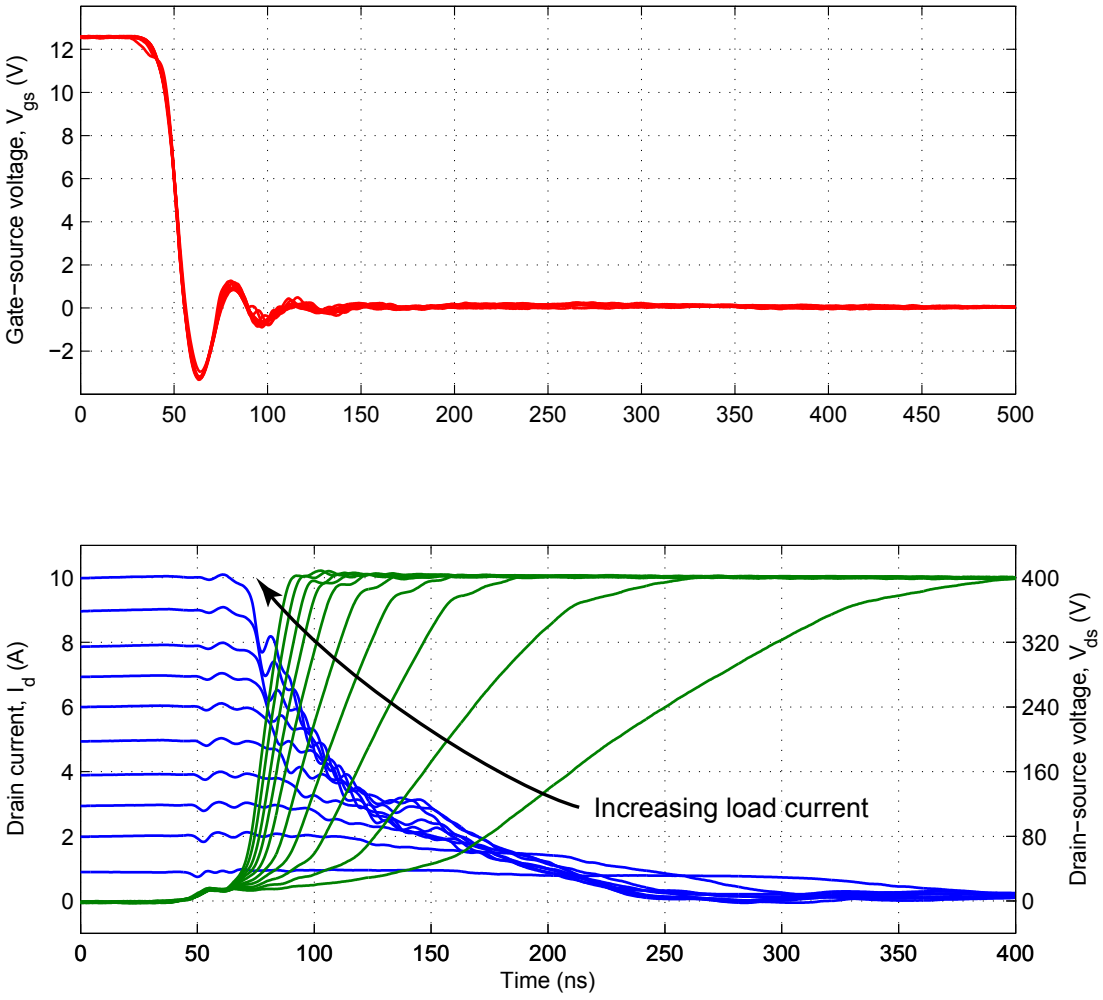


Figure 4.11: Turn-off switching waveforms for the experimental prototype operating at $I_L = 1$–$10\,\text{A}$ with $R_{gle} = 220\,\Omega$ and $C_{gshe} = 10\,\text{nF}$.

Conversely, the drain-source switching characteristics are highly load current dependent, due to the slew-rate of the drain-source voltage being driven by the charging/discharging of the parasitic capacitances by the load current. Note that for these operating points the high-voltage MOSFET gate-source voltage discharge profile plays no role in controlling the drain-source switching characteristics at turn-off; the discharge rate of the high-voltage MOSFET gate would need to be orders of magnitude slower to have any impact on the turn-off process.

Furthermore, across all 350 experimental operating points investigated and documented, the switching stresses (maximum $\mathrm{d}v/\mathrm{dt}$, maximum $\mathrm{d}i/\mathrm{dt}$) at turn-on were always higher than those observed at turn-off. Consequently, in a half-bridge configuration with minimal dead-time, the turn-on of the opposing device would result in a faster transition of the drain-source voltage and commutation of the load current.

These results confirm that the turn-on process presents the worst-case switching stresses for the cascode gate drive topology, and justifies the focus of this work on the optimisation of the turn-on process. The active gate clamp has been demonstrated to operate as expected, providing a fast discharge of the high-voltage MOSFET gate at turn-off, independent of load-current conditions. Additionally, for fast turn-off, the active gate clamp plays no role in controlling the drain-source switching characteristics, as these are dominated by time constants associated with the charge/discharge of parasitic capacitances by the load current.

4.6 Switching performance optimisation

The discussions in the preceding sections aim to highlight some of the characteristics of the cascode gate drive configuration when operated over the (R_{gle}, C_{gshe}) parameter space. The turn-on switching loss, $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}i/\mathrm{dt}$ performance metrics have been the primary focus. This section aims to demonstrate how the characteristics of cascode gate drive elucidated in the previous sections may be applied practically, for the purpose of optimising switching performance.

As an example we select an arbitrary turn-on switching loss constraint of 110 µJ and nominal load current of 10 A. In a real application such a constraint might be imposed by a loss budget for a converter. For a 10 kHz switching frequency (and assuming turn-off losses for the device are comparable) this would represent a total average dissipation of approximately 2.2 W for the device.

Given this loss constraint, it is desirable to minimise the transient voltage and current stresses on the device. It is also desirable to minimise $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}i/\mathrm{dt}$ from an EMI perspective.

The standard approach to this problem would be set the cascode MOSFET gate resistance, R_{gle}, to the highest value for which the loss constraint is satisfied, and accept the resulting $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}i/\mathrm{dt}$; based on the experimental data we would select $R_{gle} = 100\,\Omega$ (with $C_{gle} = 100$ pF, negligible additional capacitance). At this operating point we achieve a turn-on switching loss of 105 µJ, maximum $\mathrm{d}v/\mathrm{dt}$ of 58 V/ns and maximum $\mathrm{d}i/\mathrm{dt}$ of 420 A/µs (see feature extraction report #0312, Section F.1).

It is worth noting that the manufacturer specified rating for the $\mathrm{d}v/\mathrm{dt}$ ruggedness for the HV MOSFET used in the work is 50 V/ns. If this device were used in a half-bridge configuration at this operating point we would be violating this rating.

Based on the analysis presented in this thesis, however, we have access to a second degree of freedom: adding additional gate-source capacitance, C_{gshe}, to the HV MOSFET. We understand that in general, increasing the value of C_{gshe} tends to reduce the switching losses. To aid in the selection of an appropriate value for C_{gshe} we refer to the experimental turn-on switching loss surface, presented as a contour plot in Figure 4.12.

From the turn-on loss contour plot we select three additional candidate operating points within the (R_{gle}, C_{gshe}) parameter space. Note that as we increase the value of C_{gshe} it is possible to increase the value of R_{gle} while still meeting the 110 µJ loss constraint. A summary of the switching performance metric at each operating point is presented below in Table 4.4.

Note that the final operating point (152 Ω, 40 nF) results in a turn-on loss

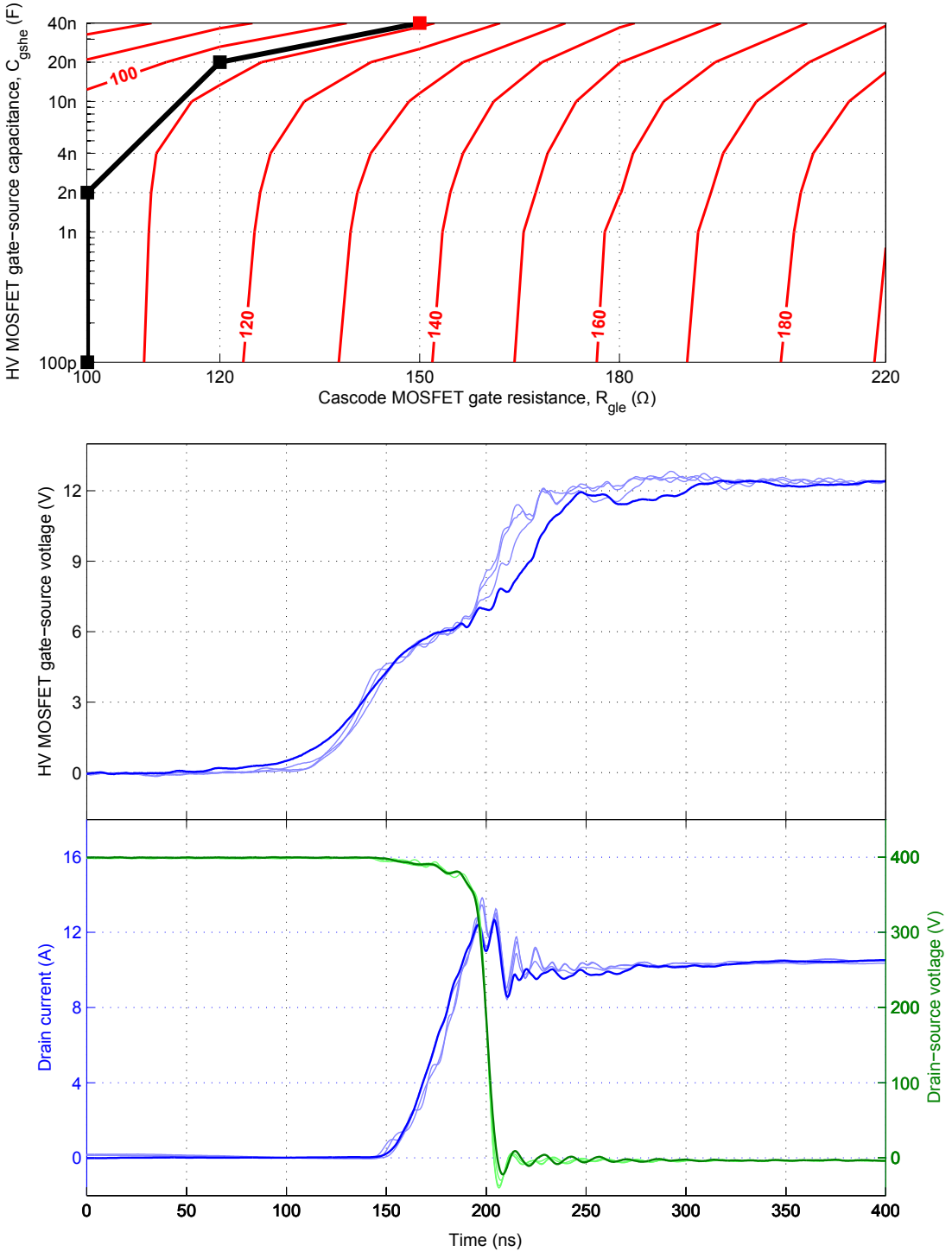


Figure 4.12: Various operating points over the (R_{gle}, C_{gshe}) parameter space given a turn-on loss constraint of 110 µJ. Transient switching waveforms are plotted for each operating point; the bold traces correspond to the optimum operating point indicated by the red data point in the turn-on loss contour plot.

R_{gle} (Ω)	C_{gshe} (nF)	Turn-on loss (µJ)	Max. dv/dt (V/ns)	Max. di/dt (A/µs)
100	0.1	105	58	420
100	2	105	56	420
119	20	108	48	330
152	40	111	43	360

Table 4.4: Summary of candidate operating points to address 110 µJ turn-on loss constraint.

that is marginally outside the 110 µJ target; we choose to include this operating point in the example for illustration purposes. This is also reasonable given that the experimental test was conducted at a slightly higher load current (10.1 A) and that in practice the gate resistance could be adjusted slightly to achieve the required loss target.

Table 4.4 illustrates that through control of both the R_{gle} and C_{gshe} parameters in combination it is possible to achieve a more optimum result than control of R_{gle} alone. Both the 119 Ω and 152 Ω operating points result in maximum dv/dt that is below the 50 V/ns ruggedness rating specified for the device. The 119 Ω operating point achieves the lowest maximum di/dt (330 A/µs) while the 152 Ω operating point achieves the lowest maximum dv/dt (43 V/ns); selection between these two operating points may depend on the relative benefit of decreasing these metrics.

It is also worth inspecting the experimental turn-on waveforms for each of these operating points; the waveforms corresponding to the 152 Ω operating point are shown bold. Considering the turn-on waveforms it should be noted that the 152 Ω operating point has some additional benefits, namely the lowest peak drain current and the lowest drain-source voltage undershoot during turn-on. There is also substantially less trailing-edge ring present in the drain current trace.

Some ancillary benefits of the alternative operating points are worth highlighting. Firstly, by increasing the value of R_{gle} the gate drive requirements of the cascode MOSFET are substantially reduced. For example with a 100 Ω gate resistance and 5 V drive voltage, the peak driver current requirement is 50 mA. By increasing the gate resistance to 152 Ω this requirement is reduced to 33 mA peak.

Secondly, adding additional external gate-source capacitance to the high-voltage MOSFET provides improved decoupling from parasitic-induced effects. For example, note that for the (100 Ω, 100 pF) operating point (see feature extraction report #0312, Section F.1) there are visible oscillations present in the gate-source voltage during turn-on. The magnitude of these oscillations does not seem to be a cause for concern, however, on inspection of the drain current trace we note that the oscillation of the gate-source voltage appear to be modulating

the drain current. The modulation of the drain current is additionally evidenced by oscillations in the drain-source voltage, most likely due to the presence of inductance in the drain current path.

In this case the oscillations appear to be tolerable. There exists a potential positive feedback mechanism via the gate-drain capacitance, however, which could, under different operating conditions, lead to undesirable ringing of drain current or drain-source voltage or, ultimately, failure of the switching device. Addition of a small amount of external gate-source capacitance (e.g the 100 Ω, 2 nF operating point, see feature extraction report #0334, Section F.1) largely eliminates this effect, as substantially more current must be injected into the gate in order to affect a change in gate-source voltage.

This exercise demonstrates that the characteristics of the cascode gate drive elucidated in this work can provide practical, "bankable" benefits in terms of switching performance. While this example focused on a loss constraint, a similar process could be used to optimise other metrics, such as minimising switching loss given maximum $\mathrm{d}v/\mathrm{dt}$ (based on MOSFET $\mathrm{d}v/\mathrm{dt}$ ruggedness) and maximum $\mathrm{d}i/\mathrm{dt}$ (based on EMI) constraints.

4.7 Conclusions

1. **The cascode MOSFET gate resistance, $\boldsymbol{R_{gle}}$**, is an effective mechanism for controlling switching speed. Sensitivity of all switching metrics to this parameter is high. In general, *decreasing* values of R_{gle} result in increased switching speeds and reduced switching losses.

2. **The high-voltage MOSFET gate-source capacitance, $\boldsymbol{C_{gshe}}$**, provides a second degree of freedom for controlling switching characteristics. In general, *increasing* values of C_{gshe} result in increased switching speeds and reduced switching losses.

3. **For high values of $\boldsymbol{R_{gle}}$**, increases to C_{gshe} result in a decrease in the observed maximum dv/dt during the switching transition.

4. **Average d$\boldsymbol{i}$/dt** of the switching transition can be increased by increasing the value of C_{gshe}.

5. **The maximum d$\boldsymbol{i}$/dt** is relatively insensitive to increases in C_{gshe} (up to a point).

6. **A boundary exists** within the (R_{gle}, C_{gshe}) parameter space beyond which increases in C_{gshe} result in increases to maximum dv/dt and di/dt during switching transients.

7. **The gate-source voltage waveform** for the cascode gate drive is distinctly different to that of a conventional gate drive. Charging time for the gate is substantially reduced with the Miller plateau and RC charging time constants eliminated. The characteristics of the gate-source voltage waveform can be mapped to the switching performance and mechanisms for the cascode gate drive topology.

8. It is suitable to take **the peak load current operating point** as representative of the worst-case expected maximum dv/dt, maximum di/dt and turn-on switching loss metrics for a cascode gate drive operating over the (R_{gle}, C_{gshe}) parameter space.

4.8 Experimental result figures

To aid in the presentation of this chapter, figures used to describe the characteristics and experimental performance of the cascode MOSFET drive configuration have been collected into this section. Figures are not necessary presented in the order they appear in-text, but are instead optimally placed to allow convenient figure-to-figure comparison by the reader.

Where possible, figures are accompanied by a self-contained captions such that readers may browse the collection of experimental results without needing to refer to the body of the chapter in order to interpret the figures. Back-references to relevant sections of the chapter body are also provided such that readers may easily locate in-depth analyses of each figure.

4.8.1 Turn-on switching loss surfaces

4.8.1.1 Contour plot

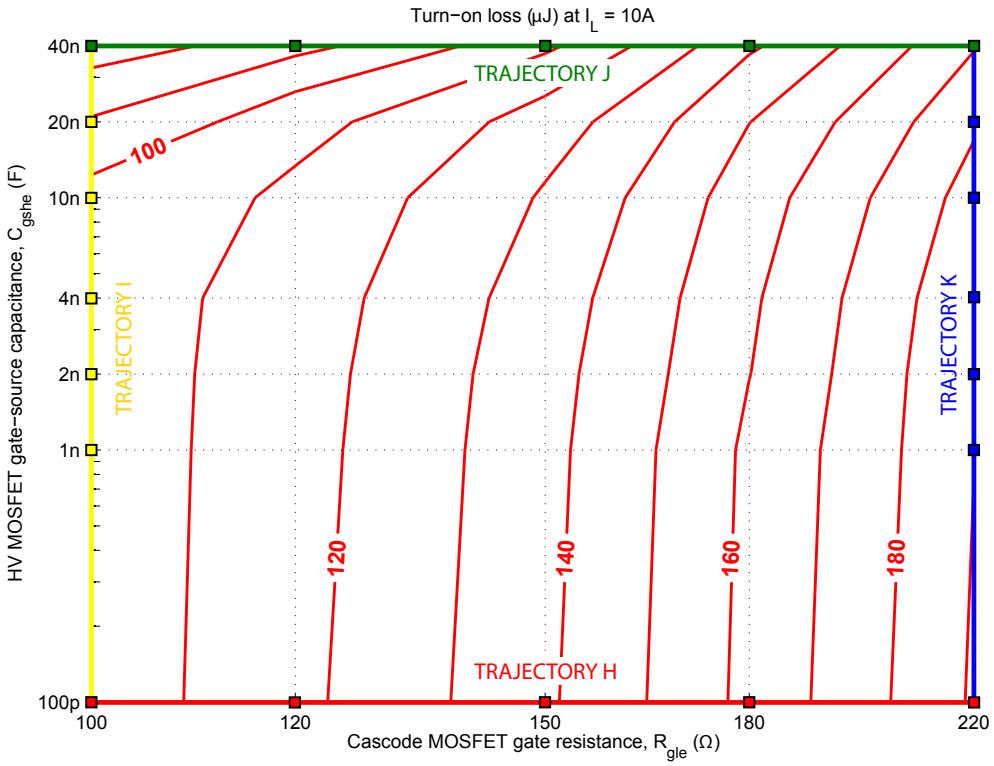


Figure 4.13: Turn-on switching loss experimental result surface shown as a contour plot for the nominal load current of 10 A. Trajectories H–K corresponding to Figure 4.14 are shown. Referenced on page 92.

4.8.1.2 Surface plot from three perspectives

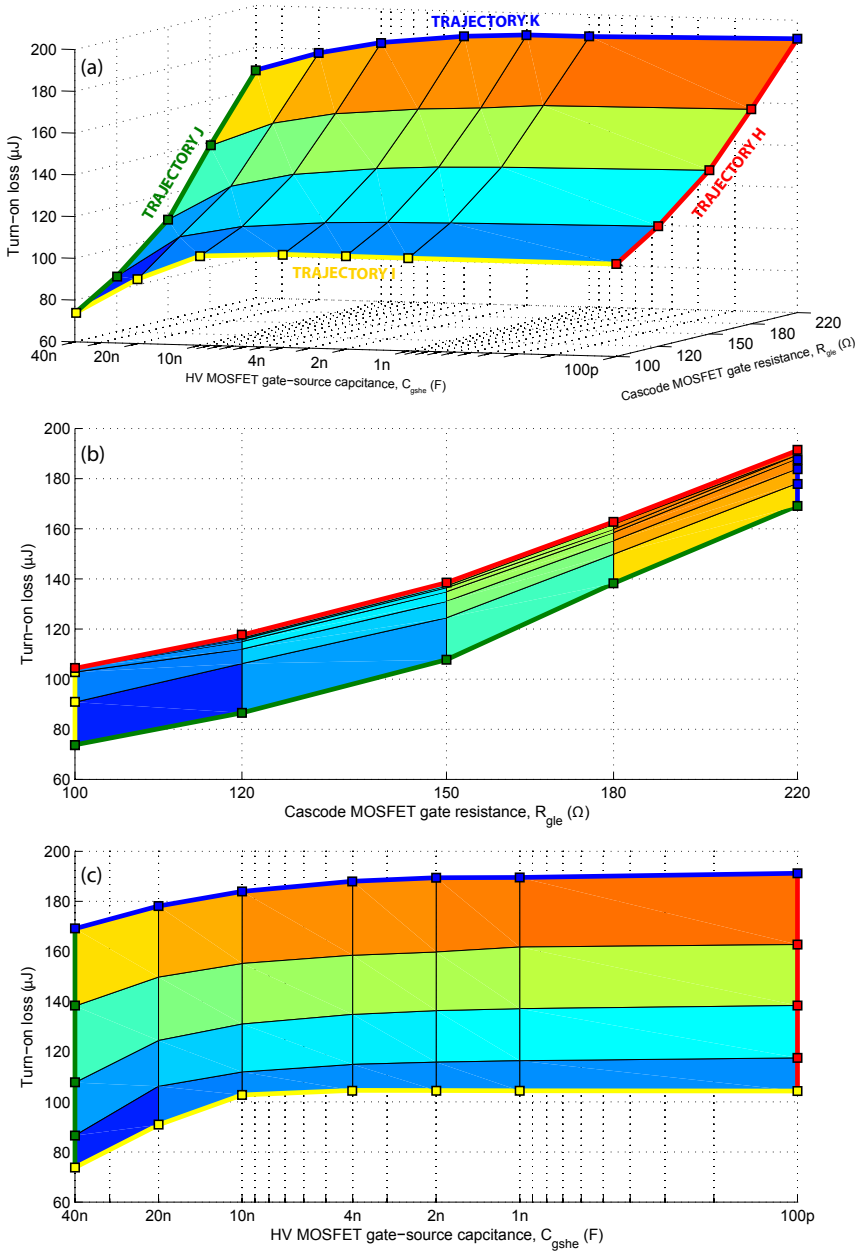


Figure 4.14: (a) Turn-on switching loss results surface for the nominal load current of 10 A, additionally shown with the view aligned to the (b) R_{gle} axis and (c) C_{gshe} axis. Referenced on pages 92, 94 and 108.

4.8.2 dv/dt and di/dt characteristics

4.8.2.1 Contour plots over the (R_{gle}, C_{gshe}) parameter space

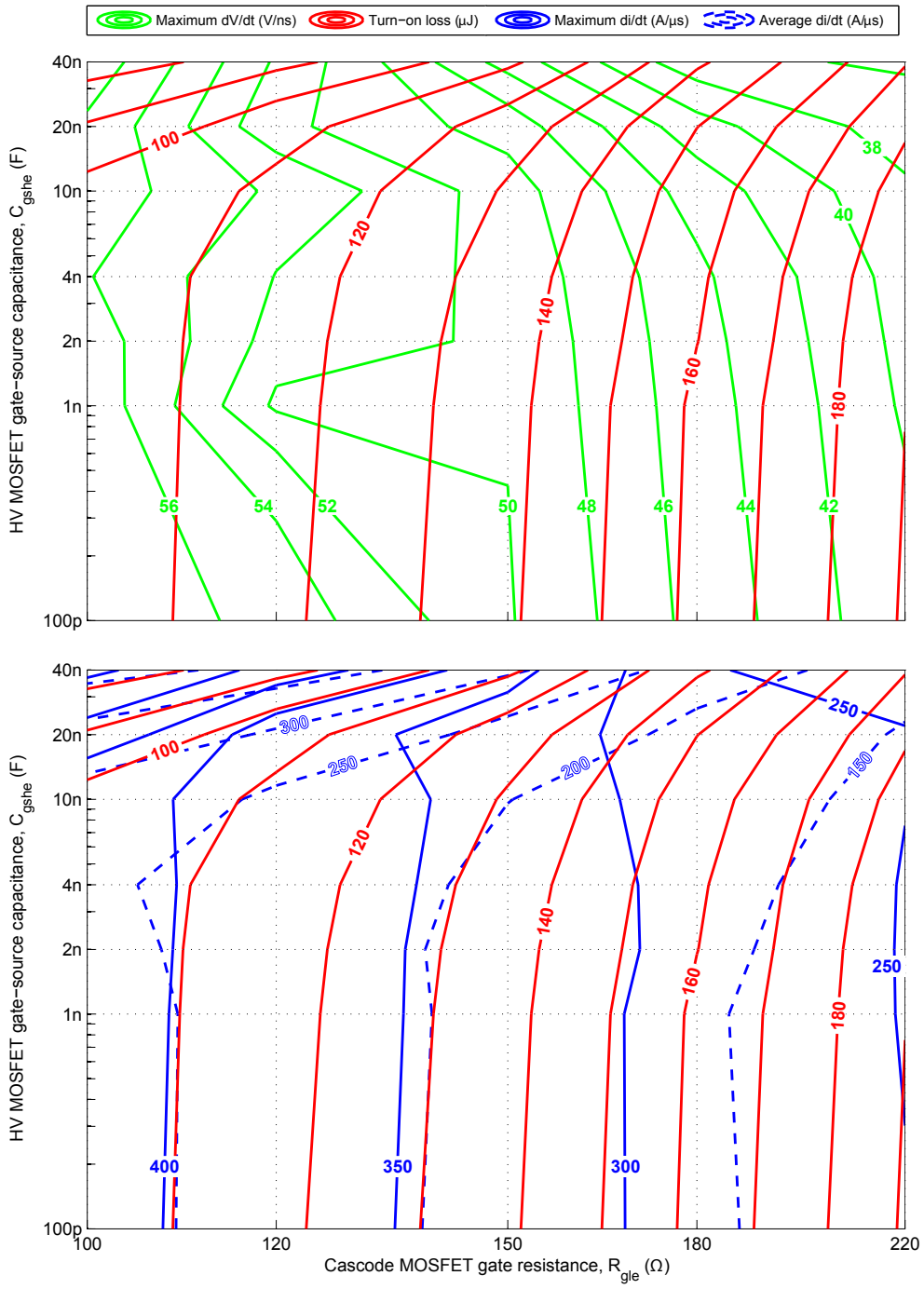


Figure 4.15: Switching performance surfaces presented as contour plots over the (R_{gle}, C_{gshe}) parameter space for the nominal load current of $I_L = 10\,\text{A}$. Referenced on pages 94 to 96 and 98.

4.8.2.2 Performance as a function of R_{gle} for constant C_{gshe} slices

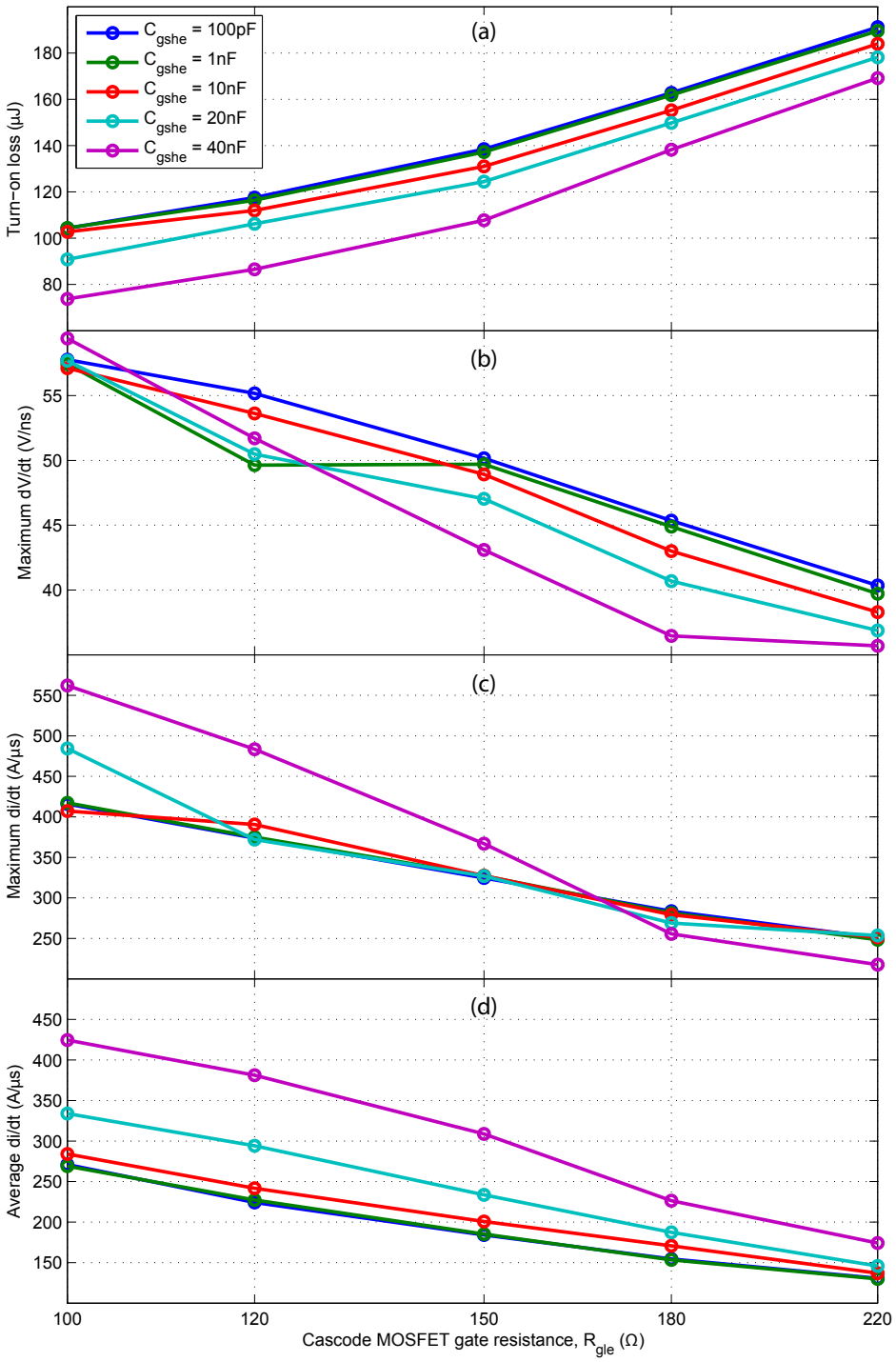


Figure 4.16: Turn-on switching metrics as a function of R_{gle} for various values of C_{gshe} (a) Turn-on loss. (b) Maximum dv/dt. (c) Maximum di/dt. (d) Average di/dt. Referenced on pages 95 and 96.

4.8.3 Turn-on switching waveforms

4.8.3.1 Performance as a function of R_{gle} for $C_{gshe} = 100\,\text{pF}$

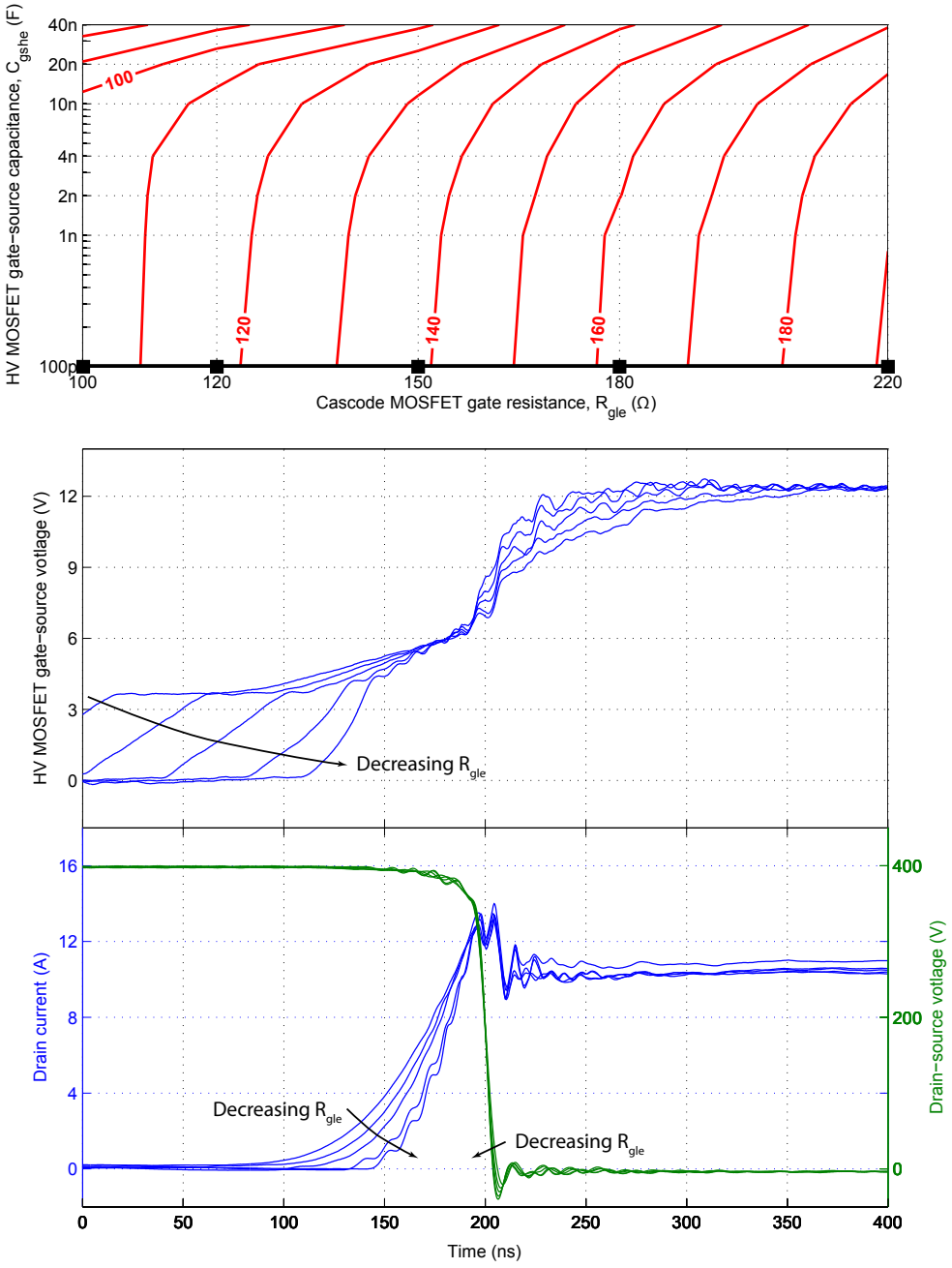


Figure 4.17: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 100\,\text{pF}$ and $I_L = 10\,\text{A}$. Referenced on pages 95 and 97 to 99.

4.8.3.2 Performance as a function of C_{gshe} for $R_{gle} = 182\,\Omega$

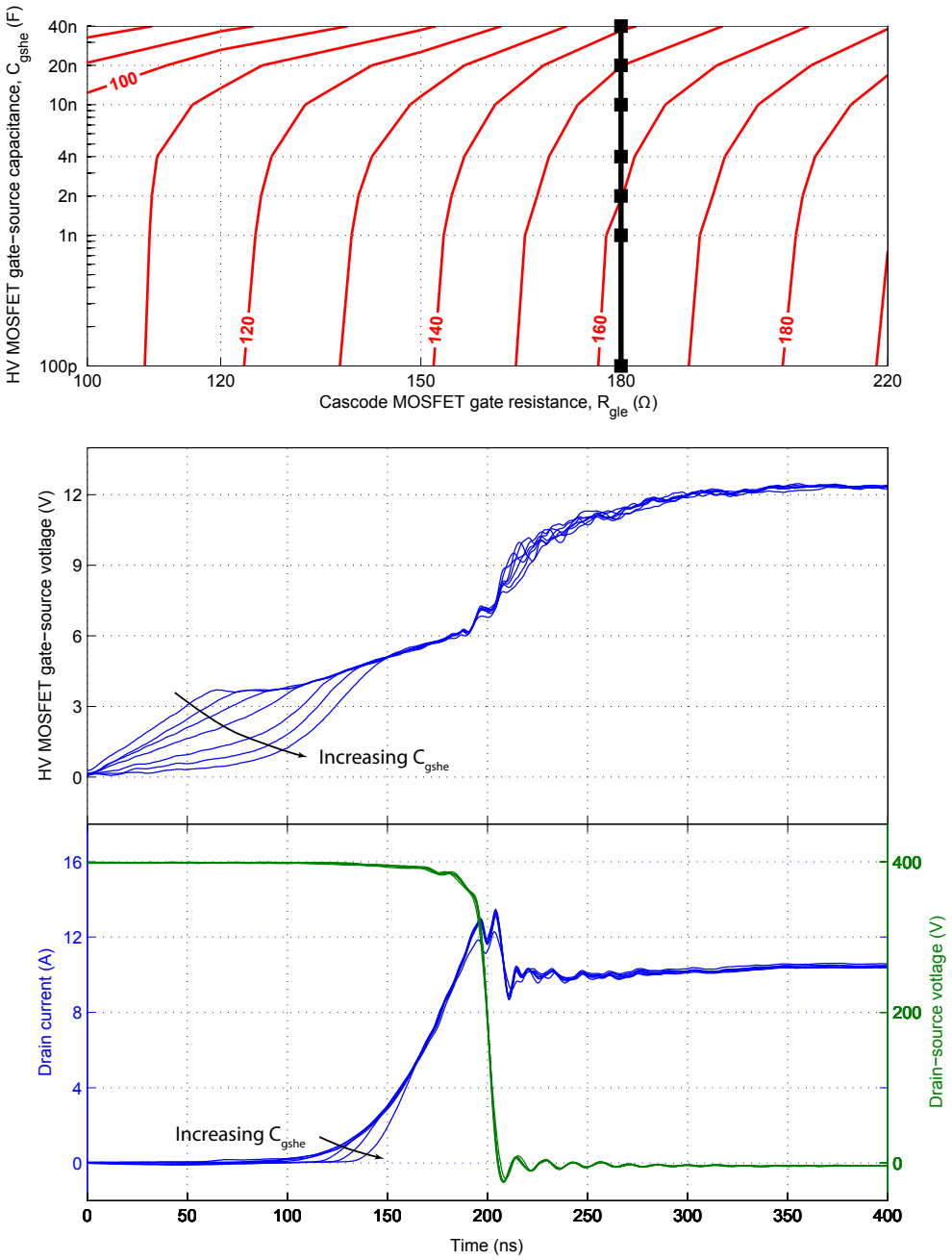


Figure 4.18: Experimental turn-on switching waveforms for a constant R_{gle} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100 pF–40 nF with $R_{gle} = 182\,\Omega$ and $I_L = 10$ A. Referenced on pages 96 and 97.

4.8.3.3 Gate-source voltage characteristics

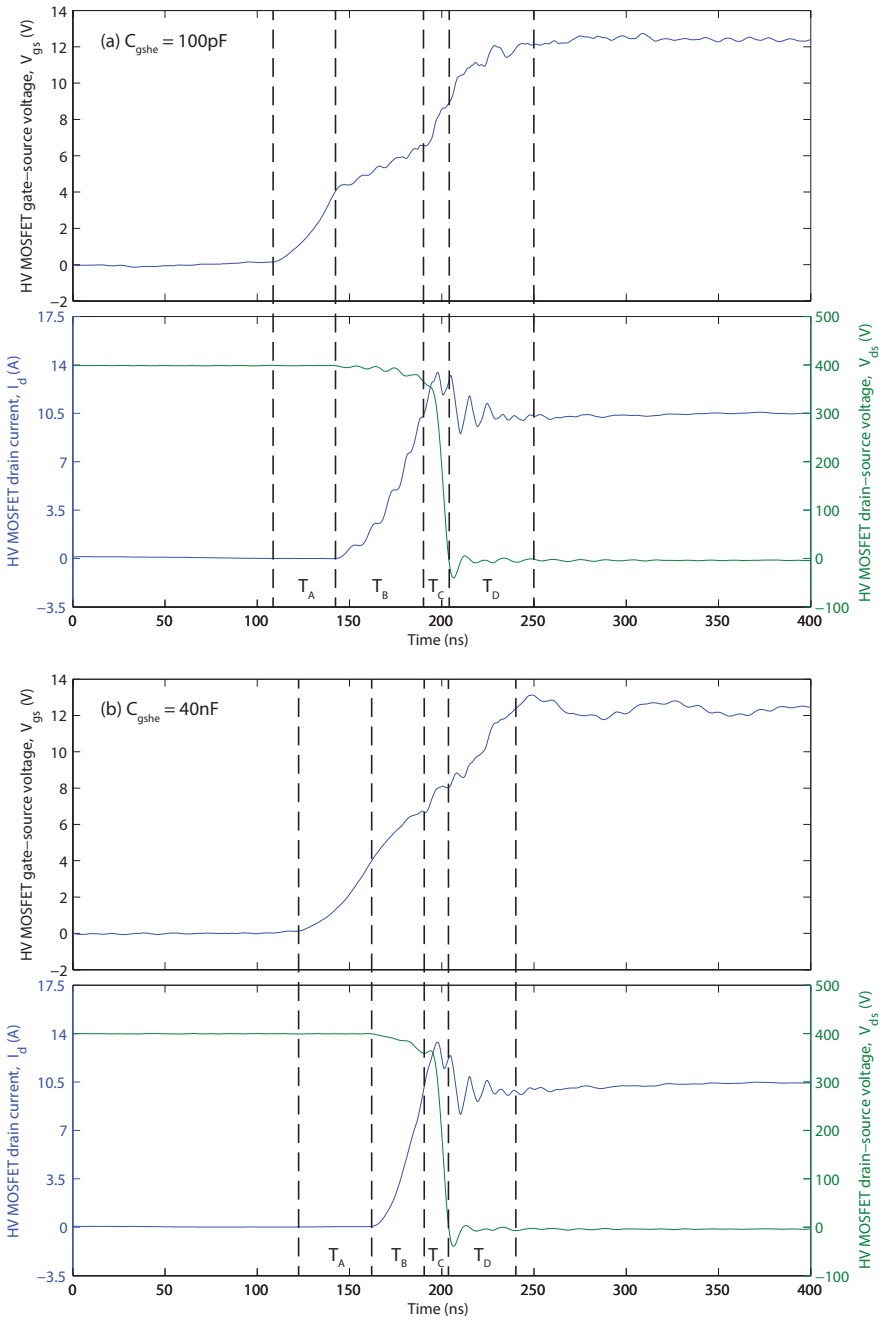


Figure 4.19: Experimental turn-on switching waveforms for $R_{gle} = 100\,\Omega$ with (a) $C_{gshe} = 100\,\text{pF}$ and (b) $C_{gshe} = 40\,\text{nF}$. Plots are annotated with intervals T_A-T_D which illustrate the various stages of the turn-on process and the corresponding segments of the gate-source voltage waveform: T_A – Turn-on delay; T_B – Drain-current rise; T_B – Drain-source voltage fall; and T_D – Full enhancement of MOSFET channel. Referenced on pages 96 and 99.

4.8.4 Load-current sensitivity

4.8.4.1 Contour plots over the (R_{gle}, I_L) parameter space

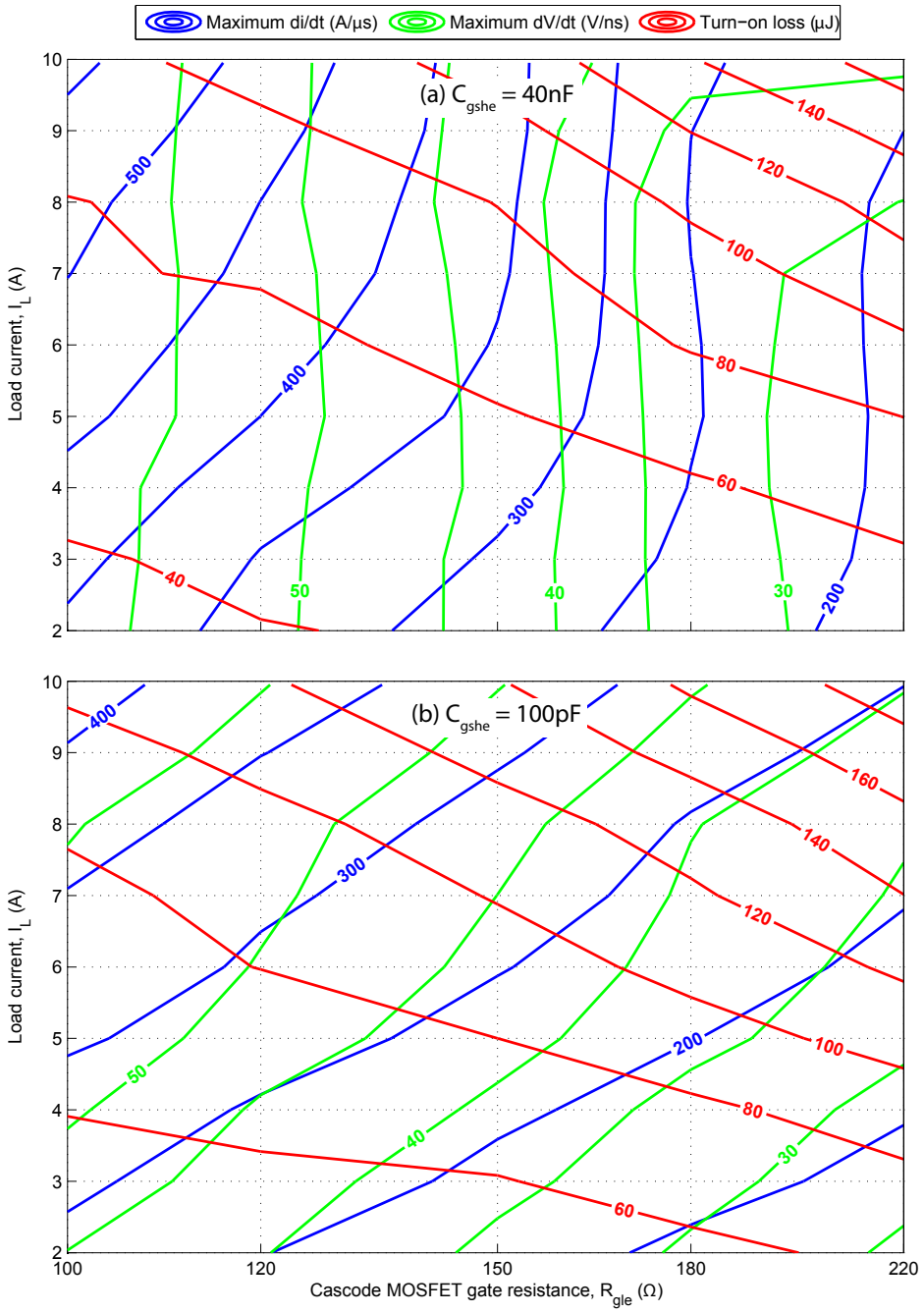


Figure 4.20: Turn-on loss, maximum dv/dt and maximum di/dt surfaces presented as contour plots over the (R_{gle}, I_L) parameter space to demonstrate the effect of load current on switching performance. Plots are provided for C_{gshe} values of (a) 40 nF and (b) 100 pF. Referenced on pages 99 and 100.

4.8.4.2 I_L sensitivity over constant R_{gle} slices for $C_{gshe} = 100\,\text{pF}$

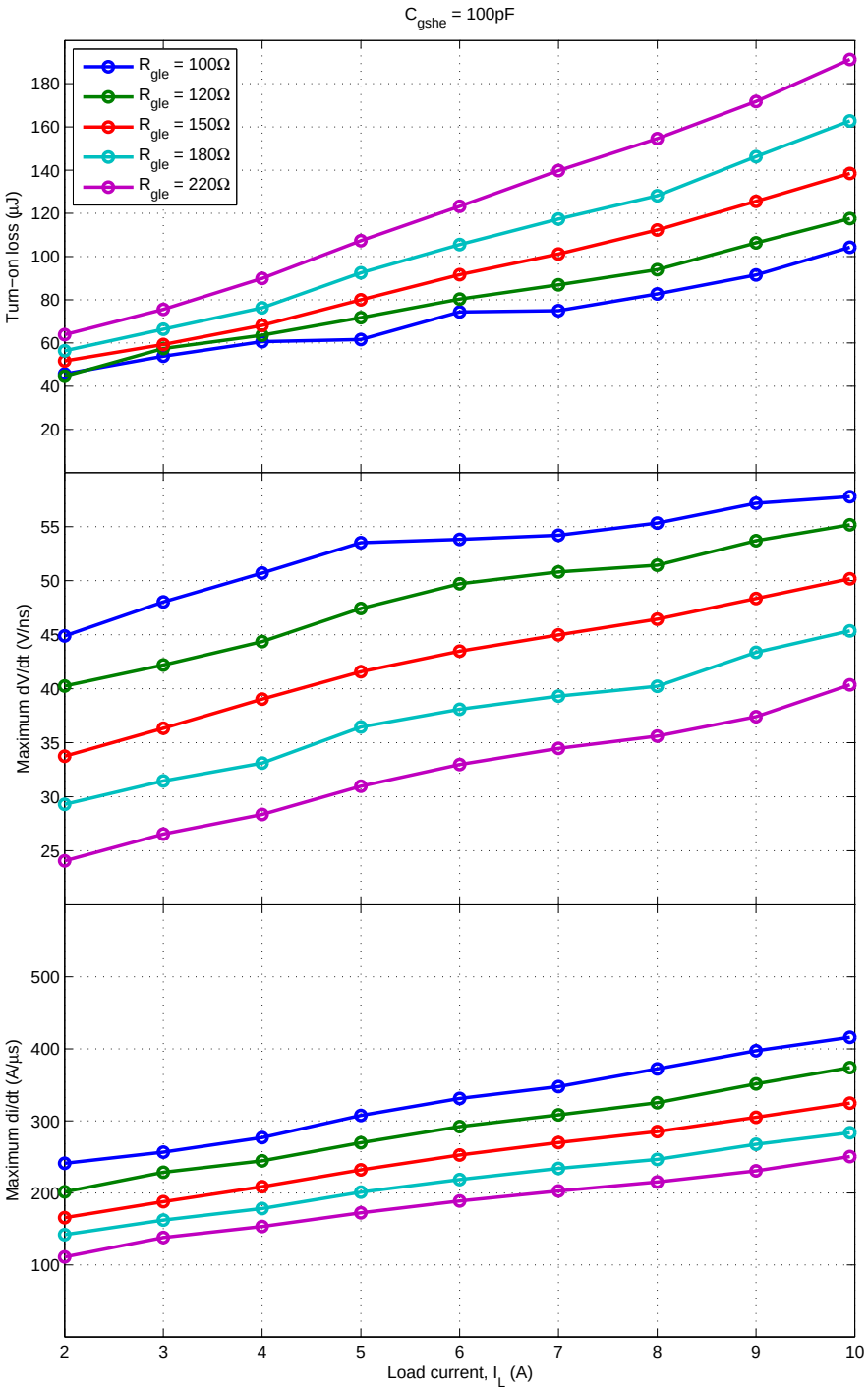


Figure 4.21: Turn-on loss, maximum dv/dt and maximum di/dt sensitivity to load current, I_L, for various values of R_{gle} with C_{gshe} fixed at 100 pF. Referenced on page 100.

4.8.4.3 I_L sensitivity over constant R_{gle} slices for $C_{gshe} = 40\,\text{nF}$

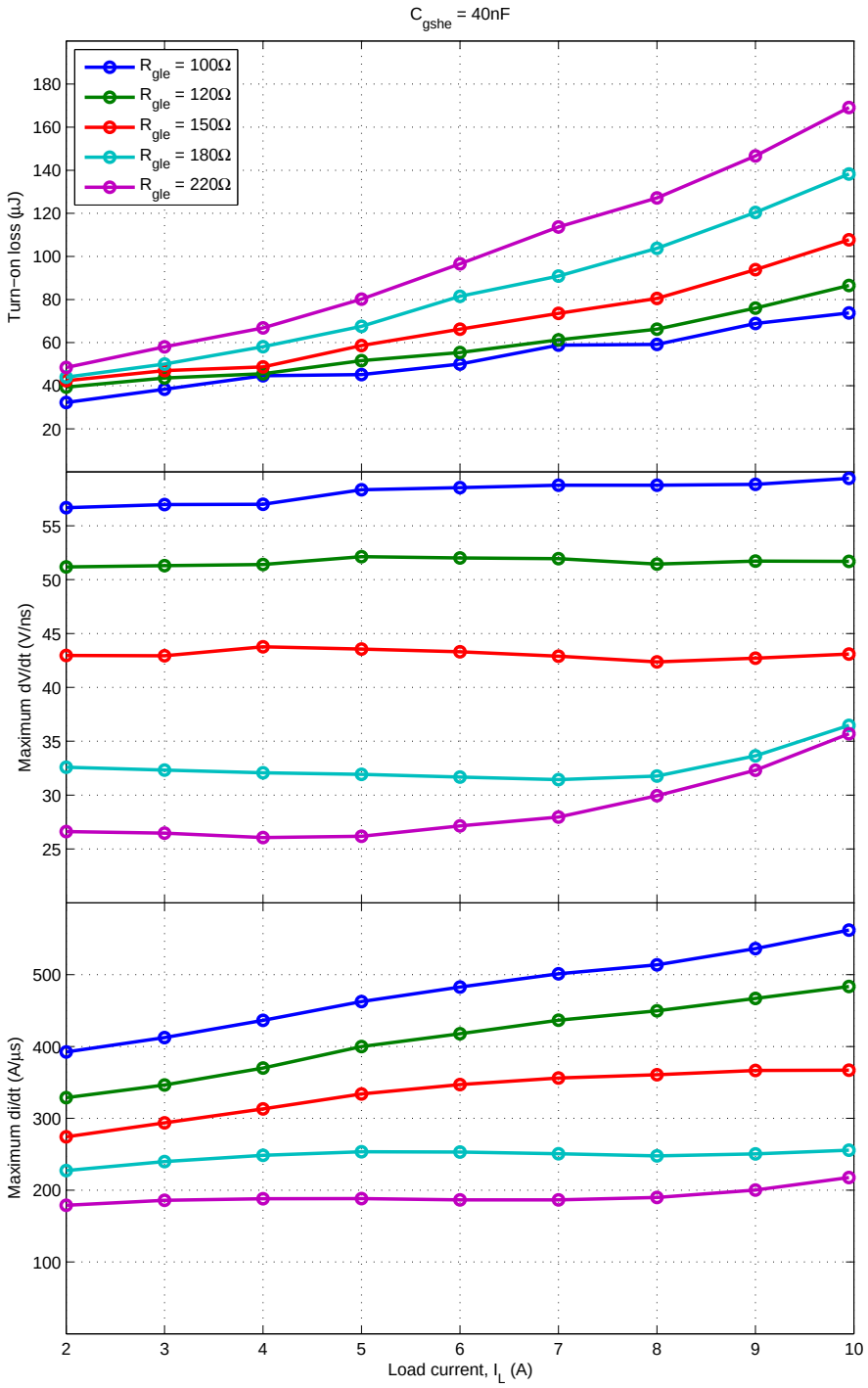
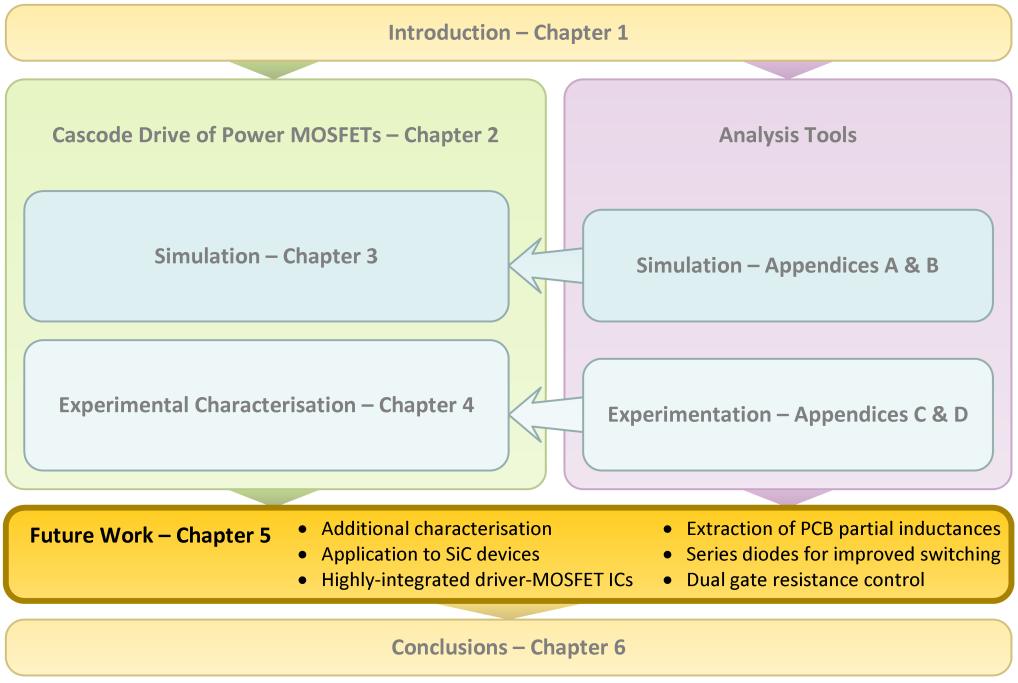


Figure 4.22: Turn-on loss, maximum dv/dt and maximum di/dt sensitivity to load current, I_L, for various values of R_{gle} with C_{gshe} fixed at 40 nF. Referenced on page 100.

Chapter 5

Future work

This chapter outlines future research opportunities that have been identified during the course of this work, but fell outside the scope of this thesis. Application of the cascode gate drive topology to silicon carbide (SiC) MOSFETs is discussed, along with a number of modifications to the cascode gate drive topology, including use of highly integrated MOSFET-driver ICs and the inclusion of low-voltage series diodes for body-diode reverse recovery elimination. Investigation of the combined use of cascode and high-voltage MOSFET gate resistances for switching performance optimisation is also proposed.



5.1 Further analysis and characterisation

Further analysis and characterisation of the cascode gate drive of power MOSFETs is recommended. This work has provided new insight into the switching mechanisms and control of the proposed cascode gate drive topology, but is by no means exhaustive. For example, this work investigates only one combination of cascode and high-voltage MOSFETs; while the characteristics elucidated in this work are expected to be broadly applicable, it is recommended that other device combinations be investigated to assess the sensitivity to device selection.

Equally, this work focused exclusively on switching performance in a clamped inductive switching application – understanding how the cascode switching process would change under different loading configurations (e.g. resistive, capacitive) would also be of value.

This work also provided new understandings of the switching mechanisms of the proposed topology. It should be possible to develop a more detailed analytical model of the switching process, which would aid in predicting the characteristics which were observed via simulation and experimental characterisation in this work.

Finally, investigation of the performance of the cascode gate drive in typical application circuits is recommended. It is expected that the application of cascode gate drive to typical converter topologies should allow improved performance compared with conventional gate drives. There may, however, be certain topologies for which cascode gate drive is better suited. Active power factor correction (PFC), for example, has been identified as an application of particular interest, for which the cascode gate drive topology may provide specific benefits.

5.2 Application of cascode gate drive to silicon carbide (SiC) MOSFETs

The proposed cascode gate drive topology exhibits some unique features that potentially make it ideally suited for the driving of silicon carbide (SiC) MOSFETs. SiC MOSFETs potentially offer substantial advantages in terms of voltage rating (up to 1200 V), switching performance and power density, however, driving these devices is more challenging than driving conventional silicon MOSFETs.

Firstly, the transconductance of SiC MOSFETs is lower. This means that to achieve fast switching, these devices must be driven more quickly through the active region (i.e. charging the gate from the threshold voltage to the point at which the load current is fully supported). If we consider a candidate device such

as CREE's CPM2-1200-0025B, the continuous rated load current of 60 A is supported for gate voltages exceeding 8 V (depending on the operating conditions).

Additionally the threshold voltage for SiC devices is significantly lower than high-voltage silicon MOSFETs and shows a substantial temperature dependence. Again consider the example CREE device, a minimum threshold voltage of 1.6 V is specified. To drive this device through the active region at rated load current requires the gate to be driven from 1.6 V to above 8 V (a 6.4 V swing). If we compare this with the silicon device used in this work (IPL60R199CP), the gate need only be driven between 2.5 V to 5 V (a 2.5 V swing) to traverse the active region.

The low threshold voltage potentially makes these devices sensitive to $\mathrm{d}v/\mathrm{dt}$ induced turn-on, as potentially small currents injected into the gate via parasitic capacitances could push the gate voltage above the threshold voltage. CREE recommends a negative gate bias be applied during the off period to ensure the device is held off.

In summary, the drive requirements for SiC MOSFETs are more stringent compared with silicon power MOSFETs; the gate must be driven more quickly through the active region, which spans a wider voltage range due to the lower transconductance. Higher bias voltages are required to minimise conduction losses, and a negative gate bias is recommended to ensure the devices are held off. For the CREE device used as an example, a -5 V to 20 V gate drive through a 2.5 Ω gate resistance is used to characterise switching performance.

These gate drive requirements are challenging to meet with a conventional gate driver; most commercial drive ICs are not rated for a 25 V gate voltage swing, nor have the capacity to provided a negative gate bias. The necessity to drive the gate through the active region quickly also requires a candidate drive to have high current sourcing capability (>8A using the 20 V/2.5 Ω example above).

The proposed cascode drive configuration, conversely, is ideally suited to driving SiC MOSFETs. Drive currents are not sourced through a gate resistance, allowing high peak currents to be delivered to the gate and the SiC MOSFET to be driven quickly through the active region. Higher gate voltage biases can be easily accommodated through suitable selection of the cascode and clamp MOSFETs. The devices used in this work, for example, have a 30 V rating, and would be perfectly suitable for driving the example CREE device.

Finally, the cascode gate drive topology can be trivially modified to provide a negative gate bias, as shown in Figure 5.1a. Instead of connecting the drain of the clamp MOSFET to the gate of the driven high-voltage MOSFET, it is instead connected to a voltage source at a higher potential than the voltage source to which the gate is connected. Thus, when the clamp MOSFET is turned on, the

source of the high-voltage MOSFET is pulled to a higher potential than the gate, resulting in a negative gate bias.

The second drive voltage supply can also be trivially implemented by deriving the positive gate drive supply ($V_{drive,HV+}$) as a regulated version of a slightly higher voltage supply ($V_{drive,HV-}$); the difference between these two supplies is the magnitude of the negative gate bias. Coincidentally, this was how the gate voltage supply of the experimental prototype was structured: the positive gate drive supply (12 V) was a derived form a 15 V unregulated supply (the output of an isolated DC-DC converter). A -3V gate bias could be simply realised by connecting the drain of the clamp MOSFET to the 15 V rail instead of the gate of the driven high voltage MOSFET.

In conclusion, the proposed cascode gate drive topology appears to be particularly well suited to driving SiC MOSFETs. Further research is recommended as it is envisaged that this may be the key application area for the proposed gate drive topology.

5.3 Use of highly integrated driver-MOSFET ICs

Since the conception of the research topic, advances have been made in the availability of highly integrated low-voltage power switching stages. This has primarily been driven by increasing power requirements of processors in consumer electronics, with low core voltages (sub 3.3 V). These applications require low-voltage power-electronic switching regulators to be placed as close as possible to the load in order to minimise voltage drops at high currents. These devices have also been exploited for use in research applications [60, 61].

The low-voltage MOSFET pair (Texas Instruments part CSD86350Q5D [57]) used throughout this research was originally intended for this application. The driving justification for the use of this device was the minimisation of packaging parasitics through both the lead-less packaging and stacking of the low-voltage MOSFET dies. The use of clip-bonds rather than wire-bonds in these devices was also attractive. In a package of 5 mm × 6 mm, footprint area was also substantially reduced compared with an implementation using discrete MOSFETs.

A bootstrap driver IC was paired with these power devices to provided control of both the upper (sync or clamp) and lower (control or cascode) MOSFET devices. The driver IC occupied approximately a quarter of the footprint area of the power devices (3 × 3 mm compared with 5 × 6 mm). The driver IC was placed immediately under the power device package, on the opposite side of the PCB; this design was intended to minimise trace lengths and loop sizes in the drive current paths and to minimise the impact of the placement of the driver IC

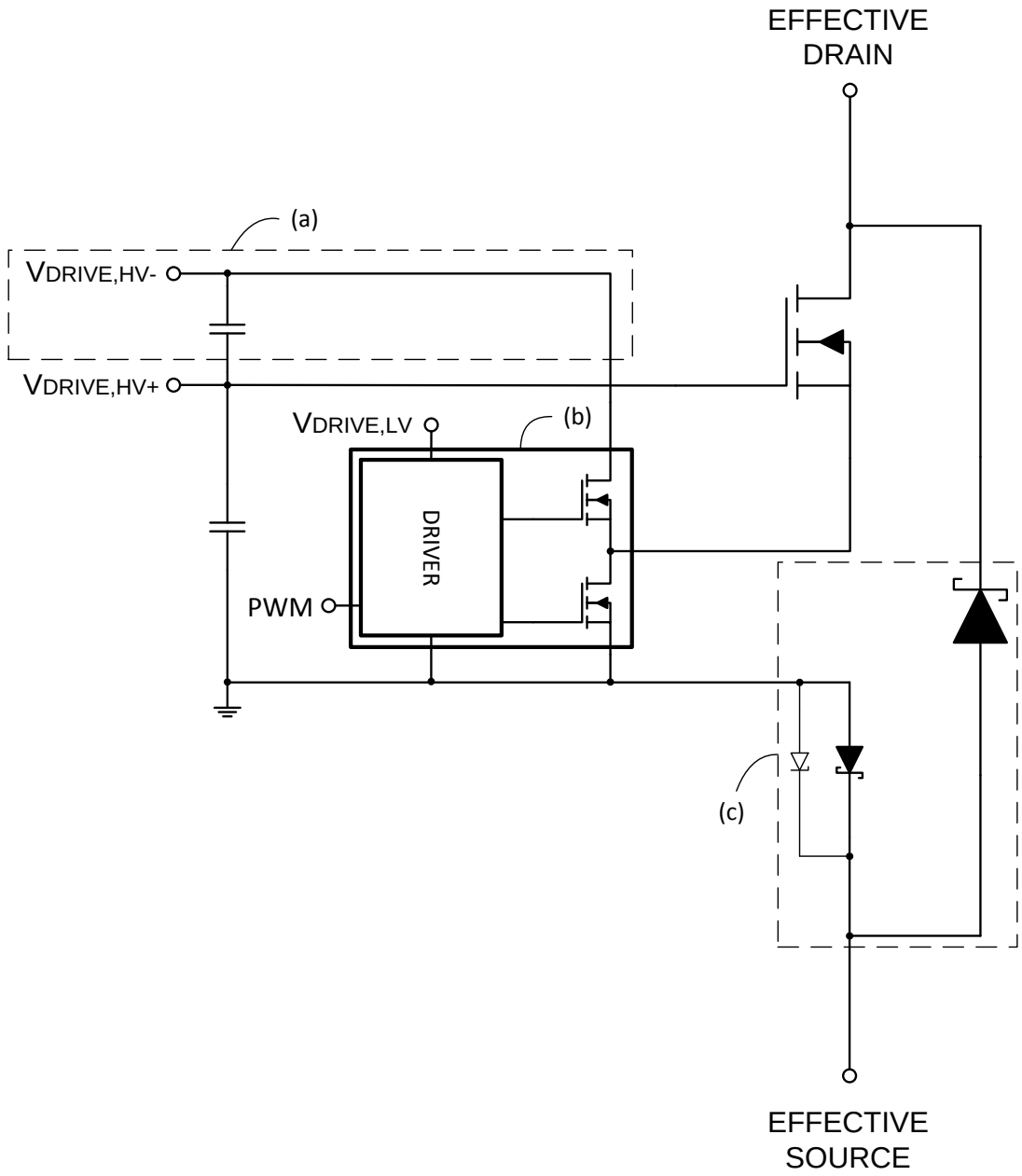


Figure 5.1: Modified cascode gate drive circuit illustrating potential opportunities for future research. (a) Modification to permit a negative gate bias during turn off. (b) Use of highly integrated drive-MOSFET IC in the cascode topology. (c) Inclusion of a low-voltage series diode and high-voltage anti-parallel SiC Schottky diode for reverse recovery elimination. A TVS diode for clamping of the series diode reverse voltage is also shown.

on the routing of the high-current traces to the power MOSFET pair.

Over the course of this research, however, a new generation of this technology has become available, where both the power MOSFETs and drive circuitry are incorporated within the same package without increasing the footprint size. Higher-density versions are also available (e.g. Texas Instruments part CSD95379Q3M) where the footprint has been reduced to 3.3×3.3 mm at the expense of lower voltage (20 V compared with 30 V) and current (20 V compared with 40 V) ratings. Even at these reduced ratings these devices would still be suitable for driving typical silicon high-voltage power MOSFETs, which typically require drive voltages on the order of 10–15 V, in application with continuous load currents up to 20 A. An example showing the modification of the proposed cascode gate drive topology incorporating a integrated driver-MOSFET IC is provided in Figure 5.1b.

This new generation of integrated driver-MOSFET ICs potentially provides a number of advantages. The reduced footprint size means that the proposed cascode drive topology could be more easily implemented, with a lower component count and reduced footprint area. Inclusion of the driver IC into the same package as the driven low voltage power MOSFETs provides tighter coupling to these devices and minimises parasitic inductances in the drive current paths. The smaller footprint of the package means that better PCB layouts can be achieved with the low-voltage MOSFETs placed closer to the driven high-voltage power MOSFET. Routing of critical current traces is also potentially improved as the reduced footprint of the integrated IC presents less of an obstruction to optimal routing paths.

The reduced component footprint also has broader implications for the layout of switching bridges; a single integrated drive-MOSFET IC enables a PCB implementation in which all components reside on one layer, rather than on both sides of the PCB. This provides the opportunity to implement an optimal layout for the switching half-bridge, either with the high-side device on the top layer and low-side device on the bottom layer, or both high- and low-side devices on the same side of the PCB and return currents routed on an internal layer. In both cases the critical commutation current loop size/area is substantially reduced compared with a lateral layout, allowing parasitic inductances to be minimised and switching performance to be improved.

Use of an integrated driver-MOSFET IC, however, has serious implications for the realisation of the proposed cascode drive configuration. When the driver IC is incorporated into the same package as the low-voltage power MOSFETs, the capability to adjust the gate resistances of the cascode and clamp MOSFETs is lost. Typically the switching speed of the low voltage MOSFETs is optimised by the manufacturer for the original intended application (e.g. switching buck

regulator); switching speed are maximised and dead time between the upper and lower devices is minimised. The integrated driver may also include various protection features, such as maximum pulse width protection, which, while suitable for buck converter applications, may hinder the use of these devices in the proposed cascode drive topology.

Much of the research presented in this work focused on the use of the cascode MOSFET gate resistance as the key parameter for controlling the switching characteristics of the cascode drive topology. If a designer wished to utilise one of the integrated drive-MOSFET ICs to realise some of the advantages discussed above, this degree of freedom is no longer available. As these integrated driver-MOSFET ICs are typically designed to maximise switching speeds for the purposes of minimising switching losses, it is likely that in a cascode drive application this would result in unacceptably high switching speeds for the high-voltage MOSFET. In this scenario, different methods would be required to satisfactorily control the switching speed of the high-voltage MOSFET.

One potential option may be the addition of additional gate resistance between the high-voltage MOSFET gate and the drive voltage supply. Such a mechanism is outside the scope of this work as it introduces significant impedance in the drive path, changing the characteristics of the drive process and invalidating some of the assumptions made in the conceptualisation of the simplified turn-on process. This potential avenue of research is discussed further in Section 5.6.

5.4 Extraction of PCB partial inductances

Parasitic inductances will be present in all practical power electronic circuits due to non-ideal PCB layouts. In this work, parasitic layout inductance was explicitly excluded from circuit simulations, and instead a rigorous experimental approach was use to characterise the switching performance of the circuit under test, allowing the effects of parasitic elements in a hardware implementation to be captured.

A more attractive solution would be the explicit inclusion of parasitic inductances at the design and simulation stages of the development cycle, to allow circuit layout effects to be analysed at the design stage. Feedback regarding the performance of the PCB layout could then be incorporated into the design before any hardware is produced.

Inclusion of parasitic inductances in the design and simulation of the cascode gate drive circuit is particularly challenging due to the numerous shared current paths during a switching transition (see Fig. 2.3). At least three critical current paths exist: the load current loop, the high-voltage MOSFET gate charging loop

and the cascode MOSFET gate charging loop. Equally it is possible to identify at least seven discrete positions where parasitic inductance could be lumped in the cascode gate drive circuit. Each lumped inductance may be shared between up to three of the critical current loops and each critical current loop flows through up to five of the lumped parasitic inductances.

Based on the layout geometry it would be possible to estimate the loop inductance for each of the critical current loops. Allocation of the loop inductance across the seven lumped parasitic inductances, however, would be largely arbitrary. Additionally the current loops during the switching transition are dynamic, with different loops present in each sub-interval of the switching process.

To properly capture the effect of parasitic layout inductances we must instead consider the concept of partial inductances. For each lumped inductance identified in the circuit we assign both a self partial inductance, and a mutual partial inductance between the lumped inductance in question and every other lumped inductance in the circuit. By taking this approach it would be possible to properly model the interaction of the various critical current loops via the parasitic inductances.

To estimate the self and mutual partial inductances, finite element analysis (FEA) is proposed. Via this method, a 3D CAD model of the physical PCB copper can be used at the design time for the estimation of the parasitic partial inductances.

The proposed methodology is that an electromagnetic FEA tool (COMSOL Multiphysics is one such candidate) can be used to simulate excitation of each critical current loop. The vector magnetic potential, $\mathbf{A}$, and current density, $\mathbf{J}$, for each current loop can be simulated over the modelled 3D volume. The self and mutual partial inductances of relevant PCB segments (corresponding to the position of lumped inductances in the circuit model) can then be calculated through the correct formulation and integration of these vector quantities over the volume of copper that defines each segment of the current loop, according to equations (5.4.0.1) through (5.4.0.4) [62]:

$$L_{p1} = \frac{1}{I_1^2} \int_{v_1} \mathbf{A}_1 \cdot \mathbf{J}_1 \, \mathrm{d}v_1 \tag{5.4.0.1}$$

$$L_{p2} = \frac{1}{I_2^2} \int_{v_2} \mathbf{A}_2 \cdot \mathbf{J}_2 \, \mathrm{d}v_2 \tag{5.4.0.2}$$

$$M_{p12} = \frac{1}{I_1 I_2} \int_{v_2} \mathbf{A}_1 \cdot \mathbf{J}_2 \, \mathrm{d}v_2 \tag{5.4.0.3}$$

$$M_{p21} = \frac{1}{I_1 I_2} \int_{v_1} \mathbf{A}_2 \cdot \mathbf{J}_1 \, \mathrm{d}v_1 \tag{5.4.0.4}$$

where the subscripts denote the PCB land segments such that I_1 is the current carried by land 1, $\mathbf{A}_1$ is the vector magnetic potential resulting from I_1, v_1 is the volume of PCB land 1 and $\mathbf{J}_1$ is the current density enclosed by volume v_1. Readers should refer to [62] for further information on the derivation and application of these equations.

Using this methodology it should be possible to extract from the 3D model of the PCB copper the parasitic inductances of the circuit layout. These inductances can then be modelled as lumped elements in a SPICE simulation to provide a more truthful representation of the switching performance of the circuit when realised in hardware.

Use of FEA simulation tools also permits frequency domain effects to be investigated. This is of particular interest for PCB design of power electronic circuits, as wide PCB lands are often implemented in order to handle high continuous or steady-state (low frequency) currents, while during switching transients, very high frequency components exist in the current. High frequency current are likely to take a different path through the PCB land (for example, may be constrained to the surface of the land), which will likely result in the effective parasitic inductances being frequency dependent.

A proof-of-concept study is required to validate the methodology proposed above. This could then be extended to modelling the parasitic inductances in a cascode gate drive PCB layout to improve the accuracy of simulation results.

5.5 Use of low-voltage series diodes for improved switching performance

The application of the cascode drive topology to power MOSFETs provides the opportunity to drive the MOSFETs much faster due to the capacity to deliver high peak currents to the gate of the driven MOSFET. The maximum practical switching speed will then most likely not be bounded by the capability of the drive circuit or switching performance of the power MOSFET, but by other considerations such as layout parasitics (as discussed in the previous section), EMI considerations and other external factors.

The driving rationale for the increase in switching speed is the reduction of switching losses; by reducing the total switching transition time the switching

losses are reduced proportionally allowing either increased efficiency or an increase in switching frequency for the same losses. In half-bridge applications, however, where the half-bridge is formed by MOSFETs in both the high- and low-side positions, the switching transition time may be largely dominated by the reverse recovery of the MOSFET body-diode.

If we consider the MOSFET used in this work (IPL60R199CP) the reverse recovery time, t_{rr}, at the datasheet test conditions (9.9 A load current) is 340 ns, with a peak reverse recovery current of 33 A. Compare this with the on-time, t_{on}, of 15 ns at the same load current but in the absence of reverse recovery: in the presence of reverse recovery the switching time is more than twenty times longer and the peak drain current is more than four times higher. The reverse recovery time could be reduced by increasing the rate-of change of current, however this would result in even more extreme device stresses (peak current). For fast-switching MOSFETs, reverse recovery dominates the turn-on time, and hence, switching losses.

In an inductive switching application it is usual for the load current to commutate to at least one of the MOSFET body-diodes over the course of one switching cycle, due to the required dead time between the switches in a half-bridge. In soft-switched converters the load current may commutate to the body diodes of both MOSFETs over the course of a switching cycle. Whenever the body diode of one of the switches conducts current, the diode must be recovered in the next switching transition.

The reverse recovery process requires the removal of the stored charge from the body-diode junction before the body-diode, and hence power MOSFET, will support a reverse voltage. The stored charge is proportional to the peak forward current that was supported by the body-diode. In practical terms the reverse recovery process requires the opposing switching device to conduct additional current in excess of the load current after the full load current is supported by the device, but before the voltage transition can occur. The reverse recovery current, then, contributes to both the peak current seen by the opposing switch as well as the peak switching loss.

Certain switching strategies may prevent the body diodes carrying current during the dead-time by timing the switching transition such that the MOSFET channel is conducting before current commutates to the body diode. Current then preferentially flows through the MOSFET channel (reverse conduction). Even in this scenario, however, current is not prevented from flowing in the body diode. The forward voltage of the body diode will typically be of the same order of magnitude as the voltage drop across the channel of the power MOSFET, resulting in the body diode shunting a portion of the load current

even when reverse channel conduction of the power MOSFET is utilised. The current shunted by the body diode may be on the order of 10–20 % of the load current. While this strategy will reduce the effects of reverse recovery it will not eliminate it entirely.

To entirely avoid reverse recovery, current must be prevented from flowing through the MOSFET body-diode. One mechanism by which this can be achieved is through the inclusion of a diode in series with the power MOSFET to prevent reverse current conduction. A second diode is then typically placed in anti-parallel with the MOSFET-diode combination to provide a path for free-wheeling currents. If this anti-parallel diode is selected to be a Schottky diode, reverse recovery can be avoided.

The primary drawback of this techniques is that it introduces additional power losses due to the forward voltage drop of the series diode in the load current path. Additionally it means that the power MOSFET channel can no longer be utilised for reverse conduction; reverse current is instead carried by the anti-parallel Schottky diode, resulting in a higher voltage drop that would typically be exhibited by the channel. This implementation also requires two additional power semiconductor devices.

Inclusion of a series diode is not an new strategy; this method has been used in the past to avoid the poor characteristics of MOSFET body-diodes or to add reverse blocking capabilities to power MOSFETs. Historically, however, such an implementation would involve the use of high-voltage series diodes which exhibit a relatively high forward voltage and/or exhibit far-from-ideal reverse recovery performance. If the series diode is being introduced solely to block reverse current from flowing through the power MOSFET, the series diode can be chosen to be a low-voltage device, optimised for a low forward voltage drop.

The ideal candidate for this application is a low-voltage, high-current Schottky diode. A high-voltage silicon carbide Schottky diode can be used for the anti-parallel diode, preventing reverse recovery. The series diode only needs to have a reverse voltage rating equal to the maximum forward voltage of the anti-parallel Schottky diode while conducting the peak reverse current, as the anti-parallel diode clamps the maximum reverse voltage seen by the series diode. Use of a suitably sized series Schottky diode allows the forward voltage drop to be minimised (on the order of 0.3–0.4 V) to reduce the additional conduction losses.

In principle the inclusion of a low-voltage series diode should allow reverse recovery to be eliminated to allow better switching performance at the expense of additional conduction losses. To evaluate the potential benefits of such an implementation, an estimation of key performance parameters is made below using typical power semiconductor devices and operating points. The example test con-

ditions are summarised in Table 5.1 and the performance metrics are summarised in Table 5.2. The test case observes the MOSFET switching performance assuming that is sees the reverse recovery current of an opposing MOSFET of the same type. Operation near 100 % duty cycle (the worst case in terms of the additional conduction losses of the added series diode) is considered.

From the results summarised in Table 5.2 it can be seen that the reverse recovery dominates both the losses and switching times. For the selected devices we can expect up to a four times reduction in losses through the addition of a low-voltage series diode, and almost an eight times reduction in the total turn-on time. It should be noted that for this test a relatively low switching frequency was selected; for higher switching frequencies the results would be even more preferential towards the series-diode case (reverse recovery loss would stay constant while the conduction loss would decrease). The additional conduction losses introduced by the inclusion of the series diode are more than offset by the elimination of the loss associated with reverse recovery.

This exercise demonstrates the potential of this mechanism to improve the switching performance of power MOSFETs. This is only a single test case, however. While net benefits are expected over a wide range of devices and operating points, the difference between the two cases will not be as stark in certain circumstances, for example, when applied to fast-recovery MOSFETs or at reduced load currents. A comparative analysis should also be conducted in a typical application

Parameter	**Value**	**Description**
Power MOSFET	IPL60R199CP	650 V 9.9 A CoolMOS
Series diode	PMEG3050EP	30 V 5 A silicon Schottky diode
Anti-paralle diode	IDD12SG60C	600 V 12 A SiC Schottky diode
Load current	10 A	
Bus voltage	400 V	
di/dt	200 A/µs	Rate of change of drain-source current
dv/dt	50 V/ns	Rate of change of drain-source voltage
Switching frequency	10 kHz	

Table 5.1: Test conditions for evaluation of low-voltage series diode performance.

Parameter	**Without series diode**	**With series diode**
Current rise time, t_r (ns)	50	50
Reverse recovery time, t_{rr} (ns)	340	0
Voltage fall time, t_f (ns)	8	8
Total turn-on time, t_f (ns)	398	58
Turn-on loss, E_{on} (µJ)	116	116
Reverse recovery loss, E_{rr} (µJ)	3604	0
Conduction loss, E_{cond} (µJ)	180	555
Total losses, E_{tot} (µJ)	4016	787

Table 5.2: Estimated switching performance of low-voltage series diode case against base test case.

over the entire operating range rather than a single operating point, particularly where load current and duty cycles change (e.g. a sine-wave modulated inverter).

There are additionally potential implementation issues that must be investigated and addressed. One issue identified is that there is no mechanism in the series diode configuration to clamp the drain (or source, depending on location of the series diode) voltage of the power MOSFET. Under transients this may lead to the series diode being over-voltaged, depending on the relative magnitudes of parasitic elements including capacitances and leakage currents. A potential solution to this problem may include the addition of a transient voltage suppressor (TVS) diode to protect the low-voltage series diode (see Fig. 5.1c).

5.6 Control of the switching process by cascode and high voltage MOSFET gate resistances

The parameter space composed of the cascode MOSFET gate (R_{gle}) and high-voltage MOSFET gate resistance (R_{ghe}) was identified in Section 3.7 as a candidate to affect independent control of dv/dt and di/dt switching performance metrics. The (R_{gle}, R_{ghe}) parameter space was excluded from further investigation on the basis that introducing external gate resistance to the high-voltage MOSFET would fundamentally change the operation of the proposed topology.

While outside the scope of this thesis, the parameter space exhibited promising characteristics that warrant further investigation. The simulated average di/dt, average dv/dt and turn-on switching loss performance surfaces for the (R_{gle}, R_{ghe}) parameter space are shown in Figure 5.2. The process by which these surfaces were generated is detailed in Chapter 3.

Firstly, note the characteristic shape of the result surfaces over the upper-left-hand region of the plot. In this region all of the contours run parallel and close to horizontal. This indicates that the three switching performance metrics are tightly coupled over this region, and largely insensitive to changes in R_{gle}.

In this region, R_{ghe}, the gate resistance of the high-voltage MOSFET, dominates and the characteristics of the gate drive effectively reduce to that of a conventional gate drive; the switching process is controlled solely by R_{ghe} which can be adjusted to set the switching speed.

As the value of R_{ghe} is reduced and the value of R_{gle} is increased, however, the shape of the three surfaces diverge. We can define approximately the boundary in the parameter space for which this change in behaviour occurs as $R_{gle} > R_{ghe}$ (the lower-right-hand region of the plot).

In this region of the plot the average di/dt and average dv/dt contours appear

almost orthogonal, meaning it would be possible to achieve excellent independent control of these metrics over this region. For example, note that we can follow the 50 V/ns average dv/dt contour while traversing the average di/dt contours from 200 A/µs to 1000 A/µs; this is a five times increase in average di/dt while holding average dv/dt constant. Excellent sensitivity of the switching performance metrics is observed over this region of the parameter space.

While these initial results are promising, a detailed analysis of this parameter space has not been conducted; maximum di/dt and dv/dt sensitivity should be investigated along with load current sensitivity. Additionally, the effect of re-introducing significant gate resistance to the high-voltage MOSFET should be assessed, particularly with respect to immunity to currents injected into the gate via parasitic capacitances during switching transitions.

It may also be possible to introduce C_{gshe} as a third degree of freedom to achieve better control and optimisation of the cascode switching process.

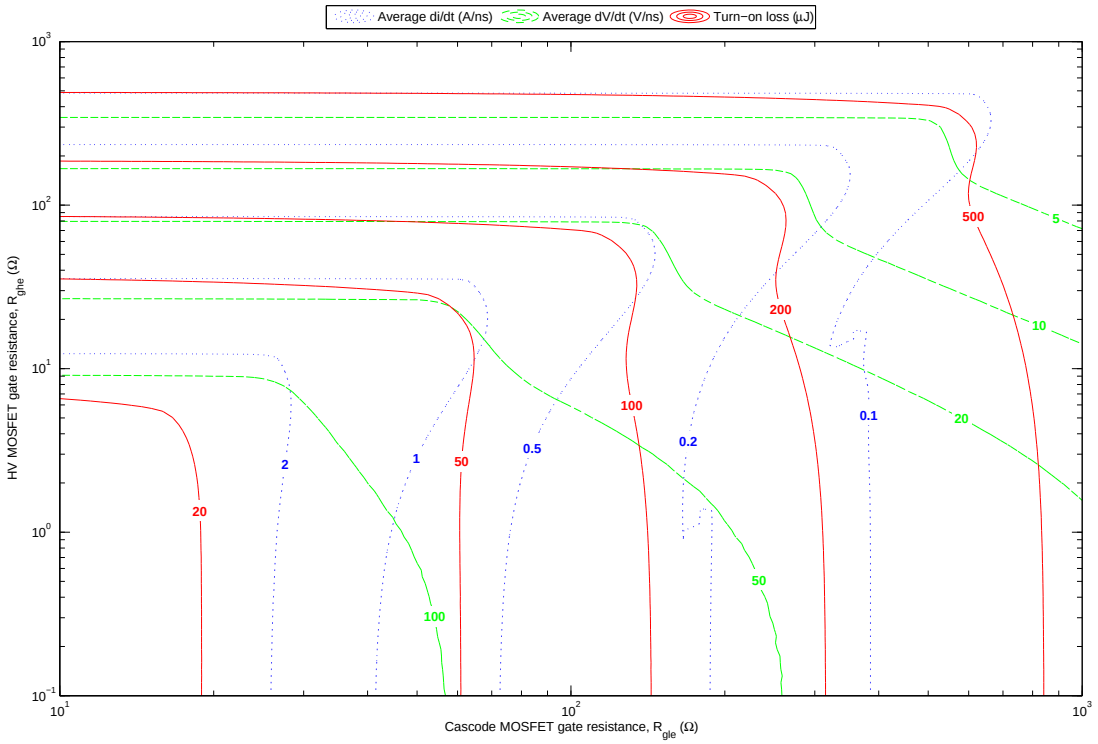


Figure 5.2: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, HV MOSFET gate resistance parameter space.

5.7 Reverse-conduction characteristics

This work primarily focused on the cascode gate drive topology under forward-conduction (i.e. drain-source current flow). For many applications this is sufficient (active power factor correction, boost converters, fly-back converters etc.). A defining feature of MOSFETs is the intrinsic body-diode, which provides a commutation path for reverse currents. One of the key advantages of power MOSFETs compared with other transistor technologies, however, is the ability of the channel to conduct current in both directions (i.e. both drain-source and source-drain).

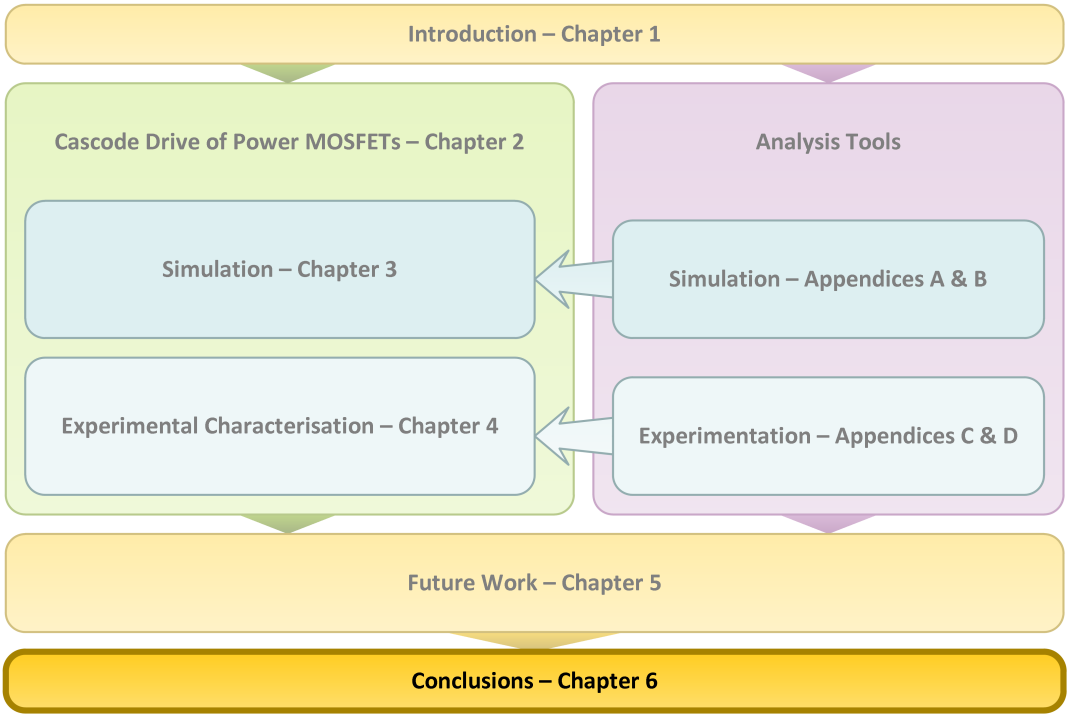
The cascode topology potentially offers some unique characteristics in this operating mode. The positive gate bias will ensure that even under uncontrolled reverse conduction (i.e. when the cascode and clamp MOSFETs are held off), the gate of the high-voltage MOSFET will be enhanced and source-drain load current will be conducted by the channel of the high-voltage MOSFET rather than the body-diode. This may have positive benefits for soft-switching or synchronous rectification applications if it allows the effects of body-diode reverse recovery to be mitigated to some degree, or even eliminated entirely.

Conversely, it has been identified that it would be disadvantageous to hold the clamp MOSFET on during reverse conduction, as this forces the load current to flow though the gate-drive supply. This not only discharges the gate-drive supply, but also imposes in the load current path a voltage drop equal to the drive voltage. In typical applications where the dead-time is minimised, this effect should not cause an issue, but warrants further investigation. Alternatively, careful coordination of the clamp and cascode MOSFET drive timing may be sufficient. The inclusion of a low-voltage series diode and high-voltage anti-parallel diode, as discussed in Section 5.5, would eliminate this effect and allow the clamp MOSFET to be held on indefinitely independent of the direction of the load current.

Chapter 6

Conclusions

The key contributions and findings of this work are presented in this chapter. A novel cascode gate drive topology for power MOSFETs in clamped-inductive switching applications has been developed. Mechanisms that control the switching process are identified and discussed, along with the advantages and limitations of the proposed cascode gate drive topology. Opportunities for switching performance optimisation using the proposed topology have been elucidated via simulation and validated experimentally using unique analysis techniques.



6.0.1 Cascode gate drive of power MOSFETs

A novel cascode gate drive configuration for power MOSFETs in switching applications was developed. The circuit is composed of two low-voltage n-channel power MOSFETs which drive the source of a high-voltage power MOSFET. In contrast to conventional gate drive, gate current is not sourced through a resistor, allowing high peak currents to be delivered to the gate during turn-on: long charging delays and the Miller plateau are eliminated.

The second low-voltage MOSFET acts as an active gate clamp to ensure the high-voltage MOSFET may be driven off under all load conditions, and holds the MOSFET off with a low-impedance clamp. Alternative implementations were also proposed, including substitution of a p-channel device for the clamp MOSFET to simplify implementation.

The action of the clamp MOSFET in the switching process was described. The natural and forced turn-off mechanisms were identified.

The simplified turn-on waveforms for cascode gate drive of power MOSFETs were derived. Mechanisms that control the switching process were identified and discussed, along with the advantages and limitations of the proposed cascode gate drive topology.

6.0.2 Simulation

A platform for the simulation of the cascode gate drive of power MOSFETs was developed. A methodology for the extraction of power semiconductor SPICE models from datasheet parameters was proposed and demonstrated. Characteristic switching waveforms for the proposed cascode gate drive were presented and compared to switching waveforms for a conventional gate drive.

An exploration of the parameter space for the proposed cascode gate drive was conducted to determine potential mechanisms for control of switching performance. The parameter space composed of the cascode MOSFET gate resistance (R_{gle}) and high-voltage MOSFET gate-source capacitance (C_{gshe}) was identified as a candidate for more detailed investigation.

A detailed investigation of switching performance over the (R_{gle}, C_{gshe}) parameter space was conducted via simulation. In general, increasing C_{gshe} was shown to reduce turn-on switching losses for a given value of R_{gle}, while the maximum $\mathrm{d}v/\mathrm{dt}$ during the switching transient was decreased and the maximum $\mathrm{d}i/\mathrm{dt}$ during the transition remained relatively constant.

Switching optimisation was performed via application of a novel analysis technique featuring overlaid contour plots of multiple switching performance metric surfaces. Practical examples demonstrating switching loss optimisation in the

presence of slew-rate constraints using cascode gate drive were formulated and presented.

6.0.3 Experimental characterisation

An experimental prototype of the proposed cascode gate drive topology was developed. Operation of the prototype was successfully demonstrated in a clamped inductive switching application at 400 V and 10 A. The observed experimental gate-source voltage waveforms were distinctly different from that of a conventional gate drive, with RC charging delays and the Miller plateau eliminated. Switching performance of the prototype was characterised experimentally at 350 discrete operating points over the (R_{gle}, C_{gshe}) parameter space for load currents ranging from 1 A to 10 A. At the highest demonstrated switching speed, a turn-on switching loss of 74 µJ was achieved for a maximum $\mathrm{d}v/\mathrm{dt}$ of 59 V/ns and maximum $\mathrm{d}i/\mathrm{dt}$ of 560 A/µs.

The switching behaviour observed in simulation was validated experimentally: independent control of $\mathrm{d}i/\mathrm{dt}$ and $\mathrm{d}v/\mathrm{dt}$ switching metrics were demonstrated, enabling optimisation of switching performance unachievable via conventional gate drive. Mechanisms that control the switching process were identified and mapped to the observed gate-source voltage waveforms.

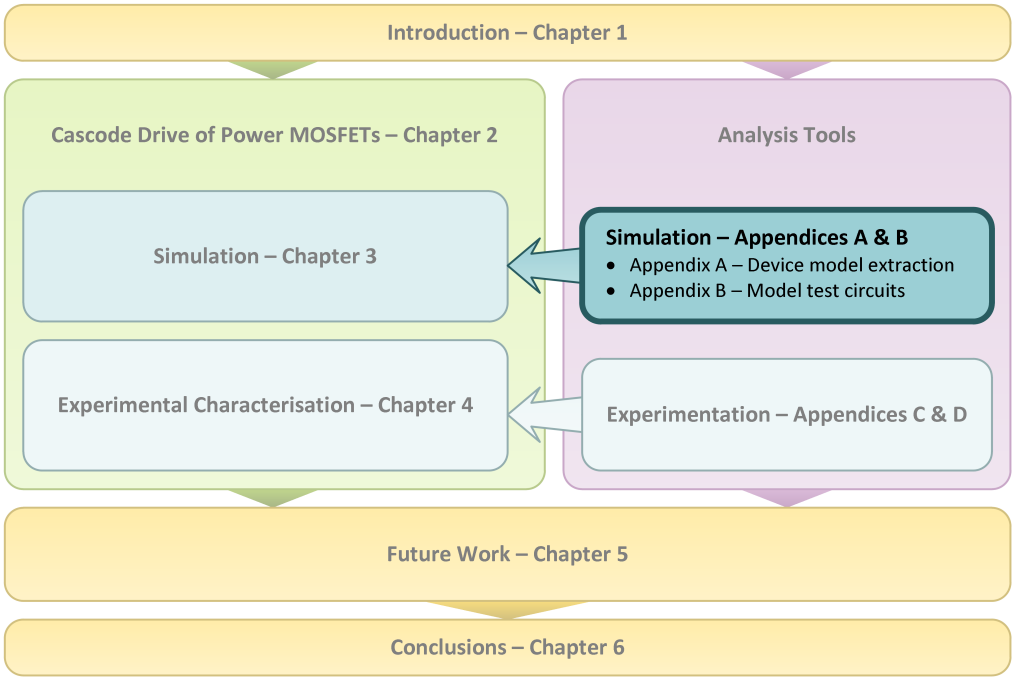
6.0.4 Future work

Recommendations were made for future research pathways arising from this work. Application of the cascode gate drive topology to silicon carbide (SiC) MOSFETs was proposed, along with a number of modifications to the cascode gate drive topology, including the use of highly integrated MOSFET-driver ICs and the inclusion of low-voltage series diodes for body-diode reverse recovery elimination. Investigation of the combined use of cascode MOSFET and high-voltage MOSFET gate resistances for switching performance optimisation was also proposed.

Appendix A

Extraction of semiconductor models from datasheet parameters

Presented in this appendix are practical methodologies for the extraction of power semiconductor device models from typical information available on manufacturer published datasheets. Specific focus is placed on the modelling of power MOSFETs using the LTspice VDMOS device model. Example applications of the extraction processes are provided for the devices used in this work, including the IPL60R199CP high-voltage power MOSFET, CSD86350Q5D "Sync" low-voltage MOSFET and IDD12SG60C SiC Schottky diode.



A.1 Introduction

Simulation is a valuable tool for design, evaluation of circuit performance, component selection and exploration of the parameter space. The value of the simulation results, however, depends largely on the quality of the device models which are used. This is particularly true for switching applications where both the DC and AC characteristics of the switching devices are critical and the frequency domain of interest may extend from DC (e.g. conduction losses) to hundreds of megahertz (e.g. switching transients).

At design time, available information regarding device behaviour is typically limited to the information provided by manufacturers on device datasheets. Manufacturers may also publish SPICE models for their devices, however, these models may be of limited accuracy, suitable only for certain simulation domains or utilise complex sub-circuits that result in extended simulation times. Characterisation of a physical device is also an option, however, this requires access to physical components during the design phase and often specialised equipment.

This section aims to address the aforementioned issues by providing a pragmatic process for the modelling of power switching devices based on information typically available in manufacturer datasheets. An overview of the critical device models and parameters is provided followed by a outline of parameter extraction techniques. Examples of the parameter extraction process are provided, based on the power devices modelled for use in this research. Schematics and net listings for test circuits used for the modelling and validation of power devices in this chapter are provided in Appendix B.

LTspice [63] is selected as the simulation program of choice as it provides an intrinsic model for the Vertical Diffused MOS (VDMOS) transistor which models the switching behaviour of power MOSFETs more accurately compared with the SPICE monolithic MOSFET model. As LTspice is a SPICE-based simulator, much of the following section is also easily extensible to other SPICE-based simulation environments.

A.2 SPICE device models

A.2.1 The SPICE diode model

The SPICE diode model is well documented in [64]. For the purposes of this work we are interested primarily in the forward conduction and junction capacitance characteristics, described by equations (A.2.1.1) and (A.2.1.2) respectively.

Equation (A.2.1.1) models the DC characteristics of the diode:

$$i_D = IS\left\{e^{\left(\frac{v_D}{N \cdot V_t}\right)} - 1\right\} + GMIN \cdot v_D \tag{A.2.1.1}$$

where i_D is the forward current, v_D is the forward voltage, V_t is the thermal voltage (a temperature dependant constant) and IS, N and $GMIN$ are parameters of the model.

Equation (A.2.1.1) models the AC characteristics of the diode:

$$C_j = C_{j0}\left\{1 - \frac{v_D}{V_j}\right\}^{-M} \tag{A.2.1.2}$$

where C_j is the junction capacitance, v_D is the forward voltage and C_{j0}, V_j and M are parameters of the model.

Readers should refer to [64] for additional detail regarding the physical meaning of the parameters and commonly used model extraction techniques.

A.2.2 The SPICE MOSFET model

The DC behaviour of the level-1 SPICE MOSFET model is described by three equations which describe the cutoff, ohmic and active regions respectively. Equations (A.2.2.1) through (A.2.2.3) describe the current-voltage characteristic of the level-1 MOSFET model.

If $v_{gs} < V_{th}$ (cutoff region):

$$i_d = 0 \tag{A.2.2.1}$$

If $v_{ds} < v_{gs} - V_{th}$ (ohmic region):

$$i_d = KP\frac{W}{L}\left(1 + \lambda \cdot v_{ds}\right)\left(v_{gs} - V_{th} - \frac{v_{ds}}{2}\right)v_{ds} \tag{A.2.2.2}$$

If $v_{ds} > v_{gs} - V_{th}$ (active region):

$$i_d = \frac{KP}{2}\frac{W}{L}\left(1 + \lambda \cdot v_{ds}\right)\left(v_{gs} - V_{th}\right)^2 \tag{A.2.2.3}$$

where Table A.1 provides a summary of the parameters.

The body diode of the MOSFET is modelled by the SPICE diode model as described previously in Section A.2.1. The level-1 MOSFET AC model will not be described in this section as the LTspice VDMOS model differs from the standard SPICE model. The AC model of the VDMOS is described in Section A.2.3.

Parameter	Description
KP	Transconductance
V_{th}	Zero-bias threshold voltage
λ	Channel-length modulation
L	Length scaling
W	Width scaling

Table A.1: Summary of parameters for the DC SPICE level-1 MOSFET model.

A.2.3 The LTspice VDMOS model

LTspice provides an intrinsic device model for the Vertical Diffused MOS (VDMOS) structure commonly employed for power MOSFETs. The LTspice VDMOS model incorporates two major changes, compared with the standard monolithic MOSFET models, to better represent the behaviour of VDMOS devices; the body diode is connected differently to the external terminals and the gate-drain capacitance is modelled as an empirical function of the applied gate-drain voltage. The DC model of the VDMOS is the same as the level-1 SPICE MOSFET model except that the length (L) and width (W) scaling parameters default to a value of one to allow the transconductance to be specified directly. The AC model of the VDMOS uses a constant capacitance to model the gate-source capacitance. The gate-drain capacitance is modelled by the junction capacitance of a diode connected between the source and drain terminals, as previously described by equation (A.2.1.2). The gate drain capacitance is modelled as an empirical function of the applied gate-drain voltage. The equation that describes this behaviour is of the form:

$$C_{gd}(v_{gd}) = \begin{cases} A \cdot \tanh\left(a \cdot v_{gd}\right) + B, & \text{if } v_{gd} > 0 \\ C \cdot \arctan\left(a \cdot v_{gd}\right) + D, & \text{if } v_{gd} \leq 0 \end{cases} \tag{A.2.3.1}$$

where,

$$C_{gd}(-\infty) = C_{gd,min} \tag{A.2.3.2}$$

$$C_{gd}(\infty) = C_{gd,max} \tag{A.2.3.3}$$

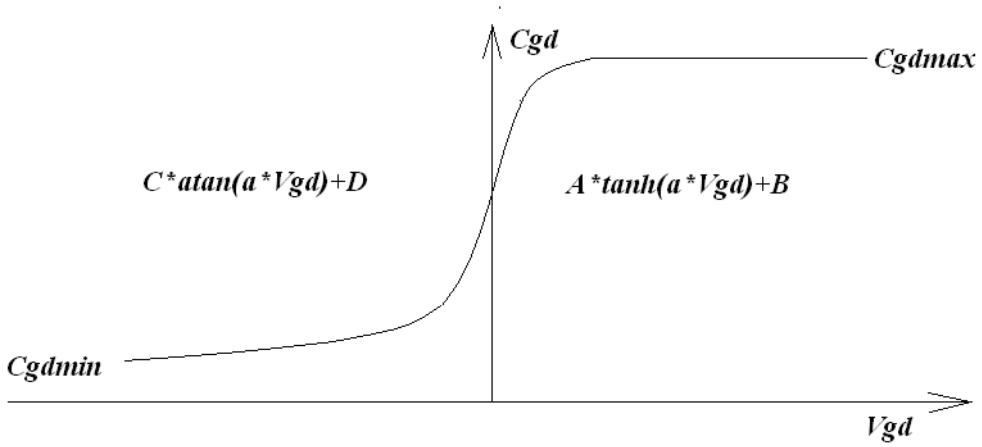


Figure A.1: Empirical form of the relationship between gate-drain voltage and gate-drain capacitance in the LTspice VDMOS model [63].

The gate drain capacitance is specified by parameters a, $C_{gd,min}$ and $C_{gd,max}$. Parameters A, B, C, and D are internally calculated by LTspice to fit the form of the equation to the specified parameters. Figure A.1 provides a graphical representation of the form of equation (A.2.3.1) and all important parameters.
Equation (A.2.3.1) may be simplified by considering that both its value and gradient should be continuous at $v_{gd} = 0$. Equating both intervals of the function at $v_{gd} = 0$ yields:

$$C_{gd}(0) = B = D = C_{gd0} \tag{A.2.3.4}$$

where we now define a new parameter, C_{gd0}, which is the gate-drain capacitance at zero gate-drain voltage. Similarly, differentiating equation (A.2.3.1) with respect to v_{gd} and equating both intervals at $v_{gd} = 0$ yields:

$$A = C \tag{A.2.3.5}$$

The simplified form of equation (A.2.3.1) is constructed by substituting equations (A.2.3.4) and (A.2.3.5) into equation (A.2.3.1):

$$C_{gd}(v_{gd}) = \begin{cases} A \cdot \tanh\left(a \cdot v_{gd}\right) + C_{gd0}, & \text{if } v_{gd} > 0 \\ A \cdot \arctan\left(a \cdot v_{gd}\right) + C_{gd0}, & \text{if } v_{gd} \leq 0 \end{cases} \tag{A.2.3.6}$$

Finally, parameters $C_{gd,min}$ and $C_{gd,max}$ may be expressed in terms of C_{gd0} and A by combining equation (A.2.3.6) with equations (A.2.3.2) and (A.2.3.3) respectively:

$$C_{gd,min} = C_{gd0} - \frac{\pi}{2}A \tag{A.2.3.7}$$

$$C_{gd,max} = C_{gd0} + A \tag{A.2.3.8}$$

A.2.3.1 Additional VDMOS model parameters

The LTspice VDMOS model provides two additional, largely undocumented, model parameters: *mtriode* and *subthres*.

mtriode is a conductance multiplier for the ohmic (triode) region of operation (compared with KP which is common to both the ohmic and active regions). The *mtriode* may be used to independently match MOSFET behaviour in both the ohmic and active regions.

subthres allows subthreshold conduction of the power MOSFET to be modelled. *subthres* specifies the current per volt of drain-source voltage for which exponential subthreshold conduction transitions to the current relationships defined in equations (A.2.2.2) and (A.2.2.3).

A.3 Parameter extraction methods

A.3.1 Diode forward characteristics

Parameter extraction methods for diode forward characteristics are well documented and include the three point I-V method, linear regression with fixed R_s and non-linear curve fit with fixed IS. Application of these methods is discussed in detail in [64]. Choice of method will be dependant largely on the type of data available for a particular device. Typically, characteristic data presented on a log-log scale will be a better candidate for linear regression. Where limited data are available the three point I-V method may be more appropriate. Two applications of these methods are presented in Section A.4 for a MOSFET body diode and SiC Schottky diode respectively.

A.3.2 Diode junction capacitance

Parameter extraction methods for diode junction capacitance are well documented and include the three point C-V method and linear regression with fixed V_j. Application of these methods is discussed in detail in [64]. The linear regression method is preferred where good data are available. An example application of the linear regression method for a SiC Schottky diode is presented in Section A.4.3.

A.3.3 MOSFET DC characteristics

A.3.3.1 Estimating the λ parameter

In the active region of the MOSFET output characteristics graph the drain current is directly proportional to the drain-source voltage. For each characteristic curve presented in the datasheet the gate-source voltage is held constant ($v_{gs} = V_{gs}$). Equation (A.2.2.3) may then be rewritten in the form:

$$i_d = \frac{KP\,(V_{gs} - V_{th})^2}{2} + \frac{KP\,(V_{gs} - V_{th})^2}{2}\lambda v_{ds} \tag{A.3.3.1}$$

which is the form of a straight line with intercept:

$$c = \frac{KP\,(V_{gs} - V_{th})^2}{2} \tag{A.3.3.2}$$

and slope:

$$m = \frac{KP\,(V_{gs} - V_{th})^2}{2}\lambda \tag{A.3.3.3}$$

The parameter λ may be determined by performing linear regression on data points from the active region of the characteristic curves and then dividing the slope by the intercept:

$$\lambda = \frac{m}{c} \tag{A.3.3.4}$$

For each characteristic curve reported in the datasheet (at different gate-source voltages) a different value for λ is likely to be obtained. Taking the average of the values obtained for each curve is suggested as a suitable method to calculate an overall value for the λ parameter for the simulation model.

A.3.3.2 Estimating parameters KP and V_{th}

In the active region of the transfer characteristic plot, the drain current is proportional to the square of the drain-source voltage. Taking the square root of both sides of equation (A.2.2.3) yields:

$$\sqrt{i_d} = \sqrt{\frac{KP\,(1 + \lambda \cdot v_{ds})}{2}} v_{gs} - V_{th}\sqrt{\frac{KP\,(1 + \lambda \cdot v_{ds})}{2}} \tag{A.3.3.5}$$

As v_{ds} is held constant for the transfer characteristic graph ($v_{ds} = V_{ds}$), equation (A.3.3.5) is in the form of a straight line with slope:

$$m = \sqrt{\frac{KP\,(1 + \lambda \cdot V_{ds})}{2}} \tag{A.3.3.6}$$

and intercept:

$$c = -V_{th}\sqrt{\frac{KP\,(1 + \lambda \cdot V_{ds})}{2}} \tag{A.3.3.7}$$

Estimates for parameters KP and V_{th} can therefore be obtained by performing linear regression of the square root of drain current against the gate-source voltage using data points from the active region of the transfer characteristic graph. Using the previously obtained estimate for λ and equation (A.3.3.6) for the slope of line determined by linear regression, parameter KP can be calculated from:

$$KP = 2\frac{m^2}{1 + \lambda V_{ds}} \tag{A.3.3.8}$$

Similarly, an estimate for the value of parameter V_{th} may be obtained from the slope and intercept:

$$V_{th} = -\frac{c}{m} \tag{A.3.3.9}$$

A.3.3.3 Improved matching using series resistances R_s and R_d

The parameters estimated in the previous section typically provide good matching for low drain currents. At gate-source voltages well above the threshold voltage the drain current tends to be overestimated. Better matching of the simulation model performance to the characteristic data can be achieved using the drain and source resistances, R_d and R_s respectively.

The source resistance is in the drain-source current path and therefore provides negative feedback; increasing drain current drives the gate-source voltage down, reducing the effective transconductance. Therefore, a small increase in the source resistance has a large impact on the output and transfer characteristics of the model. Additionally, introducing a source resistance requires the previously estimated transconductance parameter, KP, to be adjusted to take into account the negative feedback provided by the source resistance. Equation (A.3.3.10) relates the gate-source voltage used in the level-1 MOSFET model to the gate-source voltage applied to the terminals of the device, v'_{gs}, that is, taking into account the effect of a series source resistance.

$$v_{gs} = v'_{gs} - i_d R_s \tag{A.3.3.10}$$

To calculate a suitable value for R_s, let us firstly assume that as the value of λ is small, the sensitivity of the drain current to drain-source voltage is negligible. As $\lambda \to 0$, for the drain-source voltage dependant term in equation (A.2.2.3), we effectively have:

$$(1 + \lambda \cdot v_{ds}) \to 1 \tag{A.3.3.11}$$

Using this approximation we can also assume that the effect of a small drain resistance will be negligible. Modifying equation (A.2.2.3) using equation (A.3.3.10) and the approximation of equation (A.3.3.11) yields:

$$i_d = \frac{KP}{2}\Big(v'_{gs} - V_{th} - i_d R_s\Big)^2 \tag{A.3.3.12}$$

We can now select two points at the same drain-source voltage from either the output or transfer characteristic plot and use equation (A.3.3.12) to solve simultaneously for R_s. To get the best matching at high drain currents, points at higher gate source voltages are preferred. Care should be taken to ensure points are taken from the active region of the characteristic curves. Typically the intersection of the curves from the output characteristic graph with the right hand axis (maximum applied drain source voltage) are a convenient choice. Having selected two gate-source voltage, drain current pairs, equation (A.3.3.13) can be

solved to calculate a value for R_s:

$$\sqrt{\frac{I_{d1}}{I_{d2}}} = \frac{V'_{gs1} - V_{th} - I_{d1}R_s}{V'_{gs2} - V_{th} - I_{d2}R_s} \tag{A.3.3.13}$$

Finally, the adjusted value for KP can be calculated using one of the points chosen in the previous step from equation (A.2.2.3) modified by equation (A.3.3.10). Equation (A.3.3.14) below may be solved to calculate the new value for KP.

$$i_d = \frac{KP}{2}(1 + \lambda \cdot v_{ds})\left(v'_{gs} - V_{th} - i_d R_s\right)^2 \tag{A.3.3.14}$$

Due to the weak dependence of drain current on drain-source voltage, the drain resistance has minimal contribution to the transfer characteristics for low drain currents. The drain resistance, R_d, may be chosen to provide better matching of the transfer characteristics for high drain currents or alternatively for better matching of the output characteristics in the ohmic region; which choice is most suitable should be determined based on the context in which the model will be used and the typical operating range for the MOSFET.

A.3.4 MOSFET AC characteristics

MOSFET AC characteristics are modelled by the three parasitic capacitances C_{gs}, C_{ds}, and C_{gd}. Manufacturers usually report MOSFET capacitances in terms of input capacitance (C_{iss}), output capacitance (C_{oss}) and reverse transfer capacitance (C_{rss}), as these parameters can be measured directly. Equations (A.3.4.1) through (A.3.4.3) relate the capacitances reported on manufacturer datasheets to the physical capacitances which model the MOSFET AC characteristics.

$$C_{iss} = C_{gs} + C_{gd} \tag{A.3.4.1}$$

$$C_{oss} = C_{ds} + C_{gd} \tag{A.3.4.2}$$

$$C_{rss} = C_{gd} \tag{A.3.4.3}$$

The following section describes methods for extracting the model parameters from the characteristic capacitance data presented on manufacturer datasheets.

A.3.5 Estimating parameter C_{gs}

As described in Section A.2.3, the gate-source capacitance is modelled as a fixed capacitance given by parameter C_{gs}. The gate-source capacitance is determined from the C_{iss} and C_{rss} parameters reported on the datasheet according to equation (A.3.4.1). As the values for C_{iss} and C_{rss} are typically relatively constant for higher drain-source voltages, these values may usually be read directly from the typical capacitances plot.

A.3.6 Estimating parameters $C_{gd,min}$, $C_{gd,max}$ and a

The LTSpice VDMOS model for gate-drain capacitance is described in detail in Section A.2.3. Due to the highly non-linear relationship between gate-drain voltage and gate-drain capacitance, it is not possible to get a good fit for the gate-drain capacitance over the entire operating range, particularly around the gate-drain voltage range over which the gate-drain capacitance changes most rapidly. A reasonable fit can be obtained, however, by considering the bounds of operation, specifically the gate-drain capacitance at zero bias voltage and maximum applied gate-drain voltage. The following extraction method aims to provided matching of the gate-drain capacitance at zero drain source voltage, maximum drain-source voltage and a third point chosen in the transition region to provide a reasonable fit.

The gate-drain capacitance is equal to the reverse transfer capacitance (C_{rss}) reported on the datasheet, as described by equation (A.3.4.3). Characteristic capacitances on MOSFET datasheets are typically reported at zero gate-source voltage. The gate-drain voltage is then directly related to the drain-source voltage by:

$$v_{gd} = -v_{ds} \tag{A.3.6.1}$$

Noting these relationships it is possible to read both the gate-drain capacitance and gate-drain voltage directly from the datasheet characteristic capacitance plot.

For the purposes of extracting values for the model parameters we will define two parameters which can be read directly from the datasheet plot: C_{gd0} is defined as the gate-drain capacitance at zero gate-drain voltage and $C_{rss,min}$ is the minimum gate-drain capacitance reported (read from the plot at maximum drain-source voltage, $V_{ds,max}$). A third point, denoted $(V_{ds,test}, C_{rss,test})$, is chosen within the region of rapid transition of gate-drain capacitance to provide reasonable matching over this region. While the value for C_{gd0} may be difficult to read from the datasheet plot due to the scaling and rapid rate of change at $v_{gd} = 0$, a reasonable estimate can usually be interpreted. Alternative methods, such as de-

termination of an intercept by extrapolating digitised data may be inappropriate due to the highly non-linear nature of the change in capacitance.

Along with C_{gd0}, values for two additional parameters need to be determined in order to fully define the gate-drain capacitance. These are parameters A and a defined in equation (A.2.3.6). Equation (A.2.3.6) is most easily solved via an iterative solution. Equations (A.3.6.2) and (A.3.6.3) can be used to solve for values of A and a respectively, in terms of the previously defined voltages and capacitances.

$$A_n = \frac{C_{rss,min} - C_{gd0}}{\arctan(-a_n \cdot V_{ds,max})} \tag{A.3.6.2}$$

$$a_{n+1} = \frac{1}{V_{ds,test}} \tan\left(\frac{C_{gd,test} - C_{gd0}}{A_n}\right) \tag{A.3.6.3}$$

The default value for a is a suitable choice for an initial value, that is, $a_0 = 1$. Convergence to an appropriate precision is usually achieved within a few iterations ($n < 5$). Having determined a value for parameter A, the remaining model parameters $C_{gd,min}$ and $C_{gd,max}$ may be calculated using equations (A.2.3.7) and (A.2.3.8) respectively.

A.3.7 Estimating parameters C_{j0}, V_j and M

The MOSFET drain-source capacitance is modelled by the junction capacitance of the body diode as described previously in section A.2.1. While the parameter extraction techniques used for a diode, as described in section A.3.2, could also be used for modelling the MOSFET drain-source capacitance, alternative methods can be used to achieve better matching of the features of interest.

Parameter C_{j0} may be read directly from the characteristic capacitance plot at $v_{ds} = 0$ using:

$$C_{j0} = C_{oss}(0) - C_{rss}(0) \tag{A.3.7.1}$$

Values for the remaining parameters can be calculated by fitting the junction capacitance equation to two additional points. The first recommended point is $(V_{ds,max}, C_{oss,min})$, which is the minimum MOSFET output capacitance read from the characteristic capacitance plot at maximum drain-source voltage. The second point, denoted $(V_{ds,test}, C_{oss,test})$, can be chosen anywhere along the output capacitance curve, however, somewhere towards the bottom of the interval of high rate of change of capacitance is recommended for reasonable matching over the entire domain. The corresponding drain-source capacitance at each of these points can then be determined by subtracting the reverse transfer capacitance at the same drain-source voltage, according to equation (A.3.4.2).

Substituting the drain-source capacitance calculated at these two points into

equation (A.2.1.2) yields the following system of equations:

$$C_{ds,min} = C_{j0}\left\{1 - \frac{-V_{ds,max}}{V_j}\right\}^{-M} \tag{A.3.7.2}$$

$$C_{ds,test} = C_{j0}\left\{1 - \frac{-V_{ds,test}}{V_j}\right\}^{-M} \tag{A.3.7.3}$$

This system of equations can then be solved by numerical methods, such as the multi-variable Newton-Raphson method, to determine values for V_j and M.

A.3.8 MOSFET body diode characteristics

The parameters to model the forward characteristics of the MOSFET body diode can be extracted using the same techniques as described in Section A.3.1 for a discrete diode. Body-diode junction capacitance need not be modelled independently as this is included in the MOSFET drain-source capacitance modelling.

A.3.9 Reverse recovery

Parameter extraction methods for reverse recovery are documented for diodes, however, analytical methods are sensitive to the test circuit used to measure reverse recovery characteristics and do not take into account the effect of other parasitic capacitances that may be present in the device. This is particularly relevant for MOSFETs where the impact of the three parasitic capacitances cannot be neglected. In the SPICE diode model a single parameter, the forward transit time, TT, models the reverse recovery behaviour. Additionally, reverse recovery data is usually only provided for a single test condition in manufacturer datasheets. It is trivial to perform a sweep of this parameter in a SPICE simulation in order to choose a value for this parameter that most closely matches the behaviour documented on a datasheet. This methodology also ensures that any impact of other device characteristics is considered. Application of this methodology is presented in Section A.4.1 for the body-diode of a power MOSFET.

A.4 Case studies

A.4.1 Modelling of the IPL60R199CP power MOSFET

The IPL60R199CP is a n-channel silicon power MOSFET manufactured by Infineon Technologies [56]. The key features of this device are a reverse voltage rating of 650 V, a continuous forward current rating of 9.9 A and a maximum $R_{ds,on}$ of 199 mΩ. The device is available in a low-inductance, surface mount, 8 mm × 8 mm ThinPAK (VSON-4) package.

The characteristics to be modelled for this device include the DC characteristics (output and transfer characteristics), AC characteristics (typical capacitances) and body diode characteristics (forward conduction and reverse recovery). The corresponding information of interest on the datasheet are the typical output and transfer characteristics (datasheet Tables 10 and 12) typical capacitances (datasheet Table 8) and body diode reverse recovery and forward conduction characteristics (datasheet Tables 7 and 15). Modelling is conducted for a junction temperature of 25 °C.

A.4.1.1 DC characteristics

Firstly, DC parameters for the MOSFET are modelled. Output characteristics are provided over a linear drain-source voltage range of 0–20 V for a set of discrete gate-source voltages ranging from 4.5–20 V. To extract the λ parameter it is the active region of the plot that is of interest, which is the near-horizontal portion of some of the characteristic curves. The curves for gate-source voltages of 4.5 V, 5 V, 5.5 V and 6 V were selected for extraction of the λ parameter. These four curves were digitised into a series of drain-source voltage, drain current (v_{ds}, i_d) pairs. As only the active region is of interest, only the right hand portion of each of these curves was considered; data points approaching and beyond the knee of each curve were excluded.

The λ parameter may be determined by finding the gradient and intercept of these curves in the active region. Linear regression was performed to fit a straight line to each set of data yielding four gradient-intercept (m, c) pairs of (0.0074, 4.4288), (0.0247, 10.283), (0.0254, 18.284) and (0.0241, 27.807) for the four curves respectively. Equation (A.3.3.4) was then applied to extract a value for the λ parameter for each curve: 0.00167, 0.00240, 0.00139 and 0.00087 respectively. The four resulting values were then averaged to calculate the overall λ value for the model. The final value selected for the model was $\lambda = 0.0016$.

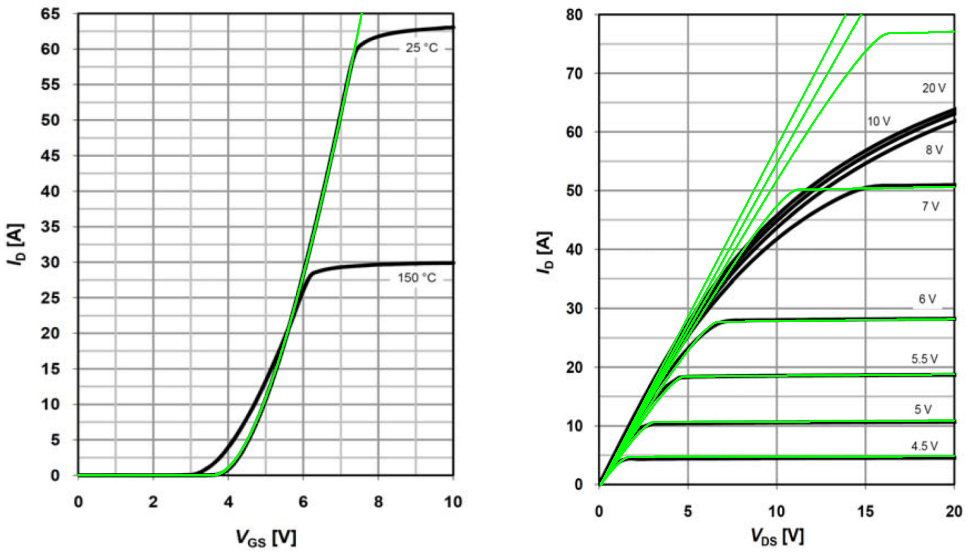
Having selected a value for the λ parameter the transconductance (KP) and threshold voltage (V_{th}) parameters can now be extracted. Again we select the ac-

tive region of operation but now choose the data from the transfer characteristic curve. The curve for a 25 °C junction temperature is digitised from the datasheet typical transfer characteristics plot, resulting in a set of gate-source voltage, drain current (v_{gs}, i_d) pairs. The gate-source voltage is then plotted against the square root of drain current. On plotting the data it is noted that for high currents the data departs from the form of a straight line. For this reason all data point for currents above 3.6 A were excluded. Linear regression was then used to fit a straight line to the remaining data points, yielding a gradient of 2.315 and an intercept of -8.328 with an R^2 value of 0.9994. Equations (A.3.3.8) and (A.3.3.9) can then be use to calculate values for the transconductance and threshold parameters: $KP = 10.386$ and $V_{th} = 3.597\,\mathrm{V}$.

These parameter values provide good matching of the transfer characteristics for low drain current but, due to the exclusion of high-current data-points, overestimate the drain current at higher gate-source voltages. The source resistance parameter, R_s, can be used to provide better matching in the high-current region. Equation (A.3.3.13) is used to calculate an appropriate value for the source resistance parameter based on two points selected from the high-current portion of the transfer or output characteristic curves. For convenience, data points are selected from the right-hand axis ($V_{ds} = 20\,\mathrm{V}$) on the output characteristic plot in the datasheet; the active region in this plot is well defined and the near-horizontal gradient of the curves at the intersection with the axis means the current can be easily read. The 6 V and 7 V gate-source voltage curves were selected (for matching of the highest drain currents documented in the active region). It should be noted that due to the choice of $V_{ds} = 20\,\mathrm{V}$, the selected point should correspond to points on the transfer characteristics curve also.

The two selected points provide the following gate-source voltage, drain current (v_{gs}, i_d) pairs: (6 V, 28.27 A), (7 V, 51.05 A). Using these points and equation (A.3.3.13) the source resistance can be calculated as $R_s = 0.013\,34\,\Omega$. The value of the transconductance parameter, KP, must now be adjusted to account for the contribution of the added source resistance (effectively a negative feedback term). The adjusted value for KP is calculated using the point (7 V, 51.05 A) and equation (A.3.3.14), yielding $KP = 13.362$.

On simulating the output characteristics using the extracted parameter values it is found that the drain currents are overestimated in the ohmic region. To provide better matching of the output characteristics in the ohmic region additional drain resistance may be introduced via parameter R_d. Parameter R_d is tuned in successive simulations by performing a sweep of its value in the MOSFET test circuit for output characteristics. The value that provides the best matching over the operation region of interest is selected. In this case a value of $R_d = 0.155\,\Omega$



(a) (b)

Figure A.2: Simulation of modelled DC characteristics for the IPL60R199CP power MOSFET (green) overlaid on original datasheet plots [56]. (a) Transfer characteristics. (b) Output characteristics.

was selected for best matching of gate-source voltages up to 6 V and currents up to 30 A in the ohmic region.

Figure A.2 shows the simulated transfer and output characteristics for the parameter values extracted above overlaid on the original datasheet plots. It can be seen that excellent matching has been achieved of the transfer characteristic for gate voltages up to 7.25 V. For higher gate voltages the drain current is overestimated, however, this region is well outside the typical operating conditions for this MOSFET and therefore good matching in this region is not required. For the output characteristics excellent matching is achieved in the active region for gate-source voltages up to 6 V. Excellent matching is also achieved in the ohmic region for currents up to 30 A. For higher gate-source voltages the drain current is over-estimated, however, this is outside the typical operating region and is therefore unlikely to affect the accuracy of the model in simulations.

A.4.1.2 AC characteristics

Next, the AC parameters for the MOSFET are extracted, which involves modelling the typical capacitances. Typical capacitances are provided on the datasheet over a linear drain-source voltage range of 0–600 V. Capacitances are presented on a logarithmic scale from 1 pF to 100 nF. Capacitance values are particularly difficult to read from plots presented in this manner due to the high rate of change of capacitance as the drain-source voltage approaches 0 V.

The gate source capacitance is modelled as a fixed capacitance. The C_{iss} value

presented on the datasheet graph is the sum of C_{gs} and C_{gd} (C_{rss}). To calculate the value for the C_{gs} parameter we must therefore read a value for both C_{iss} and C_{rss} from the datasheet graph at the same drain-source voltage. 600 V is selected as a convenient voltage (on the right-hand axis) for which values of C_{iss} = 1.518 nF and C_{rss} = 1.790 pF are read. The calculated value for the gate-source capacitance parameter is therefore C_{gs} = 1.516 nF.

The reverse transfer capacitance (C_{rss}) is equal to the gate-drain capacitance (C_{gd}) and is modelled for the LTspice VDMOS model by empirical equation (A.2.3.1). As described in Section A.3.6, three drain-source voltage, gate-drain capacitance (v_{ds}, C_{gd}) points are required to extract the model parameters: $(0, C_{gd0})$, $(V_{ds,max}, C_{gd,min})$ and $(V_{ds,test}, C_{gd,test})$. C_{gd0} = 1 nF is the C_{rss} value read from the datasheet graph at v_{ds} = 0 V. $C_{gd,min}$ = 1.79 pF is the C_{rss} value read from the datasheet graph at maximum drain-source voltage, $V_{ds,max}$ = 600 V (intersection of the C_{rss} curve with the right-hand axis). The final point is selected somewhere along the C_{rss} curve to provide a reasonable fit. A point in the region of high rate of change of capacitance is recommended. In this case the point selected was at a drain-voltage of 50 V (near the start of the capacitance transition) to provide good matching of capacitance over the 50–600 V drain-source voltage region (at this is the range over which the bulk of the switching transition occurs). For $V_{ds,test}$ = 50 V a value of $C_{gd,test}$ = 4.28 pF was read from the datasheet plot.

Having selected three points from the datasheet graph, equations (A.3.6.2) and (A.3.6.3) were used to calculate values for parameters A and a. Convergence of the iterative solution to within 0.001% tolerance was achieved within six iterations to yield values of $A = 6.3562 \times 10^{-10}$ and a = 4.6710. Using the calculated value for A and the value for C_{gd0} read from the datasheet graph, equations (A.2.3.7) and (A.2.3.8) can now be used to calculate for the remaining model parameters values of $C_{gd,min}$ = 1.5628 pF and $C_{gd,max}$ = 1.6356 nF.

The output capacitance (C_{oss}) is modelled by the reverse junction capacitance of the body diode. As such, the standard extraction techniques used for diodes could be used to model this capacitance. However, due to the poor fit of the IPL60R199CP characteristic output capacitance to the diode model of capacitance, the alternative three-point extraction technique presented in Section A.3.7 is used instead. This method requires three drain-source voltage, drain-source capacitance (v_{ds}, C_{ds}) pairs to be extracted from the datasheet graph: $(0, C_{ds0})$, $(V_{ds,max}, C_{ds,min})$ and $(V_{ds,test}, C_{ds,test})$. As the output capacitance is the sum of C_{ds} and C_{gd} (C_{rss}), for each point read off the C_{oss} curve, the C_{rss} value at the same voltage must be read and subtracted from the C_{oss} value to give the value for C_{ds}.

$C_{ds0} = 9\,\text{nF}$ is the C_{ds} value read from the datasheet graph at $v_{ds} = 0\,\text{V}$, and is equal to parameter C_{j0} used throughout equations (A.3.7.1) through (A.3.7.3). $C_{ds,min} = 43.850\,\text{pF}$ is the C_{ds} value read from the datasheet graph at maximum drain-source voltage, $V_{ds,max} = 600\,\text{V}$ (at the right-hand axis). The final point is selected somewhere along the C_{oss} curve to provide a reasonable fit. A point in the region of high rate of change of capacitance is recommended. In this case the point selected was at a drain-voltage of 65.25 V again to provide good matching of capacitance over the 50–600 V drain-source voltage region. For $V_{ds,test} = 65.254\,\text{V}$ a value of $C_{ds,test} = 117.49\,\text{pF}$ was calculated from the datasheet graph.

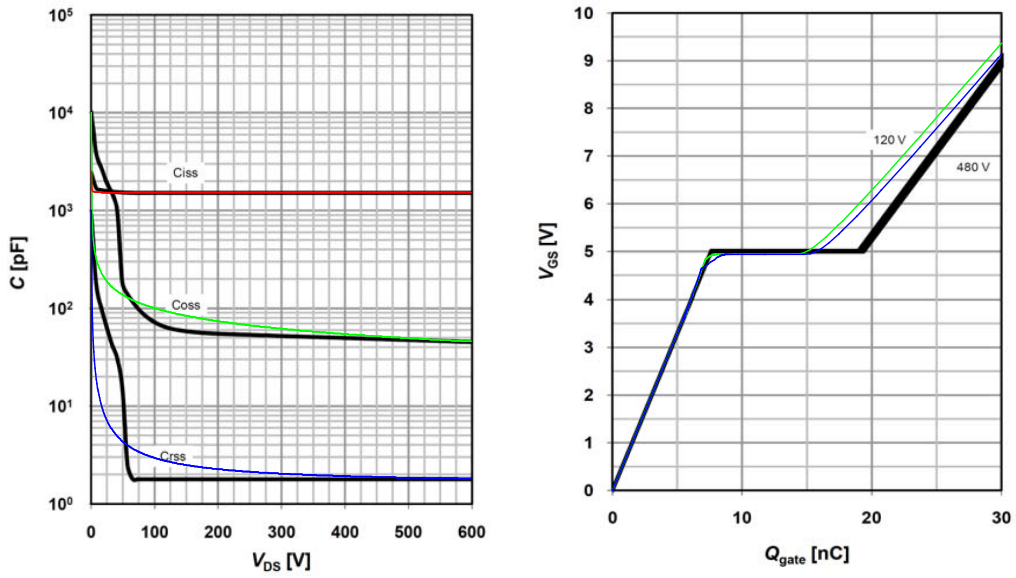
Having selected three points from the datasheet graph, the multi-variable Newton-Raphson method was applied to equations (A.3.7.2) and (A.3.7.3) to solve for values of V_j and M. Initial values of 0.05 and 0.5 respectively were used. Convergence of the iterative solution to within a tolerance of 0.0001 was achieved within 9 iterations to yield values of $V_j = 0.0037\,\text{V}$ and $M = 0.4442$.

Figure A.3a shows the simulated characteristic capacitances for the parameter values extracted above, overlaid on the original datasheet plot. Good matching of the input capacitance (red) is observed over the entire drain-source voltage range. For the reverse transfer capacitance, good matching is achieved for drain-source voltage in the range of 100–600 V (within 1 pF of the datasheet value). Below 100 V the transition of capacitance is not well matched, and is typically underestimated over the 0–50 V range. As the bulk of the switching transition occurs in the 50–600 V range, the underestimation of gate-drain capacitance over the 0–50 V region should not greatly affect the performance of the model in switching applications. Similarly the output capacitance is reasonably well matched over the 50–600 V range but is underestimated below 50 V.

Additionally the gate charge characteristics were simulated and presented in Figure A.3b, overlaid on the original datasheet graph for comparison. Good matching was achieved for both clamping voltages over the 0–5 V gate-source voltage range. Between 5 V and 9 V the model underestimates the gate charge, which is most likely attributed to the underestimation of the gate-drain and drain-source capacitances in the 0–50 V drain source voltage region (the drain-source voltage starts to decrease from the clamping voltage in the gate-charge test for gate-source voltages higher than the plateau voltage, 5 V).

A.4.1.3 Body diode characteristics

The remaining model parameters to be extracted are the body diode characteristics. Body diode forward conduction characteristics are presented in the device datasheet on a logarithmic current scale and linear voltage scale. The datasheet graph is an ideal candidate for digitisation, allowing linear regression to be used



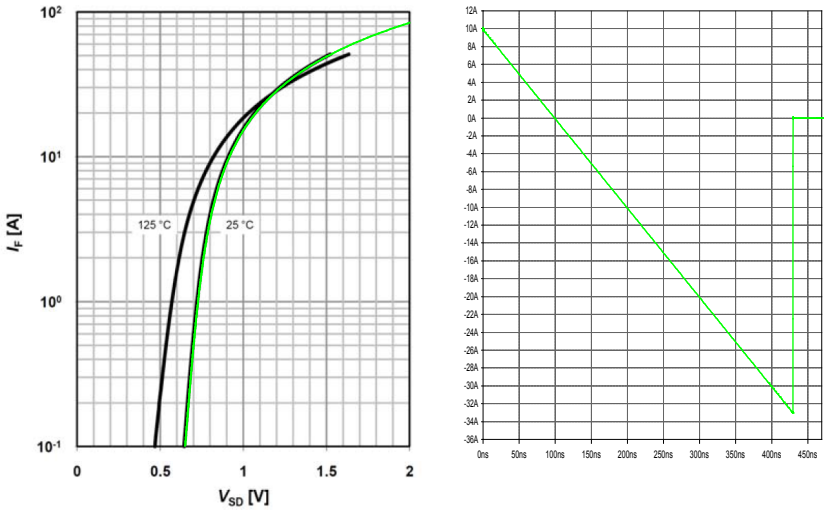
(a) (b)

Figure A.3: Simulation of modelled AC characteristics for the IPL60R199CP power MOSFET overlaid on original datasheet plots [56]. (a) Typical capacitances. (b) Typical gate charge.

to extract the diode model parameters. The forward characteristics graph, from datasheet Table 15, was digitised and linear regression used to fit a straight line to the data as outline in Section A.3.1. The series resistance value, R_s, used in the calculation of the regression variables was optimised to minimise the R^2 value for the linear regression. An R^2 value of 0.9979 was achieved with a value of R_s = 0.013835. The gradient and intercept of the resulting fitted line were m = 0.91530 and c = -25.291 respectively. From this result values for the remaining parameters were calculated as $N = 1.0925$ and $IS = 1.0381 \times 10^{-11}$.

A single parameter, TT, controls the reverse recovery behaviour of the VDMOS model. To determine a suitable value for this parameter a simulation of the MOSFET model was performed in LTspice at the test conditions presented in datasheet Table 7. A sweep of the TT parameter value was performed to achieve a match for the peak reverse recovery current of 33 A at the test conditions. From the simulation results a value of $TT = 670 \times 10^{-9}$ was selected. As a rule of thumb this value will be roughly two times the reverse recovery time (340 ns) for the typical power MOSFET reverse recovery test conditions.

Figure A.4a shows the simulated forward characteristics for the body diode overlaid on the original datasheet plot. It can be seen that excellent matching is achieved over the entire operating range. The simulated reverse recovery waveform for the body diode is presented in Figure A.4b. The simulated waveform shows that the peak reverse recovery current of 33 A has been matched with a total reverse recovery time of 330 ns, slightly lower than the value of 340 ns



(a) (b)

Figure A.4: Simulation of modelled body diode characteristics for the IPL60R199CP power MOSFET. (a) Forward characteristics overlaid on original datasheet plot [56]. (b) Reverse recovery waveform for datasheet test conditions with diode current plotted against time.

reported on the datasheet. The reverse recovery behaviour of the model is extremely "snappy" (evidenced by the near vertical transition to 0 A after the peak reverse recovery current) which from experimental observations is a reasonable representation of the behaviour of this family of power MOSFET (CoolMOS CP family). The model may not represent MOSFETs with a "softer" reverse recovery characteristic as faithfully.

A.4.1.4 LTspice model statement

Presented in Figure A.5 below is the final LTspice `.model` statement for the IPL60R199CP power MOSFET incorporating all the parameters extracted in the above section. The model command is presented in a multi-line format for readability, but can be simply condensed into a single line format (for inclusion in the LTspice "standard.mos" MOSFET library, for example).

```
* LTSpice VDMOS model for Infineon IPL60R199CP 650V power MOSFET
.model IPL60R199CP VDMOS(
+ KP=13.4 VTO=3.6 LAMBDA=0.0016
+ RS=0.0133 RD=0.155 RG=2.0
+ CGS=1516.4p
+ CGDMAX=1.6356n CGDMIN=1.5628p a=4.671
+ Cjo=9n m=0.4442 Vj=0.0037
+ IS=1.0381E-11 N=1.0925 RB=13.835m TT=670n )
```

Figure A.5: LTspice VDMOS model for Infineon IPL60R199CP 650 V power MOSFET extracted from datasheet parameters.

A.4.2 Modelling of the CSD86350Q5D "Sync" MOSFET

The CSD86350Q5D is a stacked configuration of two low-voltage n-channel power MOSFETs manufactured by Texas Instruments [57]. The stacked configuration results in a highly integrated, low-inductance, surface mount half-bridge. The module is rated at 25 V and 40 A. The low- and high-side devices are asymmetric with typical on-resistances of 1.1 mΩ and 5 mΩ respectively. The module is optimised for 5 V gate drive.

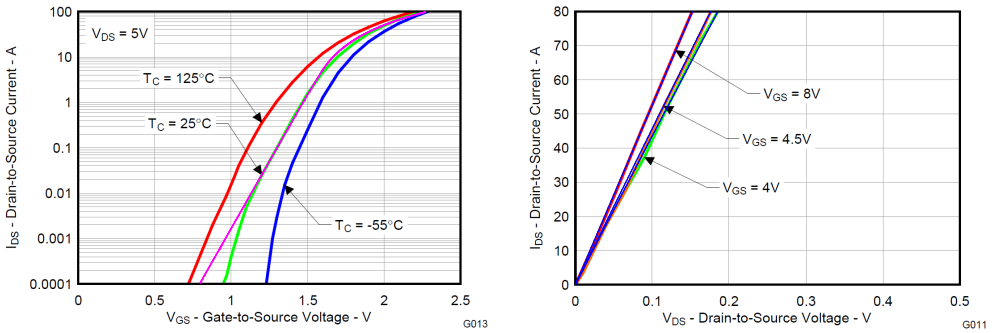
The same parameter extraction process can be used for both the low- and high-side devices. Additionally only the low-side device is used in simulations performed in this work. As such, a detailed description of the parameter extraction process will only be presented below for the low-side device (the "Sync MOSFET" in the datasheet nomenclature).

The characteristics to be modelled for this device include the DC characteristics (output and transfer characteristics), AC characteristics (typical capacitances) and body diode characteristics (forward conduction and reverse recovery). The corresponding information of interest on the datasheet are the saturation and transfer characteristics (datasheet Figures 11 and 13), typical capacitances (datasheet Figure 17) and body diode forward conduction (datasheet Figure 25) and reverse recovery characteristics (datasheet "Diode characteristics" table). Modelling is conducted for a junction temperature of 25 °C.

A.4.2.1 DC characteristics

Firstly, DC parameters for the MOSFET are modelled. Output characteristics are only provided in the saturation (ohmic) region over a linear drain-source voltage range of 0–1 V for gate-source voltages of 4 V, 4.5 V and 8 V. As the active region of the output characteristics is not documented, there are no data available to estimate the λ parameter. Consequently, we set $\lambda = 0$.

The transconductance (KP) and threshold voltage (V_{th}) parameters are now extracted. We select the active region of operation using the data from the transfer characteristic curve. The curve for a 25 °C junction temperature is digitised from the datasheet typical transfer characteristics plot, resulting in a set of gate-source voltage, drain current (v_{gs}, i_d) pairs. The gate-source voltage is then plotted against the square root of drain current. On plotting the data it is noted that for high currents (above approximately 50 A) and low gate-source voltages (below approximately 1.6 V) the data departs from the form of a straight line. For these reasons only data points for gate voltages between 1.6 V and 2 V are selected for inclusion in the subsequent regression analysis. Linear regression was used to fit a straight line to the selected data points, yielding a gradient of



(a) (b)

Figure A.6: Simulation of modelled DC characteristics for the CSD86350Q5D "Sync" power MOSFET (magenta in (a), blue in (b)) overlaid on original datasheet plots [57]. (a) Transfer characteristics. (b) Output characteristics.

12.301 and an intercept of -17.693 with an R^2 value of 0.9986. Equations (A.3.3.8) and (A.3.3.9) can then be use to calculate values for the transconductance and threshold parameters: $KP = 302.64$ and $V_{th} = 1.4383\,\mathrm{V}$.

To achieve better matching of the drain current characteristics in the subthreshold and ohmic regions, it was necessary to use the poorly documented *subthres* and *mtriode* parameters. Increasing the *subthres* parameter allowed the drain current in the subthreshold region to be increased, while changing the *mtriode* parameter allowed the transconductance in the ohmic region to be changed without effecting the transfer characteristics.

As no formal methodology was proposed to extract these parameter values, instead an iterative process was used, whereby one parameter was adjusted and matching assessed by inspection of the simulated characteristics, compared with the datasheet plot. In general, R_s and *mtriode* were used to achieve good matching in the ohmic region, with the consequence that R_s effected the transfer characteristics. The λ and *subthres* parameters could be used to adjust the transfer characteristics. These four parameters were therefore adjusted in an iterative fashion to achieve good matching of both the output and transfer characteristics. The final values selected for these parameters were $R_s = 1.65\,\mathrm{m\Omega}$, $\lambda = 0.1$, $subthres = 0.46$ and $mtriode = 2.1$.

Figure A.6 shows the simulated transfer and output characterised for the parameter values extracted above overlaid on the original datasheet plots.

A.4.2.2 AC characteristics

Next, the AC parameters for the MOSFET are extracted, which involves modelling the typical capacitances. Typical capacitances are provided on the datasheet over a linear drain-source voltage range of 0–25 V. Capacitances are presented on a logarithmic scale from 10 pF to 10 nF.

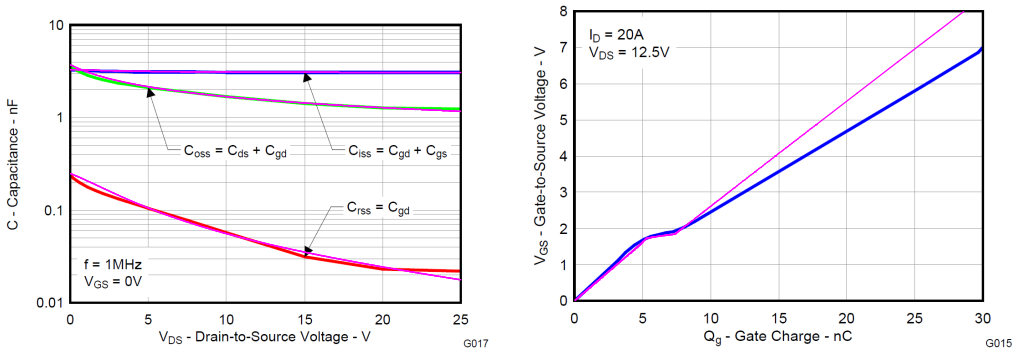
The gate source capacitance is modelled as a fixed capacitance. The C_{iss} value presented on the datasheet graph is the sum of C_{gs} and C_{gd} (C_{rss}). To calculate the value for the C_{gs} parameter we must, therefore, read a value for both C_{iss} and C_{rss} from the datasheet graph at the same drain-source voltage. 25 V is selected as a convenient voltage (on the right-hand axis) for which values of $C_{iss} = 3.0854\,\text{nF}$ and $C_{rss} = 22.026\,\text{pF}$ are read. The calculated value for the gate-source capacitance parameter is therefore $C_{gs} = 3.0634\,\text{nF}$.

The reverse transfer capacitance (C_{rss}) is equal to the gate-drain capacitance (C_{gd}) and is modelled for the LTspice VDMOS model by empirical equation (A.2.3.1). As described in Section A.3.6, three drain-source voltage, gate-drain capacitance (v_{ds}, C_{gd}) points are required to extract the model parameters: $(0, C_{gd0})$, $(V_{ds,max}, C_{gd,min})$ and $(V_{ds,test}, C_{gd,test})$. $C_{gd0} = 250\,\text{pF}$ is the C_{rss} value read from the datasheet graph at $v_{ds} = 0\,\text{V}$. A maximum drain-source voltage of 13 V is selected to provide better matching of the gate-drain capacitance over the operating region of interest (a nominal gate drive supply of 12 V for driving the IPL60R199CP silicon power MSOFET). $C_{gd,min} = 42.1\,\text{pF}$ is the C_{rss} value read from the datasheet graph at maximum drain-source voltage, $V_{ds,max} = 13\,\text{V}$. The final point is selected somewhere along the C_{rss} curve to provide a reasonable fit. In this case good matching was achieved by selecting a point at $V_{ds,test} = 11.1\,\text{V}$ for which a value of $C_{gd,test} = 50.2\,\text{pF}$ was read from the datasheet plot.

Having selected three points from the datasheet graph, equations (A.3.6.2) and (A.3.6.3) were used to calculate values for parameters A and a. Convergence of the iterative solution to within 0.001% tolerance was achieved within 29 iterations to yield values of $A = 1.6536 \times 10^{-10}$ and $a = 0.23725$. Using the calculated value for A and the value for C_{gd0} read from the datasheet graph, equations (A.2.3.7) and (A.2.3.8) can now be used to calculate for the remaining model parameters values of $C_{gd,min} = -2.1864\,\text{pF}$ and $C_{gd,max} = 20.746\,\text{nF}$.

The output capacitance (C_{oss}) is modelled by the reverse junction capacitance of the body diode. As such, the standard extraction techniques used for diodes could be used to model this capacitance. As the output capacitance of the CSD86350Q5D is not a good fit for the characteristic diode capacitance curve the alternative three-point extraction technique presented in Section A.3.7 is used instead. This method requires three drain-source voltage, drain-source capacitance (V_{ds}, C_{ds}) pairs to be extracted from the datasheet graph: $(0, C_{ds0})$, $(V_{ds,max}, C_{ds,min})$ and $(V_{ds,test}, C_{ds,test})$. As the output capacitance is the sum of C_{ds} and C_{gd} (C_{rss}), for each point read off the C_{oss} curve, the C_{rss} value at the same voltage must be read and subtracted from the C_{oss} value to give the value for C_{ds}.

$C_{ds0} = 3.483\,\text{nF}$ is the C_{ds} value read from the datasheet graph at $v_{ds} =$



(a) (b)

Figure A.7: Simulation of modelled AC characteristics for the CSD86350Q5D "Sync" power MOSFET (magenta) overlaid on original datasheet plots [57]. (a) Typical capacitances. (b) Typical gate charge.

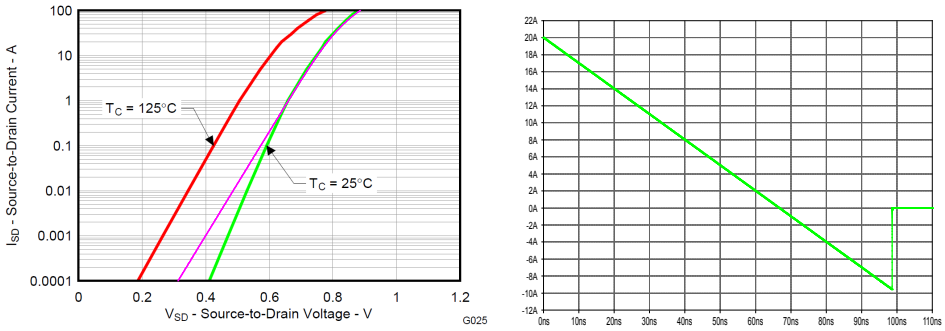
0 V, and is equal to parameter C_{j0} used throughout equations (A.3.7.1) through (A.3.7.3). $C_{ds,min} = 1.486\,\text{nF}$ is the C_{ds} value read from the datasheet graph at maximum drain-source voltage, $V_{ds,max} = 13\,\text{V}$ (selected as the maximum drain-source voltage for a nominal 12 V gate drive supply, see above). The final point is selected somewhere along the C_{oss} curve to provide a reasonable fit. In this case good matching was achieved by selecting a point at $V_{ds,test} = 5.018\,\text{V}$ for which a value of $C_{ds,test} = 2.053\,\text{nF}$ was calculated from the datasheet graph.

Having selected three points from the datasheet graph, the multi-variable Newton-Raphson method was applied to equations (A.3.7.2) and (A.3.7.3) to solve for values of V_j and M. Initial values of 2 and 0.4 respectively were used. Convergence of the iterative solution to within a tolerance of 0.0001 was achieved within 3 iterations to yield values of $V_j = 2.0609\,\text{V}$ and $M = 0.4283$.

Figure A.7a shows the simulated characteristic capacitances for the parameter values extracted above, overlaid on the original datasheet plot. Good matching of the input capacitance (red) is observed over the entire drain-source voltage range.

A.4.2.3 Body diode characteristics

The remaining model parameters to be extracted are the body diode characteristics. Body diode forward conduction characteristics are presented in the device datasheet on a logarithmic current scale and linear voltage scale. The datasheet graph is an ideal candidate for digitisation, allowing linear regression to be used to extract the diode model parameters. The forward characteristics graph, from datasheet Figure 25, was digitised and linear regression used to fit a straight line to the data as outlined in Section A.3.1. The series resistance value, R_s, used in the calculation of the regression variables was optimised to minimise the R^2



(a) (b)

Figure A.8: Simulation of modelled body diode characteristics for CSD86350Q5D "Sync" power MOSFET. (a) Forward characteristics (magenta) overlaid on original datasheet plot [57]. (b) Reverse recovery waveform for datasheet test conditions with diode current plotted against time.

value for the linear regression. An R^2 value of 0.9994 was achieved with a value of $R_s = 53.4\,\text{m}\Omega$. The gradient and intercept of the resulting fitted line were $m = 0.68550$ and $c =$ -17.508 respectively. From this result values for the remaining parameters were calculated as $N = 1.4588$ and $IS = 2.4908 \times 10^{-8}$.

A single parameter, TT, controls the reverse recovery behaviour of the model. To determine a suitable value for this parameter a simulation of the MOSFET model was performed in LTspice at the test conditions presented in "Diode characteristics" portion of the "Electrical characteristics" datasheet table. A sweep of the TT parameter value was performed to achieve a match for the reverse recovery time of 32 ns at the test conditions. From the simulation results a value of $TT = 30 \times 10^{-9}$ was selected. As a rule of thumb this value will be roughly equal to the reverse recovery time (32 ns) for the typical low-voltage power MOSFET reverse recovery test conditions.

Figure A.8a shows the simulated forward characteristics for the body diode, overlaid on the original datasheet plot. It can be seen that excellent matching is achieved over the entire operating range. The simulated reverse recovery waveform for the body diode is presented in Figure A.8b. The simulated waveform shows that the reverse recovery time of 32 ns has been matched.

A.4.2.4 LTSpice model statement

Presented in Figure A.9 is the final LTspice `.model` statement for the low-side device ("Sync" MOSFET) in the CSD86350Q5D power MOSFET pair. The model commands are presented in a multi-line format for readability, but can be simply condensed into a single line format (for inclusion in the LTspice "standard.mos" MOSFET library, for example).

```
* LTSpice VDMOS model for TI CSD86350Q5D "Sync" MOSFET (low-side device)
.model CSD86350Q5D_Sync VDMOS(
+ KP=302 VTO=1.4383 LAMBDA=0.1
+ mtriode=2.1 subthres=0.46
+ RS=1.65m RD=0 RG=1.4
+ CGS=3063.4p
+ CGDMAX=415.34p CGDMIN=-9.72e-12 a=0.23734
+ Cjo=3483p m=0.4283 Vj=2.0609
+ IS=24.908n N=1.4588 RB=0.534m
+ TT=30n )
```

Figure A.9: LTspice VDMOS model for the Texas Instruments CSD86350Q5D "Sync" power MOSFET, extracted from datasheet parameters.

A.4.3 Modelling of the IDD12SG60C SiC Schottky diode

The IDD12SG60C is a silicon carbide (SiC) Schottky diode manufactured by Infineon Technologies [58]. The key features of this device are a reverse voltage rating of 600 V and a continuous forward current rating of 12 A. The device is available in the TO-252 (DPAK) package.

Parameters to be modelled include the forward conduction characteristics and junction capacitance. Reverse recovery does not need to be modelled as the device is a Schottky diode and hence, does not undergo forward or reverse recovery. For the purposes of modelling the device, the information of interest on the datasheet includes the typical forward characteristic graph (datasheet Figure 3) and the typical capacitance vs. reverse voltage graph (datasheet Figure 8). Modelling is conducted for a junction temperature of 25 °C.

Forward characteristics are provided for forwards currents on a linear scale from 0 A to 20 A, for a number of junction temperatures. Corresponding forward voltages are also reported on a linear scale. Due to the choice of linear scaling and the overlap of multiple characteristic curves, only a limited number of useful data points can be extracted from this graph. For this reason the three-point method is selected for the extraction of the DC parameters.

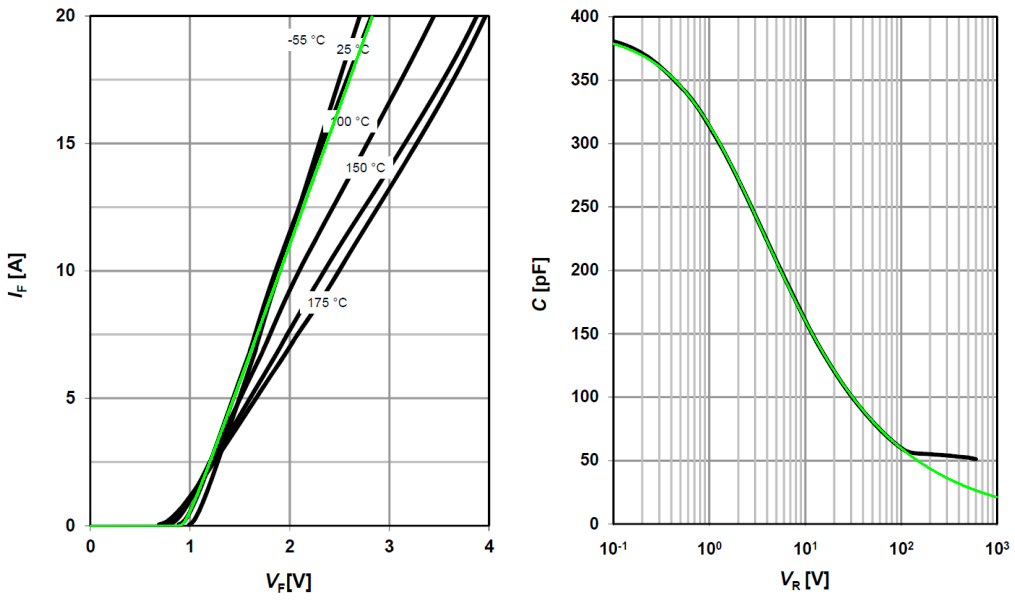
Three forward-current, forward-voltage pairs (i_f, v_f) were extracted from the datasheet graph in Amps and Volts respectively: $(0.1983, 0.9493)$, $(1.1048, 1.0797)$ and $(19.7734, 2.8044)$. Applying the three-point extraction method to these data points yielded the following model parameter values: $IS = 4.195 \times 10^{-15}$, $N = 1.152$ and $RS = 8.781 \times 10^{-2}\,\Omega$.

Figure A.10a plots the modelled forward characteristics overlaid on the original datasheet graph. A good fit is observed for currents less than 7 A and for currents above 17 A. Between these values the simulated forward characteristics do depart from the datasheet graph slightly, but at all times remains within 50 mV of the forward voltage reported on the datasheet.

The typical capacitance is reported on a linear scale against reverse voltage on a logarithmic scale. This graph is an ideal candidate for digitising and data points can be accurately interpolated for the entire length of the curve. As a large number of data points are available, linear regression with a fixed V_j is selected as the parameter extraction technique.

On plotting the regression quantities is was noted that above approximately 100 V reverse voltage the typical curve departs from the ideal behaviour. All data points above 100 V were therefore excluded from the regression analysis. Linear regression was performed on the remaining data points with V_j as a parameter. The optimum value for V_j was determined by maximising the R^2 value for the regression. The optimum value for V_j was found to be 1.7 V which resulted in an R^2 value of 0.999956. The remaining model parameters were determined from the linear regression. The resulting model parameters were: $C_{j0} = 3.8975 \times 10^{-10}$, $M = 0.4584$ and $V_j = 1.7\,\mathrm{V}$.

The diode capacitance test circuit was used to validate the extracted parameters. Figure A.10b plots the modelled typical capacitance characteristics overlaid on the original datasheet graph. It can be seen that the simulated results fit the datasheet curve extremely well for reverse voltages below 100 V. Between 100 V and 600 V the modelled capacitance is underestimated, however, the maximum excursion over this range was less than 25 pF.



(a) (b)

Figure A.10: Simulation of extracted model for the IDD12SG60C SiC Schottky diode (green) overlaid on original datasheet plots [58]. (a) Forward characteristics. (b) Capacitance vs. reverse voltage.

A.4.3.1 LTspice model statement

Presented in Figure A.11 is the LTspice `.model` statement for the IDD12SG60C SiC Schottky diode, incorporating all the parameters extracted in the above section. The model command is presented in a multi-line format for readability, but can be simply condensed into a single line format (for inclusion in the LTspice "standard.dio" diode library, for example).

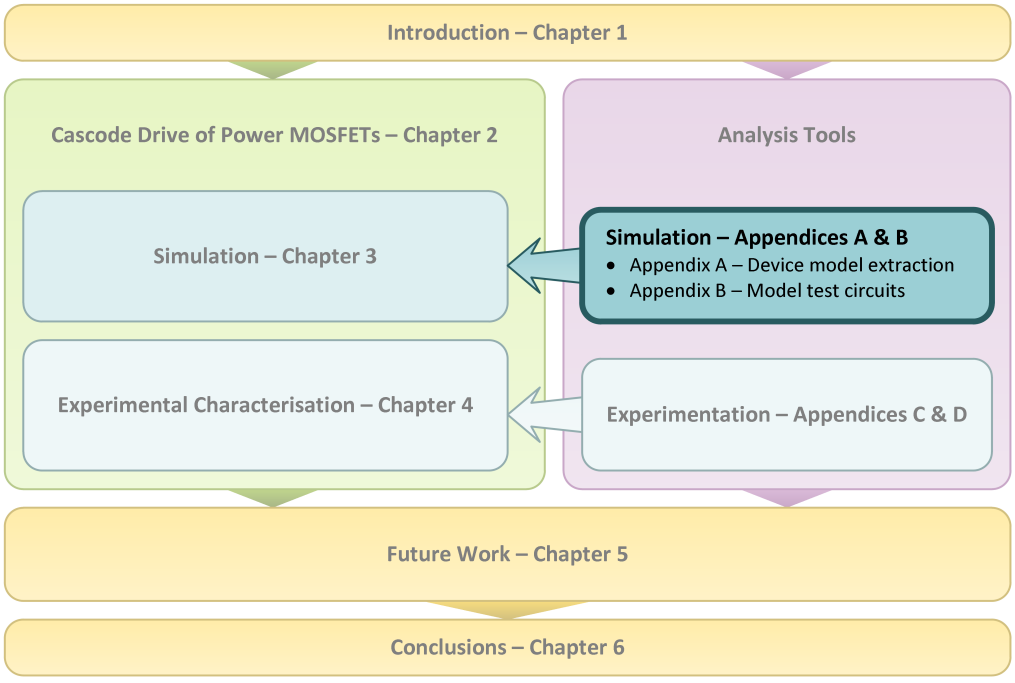
```
* LTSpice diode model for Infineon IDD12SG60C 600V SiC Schottky diode
.model IDD12SG60C D(
+ Is=2.394e-29 N=0.5594 Rs=9.158e-2
+ M=0.45841 Vj=1.7 Cjo=389.75p FC=0.5 )
```

Figure A.11: LTspice diode model for Infineon IDD12SG60C 600 V SiC Schottky diode extracted from datasheet parameters.

Appendix B

Simulation circuits for semiconductor model validation

This appendix documents LTspice circuits for use in modelling of power semiconductor devices, specifically diodes and MOSFETs. These test circuits have been designed to allow comparison of modelled devices to typical characteristics graphs provided in manufacturer datasheets. A graphical LTspice schematic is provided for each circuit along with a brief description of usage and a listing of the generated SPICE code. Additionally an example output plot is provided for each circuit.



B.1 Diode forward characteristics

Diode forward characteristics are generated by performing a DC sweep of forward current over the range of interest and measuring the resulting forward voltage drop across the diode. The forward current range is specified by the `.dc` dot command (see Figs B.1 and B.3). The resulting plot in LTspice (see Fig. B.2) has the axes reversed compared with what would typically be seen on a datasheet (i.e. forward voltage would usually be plotted on the horizontal axis) making it difficult to compare the results by inspection; either the LTspice plot or the datasheet figure must be manipulated (rotated/flipped) to perform a good comparison.

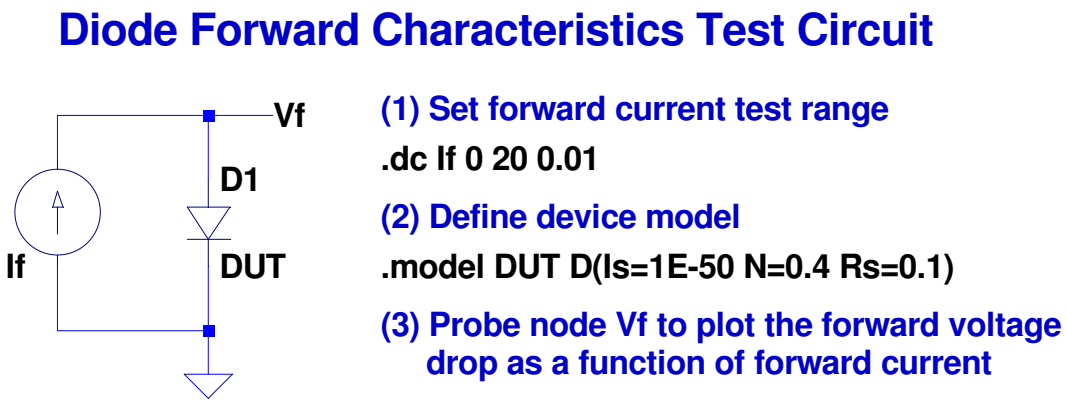


Figure B.1: LTspice test circuit for diode forward characteristics.

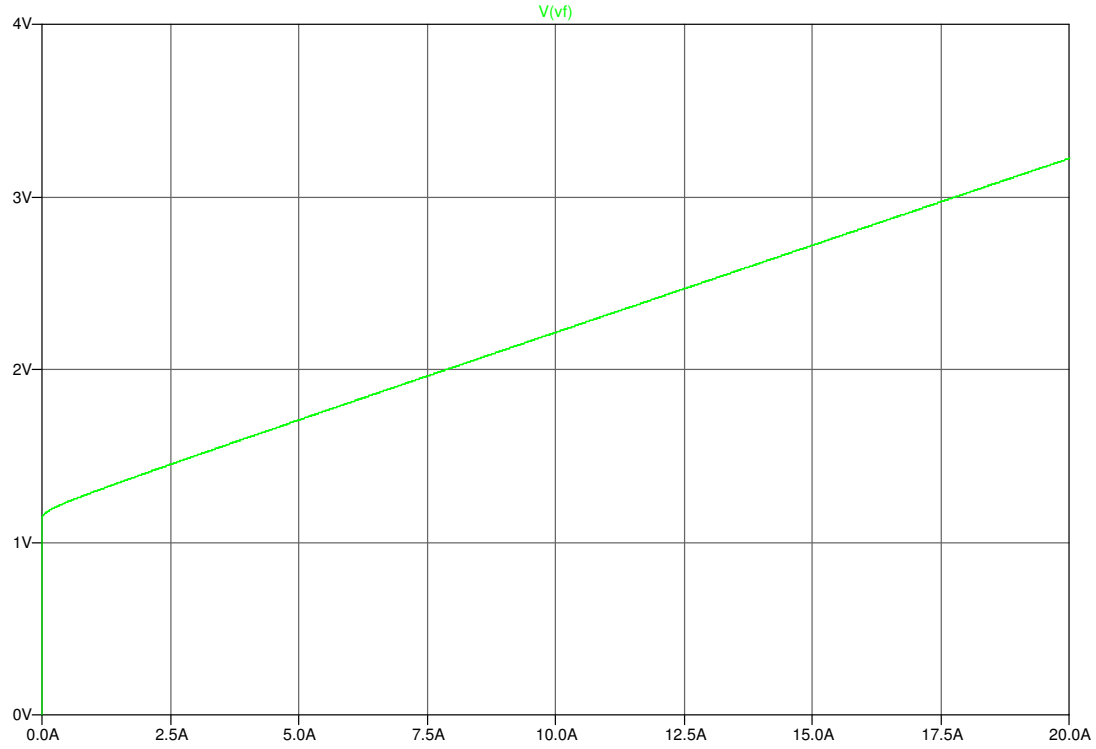


Figure B.2: Example output of diode forward characteristics test circuit.

```
***
*  Diode Forward Characteristic Test Circuit
*
*  Plots forward voltage as a function of forward current.
*
*  USAGE: (1) Set the range for forward current, If
*             (default = 0-20A)
*         (2) Define the device model (DUT)
*         (3) The voltage at node Vf gives diode forward voltage
*
*  Author:    Mark Broadmeadow
*  Date:      19/11/2013
*

* SIMULATION COMMAND & PARAMETERS
.dc If 0 20 0.01 ; Set the test current range here

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT D(Is=1E-50 N=0.4 Rs=0.1)

* CIRCUIT
If 0 Vf 0
D1 Vf 0 DUT

.backanno
.end
```

Figure B.3: LTspice netlist for testing diode forward characteristics.

B.2 Diode junction capacitance

Diode junction capacitance measured by performing an AC analysis at the relevant test frequency (typically 1 MHz). The test frequency is specified by the parameter `freq` (see Figs B.4 and B.6). The small signal AC excitation is provided by a voltage source, Vr, with a default AC amplitude of 1 V. The AC analysis is performed for a range of reverse bias voltages specified with a `.step` command. Capacitance is calculated from the AC current supplied by the voltage source and the test frequency parameter using a behavioural voltage source. The voltage measured at node Cj in Volts corresponds to the junction capacitance in Farads (see Fig. B.5).

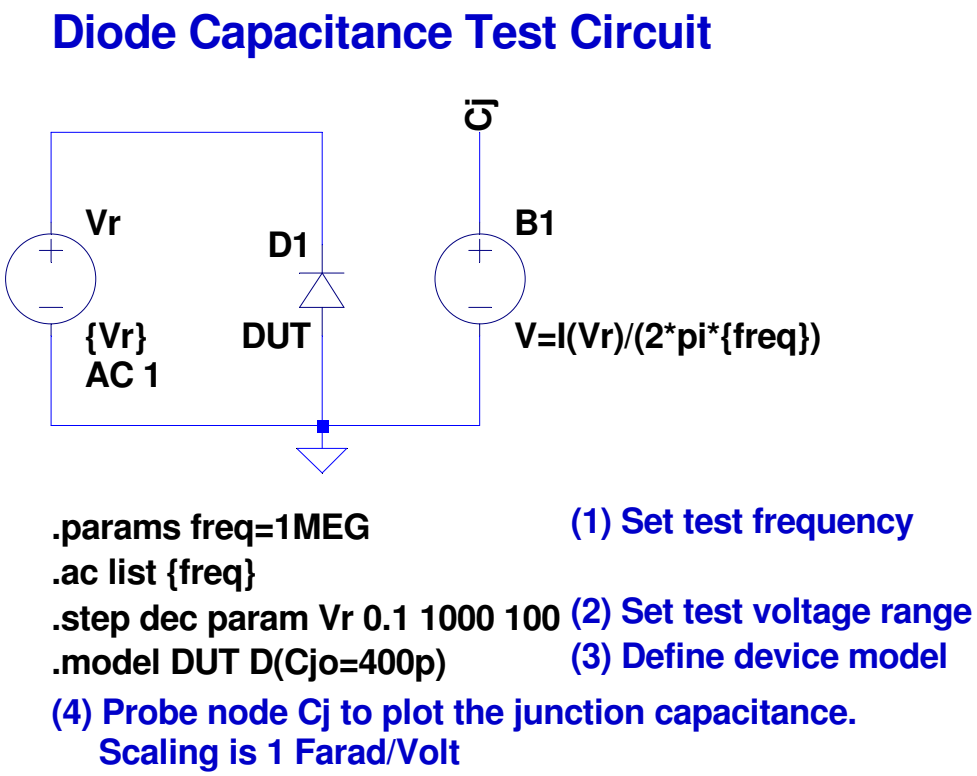


Figure B.4: LTspice test circuit for diode junction capacitance.

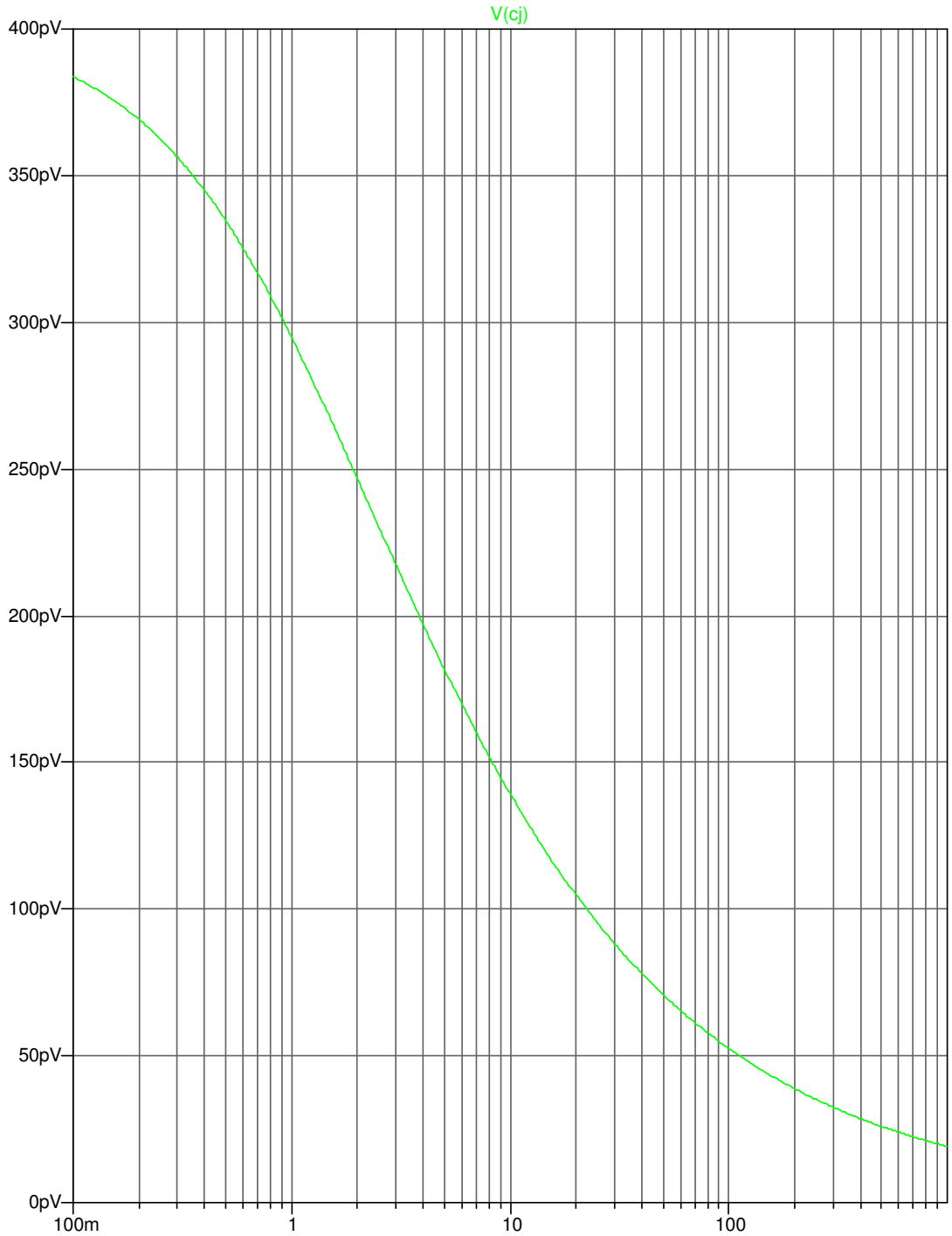


Figure B.5: Example output of diode junction capacitance test circuit.

```
***
*  Diode Capacitance Test Circuit
*
*  Plots junction capacitance as a function of Vr
*
*  USAGE: (1) Set the test frequency (default = 1MHz)
*         (2) Set the range for Vr (default = 0-1000V)
*         (3) Define the device model (DUT)
*         (4) Voltage at node Cj gives the junction
*             capacitance scaled to 1 Farad/Volt
*
*  Author:    Mark Broadmeadow
*  Date:      18/11/2013
*

* SIMULATION PARAMETERS
.params freq=1MEG                ; Set the test frequency here
.step dec param Vr 0.1 1000 100  ; Set the test voltage range here

* SIMULATION COMMAND
.ac list {freq}

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT D(Cjo=400p)

* CIRCUIT
Vr K 0 {Vr} AC 1
D1 0 K DUT

* Capacitance calculation (1 Farad/Volt)
B1 Cj 0 V=I(Vr)/(2*pi*{freq})

.backanno
.end
```

Figure B.6: LTspice netlist for testing diode junction capacitance.

B.3 MOSFET output characteristics

MOSFET output characteristics are generated by performing a DC sweep of drain-source voltage and plotting the resulting drain current. The drain-source voltage range is specified by the `.dc` dot command (see Figs B.7 and B.9). Sweeps are repeated for a range of gate-source bias voltages specified by the `.step` command. The example output plot (see Fig. B.8) has been annotated with the gate-source voltage corresponding to each trace.

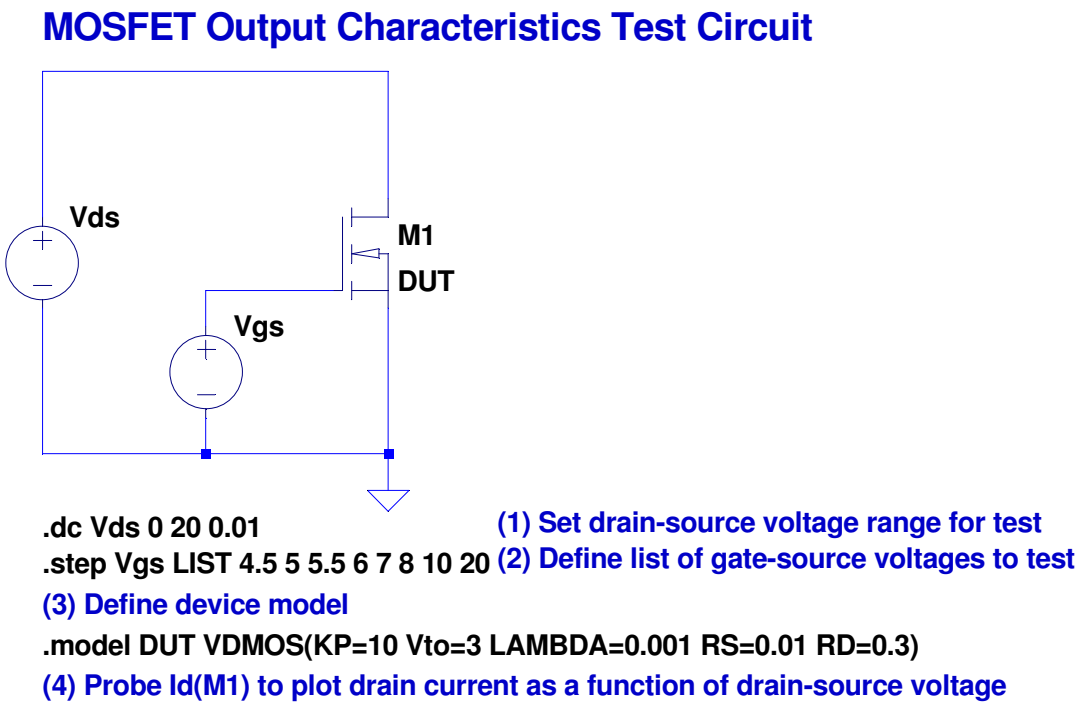


Figure B.7: LTspice test circuit for MOSFET output characteristics.

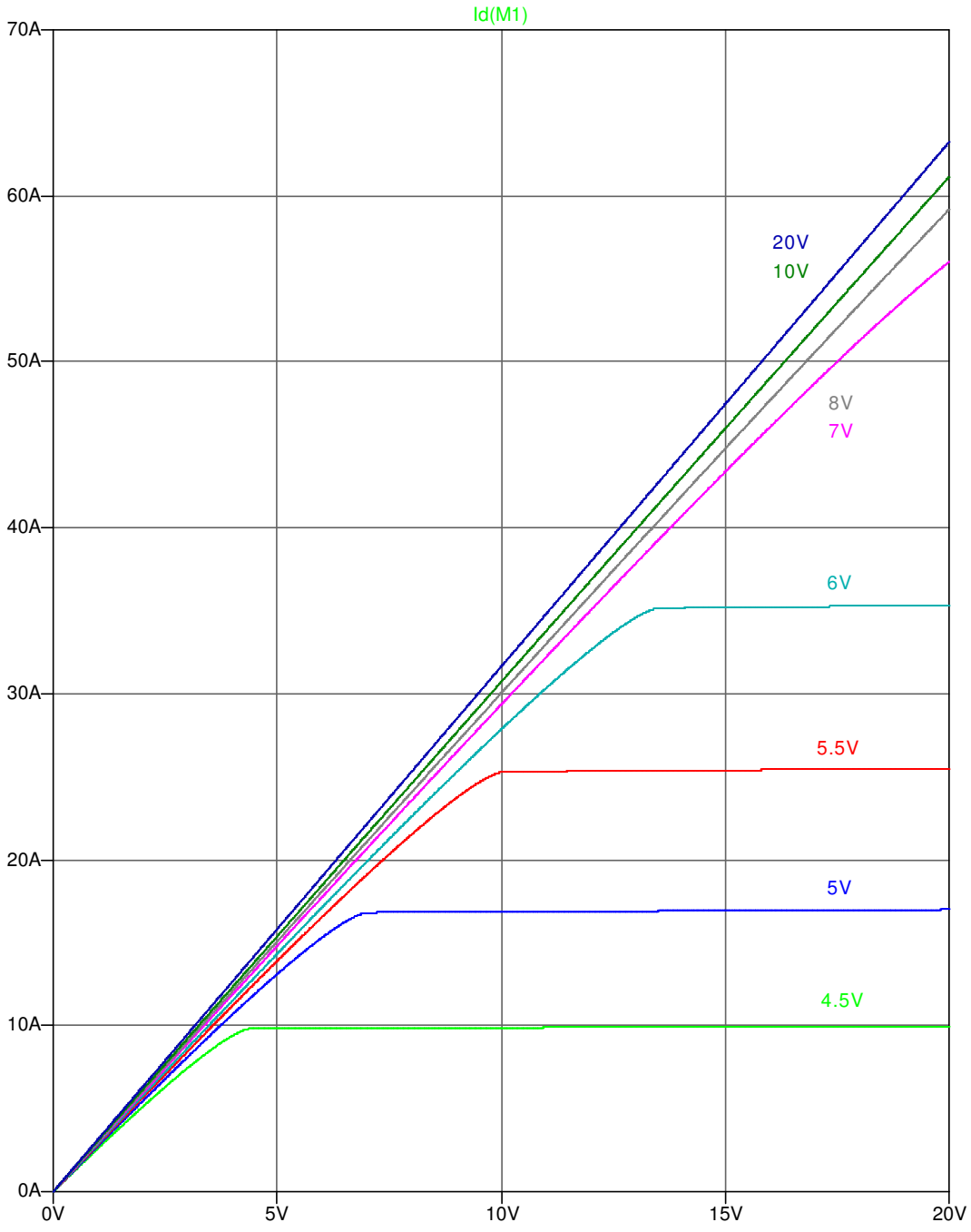


Figure B.8: Example output of MOSFET output characteristics test circuit.

```
***
*  MOSFET Output chracteristics Test Circuit
*
*  Plots drain current as a function of applied drain-source voltage,
*  with gate-source bias voltage as a parameter.
*
*  USAGE: (1) Set drain-source voltage range for test (default = 0-20V)
*         (2) Define the list of gate-source voltages to test
*         (3) Define the device model (DUT)
*         (4) Probe Id(M1) to plot drain current as a function
*             of drain-source voltage
*
*  Author:    Mark Broadmeadow
*  Date:      15/11/2013
*

* SIMULATION PARAMETERS
.step Vgs LIST 4.5 5 5.5 6 7 8 10 20    ; Define list of Vgs here

* SIMULATION COMMAND
.dc Vds 0 20 0.01    ; Set drain-source voltage range here

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT VDMOS(KP=10 Vto=3 LAMBDA=0.001 RS=0.01 RD=0.3)

* CIRCUIT
M1 D G 0 0 DUT
Vgs G 0 0
Vds D 0 0

.backanno
.end
```

Figure B.9: LTspice netlist for testing MOSFET output characteristics.

B.4 MOSFET transfer characteristics

MOSFET transfer characteristics are generated by performing a DC sweep of the gate-source voltage and plotting the resulting drain current for a fixed drain-source voltage (see Fig. B.11). The gate-source voltage range is specified by the `.dc` dot command (see Figs B.10 and B.12). The drain-source voltage is defined by voltage source Vds.

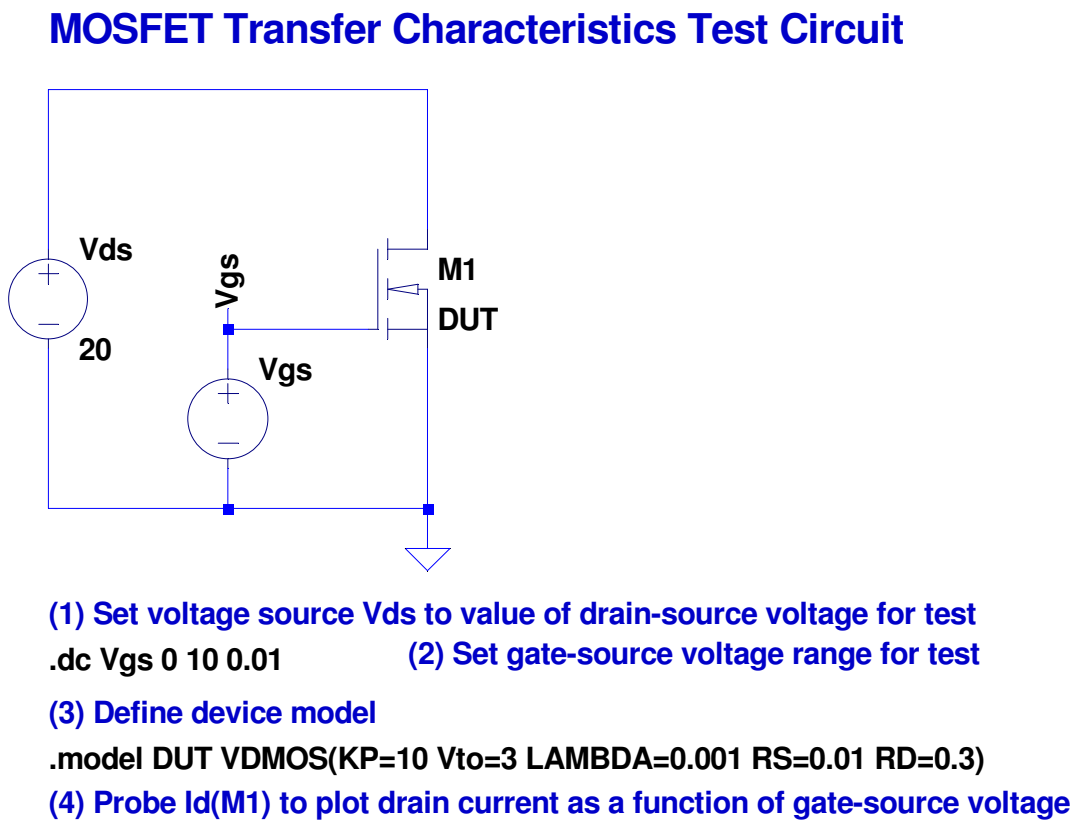


Figure B.10: LTspice test circuit for MOSFET transfer characteristics.

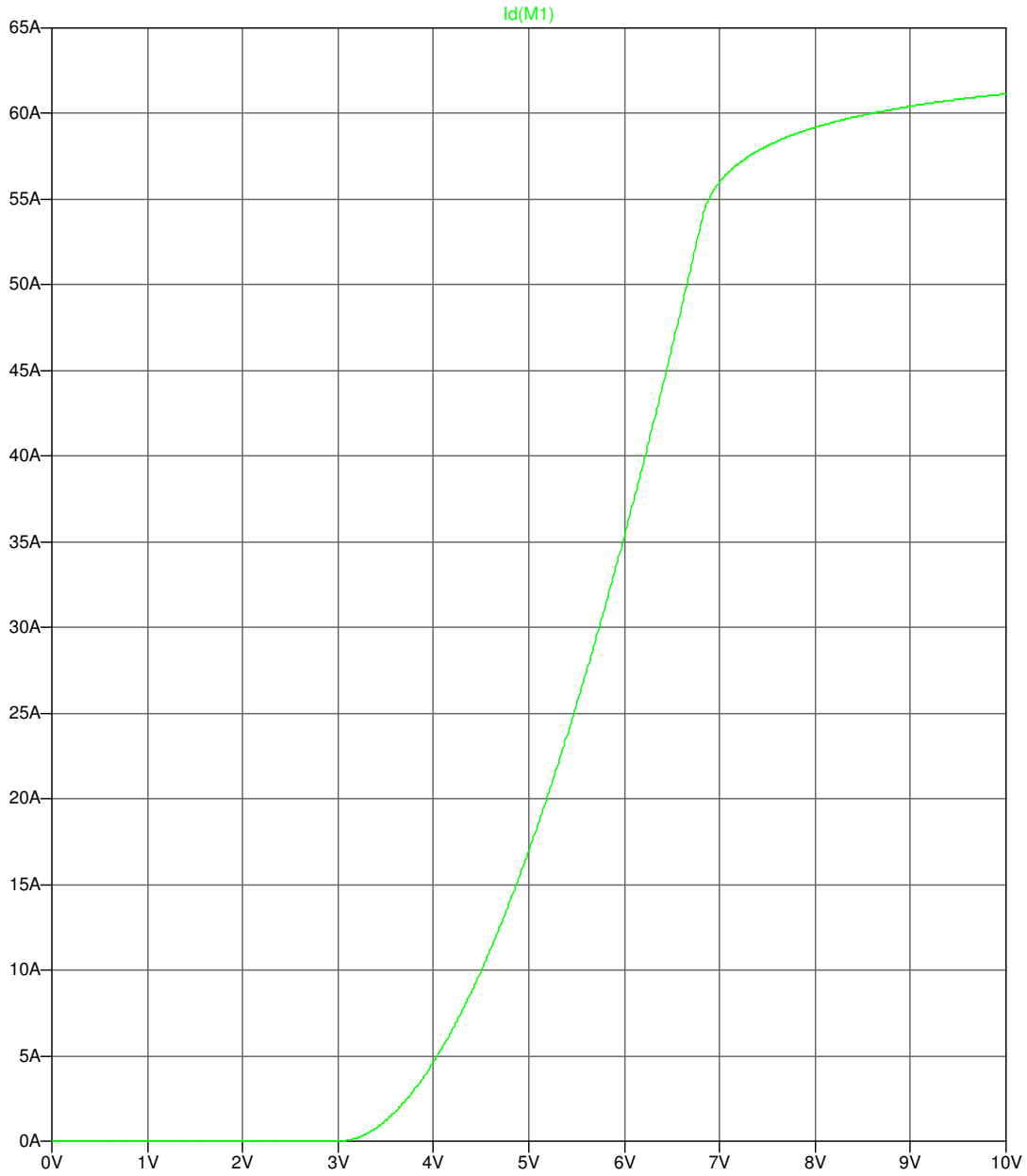


Figure B.11: Example output of MOSFET transfer characteristics test circuit.

```
***
*  MOSFET Output chracteristics Test Circuit
*
*  Plots drain current as a function of applied drain-source voltage,
*  with gate-source bias voltage as a parameter.
*
*  USAGE: (1) Set voltage source Vds to value of drain-source voltage for test
*         (2) Set drain-source voltage range for test (default = 0-10V)
*         (3) Define the device model (DUT)
*         (4) Probe Id(M1) to plot drain current as a function
*             of gate-source voltage
*
*  Author:    Mark Broadmeadow
*  Date:      15/11/2013
*

* SIMULATION COMMAND
.dc Vgs 0 10 0.01    ; Set gate-source voltage range here

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT VDMOS(KP=10 Vto=3 LAMBDA=0.001 RS=0.01 RD=0.3)

* CIRCUIT
M1 D Vgs 0 0 DUT
Vgs Vgs 0 0
Vds D 0 20           ; Set value for Vds here

.backanno
.end
```

Figure B.12: LTspice netlist for testing MOSFET transfer characteristics.

B.5 MOSFET gate charge

MOSFET gate charge characteristics are determined for a fixed maximum drain current and clamped drain source voltage. The gate charge of the MOSFET is controlled by injecting a fixed current of 1 nA into the gate; the total gate charge is therefore proportional to the simulation time with 1 s of simulation time corresponding to 1 nC of gate charge. Plotting the gate-source voltage against simulation time yields the gate charge characteristic (see Fig. B.14). The total gate charge range for the test is specified by the simulation end time parameter of the `.tran` command (see Figs B.13 and B.15). The maximum drain current is controlled by current source IL; the value of this current should be matched to the pulsed test current specified on the datasheet. The drain-source voltage is clamped through an ideal diode to a maximum value specified by voltage source Vdss. The simulation is performed for the list of drain-source clamping voltages specified in the `.step` command. The example output plot (see Fig. B.14) has been annotated with the drain-source voltage corresponding to each trace.

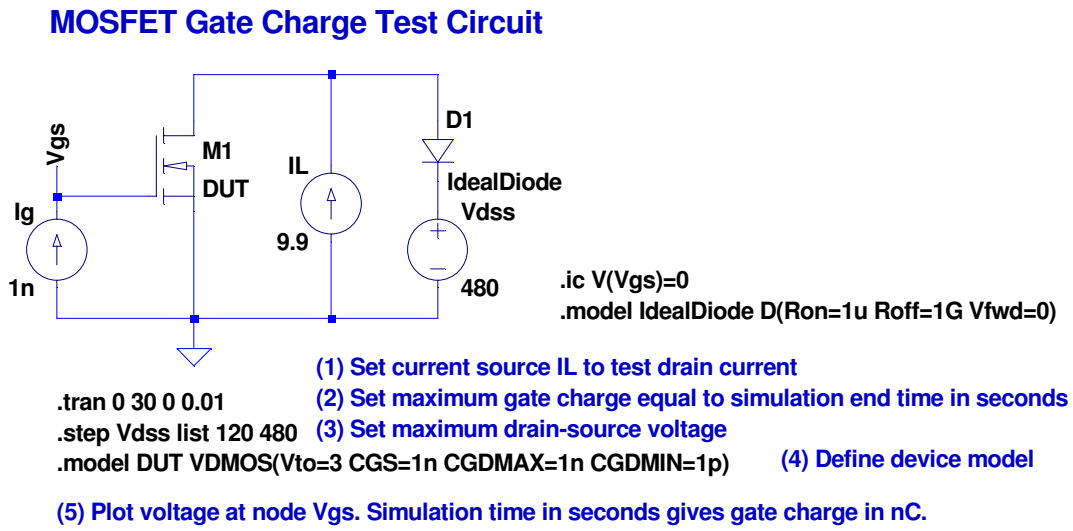


Figure B.13: LTspice test circuit for MOSFET gate charge.

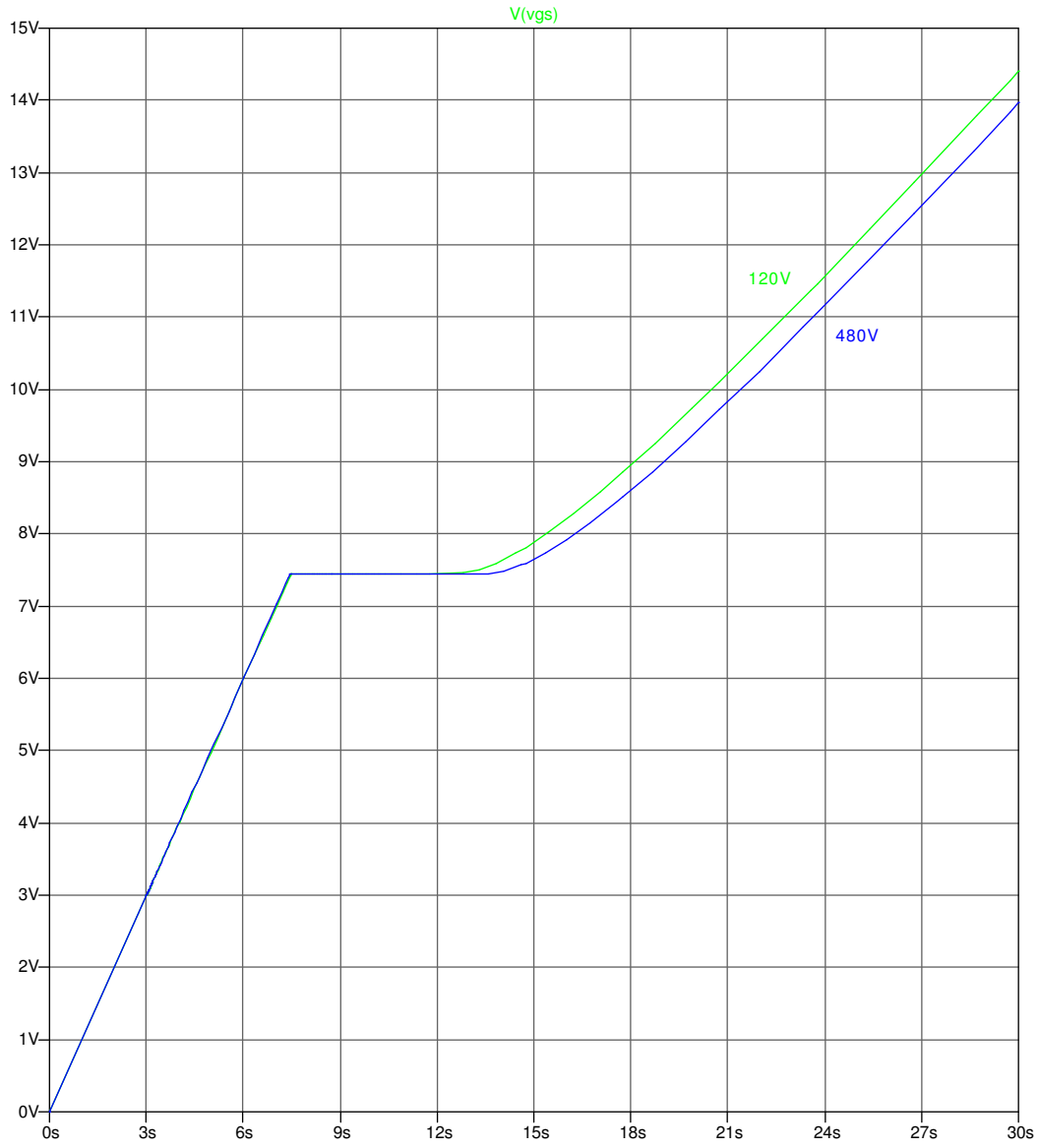


Figure B.14: Example output of MOSFET gate charge test circuit.

```
***
*  MOSFET Gate Charge Test Circuit
*
*  Plots Vgs against gate charge for a set of maximum drain-source voltages.
*
*  USAGE: (1) Set current source IL to the pulsed drain current for the test
*         (2) Set the simulation end time in seconds equal to the
*             maximum gate charge in nC
*         (3) Provide a set the maximum drain-source voltages
*         (4) Define the device model (DUT)
*         (4) Plot the gate-source voltage at node Vgs.
*             Simulation time in seconds gives gate charge in nC.
*
*  Author:    Mark Broadmeadow
*  Date:      14/11/2013
*

* SIMULATION PARAMETERS
.step Vdss list 120 480   ; Set the list of test voltages here

* SIMULATION COMMAND
.tran 0 30 0 0.01         ; Set the simulation end time here

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT VDMOS(Vto=3 CGS=1n CGDMAX=1n CGDMIN=1p)

* OTHER DIRECTIVES
.ic V(Vgs)=0
.model IdealDiode D(Ron=1u Roff=1G Vfwd=0)

* CIRCUIT
M1 Vd Vgs 0 0 DUT
Ig 0 Vgs 1n
IL 0 Vd 9.9               ; Set the test current here
Vdss Vclamp 0 480
D1 Vd Vclamp IdealDiode

.backanno
.end
```

Figure B.15: LTspice netlist for testing MOSFET gate charge.

B.6 MOSFET capacitances

MOSFET characteristic capacitances are measured by performing an AC analysis at the relevant test frequency (typically 1 MHz). The test frequency is specified by the parameter `freq` (see Figs B.16 and B.18). The small signal AC excitation is provided by voltage sources Vds and Vgs respectively. An AC amplitude of 1 V is used for the drain source excitation while 0.1 V is used for the gate-source excitation. The AC analysis is performed for a range of applied drain-source voltages specified with the `.step` command. Capacitance is calculated from the AC current supplied by the excitation sources, adjusted by the test frequency parameter and excitation voltage amplitude using a behavioural voltage source. The voltages measured, in Volts, at each of nodes Ciss, Coss and Crss correspond to the respective characteristic capacitances, measured in Farads (see Fig. B.17).

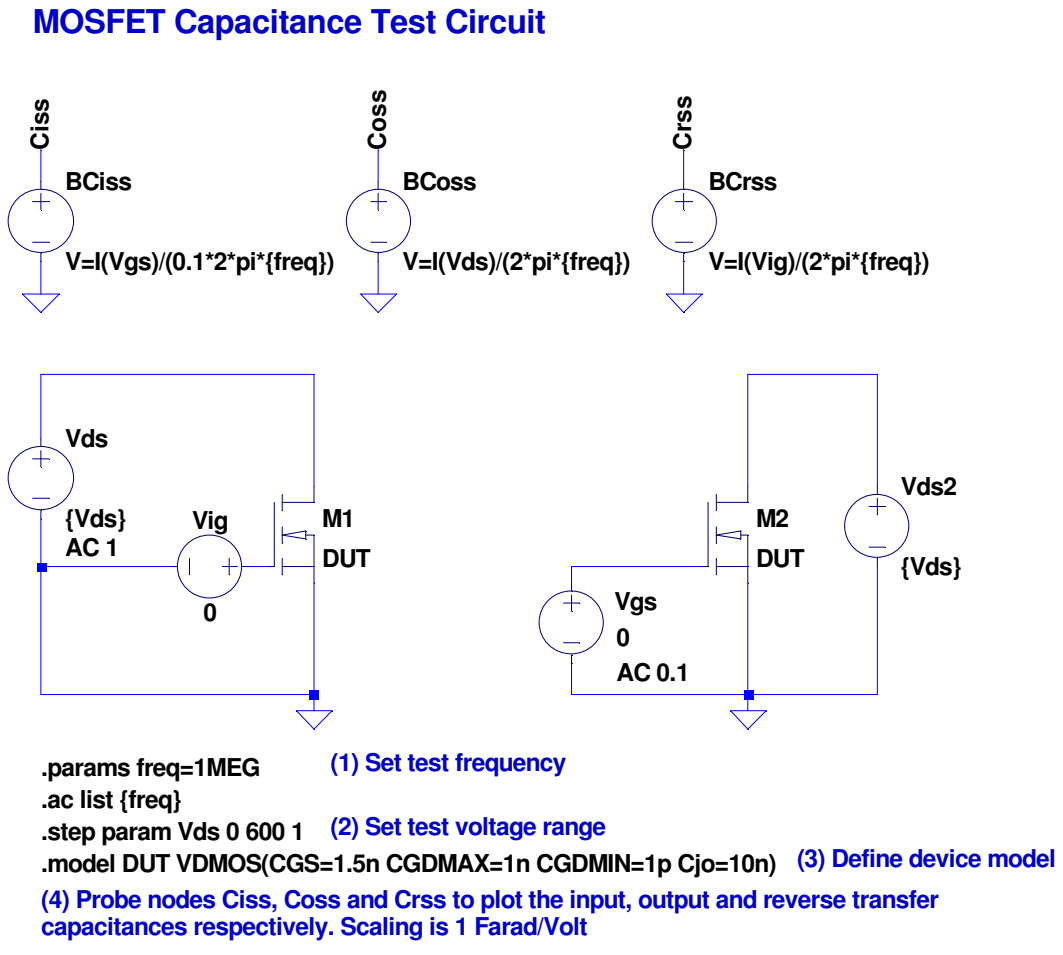


Figure B.16: LTspice test circuit for MOSFET characteristic capacitances.

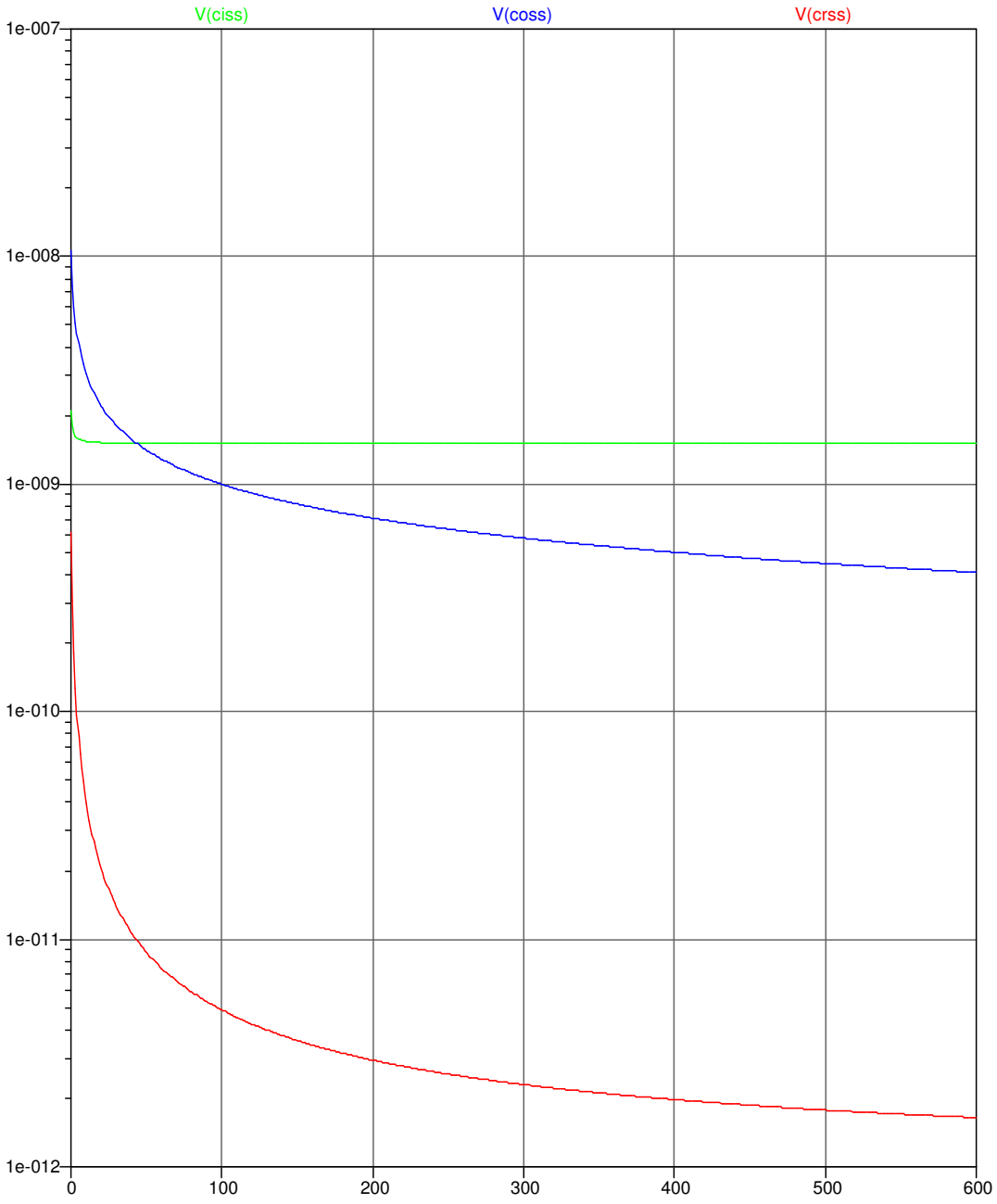


Figure B.17: Example output of MOSFET characteristic capacitances test circuit.

```
***
*  MOSFET Capacitance Test Circuit
*
*  Plots Ciss, Coss and Crss as a function of Vds
*
*  USAGE: (1) Set the test frequency (default = 1MHz)
*         (2) Set the range for Vds (default = 0-600V)
*         (3) Define the device model (DUT)
*         (4) Voltages at nodes Ciss, Coss & Crss give
*             the capacitances scaled to 1 Farad/Volt
*
*  Author:    Mark Broadmeadow
*  Date:      12/11/2013
*

* SIMULATION PARAMETERS
.params freq=1MEG        ; Set the test frequency here
.step param Vds 0 600 1  ; Set the test voltage range here

* SIMULATION COMMAND
.ac list {freq}

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT VDMOS(CGS=1.5n CGDMAX=1n CGDMIN=1p Cjo=10n)

* Coss & Crss extraction circuit
M1 D1 G1 0 0 DUT
Vds D1 0 {Vds} AC 1
Vig G1 0 0

* Ciss extraction circuit
M2 D2 G2 0 0 DUT
Vgs G2 0 0 AC 0.1
Vds2 D2 0 {Vds}

* Capacitance calculation (1 Farad/Volt)
BCiss Ciss 0 V=I(Vgs)/(0.1*2*pi*{freq})
BCoss Coss 0 V=I(Vds)/(2*pi*{freq})
BCrss Crss 0 V=I(Vig)/(2*pi*{freq})

.backanno
.end
```

Figure B.18: LTspice netlist for testing MOSFET characteristic capacitances.

B.7 MOSFET body diode forward characteristics

MOSFET body diode forward characteristics are measured in exactly the same manner as described for a standard diode in Section B.1. In this version of the test circuit (see Figs B.19 and B.3) the diode is simply replaced by a MOSFET with its gate and source terminals shorted. The body diode forward voltage is measured by plotting the source-drain voltage (see Fig. B.20).

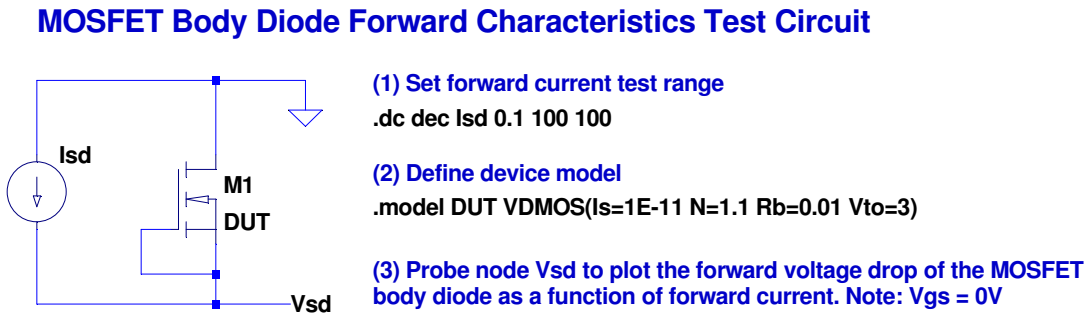


Figure B.19: LTspice test circuit for body diode forward characteristics.

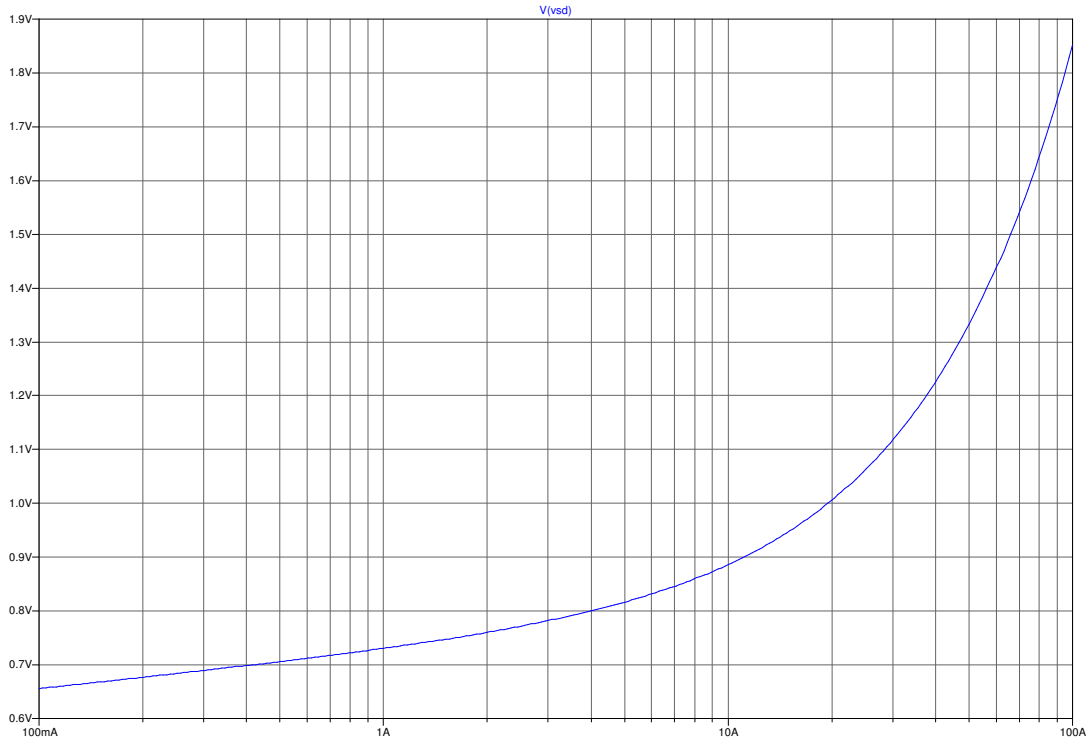


Figure B.20: Example output of body diode forward characteristics test circuit.

```
***
*  MOSFET Body Diode Forward Characteristic Test Circuit
*
*  Plots Vsd as a function of source-drain current
*
*  USAGE: (1) Set the range for forward current, Isd
*             (default = 100mA-100A)
*         (2) Define the device model (DUT)
*         (3) The voltage at node Vsd gives
*             the body diode forward voltage
*
*  Author:    Mark Broadmeadow
*  Date:      19/11/2013
*

* SIMULATION COMMAND & PARAMETERS
.dc dec Isd 0.1 100 100 ; Set the test current range here

* MODEL FOR DEVICE UNDER TEST (DUT)
.model DUT VDMOS(Is=1E-11 N=1.1 Rb=0.01 Vto=3)

* CIRCUIT
M1 0 Vsd Vsd Vsd DUT
Isd 0 Vsd 0

.backanno
.end
```

Figure B.21: LTspice netlist for testing body diode forward characteristics.

B.8 Reverse recovery

Reverse recovery characteristics (for either a discrete diode or MOSFET body diode) are measured by performing a transient analysis at the appropriate test conditions. The test circuit is configured for a typical clamped inductive application, for which reverse recovery performance is usually specified. The forward test current is specified by parameter `If` while the current commutation speed is specified by parameter `didt` (in A/s). Parameter `Irm` must be set to a value higher than the expected peak reverse recovery current. Parameter `Vbus` sets the clamping voltage for the test (see Figs B.22 and B.24).

The device under test should be connected from the A (anode) to K (cathode) terminals – this configuration allows either a MOSFET or diode model to be tested without modification of the base circuit/netlist. Note that for a MOSFET test, its gate and source terminals should be shorted. The reverse recovery voltage and current waveforms can be measured between the A and K terminals (see Fig. B.23).

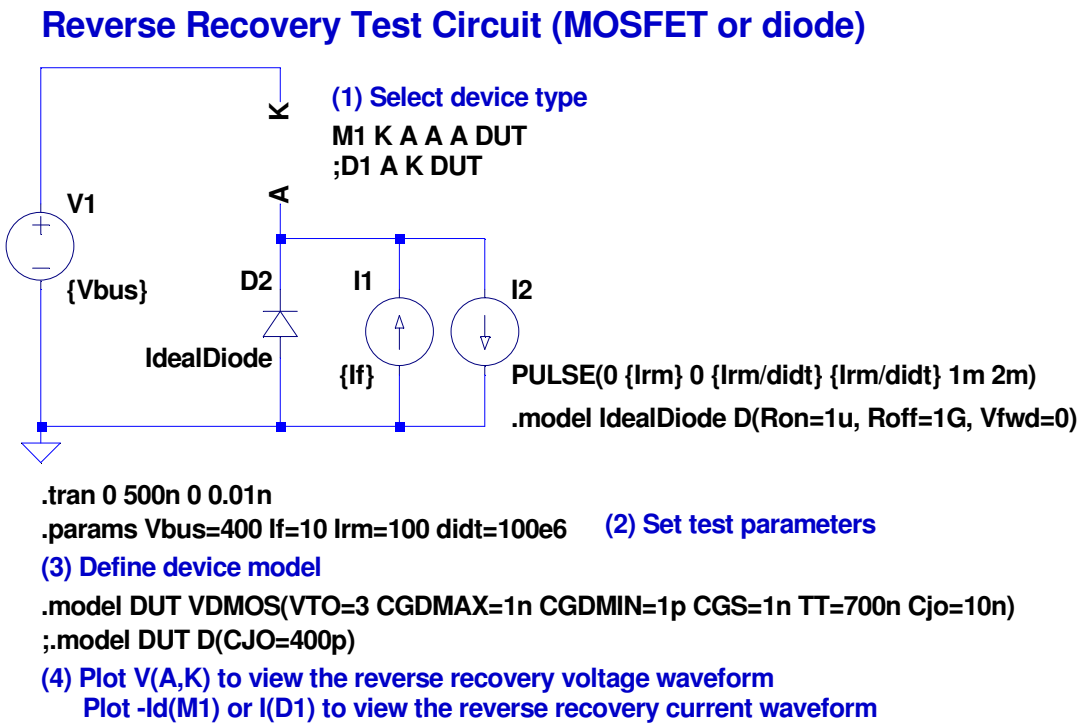


Figure B.22: LTspice test circuit for reverse recovery characteristics.

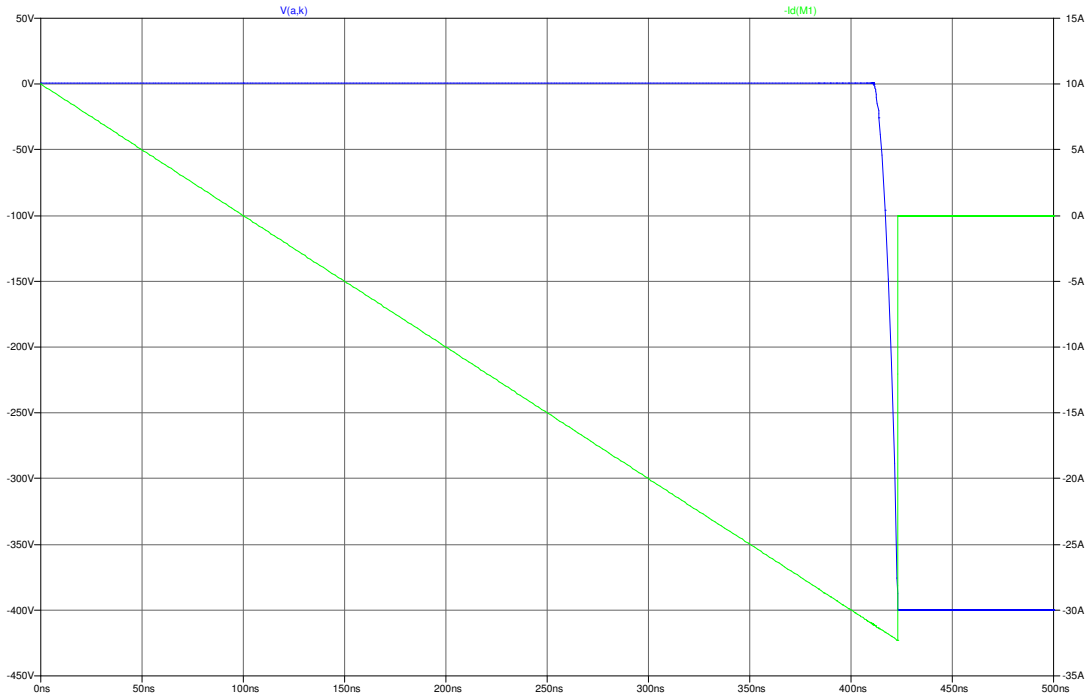


Figure B.23: Example output of reverse recovery characteristics test circuit.

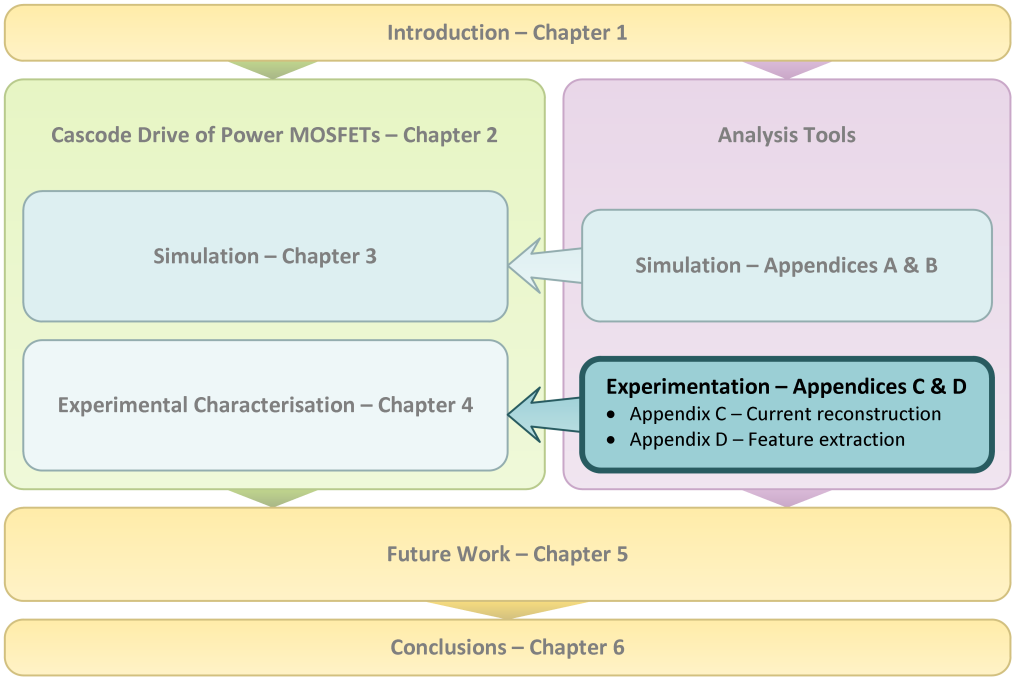
```
***
*  Reverse Recovery Test Circuit (MOSFET or diode)
*
*  Plots the reverse recovery voltage and current waveforms
*  for a MOSFET or diode.
*
*  USAGE: (1) Set reverse recovery test parameters
*             Vbus - Test reverse voltage (default = 400V)
*             If   - Test forward current (default = 10A)
*             Irm  - Reverse current (must be >> If + Irrm)
*             didt - Test di/dt in A/s (default = 100A/us)
*         (2) Selecte circuit element to test (MOSFET or diode)
*         (3) Define the device model (DUT)
*         (4) V(A,K) gives the reverse recovery voltage waveform
*             -Id(M1) or I(D1) gives the reverse recovery current waveform
*
*  Author:    Mark Broadmeadow
*  Date:      18/11/2013
*

* SIMULATION PARAMETERS
.params Vbus=400 If=10 Irm=100 didt=100e6    ; Define test parameters here

* SIMULATION COMMAND
.tran 0 500n 0 0.01n    ; Maximum simulation time can be adjusted here

* MODEL FOR DEVICE UNDER TEST (DUT) (Uncomment relevant device model)
.model DUT VDMOS(VTO=3 CGDMAX=1n CGDMIN=1p CGS=1n TT=700n Cjo=10n)
;.model DUT D(CJO=400p)

* OTHER DEVICE MODELS
.model IdealDiode D(Ron=1u, Roff=1G, Vfwd=0)

* CIRCUIT
V1 K 0 {Vbus}
D2 0 A IdealDiode
I1 0 A {If}
I2 A 0 PULSE(0 {Irm} 0 {Irm/didt} {Irm/didt} 1m 2m)

* DEVICE SELECTION
M1 K A A A DUT      ; Uncomment to select MOSFET
;D1 A K DUT         ; Uncomment to dlect diode

.backanno
.end
```

Figure B.24: LTspice netlist for testing reverse recovery characteristics.

Appendix C

Reconstruction of true current from di/dt polluted current shunt measurements

In this appendix a post-processing methodology for reconstruction of true current from di/dt polluted current shunt measurements is developed. Performance of the proposed reconstruction filter is analysed and the sensitivity of the filter to circuit parasitics and mismatched time-constants is explored. Finally, a novel method for tuning the reconstruction filter using experimental double-pulse switching waveforms is described.



C.1 Introduction

The use of resistive shunts to measure current is common practice. A small resistance is introduced in series with the current to be measured and the voltage across this resistor is measured. For a pure resistance the measured terminal voltage will be directly proportional to current. When used to measure switching transients the frequency response of the shunt resistor must be considered.

High rates of change of current ($\mathrm{d}i/\mathrm{dt}$) exist during the switching transition, often exceeding 200 A/µs. The contribution of parasitic series inductances to the terminal voltage of the shunt resistor can be of magnitudes exceeding the resistive contribution. In this appendix the effect of parasitic elements on current shunt measurements is discussed and a method for reconstructing the true current is presented.

C.2 Shunt resistor equivalent circuit

The lumped circuit model of a non-ideal resistor is shown below in Figure C.1 and consists of a series inductance and shunt capacitance. The value of the parasitic elements depends on a wide range of factors which can be broadly categorised into either resistor construction and placement in-circuit. Construction factors include resistor type (wire wound, thin film, foil etc.), package (leaded, 1206, 0603 etc.), method of trimming (L-cut, S-cut) and termination style (wrap around, flip chip etc.) [65]. The effect of resistor placement in-circuit is determined largely by the geometry of the current loop which will be affected by resistor placement and orientation, the routing of traces and placement of planes.

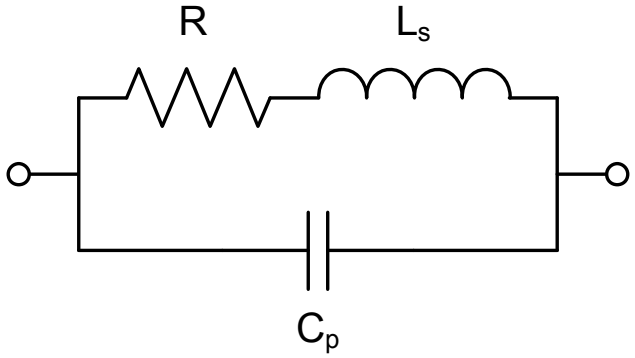


Figure C.1: Lumped circuit model of a non-ideal resistor.

C.2.1 Typical values for parasitic elements

For the purposes of this analysis, it is assumed that surface mount resistors are used for the current shunt. Current sense resistors are typically of a larger form factor than other surface mount resistors due to the need to carry high currents and dissipate comparatively high average or peak powers. An example of a typical resistor that may be used for current sense applications, and the current sense resistor used in this research, is the Vishay CSM2512 series foil resistor [66]. A resistance value of 100 mΩ is used in this research and will therefore be considered for further analysis. This value is relatively high (10 W dissipation at the nominal continuous current rating of the MOSFETs), however, as the primary purpose is the measure switching transients in low duty cycle tests, the higher V/A gain is preferred.

To consider the effect of the parasitic elements, reasonable bounds for their values must be determined. As discussed above, a wide range of factors affect the value of these parasitics. To consider a general case, a simplified geometry will be used and some basic assumptions will be made to provide an estimate of typical and worst case values for the parasitic elements.

For capacitance calculations the resistor geometry will be considered as an infinitely thin rectangular plate the same dimensions as a 2512 packaged resistor (l_r = 6.4 mm, w_r = 3.2 mm) mounted directly on top of the copper trace on a PCB (see Fig. C.2). Return current will be considered to flow on a parallel

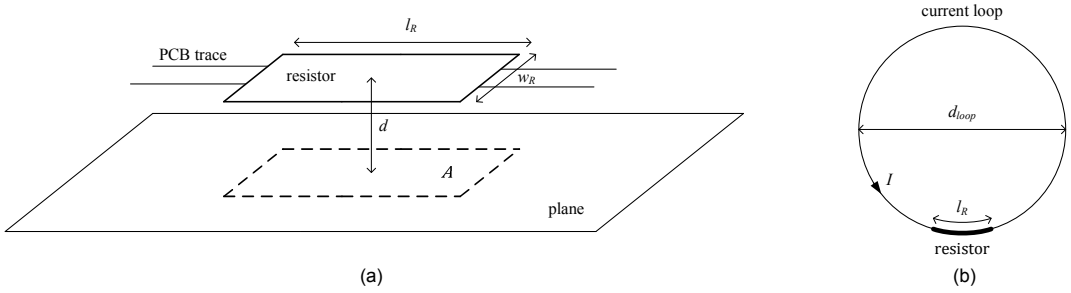


Figure C.2: Simplified geometries for estimation of values for (a) parasitic capacitance and (b) partial inductance.

Parameter	Typ.	Min./Max.	Notes
Resistor length, l_r	6.4 mm	-	*For 2512 resistor*
Resistor width, w_r	3.2 mm	-	*For 2512 resistor*
Separation distance, d	1.57 mm	254 µm	*Distance between adjacent layers for 2-(typ.) and 4-layer (min.) PCBs with* 1.6 mm *thickness*
Loop diameter, d_{loop}	20 mm	100 mm	*Single-layer lateral half-bridge layout*

Table C.1: Representative geometry parameters for calculating values for parasitic elements.

copper plane on a layer below the resistor, separated by some distance. For mutual partial inductance calculations the resistor will be considered as an arc segment of a circular loop of wire with a circular radius. The resistor segment will be taken to be the same length as a 2512 resistor ($l_r = 6.4\,\text{mm}$) and the diameter of the wire will be set to $0.443 \times w_r$ to give approximately the same self partial inductance for the resistor segment as if the resistor were considered to be a plane of width w_r with zero thickness [62]. Table C.1 summarises the values chosen as representative for typical and worst case for calculation of parasitics.

C.2.1.1 Capacitance calculation

The parasitic capacitance is modelled as two parallel plates of area A separated by distance d. The dielectric is assumed to be FR4 ($\epsilon_r = 4.7$). Equation (C.2) gives the capacitance for this geometry.

$$C = \epsilon_r \epsilon_0 \frac{A}{d} \tag{C.2.1.1}$$

Substituting the relevant geometric parameters into equation (C.2.1.1) yields:

$$C_p = 4.7\epsilon_0 \frac{l_r w_r}{d} \tag{C.2.1.2}$$

where C_p is the estimated parasitic capacitance of the current sense resistor based on the assumptions and geometry defined above.

C.2.1.2 Inductance calculation

The parasitic inductance is calculated by determining the partial inductance of the resistor segment within the current loop. The resistor is modelled as an arc segment of a circular current loop. As the loop is symmetrical, the ratio of the length of the resistor segment to the total loop circumference must be equal to the ratio of the partial inductance of the resistor segment to the loop inductance. For a loop radius, a, much larger than the radius of the conductor, r_w, the loop inductance of a circular loop can be approximated by:

$$L_{loop} = \mu_0 a \left(\ln \frac{8a}{r_w} - 2 \right) \qquad a \gg r_w \tag{C.2.1.3}$$

Substituting the relevant geometric parameters into equation (C.2.1.3) and calculating for the proportion of the loop inductance that can be attributed to the arc representing the resistor yields:

$$L_s = \frac{\mu_0}{2\pi} l_r \left[\ln \left(9.029 \frac{d_{loop}}{w_r} \right) - 2 \right] \tag{C.2.1.4}$$

where L_s is the estimated parasitic inductance of the current sense resistor based on the assumptions and geometry defined above.

C.2.1.3 Parasitic element bounds

Minimum and maximum bounds for the parasitic capacitance and inductance can be calculated based on Table C.1 using equations (C.2.1.2) and (C.2.1.4), respectively. Table C.2 summarises the expected bounds for parasitic elements of the current sense resistor used in this work.

Parameter	**Min.**	**Typ.**	**Max.**
Parasitic inductance, L_s (nH)	0	2.6	4.7
Parasitic capacitance, C_p (pF)	0	0.5	3.4

Table C.2: Estimated bounds and typical values for current sense resistor parasitics.

C.3 Reconstruction filter

Assuming that the parasitic shunt capacitance of the current sense resistor is negligible (validated in Section C.3.1.3), the transfer function that describes the relationship between the sense current and the resistor terminal voltage is:

$$\frac{V(s)}{I(s)} = R + sL_s = R\left(1 + s\frac{L_s}{R}\right) \tag{C.3.0.5}$$

where sL_s is the frequency dependant gain error term which we want to eliminate. We can apply a filter of the form:

$$G(s) = \frac{1}{1 + s\frac{L_s}{R}} \tag{C.3.0.6}$$

to compensate for the frequency dependant term in equation (C.3.0.5):

$$\frac{V'(s)}{I(s)} = \frac{V(s)G(s)}{I(s)} = R\left(1 + s\frac{L_s}{R}\right) \cdot \frac{1}{1 + s\frac{L_s}{R}} = R \tag{C.3.0.7}$$

The filter given by equation (C.3.0.6) is effectively a first-order low pass filter with a time constant given by L_s/R. This filter may be implemented in hardware by a simple RC network tuned such that $L_cR_c = L_s/R$. Alternatively, the voltage across the terminals of the current sense resistor can be measured and the recorded waveform post-processed to reconstruct the true current. If the post-processing option is used the filter given by equation (C.3.0.6) may be modified to additionally compensate for the gain of the current sense resistor:

$$H(s) = \frac{1}{R}G(s) = \frac{1}{R + sL_s} \tag{C.3.0.8}$$

C.3.1 Simulation

Validation of the above analysis is performed through simulation of the reconstruction filter in LTspice. The simulation circuit is provided in Figure C.3. The shunt resistor is modelled according to the equivalent circuit shown in Figure C.1, with the parasitic inductance and capacitance parameterised by `Ls` and `Cp` respectively. Current excitation is provided by a current source. The reconstruction filter is modelled by a behavioural voltage source (to provide gain) plus an RC network to provide the first-order low pass response. The simulation model is parameterised using the two filter parameters, `Rf` and `Lf`, which correspond to R and L_s respectively in equation (C.3.0.8).

An AC small signal analysis is performed over the 50 kHz to 500 MHz frequency range. The upper frequency limit is chosen given this is the bandwidth limit of the oscilloscope used in this work. The frequency response of the system is analysed through the inspection of the resulting Bode plots.

C.3.1.1 Ideally tuned filter

We firstly analyse the response of the filter assuming that the filter time constant is perfectly matched to the L_s/R time constant of the shunt resistor. For this purpose we select the typical value of parasitic inductance from Table C.1 and set the parasitic capacitance to zero. The frequency response of the current shunt (scaled to 0 dB at DC) and the filtered output are presented in Figure C.4.

The effect of the series inductance on the current shunt frequency response is clearly evident in this plot, with a 20 dB gain at 100 MHz (shown in blue). A substantial phase shift is also observed for frequencies above 1 MHz, approaching 90° at 500 MHz. Note the corner frequency for the current sense resistor response occurs at approximately 6 MHz.

Conversely the filtered output (shown in green) provides the ideal response across the entire frequency range with 0 dB gain and 0° phase shift.

C.3.1.2 Sensitivity to changes in resistance

Given the shunt resistor will have some tolerance, it is of interest to investigate the effect of changes in resistance on the reconstruction filter performance. The shunt resistor used in this work has a specified tolerance of 0.1 % and a negligible temperature coefficient. Rather than modify the sense resistor value in the simulation circuit, the filter resistance parameter, `Rf`, is instead adjusted by ±0.1 % and the frequency response of the reconstruction filter is simulated for the nominal and extreme cases. The parasitic inductance is set to the typical value of

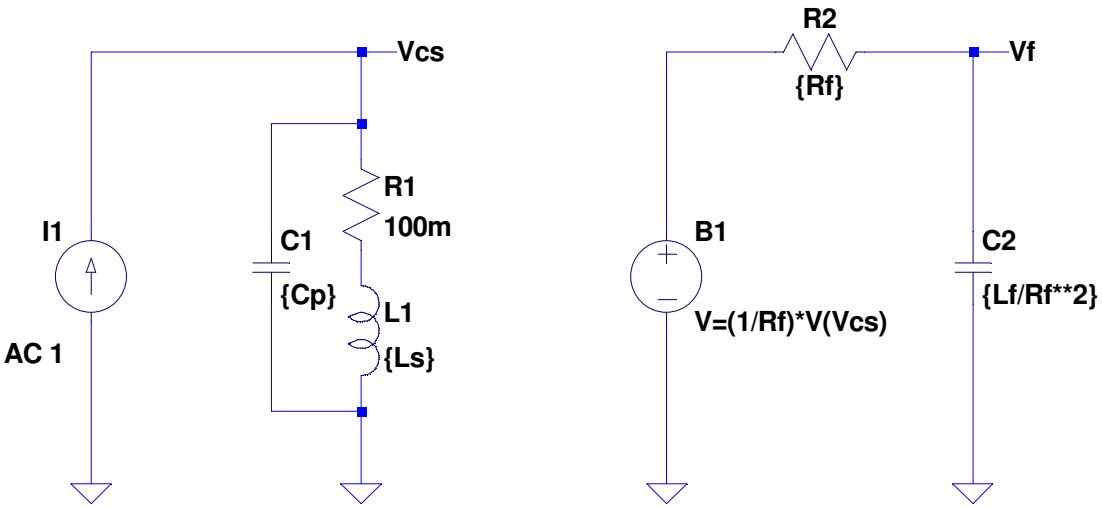


Figure C.3: LTspice schematic for simulation of the performance of the current reconstruction filter.

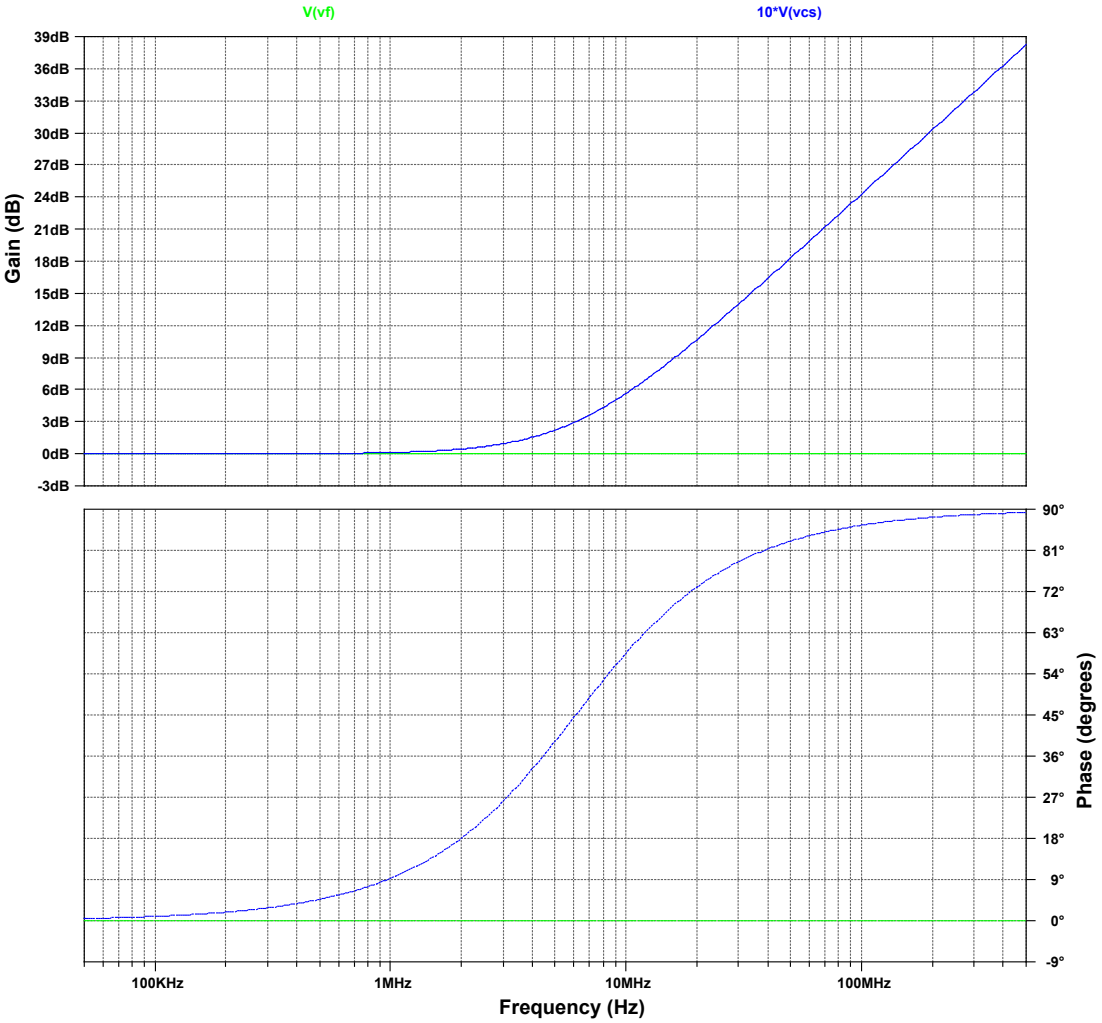


Figure C.4: Bode plot showing the shunt resistor frequency response (blue, scaled by a factor of 10 to 0 dB at DC) and the filter response (green).

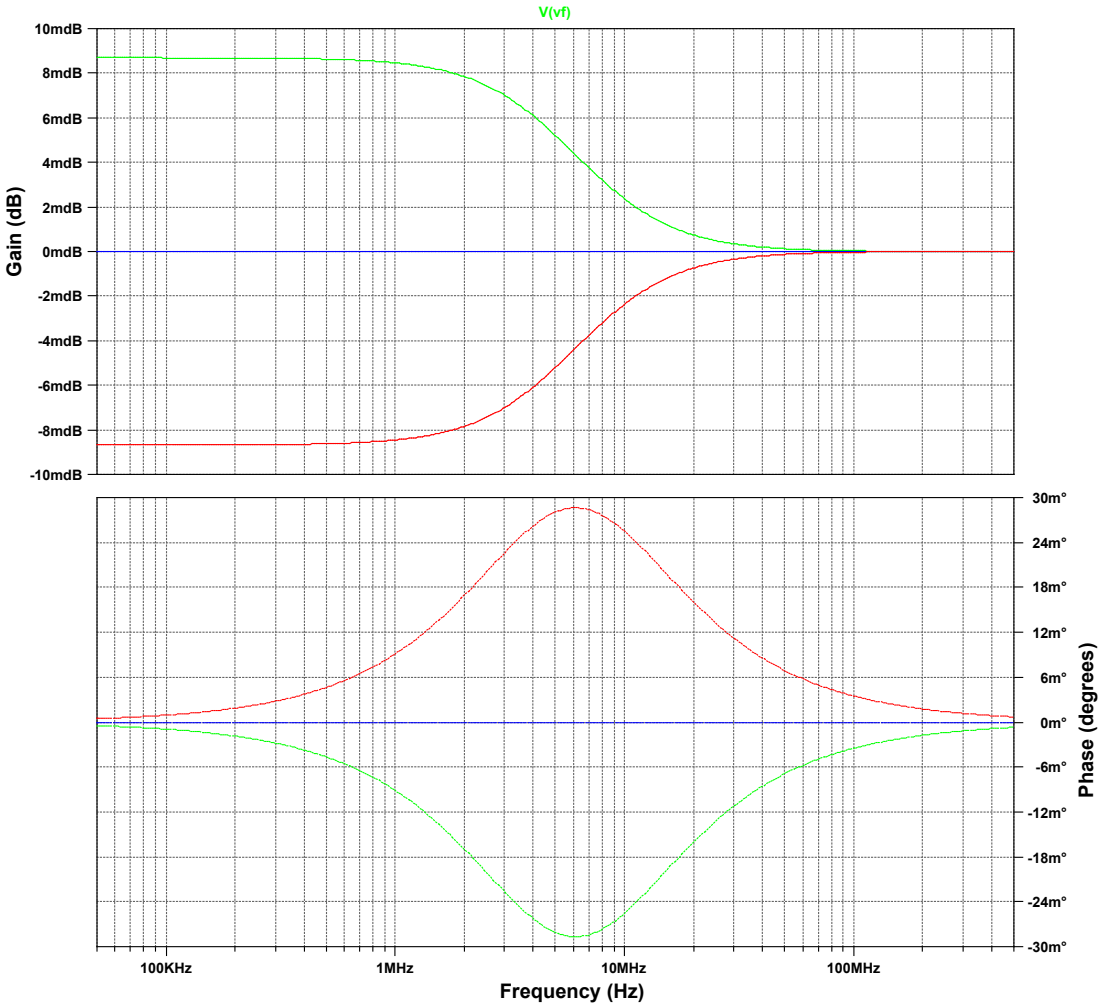


Figure C.5: Bode plot showing the effect of resistance changes on the reconstruction filter frequency response. Frequency response is plotted for `Rf` values of 100 mΩ (blue), 99.9 mΩ (green) and 100.1 mΩ (red).

2.6 nH and the filter is tuned for the nominal resistance. The simulated frequency response is presented in Figure C.5.

The frequency response shows that changes in the resistance have the greatest impact on the DC and low frequency response; for higher frequency the frequency dependant term dominates, and hence, the small resistance error has little impact. The maximum error is equal to the resistor tolerance, 0.1 %, at DC. The observed phase shift is less than 0.03° over the entire frequency range and is therefore also negligible.

C.3.1.3 Sensitivity to parasitic capacitance

Next, the effect of parasitic capacitance on the reconstruction filter is investigated. The frequency response of the reconstruction filter is simulated for the parasitic capacitance values identified in Table C.1. The parasitic inductance is set to the typical value of 2.6 nH and the filter is ideally tuned. The simulated frequency

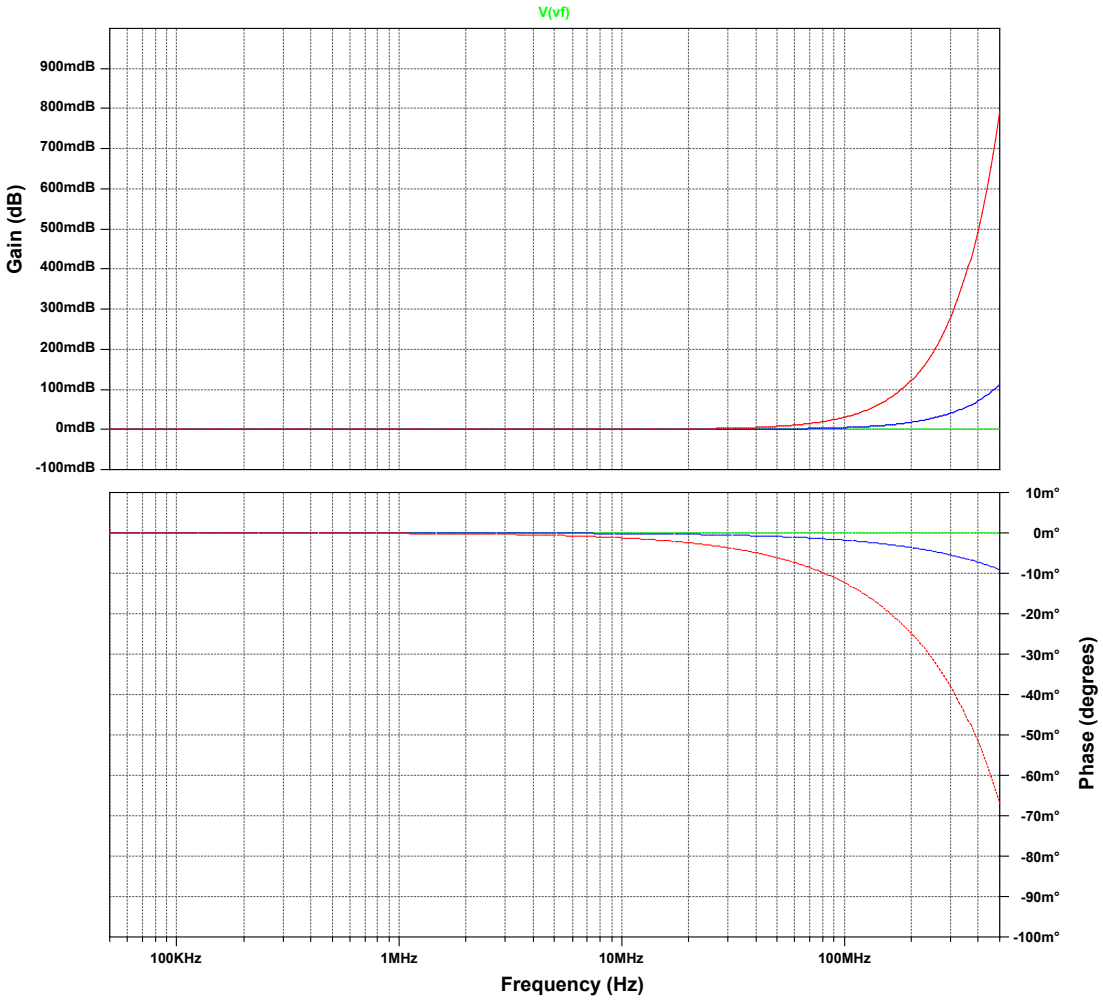


Figure C.6: Bode plot showing the effect of parasitic capacitance on the reconstruction filter frequency response. Frequency response is plotted for `Cp` values of 0 pF (green), 0.5 pF (blue) and 3.4 pF (red).

response is presented in Figure C.6.

It can be seen that the effect of parasitic capacitance on the filter performance can be completely neglected. Even at the maximum capacitance bound the magnitude deviation across the entire frequency range is less than 0.8 dB. Similarly the maximum observed phase shift was less than 0.1°.

C.3.1.4 Sensitivity to parasitic inductance

Finally, the effect of parasitic inductance on the reconstruction filter is investigated. Particularly of interest is the effect of mismatches between the physical current sense resistor series inductance, `Ls`, and the inductance value used for the reconstruction filter, `Lf`. The frequency response of the reconstruction filter is simulated for nominal `Ls` value of 2.6 nH identified in Table C.1. Mismatches in the inductance parameter for the reconstruction filter, `Lf`, of ±20 %, −50 % and +100 % are investigated. In each case the frequency response if simulated and

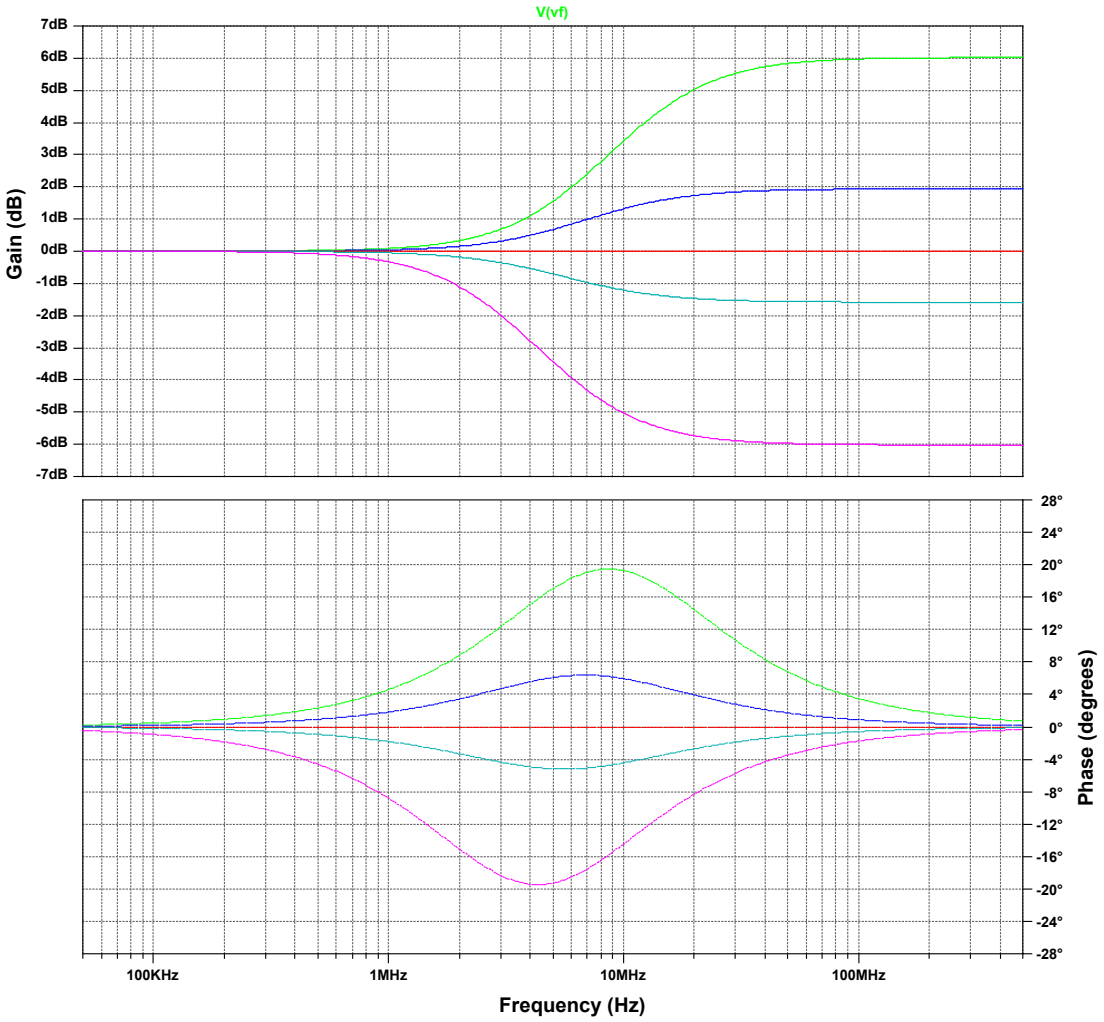


Figure C.7: Bode plot showing the effect of mismatched parasitic inductance values on the reconstruction filter frequency response. Frequency response is plotted for `Ls` = 2.6 nH and `Lf` values of 2.6 nH (nominal, red), 5.2 nH (200 %, magenta), 3.12 nH (120 %, cyan), 2.08 nH (80 %, blue) and 1.3 nH (50 %, green).

presented in Figure C.6.

It can be seen that the mismatches in the filter inductance parameter, `Lf`, have the greatest effect on the performance of the reconstruction filter. For a factor of two mismatch in the assumed series inductance value, a maximum error of 6 dB and phase shift of 20° are observed over the investigated frequency range. For errors in the inductance value of ±20 % the magnitude and phase error observed in the frequency response are within 2 dB and 7° respectively. Based on this result we can expect the maximum error resulting from a mismatch in the inductance value to be of the same order as the percentage error in the inductance value. Phase shift should be negligible for errors in inductance less than 20 %.

As the switching features of interest are usually extracted from the time-domain waveforms, we also analyse the effect of mismatched inductance on the response to a step change in current. A transient analysis has been performed for

a 1A current step with 10 ns rise time applied to the sense resistor model. The resulting time-domain response is presented in Figure C.8.

Firstly we note that a mismatch in the inductance value affects the observed di/dt and peak current; di/dt and peak current are overestimated for low values of `Lf` and underestimated for high values of `Lf`. In both cases, however, for all tested values the percentage error in these metrics was lower than percentage error in the inductance value. The other feature of note is that the response to a step change can be used to judge whether the filter is correctly tuned; for both over- and under-compensated cases an exponential rise/decay to the stepped current is observed while for the current tuning (red trace) the step response is perfectly reconstructed.

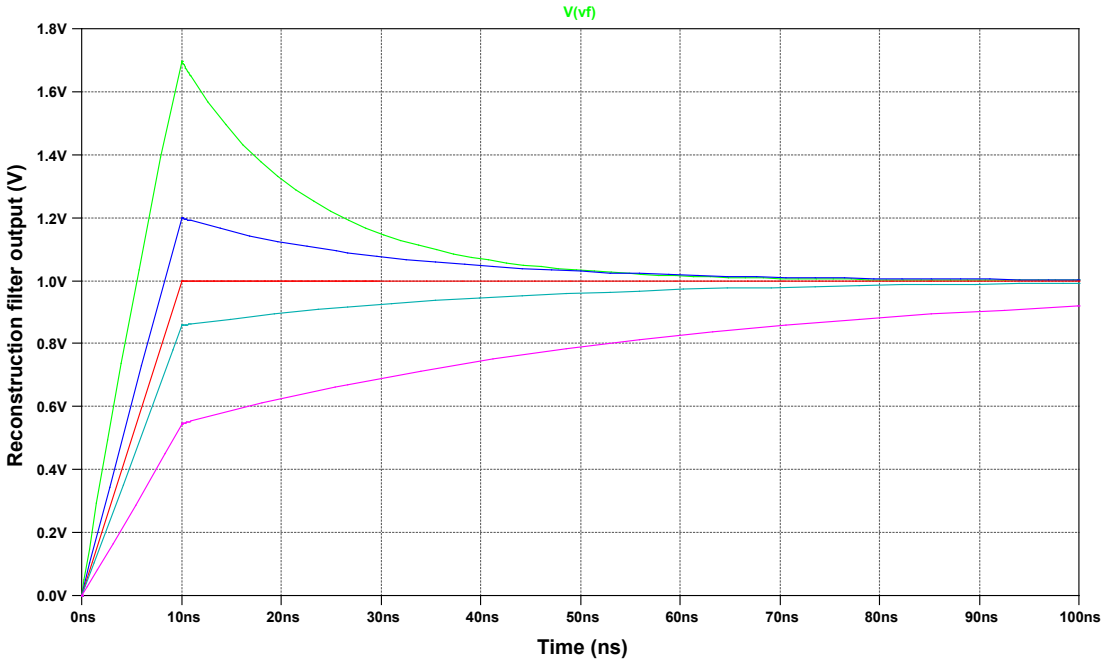


Figure C.8: Transient simulation showing the effect of mismatched parasitic inductance values on the reconstruction filter step response. Step response to a 1 A current change with 10 ns rise time is plotted for `Ls` = 2.6 nH and `Lf` values of 2.6 nH (nominal, red), 5.2 nH (200 %, magenta), 3.12 nH (120 %, cyan), 2.08 nH (80 %, blue) and 1.3 nH (50 %, green).

C.4 Tuning the reconstruction filter

Tuning of the reconstruction filter is challenging given the expected magnitude of the parasitic elements and the unknown parasitic impedances in the primary load current loop. Measurement of the parasitic inductance of the current sense resistor is impractical as this test would have to be performed *in situ* given the dependence of the parasitic inductance on the current loop geometries.

Instead we take the approach of tuning the current reconstruction filter during post-processing using the features of the capture double-pulse switching waveforms.

Firstly we define the goal of the tuning process as to set the time constant of the current reconstruction filter to be equal to the time constant of the filter. We note that the value of the sense resistance is known and of a high tolerance (0.1 %). Setting the time constant, therefore, requires setting the inductance term in reconstruction filter transfer function (C.3.0.8) to the true value of the series inductance in the sense resistor equivalent circuit (see Fig. C.1). For clarity we now denote L_f as the value of the inductance term in the reconstruction filter transfer function and L_s as the true value of the current sense resistor equivalent series inductance. The tuning process then becomes an exercise in setting $L_f = L_s$.

Secondly, we note that the excitation applied to the current sense resistor by the double-pulse waveform can be approximated by a step function at the switching edge. We therefore analyse the response of the current reconstruction filter to a step function in the case of mismatched time constants. From equations (C.3.0.5) and (C.3.0.8) we have:

$$I_{comp}(s) = \frac{1}{R + sL_f} \cdot (R + sL_s) \cdot I(s) \tag{C.4.0.1}$$

The step response to a step change in current from 0 to i_0 is then:

$$I_{step}(s) = \frac{i_0}{s} \cdot \frac{R + sL_s}{R + sL_f} \tag{C.4.0.2}$$

Taking the inverse Laplace transform of equation (C.4.0.2) yields the time-domain response of the reconstruction filter:

$$i_{step}(t) = i_0 \left[1 - \frac{L_f - L_s}{L_f} e^{\left(-\frac{R}{L_f}t\right)}\right] \tag{C.4.0.3}$$

For $L_f = L_s$ equation (C.4.0.3) decomposes to $i_{step}(t) = i_0$. Where $L_f \neq L_s$, however, the time-domain response of the filter either overshoots (for $L_f < L_s$) or undershoots (for $L_f > L_s$) before exponentially decaying back to i_0.

This behaviour can be exploited in order to determine the correct value for L_f by applying a series of reconstruction filters of different time constants to the experimental double-pulse waveform data and analysing the time-domain response. While it should be possible sweep L_f over any value range, choosing values of $L_f > L_s$ has the added benefit of attenuating high-frequency content in the experimental waveform data.

By sampling the time domain response at a fixed time delay for a range of values of $L_f > L_s$ and noting that for $L_f = L_s$ the observed reconstructed current should be equal to the expected load current. To achieve this, it is necessary to fit the sampled points to a model of the form of equation (C.4.0.3).

Equation (C.4.0.3) is inherently non-linear and can therefore not be rearranged to allow the use of linear regression. It is possible to make some approximations to simplify equation (C.4.0.3). For example, if we select a value of t for the sampling instant much smaller than the time constant $\tau = \frac{L_f}{R}$ then the exponential component of equation (C.4.0.3) approaches 1 resulting in:

$$i_{step}(t) \approx i_0 L_s \cdot \frac{1}{L_f}, \qquad t \ll \frac{L_f}{R} \tag{C.4.0.4}$$

In practice this approximation is difficult to implement, however, as the leading edge of the current rise in experimental waveform data is not a clean step, but is instead a fast ramp with overshoot. Choosing small values of t is therefore difficult. Equally, choosing large values of τ is not possible, as the overshoot component of the current waveform becomes smeared for small values of t, invalidating the assumption of a step function.

Given these limitations an alternative methodology is proposed. Firstly we rearrange Equation (C.4.0.3) as follows:

$$\frac{1 - \frac{i_{step}(t)}{i_0}}{e^{-\frac{R}{L_f}t}} = 1 - \frac{L_s}{L_f} \tag{C.4.0.5}$$

Equation (C.4.0.5) is still not in a form suitable to utilise linear regression in order to extract the value of L_s, due to the presences of the exponential term in the denominator of the left hand side of the equation. This term contains both the independent variable, L_f, as well as the unknown sampling time, t. The right hand side of the equation is in the form of a straight line with intercept fixed at 1 and the slope equal to the L_s, the quantity of interest.

Given the value for R_f is known at each sample point it should be possible to select a value t in order to transform the sampled data points such that they model a straight line to which linear regression can be applied. Based on equation (C.4.0.5) the sampled (L_f, i_{step}) data points can be transformed into the

regression variables (X, Y) as shown in equations (C.4.0.6) and (C.4.0.7).

$$X = \frac{1}{L_f} \tag{C.4.0.6}$$

$$Y = \frac{1 - \frac{i_{step}(t)}{i_0}}{e^{-\frac{R}{L_f}t}} - 1 \tag{C.4.0.7}$$

Note that the equation for Y has been adjusted such that the modelled line should have a Y-intercept of zero. Given this property, the value for t can be chosen to maximise the fit of the linear model to the regression variables. The R^2 value for the linear model is selected as the metric used to describe "goodness of fit" for each tested value of t. Note that the value for t is expected to be close to the sampling delay between the switching and sampling instants.

Having determined an appropriate value of t to compensate for the exponential term the values for the regression values, X and Y can be calculated and linear regression used to determine a value for the slope, m of the fitted line. Note that we force the model through to have a Y-intercept of zero. The value for L_s can then be extracted from the slope using:

$$L_s = -m \tag{C.4.0.8}$$

The methodology proposed above has been implemented in MATLAB as described in Section C.5. The process described above can be used to extract a value of L_s based on each experimental waveform. The value for L_s is expected to be the same across all tests, however, given a consistent experimental fixture. Therefore it is proposed to take the mean of the extracted values of L_s across multiple experimental tests.

C.4.1 Tuning results

The methodology presented above in Section C.4 was implemented in MATLAB as outlined in Section C.5. Experimental double-pulse switching waveforms were then post-processed using this MATLAB script in order to extract a value for L_s. Waveforms from across the entire investigated parameter space were processed. Only switching waveforms for load currents of approximately 10 A were included to maximise the excitation and minimise the changes to timing due to varying load current. Consequently 35 switching waveforms were selected for processing.

A value of L_s was extracted from each processed waveform, along with the tuned value for t in each case and the R^2 describing the quality of fit of the proposed model.

From the 35 samples a mean value for L_s of 6.5 nH was calculated with a standard deviation of 0.28 nH. Across all samples the minimum R^2 value calculated was 0.999995. The mean tuned value for t across the dataset was 97.5 ns with a standard deviation of 7.6 ns.

An example application of the reconstruction filter to experimental data is presented in Figure C.9. Without compensation the current as measured across the current sense resistor overestimates the true current by a factor of more than five. Additionally high-frequency content in the current swamp the low-frequency information of interest. The reconstruction filter is able to reveal the true current from what appears, on inspection, to be a very noisy measurement, highly polluted by $\mathrm{d}i/\mathrm{dt}$ content.

Figure C.10 shows the reconstructed drain current in the context of the drain-source voltage transition and expected inductor current, I_L. The reconstructed current appears reasonable in this context; the current ramps up to the load current and once the load current is fully supported by the switching device, the drain-source voltage transition occurs. A drain current overshoot of ap-

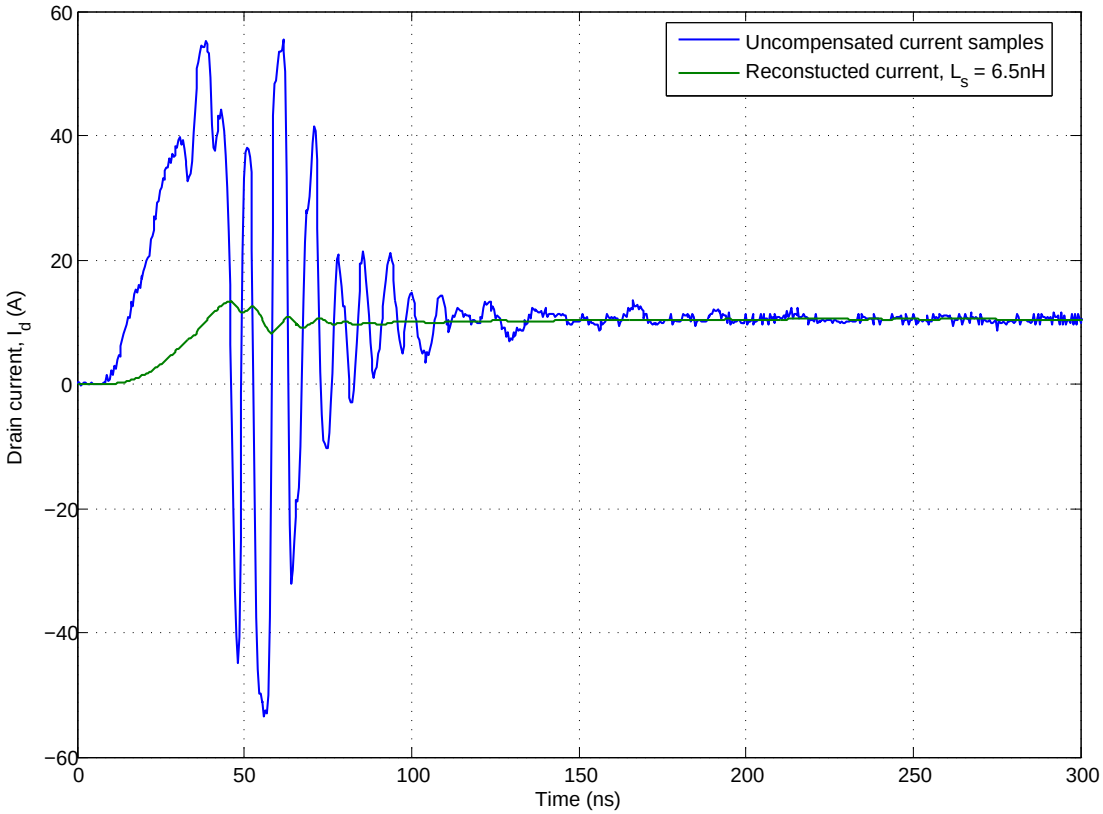


Figure C.9: Example application of the reconstruction filter to experimental data. Shown is the turn-on drain current transient for $R_{gle} = 100\,\Omega$, $C_{gshe} = 40$ nF and $I_L = 10$ A. The blue trace shows the drain current as measured across the current sense resistor without any compensation for the series inductance. The green trace shows the resulting current after application of the reconstruction filter tuned for $L_s = 6.5$ nH.

proximately 3 A is observed during the voltage transition due to the capacitive charge/discharge of parasitic capacitances in the circuit. A high-frequency ring is observed in the current following the switching transition, centred around the estimated inductor current as expected.

Finally, to assess the performance of the filter tuning process, Figure C.11 presents the reconstructed current for filter designs using three different values of L_s: the nominal extracted value of 6.5 nH and ±20 % of the nominal value, 5.2 nH and 7.8 nH respectively. The response in the case of $L_s = 7.8$ nH indicates overcompensation, evidenced by the initial undershoot of the expected inductor current and subsequent exponential rise towards the expected current. Conversely the response in the case of $L_s = 5.2$ nH appears under-compensated, evidenced by an initial overshoot and then subsequent exponential decay towards the expected inductor current. Note also in this case the lower attenuation of the high-frequency ring on the trailing edge. The nominal case of $L_s = 5.2$ nH appears reasonable, with no apparent overshoot or undershoot of the expected load current following the switching transition, and the trailing high-frequency ring centred around the expected inductor current.

These results agree with the predicted performance of the reconstruction filter subjected to a step change in current, based on the analysis of the transfer function and time-domain response presented in equation (C.4.0.3). The extracted value of 6.5 nH appears to provide a reasonable result, ±20 % variations in this value appear to provide an over- and under-compensated response respectively, providing confidence that the selected value of $L_s = 6.5$ nH is reasonable, and well within the error range of ±20 %.

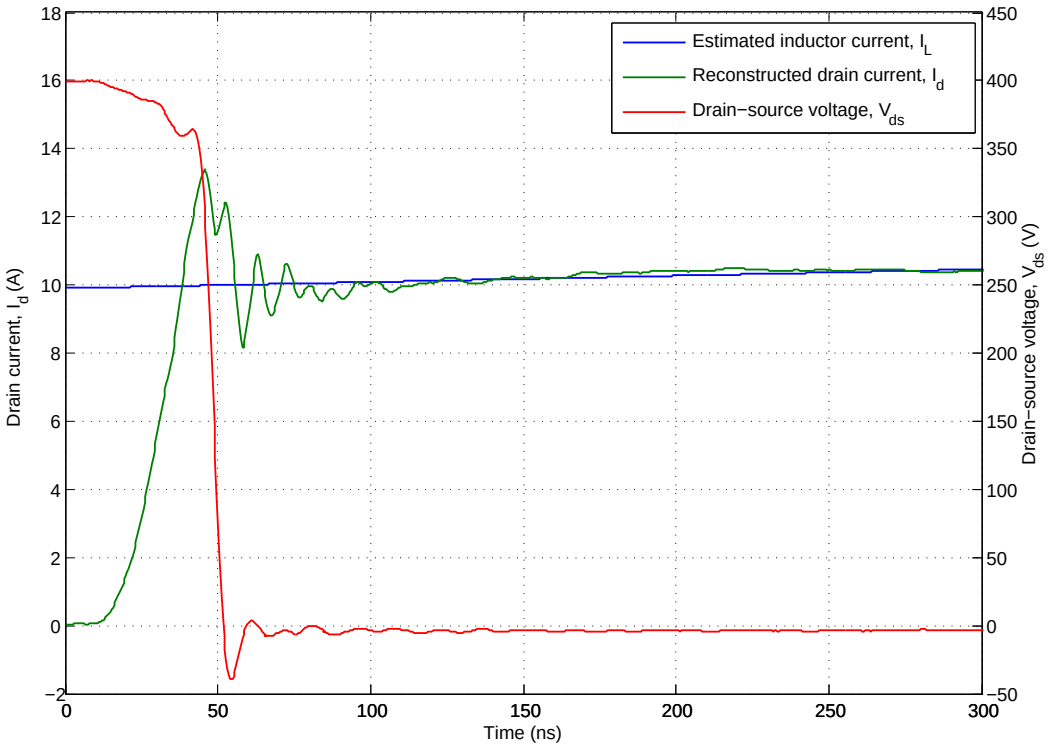


Figure C.10: Example application of the reconstruction filter to experimental data with $L_s = 6.5\,\text{nH}$. Shown is the reconstructed turn-on drain current (green) and drain-source voltage (red) transients for $R_{gle} = 100\,\Omega$, $C_{gshe} = 40\,\text{nF}$ and $I_L = 10\,\text{A}$. The blue trace shows the estimated inductor current, I_L during the switching transition.

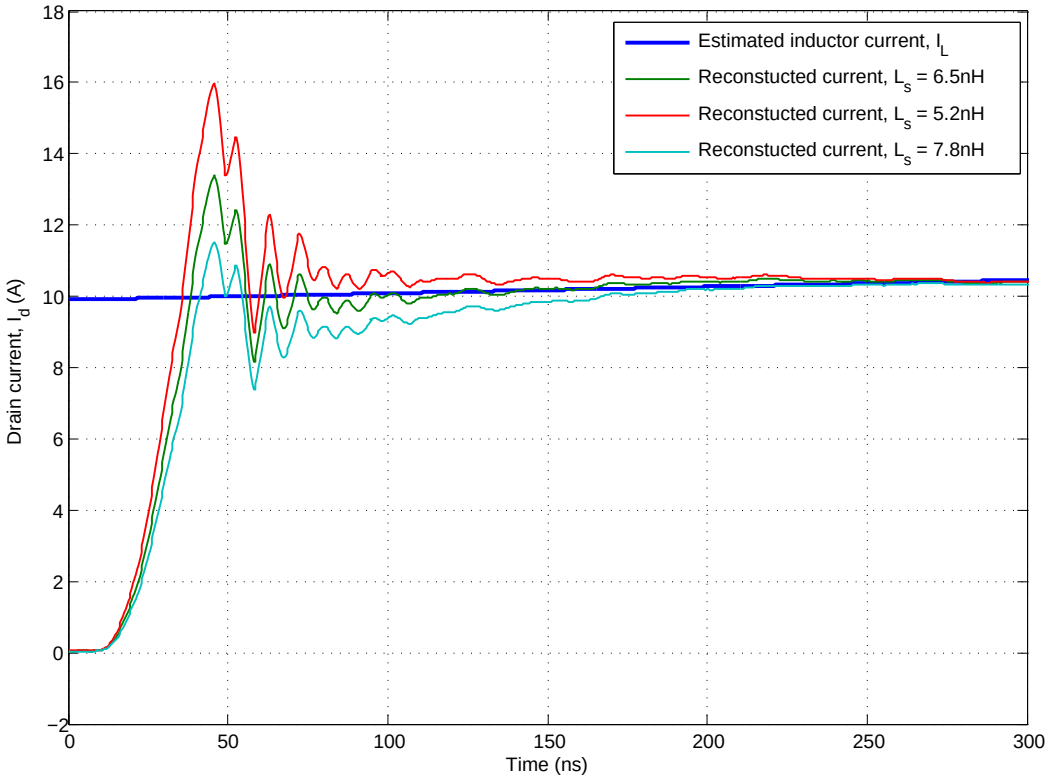


Figure C.11: Response of the reconstruction filter applied to experimental data for different values of L_s.

C.5 Post-processing implementation

C.5.1 MATLAB Script: `extractLs.m`

`extractLs.m` provides a MATLAB implementation for extracting a value for L_s, the effective parasitic inductance of a resistive current shunt, from experimental double-pulse waveform data. The extracted value of L_s can be used to tune the reconstruction filter described previously in this appendix. Parameters and return values for this implementation are outlined below and the function listing is provided in Figure C.12.

Parameters:

`filename` Filename prefix of waveform set to process. `extractLs` expects two waveforms (CH1–CH2) with the `*.isf` extension and format. Example: passing a filename value of `'waveform'` would attempt to open and process the waveform files `waveformCH1.isf` and `waveformCH2.isf`.

Returns:

`features` MATLAB structure containing the extracted value for L_s plus other features extracted during the estimation process.

Figure C.12: MATLAB function for extracting a value for L_s from experimental double-pulse waveform data.

```
function out = extractLs(filename)

fileCH1 = sprintf('%sCH1.isf', filename);
fileCH2 = sprintf('%sCH2.isf', filename);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% INITIALISATION
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
warning('off','all');

Ts = 0.4e-9;    % sample time

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 1) IMPORT WAVEFORMS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
isf = isfread(fileCH1);    % Vds trace
t = isf.x;      % time
Vds = isf.y;    % Vds

isf = isfread(fileCH2);    % Id trace (V across shunt resistor)
iraw = isf.y;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 2) REMOVE ZERO OFFSETS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
leadtime = 1e4;                 % leading edge of zero V, A (samples)

```

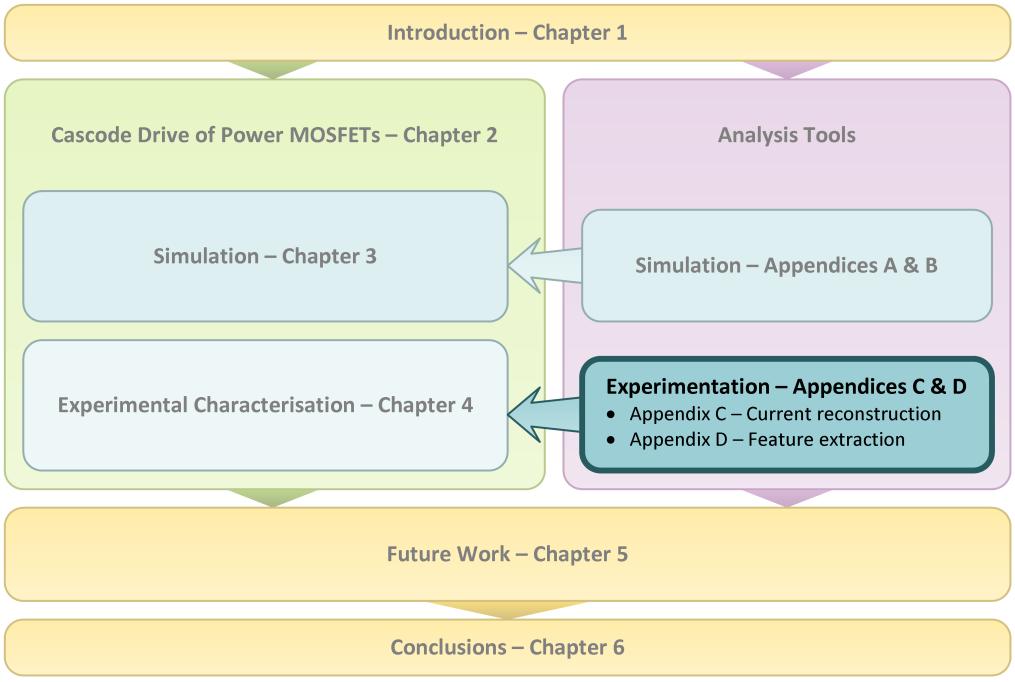
```
% calculate offsets
ioffset = mean(iraw(1:leadtime));

% remove offsets
iraw = iraw - ioffset;
t = t - t(1);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 3) RECONSTRUCT TRUE CURRENT (ASSUME 6.5nH)
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Filter parameters
R = 0.1;        % sense resistance
L = 6.5e-9;     % inductance compensation

% Build filter
G = tf([1], [L R]); % Filter transfer fuction

% Filter current
Vr = R*iraw;        % Voltage across sense resistor
Id = lsim(G,Vr,t);   % Filter current

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 4) FEATURE EXTRACTION
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
leadtime = 4e-6;                    % Clean leading edge of test

%%% EXTRACT BUS VOLTAGE FROM CLEAN LEADING EDGE
Vbus = mean(Vds(1:leadtime/Ts));    % bus voltage

%%% FIND SWITCHING EDGES
trigger = 1;
while (Vds(trigger) > Vbus/2)
    trigger = trigger + 1;          % find first voltage fall
end;
turnOn_1st = trigger;
trigger = trigger + 100e-9/Ts;      % 100ns holdoff
while (Vds(trigger) < Vbus/2)
    trigger = trigger + 1;          % find first voltage rise
end;
turnOff_1st = trigger;
trigger = trigger + 100e-9/Ts;      % 100ns holdoff
while (Vds(trigger) > Vbus/2)
    trigger = trigger + 1;          % find first voltage fall
end;
turnOn_2nd = trigger;

%%% DEFINE WINDOW FOR CURRENT RAMP
rampWindow = (turnOn_1st+400e-9/Ts):(turnOff_1st-100e-9/Ts);
currentRamp = Id(rampWindow);

%%% FIT POLYNOMIAL TO CURRENT RAMP
fo = fit(t(rampWindow),currentRamp,'poly4');
P = coeffvalues(fo);
currentFit = polyval(P,t-((turnOn_2nd-turnOff_1st)*Ts));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 5) Ls ESTIMATION
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Filter parameter sweep to perform (overcompensated)
```

```
87  Lf = logspace(log10(10e-9),log10(20e-9),20);
88  numsamples = length(Lf);
89
90  % Extract current samples from filtered versions
91  Isamples = zeros(numsamples,1);
92
93  for i = 1:length(Lf)
94      G = tf([1], [Lf(i) R]);
95      Idcomp = lsim(G,Vr,t);
96      Isamples(i) = Idcomp(turnOn_2nd+150);
97  end;
98
99  % Find load current for step compensation
100 I0 = currentFit(turnOn_2nd+150);
101
102 % Tune "t" to maximise Rsq value (for best fit)
103 X = 1./Lf'; % regression vector
104
105 Rsq = 0;    % initialise to zero for seek
106 tstep = 0;
107
108 % precalculate first itteration
109 newRsq = corr(X,calcY(Isamples,Lf',I0,tstep+1e-9))^2;
110
111 while (newRsq > Rsq)
112     tstep = tstep + 1e-9;
113     Rsq = newRsq;
114     newRsq = corr(X,calcY(Isamples,Lf',I0,tstep+1e-9))^2;
115 end
116
117 % Calculate tuned regression vector
118 Y = calcCompY(Isamples,Lf',I0,tstep);
119
120 % Calculate Ls value from slope
121 m = X\Y;
122 Ls = -m;
123
124 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
125 % 7) RETURN
126 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
127 out = struct;
128
129 out.Ls = Ls;
130 out.Rsq = Rsq;
131 out.t = tstep;
132 out.I0 = I0;
133
134 % LOCAL FUNCTION
135 % Calculation of regression variable "Y"
136 function Y = calcCompY(i, Lf, I0, t)
137     Y = ((1-(i/I0))./exp(-R*t./Lf))-1;
138 end
```

Appendix D

Feature extraction of switching performance metrics from double-pulse waveform data

A system for automated post-processing of experimental double-pulse waveform data to extract switching performance metrics is developed and presented in this appendix. The methodology and feature extraction techniques developed and applied in this work are described. Finally, A MATLAB implementation of the post-processing techniques is provided.



D.1 Introduction

Rigorous experimental characterisation of the effect of gate drive parameters on switching performance requires the exploration of multi-dimensional parameter spaces. When more than one degree of freedom is investigated, the size of the collected dataset rapidly increases with the sample number of any of the independent variables. Manual extraction of switching performance metrics from waveform data, for multi-dimensional parameter spaces, quickly becomes impractical. Instead, a methodology is proposed in this chapter for the automated post processing of double-pulse waveform data to extract the switching performance metrics of interest.

D.2 Feature extraction methodology

D.2.1 Offset removal

Where active probes, such as high-voltage differential probes, are used to record the waveform data, DC offsets may be present in the recorded waveforms due to drift over time and temperature. Fortunately, the double pulse waveform provides opportunities to detect and remove any DC offsets. For both the drain-current and gate-source voltage traces the expected current and voltage respectively are zero before the first pulse. Any offsets can, therefore, be calculated by taking the mean value of the waveform samples over an interval within the clean leading edge of the captured waveform data. The averaging window can be selected to be a fixed length, as long as the window length never exceeds the length of the clean leading edge of the waveform, or the window time can be adaptively controlled based on extracted timing data (see Section D.2.7). The calculated mean value can then be subtracted from the entire waveform to remove any offset.

Note that this process is not suitable for removing any offset in the drain-source voltage trace, as the drain-source voltage transitions between the bus voltage and the on-voltage of the switch under test, which is *non-zero*. As a passive voltage probe was used to capture the gate-source voltage waveform, this was not an issue as no offset was present. Similarly de-skew in time may be required between oscilloscope channels where different types of probe are used due to different propagation delays. In this work probes were de-skewed using oscilloscope settings, so channel-channel skew was not present in the data. If this feature were not available, an appropriate offset would need to be added to the sample times of the relevant channels to bring them into time-alignment.

A MATLAB implementation is shown in Figure D.15, lines 36–48.

D.2.2 Extraction of bus voltage, V_{bus}

Extraction of the bus voltage can be achieved via the same process as described in Section D.2.1 by taking the mean of the drain-source voltage trace over a window within the clean leading edge of the waveform. Implementation of bus voltage extraction in MATLAB is shown in Figure D.15, lines 90–93. A visualisation of the bus voltage extraction process is also provided in Figure D.1.

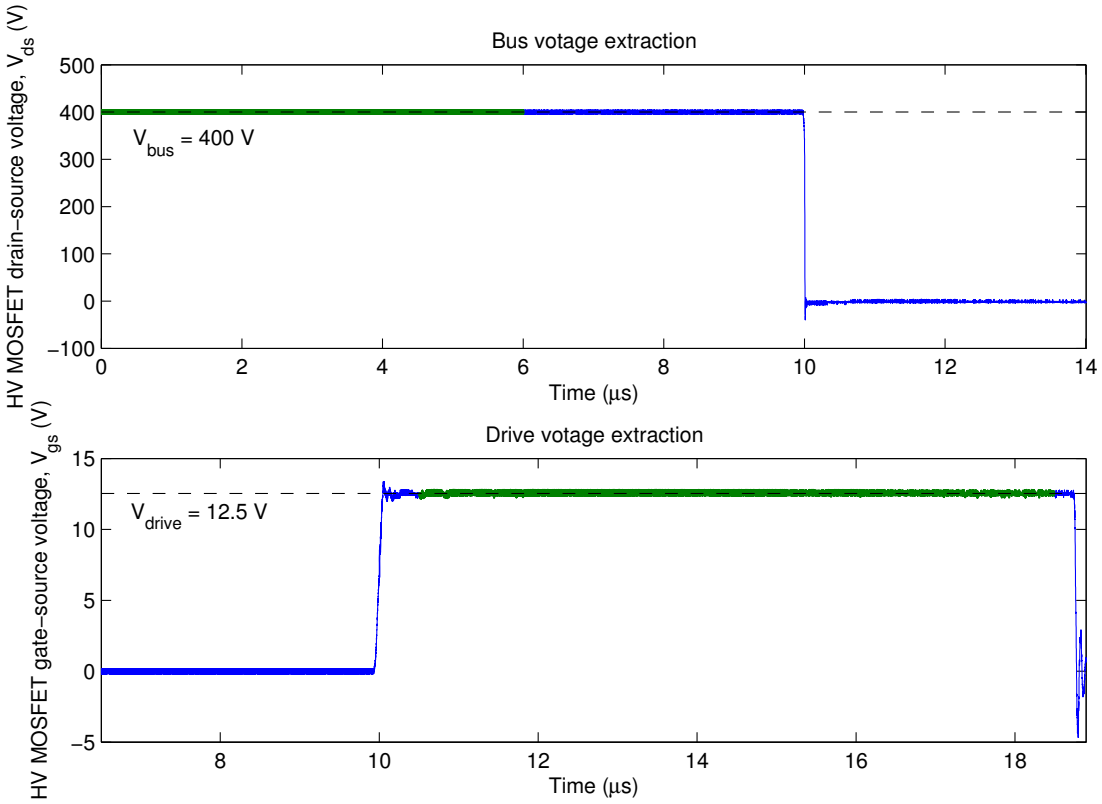


Figure D.1: Visualisation of the bus voltage and gate drive voltage feature extraction. The blue traces show the raw waveforms. The overlaid green portions of the waveform show the portion of the original waveform from which the average voltage values have been extracted. Both plots are annotated with the calculated average voltage level.

D.2.3 Pulse timing extraction

Many of the extraction techniques described in the subsequent sections require information to locate the appropriate section of the captured waveform. The drain-source voltage waveform is the most appropriate source for determining the pulse timing, due to the large signal levels (0–40 V for a nominal 400 V bus using a 10× voltage probe) and high transition rates (typically in excess of 40 V/ns), leading to clean switching edges.

The proposed methodology selects an arbitrary drain-source voltage level, V_{trig}, to define a voltage transition, and hence, edge of a pulse. Half of the extracted bus voltage, $V_{trig} = V_{bus}/2$, is selected as a reasonable value to avoid any false triggering due to ringing at the leading or trailing edge of the transition.

The leading edge of the first pulse is detected by finding the first fall in the bus voltage below V_{trig} (see Fig. D.2). A hold-off period of 100 ns is then implemented by advancing the waveform pointer by 250 samples to avoid re-triggering. The trailing edge of the first pulse is then detected by finding the next rise in drain-source voltage above V_{trig}. A hold-off interval is again implemented to avoid re-triggering. This process is repeated to find the leading and trailing edges of the second pulse. Detecting these four time instants fully maps the double-pulse timing from the waveform data.

Implementation of double-pulse timing detection in MATLAB is shown in Figure D.15, lines 95–115.

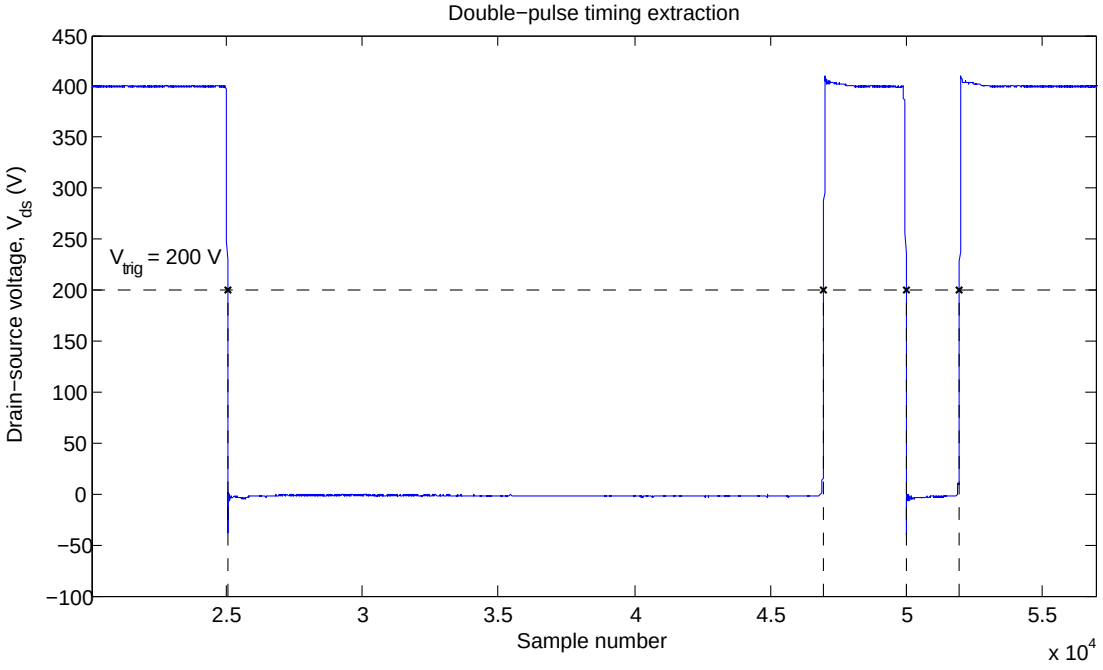


Figure D.2: Visualisation of the double-pulse timing extraction from the drain-source voltage waveform. Shown is the trigger voltage level, V_{trig}, and the extracted pulse edges based on this threshold.

D.2.4 Current reconstruction

As discussed in Appendix C, it is necessary to post-process the measured voltage across the current sense resistor in order to reconstruct the true current. This process involves the design and application of a first-order low pass filter to the captured waveform data. The underlying theory and filter design process are presented in Appendix C. Implementation of the current reconstruction process as a component of the feature extraction process is shown in Figure D.15, lines 50–63. An example visualisation of the current reconstruction process is additionally provided in Figure D.3.

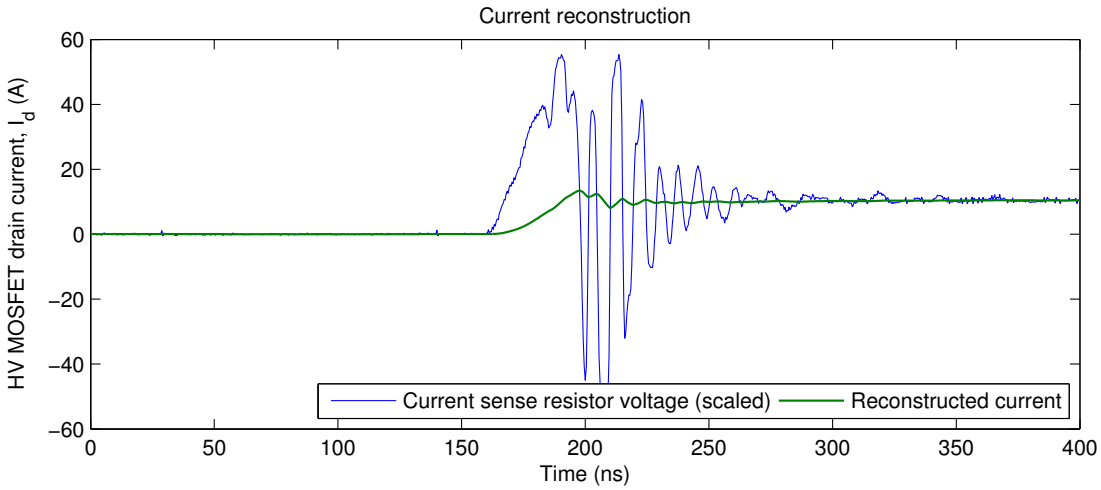


Figure D.3: Visualisation of the current reconstruction results. The blue traces shows the current as measured across the current sense resistor, without any post-processing. The overlaid green trace shows the reconstructed current waveform after application of the reconstruction filter.

D.2.5 Extraction of test (load) current, I_L

The test (load) current is determined by the length of the first pulse, during which current ramps up though the inductor. We assume that during the off period between pulse one and two that and decay in the inductor current is negligible; a reasonable assumption given that the forward voltage of the clamping diode is small compared to the bus voltage and the off period is short.

If only the drain-current of the switching device under test is instrumented, we only have information about the inductor current while the device is on, and hence not during the off period. We also can not rely on the measured drain current being representative of the inductor current during the switching transient.

Given these issues we select the interval defined by the first pulse as the portion of the waveform from which to extract the test current; the inductor current at the end of this interval should be approximately equal to the test current. We

note, however, that the inductor current begins to commutate from the device under test to the clamping diode before the end of the pulse, that is, before the drain-source voltage transitions. We therefore cannot interpolate the test current value from the drain-current trace.

Instead, we propose fitting a line to the current ramp curve of the load inductor and extrapolating to the end of the pulse, defined by the time instant at which the drain-source voltage falls as described in Section D.2.3. For an ideal inductor a linear fit should be suitable, however, where the series resistance is not negligible and/or saturation effects are present, a higher-order polynomial fit may be more appropriate.

For the experimental data collected in this work a 4^{th} order polynomial was selected. For test currents $\leq 2\,\text{A}$, a lower order polynomial was required to achieve a good fit, due to the shorter length of the current ramp; a 2^{nd} order polynomial was therefore selected for low test currents. A line is fitted to the drain current data samples over the interval defined by the first pulse. The fitted polynomial equation is evaluated at the time instant corresponding to the falling edge of the first pulse to extract the test current. This process is shown in Figure D.4. The MATLAB implementation for this process is provided in Figure D.15, lines 117–133.

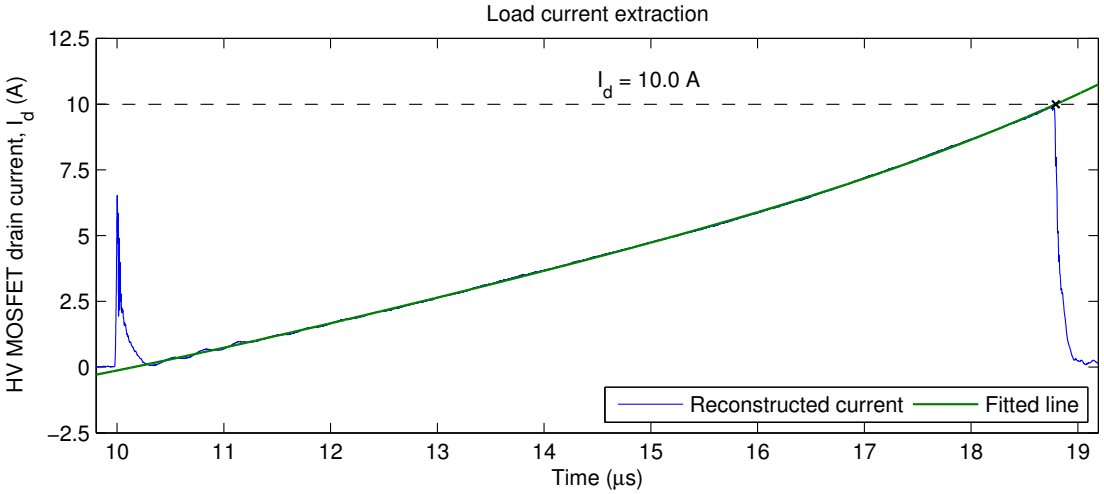


Figure D.4: Visualisation of the test (load) current feature extraction process. The blue trace shows the reconstructed current waveform. The green trace shows the 4^{th} order polynomial function fitted to the inductor current ramp. The annotated "X" shows the point at which the fitted polynomial is evaluated to determine the test (load) current. The extracted load current value and level are also shown.

D.2.6 Extraction of maximum dv/dt and di/dt

Sampled waveforms captured from an oscilloscope are not typically suitable for directly calculating approximate derivatives due to the presence of high-frequency random noise, or depending on the oscilloscope, the discretisation of the samples over the vertical scale. A more appropriate method for extraction of the time-derivative of the captured waveforms is through the application of a smoothing filter.

The use of a Savitzky-Golay filter is recommended for this task [67]. The Savitzky-Golay filter is a digital filter that uses a process of convolution to fit a low-order polynomial to successive adjacent windows of the waveform by least squares. Through a suitable selection of the filter window length and order, good smoothing can be achieved while maintaining the characteristic shape and high-frequency content of the waveforms. An example application of this process is shown in Figure D.5.

Importantly, as a polynomial is fitted locally to each data point, the local first derivative (and higher order derivatives if desired) can be trivially calculated from the polynomial equation. A good choice of filter order and window length can usually be achieved by inspection, by plotting the smoothed waveform on top

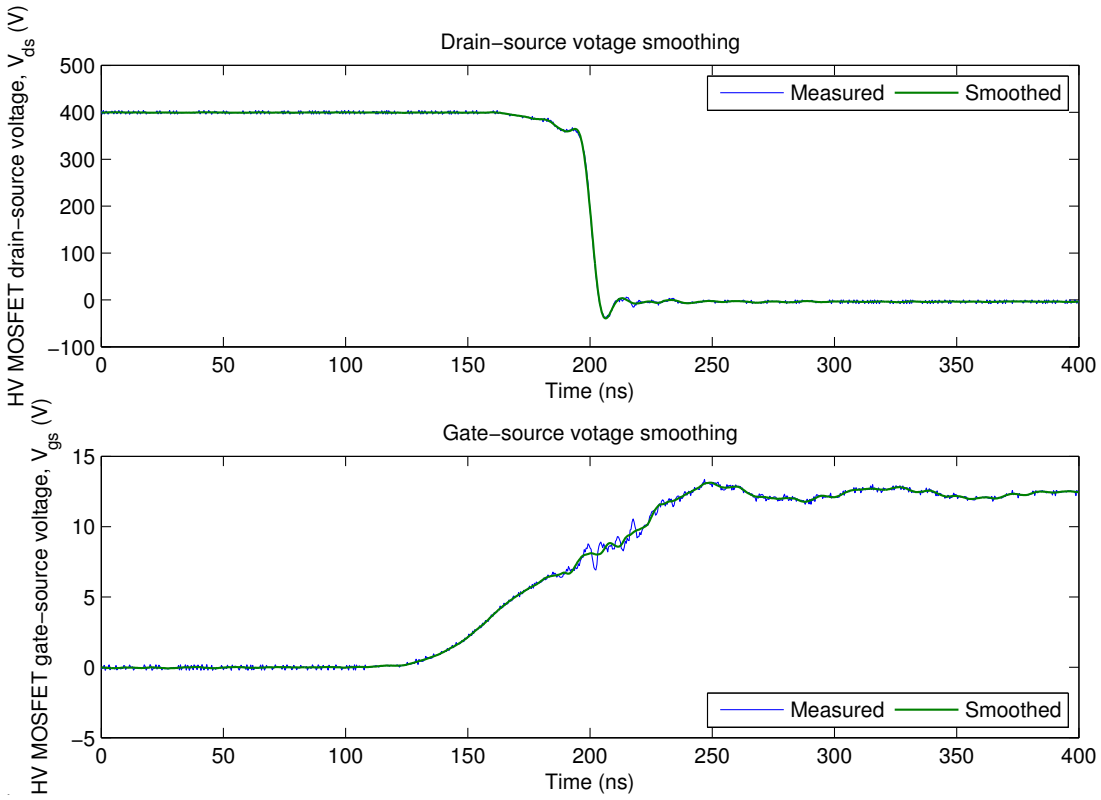


Figure D.5: Smoothing of the drain-source and gate-source voltage waveforms using the selected Savitzky-Golay filter. The blue traces show the original waveforms. The overlaid green traces show the smoothed versions of the waveforms.

of the raw data. For the experimental data used in this work a 9^{th} order filter with window length of 71 points (corresponding to a window length of 28.4 ns) is selected to smooth and perform differentiation of the voltage traces.

In the case of the drain current, smoothing will not be necessary if the current reconstruction method presented in Appendix C has been used, as the low-pass filter process will deal with the issues highlighted above. There is, however, likely to be high-frequency ringing present in the observed current. In terms of the switching performance metrics this component of the current may not be of interest as it does not describe the shape of the current rise, but rather, is due to ringing of parasitic elements in the circuit.

A low-order Savitzky-Golay filter is proposed to reject the high-frequency ringing present in the current waveform but maintain the characteristic shape of the current transient (see Fig. D.6). Additionally the application of the Savitzky-Golay filter allows the $\mathrm{d}v/\mathrm{dt}$ to be calculated at each sample point. Implementation of waveform smoothing and derivative calculation via application of a Savitzky-Golay filter in MATLAB is shown in Figure D.15, lines 65–85.

Finally, maximum $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}i/\mathrm{dt}$ can be extracted by taking the maximum of the smoothed drain-source voltage and drain current first derivatives respectively over the region of interest. For a double-pulse test the region of interest for turn-on is centred around the leading edge of the second pulse as extracted in Section D.2.3. Note that the $\mathrm{d}v/\mathrm{dt}$ will be negative for a turn on transient (fall in voltage) in which case the *minimum* value should be taken. Alternatively, turn-off metrics can be capitulated from the trailing edge of the first pulse. Implementation of the maximum $\mathrm{d}v/\mathrm{dt}$ and $\mathrm{d}v/\mathrm{dt}$ extraction process in MATLAB is provided in Figure D.15, lines 139–160, and a visualisation of the process is shown in Figure D.7.

D.2.7 Extraction of rise, fall and switching times

The 10–90 % rise and fall times from drain current and drain-source voltage respectively can be calculated based on the extracted values for V_{bus} and I_L. Firstly the 10 % and 90 % thresholds for current and voltage are calculated. The interval of interest from the waveforms is then isolated, specifically the rising edge of the second pulse for turn-on. The selected waveform interval is then searched for the first current sample above the 10 % and 90 % thresholds and the first voltage samples below the 90 % and 10 % thresholds. The rise/fall times are subsequently calculated from the time difference between the identified samples (see Fig. D.15, lines 162–205). Total switching time can be calculated as the time interval between the 10 % rise in drain current to the 10 % fall in drain-source voltage. A

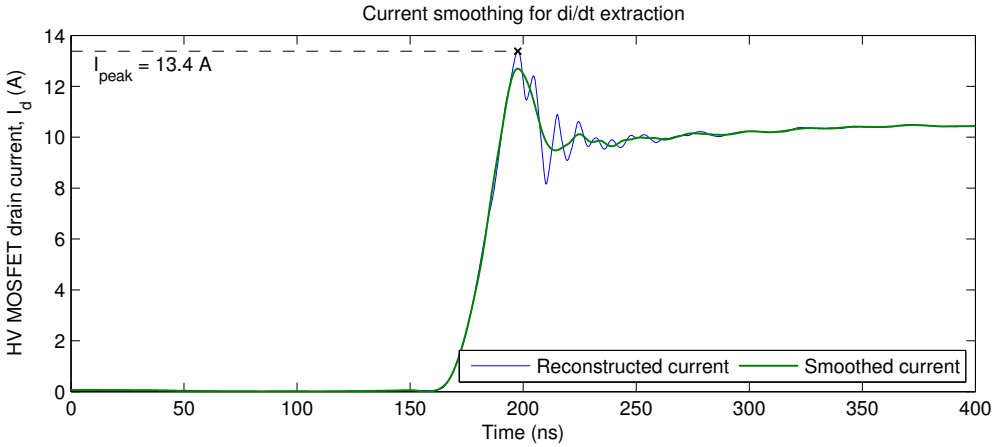


Figure D.6: Smoothing of the drain current waveform using a low-order Savitzky-Golay filter. The blue trace shows the reconstructed current waveform. The overlaid green trace shows the smoothed version of the reconstructed current waveform.

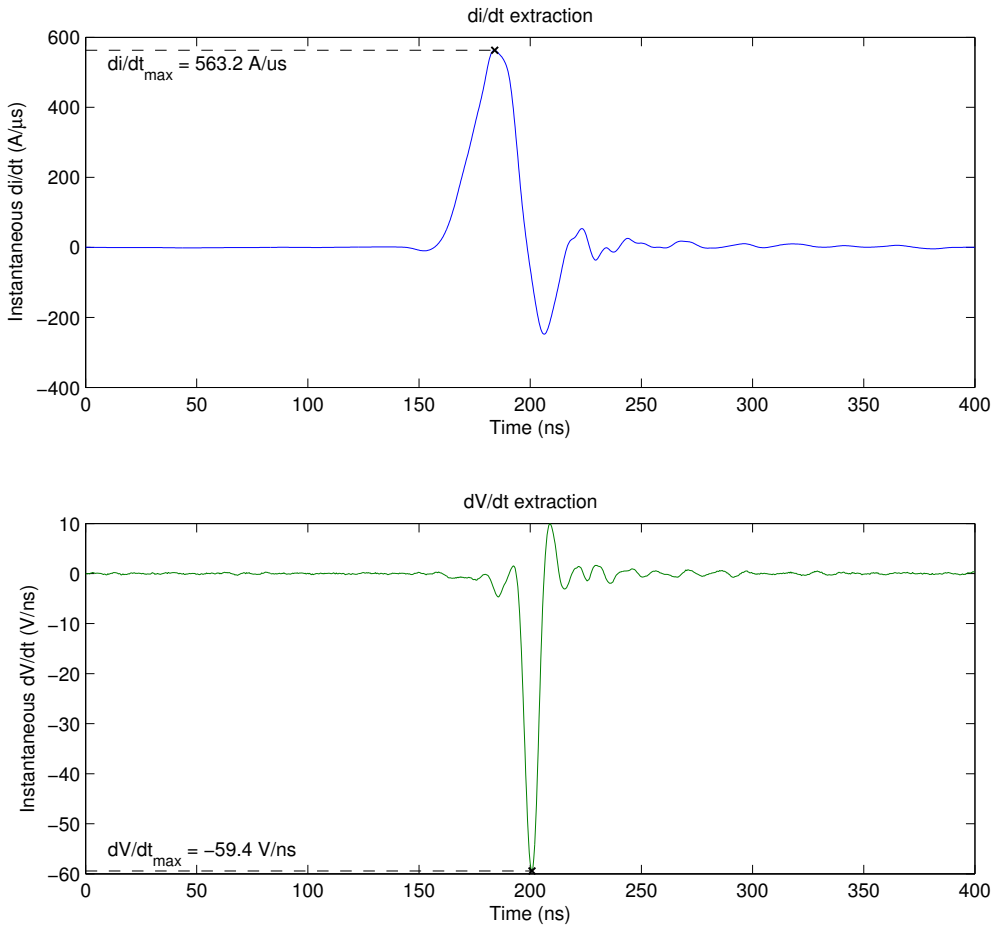


Figure D.7: Visualisation of the extraction of the maximum dv/dt (top) and dv/dt metrics (bottom). The traces show the instantaneous first derivative of the smoothed reconstructed drain current and smoothed drain-source voltage waveforms, respectively, as calculated from application of the Savitzky-Golay filters. The plots are annotated with the extracted values for the maxima.

visualisation of the timing feature extraction is provided in Figure D.8. A similar process can be use to extract the turn-off timing information (see Fig. D.15, lines 223–299).

This method limits the timing resolution to that of the sample time; if more resolution is desired interpolation of the waveforms would be required. Another alternative is to use the smoothed waveform data rather than the raw sampled data. This approach is taken in this work. The smoothed data not only avoids false triggering due to any high-frequency content in the data, but would also better facilitate interpolation if higher timing resolution was required. Note also that the rise time metric does not capture information regarding any overshoot of the drain current above the load current.

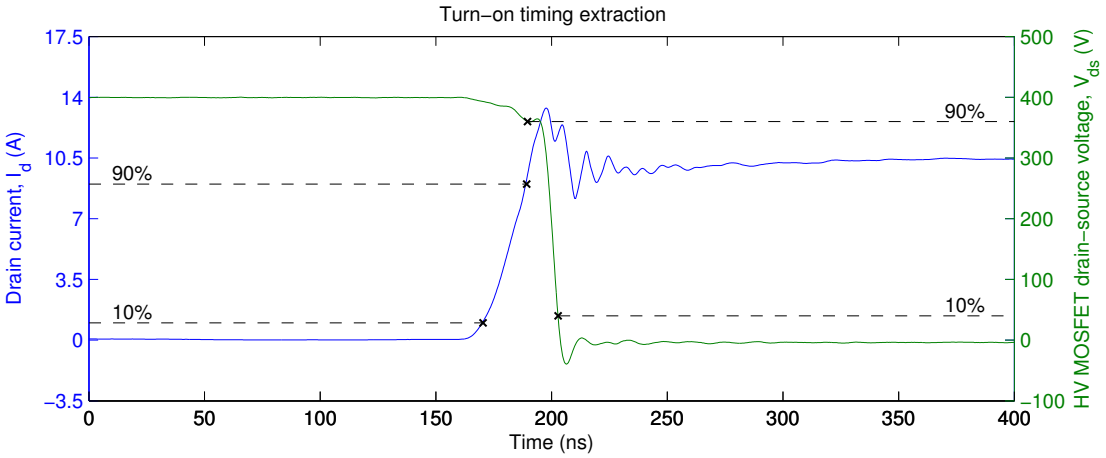


Figure D.8: Visualisation of the extraction of the rise/fall timing from the reconstructed drain-current (blue) and smoothed drain-source voltage (green) waveforms. The plot is annotated with the extracted 10 % and 90 % thresholds and timing.

D.2.8 Extraction of other switching performance metrics

Any number of other waveform features can be extracted by using and combining the techniques presented in Sections D.2.1 through D.2.7. Three additional switching metrics of interest are peak drain current, gate-drive voltage and switching loss. Peak drain current can be extracted by simply taking the maximum drain current over the interval of interest (centred at the rising edge of the second pulse) (see Fig. D.6 and Fig. D.15, lines 215–221). The gate drive voltage can be determined by taking the mean of the gate-source voltage waveform during the first pulse (shortened slightly to exclude the charge/discharge transients) (see Fig. D.1 and Fig. D.15, lines 135–137). Switching loss is determined by calculating the instantaneous power by taking the product of the drain current and drain-source voltage waveforms and integrating over the interval of interest (see Fig. D.15, lines 211–213).

Care should be taken to ensure the suitable versions of the waveform data are used, that is, the raw or filtered/smoothed versions. For example, it would be suitable to use the un-smoothed version of the gate-source waveform to extract the gate drive voltage, but may be preferential to use the smoothed version of the drain current to extract the effective peak current while rejecting the high-frequency ring.

In the techniques presented above there is also a lot of information discarded. Significantly more information can be extracted from the waveform data with appropriate additional post-processing. Particularly, there is another two switching edges which have not been analysed: a zero-current turn-on edge and two turn-off edges, one at the load current and one at a slightly higher current. Only minor modification to the processing described above would be required to extract this additional information. In this work extraction of the turn off transient at the same test current is also implemented, but the other two switching edges are ignored.

D.3 Visual validation of extracted features

Where large quantities of waveforms are to be processed automatically it is critical that mechanisms be put in place to validate quickly that feature extraction has been successful. This is most easily achieved visually, which requires a visual summary of the various steps of the feature extraction process as well as the final results. Plots showing the original/filtered waveforms annotated with visual representations of the extracted features, as well as the points from which features have been extracted, provide a good solution.

In the MATLAB implementation presented in this work, a six page feature extraction report is generated for each set of double-pulse waveforms processed (see Fig. D.15, lines 309–709). These reports provides a quick visual summary of the key feature extraction processes, allowing any errors in automated feature extraction of large datasets to be easily identified. An example feature extraction report generated in this work is presented in Figures D.9 through D.14.

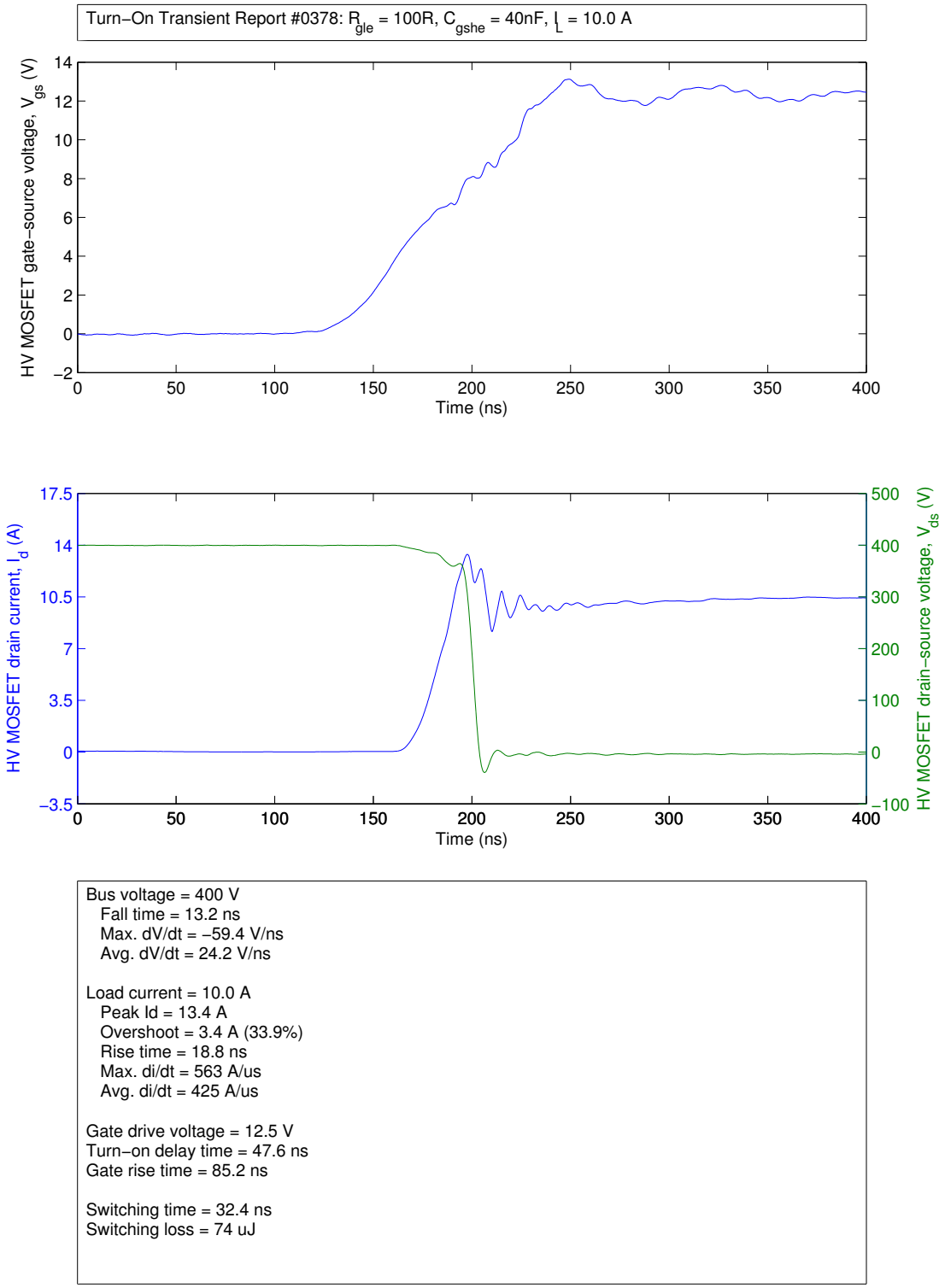


Figure D.9: Page 1 of 6 of an example feature extraction report. Shown are the post-processed turn-on gate-source voltage (top), drain-source voltage (middle, green) and drain current (middle, blue) waveforms along with a summary of the extracted turn-on switching performance metrics.

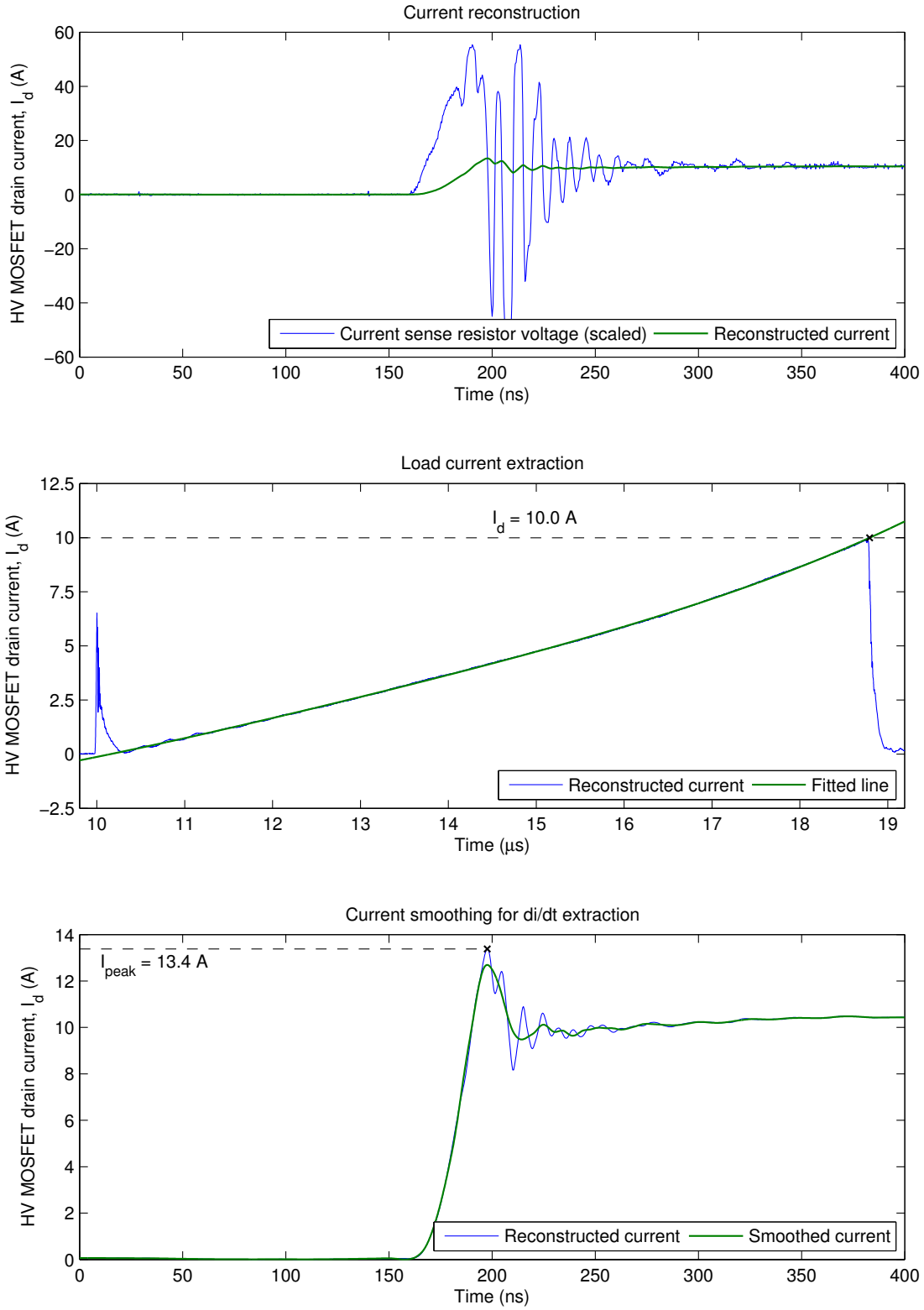


Figure D.10: Page 2 of 6 of an example feature extraction report. Visualised are the current reconstruction (top), load current extraction (middle) and current smoothing post-processing steps.

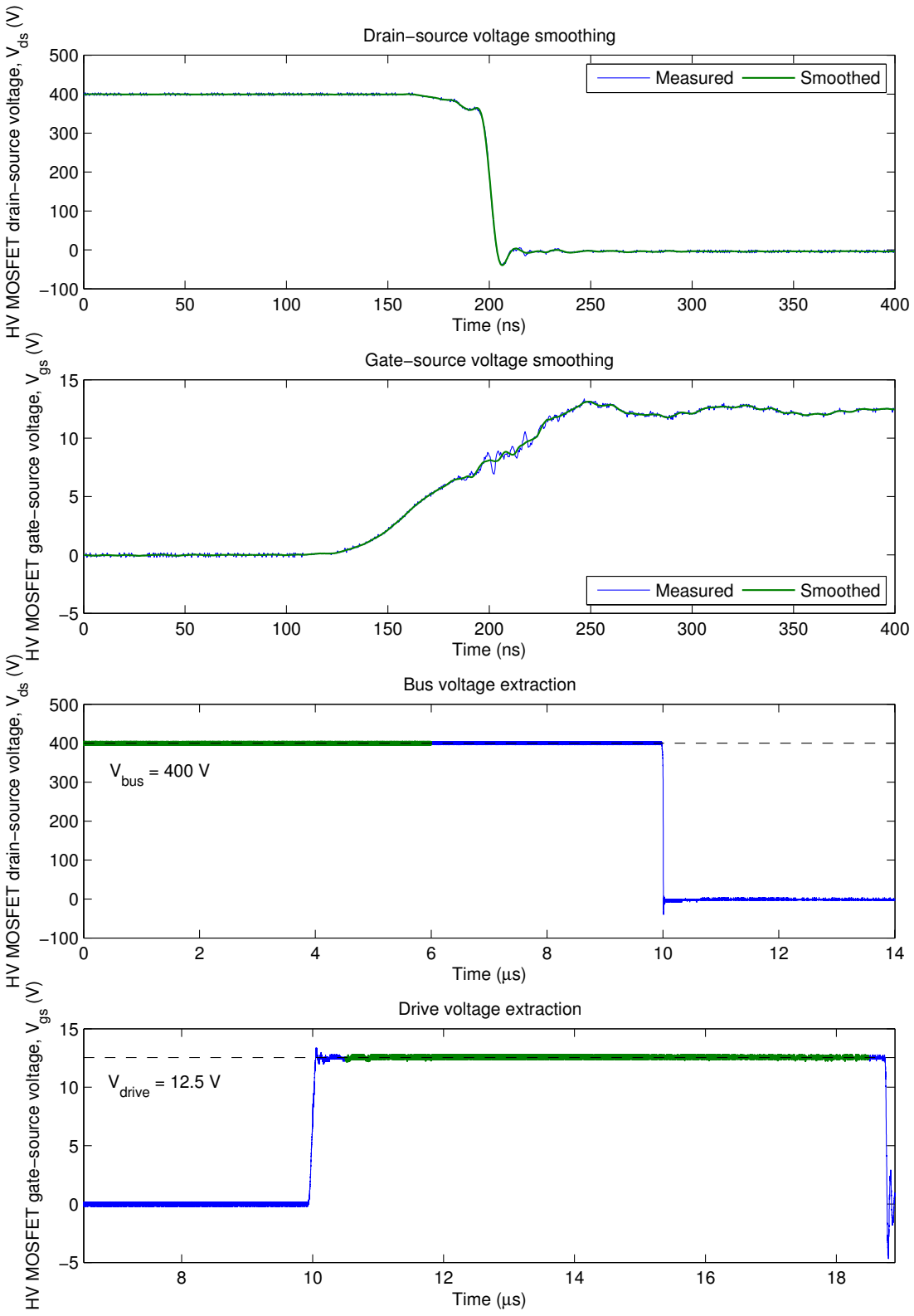


Figure D.11: Page 3 of 6 of an example feature extraction report. Visualised are the voltage waveform smoothing (top) and bus voltage and gate drive voltage extraction (bottom) post-processing steps.

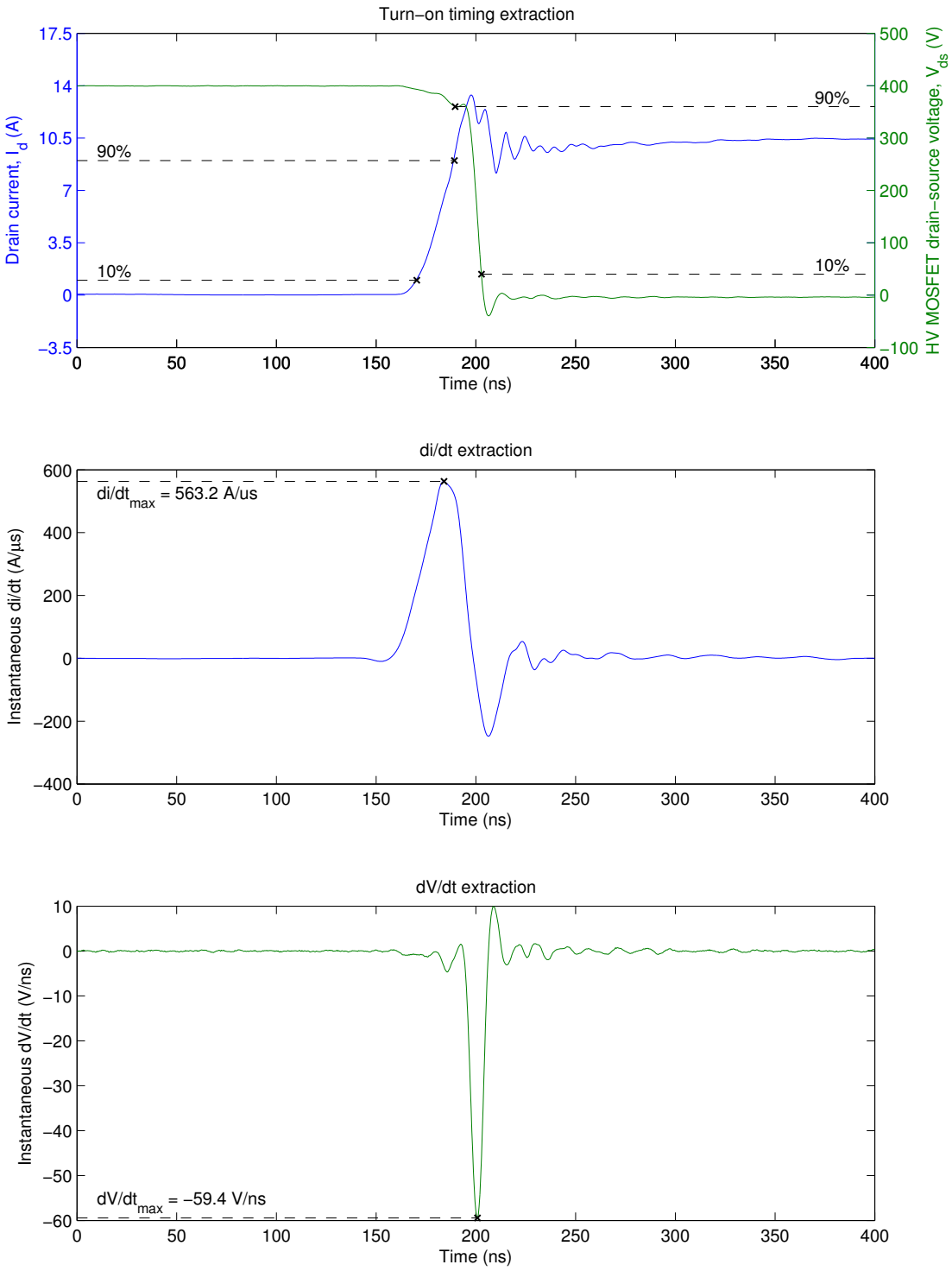


Figure D.12: Page 4 of 6 of an example feature extraction report. Visualised are the rise/fall timing (top), maximum dv/dt (middle) and maximum dv/dt (bottom) post-processing steps for a turn-on switching transient.

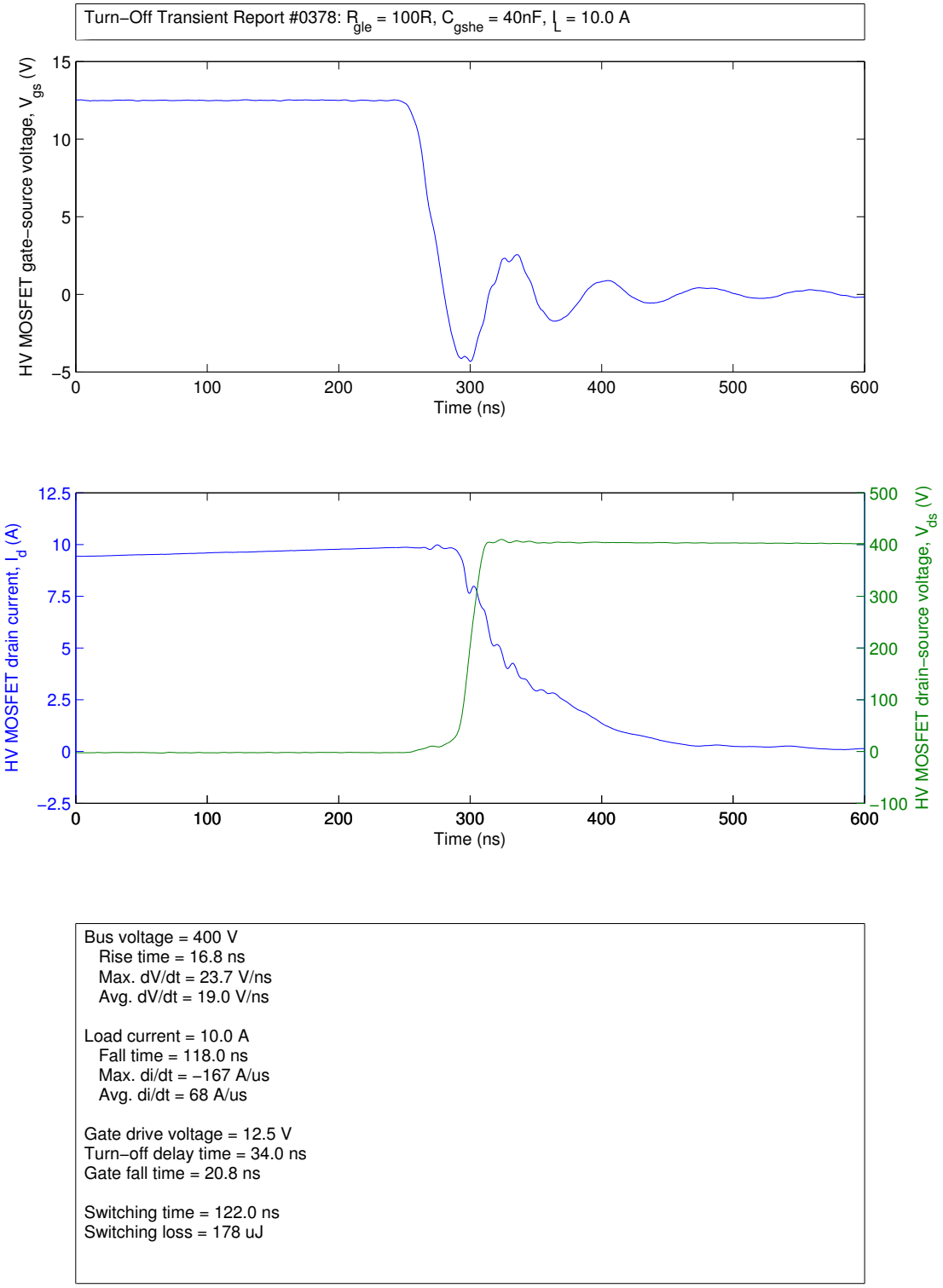


Figure D.13: Page 5 of 6 of an example feature extraction report. Shown are the post-processed turn-off gate-source voltage (top), drain-source voltage (middle, green) and drain current (middle, blue) waveforms along with a summary of the extracted turn-off switching performance metrics.

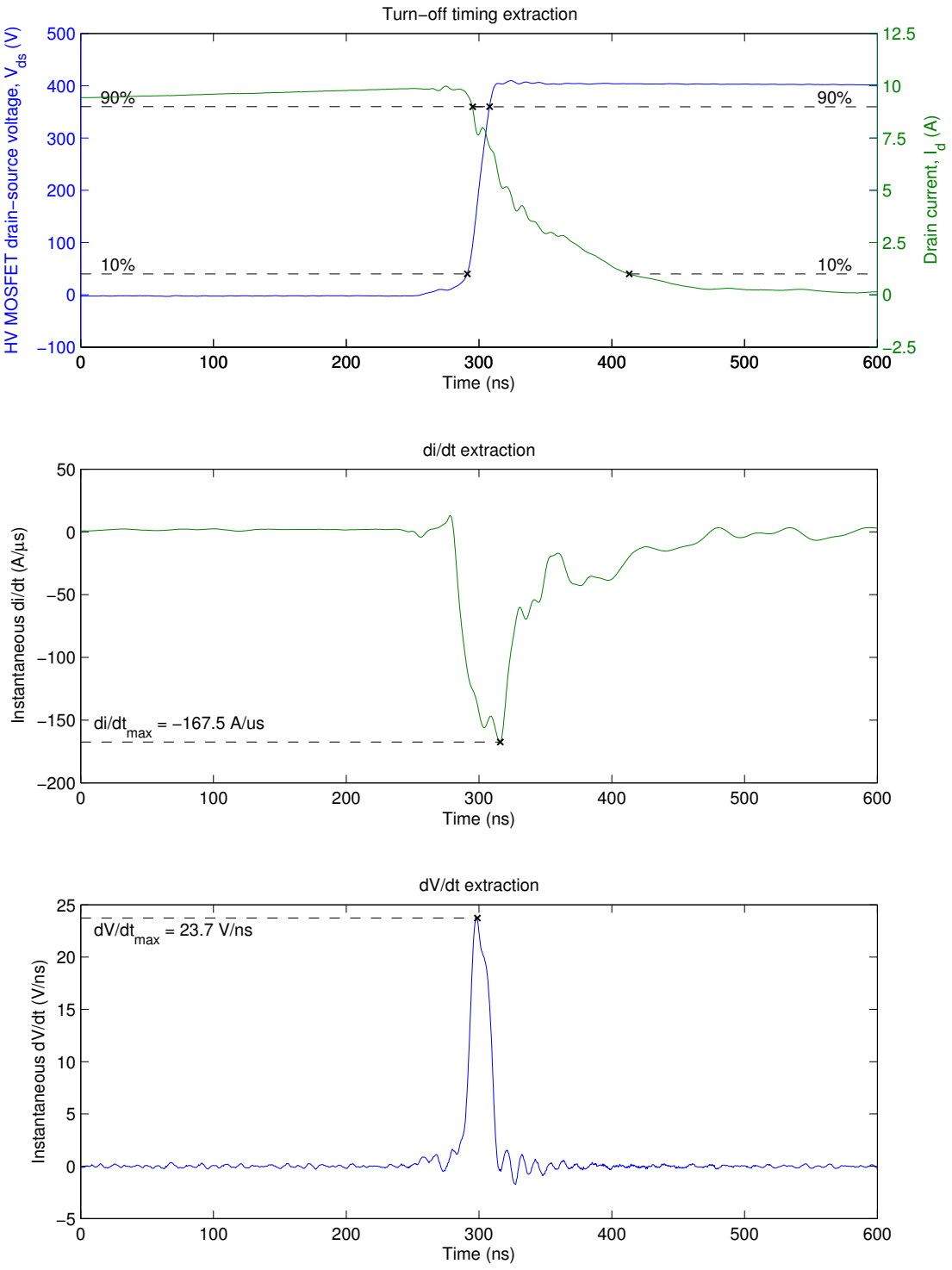


Figure D.14: Page 6 of 6 of an example feature extraction report. Visualised are the rise/fall timing (top), maximum dv/dt (middle) and maximum dv/dt (bottom) post-processing steps for a turn-off switching transient.

D.4 Post-processing implementation

A MATLAB script was developed to implement the feature extraction techniques described in Section D.2.

Each set of experimental waveform data was processed by the MATLAB script. A number of outputs were generated for each individual test: a feature extraction report in PDF format and the post-processed waveform and feature variables as a MATLAB struct. One output was generated from the entire dataset: a MATLAB struct containing all test conditions and extracted switching performance metrics.

D.4.1 Dependencies

D.4.1.1 isfread

`isfread` is a MATLAB function authored by Iain Robinson for the reading of Tektronix ISF binary waveform files into MATLAB. This function is published on MATLAB Central File Exchange. This function is required to load experimental waveform data captured from the Tektronix oscilloscope used in this work.

Files required: `isfread.m`
Available from: `isfread` at MATLAB Central File Exchange

D.4.1.2 append_pdfs

`append_pdfs` is a set of MATLAB functions authored by Oliver Woodford for the concatenation of multiple PDF documents into a single document. These functions are published on MATLAB Central File Exchange. These functions are used in this work to combine the individual PDF pages generated throughout the feature extraction process into a single feature extraction report.

Files required: `append_pdfs.m`, `ghostscript.m`, `user_string.m`
Available from: `append_pdfs` at MATLAB Central File Exchange

D.4.1.3 Ghostscript

Ghostscript is a utility required by `append_pdfs` for the processing and generation of PDF documents. Most users will likely already have a distribution of Ghostscript already installed. If this is not the case Ghostscript is available for download as outlined below.

Available from: Ghostscript Downloads

D.4.2 MATLAB Scripts

D.4.2.1 Feature extraction: `isfReport.m`

`isfReport.m` provides a MATLAB implementation for automated switching performance feature extraction from experimental double-pulse waveform data. The function takes the filename prefix for a set of double-pulse waveforms recorded from a Tektronix oscilloscope in the ISF binary file format. `isfReport.m` performs post-processing to extract switching performance metrics and returns the extracted features as well as generating a feature extraction report in PDF format. The function additionally saves the post-processed waveform data and low-level features used during the post-processing process (for use if subsequent post-processing, analysis or visualisation of the data are required). Parameters, return values and outputs for this implementation are outlined below and the function listing is provided in Fig. D.15.

Parameters:

`filename` Filename prefix of waveform set to process. `isfReport` expects three waveforms (CH1-CH3) with the `*.isf` extension and format. Example: passing a filename value of `'waveform'` would attempt to open and process the waveform files `waveformCH1.isf`, `waveformCH2.isf` and `waveformCH3.isf`.

Returns:

`features` MATLAB structure containing values for the extracted switching performance metrics.

Outputs:

`(filename).pdf` Feature extraction report in PDF format.

`(filename).mat` MATLAB structure containing the post-processed waveform data, extracted switching performance metrics and other low-level features extracted during post-processing.

Figure D.15: MATLAB function for extraction of switching performance features from double-pulse waveform data.

```
function features = isfReport(filename)

fileCH1 = sprintf('%sCH1.isf', filename);   % Vds trace
fileCH2 = sprintf('%sCH2.isf', filename);   % Id trace
fileCH3 = sprintf('%sCH3.isf', filename);   % Vgs trace

fileOut = sprintf('%s.pdf', filename);
delete(fileOut);

tokens = regexp(filename, '_', 'split');
Rgle = tokens{2};
Cgshe = tokens{3};
targetIL = tokens{4};
id = tokens{5};

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% INITIALISATION
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
warning('off','all');

Ts = 0.4e-9;    % sample time

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 1) IMPORT WAVEFORMS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
isf = isfread(fileCH1);    % Vds trace
t = isf.x;      % time
Vds = isf.y;    % Vds

isf = isfread(fileCH2);    % Id trace (V across shunt resistor)
iraw = isf.y;

isf = isfread(fileCH3);    % Vgs trace
Vgs = isf.y;

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 2) REMOVE ZERO OFFSETS
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
leadtime = 1e4;                 % leading edge of zero V, A (samples)

% calculate offsets
ioffset = mean(iraw(1:leadtime));
voffset = mean(Vgs(1:leadtime));

% remove offsets
iraw = iraw - ioffset;
Vgs = Vgs - voffset;
t = t - t(1);

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 3) RECONSTRUCT TRUE CURRENT
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Filter parameters
R = 0.1;        % sense resistance
```

```
L = 6.5e-9;     % inductance compensation

% Build filter
G = tf([1], [L R]); % Filter transfer fuction

% Filter current
Vr = R*iraw;        % Voltage across sense resistor
Id = lsim(G,Vr,t);   % Filter current

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 4) SMOOTH WAVEFORMS & CALCULATE DERIVATIVES
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Savitzky-Golay filter parameters for voltage smoothing
N = 9;
F = 71;

% Smooth Vds and calculate first derivative
Vds_smooth = sgolayfilt(Vds, N, F);
dvdt = sgolayfiltd(Vds, N, F, t(2));

% Smooth Vgs
Vgs_smooth = sgolayfilt(Vgs, N, F);

% Savitzky-Golay filter parameters for current smoothing
N = 4;
F = 101;

% Smooth Id and calculate first derivative
Id_smooth = sgolayfilt(Id, N, F);
didt = sgolayfiltd(Id, N, F, t(2));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 5) FEATURE EXTRACTION
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
leadtime = 6e-6;                    % Clean leading edge of test

%%% EXTRACT BUS VOLTAGE FROM CLEAN LEADING EDGE
Vbus = mean(Vds(1:leadtime/Ts));    % bus voltage

%%% FIND SWITCHING EDGES (use smooth Vds version)
trigger = 1;
while (Vds_smooth(trigger) > Vbus/2)
    trigger = trigger + 1;          % find first voltage fall
end;
turnOn_1st = trigger;
trigger = trigger + 100e-9/Ts;      % 100ns holdoff
while (Vds_smooth(trigger) < Vbus/2)
    trigger = trigger + 1;          % find first voltage rise
end;
turnOff_1st = trigger;
trigger = trigger + 100e-9/Ts;      % 100ns holdoff
while (Vds_smooth(trigger) > Vbus/2)
    trigger = trigger + 1;          % find first voltage fall
end;
turnOn_2nd = trigger;
trigger = trigger + 100e-9/Ts;      % 100ns holdoff
while (Vds_smooth(trigger) < Vbus/2)
    trigger = trigger + 1;          % find first voltage rise
end;
```

```
115 turnOff_2nd = trigger;
116
117 %%% DEFINE WINDOW FOR CURRENT RAMP
118 % Trim 400ns from start and 100ns from end of pulse one
119 rampWindow = (turnOn_1st+400e-9/Ts):(turnOff_1st-100e-9/Ts);
120 currentRamp = Id(rampWindow);
121
122 %%% FIT POLYNOMIAL TO CURRENT RAMP
123 if (sscanf(targetIL, '%d') <= 2)
124     fo = fit(t(rampWindow),currentRamp,'poly2');
125 else
126     fo = fit(t(rampWindow),currentRamp,'poly4');
127 end;
128
129 P = coeffvalues(fo);
130 currentFit = polyval(P,t);
131
132 %%% EXTRACT LOAD CURRENT
133 IL = currentFit(turnOff_1st);
134
135 %%% EXTRACT GATE DRIVE VOLTAGE
136 vgsWindow = rampWindow(250:end-500);
137 Vdrive = mean(Vgs(vgsWindow));
138
139 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% TURN-ON %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
140
141 %%% DEFINE WINDOW FOR TURN-ON INSTANT OF INTEREST
142 window = (turnOn_2nd-200e-9/Ts):(turnOn_2nd+200e-9/Ts);
143
144 %%% WINDOW PARAMETERS OF INTEREST
145 w_t = t(window);
146 w_t = w_t - w_t(1);
147
148 w_Vds = Vds_smooth(window); % use smoothed version
149 w_Vgs = Vgs_smooth(window); % use smoothed version
150 w_Id = Id(window);
151
152 w_dvdt = dvdt(window);
153 w_didt = didt(window);
154
155 %%% EXTRACT MAX DDT METRICS
156 max_dvdt = min(w_dvdt);
157 max_didt = max(w_didt);
158
159 t_max_dvdt = w_t(find(w_dvdt==max_dvdt, 1, 'first'));
160 t_max_didt = w_t(find(w_didt==max_didt, 1, 'first'));
161
162 %%% FIND KEY TIMING POINTS
163 % Voltage fall time
164 trigger = 1;
165 while (w_Vds(trigger) > 0.9*Vbus)
166     trigger = trigger + 1;          % Find 90% Vbus
167 end;
168 t_Vbus90 = w_t(trigger);
169
170 while (w_Vds(trigger) > 0.1*Vbus)
171     trigger = trigger + 1;          % Find 10% Vbus
172 end;
173 t_Vbus10 = w_t(trigger);
```

```
174
175 % Current rise time
176 trigger = 1;
177 while (w_Id(trigger) < 0.1*IL)
178     trigger = trigger + 1;          % Find 10% IL
179 end;
180 t_IL10 = w_t(trigger);
181
182 while (w_Id(trigger) < 0.9*IL)
183     trigger = trigger + 1;          % Find 90% IL
184 end;
185 t_IL90 = w_t(trigger);
186
187 % Gate rise time
188 trigger = 1;
189 while (w_Vgs(trigger) < 0.1*Vdrive)
190     trigger = trigger + 1;          % Find 10% Vdrive
191 end;
192 t_Vdrive10 = w_t(trigger);
193
194 while (w_Vgs(trigger) < 0.9*Vdrive)
195     trigger = trigger + 1;          % Find 90% Vdrive
196 end;
197 t_Vdrive90 = w_t(trigger);
198
199 %%% EXTRACT TIMING METRICS
200 t_sw = t_Vbus10 - t_IL10;               % Total switching time
201 t_rise = t_IL90 - t_IL10;               % Current rise time
202 t_fall = t_Vbus10 - t_Vbus90;           % Voltage fall time
203 t_rise_Vgs = t_Vdrive90 - t_Vdrive10;   % Gate-source voltage rise time
204 t_on = t_Vbus10 - t_Vdrive10;           % Turn-on time (datasheet)
205 t_don = t_Vbus90 - t_Vdrive10;          % Turn-on delay time (datasheet)
206
207 %%% EXTRACT AVG DDT METRICS
208 avg_dvdt = 0.8*Vbus/t_fall;
209 avg_didt = 0.8*IL/t_rise;
210
211 %%% CALCULATE SWITCHING LOSSES
212 w_Ploss = w_Id.*w_Vds;
213 Eloss = trapz(w_t,w_Ploss);     % Integrate switching energy
214
215 %%% EXTRACT MISC METRICS
216 Ipeak = max(w_Id);
217 t_Ipeak = w_t(find(w_Id==Ipeak, 1, 'first'));
218
219 % Find peak of smoothed version (excludes high-frequency ring)
220 Ipeaks = max(Id_smooth(window));
221 t_Ipeaks = w_t(find(Id_smooth(window)==Ipeaks, 1, 'first'));
222
223 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%% TURN-OFF %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
224
225 %%% DEFINE WINDOW FOR TURN-OFF INSTANT OF INTEREST
226 window_off = (turnOff_1st-300e-9/Ts):(turnOff_1st+300e-9/Ts);
227
228 %%% WINDOW PARAMETERS OF INTEREST
229 w_t_off = t(window_off);
230 w_t_off = w_t_off - w_t_off(1);
231
232 w_Vds_off = Vds_smooth(window_off); % use smoothed version
```

```
w_Vgs_off = Vgs_smooth(window_off); % use smoothed version
w_Id_off = Id(window_off);

w_dvdt_off = dvdt(window_off);
w_didt_off = didt(window_off);

%%% FIND KEY TIMING POINTS
% Gate fall time
trigger = 1;
while (w_Vgs_off(trigger) > 0.9*Vdrive)
    trigger = trigger + 1;          % Find 90% Vdrive
end;
t_Vdrive90_off = w_t_off(trigger);
trig_gate90 = trigger;

while (w_Vgs_off(trigger) > 0.1*Vdrive)
    trigger = trigger + 1;          % Find 10% Vdrive
end;
t_Vdrive10_off = w_t_off(trigger);
trig_gate10 = trigger;

% Voltage rise time
trigger = 1;
while (w_Vds_off(trigger) < 0.1*Vbus)
    trigger = trigger + 1;          % Find 10% Vbus
end;
t_Vbus10_off = w_t_off(trigger);
trig_Vds10 = trigger;

while (w_Vds_off(trigger) < 0.9*Vbus)
    trigger = trigger + 1;          % Find 90% Vbus
end;
t_Vbus90_off = w_t_off(trigger);
trig_Vds90 = trigger;

% Current fall time
trigger = trig_gate10;  % bound reging from gate fall
while (w_Id_off(trigger) > 0.9*IL)
    trigger = trigger + 1;          % Find 90% IL
end;
t_IL90_off = w_t_off(trigger);
trig_Id90 = trigger;

while (w_Id_off(trigger) > 0.1*IL)
    trigger = trigger + 1;          % Find 10% IL
end;
t_IL10_off = w_t_off(trigger);
trig_Id10 = trigger;

% USE 10-90% RISE FALL TIMES FOR WINDOWS
w_dvdt_off_bound = dvdt(window_off(trig_Vds10:trig_Vds90));
w_didt_off_bound = didt(window_off(trig_Id90:trig_Id10));

%%% EXTRACT MAX DDT METRICS
max_dvdt_off = max(w_dvdt_off_bound);
max_didt_off = min(w_didt_off_bound);

t_max_dvdt_off = w_t_off(trig_Vds10+find(w_dvdt_off_bound==max_dvdt_off, 1, '
    first'));
```

```
291 t_max_didt_off = w_t_off(trig_Id90+find(w_didt_off_bound==max_didt_off, 1, '
        first'));
292
293 %%% EXTRACT TIMING METRICS
294 t_sw_off = t_IL10_off - t_Vbus10_off;                % Total switching time
295 t_fall_off = t_IL10_off - t_IL90_off;                % Current fall time
296 t_rise_off = t_Vbus90_off - t_Vbus10_off;            % Voltage rise time
297 t_fall_Vgs_off = t_Vdrive10_off - t_Vdrive90_off;    % Gate-source voltage fall
         time
298 t_off = t_Vbus90_off - t_Vdrive90_off;              % Turn-on time (datasheet)
299 t_doff = t_Vbus10_off - t_Vdrive90_off;             % Turn-on delay time (
        datasheet)
300
301 %%% EXTRACT AVG DDT METRICS
302 avg_dvdt_off = 0.8*Vbus/t_rise_off;
303 avg_didt_off = 0.8*IL/t_fall_off;
304
305 %%% CALCULATE SWITCHING LOSSES
306 w_Ploss_off = w_Id_off.*w_Vds_off;
307 Eloss_off = trapz(w_t_off,w_Ploss_off);     % Integrate switching energy
308
309 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
310 % 6) PLOTTING
311 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
312 ilim = [-ceil(2*Ipeak*1.2/5) 5*ceil(2*Ipeak*1.2/5)]/2;
313 iticks = ilim(1):ceil(2*Ipeak*1.2/5)/2:ilim(2);
314
315 ilim_off = [-ceil(2*IL*1.2/5) 5*ceil(2*IL*1.2/5)]/2;
316 iticks_off = ilim_off(1):ceil(2*IL*1.2/5)/2:ilim_off(2);
317
318 %%% PAGE 1 - TURN-ON SWITCHING REPORT
319 fig1 = figure('Position',[-1000 100 850 1200]);
320
321 subplot(3,1,1); H = plot(w_t*1e9,Vgs_smooth(window));
322
323 xlabel('Time␣(ns)');
324 xlim([0 400]);
325 ylabel('HV␣MOSFET␣gate-source␣voltage,␣V_{gs}␣(V)');
326
327 subplot(3,1,2); [AX, H1, H2] = plotyy(w_t*1e9,w_Id,w_t*1e9,Vds_smooth(window))
        ;
328
329 xlabel('Time␣(ns)');
330 xlim(AX(1),[0 400]);
331 xlim(AX(2),[0 400]);
332 ylim(AX(1),ilim);
333 ylim(AX(2),[-100 500]);
334 set(AX(1),'YTick',iticks);
335 set(AX(2),'YTick',[-100:100:500]);
336 ylabel(AX(1), 'HV␣MOSFET␣drain␣current,␣I_{d}␣(A)');
337 ylabel(AX(2), 'HV␣MOSFET␣drain-source␣voltage,␣V_{ds}␣(V)');
338
339 tb = annotation('textbox',[0.13 0.076 0.775 0.28],'BackgroundColor', 'w');
340
341 s = sprintf('Bus␣voltage␣=␣%.0f␣V\n', Vbus);
342 s = horzcat(s, sprintf('␣␣␣Fall␣time␣=␣%.1f␣ns\n', t_fall*1e9));
343 s = horzcat(s, sprintf('␣␣␣Max.␣dV/dt␣=␣%.1f␣V/ns\n', max_dvdt/1e9));
344 s = horzcat(s, sprintf('␣␣␣Avg.␣dV/dt␣=␣%.1f␣V/ns\n', avg_dvdt/1e9));
345 s = horzcat(s, sprintf('\n'));
```

```
346
347 s = horzcat(s, sprintf('Load␣current␣=␣%.1f␣A\n', IL));
348 s = horzcat(s, sprintf('␣␣␣Peak␣Id␣=␣%.1f␣A\n', Ipeak));
349 s = horzcat(s, sprintf('␣␣␣Overshoot␣=␣%.1f␣A␣(%.1f%%)\n', Ipeak-IL, 100*(
        Ipeak-IL)/IL));
350 s = horzcat(s, sprintf('␣␣␣Rise␣time␣=␣%.1f␣ns\n', t_rise*1e9));
351 s = horzcat(s, sprintf('␣␣␣Max.␣di/dt␣=␣%.0f␣A/us\n', max_didt/1e6));
352 s = horzcat(s, sprintf('␣␣␣Avg.␣di/dt␣=␣%.0f␣A/us\n', avg_didt/1e6));
353 s = horzcat(s, sprintf('\n'));
354
355 s = horzcat(s, sprintf('Gate␣drive␣voltage␣=␣%.1f␣V\n', Vdrive));
356 s = horzcat(s, sprintf('Turn-on␣delay␣time␣=␣%.1f␣ns\n', t_don*1e9));
357 s = horzcat(s, sprintf('Gate␣rise␣time␣=␣%.1f␣ns\n', t_rise_Vgs*1e9));
358 s = horzcat(s, sprintf('\n'));
359
360 s = horzcat(s, sprintf('Switching␣time␣=␣%.1f␣ns\n', t_sw*1e9));
361 s = horzcat(s, sprintf('Switching␣loss␣=␣%.0f␣uJ\n', Eloss*1e6));
362
363 set(tb,'String',s);
364
365 annotation('textbox',[0.13 0.94 0.775 0.025],'String', sprintf('Turn-On␣
        Transient␣Report␣#%s:␣R_{gle}␣=␣%s,␣C_{gshe}␣=␣%s,␣I_L␣=␣%.1f␣A', id, Rgle
        , Cgshe, IL),'BackgroundColor', 'w');
366
367 %%% PAGE 2 - CURRENT POST-PROCESSING
368 fig2 = figure('Position',[-1000 100 850 1200]);
369
370 subplot(3,1,1); H = plot(w_t*1e9,iraw(window),w_t*1e9,w_Id);
371
372 xlabel('Time␣(ns)');
373 xlim([0 400]);
374 ylabel('HV␣MOSFET␣drain␣current,␣I_{d}␣(A)');
375 legend('Current␣sense␣resistor␣voltage␣(scaled)', 'Reconstructed␣current', '
        Location', 'SouthEast', 'Orientation', 'horizontal');
376 set(H(1),'LineWidth',0.5);
377 set(H(2),'LineWidth',1);
378 title(sprintf('Current␣reconstruction'));
379
380
381 fitWindow = (turnOn_1st-200e-9/Ts):(turnOff_1st+400e-9/Ts);
382 AX = subplot(3,1,2); H = plot(t(fitWindow)*1e6,Id(fitWindow),t(fitWindow)*1e6,
        currentFit(fitWindow));
383 hold on;
384 plot(t(turnOff_1st)*1e6,currentFit(turnOff_1st),'kx','MarkerSize',5,'LineWidth
        ',1);
385 plot([t(fitWindow(1)) t(fitWindow(end))]*1e6, [IL IL], 'k--');
386 hold off;
387
388 title(sprintf('Load␣current␣extraction'));
389 xlabel('Time␣({\mu}s)');
390 xlim([t(fitWindow(1)) t(fitWindow(end))]*1e6);
391 ylim(ilim_off);
392 set(AX,'YTick',iticks_off);
393 ylabel('HV␣MOSFET␣drain␣current,␣I_{d}␣(A)');
394 legend('Reconstructed␣current', 'Fitted␣line', 'Location', 'SouthEast', '
        Orientation', 'horizontal');
395 set(H(1),'LineWidth',0.5);
396 set(H(2),'LineWidth',1);
397
```

```
398 axes(AX);
399 Ylims = get(gca, 'YLim');
400 Yscale = Ylims(2)-Ylims(1);
401 Xlims = get(gca, 'XLim');
402 Xscale = Xlims(2)-Xlims(1);
403 text(Xlims(1)+0.5*Xscale, IL+(0.05*Yscale), sprintf('I_d = %.1f A', IL));
404
405 subplot(3,1,3); H = plot(w_t*1e9,w_Id,w_t*1e9,Id_smooth(window));
406 hold on;
407 plot(t_Ipeak*1e9, Ipeak, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
408 plot([0 t_Ipeak*1e9], [Ipeak Ipeak], 'k--');
409 Ylims = get(gca, 'YLim');
410 Yscale = Ylims(2)-Ylims(1);
411 text(10, Ipeak-(0.05*Yscale), sprintf('I_p_e_a_k = %.1f A',Ipeak));
412 hold off;
413
414 xlabel('Time (ns)');
415 xlim([0 400]);
416 ylabel('HV MOSFET drain current , I_{d} (A)');
417 legend('Reconstructed current', 'Smoothed current', 'Location', 'SouthEast', '
        Orientation', 'horizontal');
418 set(H(1),'LineWidth',0.5);
419 set(H(2),'LineWidth',1);
420 title(sprintf('Current smoothing for di/dt extraction'));
421
422 %%% PAGE 3 - VOLTAGE POST-PROCESSING
423 fig3 = figure('Position',[-1000 100 850 1200]);
424
425 subplot(4,1,1); H = plot(w_t*1e9,Vds(window),w_t*1e9,w_Vds);
426
427 xlabel('Time (ns)');
428 xlim([0 400]);
429 ylabel('HV MOSFET drain-source voltage , V_{ds} (V)');
430 legend('Measured', 'Smoothed', 'Location', 'NorthEast', 'Orientation', '
        horizontal');
431 set(H(1),'LineWidth',0.5);
432 set(H(2),'LineWidth',1);
433 title(sprintf('Drain-source votage smoothing'));
434
435 subplot(4,1,2); H = plot(w_t*1e9,Vgs(window),w_t*1e9,w_Vgs);
436
437 xlabel('Time (ns)');
438 xlim([0 400]);
439 ylabel('HV MOSFET gate-source voltage , V_{gs} (V)');
440 legend('Measured', 'Smoothed', 'Location', 'SouthEast', 'Orientation', '
        horizontal');
441 set(H(1),'LineWidth',0.5);
442 set(H(2),'LineWidth',1);
443 title(sprintf('Gate-source votage smoothing'));
444
445 subplot(4,1,3); H = plot(t(1:turnOn_1st+10000)*1e6,Vds(1:turnOn_1st+10000),t
        (1:leadtime/Ts)*1e6,Vds(1:leadtime/Ts));
446 hold on;
447 plot([t(1) t(turnOn_1st+10000)]*1e6, [Vbus Vbus], 'k--');
448 Ylims = get(gca, 'YLim');
449 Yscale = Ylims(2)-Ylims(1);
450 Xlims = get(gca, 'XLim');
451 Xscale = Xlims(2)-Xlims(1);
452 text(Xlims(1)+0.03*Xscale, Vbus-(0.08*Yscale), sprintf('V_b_u_s = %.0f V',
```

```
        Vbus));
453 hold off;
454
455 xlabel('Time␣({\mu}s)');
456 xlim([0 t(turnOn_1st+10000)*1e6]);
457 ylabel('HV␣MOSFET␣drain-source␣voltage,␣V_{ds}␣(V)');
458 set(H(1),'LineWidth',0.5);
459 set(H(2),'LineWidth',1);
460 title(sprintf('Bus␣votage␣extraction'));
461
462 subplot(4,1,4); H = plot(t(vgsWindow(1)-10000:vgsWindow(end)+1000)*1e6,Vgs(
        vgsWindow(1)-10000:vgsWindow(end)+1000),t(vgsWindow)*1e6,Vgs(vgsWindow));
463 hold on;
464 plot([t(vgsWindow(1)-10000) t(vgsWindow(end)+1000)]*1e6, [Vdrive Vdrive], 'k--
        ');
465
466 xlabel('Time␣({\mu}s)');
467 xlim([t(vgsWindow(1)-10000) t(vgsWindow(end)+1000)]*1e6);
468 ylabel('HV␣MOSFET␣gate-source␣voltage,␣V_{gs}␣(V)');
469 set(H(1),'LineWidth',0.5);
470 set(H(2),'LineWidth',1);
471 title(sprintf('Drive␣votage␣extraction'));
472
473 Ylims = get(gca, 'YLim');
474 Yscale = Ylims(2)-Ylims(1);
475 Xlims = get(gca, 'XLim');
476 Xscale = Xlims(2)-Xlims(1);
477 text(Xlims(1)+0.03*Xscale, Vdrive-(0.08*Yscale), sprintf('V_d_r_i_v_e␣=␣%.1f␣V
        ', Vdrive));
478 hold off;
479
480 %%% PAGE 4 - DDT FEATURE EXTRACTION
481 fig4 = figure('Position',[-1000 100 850 1200]);
482
483 subplot(3,1,1); [AX, H1, H2] = plotyy(w_t*1e9,w_Id,w_t*1e9,Vds_smooth(window))
        ;
484 hold(AX(1), 'on'); hold(AX(2), 'on');
485 plot(AX(1), t_IL10*1e9, 0.1*IL, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
486 plot(AX(1), t_IL90*1e9, 0.9*IL, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
487 plot(AX(2), t_Vbus10*1e9, 0.1*Vbus, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
488 plot(AX(2), t_Vbus90*1e9, 0.9*Vbus, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
489 plot(AX(1), [0 t_IL10*1e9], [0.1*IL 0.1*IL], 'k--');
490 plot(AX(1), [0 t_IL90*1e9], [0.9*IL 0.9*IL], 'k--');
491 plot(AX(2), [t_Vbus10*1e9 400], [0.1*Vbus 0.1*Vbus], 'k--');
492 plot(AX(2), [t_Vbus90*1e9 400], [0.9*Vbus 0.9*Vbus], 'k--');
493 hold(AX(1),'off'); hold(AX(2),'off');
494
495 xlabel('Time␣(ns)');
496 xlim(AX(1),[0 400]);
497 xlim(AX(2),[0 400]);
498 ylim(AX(1),ilim);
499 ylim(AX(2),[-100 500]);
500 set(AX(1),'YTick',iticks);
501 set(AX(2),'YTick',[-100:100:500]);
502 ylabel(AX(1), 'Drain␣current,␣I_{d}␣(A)');
503 ylabel(AX(2), 'HV␣MOSFET␣drain-source␣voltage,␣V_{ds}␣(V)');
504 title(sprintf('Turn-on␣timing␣extraction'));
505
506 axes(AX(1));
```

```
Ylims = get(AX(1), 'YLim');
Yscale = Ylims(2)-Ylims(1);
text(10, 0.1*IL+(0.03*Yscale), '10%');
text(10, 0.9*IL+(0.03*Yscale), '90%');
axes(AX(2));
Ylims = get(AX(2), 'YLim');
Yscale = Ylims(2)-Ylims(1);
text(370, 0.1*Vbus+(0.03*Yscale), '10%');
text(370, 0.9*Vbus+(0.03*Yscale), '90%');

subplot(3,1,2); H = plot(w_t*1e9,w_didt/1e6);
hold on;
plot(t_max_didt*1e9, max_didt/1e6, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
plot([w_t(1) t_max_didt]*1e9, [max_didt max_didt]/1e6, 'k--');
Ylims = get(gca, 'YLim');
Yscale = Ylims(2)-Ylims(1);
text(w_t(1)*1e9+10, max_didt/1e6-(0.05*Yscale), sprintf('di/dt_m_a_x = %.1f A/
    us', max_didt/1e6));
hold off;

xlabel('Time (ns)');
xlim([0 400]);
ylabel('Instantaneous di/dt (A/{\mu}s)');
title(sprintf('di/dt extraction'));

subplot(3,1,3); H = plot(w_t*1e9,w_dvdt/1e9,'color',[0 0.5 0]);
hold on;
plot(t_max_dvdt*1e9, max_dvdt/1e9, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
plot([w_t(1) t_max_dvdt]*1e9, [max_dvdt max_dvdt]/1e9, 'k--');
Ylims = get(gca, 'YLim');
Yscale = Ylims(2)-Ylims(1);
text(w_t(1)*1e9+10, max_dvdt/1e9+(0.05*Yscale), sprintf('dV/dt_m_a_x = %.1f V/
    ns', max_dvdt/1e9));
hold off;

xlabel('Time (ns)');
xlim([0 400]);
ylabel('Instantaneous dV/dt (V/ns)');
title(sprintf('dV/dt extraction'));

%%% PAGE 5 - TURN-OFF SWITCHING REPORT
fig5 = figure('Position',[-1000 100 850 1200]);

subplot(3,1,1); H = plot(w_t_off*1e9,w_Vgs_off);

xlabel('Time (ns)');
xlim([0 600]);
ylabel('HV MOSFET gate-source voltage , V_{gs} (V)');

subplot(3,1,2); [AX, H1, H2] = plotyy(w_t_off*1e9,w_Id_off,w_t_off*1e9,
    w_Vds_off);

xlabel('Time (ns)');
xlim(AX(1),[0 600]);
xlim(AX(2),[0 600]);
ylim(AX(1),ilim_off);
ylim(AX(2),[-100 500]);
set(AX(1),'YTick',iticks_off);
set(AX(2),'YTick',[-100:100:500]);
```

```
ylabel(AX(1), 'HV␣MOSFET␣drain␣current␣,␣I_{d}␣(A)');
ylabel(AX(2), 'HV␣MOSFET␣drain-source␣voltage␣,␣V_{ds}␣(V)');

tb = annotation('textbox',[0.13 0.076 0.775 0.25],'BackgroundColor', 'w');

s2 = sprintf('Bus␣voltage␣=␣%.0f␣V\n', Vbus);
s2 = horzcat(s2, sprintf('␣␣␣Rise␣time␣=␣%.1f␣ns\n', t_rise_off*1e9));
s2 = horzcat(s2, sprintf('␣␣␣Max.␣dV/dt␣=␣%.1f␣V/ns\n', max_dvdt_off/1e9));
s2 = horzcat(s2, sprintf('␣␣␣Avg.␣dV/dt␣=␣%.1f␣V/ns\n', avg_dvdt_off/1e9));
s2 = horzcat(s2, sprintf('\n'));

s2 = horzcat(s2, sprintf('Load␣current␣=␣%.1f␣A\n', IL));
s2 = horzcat(s2, sprintf('␣␣␣Fall␣time␣=␣%.1f␣ns\n', t_fall_off*1e9));
s2 = horzcat(s2, sprintf('␣␣␣Max.␣di/dt␣=␣%.0f␣A/us\n', max_didt_off/1e6));
s2 = horzcat(s2, sprintf('␣␣␣Avg.␣di/dt␣=␣%.0f␣A/us\n', avg_didt_off/1e6));
s2 = horzcat(s2, sprintf('\n'));

s2 = horzcat(s2, sprintf('Gate␣drive␣voltage␣=␣%.1f␣V\n', Vdrive));
s2 = horzcat(s2, sprintf('Turn-off␣delay␣time␣=␣%.1f␣ns\n', t_doff*1e9));
s2 = horzcat(s2, sprintf('Gate␣fall␣time␣=␣%.1f␣ns\n', t_fall_Vgs_off*1e9));
s2 = horzcat(s2, sprintf('\n'));

s2 = horzcat(s2, sprintf('Switching␣time␣=␣%.1f␣ns\n', t_sw_off*1e9));
s2 = horzcat(s2, sprintf('Switching␣loss␣=␣%.0f␣uJ\n', Eloss_off*1e6));

set(tb,'String',s2);

annotation('textbox',[0.13 0.94 0.775 0.025],'String', sprintf('Turn-Off␣
    Transient␣Report␣#%s:␣R_{gle}␣=␣%s,␣C_{gshe}␣=␣%s,␣I_L␣=␣%.1f␣A', id, Rgle
    , Cgshe, IL),'BackgroundColor', 'w');

%%% PAGE 6 - DDT FEATURE EXTRACTION
fig6 = figure('Position',[-1000 100 850 1200]);

subplot(3,1,1); [AX, H1, H2] = plotyy(w_t_off*1e9,w_Vds_off,w_t_off*1e9,
    w_Id_off);
hold(AX(1), 'on'); hold(AX(2), 'on');
plot(AX(2), t_IL10_off*1e9, 0.1*IL, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
plot(AX(2), t_IL90_off*1e9, 0.9*IL, 'kx', 'MarkerSize', 5, 'LineWidth', 1);
plot(AX(1), t_Vbus10_off*1e9, 0.1*Vbus, 'kx', 'MarkerSize', 5, 'LineWidth', 1)
    ;
plot(AX(1), t_Vbus90_off*1e9, 0.9*Vbus, 'kx', 'MarkerSize', 5, 'LineWidth', 1)
    ;
plot(AX(2), [t_IL10_off*1e9 600], [0.1*IL 0.1*IL], 'k--');
plot(AX(2), [t_IL90_off*1e9 600], [0.9*IL 0.9*IL], 'k--');
plot(AX(1), [0 t_Vbus10_off*1e9], [0.1*Vbus 0.1*Vbus], 'k--');
plot(AX(1), [0 t_Vbus90_off*1e9], [0.9*Vbus 0.9*Vbus], 'k--');
hold(AX(1),'off'); hold(AX(2),'off');

xlabel('Time␣(ns)');
xlim(AX(2),[0 600]);
xlim(AX(1),[0 600]);
ylim(AX(2),ilim_off);
ylim(AX(1),[-100 500]);
set(AX(2),'YTick',iticks_off);
set(AX(1),'YTick',[-100:100:500]);
ylabel(AX(2), 'Drain␣current␣,␣I_{d}␣(A)');
ylabel(AX(1), 'HV␣MOSFET␣drain-source␣voltage␣,␣V_{ds}␣(V)');
title(sprintf('Turn-off␣timing␣extraction'));
```

```
617
618  axes(AX(1));
619  Ylims = get(gca, 'YLim');
620  Yscale = Ylims(2)-Ylims(1);
621  text(15, 0.1*Vbus+(0.03*Yscale), '10%');
622  text(15, 0.9*Vbus+(0.03*Yscale), '90%');
623  axes(AX(2));
624  Ylims = get(gca, 'YLim');
625  Yscale = Ylims(2)-Ylims(1);
626  text(555, 0.1*IL+(0.03*Yscale), '10%');
627  text(555, 0.9*IL+(0.03*Yscale), '90%');
628
629  subplot(3,1,2); H = plot(w_t_off*1e9,w_didt_off/1e6,'color',[0 0.5 0]);
630  hold on;
631  plot(t_max_didt_off*1e9, max_didt_off/1e6, 'kx', 'MarkerSize', 5, 'LineWidth',
         1);
632  plot([w_t_off(1) t_max_didt_off]*1e9, [max_didt_off max_didt_off]/1e6, 'k--');
633  Ylims = get(gca, 'YLim');
634  Yscale = Ylims(2)-Ylims(1);
635  text(w_t_off(1)*1e9+10, max_didt_off/1e6+(0.05*Yscale), sprintf('di/dt_m_a_x␣=
       ␣%.1f␣A/us', max_didt_off/1e6));
636  hold off;
637
638  xlabel('Time␣(ns)');
639  xlim([0 600]);
640  ylabel('Instantaneous␣di/dt␣(A/{\mu}s)');
641  title(sprintf('di/dt␣extraction'));
642
643  subplot(3,1,3); H = plot(w_t_off*1e9,w_dvdt_off/1e9);
644  hold on;
645  plot(t_max_dvdt_off*1e9, max_dvdt_off/1e9, 'kx', 'MarkerSize', 5, 'LineWidth',
         1);
646  plot([w_t_off(1) t_max_dvdt_off]*1e9, [max_dvdt_off max_dvdt_off]/1e9, 'k--');
647  Ylims = get(gca, 'YLim');
648  Yscale = Ylims(2)-Ylims(1);
649  text(w_t_off(1)*1e9+10, max_dvdt_off/1e9-(0.05*Yscale), sprintf('dV/dt_m_a_x␣=
       ␣%.1f␣V/ns', max_dvdt_off/1e9));
650  hold off;
651
652  xlabel('Time␣(ns)');
653  xlim([0 600]);
654  ylabel('Instantaneous␣dV/dt␣(V/ns)');
655  title(sprintf('dV/dt␣extraction'));
656
657  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
658  % 7) PRINT
659  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
660
661  set(fig1, 'PaperType', 'A4');
662  set(fig1, 'PaperUnits', 'normalized');
663  set(fig1, 'PaperPosition', [0,0,1,1]);
664  print(fig1, '-dpdf', 'p1.pdf');
665
666  set(fig2, 'PaperType', 'A4');
667  set(fig2, 'PaperUnits', 'normalized');
668  set(fig2, 'PaperPosition', [0,0,1,1]);
669  print(fig2, '-dpdf', 'p2.pdf');
670
671  set(fig3, 'PaperType', 'A4');
```

```
672  set(fig3, 'PaperUnits', 'normalized');
673  set(fig3, 'PaperPosition', [0,0,1,1]);
674  print(fig3, '-dpdf', 'p3.pdf');
675
676  set(fig4, 'PaperType', 'A4');
677  set(fig4, 'PaperUnits', 'normalized');
678  set(fig4, 'PaperPosition', [0,0,1,1]);
679  print(fig4, '-dpdf', 'p4.pdf');
680
681  set(fig5, 'PaperType', 'A4');
682  set(fig5, 'PaperUnits', 'normalized');
683  set(fig5, 'PaperPosition', [0,0,1,1]);
684  print(fig5, '-dpdf', 'p5.pdf');
685
686  set(fig6, 'PaperType', 'A4');
687  set(fig6, 'PaperUnits', 'normalized');
688  set(fig6, 'PaperPosition', [0,0,1,1]);
689  print(fig6, '-dpdf', 'p6.pdf');
690
691  append_pdfs(fileOut, 'p1.pdf', 'p2.pdf', 'p3.pdf', 'p4.pdf', 'p5.pdf', 'p6.pdf
         ');
692
693  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
694  % 8) CLEANUP
695  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
696
697  delete(fig1);
698  delete(fig2);
699  delete(fig3);
700  delete(fig4);
701  delete(fig5);
702  delete(fig6);
703
704  delete('p1.pdf');
705  delete('p2.pdf');
706  delete('p3.pdf');
707  delete('p4.pdf');
708  delete('p5.pdf');
709  delete('p6.pdf');
710
711  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
712  % 9) RETURN DATA
713  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
714
715  features = struct;
716
717  % Test conditions
718  features.id = id;
719  features.Rgle = Rgle;
720  features.Cgshe = Cgshe;
721  features.targetIL = targetIL;
722
723  % DC value extraction
724  features.Vbus = Vbus;
725  features.IL = IL;
726  features.Vdrive = Vdrive;
727
728  % Turn-on features
729  features.max_dvdt = max_dvdt;
```

```
730  features.avg_dvdt = avg_dvdt;
731
732  features.max_didt = max_didt;
733  features.avg_didt = avg_didt;
734  features.Ipeak = Ipeak;
735  features.Ipeaks = Ipeaks;
736
737  features.t_rise = t_rise;
738  features.t_fall = t_fall;
739  features.t_sw = t_sw;
740  features.t_rise_Vgs = t_rise_Vgs;
741  features.t_don = t_don;
742  features.t_on = t_on;
743
744  features.Eloss = Eloss;
745
746  % Turn-off features
747  features.max_dvdt_off = max_dvdt_off;
748  features.avg_dvdt_off = avg_dvdt_off;
749
750  features.max_didt_off = max_didt_off;
751  features.avg_didt_off = avg_didt_off;
752
753  features.t_rise_off = t_rise_off;
754  features.t_fall_off = t_fall_off;
755  features.t_sw_off = t_sw_off;
756  features.t_fall_Vgs_off = t_fall_Vgs_off;
757  features.t_doff = t_doff;
758  features.t_off = t_off;
759
760  features.Eloss_off = Eloss_off;
761
762  % Summary
763  toString = sprintf('Double-pulse␣Feature␣Extraction␣Report␣#%s:␣R_{gle}␣=␣%s,␣
         C_{gshe}␣=␣%s,␣I_L␣=␣%.1f␣A\n\n', id, Rgle, Cgshe, IL);
764  toString = sprintf('%s=====␣TURN-ON␣=====\n%s\n',toString,s);
765  toString = sprintf('\n=====␣TURN-OFF␣=====\n%s\n',toString,s2);
766
767  features.toString = toString;
768
769  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
770  % 10) OUTPUT
771  %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
772
773  % Collect waveform data into structure
774  waveform = struct;
775
776  waveform.t = t;
777
778  waveform.Vds = Vds;
779  waveform.Vds_smooth = Vds_smooth;
780  waveform.dvdt = dvdt;
781
782  waveform.Vgs = Vgs;
783  waveform.Vgs_smooth = Vgs_smooth;
784
785  waveform.Id = Id;
786  waveform.Id_smooth = Id_smooth;
787  waveform.didt = didt;
```

```
788  waveform.iraw = iraw;
789
790  waveform.currentFit = currentFit;
791
792  % Collect timing data into structure
793  timing = struct;
794
795  timing.window = window;
796  timing.window_off = window_off;
797  timing.turnOn_1st = turnOn_1st;
798  timing.turnOn_2nd = turnOn_2nd;
799  timing.turnOff_1st = turnOff_1st;
800  timing.turnOff_2nd = turnOff_2nd;
801
802  % Include timing and feature data with waveform data
803  waveform.timing = timing;
804  waveform.feature = features;
805
806  % Save to file
807  save(sprintf('%s.mat', filename), 'waveform');
```

D.4.2.2 Post-processing sequencing: `postProcess.m`

`postProcess.m` provides a MATLAB implementation to iterate over an experimental dataset and perform automated feature extraction using `isfReport.m`. This function provides, additionally, a link between waveform files recorded from an oscilloscope and the test conditions for which the data were recorded. Raw waveforms files are copied into the specified output directory and renamed with meaningful filenames that capture the corresponding test conditions. The function expects waveforms to be named `tekXXXXCHY.isf`, where XXXX is the four digit ID of the waveform and Y is the channel number.

An Excel spreadsheet is used to specify the test conditions for each waveform as well as specifying which waveform data files should be post-processed. A copy of Microsoft Excel must be installed on the system on which the function is executed in order for MATLAB to process the input file. The function captures the features extracted from each waveform set, along with the corresponding test conditions, into a single MATLAB structure. This MATLAB structure, therefore, contains switching performance features across the entire parameter space and can be used for subsequent visualisation and analysis.

Parameters:

`filename` Filename of the Excel spreadsheet that specifies the set of waveform data to process. `postProcess.m` expects and Excel spreadsheet with one row of header data. Column B should contain the four digit ID for the waveform *as a string*. Columns C through F should contain the gate resistance, gate-source capacitance and target load current test conditions respectively. Capacitance values should be stored as strings with either a `'nF'` or `'pF'` suffix. Column L should contain a Boolean value (in Excel, `'TRUE'` or `'FALSE'`) indicating whether the waveform should be processed.

`name` Specifies the name of the output directory and prefix for renamed files. Should not contain underscores or this will interfere with the feature extraction post-processing. The output directory will be named `out_(name)`.

Returns:

`data` MATLAB structure containing extracted switching performance features from every processed waveform, along with corresponding test conditions.

Outputs:

`out_(name)\*.isf`	Meaningfully renamed waveform files.
`out_(name)\*.png`	Meaningfully renamed oscilloscope screen captures.
`out_(name)\*.set`	Meaningfully renamed oscilloscope settings.
`out_(name)\*.pdf`	Feature extraction report generated by `isfReport.m` for each waveform set.
`out_(name)\data.m`	MATLAB structure containing extracted switching performance features from every processed waveform, along with corresponding test conditions.

Figure D.16: MATLAB function for iteration over an experimental dataset to conduct feature extraction for each recorded waveform.

```
1  function data = postProcess(filename, name)
2
3  warning('off','all');
4
5  % Load Excel file that indexes waveforms
6  [num,txt,raw] = xlsread(filename);
7  text = txt(2:end, :);
8
9  % Filter for waveforms to be processed
10 toProcess = num(:,end) == 1;
11
12 % Extract test conditions
13 id = text(toProcess, 2);
14 Rgle = round(num(toProcess, 1));
15 Cgshe = text(toProcess, 4);
16 IL = num(toProcess, 3);
17
18 % Initialise cell arrays of waveform files to process
19 numFiles = size(id,1);
20 src = cell(numFiles,1);
21 dest = cell(numFiles,1);
22
23 % Generate source and destination filenames
24 for i = 1:numFiles
25     src{i} = sprintf('data\\tek%s',id{i});
26     dest{i} = sprintf('%s_%dR_%s_%02d_%s',name,Rgle(i),Cgshe{i},IL(i),id{i});
27 end;
28
29 % Create output directory
30 mkdir(sprintf('out_%s', name));
31
32 % Copy wavefrom data to output directory
33 for i = 1:numFiles
34     fprintf('Copying file %03d/%d: %s -> %s\n', i, numFiles, src{i}, dest{i});
35     copyfile(sprintf('%sCH1.isf', src{i}), sprintf('out_%s\\%sCH1.isf', name,
           dest{i}));
36     copyfile(sprintf('%sCH2.isf', src{i}), sprintf('out_%s\\%sCH2.isf', name,
           dest{i}));
37     copyfile(sprintf('%sCH3.isf', src{i}), sprintf('out_%s\\%sCH3.isf', name,
```

```
            dest{i}));
38      copyfile(sprintf('%s.png', src{i}), sprintf('out_%s\\%s.png', name, dest{i
            }));
39  end;
40
41  % Change to output directory
42  cd(sprintf('out_%s', name));
43
44  % Initialise output data structure
45  data = struct;
46
47  data.id = cell(numFiles,1);
48  data.Rgle = zeros(numFiles,1);
49  data.Cgshe = zeros(numFiles,1);
50  data.targetIL = zeros(numFiles,1);
51
52  data.Vbus = zeros(numFiles,1);
53  data.IL = zeros(numFiles,1);
54  data.Vdrive = zeros(numFiles,1);
55
56  data.max_dvdt = zeros(numFiles,1);
57  data.avg_dvdt = zeros(numFiles,1);
58
59  data.max_didt = zeros(numFiles,1);
60  data.avg_didt = zeros(numFiles,1);
61  data.Ipeak = zeros(numFiles,1);
62  data.Ipeaks = zeros(numFiles,1);
63
64  data.t_rise = zeros(numFiles,1);
65  data.t_fall = zeros(numFiles,1);
66  data.t_sw = zeros(numFiles,1);
67  data.t_rise_Vgs = zeros(numFiles,1);
68  data.t_don = zeros(numFiles,1);
69  data.t_on = zeros(numFiles,1);
70
71  data.Eloss = zeros(numFiles,1);
72
73  data.max_dvdt_off  = zeros(numFiles,1);
74  data.avg_dvdt_off  = zeros(numFiles,1);
75
76  data.max_didt_off  = zeros(numFiles,1);
77  data.avg_didt_off  = zeros(numFiles,1);
78
79  data.t_rise_off  = zeros(numFiles,1);
80  data.t_fall_off  = zeros(numFiles,1);
81  data.t_sw_off  = zeros(numFiles,1);
82  data.t_fall_Vgs_off  = zeros(numFiles,1);
83  data.t_doff = zeros(numFiles,1);
84  data.t_off = zeros(numFiles,1);
85
86  data.Eloss_off = zeros(numFiles,1);
87
88  data.toString = cell(numFiles,1);
89
90  % Start timer
91  tic();
92
93  % Process all waveforms and store results in data structure
94  for i = 1:numFiles
```

```
95
96      if (i > 1)
97          ETA = (numFiles-i+1)*toc()/(i-1);
98          fprintf('[ETA␣%02d:%02d:%02d]␣', floor(ETA/3600), floor(mod(ETA,3600)
                /60), floor(mod(ETA,60)));
99      else
100         fprintf('[ETA␣--:--:--]␣');
101     end;
102
103     fprintf('Processing␣%03d/%d:␣%s\n', i, numFiles, dest{i});
104
105     % Run feature extraction
106     f = isfReport(dest{i});
107
108     % Store output in struct
109     data.id{i} = f.id;
110
111     % Test conditions
112     data.Rgle(i) = sscanf(f.Rgle,'%dR');
113
114     c = sscanf(f.Cgshe,'%d%cF');
115     if (c(2) == 'n')
116         C = c(1)*1e-9;
117     else
118         C = c(1)*1e-12;
119     end;
120     data.Cgshe(i) = C;
121
122     data.targetIL(i) = sscanf(f.targetIL, '%d');
123
124     % DC features
125     data.Vbus(i) = f.Vbus;
126     data.IL(i) = f.IL;
127     data.Vdrive(i) = f.Vdrive;
128
129     % Turn-on features
130     data.max_dvdt(i) = f.max_dvdt;
131     data.avg_dvdt(i) = f.avg_dvdt;
132
133     data.max_didt(i) = f.max_didt;
134     data.avg_didt(i) = f.avg_didt;
135     data.Ipeak(i) = f.Ipeak;
136     data.Ipeaks(i) = f.Ipeaks;
137
138     data.t_rise(i) = f.t_rise;
139     data.t_fall(i) = f.t_fall;
140     data.t_sw(i) = f.t_sw;
141     data.t_rise_Vgs(i) = f.t_rise_Vgs;
142     data.t_don(i) = f.t_don;
143     data.t_on(i) = f.t_on;
144
145     data.Eloss(i) = f.Eloss;
146
147     % Turn-on features
148     data.max_dvdt_off(i) = f.max_dvdt_off;
149     data.avg_dvdt_off(i) = f.avg_dvdt_off;
150
151     data.max_didt_off(i) = f.max_didt_off;
152     data.avg_didt_off(i) = f.avg_didt_off;
```

```
153
154         data.t_rise_off(i) = f.t_rise_off;
155         data.t_fall_off(i) = f.t_fall_off;
156         data.t_sw_off(i) = f.t_sw_off;
157         data.t_fall_Vgs_off(i) = f.t_fall_Vgs_off;
158         data.t_doff(i) = f.t_doff;
159         data.t_off(i) = f.t_off;
160
161         data.Eloss_off(i) = f.Eloss_off;
162
163         % Summary
164         data.toString{i} = f.toString;
165     end;
166
167     % Save output to file
168     save('data.mat', 'data');
169
170     totalTime = toc();
171     fprintf('\nProcessed␣%d␣file(s).␣Total␣elapsed␣time␣%02d:%02d:%02d.\n\n',
            numFiles, floor(totalTime/3600), floor(mod(totalTime,3600)/60), floor(mod(
            totalTime,60)));
172
173     % Join all reports into single PDF file
174     cd('..');
175     joinReports(filename, name);
176     cd('..');
177
178     end
```

D.4.2.3 Report generation: `joinReports.m`

`joinReports.m` is used following post-processing of experimental data to concatenate a set of feature extraction reports (in PDF format) into a single PDF document. The function takes the same arguments as `postProcess.m` as it is intended to be executed based on the same inputs. Individual reports are concatenated in the order they are specified in the input Excel spreadsheet. Parameters and outputs for this implementation are outlined below and the function listing is provided in Figure D.17.

Parameters:

`filename` Filename of the Excel spreadsheet that specifies the set of waveform data to process. Should be the same file passed to `postProcess.m` to generate the feature extraction reports. See the `postProcess.m` documentation for more details on the correct format for this file.

`name` Name of the post-processed dataset. Should be the same name as was passed to `postProcess.m` to generate the feature extraction reports. The function looks in the `out_(name)` directory for the feature extraction reports. The output file will also be placed in this directory, and named `(name).pdf`

Outputs:

`(name).pdf` Single document formed by concatenating switching reports from all waveforms specified in the input Excel spreadsheet, `filename`.

Figure D.17: MATLAB function for concatenation of individual feature extraction reports into a single document.

```
function joinReports(filename, name)

warning('off','all');

% Load Excel file that indexes waveforms
[num,txt,raw] = xlsread(filename);
text = txt(2:end, :);

% Filter for waveforms to be processed
toProcess = num(:,end) == 1;

% Extract test conditions
id = text(toProcess, 2);
Rgle = round(num(toProcess, 1));
Cgshe = text(toProcess, 4);
IL = num(toProcess, 3);

% Initialise cell arrays of waveform files to process
numFiles = size(id,1);
reports = cell(numFiles,1);

% Generate report filenames
for i = 1:numFiles
    reports{i} = sprintf('%s_%dR_%s_%02d_%s.pdf',name,Rgle(i),Cgshe{i},IL(i),
        id{i});
end;

% Change to output directory
cd(sprintf('out_%s', name));

% Join all PDFs
tic();
fprintf('Joining %d PDF report(s)...\n', numFiles);
append_pdfs(sprintf('%s.pdf',name),reports{:});
totalTime = toc();
fprintf('\nProcessed %d file(s). Total elapsed time %02d:%02d:%02d.\n\n',
    numFiles, floor(totalTime/3600), floor(mod(totalTime,3600)/60), floor(mod(
    totalTime,60)));

end
```

D.4.2.4 First derivative calculation: `sgolayfiltd.m`

`sgolayfiltd.m` provides a MATLAB implementation for the calculation of the first derivative of uniformly sampled waveform data through the application of a Savitzky-Golay filter. Parameters and return values for this implementation are outlined below and the function listing is provided in Figure D.18.

Parameters:

- `X` Vector of uniformly sampled data points.
- `N` Savitzky-Golay filter order.
- `F` Savitzky-Golay filter window length. Must be an odd number.
- `dx` The sampling time interval.

Returns:

- `Y` Vector the same length as `X` containing the calculated first derivative of `X` at each sample time.

Figure D.18: MATLAB function for application of Savitzky-Golay filter to calculate first derivative of noisy waveform data.

```
1  function Y = sgolayfiltd(X, N, F, dx)
2
3  [b,g] = sgolay(N,F);   % Calculate S-G coefficients
4
5  HalfWin  = ((F+1)/2) -1;
6
7  for n = (F+1)/2:(size(X,1)-HalfWin),
8    % 1st differential
9    Y(n) =   dot(g(:,2), X(n - HalfWin: n + HalfWin));
10 end
11
12 Y = horzcat(Y,zeros(1, HalfWin));
13
14 Y = Y/dx;          % Turn differential into derivative
```

Appendix E

Parameter sweep result surfaces

Presented in this appendix are the full suite of result surfaces generated from the parameter sweeps conducted to explore the parameter space as detailed in Chapter 3. A brief interpretation and discussion of each set of result surfaces is provided; where additional analysis is merited a reference is included to the corresponding section in the body of the thesis.

The performance metrics used to generate the result surfaces are defined in Section 3.3.3. A guide to interpreting the results surfaces is additionally presented in Section 3.6.2; it is recommended that the reader familiarise themselves with this information before continuing to the presentation of the result surfaces.

E.1 Coarse parameter sweeps

Presented in this section are the result surfaces generated from the coarse parameter sweeps performed according to the methodology outlined in Section 3.6. Each plot presents average $\mathrm{d}i/\mathrm{dt}$, average $\mathrm{d}v/\mathrm{dt}$ and turn-on loss over the specified parameter space.

E.1.1 (R_{gle}, R_{ghe}) parameter space

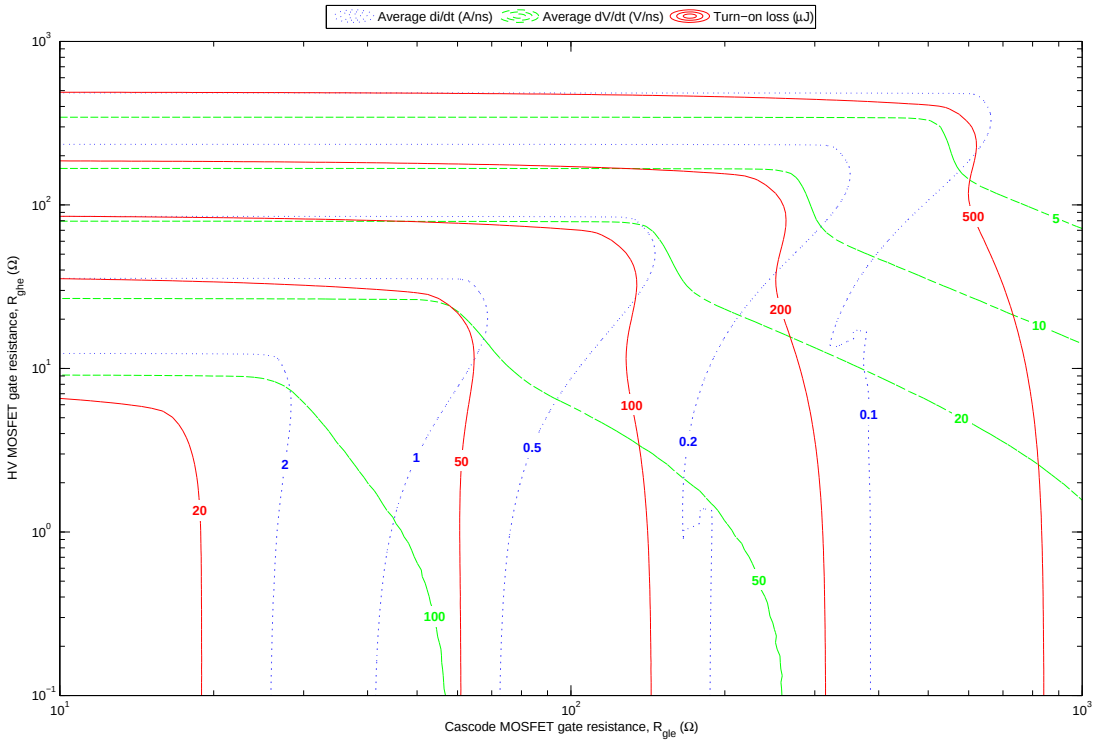


Figure E.1: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (μJ, red) result surfaces plotted over the cascode MOSFET gate resistance, HV MOSFET gate resistance parameter space.

Presented in Figure E.1 are the result surfaces for the parameter space composed of the cascode and high-voltage MOSFET gate resistances (R_{gle}, R_{ghe}).

Firstly, there a distinct characteristic region can be seen in the upper-left-hand corner of this plot. In this region the contours for the three performance metrics run parallel, indicating that independent control of these metrics is not possible in this region of the parameter space. This region is prevalent for high gate resistances of the high-voltage MOSFET, indicating that in this region of the parameter space the gate resistance of the high-voltage MOSFET dominates and largely controls the switching process. This is supported by the fact that the contours run parallel to the R_{gle} axis, indicating the performance metrics are insensitive to changes in the cascode MOSFET gate resistance. We can expect that for large values of high-voltage MOSFET gate resistance, the gate drive characteristics will approach those of a conventional resistor-fed gate drive.

Considering then the other regions of the plot, it can be seen that the contours diverge and intersect throughout the lower-right-hand portions of the plot. For small values of high-voltage MOSFET gate resistance the di/dt (blue) and loss (red) contours run close to vertically, indicating that these performance metrics

are insensitive to the high-voltage MOSFET gate resistance in this region, and are largely controlled by the cascode MOSFET gate resistance.

Over a certain region $\mathrm{d}i/\mathrm{dt}$ and $\mathrm{d}v/\mathrm{dt}$ contours are orthogonal, indicating that independent control of these metrics could be achievable within this parameter space. These results indicate that this parameter space should be investigated further as a potential method of controlling and optimising the switching process. This method of control, however, would re-introduce a large impedance into the gate of the high-voltage MOSFET, potentially limiting some of the performance benefits of the cascode MOSFET. For this reason it was decided to exclude this investigation from the scope of this thesis. Instead, potential future research pathways arising from this finding are presented in Section 5.6.

E.1.2 (R_{gle}, C_{gshe}) parameter space

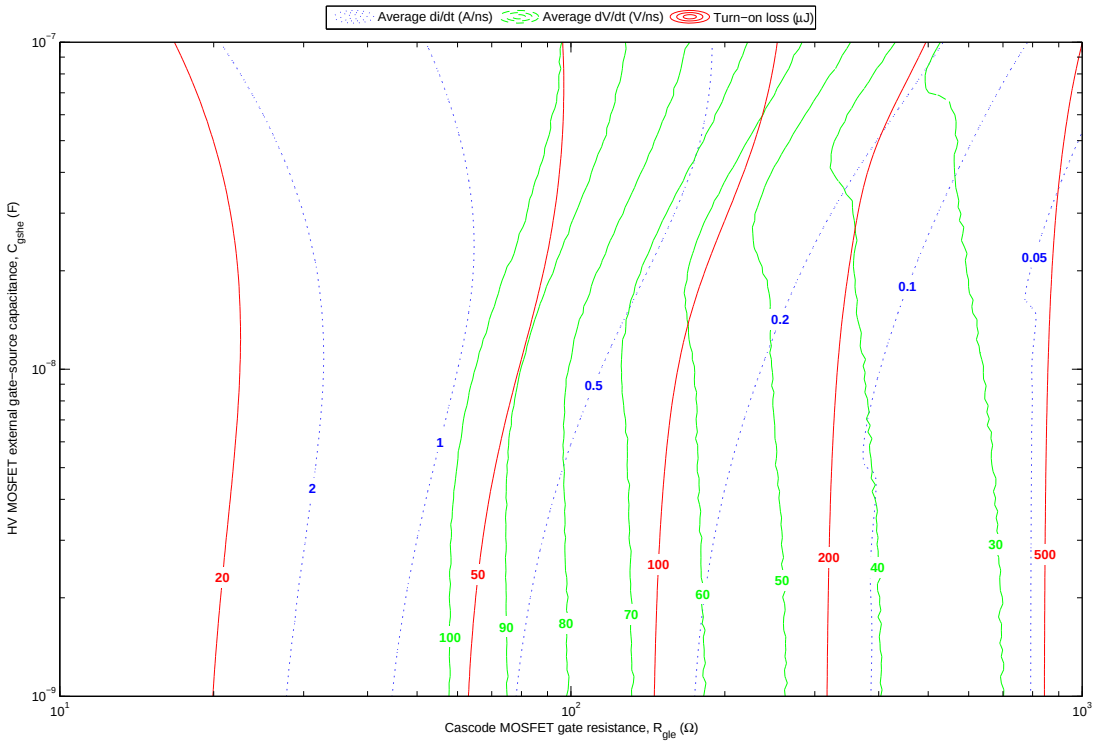


Figure E.2: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, HV MOSFET gate-source capacitance parameter space.

A detailed discussion of the (R_{gle}, C_{gshe}) parameter space is presented in Section 3.7; readers should refer to this section for interpretation and analysis of the results presented in Figure E.2.

E.1.3 (R_{gle}, C_{gsle}) parameter space

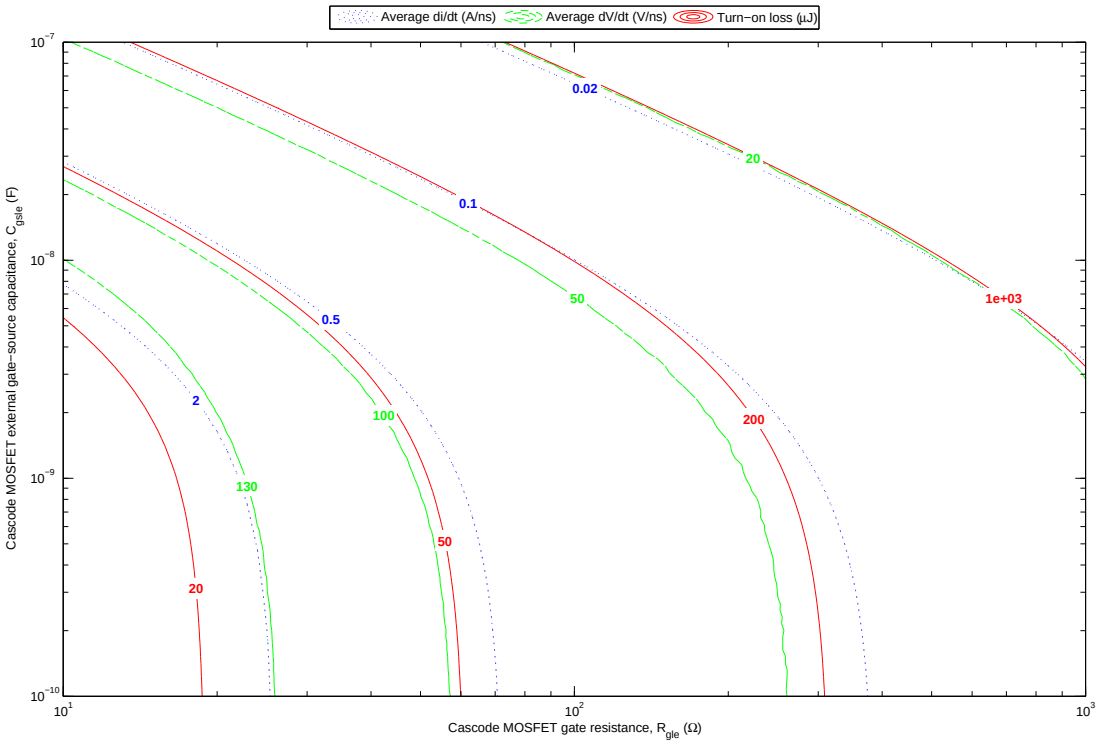


Figure E.3: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, cascode MOSFET gate-source capacitance parameter space.

Presented in Figure E.3 are the result surfaces for the parameter space composed of the cascode MOSFET gate resistance and gate-source capacitance, (R_{gle}, C_{gsle}).

The path of the contours through the parameter space shows that the plotted switching performance metrics are sensitive to changes in both parameters over the parameter space. It can be clearly seen, however, that contours for the three switching performance metrics are effectively parallel over the entire parameter space. This indicates that these metrics are tightly coupled over this parameter space, and therefore, independent control of these performance metrics will not be possible via this parameter space.

E.1.4 (R_{gle}, C_{dshe}) parameter space

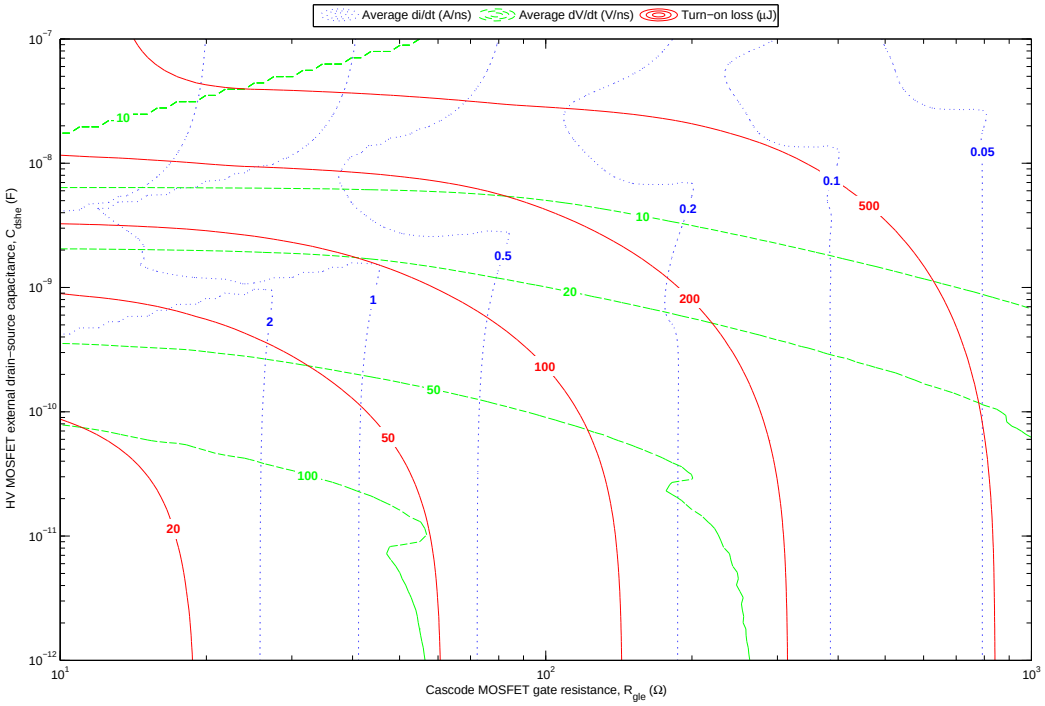


Figure E.4: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, HV MOSFET drain-source capacitance parameter space.

Presented in Figure E.4 are the result surfaces for the parameter space composed of the cascode MOSFET gate resistance and high-voltage MOSFET drain-source capacitance, (R_{gle}, C_{dshe}).

The switching performance metric surfaces exhibit some interesting characteristics over this parameter space. Firstly, note that average dv/dt is sensitive to C_{dshe}, evidenced by the nearly horizontal contours. This result is expected given that increasing the drain-source capacitance should increase the drain-source voltage transition time.

Conversely, average di/dt is largely insensitive to increases in C_{dshe}, evidenced by the vertical contour lines. Again this result is expected, given that the current transition occurs prior to any change in the drain-source voltage.

The average dv/dt and average di/dt contours are largely orthogonal over the parameter space, indicating that it is possible to get independent control of dv/dt and di/dt over this parameter space. Note, however, that this comes at the expense of a substantial increase to the switching losses for increasing C_{dshe}. Again, this result is expected as there is significant energy stored (and then dumped) in any additional drain-source capacitance, given that this capacitance is charged to the full bus voltage each switching cycle.

E.1.5 (R_{gle}, C_{dsle}) parameter space

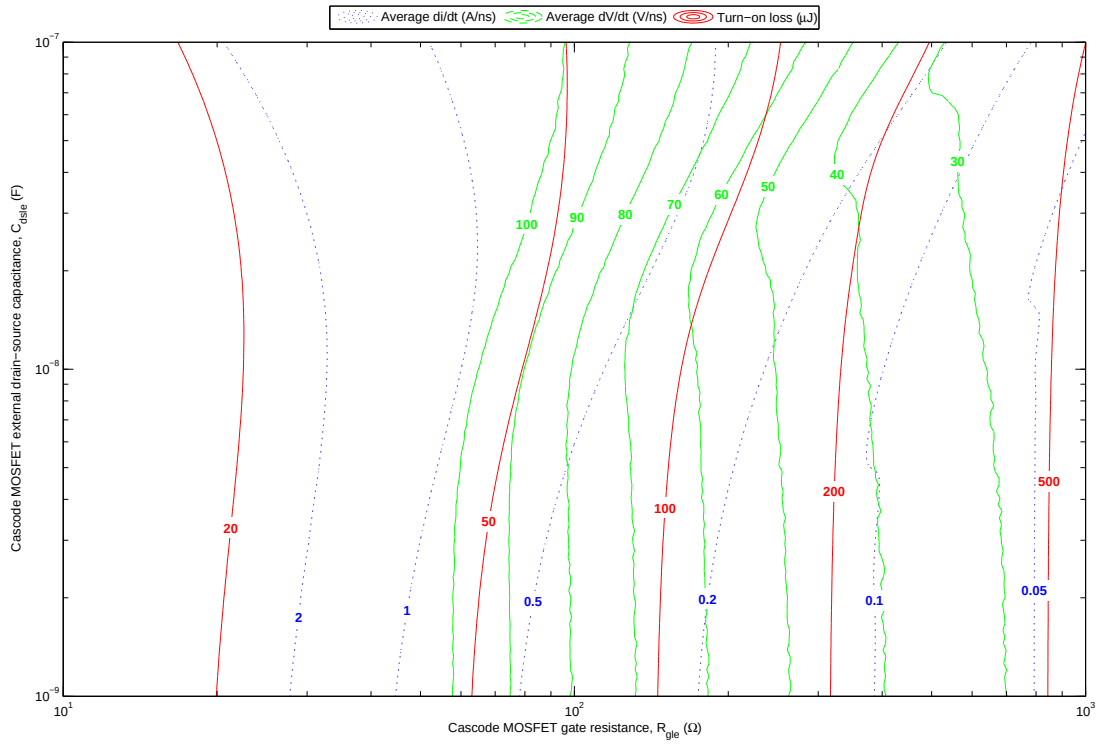


Figure E.5: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, cascode MOSFET drain-source capacitance parameter space.

Firstly compare Figure E.5 with Figure E.2; it can be seen that the result surfaces presented in Figure E.5 are the same as the result surfaces presented in Figure E.2 for the (R_{gle}, C_{gshe}) parameter space.

From inspection of the cascode gate drive topology it can be seen that this is to be expected as charging or discharging, respectively, of the C_{gshe} and C_{dsle} capacitances during turn-on would result in the same additional current being seen by the cascode MOSFET.

A detailed discussion of the (R_{gle}, C_{gshe}) parameter space is presented in Section 3.7; this discussion is applicable to (R_{gle}, C_{dsle}) parameter space, and readers should refer to this section for interpretation and analysis of the results presented in Figure E.5.

E.1.6 (R_{gle}, V_{drh}) parameter space

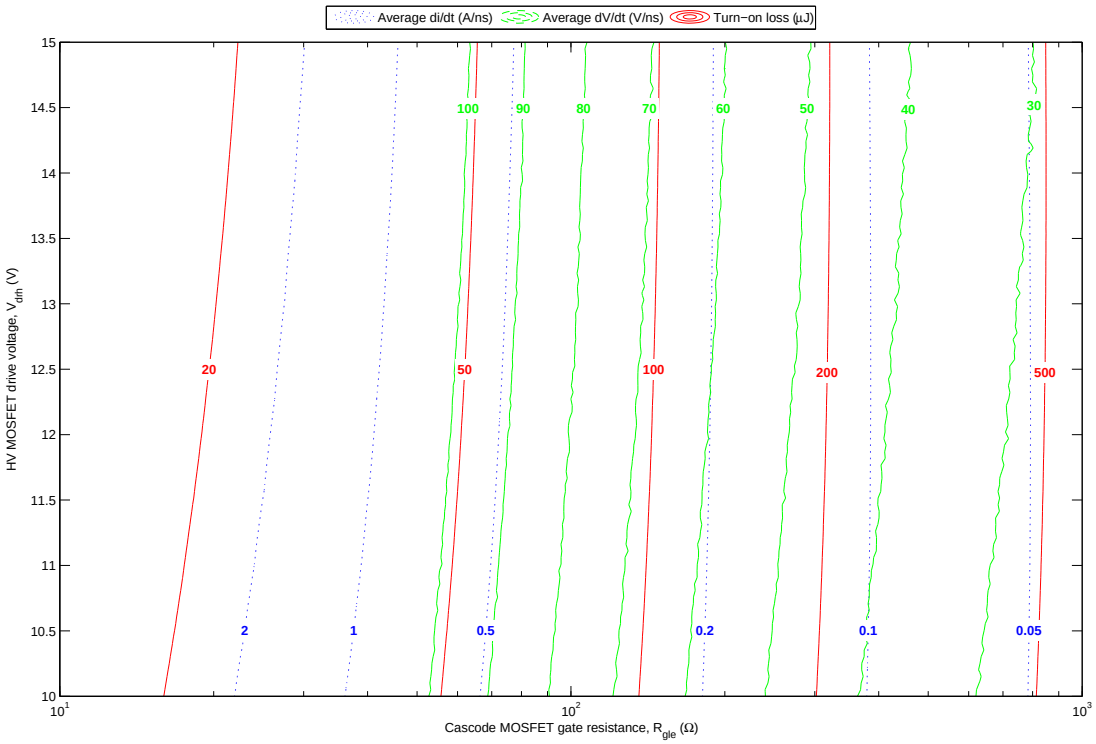


Figure E.6: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, HV MOSFET drive voltage parameter space.

Presented in Figure E.6 are the result surfaces for the parameter space composed of the cascode MOSFET gate resistance and high-voltage MOSFET drive voltage, (R_{gle}, V_{drh}).

The path of the contours through the parameter space shows that the plotted switching performance metrics are largely insensitive to changes in V_{drh}, evidenced by the contours running effectively parallel to the vertical axis. Additionally, contours for the three switching performance metrics are effectively parallel over the entire parameter space. This indicates that these metrics are tightly coupled over this parameter space, and therefore independent control of these performance metrics will not be possible via this parameter space.

E.1.7 (R_{gle}, V_{drl}) parameter space

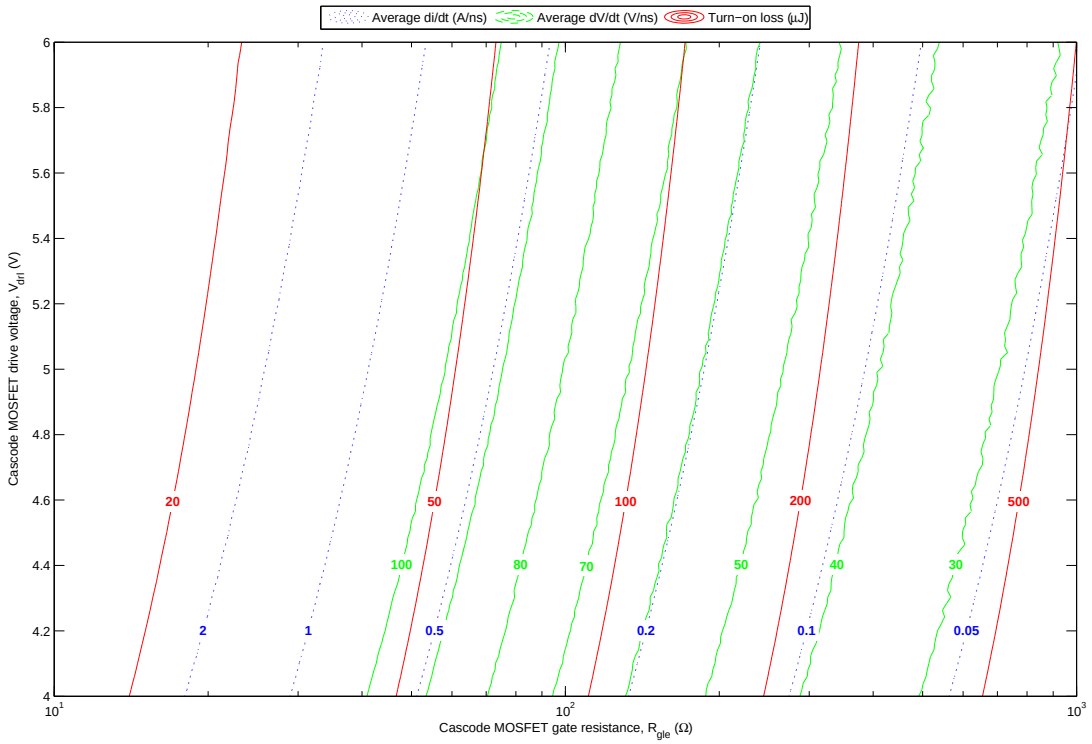


Figure E.7: Average di/dt (A/ns, blue), average dv/dt (V/ns, green) and turn-on loss (µJ, red) result surfaces plotted over the cascode MOSFET gate resistance, cascode MOSFET drive voltage parameter space.

Presented in Figure E.7 are the result surfaces for the parameter space composed of the cascode MOSFET gate resistance and drive voltage, (R_{gle}, V_{drl}).

The path of the contours through the parameter space shows that the plotted switching performance metrics are marginally sensitive to changes in V_{drl}, evidenced by the slight sweep to the right of contours for increasing V_{drl}. However, contours for the three switching performance metrics are effectively parallel over the entire parameter space. This indicates that these metrics are tightly coupled over this parameter space, and therefore independent control of these performance metrics will not be possible via this parameter space.

Appendix F

Experimental results

Presented in this appendix is a summary of the results obtained from the experimental characterisation of the cascode gate drive prototype, as detailed in Chapter 4. An index to the full set of experimental feature extraction reports is provided (attached with the digital copy of this thesis), along with a collection of switching waveforms for different trajectories through the parameter space.

F.1 Index to feature extraction reports

		Cascode MOSFET gate resistance, R_{gle}				
		100 Ω	119 Ω	152 Ω	182 Ω	222 Ω
HV MOSFET gate-source capacitance, C_{gshe}	100 pF					
	1 nF					
	2 nF					
	4 nF					
	10 nF					
	20 nF					
	40 nF					

Table F.1: Index to attached feature extraction reports (click page icon to open).

F.2 Turn-on waveforms: constant C_{gshe}

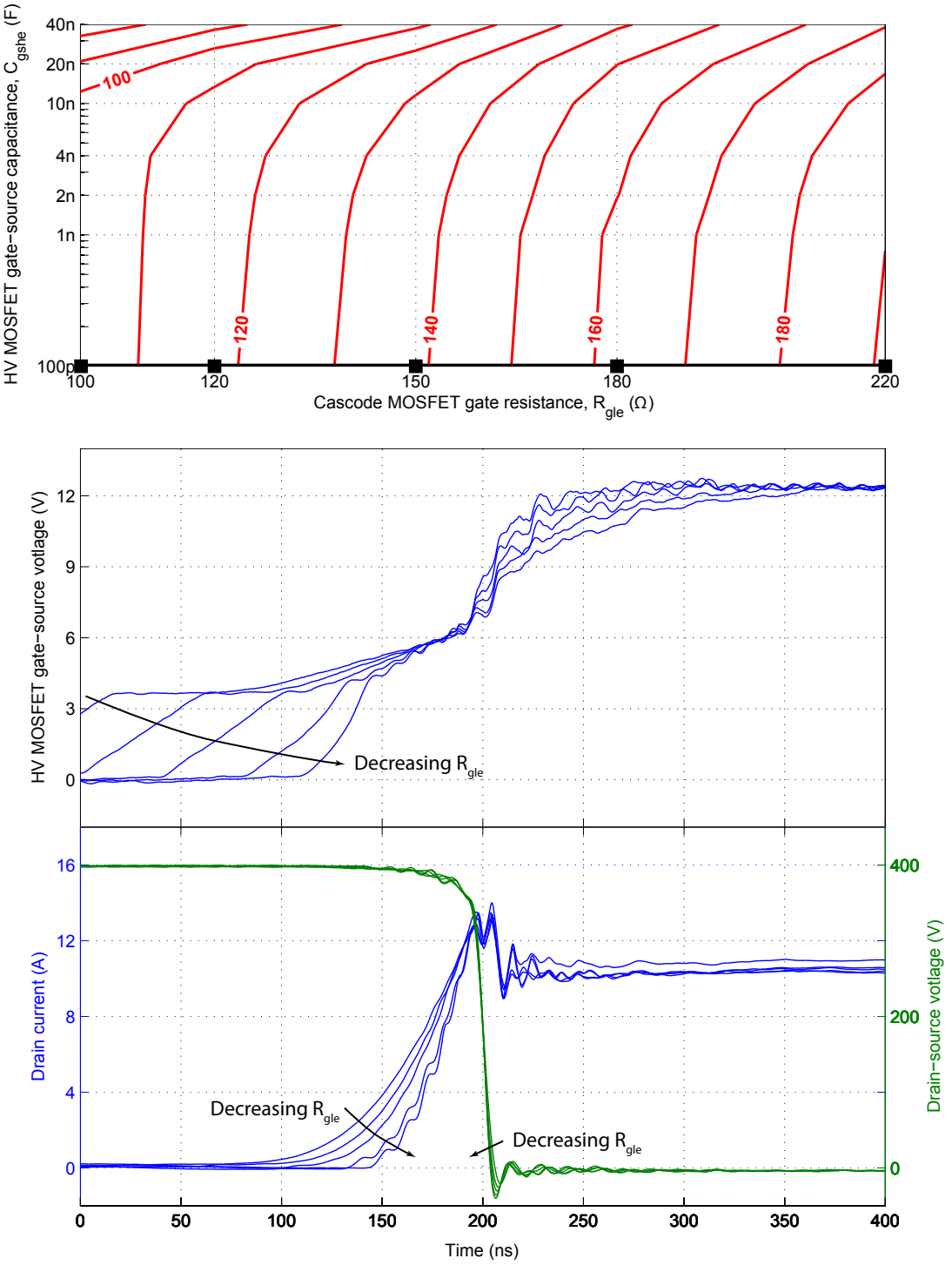


Figure F.1: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 100\,\text{pF}$ and $I_L = 10\,\text{A}$.

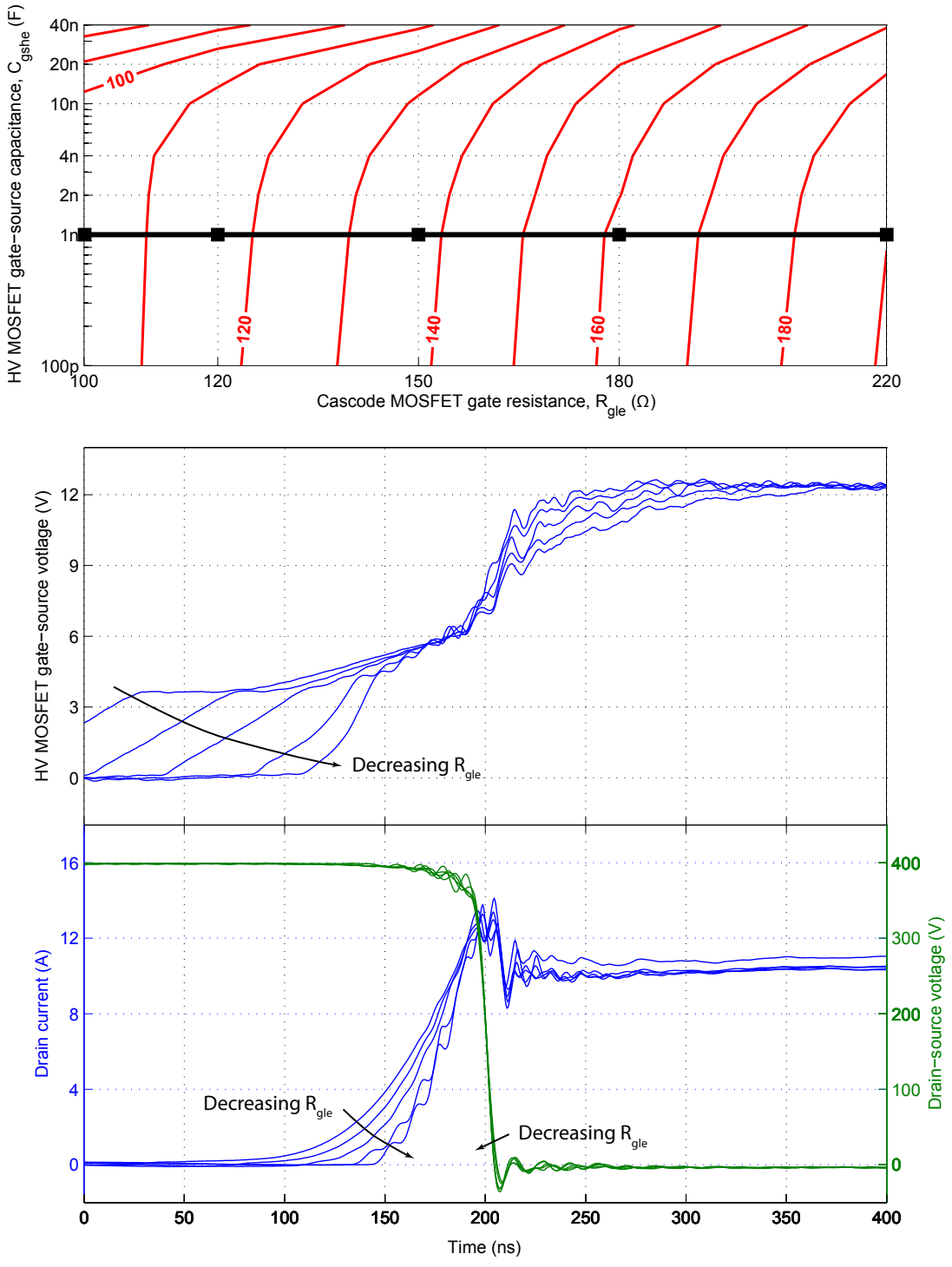


Figure F.2: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 1\,\text{nF}$ and $I_L = 10\,\text{A}$.

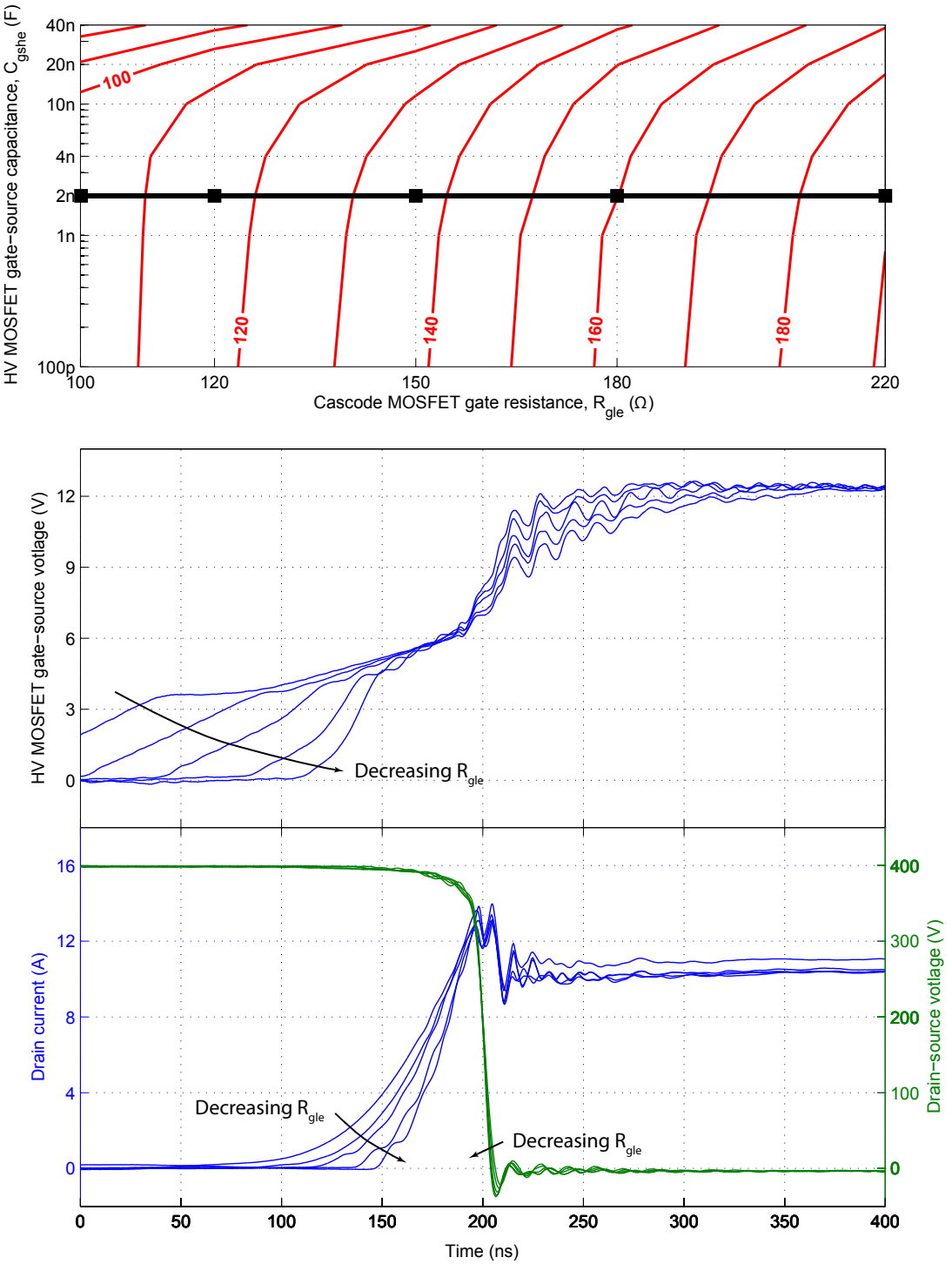


Figure F.3: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 2\,\text{nF}$ and $I_L = 10\,\text{A}$.

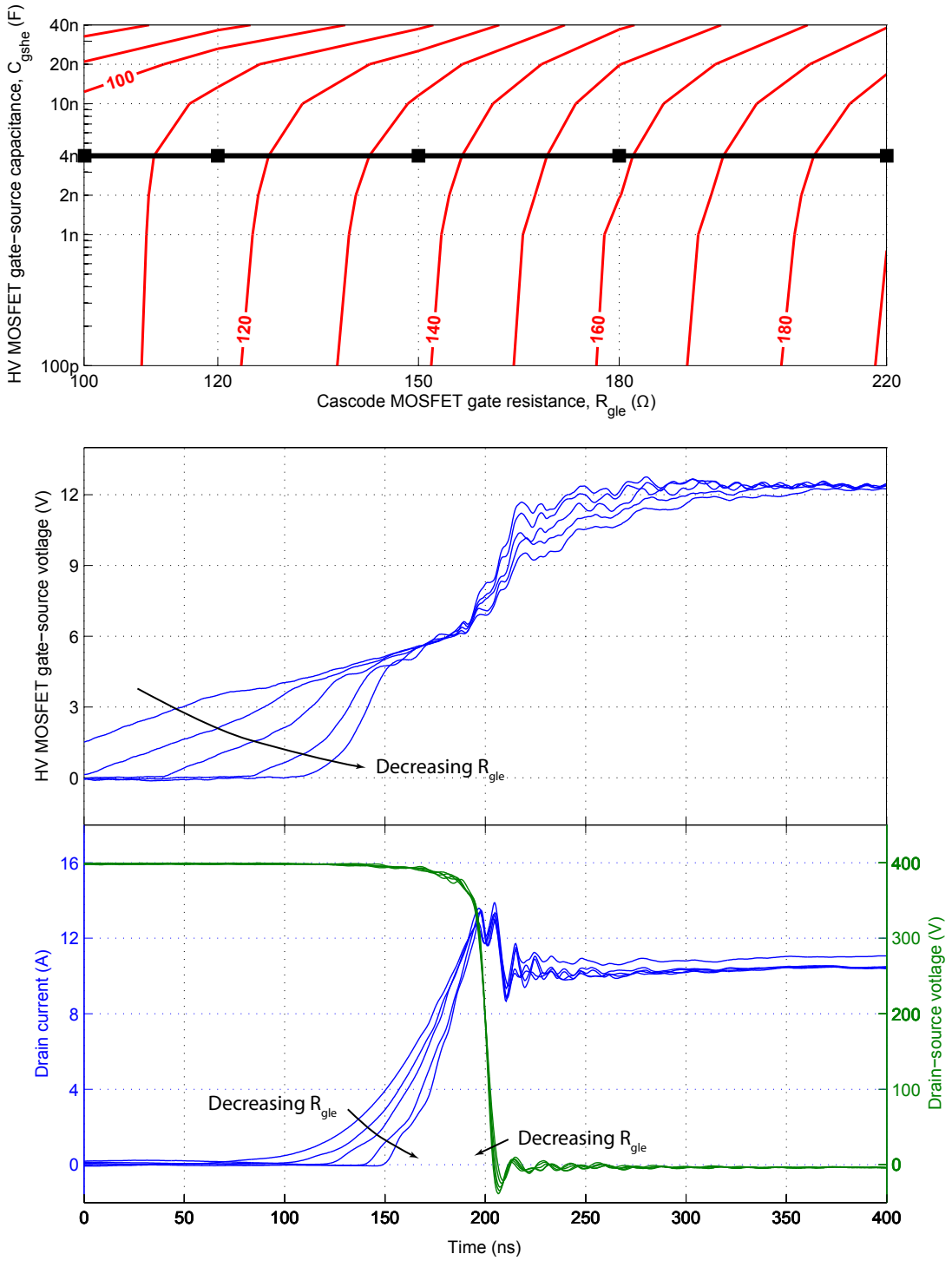


Figure F.4: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 4\,\text{nF}$ and $I_L = 10\,\text{A}$.

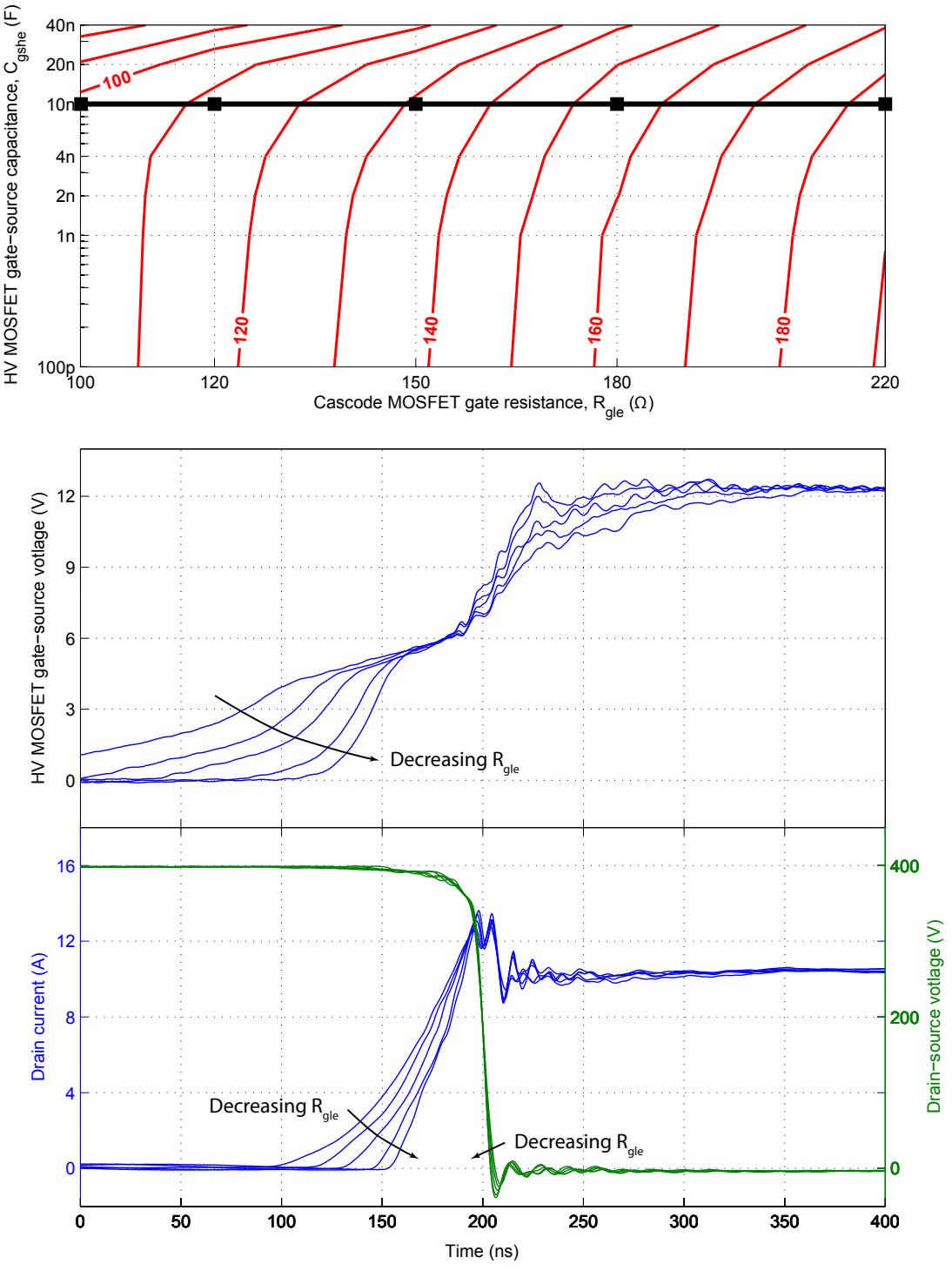


Figure F.5: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 10\,\text{nF}$ and $I_L = 10\,\text{A}$.

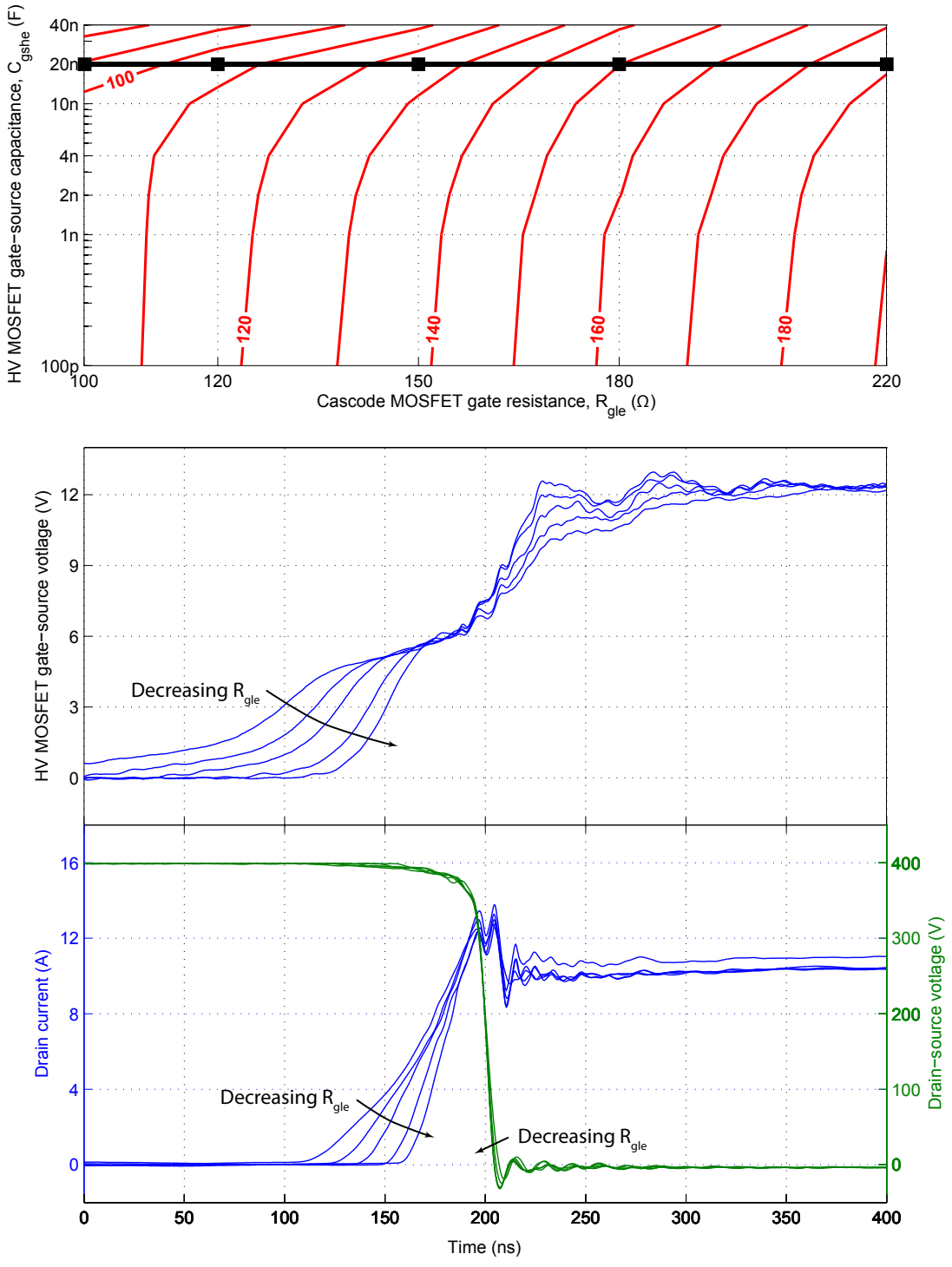


Figure F.6: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 20\,\text{nF}$ and $I_L = 10\,\text{A}$.

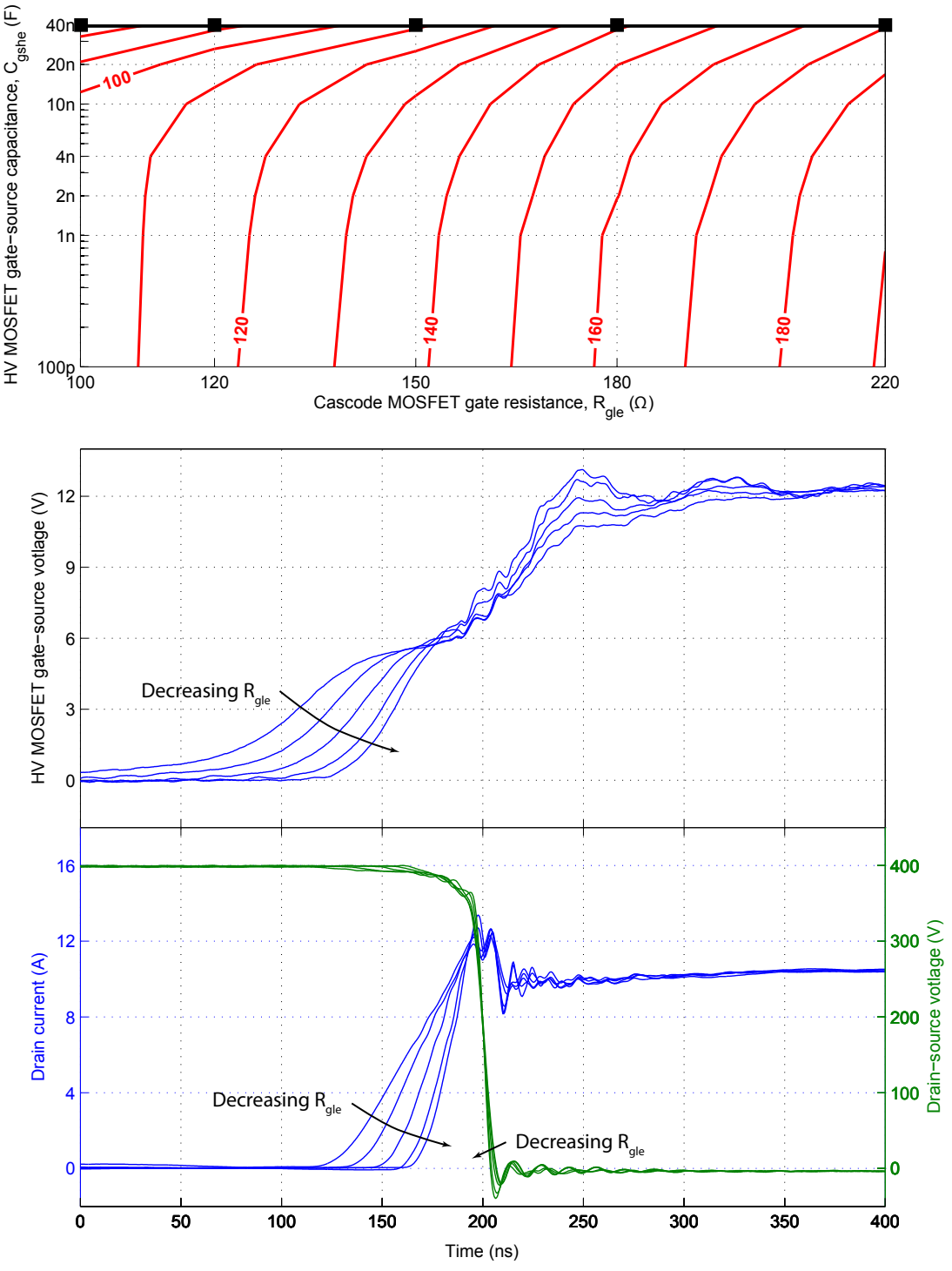


Figure F.7: Experimental turn-on switching waveforms for a constant C_{gshe} trajectory through the experimental parameter space. Cascode MOSFET gate resistance is varied between 100–222 Ω with $C_{gshe} = 40\,\text{nF}$ and $I_L = 10\,\text{A}$.

F.3 Turn-on waveforms: constant R_{gle}

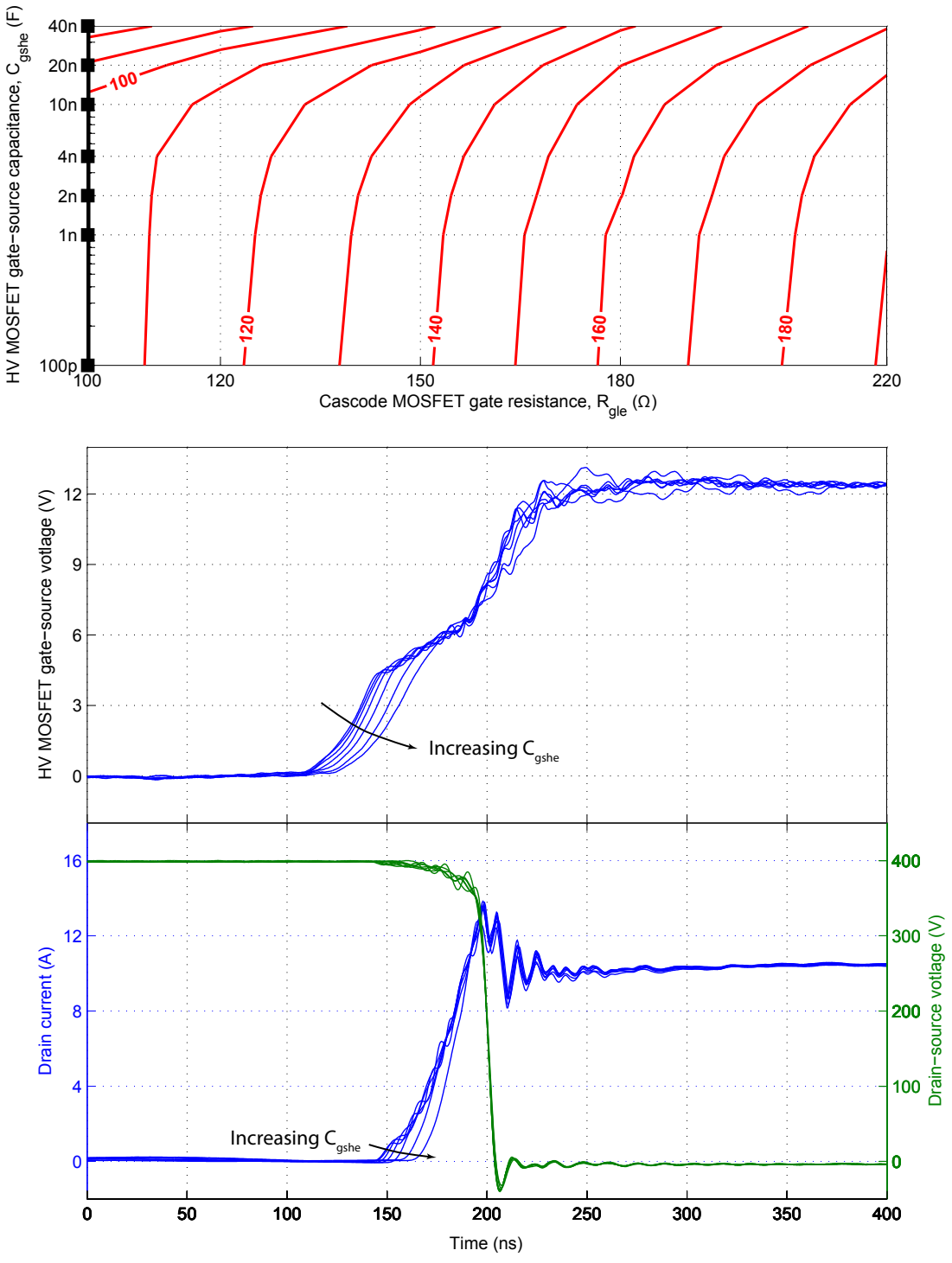


Figure F.8: Experimental turn-on switching waveforms for a constant R_{gle} trajectory through the experimental parameter space. HV MOSFET gate-source capacitance is varied between 100 pF–40 nF with $R_{gle} = 100\,\Omega$ and $I_L = 10\,\text{A}$.

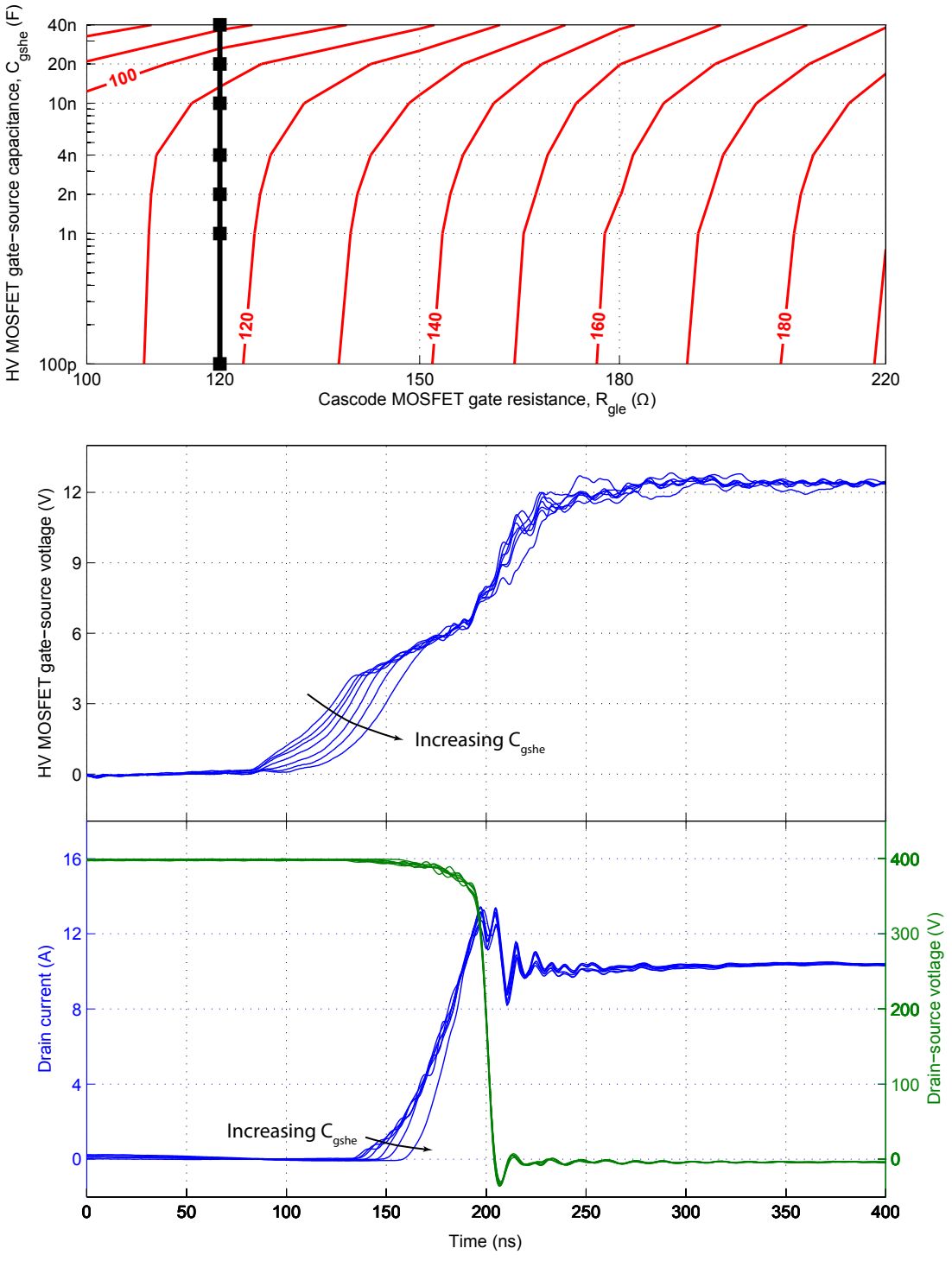


Figure F.9: Experimental turn-on switching waveforms for a constant R_{gle} trajectory through the experimental parameter space. HV MOSFET gate-source capacitance is varied between 100 pF–40 nF with $R_{gle} = 119\,\Omega$ and $I_L = 10\,\text{A}$.

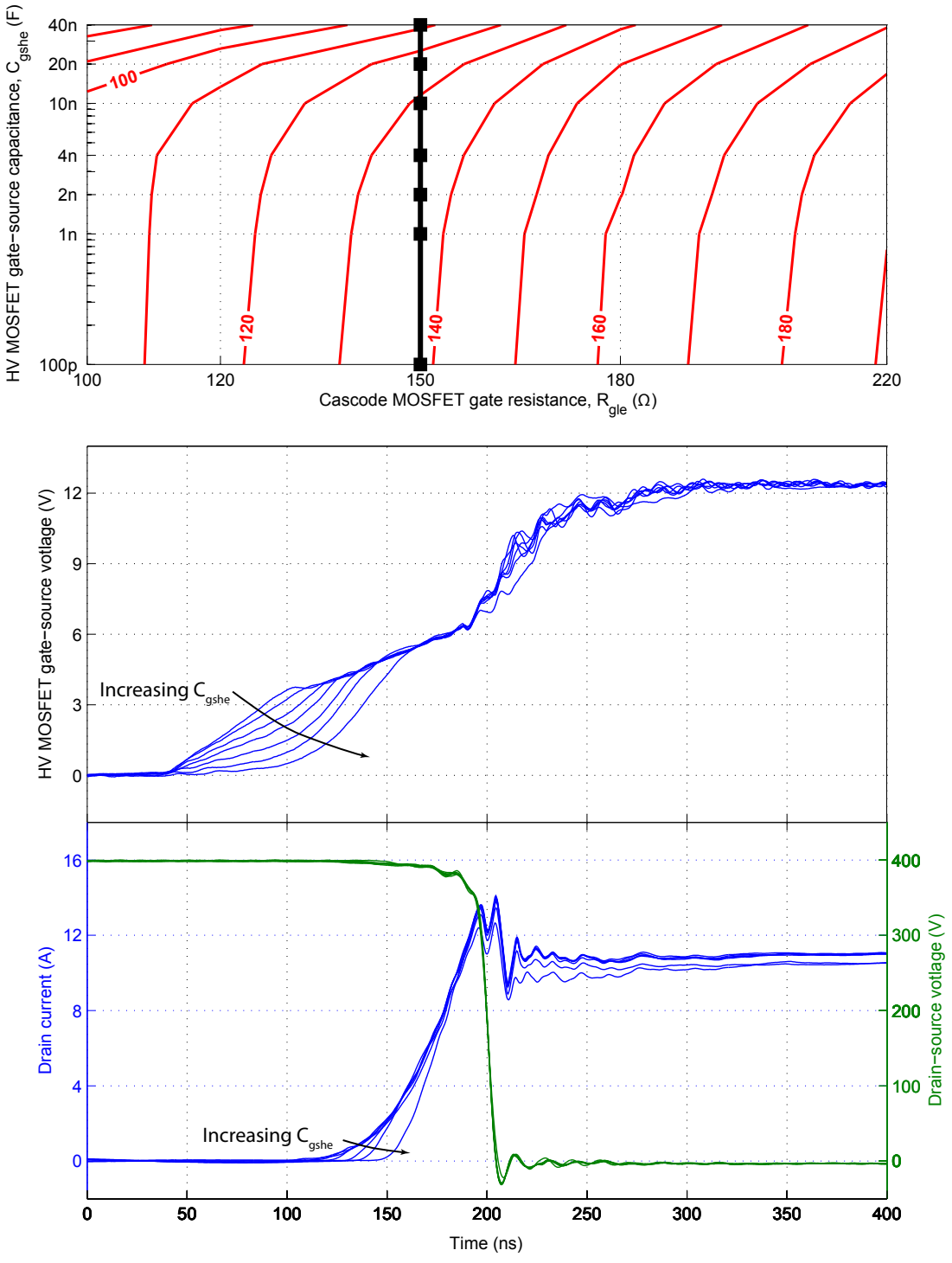


Figure F.10: Experimental turn-on switching waveforms for a constant R_{gle} trajectory through the experimental parameter space. HV MOSFET gate-source capacitance is varied between 100 pF–40 nF with $R_{gle} = 152\,\Omega$ and $I_L = 10\,\text{A}$.

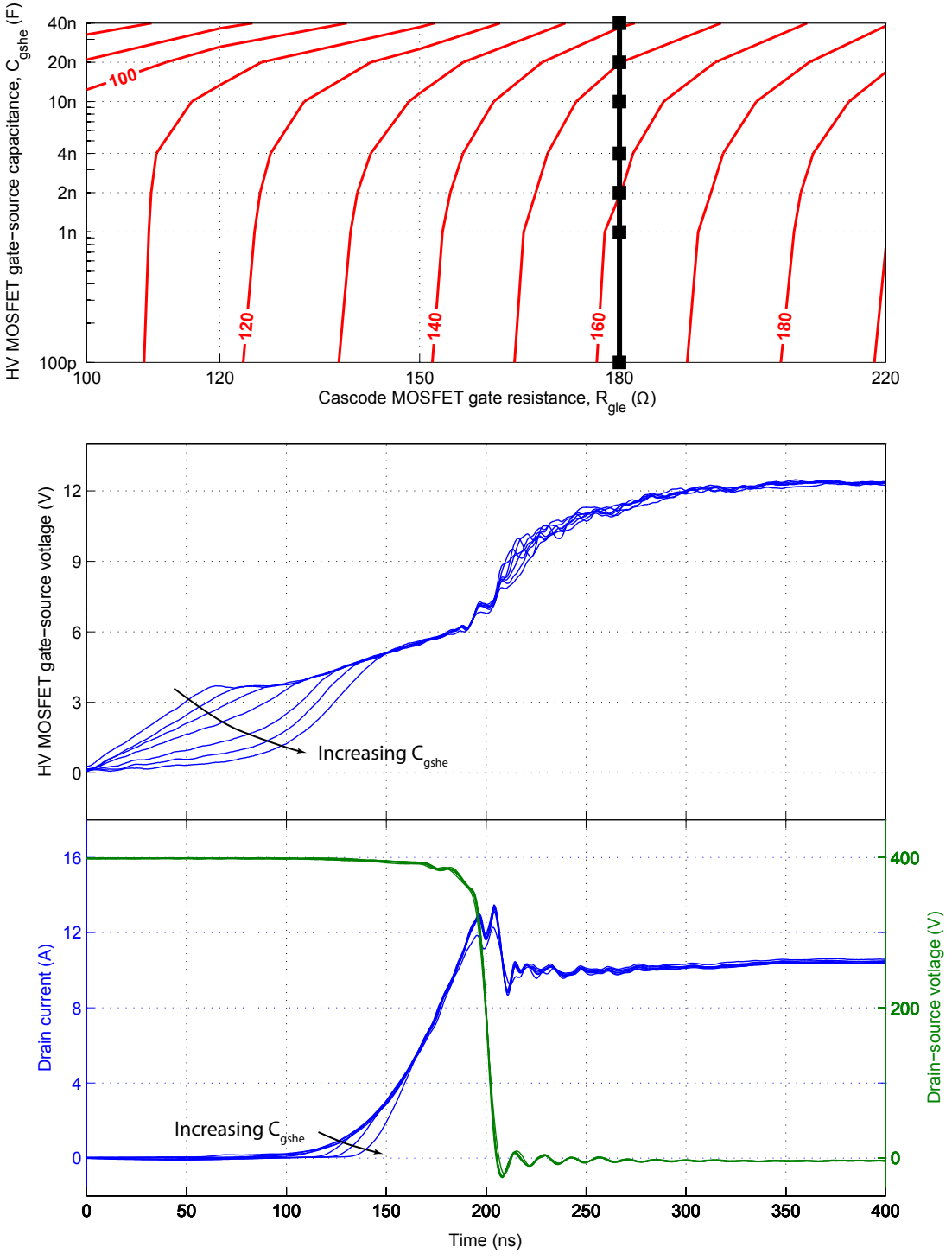


Figure F.11: Experimental turn-on switching waveforms for a constant R_{gle} trajectory through the experimental parameter space. HV MOSFET gate-source capacitance is varied between 100 pF–40 nF with $R_{gle} = 182\,\Omega$ and $I_L = 10\,\text{A}$.

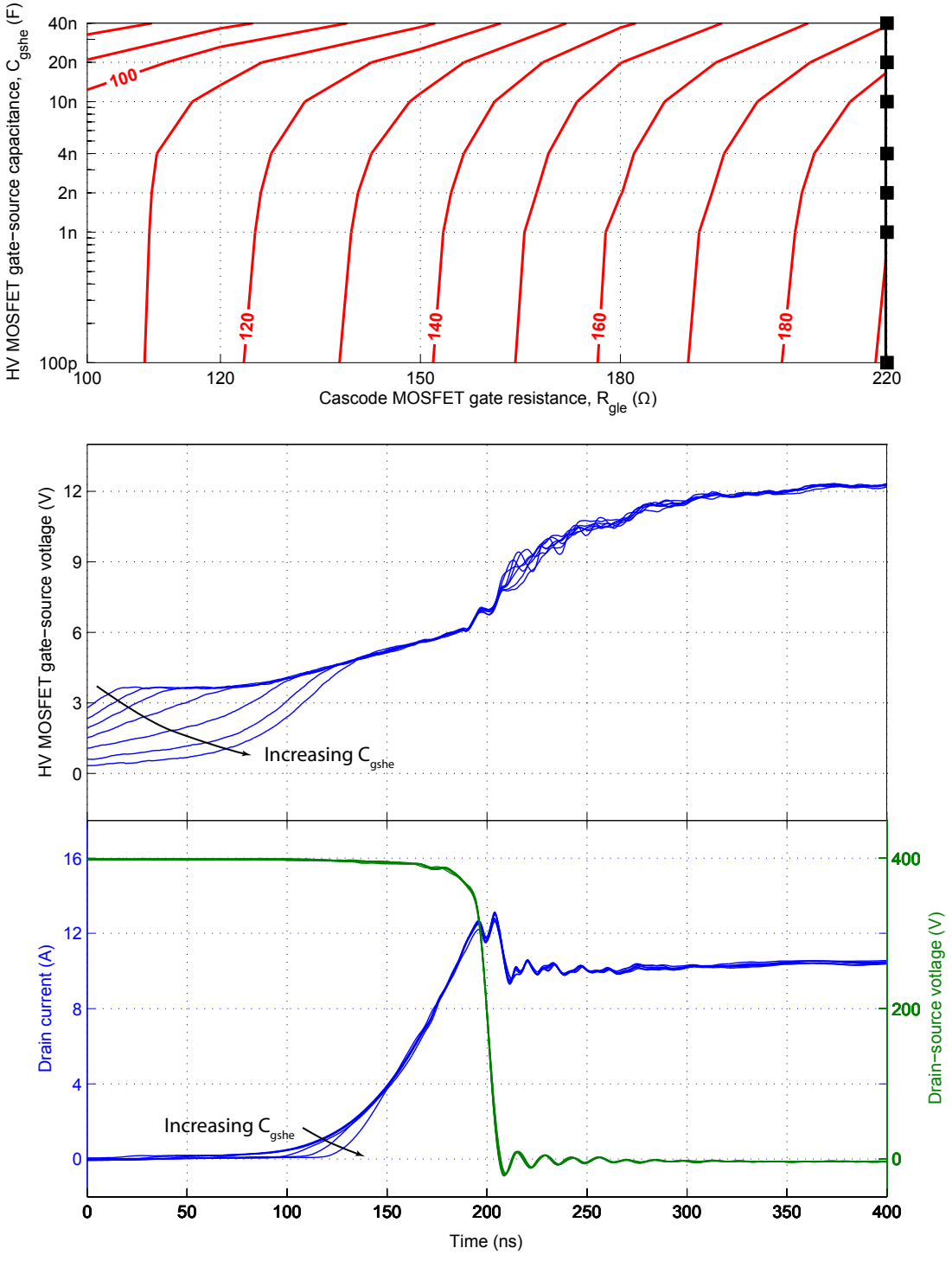


Figure F.12: Experimental turn-on switching waveforms for a constant R_{gle} trajectory through the experimental parameter space. HV MOSFET gate-source capacitance is varied between 100 pF–40 nF with $R_{gle} = 222\,\Omega$ and $I_L = 10\,\text{A}$.

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