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A Novel RF Architecture for Simultaneous Communication, Navigation, and Remote Sensing with Software-Defined Radio

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ABSTRACT

The rapid growth of SmallSat and CubeSat missions at NASA has necessitated a re-evaluation of communication and remote-sensing architectures. Novel designs for CubeSat-sized single-board computers can now include larger Field-Programmable Gate Arrays (FPGAs) and faster System-on-Chip (SoCs) devices. These components substantially improve onboard processing capabilities so that varying subsystems no longer require an independent processor. By replacing individual Radio Frequency (RF) systems with a single software-defined radio (SDR) and processor, mission designers have greater control over reliability, performance, and efficiency. The presented architecture combines individual processing systems into a single design and establishes a modular SDR architecture capable of both remote-sensing and communication applications. This new approach based on a multi-input multi-output (MIMO) SDR features a scalable architecture optimized for Size, Weight, Power, and Cost (SWaP-C), with sufficient noise performance and phase-coherence to enable both remote-sensing and navigation applications, while providing a communication solution for simultaneous S-band and X-band transmission. This SDR design is developed around the NASA CubeSat Card Standard (CS^2) that provides the required modularity through simplified backplane and interchangeable options for multiple radiation-hardened/tolerant processors. This architecture provides missions with a single platform for high-rate communication and a future platform to develop cognitive radio systems.

I. INTRODUCTION

In the past, Radio Frequency (RF) systems have featured independent transmit and receive chains, both of which require individual mixers, filters, and amplifiers to convert the gigahertz signals into the megahertz range for processing. The addition of each component increases mass, volume, and power consumption of the radio. Conventional RF systems perform modulation and demodulation with dedicated hardware, which limits support for features and modulation capabilities. Additionally, they are designed to operate over a fixed bandwidth or support selective pre-established bandwidths using switches [1]. These traditional approaches for space communication are extensively described in the Design and Performance Summary Series issued by the Deep Space Communications and Navigation Systems Center of Excellence (DESCANSO). This series thoroughly details the much larger communication systems used for popular missions including Deep Space 1 [2] and Voyager [3].

However, new space technology developments for communications have been heavily influenced by the rapid growth of SmallSat and CubeSat missions, over the larger, flagship satellite missions that historically exemplified the space industry. This new small-mission emphasis has necessitated a re-evaluation of communication and remote-sensing architectures at NASA. CubeSats are especially demonstrating their viability to perform significant contributions to radio science and communication, however, their platform-limited Size, Weight, and Power (SWaP) restrictions provide new challenges for RF systems [4]. Robust, reliable, high-performance, and efficient radios have been specifically identified as enabling NASA technology priorities for planetary science in both Small Satellite Missions for Planetary Science [5] and Visions and Voyages planetary science decadal [6].

The architecture limitations of large satellites and slow adoption of new technologies throughout the space industry have led to a number of developments in software-defined radio (SDR) technology for space

applications. On the contrary, the commercial world has seen widespread adoption of SDR technology through 4G/5G cellular networks [7], Internet of Things [8], and geoscience research [9]-[10]. NASA has previously identified the advantages that SDR can provide in several sections of the 2015 NASA Technology Roadmap [11], which persists into the 2020 NASA Technology Taxonomy [12]. Specifically, applications for SDR appear as a key topic persisting throughout varying subsections of both TA/TX 5: Communications, Navigation and Orbital Debris Tracking and Characterization Systems and TA/TX 8: Sensors and Instruments.

SDR technology has the ability to bridge the ever-growing gap between these classic RF communication systems and needs of next-generation SmallSat missions. Specifically, advances in Monolithic Microwave Integrated Circuits (MMIC) capabilities have enabled SDR technology that combines frequency synthesis, filters, mixers, amplification, and digital signal processing onto a single integrated circuit (IC) enabling seamless operation into the microwave spectrum while reducing FPGA design complexity as more signal-processing capability is integrated into the SDR. These technological advances in the RF domain are amplified by the order-of-magnitude increases in the processing power of Field-Programmable Gate Arrays (FPGAs) and System-on-Chips (SoCs) [13]. While communication and remote-sensing systems are designed independently of each other, they share many similarities. With properly configured designs, they can be leveraged to reach the end goal of a tightly integrated SmallSat bus and SDR architecture with the capability to support a wide range of mission objectives without loss of functionality.

This paper proposes a novel, integrated, SmallSat bus architecture in conjunction with a design framework for SDR systems. The developed SDR being one embodiment that unifies available SDR technology into a single, reusable design with tightly integrated and reprogrammable capabilities. Significant SWaP savings for SmallSat systems can be realized through the replacement of multiple subsystem processors with one multifunctional processor. This next-generation solution has only been recently enabled by the development of high-performance space processors. The implementation of this architecture enables mission designers to have greater control over reliability, performance, and efficiency while reducing costs and maintaining confidence in the reusability of software and FPGA interfaces. By reconsidering the classic RF architectures, this research represents a necessary technological advancement to enable artificial intelligence (AI) in communication systems, high-performance scalability through standardized backplane interfaces, and resiliency to operate in a wide variety of radiation environments that cannot be supported by current commercial offerings. The new architecture empowers scientists and mission developers to create and launch the next generation of instruments with confidence.

For the organization of the remainder of this paper, Section II provides general background information on SDR systems and supporting architectures. Section III describes the design of this SDR solution along with requirements and considerations for space design. Section IV provides background on FPGA fault mitigation techniques and our future fault-injection and radiation-beam testing methodologies. Finally, Section V provides conclusions.

II. BACKGROUND

This section provides relevant background to current SDR products offered by industry in comparison with the proposed design. Additionally, this section describes integrated bus architectures along with the state-of-the-art processor cards that complement them.

Comparison between Commercial SDR Systems

The large government-funded satellites of the past 50 years have been the primary driver of RF components and radio transceivers until recently. The increased availability of launch vehicles has driven the commercialization of low-Earth orbit (LEO) satellites in the past decade and created a dichotomy in the commercial radio market in terms of reliability, performance, and SWaP-C. With most commercial SmallSats missions operating in a LEO orbit, the probability of a heavy-ion particle strike inducing a single-event latch-up (SEL) can be orders of magnitude less than harsher environments (e.g., geosynchronous orbit). Furthermore, the relatively small total ionizing dose (TID) rate per year in LEO drives industry to design systems with commercial-off-the-shelf (COTS) components that are able to survive shorter mission durations serendipitously. Flight heritage plays a significant role during COTS components selection, and as such, component information is often not released. The limited availability of radiation performance makes direct comparisons challenging. Although multiple definitions for SDR have been developed, in this paper we refer to SDR as a system that supports the configurability of both frequency and modulation across all available outputs.

Table 1. Comparison of Industry SDRs and SmallSat Radios

Name	Frequency	Bandwidth	Resolution	MIMO TX × RX	Radiation *(Estimated)*	Processor	Size / Weight	Peak Power *RF Transmit*
GOMspace NanoCom	70 MHz - 6.0 GHz	56 MHz	TX: 12-bit RX: 12-bit	4 × 4	*20 krad* -	Zynq 7030	9.0 × 6.6 × 3.1 cm^3 350 g	15.1 W 8 dBm
Rincon AstroSDR	70 MHz - 6.0 GHz	56MHz	TX: 12-bit RX: 12-bit	2 × 2	25 – 50 krad 52 MeV·cm^2/mg	Zynq 7045	9.0 × 9.0 × 1.6 cm^3 95 g	30 W 8 dBm
Cesium SDR-1001	300 MHz - 6.0 GHz	100 MHz	TX: 14-bit RX: 16-bit	4 × 4	*20 krad* -	*Not Listed (FPGA)*	8.7 × 5.0 × 1.3 cm^3 100 g	*14.0 W* 7 dBm
SpaceMicro µSDR-C	150 MHz - 6.0 GHz	56 MHz	TX: 12-bit RX: 12-bit	1 × 1	50 / 100 krad 70 MeV·cm^2/mg	Zynq 7020	10.0 × 10.0 × 5.0 cm^3 600 g	15.5 W 8 dBm
JPL Iris V2.1	X-band	TX: 256 kbps RX: 8 kbps		3 × 2	5 krad / 15 krad 37 MeV·cm^2/mg	Virtex 6 (LEON3)	10.0 × 10.0 × 5.6 cm^3 1.2 kg	35 W 36 dBm
IQ SpaceCOM X-Link	X-band S-band (Rx)	TX: 25 Mbps RX: 64 kbps		2 × 2	-	-	9.5 × 6.5 × 2.8 cm^3 200 g	15 W 27 dBm
Vulcan NSR-SDR-S/S	S-band	TX: 2 Mbps RX: 256kbps		1 × 1	-	-	9.2 × 8.2 × 3.4 cm^3 -	15 W 36 dBm
SDL Cadet Plus	S-band	TX: 3.2Mbps RX: 50 kbps		1 × 1	-	-	10.0 × 10.0 × 2.8 cm^3 630 g	8 W 33 dBm

Table 1 provides a survey of popular, currently commercially available SDRs in blue and fixed frequency radios in green with italicized values representing estimates based on datasheet values and comparable components. The integrated radio solutions are provided as a reference to direct the requirements of communication systems in terms of SWaP and data rates. Examination of the SDR specifications shows that each device uses similar or identical hardware. In fact, each SDR in the table is designed around the Analog Devices AD9361 2×2 RF agile transceiver that can operate from 70 MHz to 6 GHz with a 56 MHz tunable channel bandwidth in a BGA package (10×10 mm^2). The Cesium SDR-1001 is designed around the AD9371, an updated version of the AD9361, with multi-gigabit transceivers and higher resolution converters. While the added functionality is promising, no known testing has been performed to show viability in a radiation environment.

While not radiation-hardened by design, the AD9361 has shown superior radiation performance during both TID and heavy-ion testing by the NASA Electronic Parts and Packaging (NEPP) and the German Aerospace Center (DLR). Both test reports showed minimal performance degradation at up to 40 krad, however a decrease in output power was observed when the total dose approached 50 krad [14]-[15]. By reducing the gain of the transmit stages from 62 dB to 50 dB, the effect was mitigated. During heavy-ion and proton testing, SEL and high current events were not observed [16]-[18], however the device did experience infrequent single-event functional interrupts (SEFIs) that were mitigated with a device restart. While not immune to SEFIs, the radiation data indicates the AD9361 is suitable for a wide variety of orbits. However, if the supporting peripheral components (e.g. power supplies, synthesizers, passives) are not selected properly, they will limit the longevity of the SDR.

The developed SDR provides improved radiation performance, fault tolerance, and noise performance to the identified cards in Table 1. Notably, several designs feature all COTS components for both the power and processor architectures. These designs also include components, such as SD cards, that would be unsuitable for upcoming deep-space science missions due to radiation effects. Another observation is that several designs have an integrated FPGA and memory devices (e.g., DDR3 memory) within the card. Unfortunately, including these devices collocated with the SDR will adversely increase system noise and make inefficient use of system power. Finally, the incorporation of switched regulators as the SDR power supply on several of these designs can cause unwanted performance in the internal RF synthesizers if not properly considered.

Advantages of Integrated Bus Architectures

One of the most apparent disadvantages of the commercial SDR systems is that several designs integrate additional processing components, such as the FPGA and DDR memory, onboard with the RF transceiver. By moving the processing off-card, the SDR architecture can be optimized for MIMO configurations, performance, reliability, and

functionality without sacrificing power efficiency. 1U CubeSat Single-Board Computers (SBCs) can provide substantial computing resources that can be used to service multiple functions within an integrated CubeSat architecture.

The new NASA Goddard Space Flight Center (GSFC) Modular Architecture for Resilient Extensible SmallSats (MARES) is a highly reliable, yet flexible architecture that supports multiple-sized configurations of the electronic slices [19]. The MARES design provides an entire bus architecture, but subsets of the design can be requisitioned for individual mission needs. A cornerstone of the design is the large Xilinx Kintex UltraScale FPGA device that performs the processing for the communication and navigation elements of the system. Figure 1 shows the NASA GSFC MARES SmallSat with a low-voltage power card, command & data handling (C&DH) processor, instrument processor, GPS, and a hybrid backplane to provide both flight-like system integration and testing functionality.

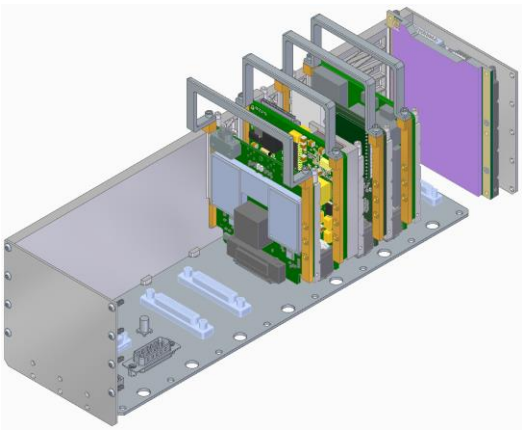

Figure 1: MARES Integrated Bus Architecture

Processor Architectures

Establishing separation of the RF transceiver with processing components allows the design to remain relatively hardware-agnostic, as long as the accompanying hardware can support the baseline FPGA interface. FPGA resources for this design approach are described in Section IV. Decoupling the processing component allows the SDR to operate independently while enabling spacecraft designers to fine-tune the accompanying SBC to best meet mission requirements. This section describes three SBCs with varying capabilities and features that can support the SDR designs through a backplane connector approach; however, other similar industry processors are compatible through the FMC interface.

One next-generation SBC that supports this architecture is the SpaceCube v3.0 Mini processor card described in [20]. This design features the resource-abundant Kintex UltraScale KU060 FPGA in a 1U CubeSat form-factor with integrated fault-tolerance features. Additionally, for missions requiring the expansive FPGA fabric, it provides significantly more resources than the previously, broadly adopted Xilinx Virtex-5, but also supports the latest advancements in tools and FPGA productivity. This simplifies integration of some of the most novel Xilinx designs such as the Deep Learning Processor Unit (DPU).

Another design that can complement the developed SDR is the SpaceCube Mini-Z [20]. This design is an evolution of the popular CSP space computer from the Nation Science Foundation (NSF) Center for Space, High-Performance, and Resilient Computing (SHREC), which features a Xilinx Zynq-7020 SoC. This processor is included on several NASA GSFC CubeSats, multiple International Space Station (ISS) missions, and has extensive flight heritage. Finally, another supporting design is the SSP space computer from SHREC. This processor card features a user-selectable Zynq-7000 SoC (Xilinx Zynq 7030, 7035, or 7045) with FPGA-interfaced DDR3 memory, multi-gigabit transceivers (MGTs), and other improvements over CSPv1.

SDR Architecture Challenges for Communication, Navigation and Remote-Sensing

The development of any system that encompasses multiple fields requires a deep understanding of each field and the associated design parameters to arrive at an optimal solution. Typically, a trade study would be used to determine the optimal design parameters. But determining specific weights for each parameter is a nontrivial task, especially when the design is not for a specific mission but for a generalized architecture across multiple fields. As such, the key parameters were identified below, and their impact will be discussed throughout this section as they pertain to developing the SDR architecture for communication, remote sensing, and navigation.

- Radiation and Reliability
- Multi-Input Multi-Output (MIMO)
- Frequency
- Phase Coherence
- ADC/DAC Resolution
- RF Connectivity

As previously noted, the radiation requirements for a mission can vary drastically, and developing a system to operate in every environment will prohibitively increase cost. Since the communication and remote - sensing systems are essential to the SmallSat

functionality, component selection is of utmost importance. The use of package-equivalent components or selective population allows for multiple radiation and cost profiles to be developed for a given mission architecture, but care must be taken to ensure that this does not degrade performance. Since most SmallSats and CubeSat missions are designed for an operational period between 1 and 5 years, full radiation-hardness is not a requirement. Based on analysis of common mission orbits [21] selecting components with at least TID rating around 50 krad and SEL greater than 50 MeV·cm^2/mg provides sufficient coverage from LEO to lunar missions (assuming appropriate shielding and mass margin).

Recent publications, e.g. [22], have begun to explore the capabilities of AI and communication systems that may require in-flight reconfiguration of the onboard frequency synthesizers and multi-channel MIMO architectures to fully realize the benefits of AI. Given the size constraints of SmallSats, a 4×4 MIMO architecture provides scalable functionality. Additionally, the MIMO architecture enables inter-satellite communication that would ideally support S-band, X-band, and Ka-band capabilities to optimize telemetry links based on environment.

Specific to remote sensing applications, high-resolution ADCs and DACs greater than 14-bit should be included to provide scientists with a sufficient measurement accuracy. The resolution increase is significant because satellite communication systems rarely require the higher resolutions that unnecessarily increases data throughput and processing requirements. The adoption of MGTs in space processors has begun to enable the high throughput capabilities of future SDRs. Lastly, since many remote-sensing applications require coherence for processing, a topology should be chosen where a common oscillator with phase coherence drives each SDR.

III. APPROACH

The primary goal of this research is to create a reliable and resilient SDR platform for communication, remote sensing, and navigation. The foundation of this approach is centered around the SpaceCube approach [13], developed by the Embedded Processing Group of the Science Data Processing branch at NASA GSFC, and also adopted by the NSF SHREC Center in the design of the SSP. This system level approach combines radiation-hardened and COTS components with fault-tolerant mitigation to provide a reliable and reconfigurable solution that can meet the high-performance needs of next-generation missions.

Hybrid SDR Architecture

While a number of high-performance SDR solutions exist that provide higher resolution and wider bandwidths, radiation performance is essential to operation across a wide number of missions, as described in the Design and Performance Summary Series [3]. As a result, the Analog Devices AD9361 RF Agile Transceiver was selected as the ideal solution based on its radiation performance, internal wide-band synthesizers, and multi-chip synchronization capabilities. In addition to the 2×2 MIMO architecture, the AD9361 provides multiple sub-channels for each transmit and receive channel that are used in a loopback configuration to enable phase coherence through signal processing instead of the external synthesizer. Figure 2 shows a PCB CAD model of the proposed 1U SDR.

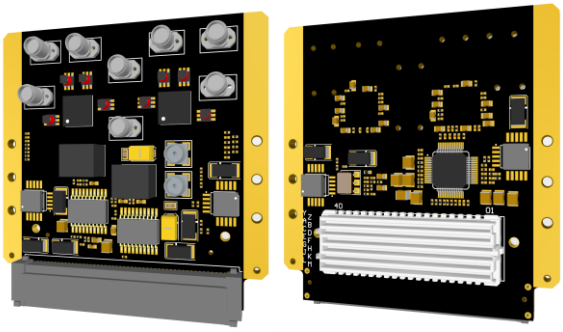

Figure 2: SDR PCB with Primary on Left and Secondary on Right

The processor communicates with each AD9361 through a dual-port 12-bit low-voltage differential signaling (LVDS) interface that provides the highest data rates between the processor and the SDR. Each AD9361 requires 18 LVDS pairs that presents a significant barrier to incorporating multiple SDRs because the large quantity of LVDS consumes much of the processors IO. As such, the design includes two AD9361 SDRs with independent control of each to enable a 4×4 MIMO architecture. Selective-population resistors on each LVDS pair presents mission designers a cold spare configuration without allocating a large quantity of LVDS from the baseband processor. Additionally, the MIMO architecture contains a large number of RF inputs and outputs making design considerations more difficult. Vertical board mounted SMA connectors were selected to provide a strong connection mount for vibration testing, and full functionality with the FMC.

Baseband and RF Synthesizer

The reusability of an SDR architecture depends upon the hardware's ability to both easily generate and reconfigure a desired RF frequency. Developments in MMIC capabilities over the past decade have enabled

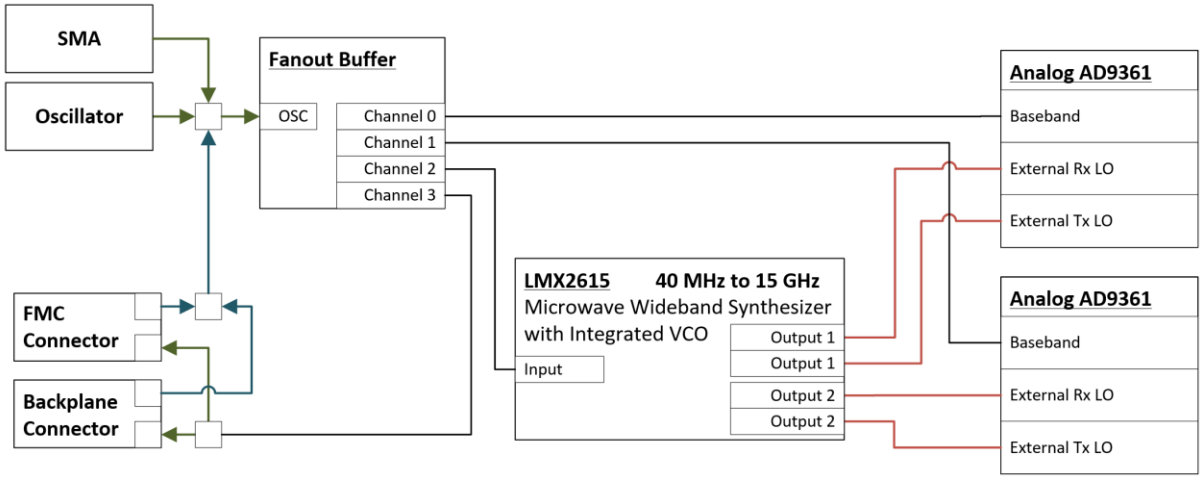

Figure 3: Internal VCO Capabilities

this functionality in silicon, which have reduced component counts, increased power efficiency, and minimized the effects of PCB interconnect mismatch and loss. The baseband on the AD9361 operates from 715 MHz to 1.43 GHz that can be a constraint for remote sensing applications, but is acceptable for communication. Internal synthesizers generate the local oscillator (LO) frequency between 6 GHz and 12 GHz. Two identical integrated fractional-N wideband synthesizers inside the AD9361 feed the LO mixer stage of the transmit and receive channels separately, representing one limitation of the selected architecture. However, the phase difference between the internal synthesizers is deterministic and can be calculated if an external transmit-to-receive loopback exists. The internal synthesizers can be bypassed if an external synthesizer drives each transmit and receive LO pin with a frequency between 140 MHz and 8 GHz. While an external LO limits the SDR's frequency range, the additional component enables phase coherence between all transmit and receive channels without additional processing. An external 40 MHz fixed frequency oscillator provides optimal noise performance for the internal synthesizers. The clock is distributed with a low jitter phase coherent fanout buffer. Figure 1Figure 3 shows the internal and external synthesizer configurations for the baseband and RF subsystems.

The Texas Instruments LMX2615-SP is a radiation-hardened wideband synthesizer with dual outputs that is capable of generating any frequency between 40 MHz and 15.2 GHz. The LMX2615 operates from a single 3.3V supply, has phase synchronization between the two outputs, and is rated to 100 krad and 120 MeV·cm^2/mg.

Power System

The design of an RF power system is nontrivial, and requires careful design to ensure noise and transients are not coupled into the SDR and translated into the RF. The design is further complicated by the integrated nature of the SDR that can consume hundreds of milliamps across many voltage rails. If care is not taken, the design can lead to coupling between the transmitter and receiver channels, producing unintended changes in LO frequencies, and harmonic spurious emissions. Under the best circumstances, this produces a severely constrained SDR with suboptimal noise performance, and at worst, leads to illegal transmission in adjacent frequencies that could impact satellite navigation and communication networks.

Based on commercially available bus architectures [23], we concluded that the low-voltage power card (LVPC) on many SmallSat and CubeSat bus architectures provide isolated 12V, 5V, and 3.3V rails to the system. Therefore, we assume these voltage rails are available in our integrated bus architecture. Typically, linear regulators are used to provide a noise-free voltage supply but are unable to provide a level of efficient regulation that is critical to an integrated bus architecture. Point-of-load (POL) switched converters are capable of providing very high efficiencies up to 90% [24] that are required for the large downstream currents produced by the C&DH system and instrument processors. However, the high efficiency of the buck converter is obtained by duty cycling the input voltage between 100 kHz and 2 MHz that can produce significant noise and hinders RF performance.

As a result, the bus architecture in its entirety must be considered when designing the power system since

placing too many cards on a single voltage rail can have unintended consequences, such as LVPC converter stability issues and large in-rush current. The developed power system design assumes instruments are primarily powered through the 12V converter, C&DH and instrument processors are primarily powered through the 5V converter, and the SDR is powered through the 3.3V regulator. Since the linear regulator efficiency is proportional to the difference between the input and output voltages, significant power can be wasted during regulation if not properly designed. Figure 4 shows the developed power system architecture for the SDR.

For optimal efficiency, intermediate PoL converter stages are placed between the backplane power supplies and the low-dropout (LDO) linear regulators that provide power to both the SDR and external synthesizer IC. Furthermore, each AD9361 has separate LDO regulators to power the RF and digital domains to minimize the impact of transients on the internal SDR synthesizer performance. The external wideband synthesizer requires 3.3V that is available from the backplane, however the external synthesizer is powered through an intermediate PoL converter and dedicated LDO from the 5V backplane supply to produce a clean uncoupled RF output. The selection of regulators was based primarily on the trade-offs between radiation performance, ripple rejection (PSRR), and output noise.

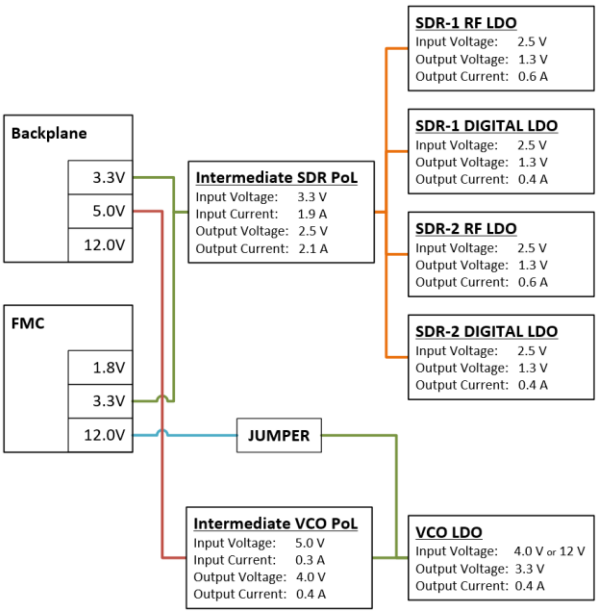

Figure 4: SDR Power System Architecture

The Texas Instruments TPS7A4501-SP LDO is rated to 100 krad and 99.2 MeV·cm^2/mg that can supply 1.5 A to a regulated output as low as 1.21V with a worst-case dropout of 750 mV. The LDO provides an excellent low-noise output of 50 µV and 65 dB ripple rejection at 10 kHz. To enable cost-constrained LEO missions where radiation requirements are not as stringent, the Texas Instruments TPS73801-SEP provides a radiation-tolerant regulator with nearly identical electrical performance to the TPS7A4501-SP. The TPS73801-SEP is rated for up to 20 krad and 45 MeV·cm^2/mg. While the radiation tolerant regulator is not directly package compatible, a selective population footprint was created to minimize PCB area.

The Texas Instruments TPS50601A-SP PoL synchronous buck converter is rated to 100 krad and 75 MeV·cm^2/mg that can supply 6A currents from a 3-7V input. The integrated MOSFETs have been sized to optimize efficiency for lower duty cycle applications. Given the high input-to-output voltage ratio required for optimal LDO efficiency, the intermediate PoL converter stage will have to operate at a slightly lower efficiency because of the higher $R_{DS(ON)}$ of the high-side integrated MOSFET. While alternative topologies can further increase efficiency, more complicated solutions will require a greater footprint.

The internal MOSFETS can be configured to switch between 100 kHz and 1 MHz. The overlap in the frequency dependent PSRR between the LDO and SDR is essential to the selection of the switching frequency of the intermediate PoL regulation stage to ensure unintended ripple harmonics are effectively attenuated by the LDO, and filtered by PCB decoupling. While the efficiency of synchronous buck converters is strongly dependent on topology and component selection, a lower switching frequency around 100 kHz has classically produced higher efficiency in silicon converters [25]. Considering the reduced PSRR of the AD9361 around 100 kHz, the TPS50601A is configured to operate at 300 kHz, providing a balance between LDO ripple rejection, transient response, inductor package size, and capacitor decoupling.

Connector Options and PCB Considerations

The SDR architecture was designed around the NASA's CubeSat Card Standard, also known as CS^2, which is managed by the Embedded Processing Group of the Science Data Processing Branch at NASA GSFC. The CS^2 standard establishes a 1U (10×10 cm^2) PCB with a variety connector configurations and mounting options to address NASA-specific concerns not met by existing standards. The standard is based on a backplane architecture that can be easily expanded for mission-specific needs, and is based on the Samtec SEAF-RA connector available in both 200-pin and 400-pin variants with flight heritage across multiple missions [26]-[27]. The 200-pin variant provides sufficient I/O (Input/Output) to accommodate the large number of LVDS pairs required for continuous data

streaming between the SDR and the processor. While the SEAF-RA connector provides an interface to backplane, another connector based on the VITA 57.1 FMC HPC standard can be populated on the secondary side of the PCB. The FMC standard provides a simple high-throughput interface for software and FPGA development with a variety of Xilinx and Intel development kits. Additionally, the adoption of VITA FMC 57.1 into 3U VPX radiation-hardened processors, including the SpaceCube v3.0 VPX and Curtiss-Wright FPE320, has gained traction in recent years. Inclusion of the FMC enhances the SDR platform functionality by enabling the long-held NASA "test-as-you-fly" paradigm, simplifies integration, and reduces FPGA development complexity.

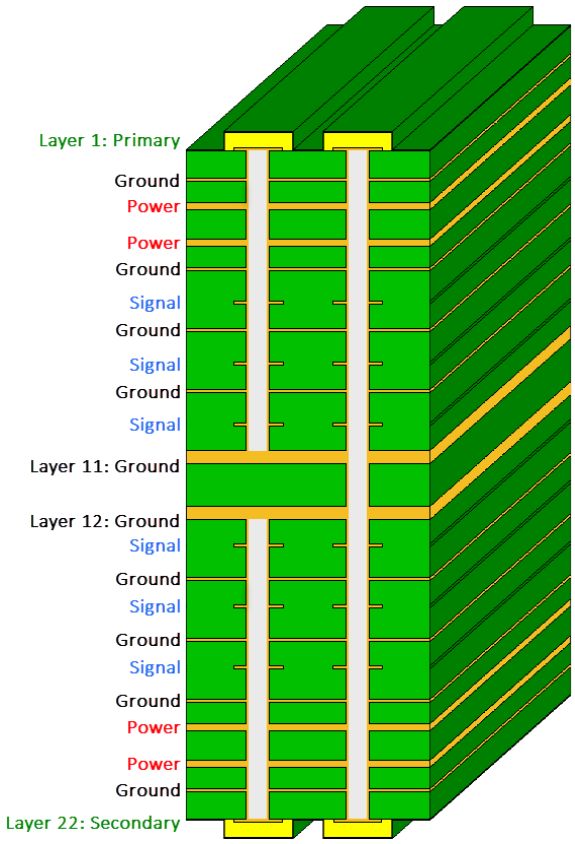

Figure 5: PCB Stackup with Blind Vias

The PCB stackup and design rules can impact SDR performance as much as RF component selection and power system design. Proper isolation between RF, digital signals, and power planes is critical to unwanted coupling of noise. RF signals are routed as coplanar waveguides on only the primary and secondary sides of the PCB to control trace impedance independent of dielectric thickness, minimize dielectric loss, and remove via stubs effects. A low loss PCB laminate on the outermost dielectric layers provides an ideal pathway for the RF I/O with less frequency dependence than polyimide used in SBC stackups. Power planes are enclosed between solid grounds and positioned close to the primary and second sides of the PCB to minimize decoupling capacitor mounting inductance. Isolating signal layers between ground planes reduces crosstalk between adjacent pairs, especially in complex designs. Figure 5shows the IPC-6012DS PCB stackup used in multiple SBCs at NASA GSFC [28].

IV. FPGA RESILIENCE

To operate each AD9361 device on the developed SDR, a full hardware/software (HW/SW) stack is required in the FPGA and CPU subsystems of the flight computer, respectively. The HW/SW stack for Xilinx SoCs (e.g., Xilinx Zynq-7000 SoC and Zynq UltraScale+ MPSoC) is illustrated in Figure 6. For Xilinx FPGAs (e.g., Xilinx Kintex UltraScale), a softcore processor (e.g., MicroBlaze) can be used to implement the software portion of the stack.

The FPGA portion of the stack includes the AXI AD9361 core and DAC/ADC pipelines. The AXI AD9361 core interfaces with the AD9361 device and provides modules for ADC channel processing, DAC channel processing, delay control, TDD control, and device/core control and status. The DAC pipeline uses a DMA to read data from memory, which is streamed through a data packer (packed data from one stream is unpacked into multiple channels), optional modulator, FIFO, and finally, the TX channel of the AXI AD9361 core. Inversely, the ADC pipeline receives data from the RX channel of the AXI AD9361 core, which is streamed through a FIFO, an optional demodulator, a data packer (data from multiple channels are packed as one stream), and finally, a DMA writes this stream to memory. Supplementary peripherals and logic (e.g., SPI and clock generators) are instantiated to provide additional control interfaces to the AD9361 device.

The software portion of the stack includes kernelspace and userspace components. The kernelspace includes devices drivers used to operate the AXI AD9361 core and other peripherals in the FPGA. In userspace, the libIIO library enables generic access to industrial I/O devices and provides an API to support the development and deployment of SDR applications.

SEE Mitigation for FPGAs

Due to the harsh environment of space, commercial SoCs are highly susceptible to radiation effects that may impact the dependability of both FPGA and software components. Two effective methods for SEE mitigation in SRAM-based FPGA designs include triple-modular redundancy (TMR) and configuration memory (CRAM) scrubbing [29]. TMR is a fault-

masking technique that involves the triplication of circuits in the FPGA design with replica outputs running through majority voters to mask single-bit errors. Despite the dependability advantages, TMR introduces a substantial overhead in the resource utilization (three replicas) and critical path (voter logic in signal path). The granularity at which TMR is applied can vary, which results in a trade-off between dependability and area. Fine-grain TMR has greater reliability because more frequent voters mask errors at a lower level. Coarse-grain TMR is more area efficient because less frequent voters are used.

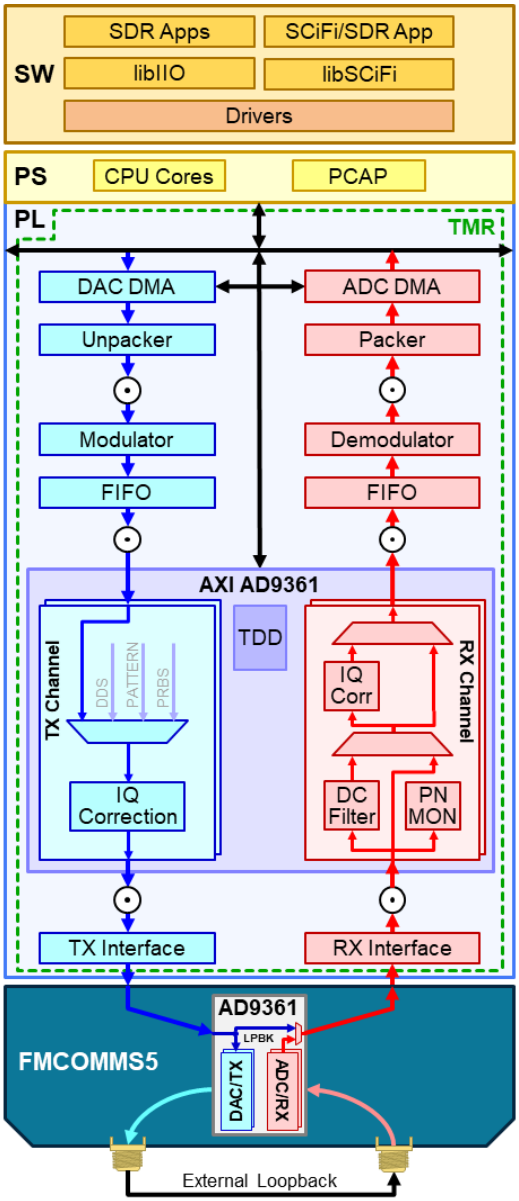

Figure 6. HW/SW Stack for Hybrid SoCs (e.g., ZC706/FMCOMMS5)

The FPGA stores the design bitstream in on-chip CRAM at runtime to implement the design on the FPGA. SEEs in CRAM can potentially change the functional operation of the implemented design. The accumulation of errors in CRAM can often overwhelm TMR systems. To prevent this accumulation of errors, a CRAM scrubber is used. This scrubber is a background process that periodically scans CRAM to detect and correct faulty frames using built-in CRC/ECC mechanisms. Several CRAM scrubbing architectures are discussed in [30].

FPGA Fault Tolerance

To demonstrate and validate the application of TMR and CRAM scrubbing for the FPGA portion of the stack, we use a provided reference design for the Xilinx ZC706 (Xilinx Zynq-7045 SoC) and Analog Devices FMCOMMS5 (ZC706/FMCOMMS5) [31]. Prior to triplication, the reference design is modified to remove logic that is not relevant for our space application (e.g., video/audio interfaces). Furthermore, the AXI AD9361 core is also modified to exclude the DDS, pattern, and PRBS options in the TX channel. The BL-TMR tool, an academic tool for selectively replicating designs at the post-synthesis stage [32], is then used to apply fine-grain TMR to the full FPGA design. I/O and clocking resources are kept unmitigated to generate a fully routable design with acceptable timing. To validate the modified and TMR designs, libIIO is used to transmit and receive the same sinusoidal signal through the DAC and ADC pipelines with the AD9361 device configured for internal, digital loopback. The resource utilization of the baseline, modified, and TMR designs are shown in Table 2.

Table 2. FPGA Resource Utilization for ZC706/FMCOMMS5 Designs

Design	LUTs (218.6k)	FFs (437.2k)	BRAM (545)	DSPs (900)	CRAM (846.1k)
Baseline	10.32%	8.56%	1.83%	7.22%	6.47%
Modified	4.99%	4.98%	1.47%	4.44%	3.68%
TMR	21.87%	14.92%	4.40%	13.33%	13.23%

BL-TMR v6.3, Vivado 2018.3 (Default settings); Release hdl_2019_r1

Radiation Testing

CRAM fault injection and radiation-beam testing will be performed to evaluate the susceptibility of the FPGA design to errors and the effectiveness of TMR with CRAM scrubbing. CRAM fault injection is the iterative process of injecting bit-flips into CRAM and observing the architectural response of the FPGA design. For each

iteration, a CRAM bit is randomly injected, and a signal is transmitted and received via internal, digital loopback. The received signal is compared against the transmitted signal to quantify the impact of the injected fault to the integrity of the transmission. The number of correct and failed transmissions are recorded. Because fault injection is controlled, the dependability of a specific subsystem of the design can be evaluated by targeting only the CRAM bits used by that subsystem. After several iterations of fault injection, two useful metrics are approximated. One is the architectural vulnerability factor (AVF) which is the probability that an error in the design will manifest into an observable failure (failed transmission). Another is the Mean-Work-To-Failure (MWTF) which is the amount of useful work completed until a failure is expected (number of successful transmissions until a failed transmission). In our fault injection experiment, SCi-Fi, a custom fault injector, is used to inject bit-flips into CRAM via the Processor Configuration Access Port (PCAP) peripheral of the PS.

In contrast to fault-injection testing, radiation-beam testing is the practice of irradiating devices under test (DUTs) by a high-energy radiation beam to induce errors. Fault-injection testing is a low cost, and relatively benign testing for DUTs, while radiation-beam testing can potentially damage the DUT and will incur the cost for using a radiation-beam facility. During radiation testing, each DUT continuously transmits and receives a signal via loopback (internal or external) and compares them to determine the integrity of the transmission. The number of correct and failed transmissions are recorded. The fluence, which refers to the number of particles that traversed the design per unit area per unit time, is also recorded. Because radiation-induced errors are uncontrolled, multiple signals of the FPGA design are probed (denoted as ⊙ in Figure 6), and the signals at these stages are also analyzed to approximate the origin subsystem that corrupted the transmission. The cross-section, which is the sensitive area of the device where a radiation-induced error will manifest into an observable failure, is calculated using the recorded counts and fluence.

These dependability experiments can enable adaptive and selective strategies to be explored for more efficient SEE mitigation. In adaptive mitigation, the FPGA can be reconfigured to switch between TMR and unmitigated designs in response to the dynamic environmental condition or changing mission phase. This adaptive approach is dynamic and allows for the system to alternate between the dependability and area trade-offs. In selective mitigation, TMR can be applied only to the subsystems most susceptible to SEEs. This selective approach is static and balances the trade-off between dependability and area.

V. CONCLUSIONS

The development of a robust, high-performance SDR architecture requires considerations and trade-offs between RF design, power systems, PCB layout, and processing domains in order to produce a single platform to support simultaneous communication, remote sensing, and navigation. This paper has described a hardware design framework for development of SWaP-C optimized RF hardware and an SDR architecture that is capable of providing the reliability needed for current missions and the performance needed to enable AI for future missions. The developed SDR is an implementation of this framework in the 1U CubeSat form factor, and provides the modularity needed for a new class of integrated bus architectures.

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