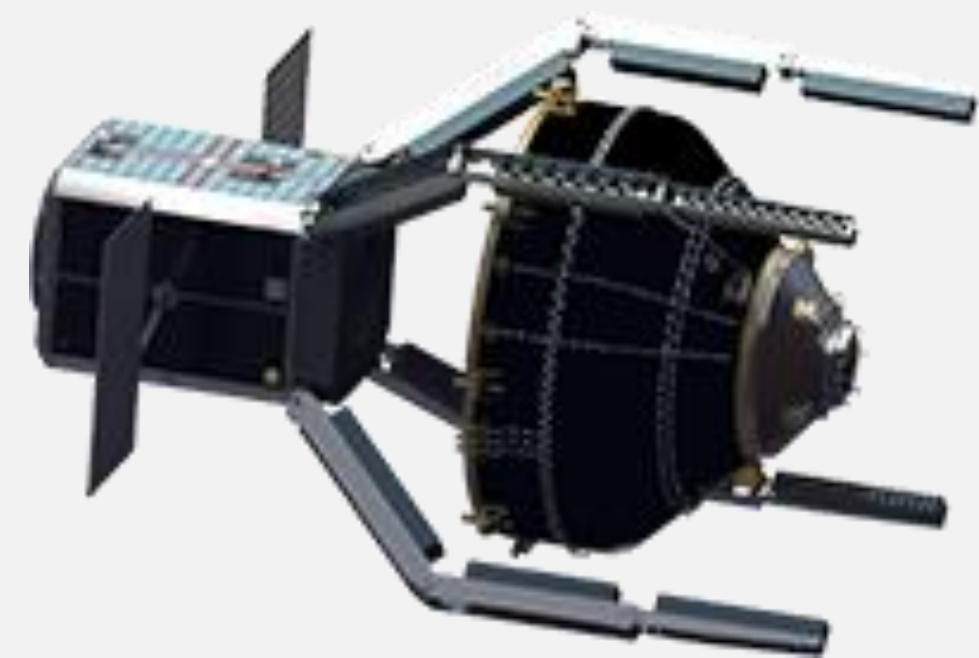


Dedicated On-Board Computer for Active Debris Removal Mission

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ClearSpace-1 Mission

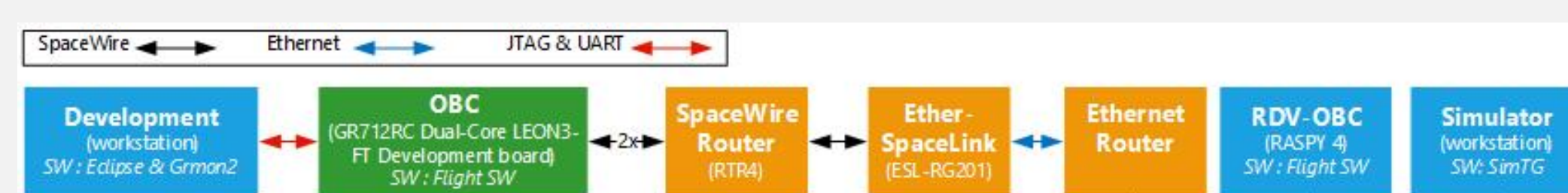
- CS-1 is an Active Debris Removal (ADR) mission led by the start-up ClearSpace and the EPFL Space Center, previously known as CSO. [1]
- The goal is to rendezvous with VESPUP (VEga Secondary Payload Adapter Upper Part) and deorbit it
- The development focuses on two main aspects :
 - A capture mechanism able to retract and deploy multiple times, moreover it should perform a soft capture of the target.
 - A Payload On-Board Computer (POBC) to host the different relative navigation and image processing algorithms. It should merge the data from various sensors needed for the approach and rendezvous phases.



CS-1 design ©ClearSpace SA

Hardware-In-the-Loop Setup

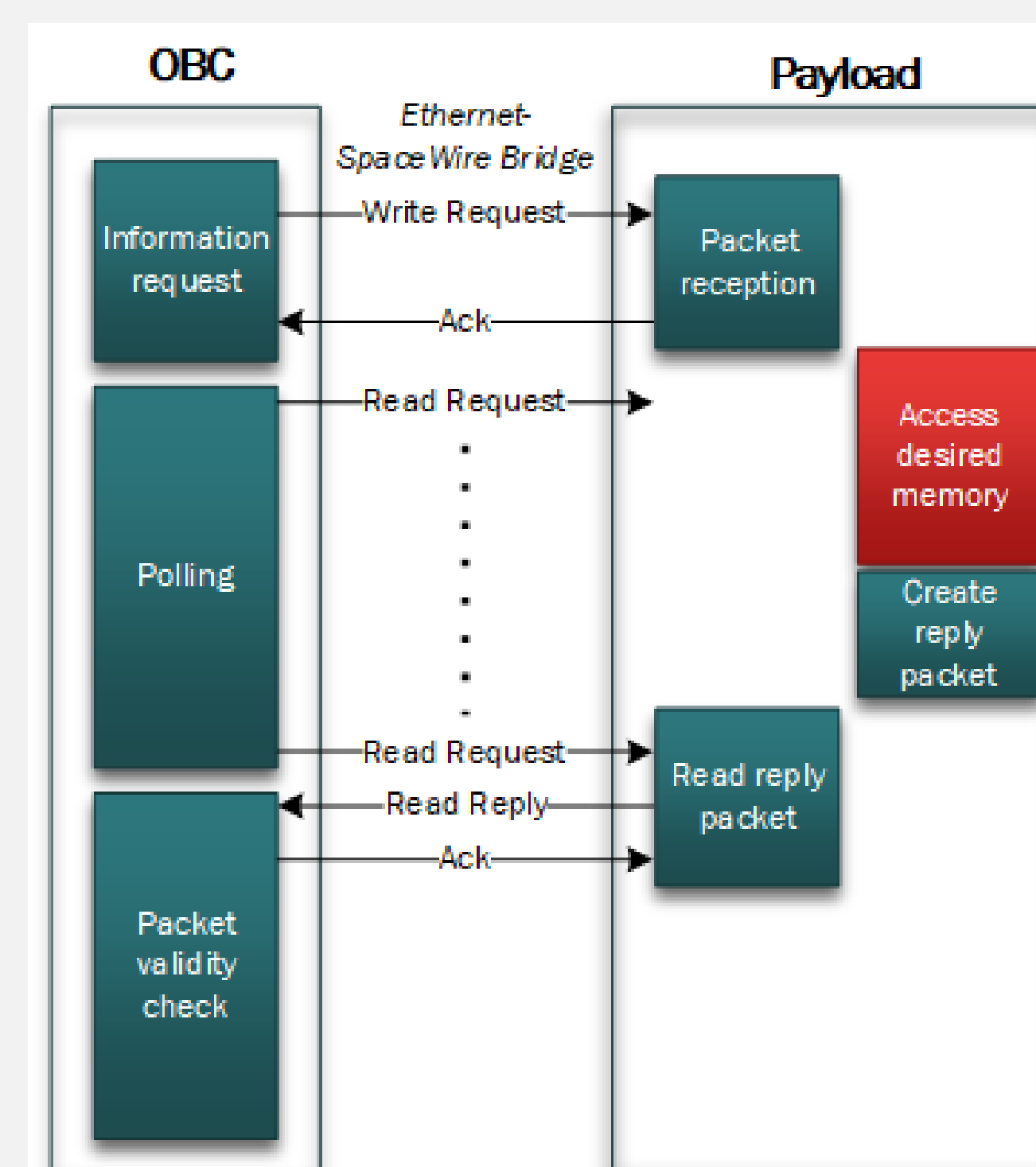
- Main avionic inherits from the FLP2 platform [2] designed by Airbus DS Friedrichshafen.
- Processor Board is connected to a SpaceWire Router and Ethernet-SpaceLink Bridge, then to the prototype payload and the simulator workstation.
- The OBC is the GR712RC development board build by Cobham Gaisler AG. It is a Dual-Core LEON3FT SPARC V8 processor.
- SpaceWire Router and Bridge are provided by 4Links.
- POBC is a Raspberry Pi 4 for the first phase of development. It will be upgraded to a more powerful board later.



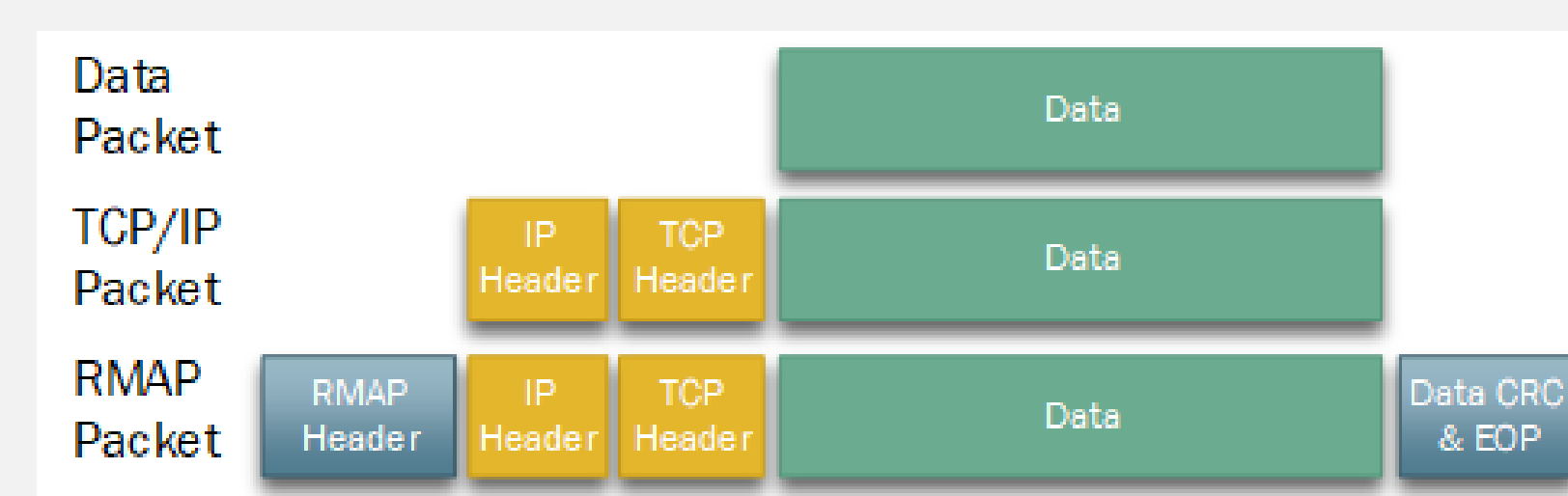
HIL Setup at EPFL Space Center

OBC-Payload Interaction

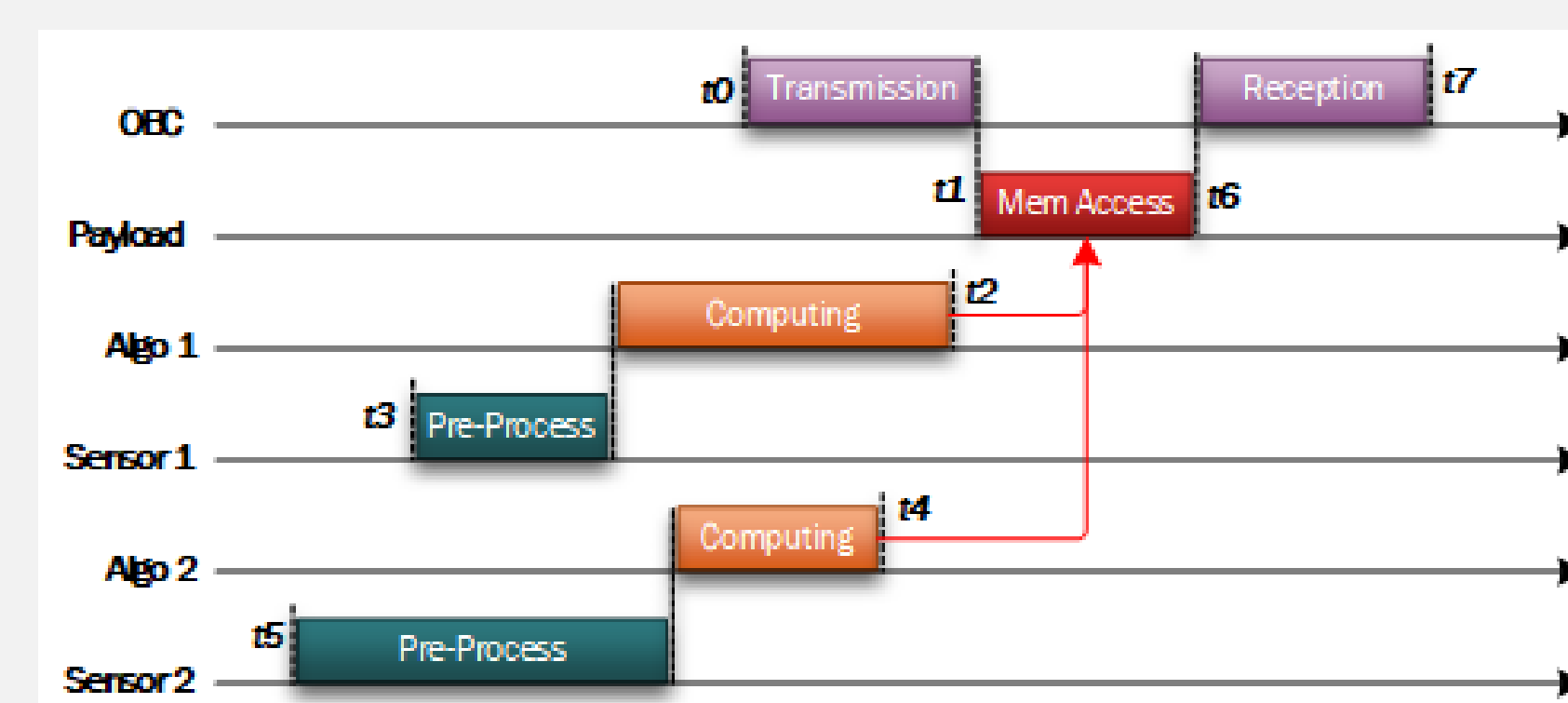
- Interaction
 - Connection through SpaceWire (SpW) & Ethernet
 - Hand-shake protocol with OBC as Master and POBC as Slave



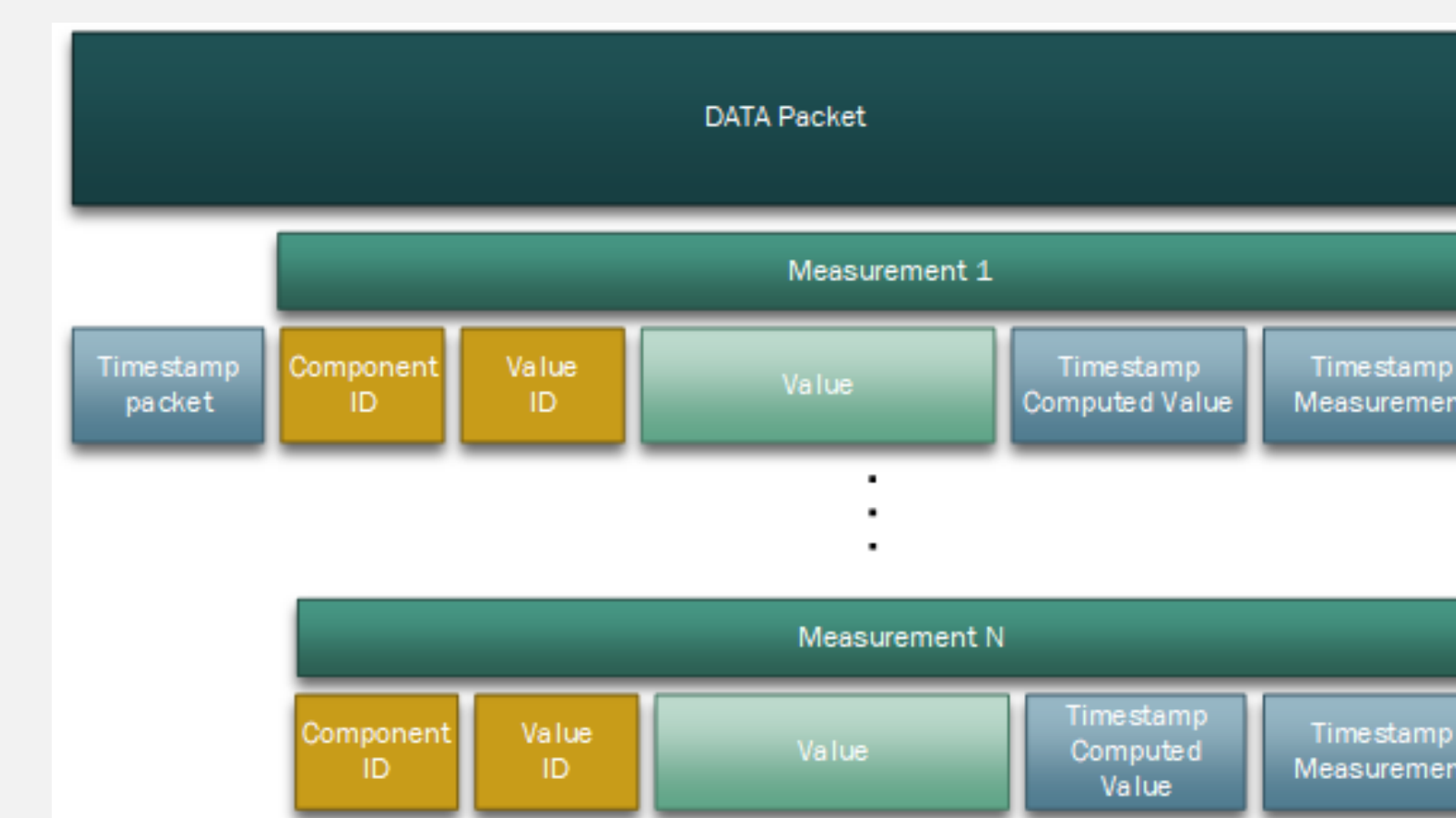
- Packets
 - Transformation from SpW to Ethernet
 - TCP/IP protocol for Ethernet & RMAP for SpW
 - Encapsulation by OBC
 - Routing management by Eth-SpW Bridge



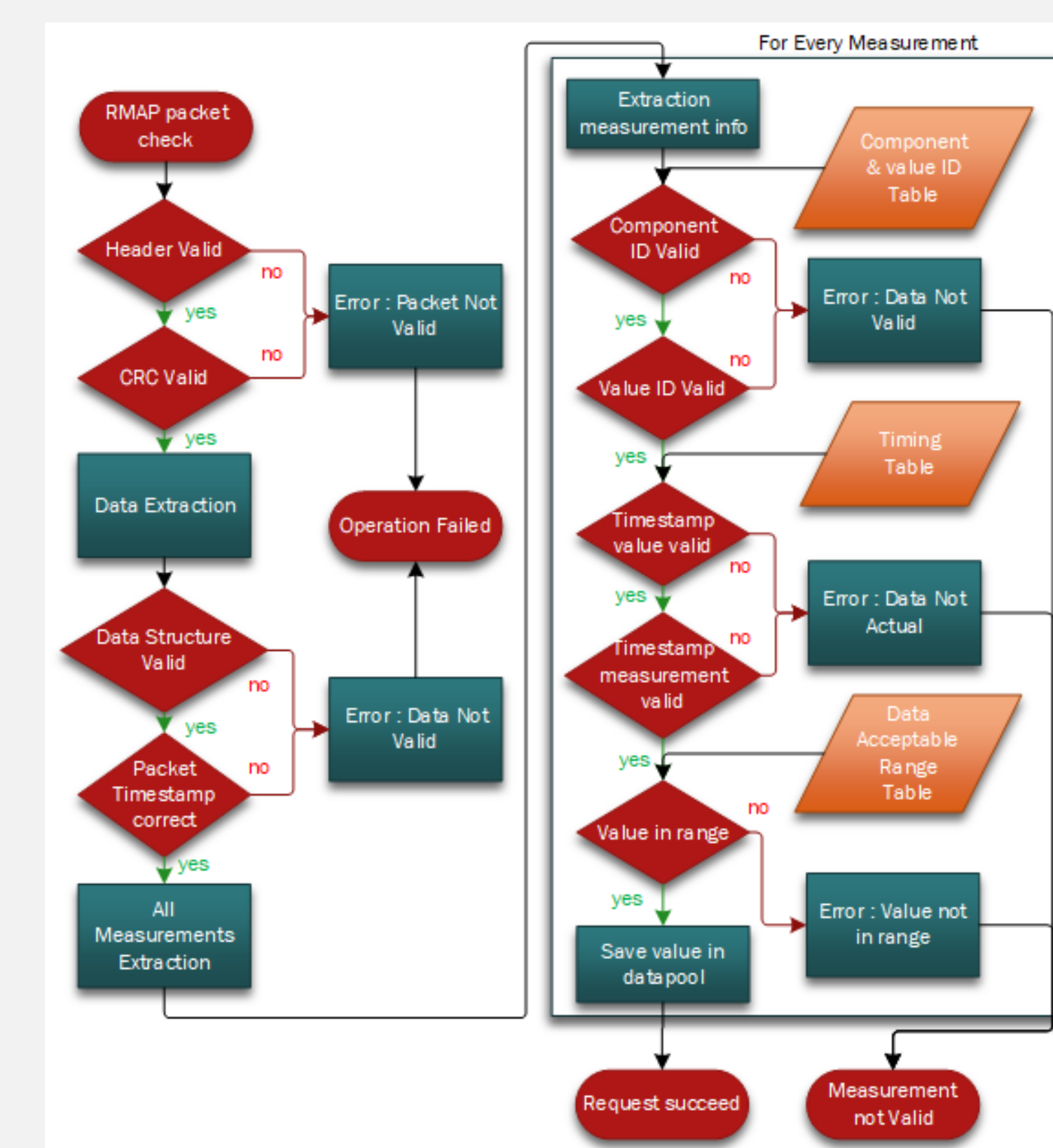
- Reaction Time
 - Determination of various timing from pre-processing to transmission protocol
 - For navigation purpose, all measurements should have a timestamp.
 - Some timing might be not deterministic



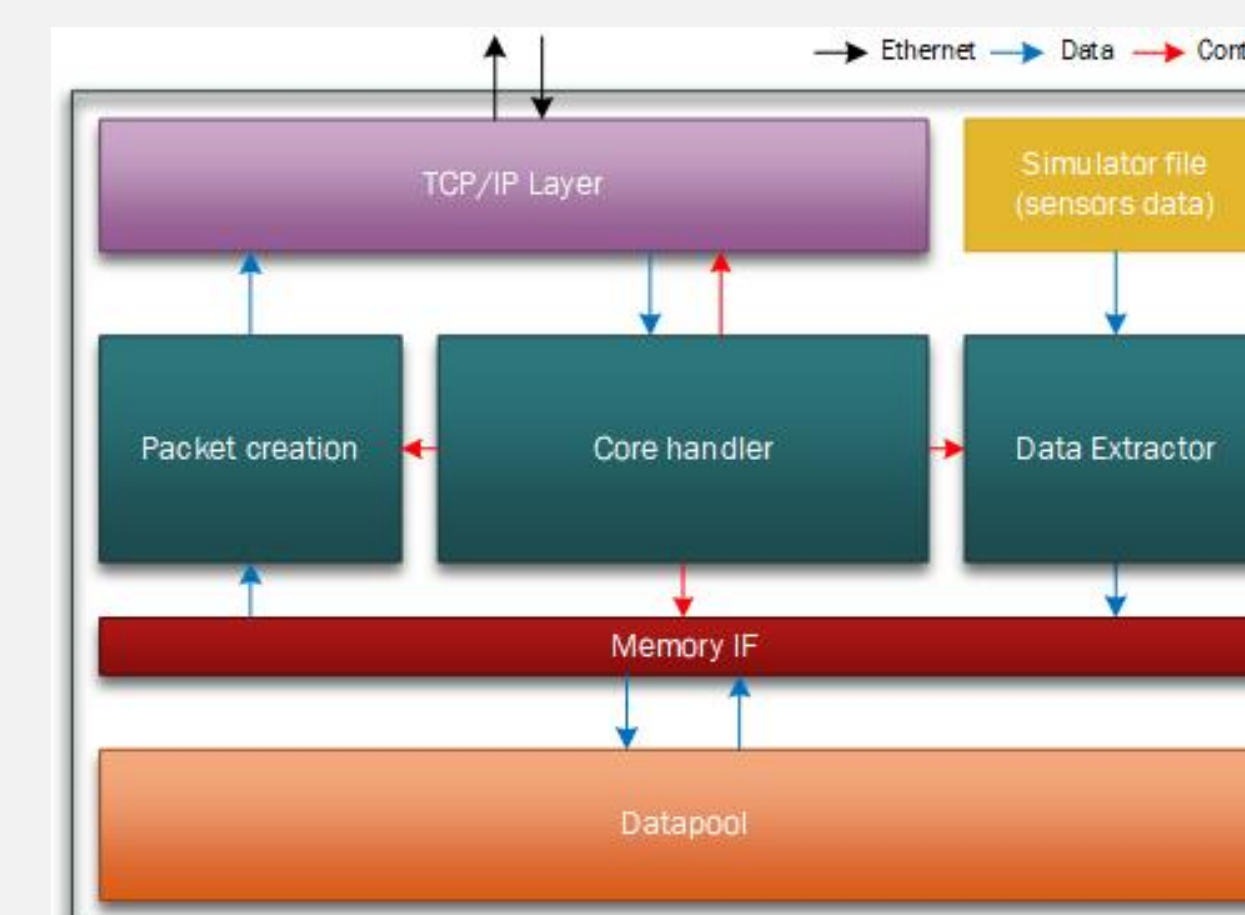
- Time Synchronization
 - Multiple timing information in each packets
 - Differentiation between measurement and process value



- Handling & Verification
 - Packet validation then structure validation
 - Comparison of each measurements with expected values (Range Table)
 - Table computed prior to mission with simulation



- Task Simulation
 - POBC prototype architecture
 - Simulation of sensors data



Challenges & Future Development

- High Priority Command
 - HPC to overcome timing issue
 - Increase in complexity & verification
 - Small data packet transfer for speed
 - POBC algorithm dependent
- OBC Polling & Redundant information
 - Determination of polling frequency
 - Constant information request thread in OBC
 - Transmission of redundant information
 - Time & resources consumption for verification procedure
- Integrity Check
 - Check of packets & measurements timestamps
 - Validity duration for measurements
 - Determination of data validity with respect to previously computed values
 - Expected data depend on mission phase
- Critical Situation Detection
 - Detection of critical situation by POBC
 - Critical status flag in regular packet
 - Increase of polling frequency
- Failure Detection, Isolation and Recovery
 - Dedicated FDIR for POBC
 - Level of autonomy of POBC vs OBC
 - FDIR information transmission through SpW
- Future Development
 - Verify protocol & timing
 - Ground control loop for POBC
 - Upgrade of POBC hardware
 - Increase complexity of payload software

Conclusion

- Prototype of communication management between OBC & POBC
- Characterization of time delay in the protocol
- Testing of timing synchronization
- Establishment of validation procedure for packets
- Elaboration of POBC prototype software
- More information in paper SSC20-P2-17

References

- [1] M. Richard, L. Kronig, F. Belloni, ..., and H. Shea, "Uncooperative rendezvous and docking for MicroSats," In 6th International Conference on Recent Advances in Space Technologies, RAST, 2013
- [2] Eickhoff, Jens (Ed.), "The FLP Microsatellite Platform - Flight Operations Manual," Springer, 2016.