AI-Based Novel Camera System with Software Defined Radio Transceiver On-board

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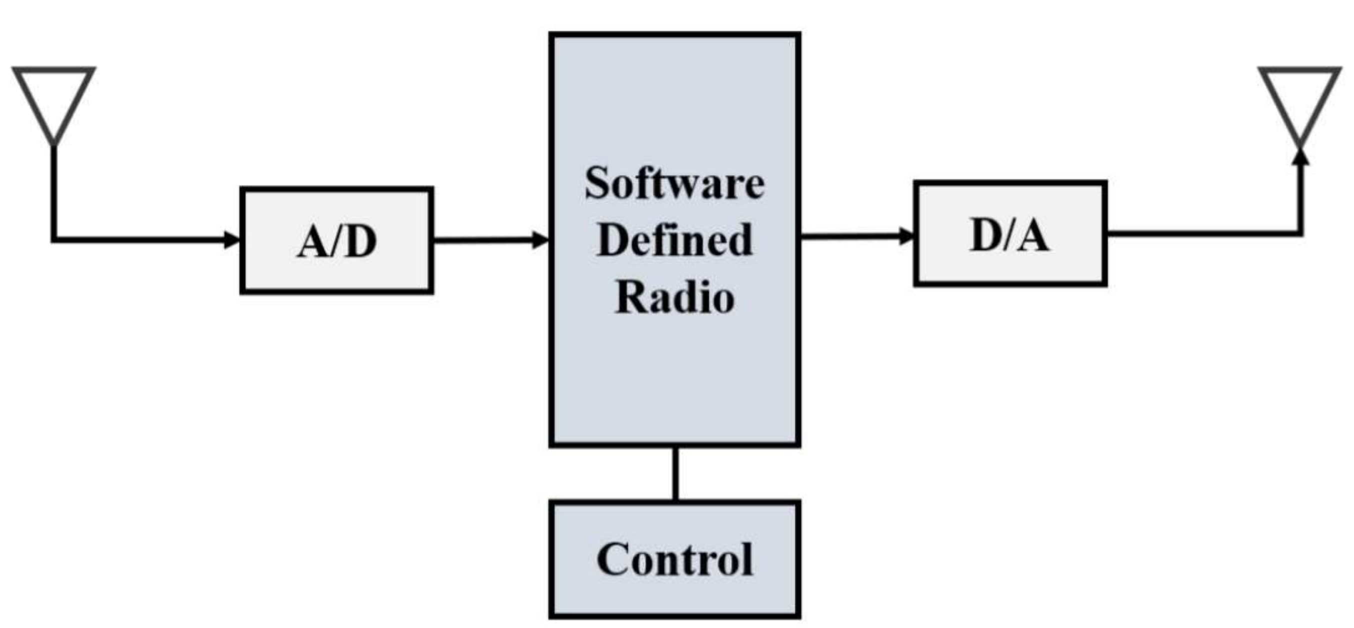
Background

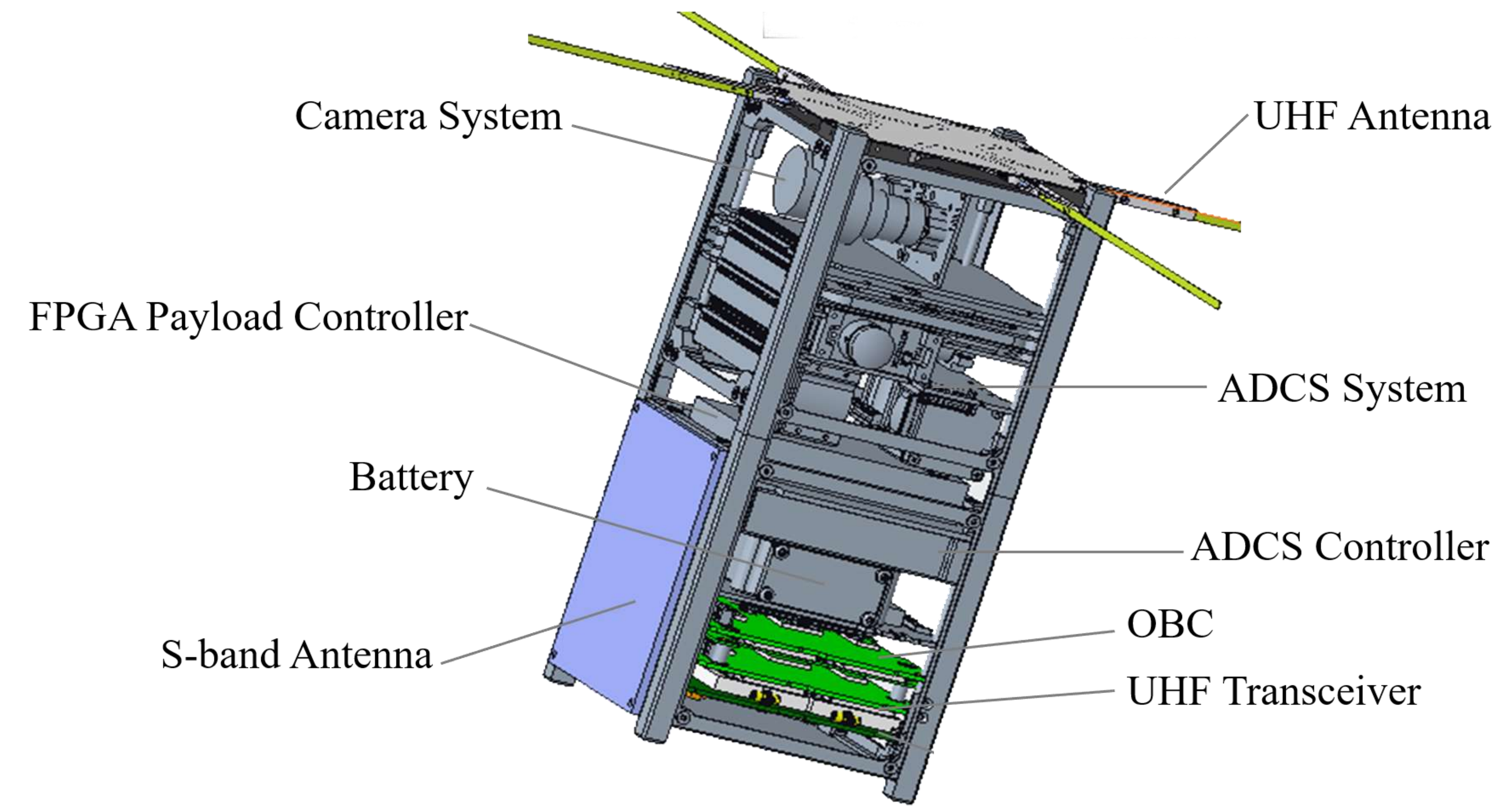
Standard RGB camera combines the number of pixels to perform RGB color, so for having each color represented in each pixel separately, three different cameras are required with different bandpass filters that allow only the required color signal to pass into the sensor. The most complicated part of developing such a system is the calibration of the cameras and building a system that can read out from different sensors and integrate the result. The other challenge in the CubeSat is the limited access time and the restricted data rate speed. Also, the high speed of the CubeSat leads to have so blurring images and some other noisy images. Moreover, in some cases where it is cloudy, the captured images have cloud-only. Thus, having an intelligent system that can classify the images using machine learning algorithms as valuable images for downlink or not valuable. Valuable images mean they are clear, no cloud, and not blurring.

Moreover, Radio communications continues to make an enormous impact on the various aspects of human lives. However, conventional or legacy radio systems are not programmable. They are designed for one fixed configuration. They are built to produce a single waveform at a specified frequency. Conventional radios limitations created a number or need for improved communication in space. For space communication, it is highly desirable to have radios that are easy to adapt to various modulation schemes, with a flexible implementation, and can be reconfigured to cater to different usage scenarios without affecting the power budget as it is very critical for these type of applications. These requirements where the main driver for the invention of the Software-defined radios (SDR), which are reconfigurable with all (some) of functional components are implemented in either pure Software or in a soft form such as RTL based. Thus, In this project, all the digital components of an SDR are developed targeting FPGA implementation. As mentioned, the SDR produced to overcome the limitation of conventional radio in terms of its flexibility. The Figure below shows the block diagram of SDR, where digital components are replacing all analog components, and the antennas are connected directly to Analog to Digital Converter (ADC) at the receiver side or Digital to Analog Converter (DAC) at the transmitter side.



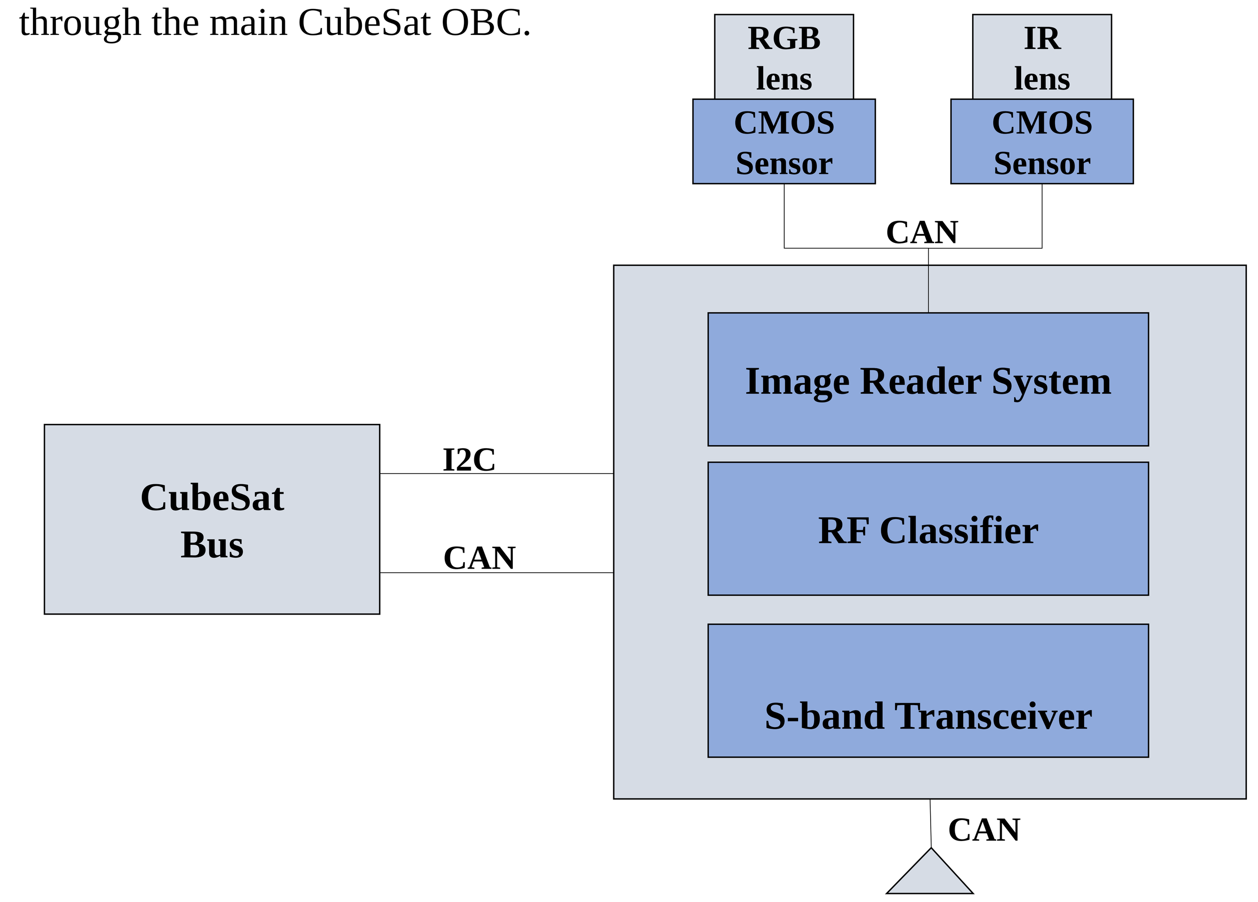
Volume Budget

The proposed payload system is fitted within a 2U CubeSat structure. The figure below shows the volume budget of the CubeSat. A 2U structure has been chosen due to the need for reaction wheels in the ADCS Subsystem. The reaction wheels are required to have accurate pointing toward the targeted area for less blurring captured images. Moreover, in order to have a light of sight communication, a target pointing is required. To be performed using reaction wheels. The camera and the S-band patch antenna are facing toward the earth in Z-axis. Thus, the CubeSat will have a horizontal orientation to increase the lifetime by decreasing the drag area.



Payload System Block Diagram

The payload system consists of an FPGA board that has the image reader system, Random Forest classifier, and S-band transceiver implemented on-board. The image reader function will collect the images from the CMOS sensor. The CubeSat main OBC is connected to the payload controller using the I2C bus. Also, it is connected to the EPS. The S-band antenna is connected directly to the FPGA board using CAN bus. As a result, the transmission time is faster because it did not require to transmit the data through the main CubeSat OBC.



Optimized Random Forest Classifier

Random Forest machine learning algorithm perform a high classification accuracy. It is a decision tree based. Accordingly, software implementation using a high-level language such as C++ execute the tree serially, however hardware implantation using HDL languages such as VHDL executes the tree in parallel. Parallel based tree execution accelerates the classifier by minimizing the required classification time. Thus, a parallel RF classifier is implemented on FPGA VHDL language with an optimized design. The result shows that the RF classifier can 15.5% less than the related work from literature. This design represents each leave node as a path of AND-OR logic. Thus, only one path will be true to represent the resulted class. The table below shows the result device utilization for RF implementation FPGA board.

Slice Logic Utilization	Used	Available	Utilization
Number of Slice Registers	33	157,200	1%
Number of Slice LUTs	114	78,600	1%
Number used as logic	114	78,600	1%
Number used as Memory	0	26,600	0%
Number of occupied Slices	41	19,650	1%
Number with an unused Flip Flop	82	115	71%
Number with an unused LUT	1	115	1%
Number of fully used LUT-FF pairs	32	115	27%
Number of slice register sites lost to control set restrictions	23	157,200	1%
Number of bonded IOBs	67	250	26%
Number of BUFG/BUFGCTRLs	1	32	3%

Payload System FlowChart

Payload will be switched ON if the CubeSat is within the Range of the targeted area. This process will be initiated using a flag based on the GPS readings. The image will be classified using an RF classifier. If it is classified as a cloudy image, then it will be deleted because not a useful image detected. Else it will be transmitted using S-band transceiver after image compression and noise reduction process.