

## . Abstract

The Quickly Universally Integrated Concept CubeSat platform, or QUIC, is an experimental space mission architecture that intends to address the need for a rapid development path towards flight readiness by standardizing essential engineering aspects of a satellite, such as chassis, avionics, and power systems, while providing an interface that can quickly and readily accept mission payloads. While the smaller form factor and theoretical simplicity of CubeSats have enabled space access at relatively low costs there still exists a very high barrier to success for first-time CubeSat builders. This is especially true in academia where engineering a CubeSat from the ground up is the longest and most difficult part of development compared to preparing the payload, especially in teams without structural, thermal, or electrical analytical expertise. Independent research has also shown that CubeSat missions often suffer from a high rate of failure and lack of replicability due to these challenges being pitted against teams unfamiliar with traditional space systems engineering processes. Furthermore, in a competitive market of space access, supply for launches has begun to outpace the demand, as not enough small satellites can be produced to keep up with traditional methods. By consolidating communication through a universal interface, various payloads can be connected without compatibility issues and clients can program data collection, computation, and transmission to suit their needs with the onboard computer without incurring significant challenges with hardware integration. As QUIC is designed to accelerate prototyping and development, all components would be easily machined or purchased as commercial off the shelf parts, and assembly can be done by even high school students, vastly expanding the range of access for Low Earth Orbit research. It also is not limited to space, as Bronco Space at Cal Poly Pomona will employ the first stages of QUIC for their high-altitude balloon program, the Balloon Launch Assessment Directive for Engineers, or BLADE.

### II. Background Information

QUIC builds off the pedigree of two past missions and design concepts. First, as a demonstration of the use of consumer grade technology for space missions, a line may be drawn from the PhoneSat series of satellites from NASA Ames Research Center (ARC). The PhoneSats employed consumer grade smartphones as the primary flight computers for a series of 1U CubeSat technology demonstration flights between 2009 and 2014. When the program concluded the PhoneSat bus itself was evolved into the TechEd bus (based on Intel's consumer grade Edison Single Board Computer) which continues to fly novel technologies to this day. A second line can be drawn from the Air Force Research Lab's NANOSATELLITE AND PLUG-AND-PLAY ARCHITECTURE (NAPA), spearheaded by Dr. James C. Lyke. NAPA is the culmination of an over 14-year effort by the AFRL to develop and demonstrate a suitably "Plug-and-Play" space mission architecture that will greatly reduce mission development times and costs to enable what the Operationally Responsive Space Office (ORSO), of the Department of Defense (DoD), has dubbed "The Six Day Satellite." Although Space Plug-and-Play Avionics has traditionally looked to the small satellite form factor for implementation, a recent push in the 6U CubeSat form factor has yielded two successful missions to validate the performance of conceptual Plug-and-Play architectures on-orbit. The heritage and on-going progress of the NAPA project is a clear indicator that a Plug-and-Play architecture such as QUIC's is viable and in demand.



# The Quickly Universally Integrated CubeSat **Rapid Integration for Small Packages**

#### Michael L. Pham, Christopher P. Artates - Cal Poly Pomona 2020

mlpham@cpp.edu • cpartates@cpp.edu

# III. Specific Goals & Expected Outcomes

Primary Objectives:

- To demonstrate that a Cal Poly Pomona dreamed, designed, and built satellite can be delivered to perform fundamental mission operations in Low Earth Orbit at lost cost.
- lead times.
- To educate the current cohort of students participating in the Bronco Space Cube Satellite Development Program in all aspects of Space Mission Engineering Secondary Objectives:
- To provide a space mission architecture and infrastructure that is repeatable without the need for highly specialized training or long lead times.
- To develop a holistic space mission ecosystem that enables a high degree of vertical integration during the space mission engineering process.



# IV. Methodology

The first designs of QUIC were constrained within a 1U, maximizing as much space for a mission payload. Current working iterations would instead concentrate essential subsystems into the 1U space that could scale up to larger unit configurations. With 3U being the most common formfactor for hosted science missions, 2U's worth of space could then be used for payload and auxiliary subsystems. The layout for mechanical integration in the extended bay would be traded between a rung, slot, and pegboard system to be compatible with various mounting methods. An attitude control subsystem could be included for missions requiring accurate pointing accuracy and/or more power via deployable solar panels. Taking advantage of the space and power in a 3U, a modern and affordable commercial off the shelf onboard computer (OBC) could push the bounds of performance of a CubeSat. Solutions such as the PyCubed, Raspberry Pi, NVIDIA Jetson, and a customized Intel NUC were evaluated as potential candidates for their low power consumption, compute potential, and user-friendly development environment for software.

• To demonstrate that the concept of a general use, "Universally Integrated," satellite can meet the needs of an academic or research mission without extensive specialized training or long

The QUIC platform is designed to be as flexible as a user needs it to be and simple to integrate with in order to minimize a CubeSat's engineering development timeline. To meet those goals, we selected the NVIDIA Jetson Nano as the central flight computer. Made for embedded systems, the Jetson line of products can run full desktop-class operating systems with a familiar development environment to both new and experienced CubeSat users. The Jetson Nano specifically uses the least amount of power while still providing a 128-core GPU for hardwareaccelerated tasks, such as image processing and machine learning. The NVIDIA Jetson Nano had not been previously flown in space, so it will undergo various testing to verify its performance in simulated conditions. A technology demonstration mission was conceived to have the Jetson Nano as the primary payload. The mission, BroncoSat-1, will record benchmark performance while in orbit, power consumption, and heat output with a custom designed thermal solution. The first planned implementation of the QUIC bus will be a mission in partnership with Texas State University (TXST). TXST would develop a payload to observe Terrestrial Gamma Ray Flashes, or TGFs, which will test the simplified integration with the unified communication interface in the allotted 2U space.



As access to space has become progressively more available, production of successful small satellites (specifically CubeSats) has proven to be a major bottleneck for groups looking to capitalize on cheap, and now dedicated, launches to space. Thus, an architecture that enables new developers in the field to fly their missions in space quickly, simply, and reliably is will be essential to support the widening market for space commercialization, utilization, and research. To prove the capability of a Quickly Universally Integrated Cubesat concept to meet the above stated needs, a joint mission was designed and conducted with partners at Texas State University following the maiden flight of an NVIDIA Jetson Nano to verify it as a space ready OBC.

Technology Demonstration Mission • Ready for System Level Testing by Q4 2020 • Ready for Flight by Q1 2021 Hosted Science Mission • Ready for System Level Testing by Q1 2021 • Ready for Flight by Q3 2021

# V. General Results

### VI. Conclusions & Next Steps

#### SSC20-WP1-06