Comparison of the gate drive parameter space for driving power MOSFETs using conventional and cascode configurations

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***Abstract*—Conventional voltage driven gate drive circuits utilise a resistor to control the switching speed of power MOSFETs. The gate resistance is adjusted to provide controlled rate of change of load current and voltage. The cascode gate drive configuration has been proposed as an alternative to the conventional resistor-fed gate drive circuit. While cascode drive is broadly understood in the literature the switching characteristics of this topology are not well documented. This paper explores, through both simulation and experimentation, the gate drive parameter space of the cascode gate drive configuration and provides a comparison to the switching characteristics of conventional gate drive.**

I. Introduction

Conventional voltage driven gate drive circuits utilise a resistor (see fig. 1) to control the switching speed of power MOSFETs [1]. The gate resistance is adjusted to provide controlled rate of change of load current and voltage. This method of drive introduces long switching delays due to the time required to charge the gate-source capacitance of the power MOSFET, described by the RC time constant of the gate resistor and capacitance. The delays in charging the gate of the power MOSFET result in increased switching losses and conduction losses. The high driving impedance also makes the MOSFET susceptible to failure modes invoked by the MOSFET parasitic capacitance during switching transitions.

Current sourced [2], [3] and resonant [4], [5] gate drivers have also been developed, which utilise an inductive magnetic element to charge the gate of a power MOSFET. These drivers provide some advantages over voltage driven gate drive, such as recovery of gate drive energy and reduced turn on times, but exhibit limitations in performance (minimum duty cycle and circulating current losses) and practical implementation (complexity, size and cost).

The cascode gate drive configuration is proposed in [6] as a solution to overcome the limitations of existing gate drivers. The proposed driver exploits the cascode configuration with the inclusion of an active gate clamp to turn off the power MOSFET under all load conditions. Gate drive current is not sourced through a resistor, allowing high peak currents to be delivered to the gate during turn-on and the Miller effect to be eliminated, at the expense of additional complexity.

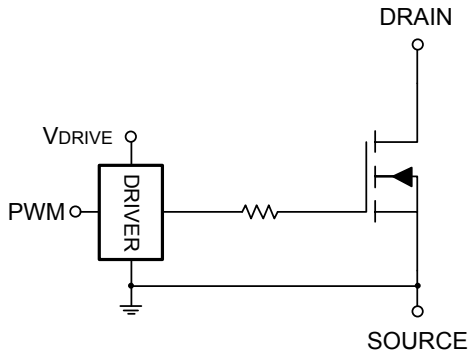

Fig. 1. Conventional resistor-fed gate drive circuit.

II. Cascode drive of power MOSFETs

The cascode configuration is broadly understood in the literature [1] but is typically applied to current driven devices such as BJTs [7], [8] or normally-on devices such as JFETs [9], [10] for which the benefits of a cascode connected drive are more readily apparent. The characteristics of a cascode drive for high-voltage power MOSFETs in switching applications are not well documented.

The proposed cascode gate drive circuit is shown in figure 2. The circuit is composed of two low-voltage n-channel power MOSFETs. Q1, the clamp MOSFET, and Q2, the cascode MOSFET, are used to drive high-voltage power MOSFET, Q3. The voltage source, $V_{drive,HV}$, supplies the drive current for the high-voltage MOSFET and sets the desired maximum gate-source voltage. The clamp and cascode MOSFETs may optionally be driven from a separate voltage source, $V_{drive,LV}$, allowing the use of low voltage MOSFETs optimised for lower drive voltages.

The high-voltage MOSFET is driven on by turning on the cascode MOSFET. The cascode MOSFET is required to carry both the drive and load currents; the turn-on process for the cascode drive configuration is therefore more complex than that of a convention gate drive. A detailed discussion of the turn-on process and relative merits of cascode gate drive is provided in [6].

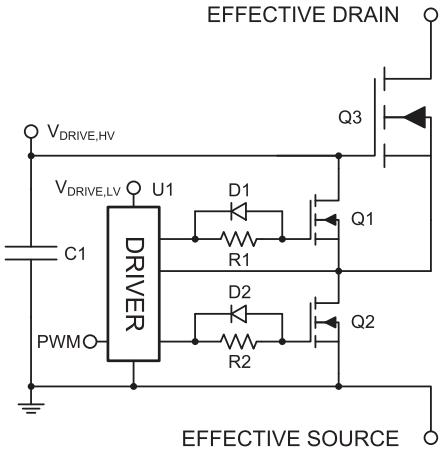

Fig. 2. Proposed cascode gate drive circuit.

III. The Gate Drive Parameter Space

Typically the only mechanism considered for the control of a conventional gate drive is the gate resistance. Gate drive voltage may be considered, but is usually maximised to reduce on-state conduction losses. Another potential mechanism for controlling the turn-on speed in a conventional gate drive is the addition of external gate-source capacitance. While addition of external gate-drain capacitance could also be used to control turn-on, it is not practical due to the increased susceptibility of the MOSFET to dV/dt induced turn-on that would result.

For the cascode gate drive configuration the primary mechanism for controlling the turn-on speed is the cascode MOSFET gate resistance. The cascode configuration provides a number of additional degrees of freedom compared with the conventional drive circuit (cascode MOSFET gate-drain, gate-source and drain-source capacitance, cascode MOSFET drive voltage etc.). For the purposes of this work we select the high-voltage MOSFET gate-source capacitance as the other control parameter of interest. It is worth noting that due to the current paths involved in charging the gate of the high-voltage MOSFET through the cascode MOSFET, adding external capacitance to the gate-source of the high-voltage MOSFET is equivalent to adding drain-source capacitance to the cascode MOSFET. Adding capacitance to the gate-source of the high-voltage MOSFET may be preferred, however, to provide a low impedance bypass for high-frequency currents injected into the gate during switching transients.

Key performance metrics that can be used to assess the effect of drive parameters on switching performance include switching loss, maximum dV/dt, maximum di/dt, rise/fall times and switching losses. We select maximum dV/dt, maximum di/dt and switching loss to characterise the switching performance for the purposes of this work. Maximum dV/dt is of interest with respect to the dV/dt ruggedness of opposing switching devices in a half-bridge configuration. Maximum di/dt is of interest from the perspective of EMI considerations as well as affecting peak reverse recovery and junction capacitance charge/discharge currents. Switching loss captures to some extent a range of switching features, but particularly gives a good sense of the total switching time and average rise/fall times.

Parameter	Value
HV MOSFET, *MH*	IPL60R199CP
Cascode MOSFET, *ML*	CSD86350Q5D, Sync
Bus voltage, V_{bus}	400V
HV MOSFET drive voltage, V_{drh}	12V
Cascode MOSFET drive voltage, V_{drl}	5V
Load current, I_L	10A
HV MOSFET gate resistance, R_{ghe}	10-500Ω
Cascode MOSFET gate resistance, R_{gle}	100-1000Ω
HV MOSFET gate-source capacitance, C_{gshe}	10pF-100nF

TABLE I. Test conditions for experimental exploration of cascode gate drive parameter space.

IV. Exploration of the Gate Drive Parameter Space by Simulation

A. Methodology

As outlined in the previous section, we select two parameters spaces for investigation. For the conventional drive configuration we select the high-voltage MOSFET gate resistance and additional gate-source capacitance, (R_{ghe}, C_{gshe}), parameter space. For the cascode drive configuration we select the cascode MOSFET gate resistance and high-voltage MOSFET additional gate-source capacitance, (R_{gle}, C_{gshe}), parameter space.

Switching characteristics are investigated for an inductive clamped switching application. Transient simulations are performed using LTspice at a number of points over the selected parameter spaces. A 650V 9.9A 199mΩ CoolMOS power MOSFET is selected as the high-voltage power MOSFET under test. The manufacturer published level-1 spice model is used. A 30V 25A 1.1mΩ MOSFET is used for the cascode device. A device model extracted from datasheet parameters was used for this device in the simulations. Ideal models are used for all other simulation components, including the clamping diode. Table I summarises the test conditions for which the parameter space exploration was performed. Figure 3 shows the circuits used for the transient simulations.

Waveform features including maximum di/dt, maximum dV/dt and turn-on switching loss were extracted for each transient simulation and collated. Finally, contour plots were produced for each result surface generated from the simulations across the parameter space.

B. Results

The maximum di/dt, maximum dV/dt and switching loss surfaces for the (R_{ghe}, C_{gshe}) parameter space for a conventional gate drive circuit in an inductive clamped switching application are presented in figure 5.

Annotation 5a shows the typical control trajectory available in a conventional resistive-fed gate drive: control of the gate resistance. Note that for this control trajectory no independent control of the plotted switching metrics is available, evidenced by the parallel contours; changing the gate resistance changes all the metrics to some degree. Alternatively consider the annotated trajectory 5b. Introducing C_{gshe} as a second degree of freedom allows this constant dV/dt contour to be tracked across the parameter space; by increasing both R_{ghe} and C_{gshe} it is possible to hold the maximum dV/dt constant at 20V/ns while decreasing the maximum di/dt from 500 to 100A/μs. Alternatively it is possible to hold the maximum di/dt constant

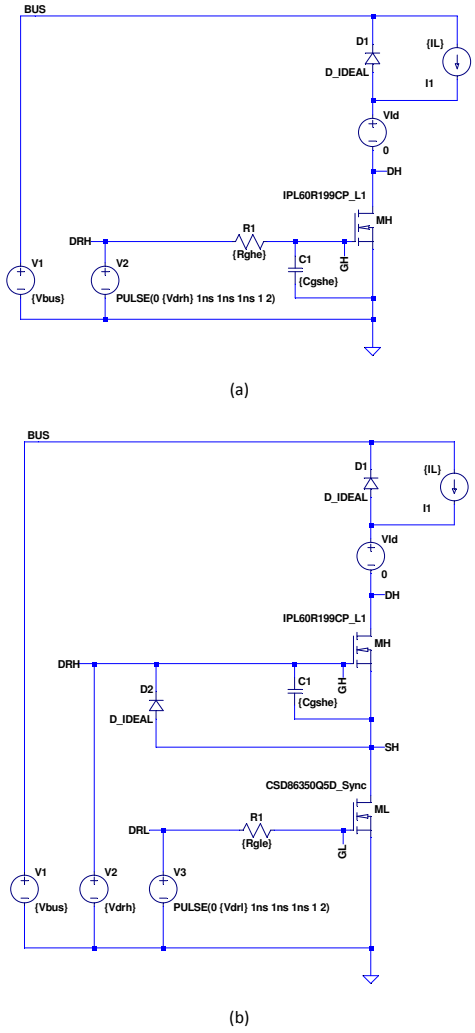

Fig. 3. Simulation schematics for the exploration of the gate drive parameter spaces of the (a) conventional and (b) cascode gate drive configurations.

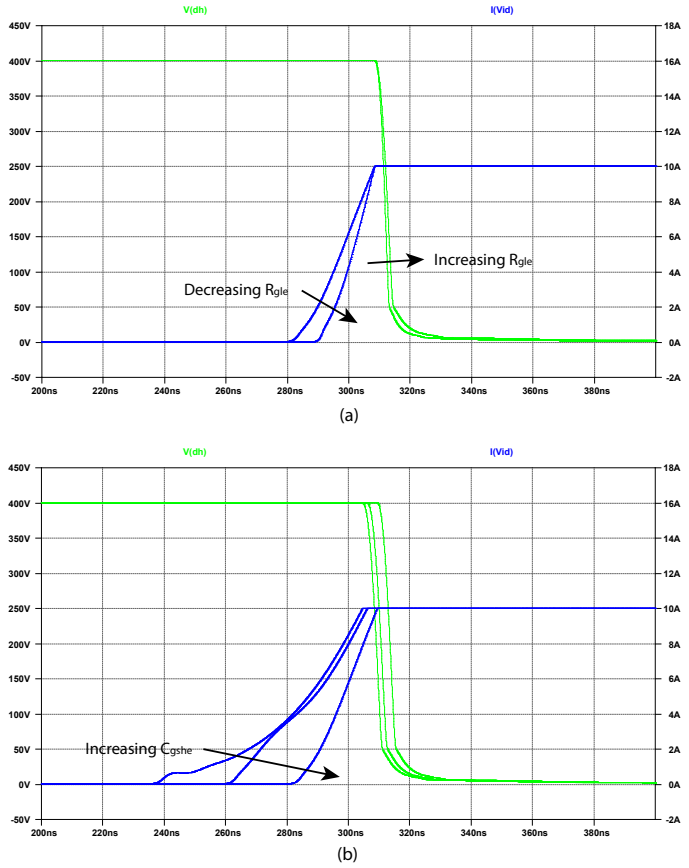

Fig. 4. Simulated turn-on transient waveforms for the cascode gate drive configuration operating a load current of 10A with (a) a fixed value of $C_{gshe} = 40nF$ and gate resistance, R_{gle}, values of 150Ω and 220Ω, and (b) a fixed value of $R_{gle} = 220\Omega$ and additional gate-source capacitance, C_{gshe}, values of 100pF, 10nF and 40nF. Traces are plotted for the drain-source voltage, V_{ds} (green), and drain current, I_d (green). Traces in (a) have been time-synchronised at the point where the load current is fully supported by the HV MOSFET ($I_d = I_L = 10A$) for easier comparison, since R_{gle} significantly influences turn-on delay.

while traversing the dV/dt contours (trajectory 5c), resulting in reduced switching losses.

Note that with the conventional gate drive, for a given maximum dV/dt constraint we can only use the (R_{ghe}, C_{gshe}) to *decrease* the maximum di/dt, and hence, increase the switching losses. Conversely, for a given maximum di/dt constraint it is only possible to increase the maximum dV/dt via this parameter space.

The maximum di/dt, maximum dV/dt and switching loss surfaces for the (R_{gle}, C_{gshe}) parameter space for a cascode gate drive circuit in an inductive clamped switching application are presented in figure 6. The result space for the cascode configuration exhibits a very different shape to that of the conventional resistor-fed circuit.

Annotation 6a shows the typical control trajectory where the cascode MOSFET gate resistance is controlled. As with the conventional gate drive, independent control of the switching metrics by this parameter alone is not possible. Note, however, that for an increase in C_{gshe} the maximum dV/dt *decreases* but switching losses actually *decrease* (constant loss contours swing to the right). The maximum di/dt is relatively insensitive to changes in gate-source capacitance for much of the parameter space (evidenced by the vertical di/dt contour lines).

To assist in the explanation of this phenomenon, corresponding transient waveform plots have been provided in figure 4 corresponding to annotated trajectories 4c and 4d in figure 4. Figure 4a shows that as R_{gle} is decreased both maximum di/dt and maximum dV/dt increase, with the benefit of reduced switching losses. Considering figure 4b it can be seen that increasing C_{gshe} substantially changes the shape of the current rise, reducing the transition time such that the average di/dt is much closer to the maximum di/dt. This phenomenon can be attributed to the additional gate drive current changing the operating point of the cascode MOSFET at the turn-on instant.

Given this phenomenon, consider the annotated example control trajectory 6b; this trajectory traces a constant maximum dV/dt path of 50V/ns through the parameter space. By following this trajectory it is possible to reduce the switching loss from 400μJ to approaching 200μJ by increasing maximum di/dt while holding maximum dV/dt constant.

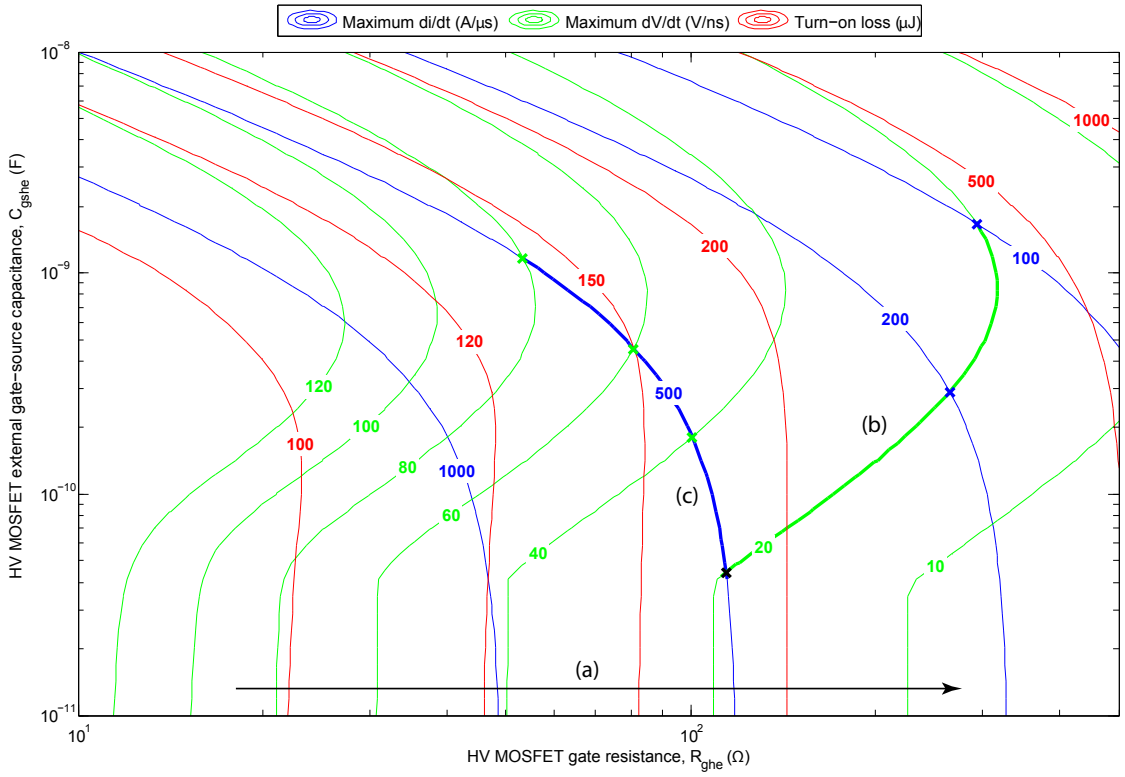

Fig. 5. Simulated switching performance surfaces for the conventional gate drive configuration over the (R_{ghe}, C_{gshe}) parameter space. Plotted are contours of constant maximum dI_d/dt (blue), maximum dV_{ds}/dt (green) and turn-on switching loss (red). (a) Typical R_{ghe} control region/trajectory within the parameter space. (b) Example constant maximum dV_{ds}/dt trajectory. (c) Example constant maximum dI_d/dt trajectory.

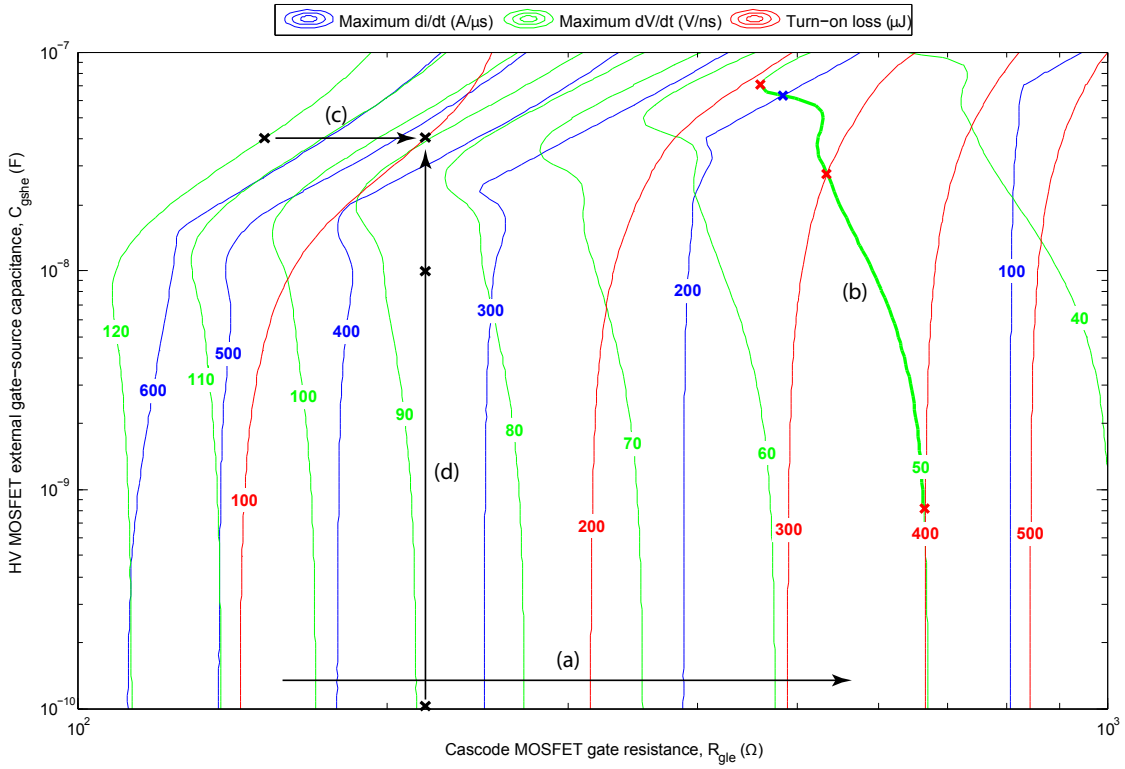

Fig. 6. Simulated switching performance surfaces for the cascode gate drive configuration over the (R_{gle}, C_{gshe}) parameter space. Plotted are contours of constant maximum dI_d/dt (blue), maximum dV_{ds}/dt (green) and turn-on switching loss (red). (a) Typical R_{gle} control region/trajectory within the parameter space. (b) Example constant maximum dV_{ds}/dt trajectory. (c) Example R_{gle} trajectory within the parameter space. (c) Example C_{gshe} trajectory within the parameter space.

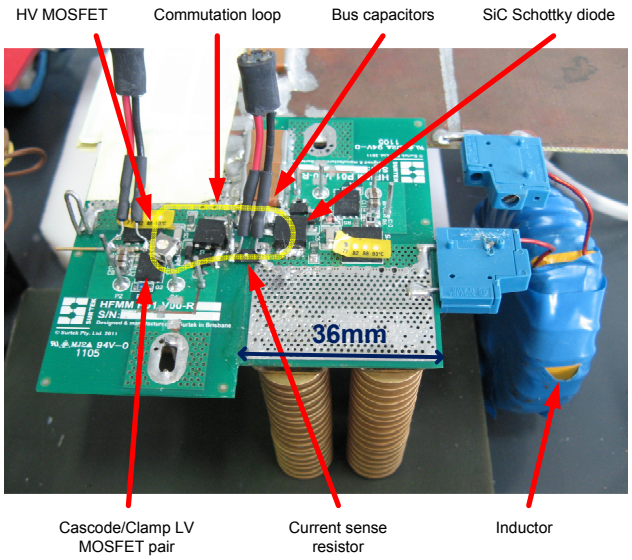

Fig. 7. Experimental prototype of the cascode MOSFET gate driver showing key components and the load current commutation loop.

V. Experimental Exploration of the Cascode Gate Drive Parameter Space

A. Hardware prototype

The cascode drive configuration was implemented in hardware (see fig. 7) using the same power MOSFET as used in the exploration of the gate drive parameter space by simulation. A 600V SiC Schottky diode was used for the clamping diode. Due to physical constraints it was necessary in the hardware prototype to drive the high-voltage MOSFET in the high-side position and place the opposing clamping diode in the low-side position. Measurements were then referenced to the half-bridge output rather than the bottom of the bus. Care was taken to ensure that stray capacitances to ground were minimised. A 0.1Ω current sense resistor was introduced between the high- and low-side devices to measure the current.

An inductor was used to provide the load current during the switching transient and a double-pulse switching pattern was used to investigate the turn-on switching transients of the cascode drive configuration. The prototype was tested under the same operating conditions as used in the exploration of the parameter space by simulation.

A 500Ω surface-mount single turn potentiometer was used to set the cascode MOSFET gate resistance. Additional gate-source capacitance could be added to the high-voltage MOSFET by fitting additional external ceramic capacitors. The load current for each test was set by selecting appropriate timing for the double-pulse waveform.

B. Methodology

Double-pulse tests were performed in order to investigate the switching performance of the hardware prototype in an inductive clamped switching application. An experimental exploration of the gate drive parameter space was conducted by changing the values of the externally added cascode MOSFET gate resistance and high-voltage MOSFET gate-source capacitance. Additionally the switching performance was recorded over a range of load currents from 1-10A. Table II provides a summary of the test conditions over which the experimental investigation was performed.

Parameter	Value
Bus voltage, V_{bus}	400V
HV MOSFET drive voltage, V_{drh}	12V
Cascode MOSFET drive voltage, V_{drl}	5V
Load current, I_L	1-10A
Cascode MOSFET gate resistance, R_{gle}	152Ω, 222Ω
HV MOSFET gate-source capacitance, C_{gshe}	100pF, 1nF, 2nF, 4nF, 10nF, 20nF, 40nF

TABLE II. Test conditions for experimental exploration of cascode gate drive parameter space.

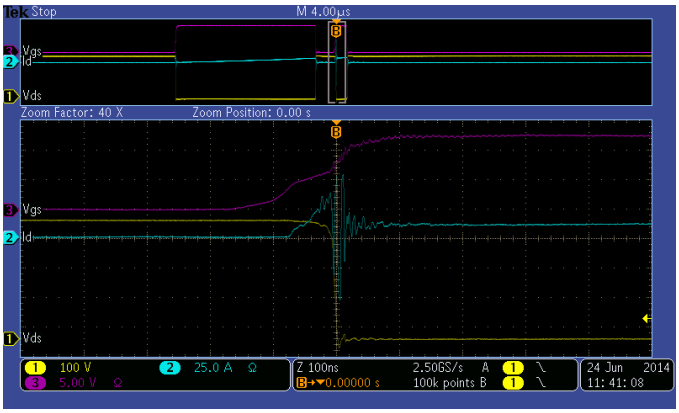

Fig. 8. Example double pulse switching waveforms recorded during the experimental exploration of the cascode gate drive parameter space. Shown are the drain-source voltage of the HV-cascode pair (CH1, 100V/div), drain current of the HV MOSFET (CH2, 25A/div) and gate-source voltage of the HV MOSFET (CH3, 5V/div).

The drain-source voltage was measured using a 500Mhz 10x passive probe. The gate-source voltage and voltage across the current sense resistor were measured using 500MHz high-voltage differential probes. Traces were recorded for the entire double-pulse waveform at a 2.5GHz sample rate with a 16x averaging acquisition mode. An example oscilloscope trace recorded from the experiment is shown in figure 8; the upper window shows the entire double-pulse waveform, while the lower window shows the turn-on transient of interest, corresponding to the B-trigger point in the waveform.

Raw data collected from the experimental test were subsequently post-processed to extract the features of interest from the waveform data. Firstly, the voltage measured across the current sense resistor was filtered to remove the contribution from the parasitic series inductance; a first order low-pass filter tuned for a 2nH series inductance was applied to reconstruct the true current. Secondly, the sampled oscilloscope data was smoothed using a Savitzky-Golay filter in order to extract the dV/dt and di/dt metrics. A 9th order filter with window length of 71 points (corresponding to 28.4ns) was applied to the voltage traces. A lower order filter with longer widow length was used to extract the di/dt metrics in order to reject the high-frequency ringing observed in the current waveform whilst capturing the lower-frequency information of interest; a 4th order filter with window length of 151 points (60.4ns) was used for this purpose.

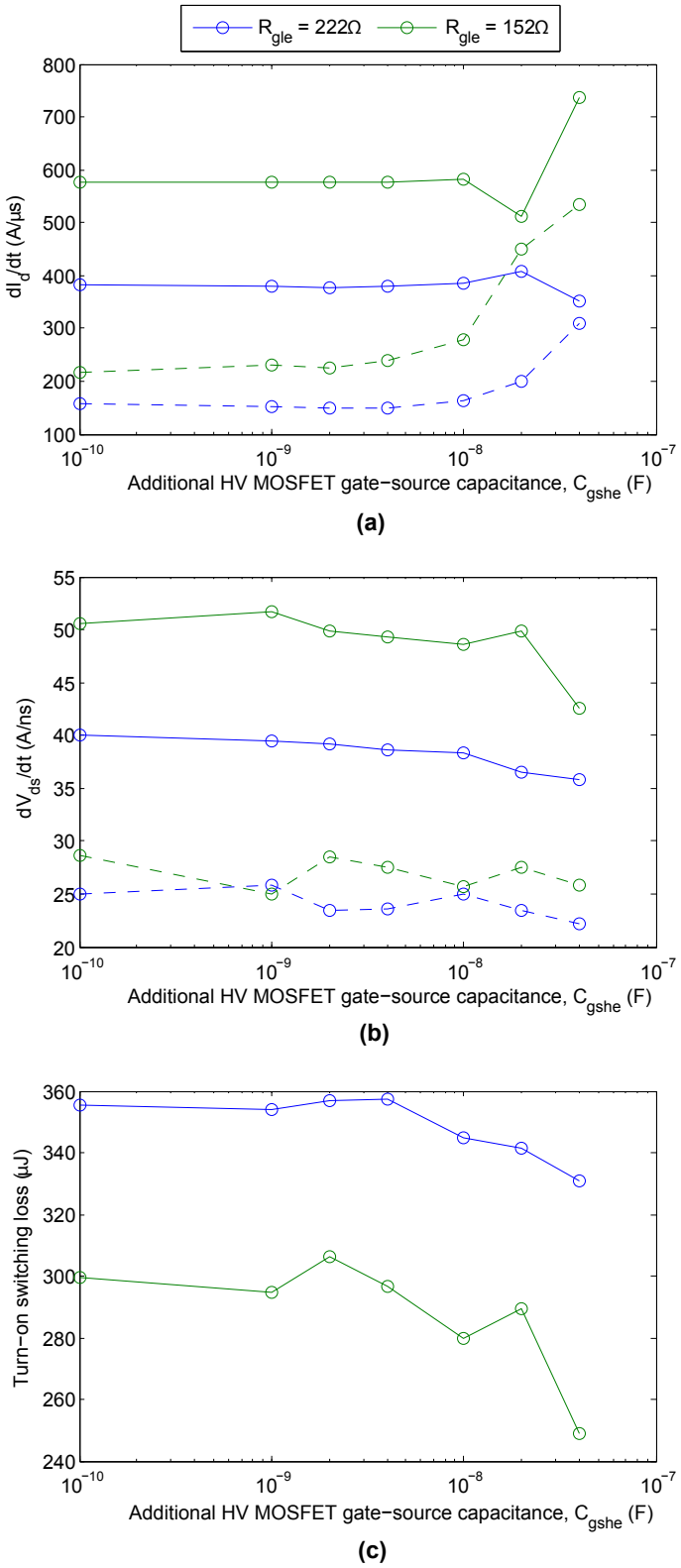

Fig. 9. Experimental switching characteristics of the cascode gate drive configuration as a function of gate-source capacitance added to the HV MOSFET, C_{gshe}. Results are shown for a fixed value of I_L = 10A. (a) Average (dashed) and maximum (solid) rate-of-change of drain current, dI_d/dt. (b) Average (dashed) and maximum (solid) rate-of-change of drain-source voltage, dV_{ds}/dt. (c) Turn-on switching losses.

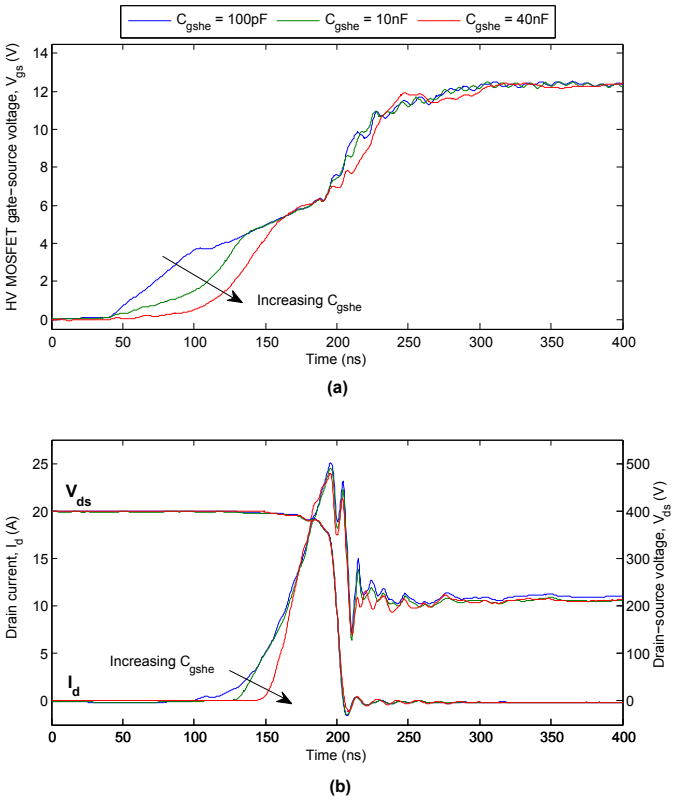

Fig. 10. Turn-on transient waveforms for the cascode gate drive configuration operating with a fixed gate resistance, $R_{gle} = 152\Omega$, and a load current of 10A. Traces are plotted for C_{gshe} values of 100pF (blue), 10nF (green) and 40nF (red). (a) Gate-source voltage, V_{gs}, waveform. (b) Drain current, I_d, and drain-source voltage, V_{ds}, waveforms.

A number of metrics were extracted from each test including maximum and average dV/dt, maximum and average di/dt, 10-90% rise/fall times, total switching time and switching energy (loss).

C. Results

Key results of the experimental exploration of the cascode gate drive parameter space are summarised in figures 9 through 12. Figure 9 shows the experimental performance of the cascode drive configuration as a function of C_{gshe} for each tested gate resistance and at a fixed load current of 10A. In figure 9a it can be seen that maximum di/dt remains relatively constant for a given value of gate resistance. As the capacitance is increased, however, the average di/dt increases, approaching the maximum di/dt for higher capacitance values.

Maximum dV/dt tends to decrease with increasing gate-source capacitance, however, changes are marginal, typically within 10% (see fig. 9b). It can be observed from figure 9c that switching losses tend to decrease with increasing gate-source capacitance, which can be attributed to the increase in average di/dt. For the 152Ω case a decrease in switching losses of almost 20% is observed over an increase in the gate-source capacitance form 100pF to 40nF. It should be noted that adding 40nF to the gate would add approximately 3μJ to the gate drive losses, but this is more than offset by the approximately 50μJ reduction in switching losses.

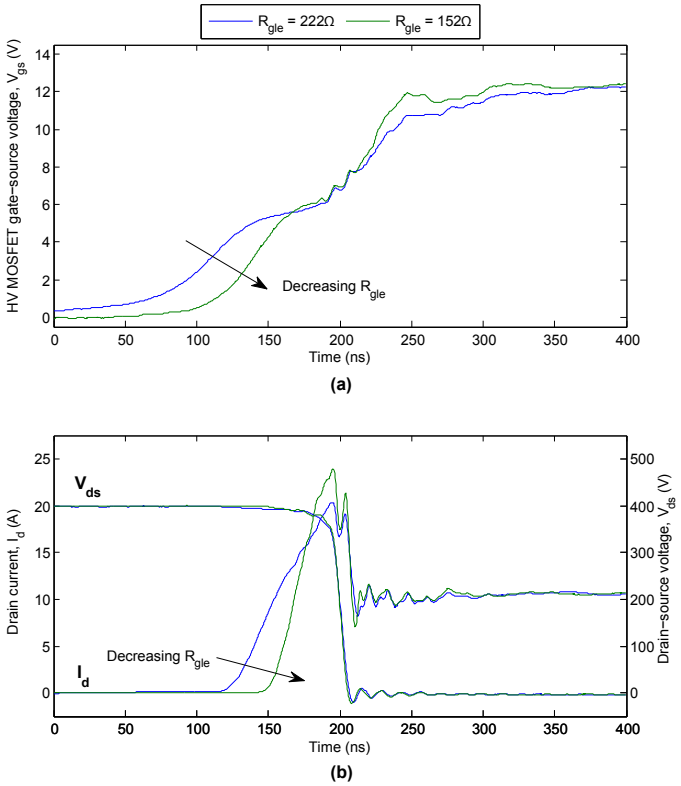

Fig. 11. Turn-on transient waveforms for the cascode gate drive configuration operating with a fixed additional gate-source capacitance, $C_{gshe} = 40nF$, and a load current of 10A. Traces are plotted for R_{gle} values of 222Ω (blue) and 152Ω. (a) Gate-source voltage, V_{gs}, waveform. (b) Drain current, I_d, and drain-source voltage, V_{ds}, waveforms.

Corresponding transient waveforms are presented in figures 10 and 11. The effect of increasing gate-source capacitance is clearly evident in figure 10b, with the current transition time decreasing and appearing to become closer to linear with increasing capacitance. Very little change in the voltage fall characteristics are evident in this plot. It is also worth noting in figure 10a that the charging time of the gate is substantially reduced with increasing capacitance. Also note the difference in the gate waveform compared with a conventional gate drive waveform: long charging delays are eliminated and no Miller plateau is evident. In the fastest case the gate is charged to full enhancement within approximately 150ns. The effect of decreasing cascode MOSFET gate resistance is presented in figure 11. A reduction in the current rise time, voltage fall time and gate-source voltage rise time can be observed with decreasing gate resistance.

Figure 12 shows the experimental performance of the cascode gate drive as a function of load current. As expected there is a strong relationship between load current and switching losses (see fig. 12c). The effect of load current on the maximum di/dt and maximum dV/dt metrics is less apparent, and different for the two tested gate resistance values. In general, however, the worst case maxima appear to coincide with the higher load current values. This is potentially an important characteristic for designers as it allows driver design to be carried out for the peak current, worst case scenario.

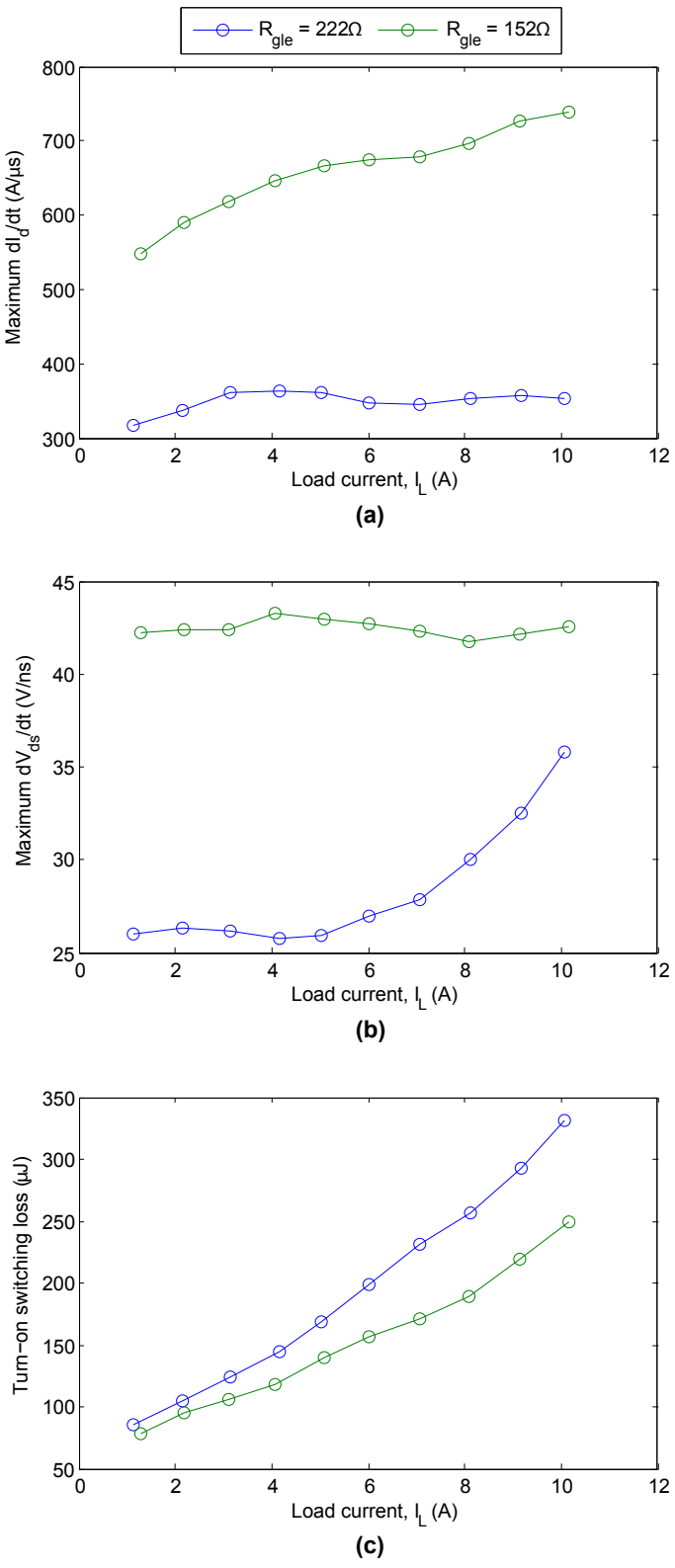

Fig. 12. Experimental switching characteristics of the cascode gate drive configuration as a function of load current, I_L. Results are shown for a fixed value of C_{gshe} = 40nF. (a) Maximum rate-of-change of drain current, dI_d/dt. (b) Maximum rate-of-change of drain-source voltage, dV_{ds}/dt. (c) Turn-on switching losses.

Compared with the simulated result surfaces, the experimental results, in general, exhibit significantly increased switching times, and hence, reduced maximum di/dt and dV/dt for a given region of the parameter space. This result is most likely attributed to the exclusion of parasitic elements (particularly parasitic inductances) from the simulation circuits. The use of an ideal clamping diode in the simulations also results in significantly shorter switching times as the device under test is not required to discharge the junction capacitance of the diode. The high current overshoot observed in the transient waveforms (figures 10 and 11) is due to discharge of the diode parasitic capacitance as well as auxiliary RC snubber circuits present on the prototype hardware. While the magnitude of the values for the switching performance metrics differ between the simulated and experimental results, the general characteristics elucidated by the exploration of the parameter space by simulation were borne out by the experimental results, namely, the effect of increasing the gate-source capacitance.

VI. Conclusion

The cascode gate drive parameter space has been explored via both simulation and experimentation, elucidating a number of key features of the cascode switching process. The addition of gate-source capacitance external to the high-voltage MOSFET provides a second degree of freedom, allowing independent control of key switching performance metrics including maximum dV/dt, maximum di/dt and switching loss. Comparison with the simulated result surfaces for the conventional resistor-fed gate drive has shown the cascode drive provides unique characteristics and opportunities to optimise switching.

The ability to reduce switching losses by increasing the high-voltage MOSFET gate-source capacitance is of particular interest. It has been validated experimentally that increasing the gate-source capacitance increases the average di/dt towards the maximum di/dt during the turn-on switching transient. Reductions in switching losses approaching 20% have been demonstrated via this mechanism.

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