Mitigation of Motor Overvoltage in SiC-Device-Based Drives using a Soft-Switching Inverter

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***Abstract*—In SiC motor drives, the high-voltage slew rate (dv/dt) of switching transients results in excessive motor overvoltage, due to the reflected wave phenomenon (RWP), which stands behind the premature failure of motor winding insulation while raises electromagnetic interference (EMI) problems. This paper adopts a soft-switching inverter topology, denoted as the auxiliary resonant commutated pole inverter (ARCPI), to mitigate the motor overvoltage caused by the RWP in SiC-based cable-fed drives. The performance of the SiC motor drive system under the RWP is first investigated to determine how the motor overvoltage is affected by the dv/dt of the inverter output voltage and the cable length. Then, a SiC ARCPI with profiled output voltage slew rate is utilized as a candidate solution to mitigate the RWP in the cable-fed motor drive. The effectiveness of the presented mitigation approach is experimentally verified, where it is shown that the ARCPI can completely eliminate the motor overvoltage and improve the EMI performance at high frequency region (500 kHz onwards) due to the prolonged rise/fall time of the output voltage, compared with the conventional hard-switching inverter.**

***Keywords*—Auxiliary resonant commutated pole inverter (ARCPI), high dv/dt, motor drives, reflected wave phenomenon, SiC MOSFET, soft-switching inverter.**

I. Introduction

Adjustable speed drives (ASDs) are expecting significant performance improvement with the adoption of wide bandgap (WBG) devices, such as silicon carbide (SiC) MOSFETs, due to their superior characteristics including faster switching speeds and elevated temperature and voltage capabilities [1]. Among these advantages, the fast switching speed plays a crucial role in reducing the switching losses and increasing the switching frequencies [2]. As a result, using SiC MOSFETs in ASDs can significantly improve the system efficiency, control accuracy and dynamic response as well as reducing the torque ripple, when compared with Si-based counterparts [3].

However, the fast switching speed results in high-voltage slew rate (dv/dt) which causes excessive overvoltage oscillations across the motor terminals in cable-fed drives as experimentally shown in Fig. 1, where v_s and v_m are the inverter output voltage and the motor voltage, respectively [4]. Such a phenomenon is known as the reflected wave phenomenon (RWP) which is conceptually similar to wave propagation in transmission lines [5]. In ASDs, the motor and the inverter are often placed in different locations where power cables are used to provide the PWM voltage pulses from the inverter to the motor [6]. The characteristic impedance of the cable is generally smaller than that of the motor, where the former is in the range of 20 Ω to 120 Ω, while the latter is much higher and typically ranges between 500 Ω and 4000 Ω depending on the motor power rating [7]. The impedance mismatch between the cable and motor results in voltage reflection causing overvoltage oscillations at the motor terminal [8]. Theoretically, the maximum voltage magnitude at the motor terminal can double the dc-bus voltage [8]. Furthermore, ASDs with higher switching frequencies and modulation indices can develop a greater than twice or even four times of the dc-bus voltage at the motor side [9]. This is denoted as the double pulsing effect, where a second voltage pulse is applied to the motor terminals before the first reflected pulse is fully decayed [9]. The resultant overvoltage caused by the RWP increases the possibility of partial discharges leading to an accelerated aging of the machine winding insulation and ultimate failure of the drive system [4]. In addition, the high frequency voltage oscillations at the motor terminal raise electromagnetic interference (EMI) problems [10].

Several possible approaches can be adopted to mitigate the RWP in SiC-based ASDs [4]-[9], [11]-[14]. The mainstream mitigation approach is employing filters to tackle the root cause of the RWP, i.e. the high dv/dt and the impedance mismatch. These filters can be generally categorized into dv/dt filters [11] and impedance matching filters [12]. The dv/dt filters suppress the overvoltage by limiting the voltage slew rate

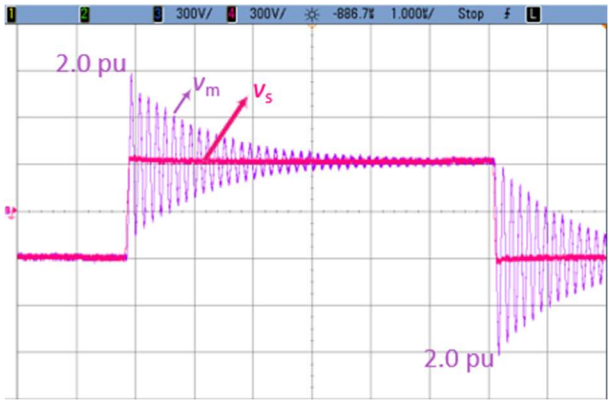


Fig.1. The reflected wave phenomenon in SiC-based motor drives [4].

applied to the system [11]. Whereas, the impedance matching filters reduce the overvoltage by including either an *RL* filter at the inverter side [12] or an *RC* filter at the motor side [13], or a combination of these two alternatives [5] to match the impedance between the cable and motor. However, the high dv/dt imposed by the SiC switching devices may interact with the parasitic inductance of the filter resistor causing high frequency impedance mismatch, which is a source of the second and the third load reflections causing higher peak motor voltage [12]. In addition, the filters have disadvantages such as bulkiness, additional power loss, and motor-control scheme variation [5]. Thus, designing a proper filter to mitigate the RWP for SiC-based ASDs is still challenging.

Another mitigation approach is the quasi-three-level (Q3L) PWM scheme which is realized by modifying the PWM voltage transition pattern based on the observation that the wave reflection can be cancelled by splitting the rising/falling edges into two equal-voltage steps separated by a proper dwelling time [4]. This approach can effectively mitigate the overvoltage across the motor terminal overcoming the filter's disadvantages. However, the motor windings still suffer from high dv/dt resulting in uneven voltage distribution across the motor turns, where the first several turns would endure higher voltage since this approach cannot flatten the voltage slew rate applied to the motor windings. Furthermore, the high dv/dt at the motor terminal will deteriorate the EMI performance, being the main source of the EMI in the ASD [10].

This paper presents a soft-switching inverter, i.e. the auxiliary resonant commutated pole inverter (ARCPI), to mitigate the RWP by reducing the inverter output voltage slew rate without sacrificing the beneficial attributes of SiC switching devices. The ARCPI was first proposed in the 1990s [15] and has become a popular soft-switching inverter topology due to its simple structure, high degree of PWM compatibility and independent phase control [16]. In addition, the ARCPI has the flowing benefits:

1) Low switching loss: the current and voltage of switching devices can be decoupled since the ARCPI is a soft-switching inverter [15], which reduces the switching loss in ASDs.

2) Profiled dv/dt: the output voltage fronts are smoothed in a sinusoidal manner since the inverter operates in a resonant mode [10]. Therefore, it can reduce the uneven voltage distribution across the motor windings and improve the EMI performance.

Accordingly, the ARCPI is employed in this paper to mitigate the RWP by slowing down the inverter output voltage slew rate. The rest of this paper is structured as follows: Section II presents the model of the RWP in ASDs and discusses the effect of the rise/fall time of the inverter output voltage on the RWP. Section III briefly describes the ARCPI and its principle of operation based on SiC devices. Section IV experimentally verifies the effectiveness of the ARCPI in the mitigation of the RWP. Finally, conclusions are drawn in Section V.

II. Modeling of the ASD and the RWP

A. Modeling of the ASD

Fig. 2 demonstrates the main components of a typical SiC-based ASD system which is composed of a dc power source, a voltage source inverter (VSI), a power cable, and an ac electric motor [17]. The VSI generates high-frequency PWM voltage pulses with a rise/fall time that is generally in the range of 10 ns to 100 ns depending on the switching device characteristics, load conditions and gate drivers [17]. With the high output voltage slew rate (dv/dt), the power cable behaves like transmission lines even at short lengths [8]. Therefore, the equivalent circuit of the ASD is illustrated as shown in Fig. 3, where the inverter is modelled as a PWM voltage source with an impedance of Z_s (typically $Z_s \approx 0$), the power cable is modelled as a lossless transmission line with an impedance Z_c, and the motor is represented by an impedance Z_m.

Referring to Fig. 3, the cable characteristic impedance Z_c is given as:

$$Z_c = \sqrt{\frac{L_c}{C_c}} \tag{1}$$

where L_c and C_c are the per-unit length inductance and capacitance, respectively [4].

The motor is equivalently modeled as an impedance Z_m which represents the stator winding leakage inductance in addition to the parasitic resistance and capacitance of the winding [18]. Therefore, in this paper, the motor model is considered as a three-phase load with fixed impedance, which is denoted as Z_m, as shown in Fig. 3.

B. Fundamentals of Voltage Reflection

In the ASD, the PWM voltage pulses generated by the VSI travel across the power cable in the same way of travelling waves on transmission lines due to the impedance mismatch between the power cable and the motor [12]. The propagation velocity v is calculated as a function of L_c and C_c, as:

$$v = \frac{1}{\sqrt{L_c C_c}} \tag{2}$$

Therefore, the propagation time τ from the inverter to the

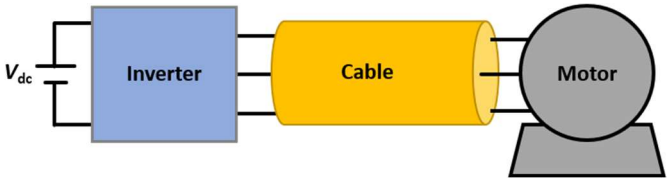


Fig. 2. Motor drive system with power cables.

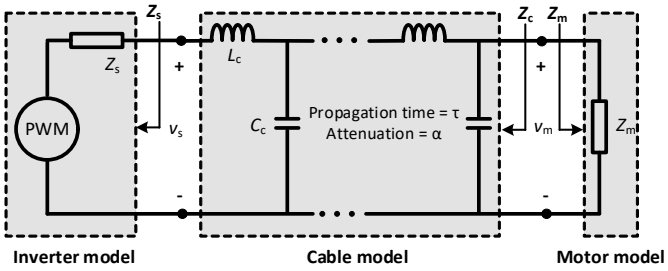


Fig. 3. The equivalent circuit of a motor drive system with power cables.

motor is a function of the cable length l and the cable per-unit length inductance L_c and capacitance C_c, as [4]:

$$\tau = l\sqrt{L_c C_c} \tag{3}$$

The voltage reflection process is depicted by the block diagram shown in Fig. 4, where the cable is represented by a block $\alpha e^{-\tau s}$, that is, the incident/reflected voltage is delayed by a time τ when travelling between the inverter and motor and is attenuated by a ratio α depending on the cable parameters [14]. Referring to Fig. 4, $V_{sn}^{x}(s)$ and $V_{mn}^{x}(s)$ are the frequency-domain voltages at the inverter side and the motor terminal, respectively, where $x = +$ or $-$, '+' denotes forward propagation while '$-$' denotes backward propagation, $n = 1, 2, 3 \ldots$ denotes the n^{th} propagation cycle.

The voltage pulse $U(s)$, i.e. the Laplace transform of v_s, generated by the inverter arrives the motor terminal after a propagation delay τ, and is then reflected due to the impedance mismatch between the motor and the cable. The delayed voltage $V_{m1}^{+}(s)$ and its reflected voltage $V_{m1}^{-}(s)$ are given by:

$$V_{m1}^{+}(s) = U(s)e^{-\tau s} \tag{4}$$

$$V_{m1}^{-}(s) = \Gamma_m V_{m1}^{+}(s) \tag{5}$$

where Γ_m is the the reflection coefficient at the motor side as given by [4]:

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{6}$$

In the ASD, the motor characteristic impedance Z_m is generally much higher than that of the cable Z_c, thus the reflection coefficient Γ_m is close to unity. Note that $\Gamma_m = 1$ means the voltage is fully reflected at the motor side.

After another propagation delay τ, $V_{m1}^{-}(s)$ arrives the inverter side and experiences a second reflection due to the impedance mismatch between the inverter and the cable. The delayed voltage $V_{s2}^{+}(s)$ and its reflected voltage $V_{s2}^{-}(s)$ are given by:

$$V_{s2}^{+}(s) = V_{m1}^{-}(s)e^{-\tau s} \tag{7}$$

$$V_{s2}^{-}(s) = \Gamma_s V_{s2}^{+}(s) \tag{8}$$

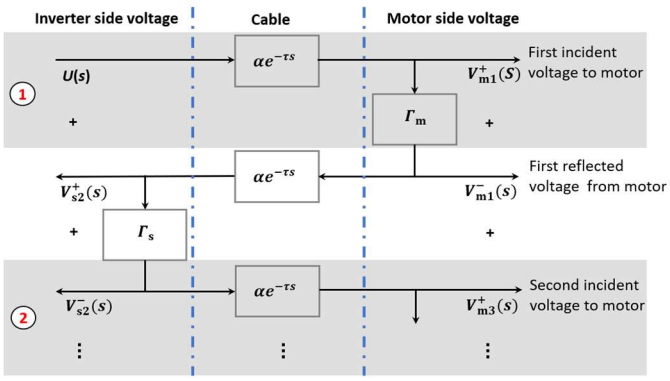


Fig. 4. A block diagram of the RWP.

where Γ_s is the the reflection coefficient at the inverter side, and is given as [4]:

$$\Gamma_s = \frac{Z_s - Z_c}{Z_s + Z_c} \tag{9}$$

Since $Z_s \approx 0$, Γ_s is close to -1. Note that $\Gamma_s = -1$ means the voltage is fully reflected at the inverter side with an inverted phase.

The voltage reflection process continues in the same manner until the motor terminal voltage is damped to the dc-bus voltage V_{dc}. By adding up the incident and reflected voltages at the motor side, the motor terminal voltage $V_m(s)$ can be expressed as [14]:

$$V_m(s) = \frac{U(s)(1+\Gamma_s)e^{-\tau s}}{1 - \Gamma_s \Gamma_m e^{-2\tau s}} \tag{10}$$

Fig. 5 shows the voltage waveform of a MATLAB simulation based on the block diagram depicted in Fig. 4, where the rise time is 20 ns, the dc-bus voltage is 500 V, the cable length is 10 m, the attenuation ratio is 0.9, and the reflection coefficients at the inverter and motor sides are -1 and 1, respectively. As can be noticed, the motor terminal voltage experiences high overvoltage oscillations due to the RWP.

C. Rise/Fall Time Effect on the RWP

In the ASD, in addition to the impedance mismatch between the cable and motor, the rise (fall) time t_r (t_f) of the inverter output voltage is another key factor that affects the motor overvoltage, where if $t_r \ll 3\tau$, a full voltage reflection will occur. In this case, the magnitude of the motor terminal voltage V_m is calculated as [19]:

$$V_m = (1 + \Gamma_m)V_{dc} \tag{11}$$

According to (6) and (11), the peak motor terminal voltage can be twice the dc-bus voltage.

If $t_r \gg 3\tau$, the peak motor terminal voltage can be calculated as [20]:

$$V_m = \left(\frac{3\Gamma_m l}{v t_r} + 1\right)V_{dc} \tag{12}$$

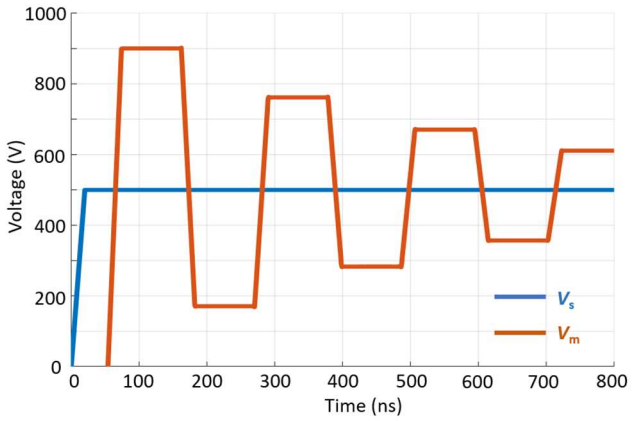


Fig. 5. Idealised waveforms of the inverter and motor voltages under RWP in ASDs.

The variation of the normalized peak motor terminal voltage with cable length and rise time is shown in Fig. 6. It can be noticed that as the rise time decreases, the motor overvoltage increases at the same cable length. Also, the critical cable length (at which the motor experiences a doubled voltage effect) decreases as the rise time is reduced. Thus, the motor overvoltage is more severe and common when fast switching SiC MOSFETs are used in ASDs.

III. The ARCPI and its Principle of Operation

As analyzed in Section II, increasing the rise/fall time of the inverter output voltage can effectively reduce the motor terminal overvoltage when the cable length is fixed. Therefore, this section adopts a soft-switching inverter, i.e. the ARCPI, to mitigate the motor terminal overvoltage caused by the RWP in the ASD since the output voltage waveform can be effectively profiled with controllable dv/dt rate by a resonant circuit [10].

Fig. 7 shows the circuit schematic of a single-phase leg SiC-based ARCPI, where a standard half bridge phase-leg (S_1 and S_4) is incorporated with an auxiliary resonant circuit between the output node A and the dc-bus middle point O [21]. The auxiliary resonant circuit is composed of two auxiliary switches (S_{a1} and S_{a4}), a resonant inductor (L_r) and two snubber capacitors (C_{r1} and C_{r4}). The three-phase ARCPI version is realized by adopting three phase-legs with auxiliary resonant circuits between the phase-legs middle points and the dc-bus middle point O [22].

A. Principle of Operation

Fig. 8 shows the gate signals waveforms, the currents of the main switches i_{S1} and i_{S4}, the resonant inductor current i_{Lr}, and the output voltage V_{pole} during switching transitions when the phase current i_{phase} is positive, where Fig. 8(a) elucidates the turn-ON process, while the opposite case is shown in Fig. 8(b) [10], [21], [22]. It is noted that the phase current I_{phase} is considered constant during the switching transitions.

Referring to Fig. 8(a), the turn-ON process can be divided into four intervals: the ramp up interval ($t_1 - t_3$), the resonant inverter ($t_3 - t_4$), the clamping interval ($t_4 - t_5$) and the post clamping interval ($t_5 - t_6$) [21], [22]. The switching transitions start with the auxiliary switch S_{a1} turning ON at t_1. During the ramp interval t_{ramp_on}, the resonant inductor current i_{Lr} ramps up to the prescribed trip current I_{trip} charging the resonant inductor L_r with sufficient energy for the imminent resonance process. Meanwhile, the outgoing main switch current i_{S4} ramps up from $-I_{phase}$ to $I_{trip} - I_{phase}$ at the same rate as i_{Lr} is ramping up, as shown in Fig. 8(a). Then the resonant interval starts when the main switch S_4 is turned OFF at t_3. During the resonant interval, L_r resonates with the two snubber capacitors C_{r1} and C_{r4} where they are charged and discharged in a sinusoidal manner, respectively. Thus, the output voltage V_{pole} swings from zero to V_{dc} in a resonant way until it is clamped by the antiparallel diode of the main switch S_1 at t_4. Then i_{Lr} starts ramping down while the voltage across the main switch S_1 is clamped to zero by its antiparallel diode. During the clamping period ($t_4 - t_5$), the switch S_1 can be turned ON under zero-voltage switching (ZVS). Afterwards, the post-clamping interval starts. The main switch S_1 starts conducting as soon as

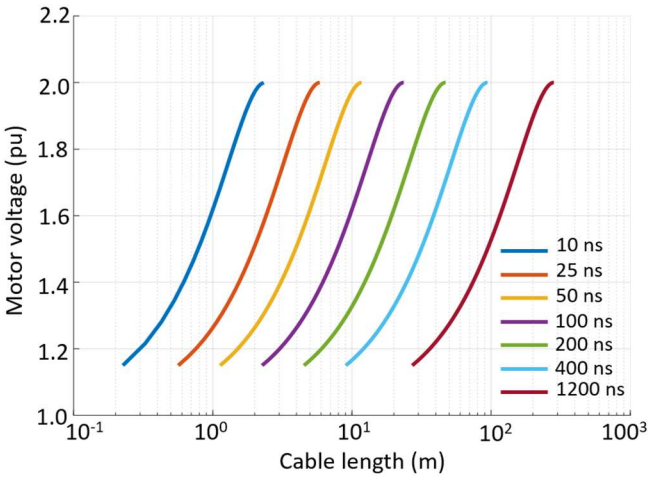


Fig. 6. Motor voltage at different cable length and rise time.

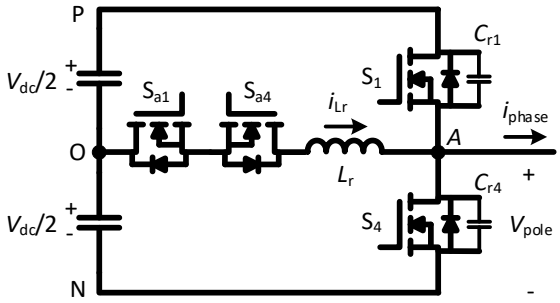


Fig. 7. A single-phase SiC-based ARCPI circuit.

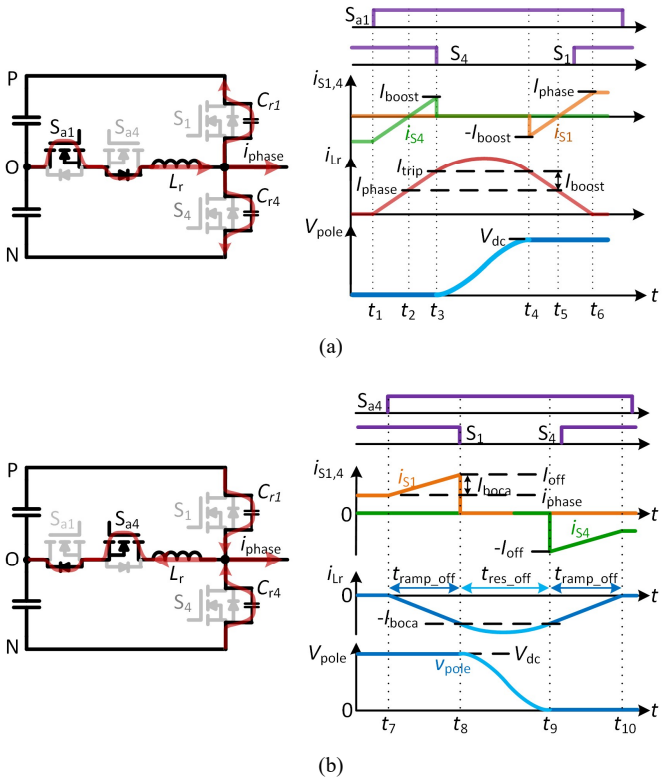


Fig. 8. The switching process of the ARCPI at positive phase current during (a) turn-ON (b) turn-OFF.

i_{Lr} falls below i_{phase}.

Referring to Fig. 8(b), the turn-OFF process can be divided into three intervals: the ramp up interval $(t_7 - t_8)$, the resonant inverter $(t_8 - t_9)$, the clamping interval $(t_9 - t_{10})$ [22]. The switching transitions start with the auxiliary switch S_{a4} turning ON at t_7. During the ramp interval t_{ramp_off}, the resonant inductor current i_{Lr} ramps down to the prescribed trip current $-I_{boca}$ charging the resonant inductor L_r with enough energy for the imminent resonance process. Meanwhile, the outgoing main switch current i_{S1} increases at the same rate as i_{Lr} is ramping down. Then the resonant interval starts when the main switch S_1 is turned OFF at t_8. During the resonant interval, L_r starts resonating with the two snubber capacitors C_{r1} and C_{r4} where they are discharged and charged in a sinusoidal manner, respectively. That is, the output voltage V_{pole} swings from V_{dc} to zero in a resonant way until it is clamped by the antiparallel diode of the main switch S_4. Then the main switch S_1 can be turned ON and the current diverts from its antiparallel diode to its channel. After S_1 conducts the phase current, the steady state is reached.

Overall, all the main switches of the ARCPI achieve ZVS and all the auxiliary switches achieve zero-current switching. The voltage and current of the main switches are decoupled and the output voltage waveform is smoothed and slowed down in a sinusoidal manner which is realized with the auxiliary resonant circuit [10]. Therefore, the ARCPI is promising in reducing the switching losses as well as the motor terminal overvoltage caused by the RWP in the ASD.

B. Equivalent Circuit of the ARCPI

Fig. 9 presents the idealized equivalent circuit of the ARCPI during the resonant process, where the initial conditions for the turn-ON process is represented by the red color, while the turn-OFF process is denoted by the blue color.

Considering the turn-ON process when the phase current I_{phase} is positive as an example, the ARCPI only performs quasi-resonant, where partial free oscillation is experienced. The resonant interval t_{res_on} can be calculated as [22]:

$$t_{res\_on} = \frac{2}{\omega_r}\tan^{-1}\left(\frac{V_{dc}}{2Z_r(I_{trip} - I_{phase})}\right) \quad (13)$$

where ω_r and Z_r are the resonant frequency and resonant impedance of the ARCPI, respectively, and are given as:

$$\omega_r = \sqrt{1/2L_rC_r} \quad (14)$$

$$Z_r = \sqrt{L_r/2C_r} \quad (15)$$

Likewise, during the turn-OFF process, the resonant inverter t_{res_off} can be calculated as [22]:

$$t_{res\_off} = \frac{2}{\omega_r}\tan^{-1}\left(\frac{V_{dc}}{2Z_r(|I_{boca}| + I_{phase})}\right) \quad (16)$$

It can be noted that for a given dc-bus voltage V_{dc} and load conditions i_{phase}, the resonant interval, i.e. the rise/fall time of the output voltage, is affected by the resonant circuit parameters L_r and C_r and its trip current. Therefore, by properly designing the resonant circuit parameters and the trip current, the output voltage can be profiled with slower output voltage edges, which can mitigate the RWP in ASDs.

C. ARCPI Design

In this sub-section, a design procedure for the ARCPI is presented. A case study for a three-phase 5 kW SiC ARCPI supplying an ac motor from a 500 V dc-link though 5 m long cable, is considered. The maximum modulation index is assumed to be 0.83, where such a circuit condition leads to the maximum load current I_{phase_max} =18 A.

1) Selection of the rise/fall time

Based on (12), the variation of the normalized peak motor terminal voltage with the rise time is shown in Fig. 10, where the reflection coefficient Γ_m is assumed to be unity which is the worst case for the ASD. It can be noticed that the maximum motor terminal voltage significantly decreases when the rise time of the output voltage is increased, specifically the maximum value is smaller than 1.15 pu when the rise time is greater than 0.2 µs. Since the rise/fall time of the output voltage also affects the high frequency response [10], to eliminate the motor terminal overvoltage while improving the system EMI performance, the rise/fall time of the inverter output voltage is selected as 1.2 µs.

2) Selection of the trip current

In the ARCPI, a smaller trip current is recommended since it

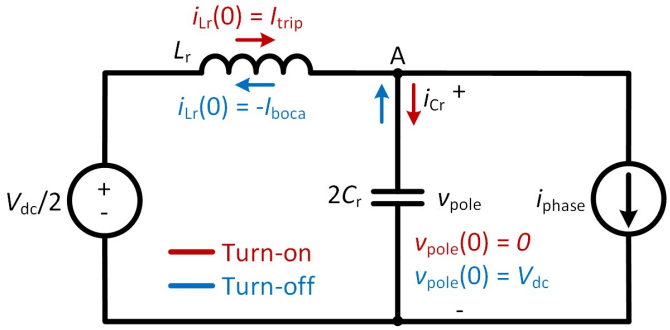


Fig. 9. The equivalent circuit of the ARCPI during the switching transitions.

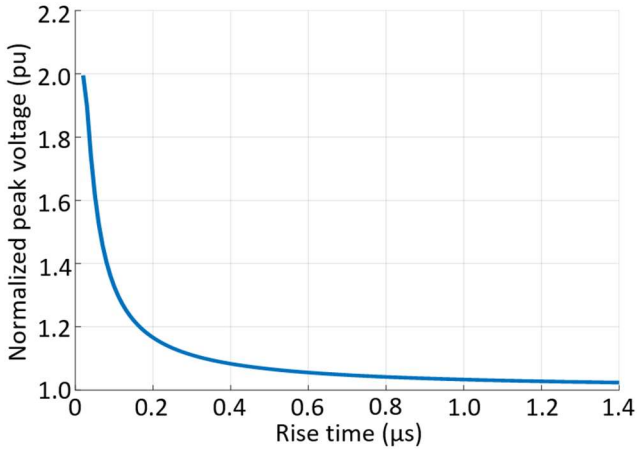


Fig. 10. The normalized peak voltage at different rise time when the cable length is 5 m.

can decrease the power loss and the current stress of the switching devices [10].

According to (13) and (16), the output voltage with the same rise and fall time can be achieved by meeting the following condition:

$$I_{\text{trip}} - I_{\text{phase}} = |I_{\text{boca}}| + I_{\text{phase}} \tag{17}$$

Therefore, the minimum trip current can be given as:

$$I_{\text{trip}} = I_{\text{phase\_max}} \tag{18}$$

$$I_{\text{boca}} = 0 \tag{19}$$

3) Selection of the resonant circuit parameters

According to the operation process in Section III, the resonant inductance can be designed as [22]:

$$L_{\text{r}} = \frac{V_{\text{dc}} t_{\text{ramp\_on}}}{4 I_{\text{phase\_max}}} \tag{17}$$

Therefore, when $t_{\text{ramp\_on}} = 400\text{ns}$, the resonant inductance is $L_{\text{r}} = 2.7$ μH based on (17), while the resonant capacitance C_{r} can be 47 nF based on (13)-(15).

IV. Experimental Results

In order to verify the proposed approach, a three-phase ARCPI based on Wolfspeed C2M0040120D SiC MOSFETs is used to supply a three-phase *RL* load ($R_{\text{phase}} = 22\ \Omega$ and $L_{\text{phase}} = 1.2$ mH) through 5 m long 12 AWG PVC cable, as shown in Fig. 11. It should be noted that the three-phase *RL* load is used to emulate the three-phase motor. The results are obtained under soft-switching operation of the ARCPI and are compared with the hard-switching case. The hard-switching inverter can be easily realized by removing the auxiliary circuit branch of the ARCPI. The SiC MOSFETs are driven using gate drivers with 25 Ω gate resistance. In this case, the switching time for the hard-switching inverter is nearly 50 ns. The inverter is supplied from 500 V dc-link and is controlled by a DSP (TI TMS320F28335) and an FPGA (XILINX XC3S400). The ARCPI is modulated using the fixed-timing control approach with 20 kHz and 50 Hz as the switching and fundamental frequencies, respectively. The hard-switching inverter is modulated with the SPWM with the same frequencies as the ARCPI. The experimental results are presented in Figs. 12-15.

Fig. 12 shows the load current of phase *A* (i_{phase}), the inverter output line voltage from phase *A* to phase *B* (v_{s}) and the line voltage at the load terminals (v_{m}) for two fundamental cycles. The experimental results for the hard-switching inverter are shown in Fig. 12(a) while the results for the ARCPI are shown in Fig. 12(b). As can be noticed, a significant overvoltage exists across the load terminals for the hard-switching inverter due to the RWP. In contrast, with the adoption of the ARCPI, the load terminal overvoltage is entirely mitigated.

Fig. 13(a) shows experimental results for one switching cycle of the hard-switching inverter. As can be noticed that the load terminal voltage oscillates in a damped manner, where the maximum overvoltage is ± 950 V for both the rising and falling edges. The high voltage oscillation is due to the RWP caused by the fast voltage slew rate (dv/dt) and the impedance mismatch, as previously analyzed. The enlarged view of this switching cycle during the falling and rising transitions are presented in Figs. 13 (b) and (c), where the rising and falling times are nearly 50 ns and the maximum load terminal voltage is 1.9 pu.

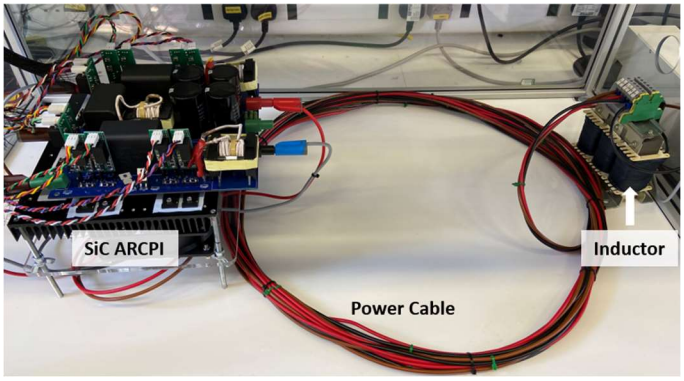
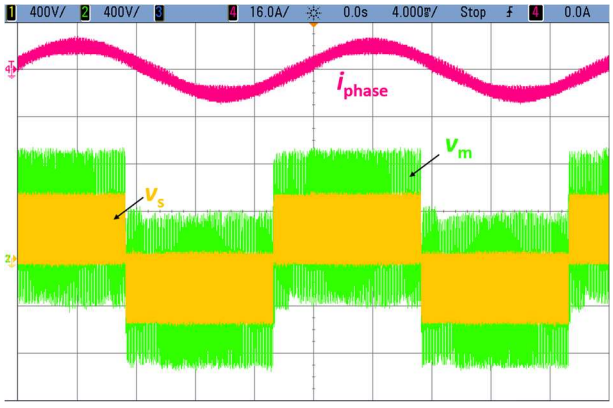
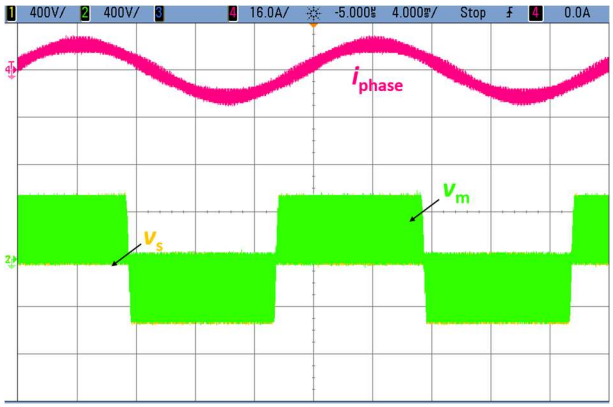


Fig. 11. The experimental setup.

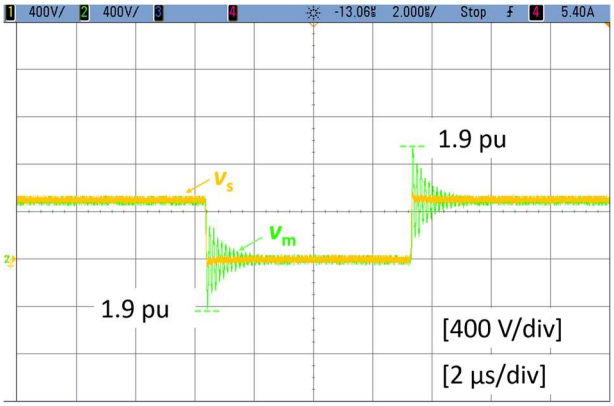


(a)

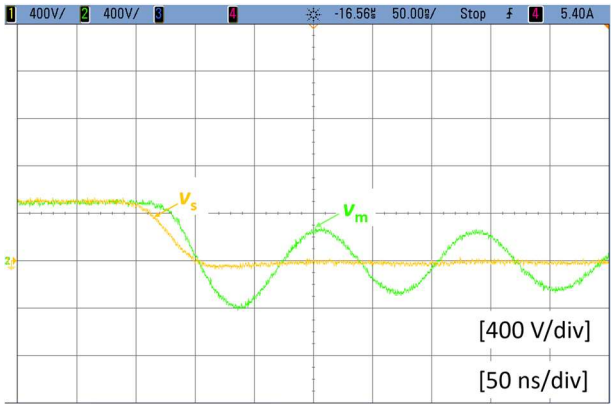


(b)

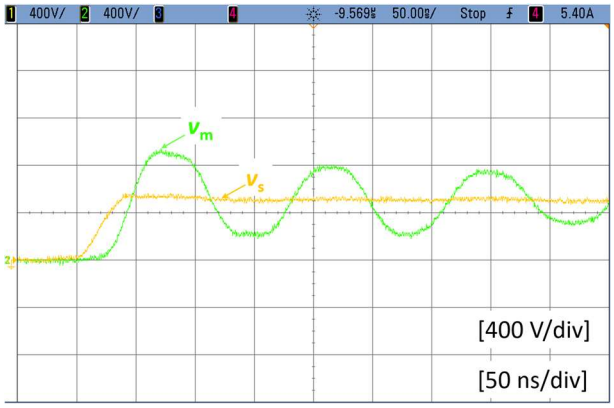
Fig. 12. Experimental results of the load current and inverter and load voltages using (a) a hard-switching inverter (b) the ARCPI.



(a)

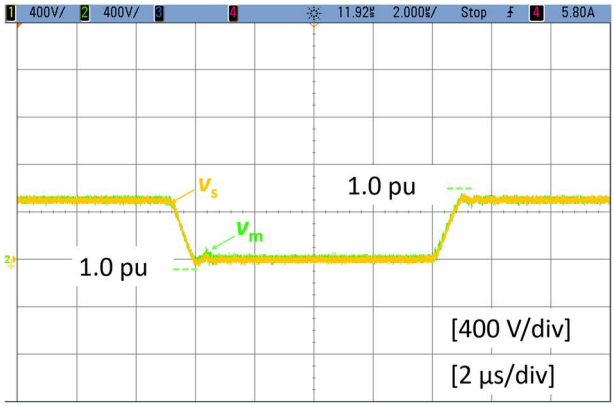


(b)

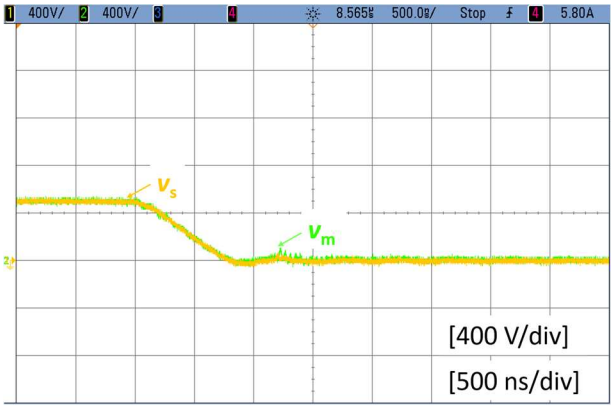


(c)

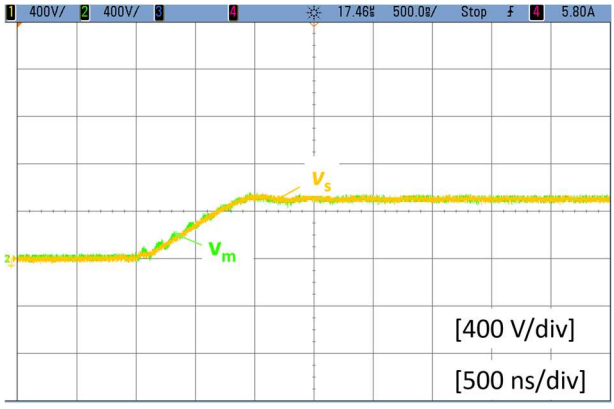
Fig. 13. Inverter and load voltages for the hard-switching inverter (a) one switching cycle view (b) extended view at falling edge and (c) extended view at rising edge.



(a)



(b)



(c)

Fig. 14. Inverter and load voltages for the ARCPI (a) one switching cycle view (b) extended view at falling edge and (c) extended view at rising edge.

With the adoption of the ARCPI, Fig. 14(a) shows one cycle of the inverter and the load voltages. As a result, the load voltage oscillation is eliminated due to the prolonged rise/fall time of the output voltage. This is highlighted in Figs. 14 (b) and (c) showing the enlarged view of this switching cycle during the falling and rising transitions, where the rising and falling times are about 1µs.

Fig. 15 shows the frequency spectrum of the load voltage under the hard-switching and the ARCPI. As can be noticed, using the ARCPI attenuates the high-frequency harmonics (500 kHz onwards). Specifically, 20 dBµV harmonic reduction can be achieved at 1 MHz using the ARCPI. The improvement in the EMI performance is due to the prolonged rise/falling times of the output voltage of the ARCPI as seen in Fig. 14, compared with that of the hard-switching inverter, as seen in Fig. 13. In addition, the high frequency voltage oscillations caused by the RWP, further deteriorates the EMI performance of the hard-switching inverter.

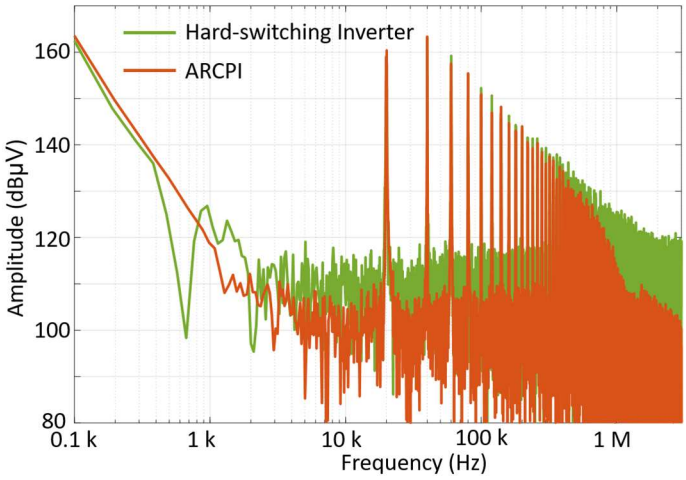


Fig. 15. Frequency spectrum of the load voltage using the hard-switching inverter and the ARCPI.

V. Conclusion

This paper has applied the ARCPI as a soft-switching inverter topology to mitigate the motor overvoltage in SiC-based cable-fed motor drives due to the RWP. The theoretical analysis shows that in addition to the impedance mismatch between the cable and the motor, the fast rise/fall time of the inverter output voltage affects the peak motor voltage when the cable length is fixed. The proposed approach tackles the RWP from the view of slowing down the inverter output voltage slew rate. The effectiveness of the ARCPI in mitigating the RWP is supported with experimental results. It has been shown that the ARCPI can completely eliminate the motor overvoltage and improve the EMI performance at high frequency region (500 kHz onwards) due to the prolonged rise/fall time of the output voltage, compared with the conventional hard-switching inverter.

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