Peer reviewed version

Link to publication record in Explore Bristol Research
PDF-document

Impact of Parasitics and Load Current on the Switching Transient Time and Motor Terminal Overvoltage in SiC-Based Drives

Wenzhi Zhou, Mohamed S. Diab and Xibo Yuan
Department of Electrical and Electronic Engineering
University of Bristol
Bristol, United Kingdom
wenzhi.zhou@bristol.ac.uk, mohamed.diab@bristol.ac.uk, xibo.yuan@bristol.ac.uk

Abstract—The fast switching speed of silicon carbide (SiC) MOSFETs has enabled converters to operate at higher switching frequencies with enhanced efficiencies, achieving performance improvement in motor drive systems. However, the high voltage slew rate (dv/dt) due to faster switching speeds results in excessive transient overvoltage at motor terminals, known as the reflected wave phenomenon (RWP). This paper systematically examines the motor terminal overvoltage in cable-fed SiC motor drive systems considering the effects of parasitic elements of SiC MOSFETs and load current during switching transitions. Starting with a half-bridge inverter, the switching transitions are analysed in detail and then extended to three-phase inverters. The theoretical and experimental results show that besides the rising edge of the inverter output waveform, the falling edge also affects the RWP depending on the load current polarity. Also, the motor terminal overvoltage has a non-uniform envelop which depends on the rise/fall switching times of the generated voltages of the SiC inverter, where these times vary with the load current due to the device parasitic capacitance.

Keywords—High dv/dt, long cable, motor drives, overvoltage, parasitics, reflected wave phenomenon, SiC MOSFET.

I. Introduction

The emergence of wide bandgap (WBG) power semiconductor devices, such as silicon carbide (SiC) MOSFETs, has led to rapid and transformative advances in power electronics [1]. Promoted by the WBG material characteristics, such as higher breakdown field and wider bandgap, SiC MOSFETs can operate at higher voltages, switching speeds, and operating temperatures than silicon (Si) IGBTs [2]. These characteristic enhancements make the SiC MOSFET a promising device choice in power converters feeding electric motors (EMs) in adjustable speed drives (ASDs) in applications such as automotive, railway and aerospace [3].

Although the fast switching speed has clear potential to reduce the switching loss and increase the switching frequency, it raises several undesired issues and technical challenges for both the inverters and motors [4-6]. One specific problem is the transient overvoltage across the motor terminals, known as the reflected wave phenomenon (RWP) [6]. The RWP is caused by high dv/dt voltage pulses travelling through power cables terminated by a motor that has significantly higher surge impedance than that of cables [6]. This issue is observed in Si inverter-fed drive systems only when the feeding cable is longer than 150ft [7]. The RWP, including the modelling and mitigation approaches, has been well studied for Si ASDs in the past decades [8-11]. For example, several graphical analysis methods such as snapshot and bounce diagram have been used to illustrate the RWP [8, 9]. Besides, mitigation approaches for the RWP including active and passive solutions have been proposed in the literature [10, 11].

With increased switching speeds and cable lengths, the motor terminal voltage can rise to twice or even four times of the dc-bus voltage [12]. The RWP is more pronounced in SiC inverter-fed motor drives, where the motor terminal voltage can be doubled with shorter cable lengths, compared to those used in equivalently rated Si-based drives, due to faster switching speed [13]. The consequent overvoltage induces undesired stress on motor windings, increasing the possibility of partial discharge while degrading the motor reliability and lifetime [6]. Therefore, studying the overvoltage phenomenon in SiC-based motor drives is essential to maximize the potential advantages of SiC MOSFETs and provide a useful reference for ASDs design.

Existing research investigates the RWP using the widely accepted double pulse test (DPT) based on a SiC half-bridge circuit, solely focusing on the rising transition of the output waveform [14, 15]. However, it is not the case for actual ASD systems where the motor is usually driven by either single-phase or three-phase inverters, that is, the output voltage waveform is different from that of the DPT circuit, being synthesized by the interaction of two phase-legs rather than only a single-phase (half-bridge) leg. Thus, the DPT may not sufficiently reveal how the motor drives operation is affected under RWP. The experimental results of the DPT may overestimate or underestimate the RWP and accordingly results in an inadequate design of drive systems.

Fig. 1 shows experimental results of the RWP in a SiC single-phase motor drive system where the motor terminal voltage (green signal, V_{motor}) unexpectedly has a non-uniform peak voltage envelop within one fundamental cycle. Since the peak reflected voltage ultimately depends on the rise/fall time of the incident voltage pulse, the rising and falling transitions of
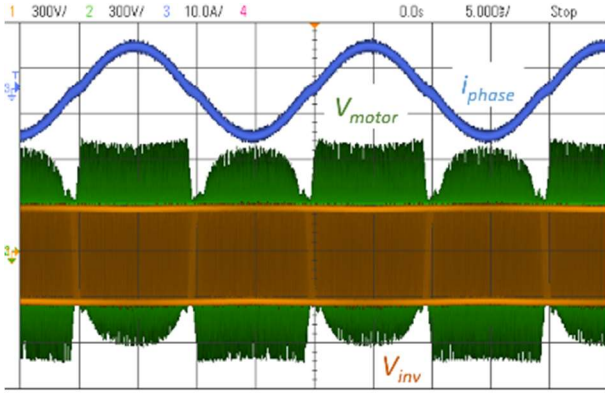
Fig. 1. Experimental result of the RWP in single-phase SiC-based motor drives.

each individual SiC device should be examined under different load current conditions to assess the parameters influencing the switching transitions. Further, the switching behaviour of the inverter is critical to design a proper overvoltage mitigation method, where for example, the quasi-three-level PWM scheme in [6] depends on the rise/fall time and the propagation time of incident voltage pulses.

This paper, therefore, systematically investigates the switching transitions and the influence of load current and parasitic elements of SiC MOSFETs on motor overvoltage transients due to the RWP. The rest of this paper is structured as follows. Section II briefly describes the RWP in SiC motor drives. Section III analyses the switching transition mechanism of SiC devices considering the effect of both load current and device parasitic capacitance in the half-bridge inverter, and then extends the analysis to three-phase SiC-based inverters being the mainstream industrial motor drives. Thereafter, experimental results are provided to validate the theoretical analysis in section IV. Finally, section V draws the paper conclusions.

II. MODELING OF THE REFLECTED WAVE PHENOMENON

A generic SiC-based ASD system consists of a dc source, a PWM inverter, a power cable, and an EM, as demonstrated in Fig. 2. The generated PWM pulses of the inverter propagate back and forth between the cable and the EM in the same way of travelling waves on transmission lines [16]. The characteristic impedance of the cable (Z_0) usually ranges between 20 Ω and 120 Ω [17]. By contrast, the EM equivalent impedance (Z_m) is always higher than that of the cable, which is in the range of 500 Ω to 4000 Ω depending on the motor power rating [17]. Due to the impedance mismatch between the power cable and the EM, the RWP occurs in the ASD system resulting in overvoltage oscillations at the motor terminal. The theoretical analysis of the RWP based on the transmission line theory has been well investigated and reported [8, 10, 11, 14]. Therefore, in this section, only a brief description of the RWP is given.

Fig. 3 depicts the voltage reflection process and the corresponding voltage waveforms at the inverter and the motor terminal, where it is assumed that the propagation time τ (in which the voltage pulse travels from one end of the cable to the other) is much longer than the rise/fall time t_r of the PWM
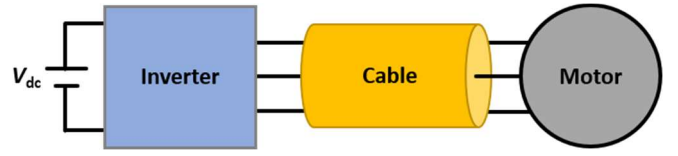

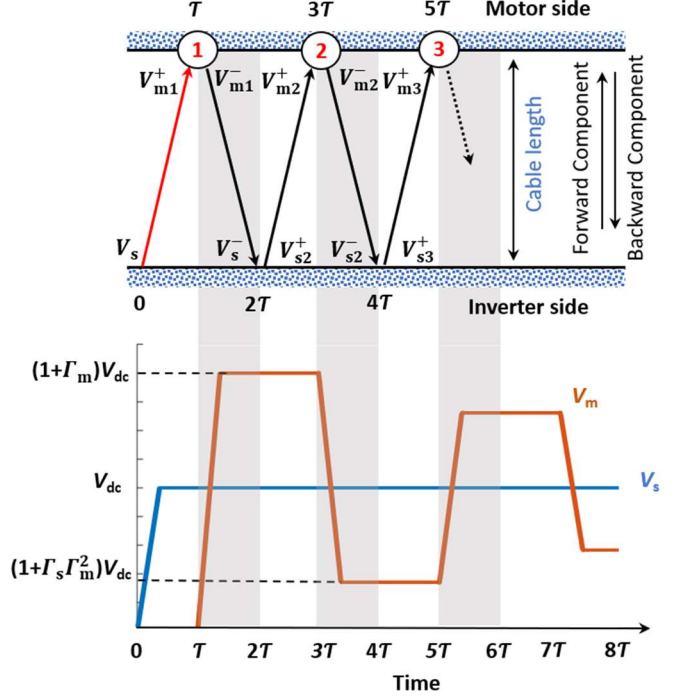Fig. 2. Motor drive system with power cables.

Fig. 3. A bounce diagram for voltage reflection in cable-fed ASDs and voltage waveforms at the motor and the inverter.

voltage pulse. The propagation time τ is given as:

$$\tau = l_c\sqrt{LC} \tag{1}$$

where l_c is the cable length while L and C are the per unit length inductance and capacitance, respectively.

Referring to Fig. 3, during the first interval ($t < \tau$), the leading edge of the PWM voltage V_s travels from the inverter to the motor, whereas the motor terminal voltage is 0 V. At the time τ, the PWM voltage arrives the motor side and experiences a voltage reflection back to the inverter. The reflected voltage V_{m1}^- can be given as:

$$V_{m1}^- = \Gamma_m V_s \tag{2}$$

where, Γ_m is the reflection coefficient at the motor side, which is determined by the cable surge impedance Z_c and the motor surge impedance Z_m, as

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \tag{3}$$

The cable surge impedance Z_c is given by:

$$Z_c = \sqrt{L/C} \tag{4}$$

Therefore, after one wave propagation cycle, the motor terminal voltage can be given as:

$$V_m(\tau) = (1 + \Gamma_m)V_s \quad (5)$$

When $t = 2\tau$, the reflected voltage V_{m1}^- arrives the inverter side where it experiences a forward voltage reflection to the motor side, as shown in Fig. 3. The reflected voltage V_{s2}^+ can be given as:

$$V_{s2}^+ = \Gamma_s V_{m1}^- \quad (6)$$

where, Γ_s is the reflection coefficient at the inverter side, which is determined by the cable surge impedance Z_c and the inverter surge impedance Z_s as:

$$\Gamma_s = \frac{Z_s - Z_c}{Z_s + Z_c} \quad (7)$$

At $t = 3\tau$, the incident voltage V_{s2}^+ arrives the motor side and experiences another backward voltage reflection to the inverter side. Therefore, the voltage at the motor terminal at $t = 3\tau$ is expressed as [14]:

$$V_m(3\tau) = (1 + \Gamma_s\Gamma_m^2)V_s \quad (8)$$

The voltage reflections continue until the voltage oscillations are damped to V_{dc}. The damping time depends on the ac skin resistance of the motor and cable, and the proximity effects in the cable.

According to the reflected waveform in Fig. 3, the oscillation frequency f_{rw} can be given by:

$$f_{rw} = \frac{1}{4\tau} \quad (9)$$

In addition to the reflection coefficients, the maximum overvoltage depends on the cable length and the rise/fall time of the voltage pulse generated by the inverter [7]. Since the peak motor voltage is affected by the rise/fall time of the PWM voltage, the following section analyzes the line voltage waveform at different switching transitions.

III. MODELLING OF SWITCHING TRANSITIONS

In the ASD system, the rise/fall time of the inverter voltage is one of the critical factors affecting the RWP when the cable length is fixed. This section analyses how the motor currents along with the parasitic capacitance of the SiC MOSFET, affect the switching transitions of the inverter's output voltage. The analysis is conducted for a half-bridge circuit, then extended for the three-phase inverter.

A. Switching Transitions of SiC MOSFETs in the Half-bridge Circuit

Fig. 4 shows the circuit schematic of the SiC half-bridge inverter employing two SiC MOSFETs (S_H and S_L) with their main parasitic elements namely, the drain-gate capacitance (C_{dg}), the gate-source capacitance (C_{gs}), and the drain-source capacitance (C_{ds}). The output current polarity is defined as positive when it flows out from the half bridge's midpoint (A), as shown in Fig. 4.

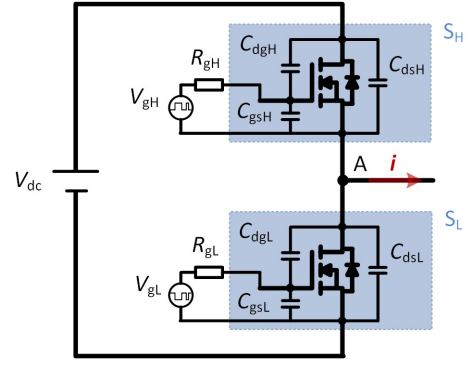Fig. 5 shows detailed switching transitions when the output

Fig. 4. The SiC-based half-bridge circuit.

current is positive, where Figs. 5(a)-(c) elucidates the turn-ON commutation from the lower switch (S_L) to the upper switch (S_H), while the opposite case is shown in Figs. 5(d)-(f).

Referring to Fig. 5(a), when the lower switch S_L is ON, the current flows through its channel instead of the freewheeling diode, where the SiC MOSFET works in "synchronous rectification mode". At a time instant t_1, S_L is turned OFF as the turn-OFF gate signal is applied to it, where the current starts to divert from the device channel to the antiparallel freewheeling diode, as shown in Fig. 5(b). In this case, the actual voltage across the lower switch V_{AN} keeps unchanged at zero. After a dead time t_{dead}, the turn-ON gate signal is applied to the complementary device S_H allowing the current to flow through its channel, as shown in Fig. 5(c). Meanwhile, the lower switch blocks the entire dc-link voltage, where V_{AN} equals V_{dc} at $t = t_2$, as shown in Fig. 5(c). It should be noted that the switching time for V_{AN} to traverse from 0 to V_{dc} is only governed by the gate resistance of the adopted gate driver. Since the switching speed is extremely fast (the rise time is within 10-100 ns), the rising edge of V_{AN} is denoted as a step edge, as shown in Fig. 6(a).

Considering the opposite commutation case, when S_L is turned ON and S_H is turned OFF, Fig. 5(d) shows the current path when the turn-OFF gate signal is applied to S_H at $t = t_3$, where the switch is instantly turned OFF. However, the voltage V_{AN} does not promptly decrease where the load current discharges the output capacitance of S_L while charges that of S_H. Thus, the voltage V_{AN} tardily decreases in a linear manner within a fall time t_{fall}, as given by:

$$t_{fall} = \frac{2C_{coss}V_{dc}}{I_{phase}} \quad (10)$$

where, $C_{oss} = C_{ds} + C_{gd}$ is the output capacitance of the SiC MOSFETs. The output capacitance of SiC MOSFETs can be considered as constant. Therefore, according to (10), the fall time depends on the instantaneous load current I_{phase}.

When the current fully discharges the output capacitance of S_L (see Fig. 5(e)), the voltage V_{AN} reaches 0 V and the current starts to flow through the antiparallel diode of S_L. After the deadtime t_{dead}, the turn-ON gate signal is applied to S_L, where the switch is turned ON and the current diverts from the antiparallel diode to the channel, maintaining V_{AN} at 0 V. Thus,
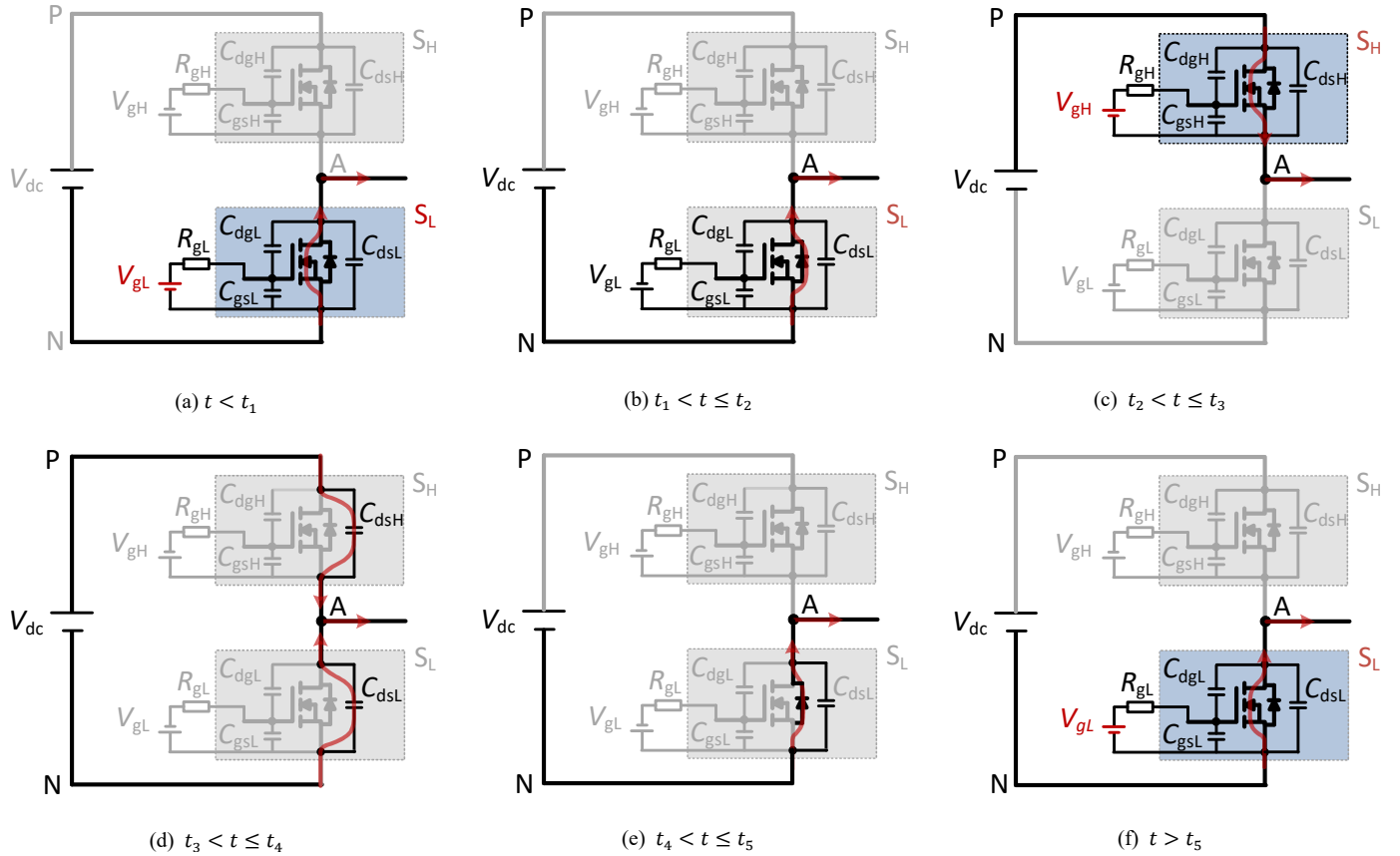
(a) $t < t_1$ (b) $t_1 < t \leq t_2$ (c) $t_2 < t \leq t_3$

(d) $t_3 < t \leq t_4$ (e) $t_4 < t \leq t_5$ (f) $t > t_5$

Fig. 5. Switching transitions of SiC half-bridge inverter.

during the turn-ON transition from S_H to S_L (interval t_3-t_5), the voltage waveform V_{AN} can be illustrated as shown in Fig. 6(a), where the falling edge of V_{AN} is denoted as a ramp edge.

Likewise, when the load current is negative, the switching transition can be obtained as shown in Fig. 6(b), where the rising edge is denoted as a ramp edge while the falling edge is denoted as a step edge.

Accordingly, when the output current is positive the falling edge of the voltage V_{AN} is influenced by the load current and the parasitic capacitance. Oppositely, when the current is negative, the rising edge of V_{AN} is affected by the load current and parasitic capacitance.

B. Line Voltages of Three-Phase SiC Inverter

Fig. 7 shows the three-phase SiC inverter-fed motor drive using power cables. Only the line voltage V_{AB} is analyzed since the switching mechanism of the three-phase voltages is the same. The line voltage V_{AB} can be given by:

$$V_{AB} = V_{AN} - V_{BN} \qquad (11)$$

Since V_{AB} is calculated as the difference between V_{AN} and V_{BN}, the switching transitions of V_{AB} depend on the relative polarities of the phase currents i_A and i_B. Within a fundamental cycle, the phase currents i_A and i_B can be classified into four regions, depending on the polarity of alternation, as shown in Fig. 8. The theoretical phase- and line-voltage waveforms at

different regions are depicted in Fig. 9. For brevity, the gate signals of the switching devices are not shown in Fig. 9.

Region I ($i_A > 0$, $i_B < 0$): the output voltage V_{AN} of phase A has a similar waveform with Fig. 6(a), the output voltage V_{BN} of phase B has a similar waveform with Fig. 6(b), and the duty cycle of V_{AN} is larger than that of V_{BN}. Therefore, the line voltage V_{AB} is synthesized as shown in Fig. 9(a), where the line voltage V_{AB} swings between 0 and V_{dc}. As can be noticed, the falling edge of the positive voltage pulses of V_{AB} are slower than the rising edges, being affected by the load current and the parasitic capacitance of SiC MOSFETs. The rising edge of V_{AB} results in the voltage swinging from 0 to V_{dc} and the falling edge of V_{AB} results in the voltage swinging from V_{dc} to 0. In this case, only the RWP caused by the rising edge of V_{AB} matters since the resultant overvoltage can exceed the design voltage level of the winding insulation. Accordingly, in this region, the RWP is only affected by the gate resistance.

Region II ($i_A > 0$, $i_B > 0$): both V_{AN} and V_{BN} have similar waveforms with Fig. 6(a). When the duty cycle of phase A is larger than that of phase B, the line voltage V_{AB} is positive, as shown in Fig. 9(b), where the line voltage V_{AB} swings between 0 and V_{dc}. Oppositely, when the duty cycle of phase A is smaller than that of phase B, the line voltage V_{AB} is negative, as shown in Fig. 9(c), where the line voltage V_{AB} swings between 0 and $-V_{dc}$. Common to both figures, one pulse of V_{AB} shapes like a rectangle and the other pulse shapes like a trapezoid. Thus, the

rising/falling edges of V_{AB} are affected either by the gate resistance or by the load current and parasitic capacitance of SiC MOSFETs. In this case, the RWP caused by the rising/falling edges can be either affected by the gate resistance or the load current and parasitic capacitance of SiC MOSFETs.

Region III ($i_A < 0$, $i_B > 0$): the output voltage V_{AN} of phase A has similar waveform with Fig. 6(b), the output voltage V_{BN} of phase B has similar waveform with Fig. 6(a), and the duty cycle of V_{AN} is smaller than that of V_{BN}. Therefore, the line voltage V_{AB} is synthesized as shown in Fig. 9(d), where the line voltage V_{AB} swings between 0 and $-V_{dc}$. As can be noticed, the rising edges of V_{AB} are slower than the falling edges, being affected by the load current and the parasitic capacitance of SiC MOSFETs. The rising edge of V_{AB} results in the voltage

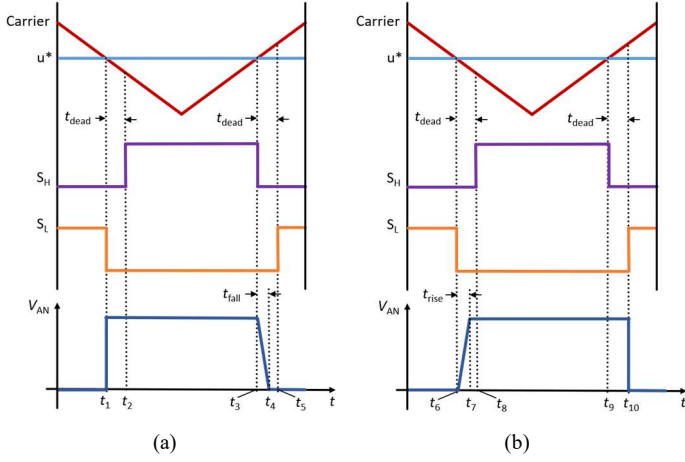(a)   (b)

(a)   (b)

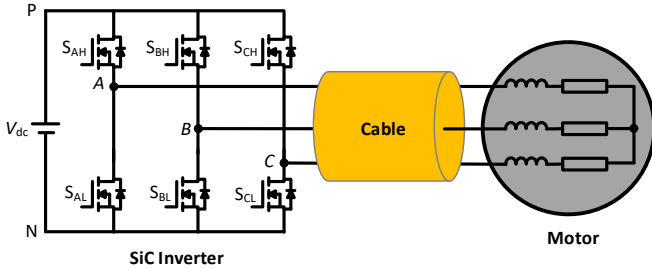Fig. 6. The output waveform of the half bridge inverter when the phase current is (a) positive and (b) negative.

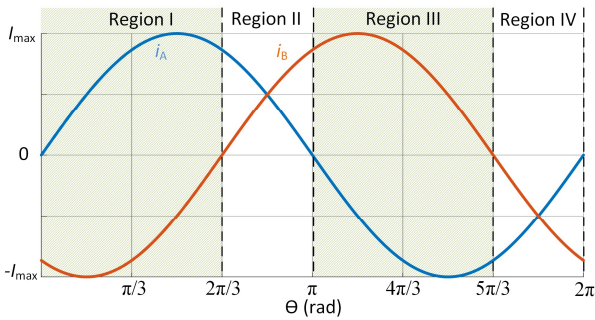Fig. 7. Three-phase SiC inverter-fed motor drive system.

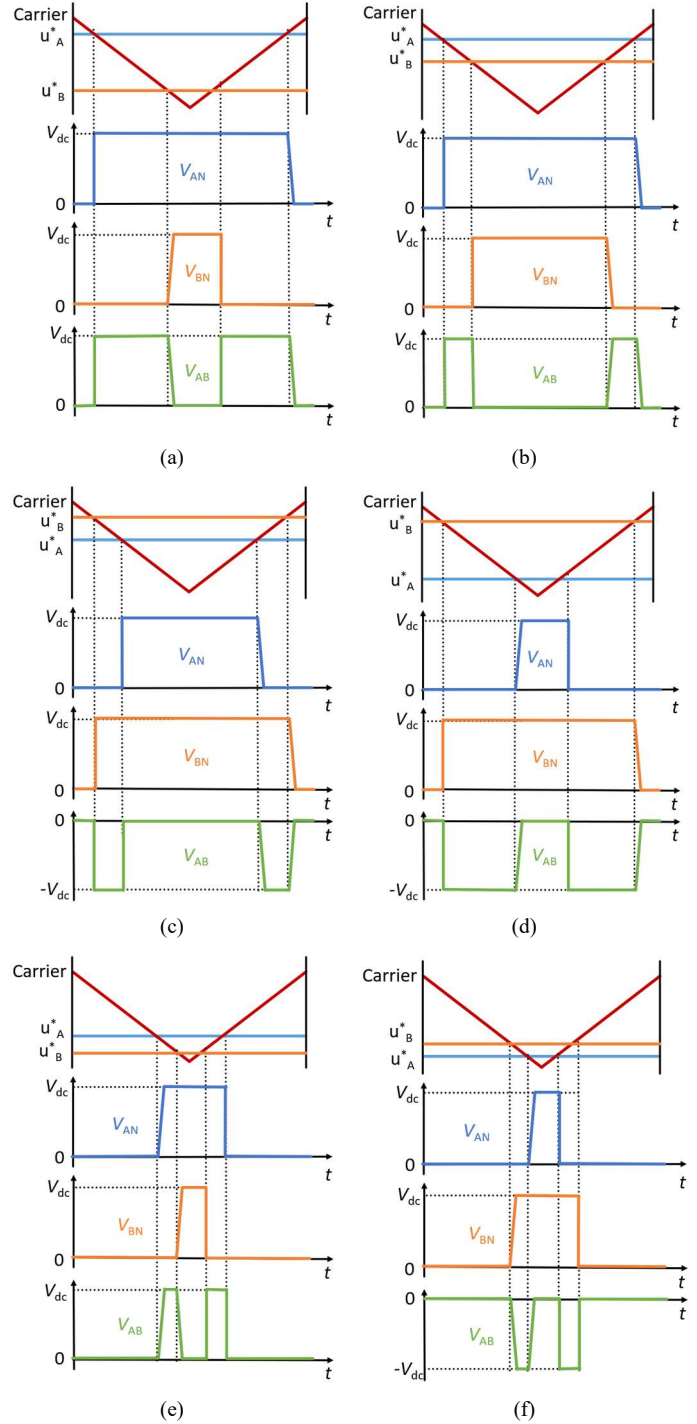Fig. 8. Classification of phase currents based on their polarities.

(c)   (d)

(e)   (f)

Fig. 9. Switching transitions of the line voltage V_{AB} in different region: (a) region I (b) region II and $V_{AN} > V_{BN}$ (c) region II and $V_{AN} < V_{BN}$ (d) region III (e) region IV and $V_{AN} > V_{BN}$ (f) region IV and $V_{AN} < V_{BN}$.

swinging from $-V_{dc}$ to 0 and the falling edge of V_{AB} results in the voltage swinging from 0 to $-V_{dc}$. In this case, only the RWP caused by the falling edge of V_{AB} matters since the resulted overvoltage impose higher voltage stress across the windings. Therefore, in this region, the RWP is affected by the gate resistance.

Region IV ($i_A < 0$, $i_B < 0$): both V_{AN} and V_{BN} have similar

waveform with Fig. 6(b). When the duty cycle of phase A is larger than that of phase B, the line voltage V_{AB} is positive, as shown in Fig. 9(e), where the line voltage V_{AB} swings between 0 and V_{dc}. Oppositely, when the duty cycle of phase A is smaller than that of phase B, the line voltage V_{AB} is negative, as shown in Fig. 9(f), where the line voltage V_{AB} swings between 0 and $-V_{dc}$. Common to both figures, one pulse of V_{AB} shapes like a rectangle and the other pulse shapes like a trapezoid. That is, the rising/falling edges of V_{AB} are affected either by the gate resistance or by the load current and parasitic capacitance of SiC MOSFETs. In this case, the RWP caused by the rising/falling edges can be either affected by the gate resistance or the load current and parasitic capacitance of SiC MOSFETs.

Accordingly, the output voltages of three-phase SiC inverter have different rise and fall times depending on corresponding phase current polarities and phase-leg duty cycles. Thus, the RWP is only pronounced at certain voltage transitions, where the rise/fall time is less than one third of the wave propagation time [7]. For a given three-phase ASD system, when the current polarity of phase A and phase B is different (Region I and Region IV), the RWP is only affected by the gate resistance. While, when the current polarity of phase A and phase B is the same (Region II and Region III), the RWP can be affected either by the gate driver or the load current and parasitic capacitance of SiC MOSFETs. Therefore, the conventional DPT, which only focuses on the rising edge of the output voltage, cannot be effectively used to reveal the RWP in three-phase inverter-fed motor drives. The RWP should be examined under different current load condition.

IV. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a three-phase inverter based on Wolfspeed C2M0040120D SiC MOSFETs is used as a laboratory prototype, as shown in Fig. 10. The SiC MOSFETs are driven by gate drivers with 25 Ω gate resistance. In this case, the rise time, where the switching device devise is turned ON, is about 51 ns. The inverter is supplied from 300 V dc-link and is controlled by a DSP (TI TMS320F28335) and an FPGA (XILINX XC3S400). The inverter is modulated using the well-known SPWM technique with 40 kHz and 50 Hz as the switching and fundamental frequencies, respectively.

As the focus of this paper is directed to the effects of parasitic elements of switches and load current on the RWP, the inverter is connected to 5 m power cables terminated by a three-phase RL load (R_{phase} = 11 Ω, and L_{phase} = 1.2 mH) to emulate the RWP in the ASD systems. It should be noted that the three-phase RL load cannot fully resemble the actual EM since it cannot emulate the capacitance between turn to turn and turn to case in the motor. However, the effects of load characteristics on RWP is beyond the scope of this paper. The effects of cable length and the characteristics of cable/load including the common mode impedance and differential mode impedance will be investigated on a proper designed setup in a dedicated paper in the future.

Fig. 11 shows the phase currents i_A and i_B, the inverter output line voltage V_{AB_Inv} and the load terminal line voltage V_{AB_Load} for two fundamental cycles. As can be noticed, a significant overvoltage exists across the load terminals due to the RWP.

However, the overvoltage does not have a uniform envelope due to the disparity in the rise and fall times of the generated voltage as a consequence of load current alternation, as previously analyzed. Fig. 12 shows a zoomed view of the obtained experimental results verifying the theoretical analysis of the line voltage waveform during region I (see Fig. 12(a)), region II (see Figs. 12(b) and (c)), region III (see Fig. 12(d)), and region IV (see Figs. 12(e) and (f)). It can be noticed that the experimental results show good agreement with the theoretical waveforms presented in Fig. 9.

As shown in region I (Fig. 12 (a)), the line voltage $V_{AB} > 0$ and the falling time of V_{AB} is about 125 ns which is 2.5 times longer than that of the rising time (50 ns). This is because the rising time is only affected by the gate driver and the falling time is affected by the load current and the parasitic capacitance of SiC MOSFETs, as analyzed in Section III. The fast rising time of V_{AB} results in a pronounced overvoltage across the load terminal. However, in region III (Fig. 12 (d)) the line voltage V_{AB} shows the opposite trend. As seen, the line voltage $V_{AB} < 0$ and the falling time is shorter (51 ns) than the rising time (121 ns). This is because in region III the falling time is only affected by the gate resistance and the rising time is affected by the load current and the parasitic capacitance of the SiC MOSFETs, as analyzed in Section III.
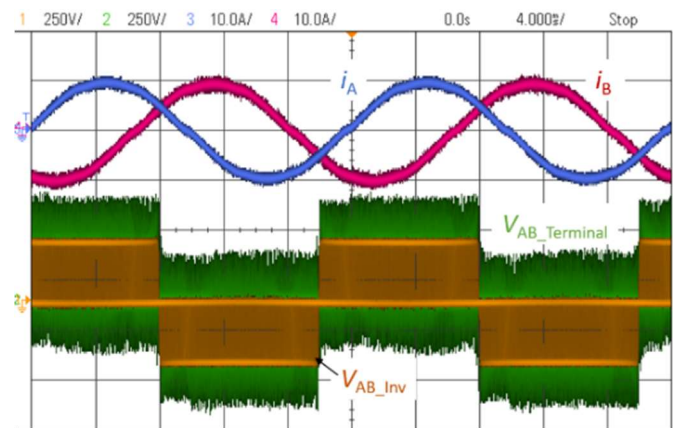

Fig. 10. The SiC inverter prototype.

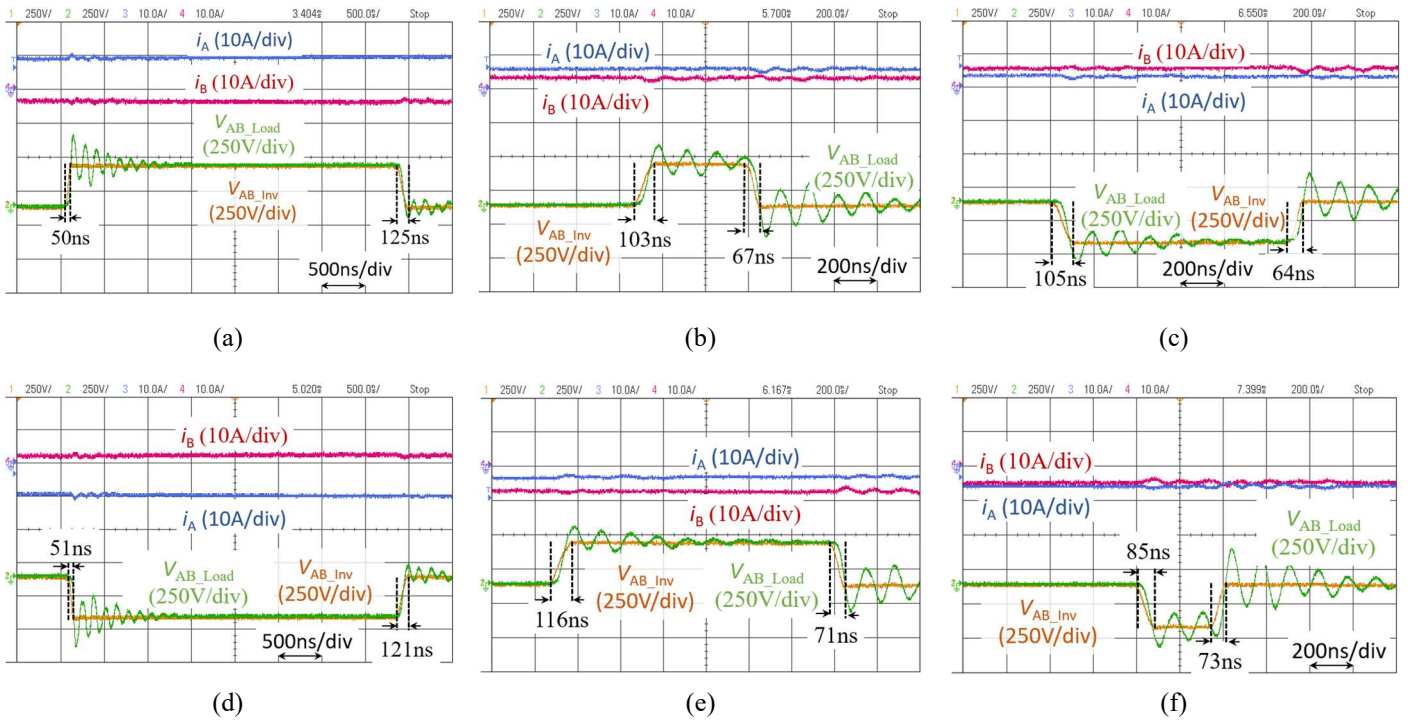Fig. 11. Experimental results of the phase currnts and the line voltage at the inverter side and load side.

Fig. 12. Experimental results of switching transitions of the line voltage V_{AB} of a three-phase SiC inverter supplying a three-phase load through power cables in different region: (a) region I (b) region II and $V_{AN} > V_{BN}$ (c) region II and $V_{AN} < V_{BN}$ (d) region III (e) region IV and $V_{AN} > V_{BN}$ (f) region IV and $V_{AN} < V_{BN}$.

Fig. 12 (b) shows the experimental results in region II when $V_{AN} > V_{BN}$. As can be noticed, the rising time and the falling time of V_{AB} are 64 ns and 105 ns, respectively. Both the rising time and falling time are longer than the switching time (50 ns) of SiC MOSFETs because both the rising and falling times are affected by the load current and parasitic capacitance of SiC MOSFETs. The discrepancy between the rising time and the falling time can be explained by (10) since the higher current will result in shorter transient time. Similar results can be observed when $V_{AN} < V_{BN}$ in region II, as depicted in Fig. 12 (c). As shown in Figs. 12 (e) and (f) in region IV, similar results can be observed. Both the rising time and falling time of V_{AB} are longer than the switching time (51 ns) of the SiC MOSFETs. The reason is both the rising and falling times are affected by the load current and parasitic capacitance of SiC MOSFETs

V. CONCLUSION

This paper has investigated the effects of load current and parasitic elements of SiC MOSFETs on motor terminal overvoltage due to the RWP. The theoretical analysis, supported with experimental verification, showed that the rise/fall times of the generated voltages of SiC inverters are varying depending on the load current value and device parasitic capacitance. The disparity in the rise/fall times of the generated voltages significantly affects the peak reflected voltage at the motor side due to the RWP in cable-fed drives. The results show that when the polarities of the phase currents are the same, the RWP is only affected by the gate resistance. Whereas, when the polarities of the phase currents are different, the RWP is affected either by the gate resistance or the load current value and device parasitic capacitance.

REFERENCES

[1] X. She, A. Q. Huang, O. Lucia, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, 2017.

[2] W. Zhou, X. Yuan, and I. Laird, "Performance comparison of the auxiliary resonant commutated pole inverter (ARCPI) using SiC MOSFETs or Si IGBTs," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2019, pp. 1981–1987.

[3] X. Yuan, "Application of silicon carbide (SiC) power devices: Opportunities, challenges and potential solutions," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 893–900.

[4] W. Zhou and X. Yuan, "Experimental evaluation of SiC MOSFETs in comparison to Si IGBTs in a soft-switching converter," *IEEE Trans. Ind. Appl.*, in press.

[5] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Evaluation of switching performance of SiC devices in PWM inverter-fed induction motor drives," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5701–5711, 2015.

[6] M. S. Diab and X. Yuan, "A quasi-three-level PWM scheme to combat motor overvoltage in SiC-based single-phase drives," *IEEE Trans. Power Electron.*, in press.

[7] P. Yi, P. K. S. Murthy, and L. Wei, "Performance evaluation of SiC MOSFETs with long power cable and induction motor," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–7.

[8] E. Persson, "Transient effects in application of PWM inverters to induction motors," *IEEE Trans. Ind. Appl.*, vol. 28, no. 5, pp.

1095–1101, 1992.

[9] A. Von Jouanne, D. A. Rendusara, P. N. Enjeti, and J. W. Gray, "Filtering techniques to minimize the effect of long motor leads on pwm inverter-fed ac motor drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 919–926, 1996.

[10] S. Lee and K. Nam, "An overvoltage suppression scheme for ac motor drives using a half dc-link voltage level at each PWM transition," *IEEE Trans. Ind. Electron.*, vol. 49, no. 3, pp. 549–557, 2002.

[11] A. Von Jouanne and P. N. Enjeti, "Design considerations for an inverter output filter to mitigate the effects of long motor leads in ASD applications," *IEEE Trans. Ind. Appl.*, vol. 33, no. 5, pp. 1138–1145, 1997.

[12] H. Xiong, J. Zhang, and A. Von Jouanne, "Control of variable frequency drive PWM to mitigate motor overvoltage due to double pulsing in reflected wave phenomenon," *in Proc. IEEE Energy Convers. Congr. Expo.,* 2018, pp. 6563–6570.

[13] B. Narayanasamy, A. S. Sathyanarayanan, F. Luo, and C. Chen, "Reflected wave phenomenon in SiC motor drives: consequences, boundaries, and mitigation," *IEEE Trans. Power Electron.*, in press.

[14] M. J. Scott *et al.*, "Reflected wave phenomenon in motor drive systems using wide bandgap devices," in *Proc. 2nd IEEE Work. Wide Bandgap Power Devices Appl. WiPDA*, *2014*, pp. 164–168.

[15] S. Walder and X. Yuan, "Effect of load parasitics on the losses and ringing in high switching speed SiC MOSFET based power converters," *in Proc. IEEE Energy Convers. Congr. Expo.,* 2015, pp. 6161–6168.

[16] R. Ruffo, P. Guglielmi, and E. Armando, "Inverter side RL filter precise design for motor overvoltage mitigation in SiC-based drives," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 863–873, 2020.

[17] G. Skibinski, "Design methodology of a cable terminator to reduce reflected voltage on AC motors," in *Proc. - IAS Annu. Meet. (IEEE Ind. Appl. Soc.)*, 1996, vol. 1, pp. 153–161.