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Comparison of Conventional and Improved Two-level Converter during ac Faults

Dimitrios Vozikis
University of Strathclyde
Glagsow, UK
dimitrios.vozikis@strath.ac.uk

Fahad Alsokhiry and Ahmed Alabdulwahab
King Abdulaziz University
Jeddah, Kingdom of Saudi Arabia
falsokhiry@kau.edu.sa
aabdulwhab@kau.edu.sa

Grain Adam
NEOM.com
grain.adam@NEOM.com

***Abstract*—An improved two-level converter (I2LC) is a practical compromise between the conventional two-level converter (C2LC) and modular multilevel converter (MMC), recently proposed for dc transmission system for relatively lower dc voltages and rated powers. The I2LC inherent the ac and dc fault behaviors of the MMC and relative simplicity of C2LC. Therefore, this paper presents a detailed quantitative comparison between the ac and dc responses of the C2LC and I2LC to symmetrical and asymmetrical ac faults. It has been showing that unlike the C2LC, the I2LC provides better controllability than the C2L at system level during asymmetrical ac faults, including two operational objectives simultaneously such as balanced output currents and ripple-free dc-link current.**

***Index Terms*—ac and dc faults, two-level converter, improved two-level converter, medium and high-voltage direct current (HVDC) transmission systems.**

I. Introduction

In recent years, voltage source converter technologies such as the C2LC, neutral-point-clamped (NPC) converter, and MMC have dominated renewable power generation, and distribution and transmission systems [1]–[7]. Whilst cascaded multilevel converter that uses full-bridge cells dominates industrial and utility power quality applications at distribution and transmission levels such as reactive compensation and active filtering of harmonics [8]–[14]. As the present trend continues, in which the MMC displaces the C2LC in HVDC applications, the C2LC remains dominant in the MVDC transmission systems for offshore oil and gas platform; especially, where variable frequency and voltage are required such as in Troll A [15]–[17]. Instead of complete displacement, the C2LC will continue to be used in general MVDC and HVDC application, with lower rated powers, where full complexity of the MMC cannot be justified [15]. The I2LC offers relative simplicity of the C2LC and MMC like ac and dc fault ride-through. On these bases, it has been put forward as potential replacement for the C2LC and MMC in dc transmission systems for offshore oil and gas platforms and relatively small islands [15], [16]. In variable ac voltage and frequency applications, in which the dc transmission systems feed large motors, the MMC cannot compete with C2LC and I2LC for the known reason of excessive cell capacitor voltage ripples at low fundamental frequencies. Moreover, the I2LC has simple power circuit and control and expected to offer similar ac and dc fault behaviors as the MMC. In [15], it has been established that the cell capacitors of I2LC do not contribute to transient or steady-state complements fault currents during pole-to-pole (P2P) dc faults. In other words, its cell capacitors do not discharge during dc fault; hence, the major weakness of C2LC which is solved in MMC is addressed in I2LC, i.e., the transient component of the dc fault current is greatly reduced. However, comparison of its dc fault behavior versus that of the C2LC has been studied [15], [16], but no detailed quantitative comparison conducted on its ac faults behaviors, which consider symmetrical and asymmetrical ac faults. Therefore, this paper compares the responses of the I2LC and C2LC to symmetrical and asymmetrical ac faults. Models of both converter being compared are constructed in EMPT-RV, with all necessary controllers for symmetrical and asymmetrical operations have been included, and results of the simulations are compressively discussed. Afterward, the main differences and similarities between the two converters are highlighted.

II. C2LC and I2LC Topologies

A. C2LC

Fig. 1(a) shows a conventional two-level converter (C2LC), which consists of six arms, each contains a self-commutated device (such as insulated gate bipolar transistor, IGBT) plus freewheeling to enable bidirectional current and power flows. The two arms of the same phase-leg operate in complementary manner. Thus, the upper and lower arm currents of each phase are discontinuous and complementary, and add to continuous output phase currents. Such operation leads to devices of the C2LC to experience lower RMS currents, they switch higher currents with the same peaks as that of the output phase currents. As the C2LC synthesizes fully controllable ac voltages from dc voltage and vice versa, sizable dc link capacitor is needed to ensure that the dc link voltage remains virtually constant in order to prevent interactions between ac and dc side (decoupling). However, this sizable capacitor becomes liability during dc fault as it contributes large transient current to dc fault. The C2LC uses phase and magnitude of positive sequence voltages to control its active and reactive powers exchange with the ac grid, while the phase and magnitude of negative sequence voltages to achieve one of the followings: suppress negative sequence currents in

order to ensure balanced three-phase output currents; ripple free dc link current; or oscillation free reactive power during unbalanced grid voltages. From broader power system point of view, ensuring balanced output currents or voltages are of more values operationally than the latter two. Therefore, only balanced output currents will be used in the comparative studies.

B. I2LC

Fig. 1(b) shows the power circuit of the three-phase I2LC. It consists of two sets of three-phase cells, each resembles a C2LC, with isolated capacitor per three arms. The two cells constitute upper and lower arms of the I2LC as depicted in Fig. 1(a). The upper and lower arms of the same phase leg of the I2LC conduct simultaneously as in the MMC, and this is facilitated by co-existence of two distinctive current paths for common and differential mode currents. Moreover, the I2LC is capable of offering two independent control objectives at system level during asymmetrical ac fault compared to one in the C2LC. For an example, manipulations of positive and negative sequence differential mode currents and common mode currents of the phase legs, allow the I2LC to match the controllability of the MMC. Intuitively, the use of a three-phase cell per three arms nullifies fundamental currents in the cell capacitors of the I2LC; thus, its cell capacitance requirement is reduced compared the MMC. Therefore, the cell capacitors of the I2LC only experience to high frequency currents caused by the converter switching, and no 2nd order harmonic circulating currents develop in its arms during balanced operation as in the MMC. Consequently, small cell capacitance and arm inductance are sufficient for correct operation of the I2LC, primarily to decouple ac side dynamics from that of the dc side and suppress the inrush currents during insertion and bypass of the cells. Generally, the I2LC employs two-level high frequency pulse width modulations or selective harmonic elimination, with special attention is needed during allocation of the gating signals to the switching devices of the upper and lower cells. It generates two-level output voltage as its C2LC counterpart. Recall that insertion of the upper cell capacitor into power path necessitates bypass of the lower cell capacitor, and vice versa. Such complementary operation is a necessary condition for prevention of shoot-through across the dc link in the C2LC. Fig. 1(c) displays the overall control systems of the C2LC and I2LC for normal and symmetrical and asymmetrical ac faults. However, for C2LC, the circulating current controllers must be omitted.

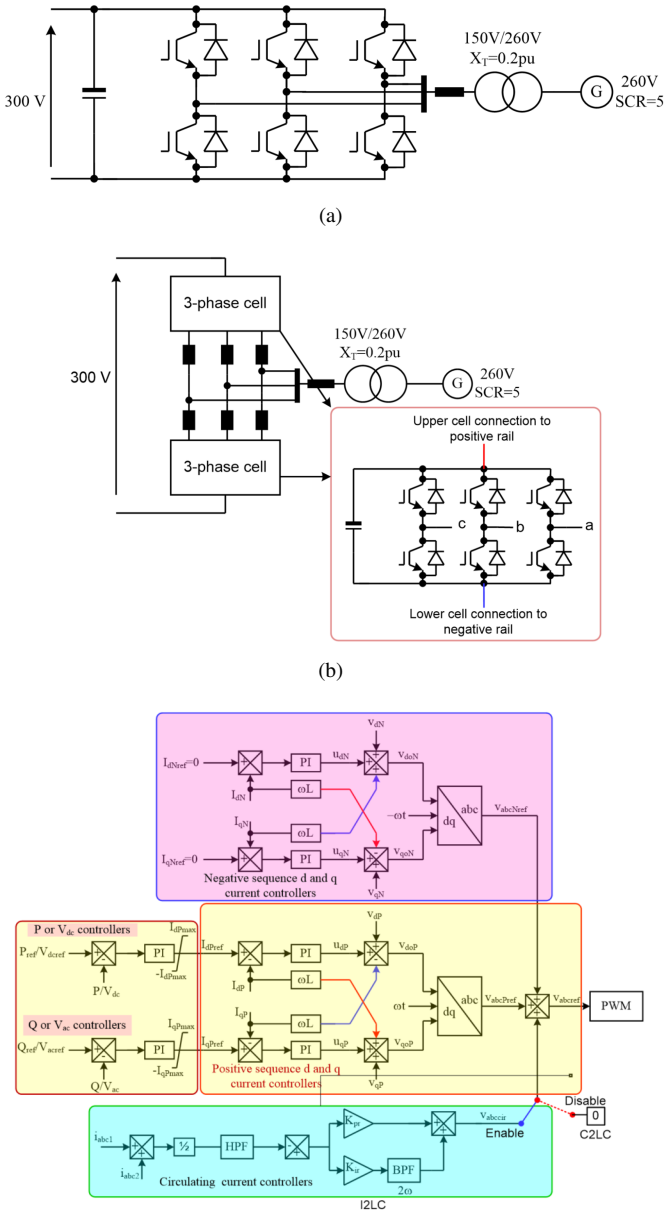

Fig. 1. Improved two-level converter: (a) C2LC power circuit, (b) I2LC power circuit, (c) control systems.

III. Simulation Results

Fig. 2 to Fig. 5 present one-to-one comparison of the responses of the C2LC and I2LC to single-phase to ground and three-phase-to-ground ac faults.. In pre-fault, both C2LC and I2LC exchange the rated active power at unity power factor

TABLE I
Simulation Specifications

Parameter	C2LC	I2LC
DC voltage	300 V	
V converter	150 V	
V grid	260 V	
Apparent Power	5.6 kVA	
Active Power	5 kW	
Reactive Power	2.5 kVAr	
Arm inductance	3.3 mH	
Cell capacitor	170 uF	360 uF
Grid frequency	50 Hz	
Switching frequency	2.5 kHz	

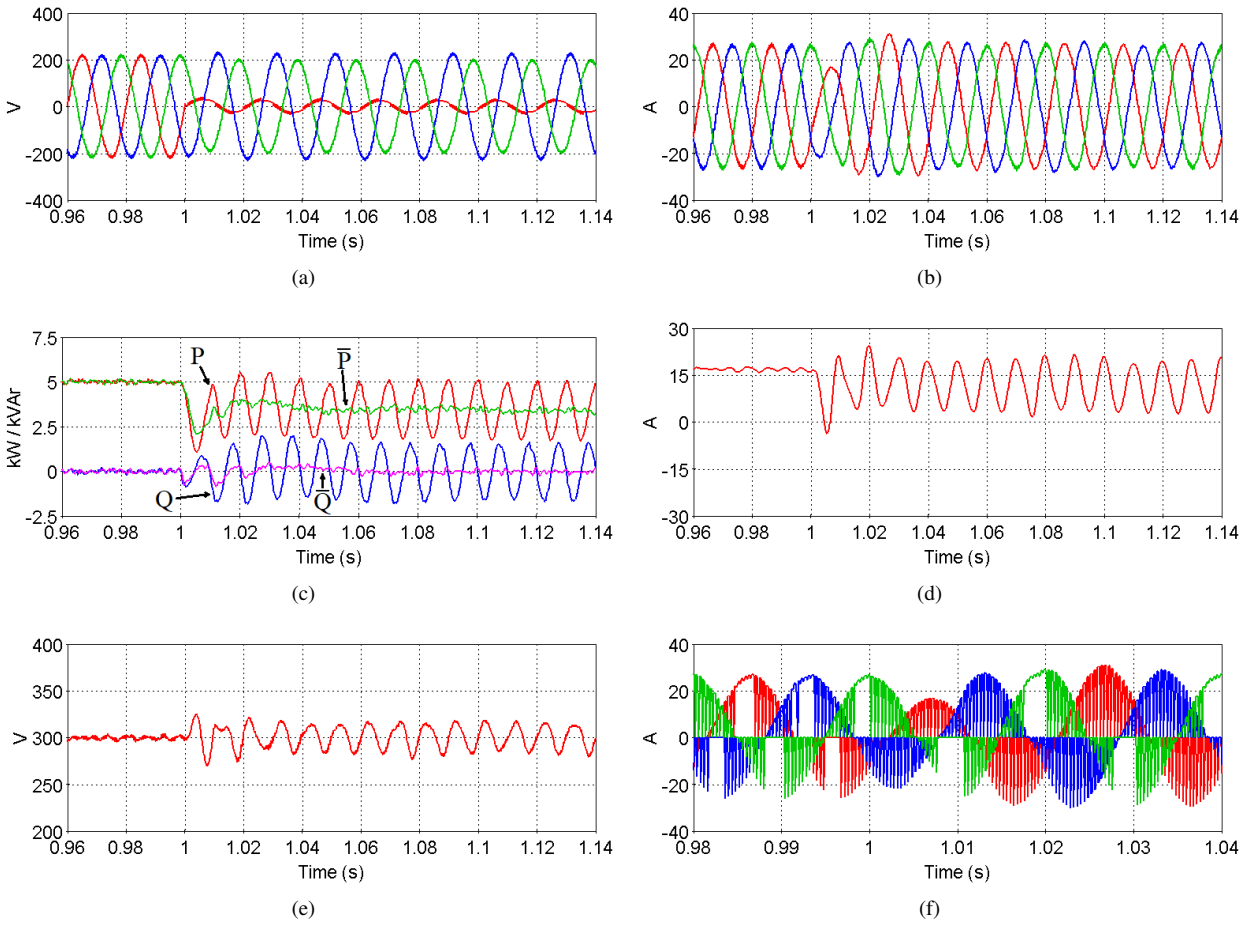

Fig. 2. Simulation waveforms of C2LC during single-phase-to-ground ac fault, with enabled negative sequence current suppression controllers: (a) Grid three-phase voltage, (b) converter-side three-phase ac currents, (c) active and reactive powers at PCC, (d) dc link current, (e dc link capacitor voltages, and, (f) focused view of the three upper arm currents.

with ac grid, and both faults are applied at t=1 s. As shown in Fig. 1(c), both C2LC and I2LC are equipped with active and reactive powers controllers, and positive and negative sequence current controllers. The I2LC is equipped with additional circulating current suppression controller. Comparative simulation results of the C2LC and I2LC are presented in the following parts. The simulation specifications are shown in Table 1.

A. Single-phase-to-ground ac fault

1) C2LC with enabled negative sequence current controllers: Fig. 2 presents selected simulation waveforms when the negative sequence current suppression controllers of the C2LC are enabled. The main observations drawn from Fig. 2 are:

- Fig. 2(a), (b), (d) and (e) show that the inducement of significant 2nd order harmonics ripples in the dc link current and voltage of the C2LC , during single-phase ac fault, despite incorporation of negative sequence current suppression controllers, which ensure balanced three-phase output currents.
- Fig. 2 (b), (d) and (e) show that the converter side currents become balanced and free of negative sequence current during fault as in pre-fault. Nonetheless, ensuring balanced ac side currents are not sufficient for nullification of the dc side current or voltage ripples as the cross-couplings between the positive sequence currents and negative sequence voltages created by the ac fault lead to oscillatory instantaneous active and reactive powers in Fig. 2(c), which in turn cause dc side current and voltage ripples. On other hand, zero average reactive power is exchanged with the ac grid during fault as defined by the reactive power order, see Fig. 2(c) and no excessive over-currents at converter side as shown in Fig. 2(b). Also, the average active power is reduced by approximately one third from the rated as one phase voltage is dully depressed to zero.
- Fig. 2(f) shows snapshot of the three upper arm currents, which exhibit differences in the loading of the IGBTs and freewheeling diodes of the three-phases. The positive and negative arm currents represent conduction through the IGBT and freewheeling diodes respectively.

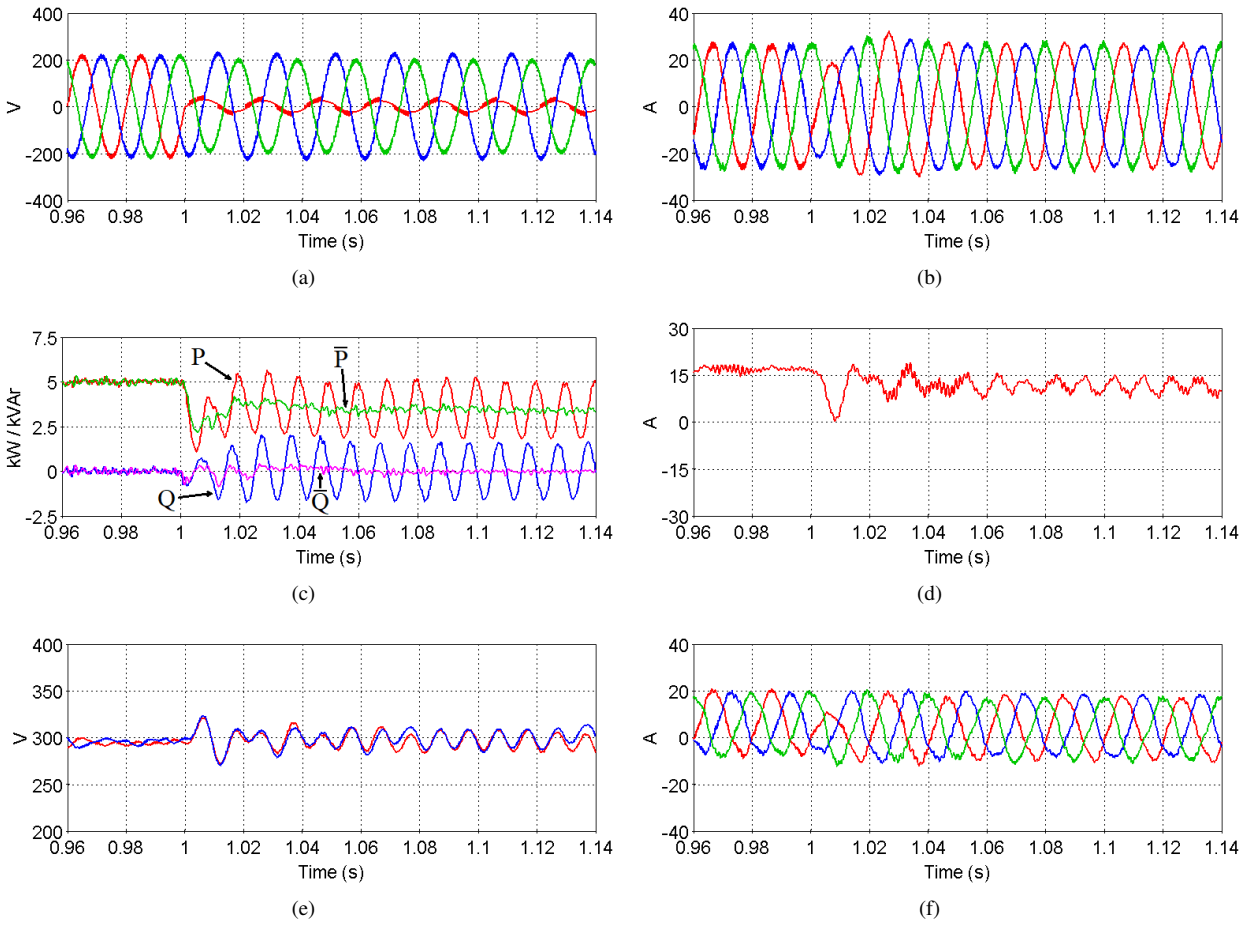

Fig. 3. Simulation waveforms of I2LC during single-phase-to-ground ac fault, with enabled the ccsc and enabled negative sequence current suppression controllers: (a) Grid three-phase voltage, (b) converter-side three-phase ac currents, (c) active and reactive powers at PCC, (d) dc link current, (e dc link capacitor voltages, and, (f) focused view of the three upper arm currents.

In summary, the above findings are in line with general scientific consensuses of the understanding of the behaviour of the C2LC during asymmetrical ac fault as per open literature. Suppression of dc current ripples in C2LC is possible but the ac side current will be unbalanced.

2) I2LC with enabled negative sequence and circulating current suppression controllers: Fig. 3 presents selected simulation waveforms when both negative sequence and circulating current suppression controllers of the I2LC are enabled. The observations drawn from Fig.3 as follows:

- Fig. 3(a), (b), (d) and (e) show the low frequency ripples are largely suppressed from the dc link current and voltage of the I2LC during single-phase ac fault.
- Fig. 3(b) and (f) show balanced converter side currents and ac components of the arm currents as both negative sequence and circulating currents are well suppressed during single-phase fault. However, the small differences shown between the arm currents during fault are due to differences in the magnitudes of their dc components, with faulty phase exhibits lower dc component. The ripples appear in the cell capacitor voltages/dc link voltage are greatly suppressed, and average reactive power exchange with ac grid remains at zero as shown in Fig. 3(c) during fault period. No excessive over-current observed at the I2LC ac side and arms during fault, and with circulating currents in the I2LC arm remain well suppressed as shown in Fig. 3(b) and (f) despite the oscillations exist in instantaneous active and reactive powers.

In summary, the observations and findings drawn from Fig. 3 show that the I2LC can match the benchmark performances of the MMC during asymmetrical ac faults such as single-phase-to-ground when correct control combinations are put in place. Moreover, these results demonstrate its capacity to achieve two control objectives at system level concurrently, during asymmetrical ac faults, i.e., balanced three-phase ac currents and near ripple free dc link current and voltage. These results confirm the superior performance of the I2LC over the C2LC equivalent during asymmetrical ac faults.

B. Three-phase-to-ground ac fault

1) C2LC: Fig. 4 presents selected simulation waveforms when the C2LC is subjected to three-phase fault. Observations

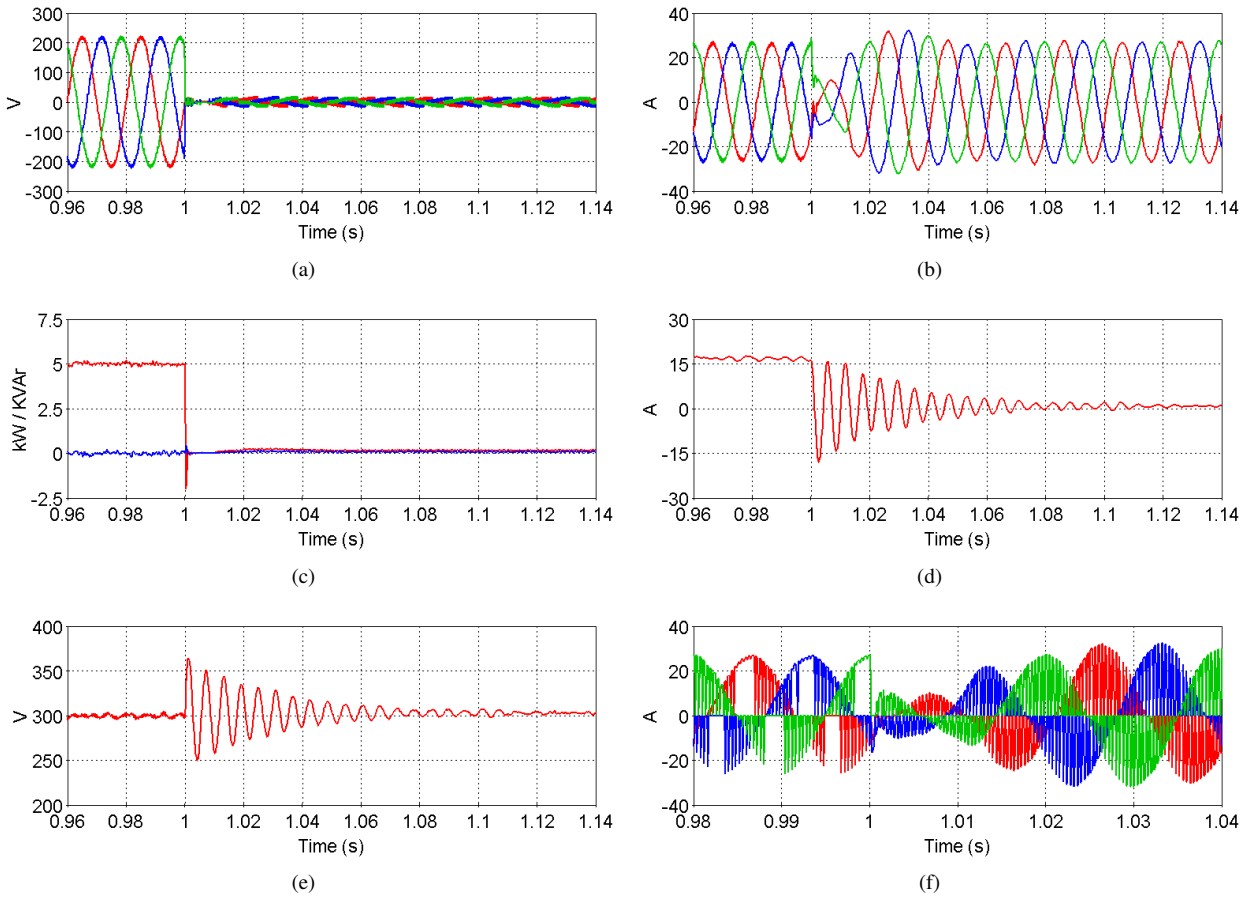

Fig. 4. Simulation waveforms of C2LC during three-phase ac fault, with enabled the ccsc and enabled negative sequence current suppression controllers: (a) Grid three-phase voltage, (b) converter-side three-phase ac currents, (c) active and reactive powers at PCC, (d) dc link current, (e dc link capacitor voltages, and, (f) focused view of the three upper arm currents.

drawn from Fig. 4 are:

- Fig. 4(a), (b), (c) and (d) show the rapid drop of the active power and dc current with the ac voltage when the C2LC is subjected to three-phase ac fault, while the ac currents hit the pre-defined limits specified at the outputs of active and reactive power controllers.
- Fig. 4 (e) shows a brief period of dc side over-voltage as a result of short duration mismatch between ac (or active) power and dc power, created by the fault. Whilst Fig. 4(f) shows the snapshot three upper arm currents of the C2LC, zoomed around fault inception, which show increased stresses on the switching devices. Notice that the majority of current conduction happens thought the IGBTs in pre-fault conditions; and this changes to equal conduction of the IGBTs and freewheeling diodes during fault as all currents become reactive.

In summary, the above findings are in line with general scientific consensuses of the understanding of the behaviour of the C2LC during symmetrical three-phase ac fault as per open literature.

2) I2LC: Fig. 5 presents selected simulation waveforms when the I2LC is subjected to three-phase ac fault. Few observations drawn from Fig. 5 are:

- Fig. 5(a), (b), (c) and (d) show the rapid drop of the active power and dc current with the ac voltage with occurrence of the three-phase ac fault, and the three-phase ac currents rise to pre-defined limits, specified at the outputs of active and reactive power controllers. In this context, the I2LC behaves similar to that of the C2LC.
- Fig. 5 (e) shows that the cell capacitor voltages/dc link voltage of the I2LC exhibits limited and short duration over-voltages compared with that of the I2LC. This is because the total over-voltage of the C2LC is distributed between the two capacitors of the I2LC, and I2LC has twice the inertia of the C2LC. Notice that despite the increase of the output phase currents during three-phase fault, the arm currents of the I2LC become smaller than the pre-fault due to disappearance of the dc components with active or dc power, see Fig. 5(f). This feature could be beneficial in emerging converter dominated power system, in which the I2LC can be used to contribute much higher fault current, without posing its semiconductor devices to risk of destruction.

In summary, the above findings show the superior performance

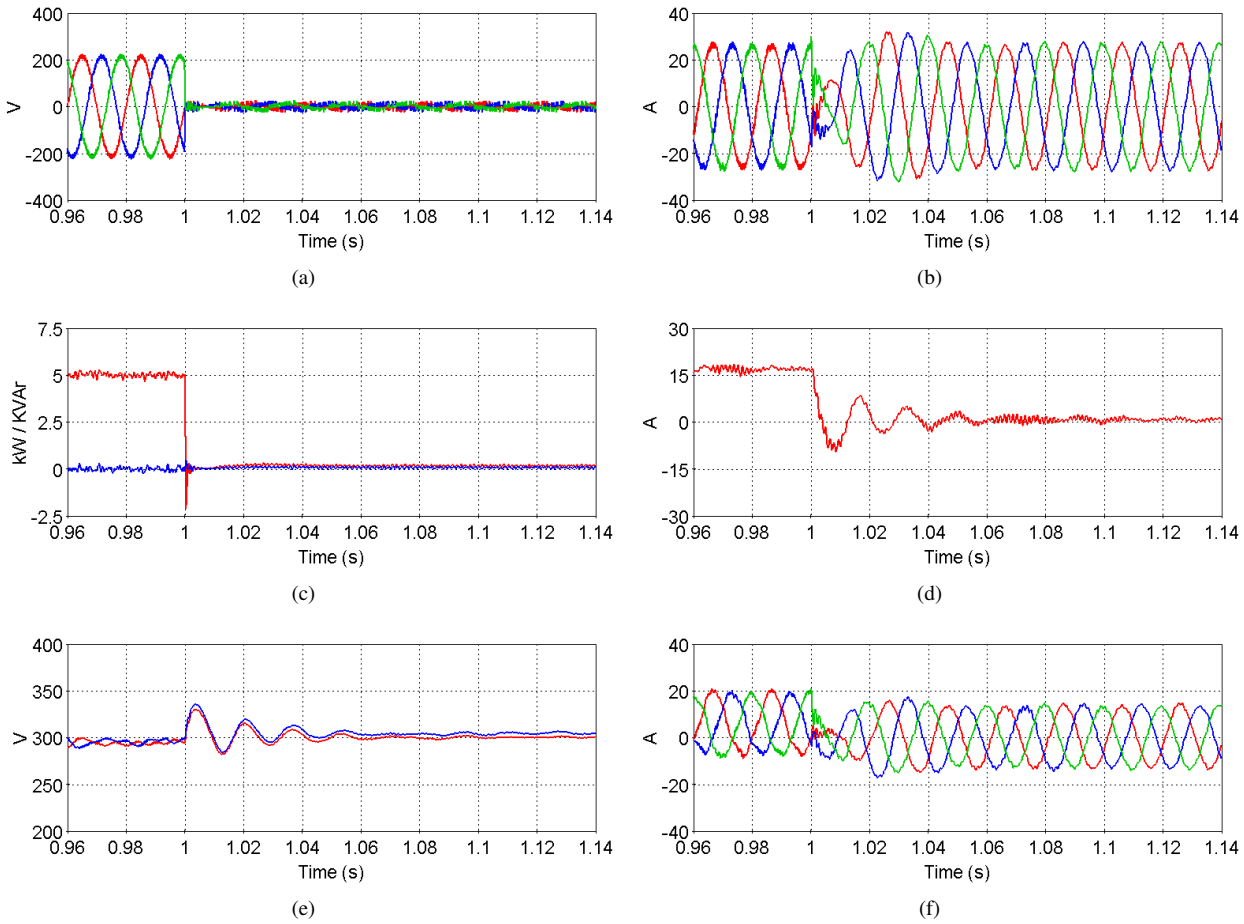

Fig. 5. Simulation waveforms of I2LC during three-phase ac fault, with enabled the ccsc and enabled negative sequence current suppression controllers: (a) Grid three-phase voltage, (b) converter-side three-phase ac currents, (c) active and reactive powers at PCC, (d) dc link current, (e dc link capacitor voltages, and, (f) focused view of the three upper arm currents.

of th I2LC over the C2LC equivalent during symmetrical ac fault.

IV. Conclusions

This paper has presented a detailed comparison of the responses of the C2LC and I2LC to symmetrical and asymmetrical ac faults, in which the I2LC inspires to achieve some of the desirable performances of the benchmark topology, i.e., MMC. Through detailed comparative simulation studies, it has been shown that the I2LC offers superior performance compared to the C2LC during symmetrical and asymmetrical ac faults to the extent it matches the ac fault performance of the MMC.

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