Symmetric 3dB Filtering Power Divider with Equal Output Power Ratio for Communication Systems

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***Abstract*—This paper presents a two-way filtering power divider (FPD) with an equal output power ratio of 1:1. This implies that each of the FPD output port would receive 50% of the power at the input port. To achieve miniaturisation, a common square open-loop resonator is used to distribute energy between the two integrated Chebyshev bandpass filters. In addition to distributing energy, the common resonator also contributes one pole to each integrated bandpass filter (BPF), hence, reducing the number of individual resonating elements used in achieving the integrated FPD. To demonstrate the proposed design technique, a prototype FPD centred at 2.6 GHz with a 3 dB fractional bandwidth of 3% is designed, simulated and presented. The circuit model and microstrip layout results of the FPD show good agreement. The microstrip layout simulation responses show that a less than 1.1dB insertion loss and a greater than 16.5dB in-band return loss were achieved. The overall footprint of the integrated FPD is 37mm by 13mm (i.e. 0.32λg x 0.11λg, for λg = guided-wavelength of the 50Ω microstrip line at 2.6 GHz). The integrated FPD reported in this paper shows some promising merits when compared to similar devices recently reported in literature.**

Keywords—3dB, bandpass filter, equal power divider, microstrip, resonator, two-way

I. INTRODUCTION

Integrating filters and power dividers into a single device is becoming very popular in modern communication systems due to its profound benefits. Power dividers (PDs) are multi-port passive devices that are essential in modern day communication systems as they are used for splitting incoming electromagnetic signals into two (or more) out-going signals in a pre-defined proportion. PDs are often used to direct the correct amount of power to or from other devices (including antennas, multiplexers, filters and amplifiers) within a communication system. The overall performance of a communication system can be significantly influenced by the features of the power divider within the system [1]. Integrating power dividers and filters into a single device not only reduces the physical footprint of a system, but also reduces losses significantly. This is because an integrated filtering power divider (FPD) eliminates the need for physically connecting two separate devices using lossy connectors. Wilkinson power divider is one of the popular and most widely used two-way PDs due to its simple structure and electrical isolation [1]. This type of power divider relies on quarter-wavelength transformers to match the output ports. The theoretical insertion loss characteristics of a power divider depends on the number of output ports it contains [2] as shown in Table I. Several authors have proposed various design techniques for achieving FPDs. [3], [4] proposed FPDs achieved by replacing the quarter-wavelength transformers in a Wilkinson power divider with bandpass filters. Two-way integrated FPDs with equal output power ratio have been proposed and achieved in [5]–[7], while those with unequal or arbitrary power ratios have been reported in [8]–[10]. Other papers have reported integrated FPDs that exhibit dual-band filtering characteristics [11], [12].

TABLE I. THEORETICAL CHARACTERISTICS OF POWER DIVIDERS

Number of output ports	Insertion loss (dB)
2	3.0
3	4.8
4	6.0
5	7.0
6	7.8
8	9.0
10	10.0
12	10.8
16	12.0
24	13.8
48	16.8

The integrated FPD reported in this paper is designed to equally divide the input power between the two output ports in the ratio of 1:1. This means that 50% of the input power would be channelled towards each of the two output ports. Microstrip technology was used in the implementation of the integrated FPD in other to validate the circuit model through simulation.

II. Circuit Model Design

The proposed integrated FPD was formed using two separate but identical three-pole bandpass filters designed following the technique reported in [13], [14]. The design specification for the channel filters are as follows: centre frequency f_0, 2.6 GHz; fractional bandwidth *FBW*, 3% and passband return loss of 20 dB. A 3-pole Chebyshev lowpass prototype (i.e. $g_0 = g_4 = 1.0$; $g_1 = g_3 = 0.8516$; and $g_2 = 1.1032$) with passband ripple of 0.04321 dB is chosen for this design. The circuit model for the proposed symmetric FPD is shown in Fig. 1. A2 & A3 and B2 & B3 shown in Fig. 1 are the second and third resonators of the first and second channel filters, respectively. CR is the common resonator which replaces the first resonator of each channel filter. Hence, CR contributes one pole to each filtering channel of the FPD. Z_0 is the 50 Ohms characteristic impedance of each termination. The values for the J-inverters (i.e. J_{01} & J_{23}), the capacitor C, and the inductor L were all calculated from [14], [15] using (1) and (2). The main contribution of this paper lies on the formulation for calculating the values of the J-inverter, J_1 shown in Fig. 1 using (3). The formulation ensures that the input power from CR is distributed through the two channel filters in the ratio of 1:1. The calculated design parameters for the symmetric two-way integrated FPD are all given in Table II.

$$J_{01} = {g_0}/{Z_0}; \quad J_{23} = \left.\sqrt{{g_1^2}/{g_1 g_2}}\right/ Z_0 \tag{1}$$

$$C = {g_1}/{\omega_0 Z_0 FBW}; \quad L = {Z_0 FBW}/{g_1 \omega_0} \tag{2}$$

$$J_1 = {J_{23}}/{\sqrt{2}} \tag{3}$$

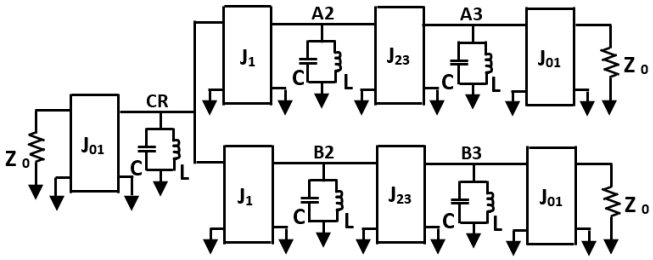


Fig. 1. Circuit model with J-inverters and identical LC resonators.

TABLE II. Calculated Design Parameters for the Symmetric Filtering Power Divider Circuit Model

L (nH)	C (pF)	J_{01}	J_{23}	J_1
0.1078	34.7529	0.02	0.0176	0.0124

The circuit model of Fig. 1 was simulated using the Keysight Advanced Design System (ADS). Before performing the simulation, the couplings between resonators were modelled using the method presented in [16]–[18], which involves replacing each J-inverter on the circuit model with a pi-network of capacitors. The circuit model simulation results are shown in Fig. 2. The results clearly show that the integrated FPD has its centre frequency at 2.6 GHz and its minimum return loss at 20 dB as designed. The 3 dB *FBW* of 3% is also achieved with minimum insertion loss of 1.1 dB (not including the 3dB division loss for a two-way power divider).

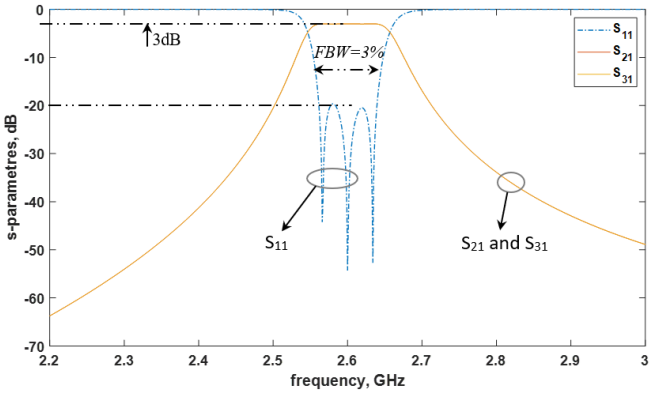
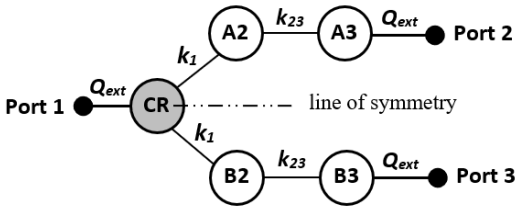


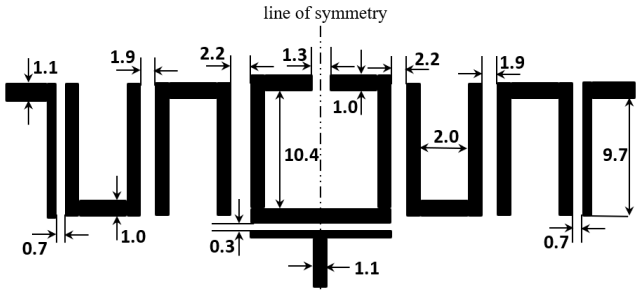
Fig. 2. Results of the symmetric filtering power divider circuit model.

III. Microstrip Layout Design

Microstrip square open-loop resonator (SOLR) [19], [20] and hair-pin resonator (HPR) [15] were used in the layout implementation of the proposed FPD. The SOLR and each HPR were designed to resonate at f_0. The FPD layout was made on Rogers RT/Duroid 6010LM substrate with a relative dielectric constant $\varepsilon_r = 10.7$, a thickness h = 1.27 mm and a loss tangent $\tan\delta = 0.0023$. The physical dimensions of the FPD were determined using the Keysight ADS full-wave electromagnetic simulator. The coupling scheme and the equivalent microstrip layout, indicating the simulated dimensions, are shown in Fig. 3. The k_{23} in Fig. 3 (a) is the coupling coefficient between each pair of channel filter resonators while Q_{ext} is the external quality factor between CR and port 1; and the last resonator of each channel filter and their respective ports (i.e. ports 2 & 3). Each port represents a 50 Ohms termination. The values for k_{23} and Q_{ext} in Fig. 3 (a) were all calculated from [2], [15] using (4), where f_1 and f_2 are the eigenmodes from simulating a pair of microstrip resonators. The calculated values for k_1 was determined using (5). These value (i.e. k_1) ensures that 50% of the input power is delivered to each output port (i.e. ports 2 and 3). Fig. 3 (b) shows the simulated dimensions for achieving the integrated FPD layout.



(a)



(b)

Fig. 3. Symmetric 3dB filtering power divider (a) coupling scheme with Q_{ext} = 28.387, k_{23} = 0.031, k_1 = 0.022, (b) microstrip layout with all dimensions in mm.

$$k_{23} = {(f_2^2 - f_1^2)}/{(f_2^2 + f_1^2)}\ ;\ Q_{ext} = {g_0 g_1}/{FBW} \qquad (4)$$

$$k_1 = {k_{23}}/{\sqrt{2}} \qquad (5)$$

The symmetric two-way FPD layout of Fig. 3 (b) was simulated using the Keysight ADS Momentum full-wave electromagnetic simulator. The simulation results are shown in Fig. 4 and clearly show that the FPD has its centre frequency at 2.6 GHz, with a simulated minimum return loss at 16.5 dB. The minimum insertion loss of 1.1 dB (not including the 3dB division loss for a two-way power divider) was also achieved as indicated in the results of Fig. 4. S_{21} and S_{31} indicate transmission zeros at 2.32 GHz. It is important to note that, unlike the FPD circuit model design that is lossless, the microstrip layout implementation included both conductor and dielectric losses. The loss tangent of the dielectric materials was kept at 0.0023, while the copper conductivity used for the simulation was maintained at 5.8 x 10^7 S/m, with a thickness of 35 micron (µm) for both the top and bottom metals of the microstrip line. Surface roughness and thickness variation of the substrate material were not considered.

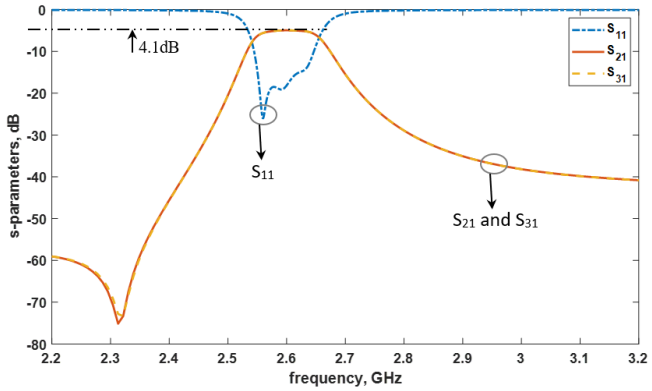


Fig. 4. Results for the microstrip filtering power divider layout.

IV. Experimentation

The proposed integrated FPD was fabricated using the same material employed in the electromagnetic simulation of the microstrip layout. Radio frequency printed circuit board (PCB) milling process technique was utilised for the circuit fabrication. A photograph of the fabricated microstrip FPD is shown in Fig. 5. The overall size of the FPD is 37 mm by 13 mm, i.e. 0.32λg x 0.11λg, where λg is the guided wavelength of the 50 Ω microstrip line at 2.6 GHz. A 50 Ohms SMA (sub-miniature version A) connector was attached to each port of the fabricated FPD to facilitate measurement using Keysight Vector Network Analyzer. The device has not been measured; hence, measurement results are not presented in this paper. This is as a result of our University campuses being shut-down due to the Coronavirus (Covid-19) pandemic.

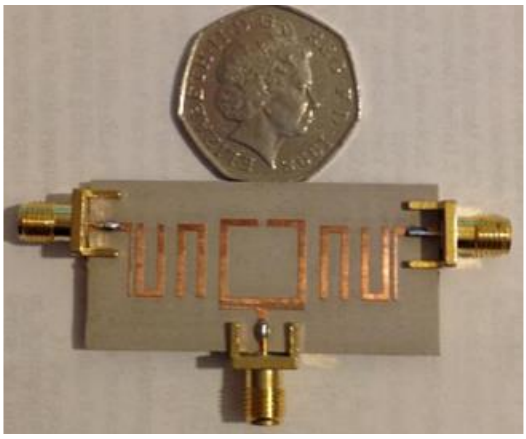
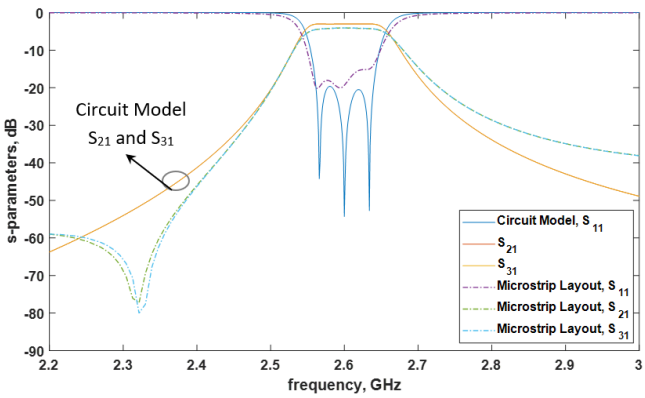


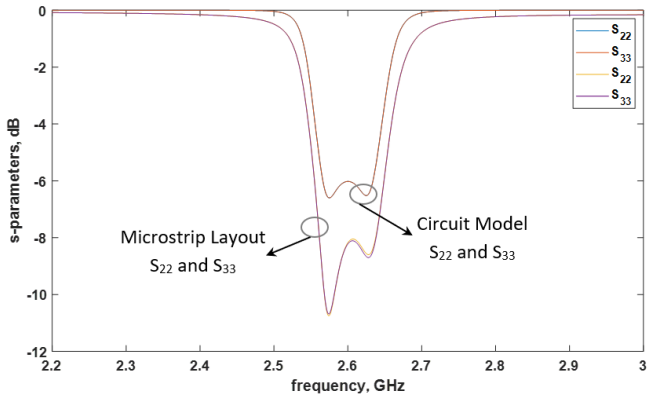
Fig. 5. Photograph of the fabricated microstrip filtering power divider.

V. Results Comparison and Discussion

The circuit model and microstrip layout results of the proposed FPD are co-presented in Fig. 6 for easy comparison. The results show good agreement with good insertion loss of less than 1.1dB. The minimum in-band return loss is greater than 16.5 dB, and the centre frequency is 2.6 GHz as designed. A comparison of the proposed FPD performance with other recently proposed power dividers is presented in Table III. The comparison with [5]–[7], [21] clearly shows that the proposed FPD is of compact size with a good insertion loss.



(a)



(b)

Fig. 6. Comparison of the circuit model and the microstrip layout results of the proposed symmetric 3dB filtering power divider (a) differential-mode responses, (b) single-ended output ports responses.

TABLE III. COMPARISON OF THE PROPOSED AND OTHER EQUAL POWER DIVIDERS

Ref.	f_0 (GHz)	Filter order	Size $(\lambda g)^2$	FP[a]	PDR[b]	IL[c] (dB)
[5]	1.0	2	0.0612	Yes	1:2	3.8
[6]	2.4	3	-	Yes	1:2	1.4
[7]	1.99	3	0.0825	Yes	1:2	3.74
[21]	3.0	3	0.2166	Yes	1:2	1.78
This work	2.60	3	0.0352	Yes	1:2	1.1

filtering property, [b.] power dividing ratio, [c.] insertion los

VI. CONCLUSION

A symmetric 3dB integrated filtering power divider has been proposed, designed and implemented using the microstrip transmission line technology. The design was completely based on simple formulations and relied on microstrip square open-loop and hair-pin resonators for miniaturisation. The circuit model and microstrip layout results show good agreement, with centre frequency of 2.6 GHz, insertion loss of less than 1.1 dB, and minimum return loss of greater than 16.5 dB.

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