An improved gate driver for power MOSFETs using a cascode configuration

M A H Broadmeadow*, G F Ledwich†, G R Walker#

All authors Queensland University of Technology, Australia.
*e-mails: *mark.broadmeadow@qut.edu.au, †g.ledwich@qut.edu.au, #geoffrey.walker@qut.edu.au*

Abstract. To overcome the limitations of existing gate drive topologies an improved gate drive concept is proposed to provide fast, controlled switching of power MOSFETs. The proposed topology exploits the cascode configuration with the inclusion of an active gate clamp to ensure that the driven MOSFET may be turned off under all load conditions. Key operating principles and advantages of the proposed gate drive topology are discussed. Characteristic waveforms are investigated via simulation and experimentation for the cascode driver in an inductive switching application at 375V and 10A. Experimental waveforms compared well with simulations with long gate charging delays (including the Miller plateau) being eliminated from the gate voltage waveform.

1. Introduction

Conventional voltage driven gate drive circuits utilise a resistor (see fig. 1) to control the switching speed of power MOSFETs [1]. The gate resistance is adjusted to provide controlled rate of change of load current and voltage. This method of drive introduces long switching delays due to the time required to charge the gate-source capacitance of the power MOSFET, described by the RC time constant of the gate resistor and capacitance. The delays in charging the gate of the power MOSFET result in increased switching losses and conduction losses. The high driving impedance also makes the MOSFET susceptible to failure modes invoked by the MOSFET parasitic capacitance during switching transitions.

Current sourced [2,3] and resonant [4,5] gate drivers have also been developed, which utilize an inductive magnetic element to charge the gate of a power MOSFET. These drivers provide some advantages over voltage driven gate drive, such as recovery of gate drive energy and reduced turn on times, but exhibit limitations in performance (minimum duty cycle and circulating current losses) and practical implementation (complexity, size and cost).

To overcome the limitations of existing gate drivers, a new gate drive concept is proposed to provide fast, controlled switching of power MOSFETs. The proposed solution provides a voltage sourced gate drive where the driver explicitly controls the rate of change of gate-source voltage of the power MOSFET. The proposed driver exploits the cascode configuration with the inclusion of an active gate clamp to turn off the power MOSFET under all load conditions. Gate drive current is not sourced through a resistor, allowing high peak currents to be delivered to the gate during turn-on and the Miller effect to be eliminated. Finally, reliability of the driven MOSFET is enhanced as the gate is always connected to a low impedance source, preventing switching-transient invoked failure modes. The following section provides the implementation and operational details of the proposed cascode gate driver.

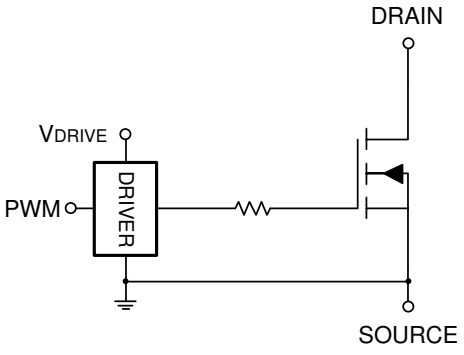

Figure 1. Conventional resistor-fed gate drive circuit.

2. Operating principles of the proposed cascode gate drive circuit

The cascode configuration is broadly understood in the literature [1] but is typically applied to current driven devices such as BJTs [6,7] or normally-on devices such as JFETs [8,9] for which the benefits of a cascode connected drive are more readily apparent. The characteristics of a cascode drive for high-voltage power MOSFETs in switching applications are not well documented.

The proposed cascode gate drive circuit is shown in Figure 2. The circuit is composed of two low-voltage n-channel power MOSFETs, Q1 and Q2, which are used to drive high-voltage power MOSFET Q3. Q2 is the cascode MOSFET which is connected from the source of Q3 to the effective source of the entire module. Q1 is the clamp MOSFET which is connected between the gate and source of Q3. A voltage source, $V_{drive,HV}$, capable of both sinking and sourcing current, is connected from the gate of the high-voltage MOSFET to the source of the cascode MOSFET. The magnitude of this voltage source should be equal to the maximum desired drive voltage for the high-voltage MOSFET. Bypass capacitors are connected in parallel with $V_{drive,HV}$. A bootstrap driver is

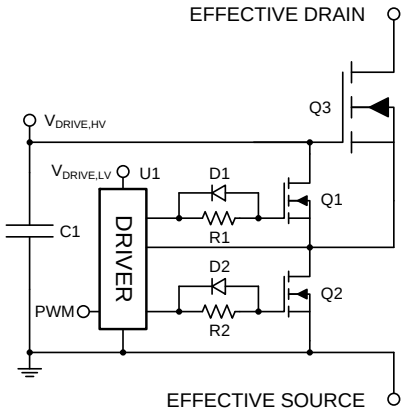

Figure 2. Proposed cascode gate drive circuit.

used to drive the clamp and cascode MOSFETs through gate resistors R1 and R2 respectively. The bootstrap driver may be supplied from a separate voltage source, $V_{drive,LV}$, to allow the use of low voltage clamp and cascode MOSFETs that are optimized for lower drive voltages. Diodes D1 and D2 may be optionally connected in anti-parallel with resistors R1 and R2 respectively to provide dead time between the clamp and cascode MOSFETs when switching.

The cascode driver circuit may be also implemented using a number of alternative configurations, to achieve the same operating characteristics. A p-channel MOSFET may be used for the clamp MOSFET, for example, to allow both the clamp and cascode MOSFETs to be driven from the same driver IC, and from the same drive voltage source as the high-voltage MOSFET, simplifying the circuit implementation.

2.1 Action of the clamp MOSFET

In the presence of positive drain-source current the high-voltage MOSFET will turn off naturally when the cascode MOSFET is turned off. The load current will commutate from the cascode MOSFET to instead discharge the gate-source capacitance of the high voltage MOSFET. Any excess current flows through the external source-gate diode (or body-diode of the clamp MOSFET in the proposed topology) and is returned to the drive voltage source $V_{drive,HV}$ which clamps the gate voltage of the high-voltage MOSFET. $V_{drive,HV}$ must be capable of sinking current to ensure the drive voltage is not pumped-up over a number of turn-off cycles.

In the case of reverse channel conduction, however, natural turn-off of the high voltage MOSFET with the cascode MOSFET is not guaranteed. Additionally, as the natural turn-off is affected by the load current the natural turn-off process is load dependant.

To overcome these limitations the clamp MOSFET is included in the proposed topology to ensure that the high-voltage MOSFET can be turned off independent of load conditions. The clamp MOSFET can be turned on to discharge the gate-source capacitance of the high-voltage MOSFET through the low impedance of the channel of the clamp MOSFET. Dead time must be introduced between the turn-on of the clamp and cascode MOSFETs to void shoot-through currents from discharging the gate-drive supply. The clamp MOSFET may also be held-on during the off-period of the high-voltage MOSFET to provide a low-impedance clamp to ensure the high-voltage MOSFET is not unintentionally turned on by applied transients.

The turn-off process is similar to that of a conventional resistive-fed gate drive with low gate resistance. Additionally, the transition of the half-bridge in an inductive switching application will typically be driven by the turn-on transient of the opposing MOSFET, rather than the turn-off transient.

2.2 Turn-on process

The turn-on process for the cascode driver circuit is more complex than that of the conventional resistor-fed gate driver, as the cascode MOSFET conducts both the load current and the gate current of the high-voltage MOSFET. We examine the turn-on process for a cascode driven high-voltage MOSFET in a clamped inductive switching application. The simplified switching waveforms and corresponding current paths during turn-on are shown in Figures 3 and 4 respectively.

Prior to turn-on, the entire load current is circulating through the clamping diode to the bus and the voltage at the drain of the high-voltage MOSFET is clamped to the bus voltage (interval T_A). The clamp MOSFET, Q1, is turned off.

At t_0, the driver IC applies the drive voltage, $V_{drive,LV}$, to the cascode MOSFET drive resistor, R2. The gate-source capacitance of the cascode MOSFET then begins to charge through the gate resistor (see fig. 4a). The gate of the cascode MOSFET continues to charge towards voltage $V_{drive,LV}$ during interval T_A (see fig. 3), following an exponential relationship with a time-constant defined by the gate resistance and gate-source capacitance. Period T_A ends at t_1, when the gate-source voltage is equal to the threshold voltage of the cascode MOSFET, $V_{gs(th),ca}$.

At time t_1, the channel of the cascode MOSFET begins conducting. During interval T_B, current flows through the channel of the cascode MOSFET to charge the gate-source capacitance of the high-voltage MOSFET (see fig. 4b). The gate-source voltage of the high-voltage MOSFET increases as the drain-source voltage of the cascode MOSFET decreases, due to the voltage $V_{drive,HV}$ being held constant. The rate of change of gate-source voltage of the high-voltage MOSFET is therefore controlled by the Miller effect of the cascode MOSFET.

During this interval the entire cascode gate current flows through the gate-drain (Miller) capacitance of the cascode MOSFET, as shown in Figure 4b. The gate current is controlled by the gate resistance, which subsequently controls the rate of change of gate-source voltage of the high-voltage MOSFET as the current flowing into the gate-drain capacitance is proportional to the rate of change of drain-source voltage on the cascode MOSFET. As all current flows through the gate-drain capacitance, no current is available to charge the gate-source capacitance such that the gate-source voltage remains constant during this interval. Interval T_B ends at t_2,

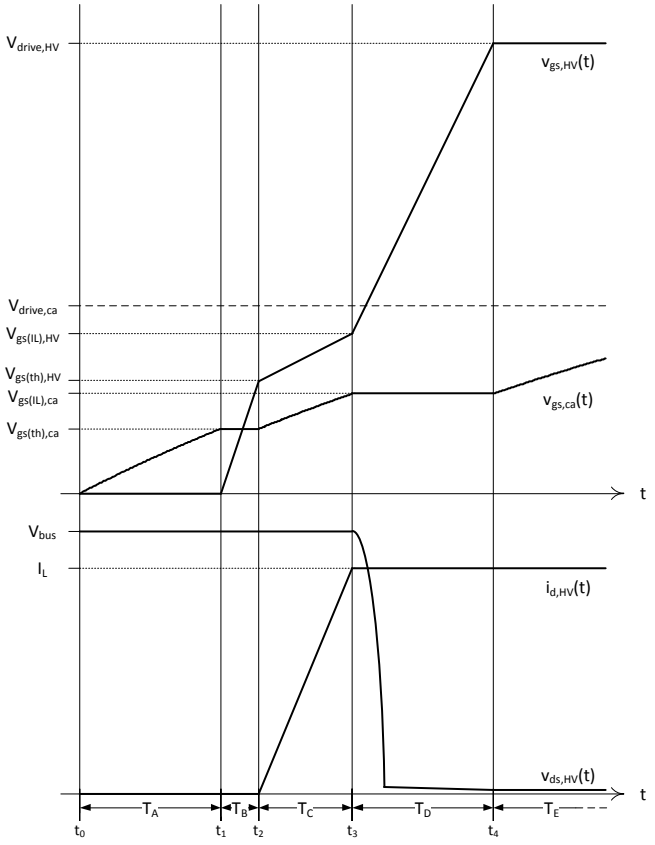

Figure 3. Simplified turn-on waveforms for the cascode gate drive circuit.

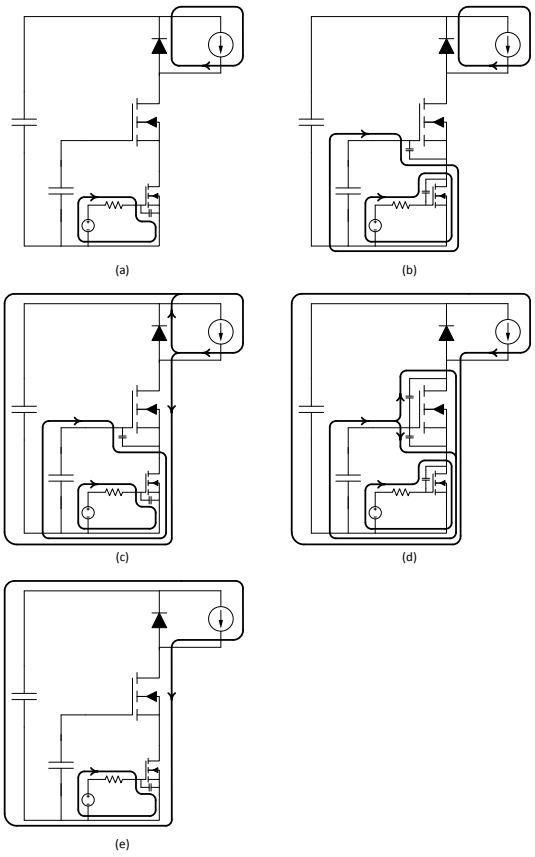

Figure 4. Current paths through the cascode driver circuit during turn-on. (a) Interval T_A. (b) Interval T_B. (c) Interval T_C. (d) Interval T_D. (e) IntervalT_E.

once the gate-source voltage of the high-voltage MOSFET reaches the threshold voltage, $V_{gs(th),HV}$.

At time t_2, the channel of the high-voltage MOSFET begins conducting the load current. As shown in Figure 4c, the load current must also be conducted by the cascode MOSFET. The gate-source voltage of both the cascode and high-voltage MOSFET must therefore increase during interval T_C to support the load current. The rate of change of drain current will be dependant on a number of factors, including the relative transconductances of the cascode and high-voltage MOSFETs. A low-voltage cascode MOSFET will usually have a transconductance orders of magnitude higher than that of the high-voltage MOSFET.

The cascode MOSFET must also conduct the current required to charge the gate of the high-voltage MOSFET. The current available to charge the gate of the high-voltage MOSFET is the difference between the drain current of the cascode MOSFET and the drain current of the high-voltage MOSFET. Typically the current required to charge the gate of the high-voltage MOSFET will be only a fraction of the load current. Combined with the difference in relative transconductances, this will typically result in the cascode MOSFET controlling the rate of change of load current during this interval.

As the drain current of the high-voltage MOSFET increases, current commutates from the high-side diode. Interval T_C ends at time t_3 when the entire load current, i_L, is supported by the high-voltage MOSFET. It should be noted that reverse recovery of the high-side diode is not considered in the simplified turn-on process, but would usually occur between intervals T_C and T_D.

At time t_3 the voltage at the drain of the high-voltage MOSFET begins to transition. During interval T_D, the drain-source voltage of the high-voltage MOSFET decreases. This results in a current flowing through the parasitic gate-drain capacitance which is proportional to rate-of-change of drain-source voltage and gate-drain capacitance. As there is no resistance in series with the gate of the high-voltage MOSFET, however, the gate current is not limited and the gate of the high-voltage MOSFET may be charged simultaneously.

As the gate of the high-voltage MOSFET is charged, the gate-source voltage of the high-voltage MOSFET increases and consequently the dV_{ds}/dt also increases. The entire gate current of the high-voltage MOSFET must be conducted by the cascode MOSFET. The drain-source voltage of the cascode MOSFET decreases as the gate-source voltage of the high-voltage MOSFET increases, and hence the time rate-of-change of gate-source voltage on the high-voltage MOSFET is controlled by the Miller effect of the cascode MOSFET, similar to interval T_B. As shown in Figure 3, the drain-source voltage of the high-voltage MOSFET decreases rapidly until it approaches the same magnitude as the gate-source voltage. At this time the gate-drain capacitance increases rapidly, due to the non-linear dependence of gate-drain capacitance on drain-source voltage.

The fall rate of drain-source voltage decreases significantly at this point due to the increase in parasitic capacitance; higher gate and drain currents are transiently required to drive the MOSFET fully on. In the absence of a Miller plateau, however, the high voltage MOSFET is still able to be driven towards full enhancement during this interval, greatly reducing the turn-on time. Interval T_D ends at time t_4, once the gate-source voltage of the high-voltage MOSFET has increased to the supply voltage $V_{drive,HV}$.

Interval T_E extends from time t_4, until the gate of the cascode MOSFET is fully charged to the drive voltage, $V_{drive,ca}$. During this interval the load current is fully supported by the high-voltage MOSFET and the high-voltage MOSFET is fully enhanced, with the channel resistance having reached its minimum, steady-state value. The gate of the cascode MOSFET continues to charge through the gate resistor, however, given that the channel resistance of the cascode MOSFET is orders of magnitude lower than that of the high-voltage MOSFET, fully enhancing the gate of the cascode MOSFET is not critical as any reduction in total resistance in the load path is negligible.

3. Advantages of the cascode driver circuit

3.1 Higher drive current capability

In a conventional resistor-fed gate drive circuit, all current required to charge the gate of the power MOSFET must be sourced from the driver, typically a driver IC or transistor pair with limited current sourcing/sinking capability. The peak current that may be delivered to the MOSFET gate is also limited by the series resistance used to control the switching speed of the MOSFET. The cascode driver allows high peak currents to be delivered to the MOSFET gate. As there is no series resistance present, the peak gate current is limited only by the cascode MOSFET. High charging current may also be delivered to the gate regardless of the state of charge of the gate.

3.2 Reduced gate charging time

In the conventional resistor-fed gate drive circuit, the charging of the MOSFET gate is constrained by the RC time constant of the gate resistor and parasitic gate-source capacitance of the power MOSFET, resulting in long turn-on delays. Instead the cascode MOSFET controls directly the rate of change of gate-source voltage of the high-voltage MOSFET. The rate of change of gate voltage is then largely linear which allows the gate-source voltage to be driven quickly to the threshold voltage and then the turn-on region to be traversed rapidly in a controlled manner. The time to fully enhance the gate to the maximum drive voltage is greatly reduced as there is no RC time constant involved in charging the gate.

3.3 Reduced gate drive power requirements

The cascode MOSFET drive requirements are significantly less than those of the high-voltage MOSFET. Further, the use of lower drive voltages and currents is possible due to the higher transconductance of low-voltage MOSFETs. In many cases it may be possible to use a logic-level output to drive the cascode MOSFET.

Due to the natural turn-off mechanism it is possible for the majority of the high-voltage MOSFET gate drive energy to be recovered into the gate drive supply from the high-voltage bus during turn off under forward channel conduction. This significantly reduces the gate drive power supply requirements.

3.4 Improved dV/dt immunity

In the cascode driver the gate of the high-voltage MOSFET is always connected to a low-impedance voltage source. Any currents which are injected into the gate via voltage transients applied to parasitic capacitances are bypassed by this supply, improving immunity to dV/dt inducted turn-on. Additionally, during the off-period the clamp MOSFET provides a very low-impedance shunt across the gate-source of the high-voltage MOSFET to hold the MOSFET off under all conditions.

3.5 Negative gate drive capability

The cascode driver is also ideally suited to provide a negative gate voltage bias during the off period. A simple modification to the topology whereby the drain of the clamp MOSFET is connected to a voltage source slightly higher than that of the drive voltage source would provide this functionality. The cascode driver would therefore be ideally suited to driving silicon carbide power MOSFETs which require a negative gate bias to hold them off and high drive current for fast switching times due to their significantly reduced transconductance compared with standard silicon power MOSFETs.

4. Simulation results

The cascode driver circuit was simulated using LTspice for a clamped inductive switching application utilising a SiC Schottky diode in the high-side position and a cascode driven high-voltage MOSFET in the low-side position (see fig. 5). Simulation models for the critical components, including MOSFETs and Schottky diode were developed from parameters extracted from device datasheets. Other components are modelled as ideal.

The cascode MOSFET is driven from 5V through a 220Ω gate resistor. The voltage source to drive the high voltage MOSFET was selected to be 12V. The nominal bus voltage was selected as 375V and the circuit operation is simulated with a fixed load current of 10A.

The clamp MOSFET is excluded from the simulation as it is not involved in the turn-on process. A clamping diode is inserted in its place. RC snubbers around both high-voltage power devices and a large gate-source resistor on the high-voltage MOSFET are included to provide a better representation of the hardware prototype. A voltage source, V_s, is introduced to measure the current flowing into the cascode drive high-voltage MOSFET.

Figure 6 shows the simulated switching waveforms. The simulated gate-source voltage waveforms compare well with the simplified conceptual model presented in section 2.

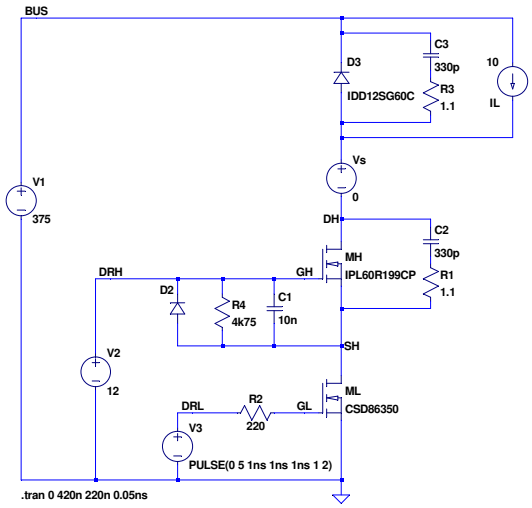

Figure 5. Simulation schematic for the cascode gate driver.

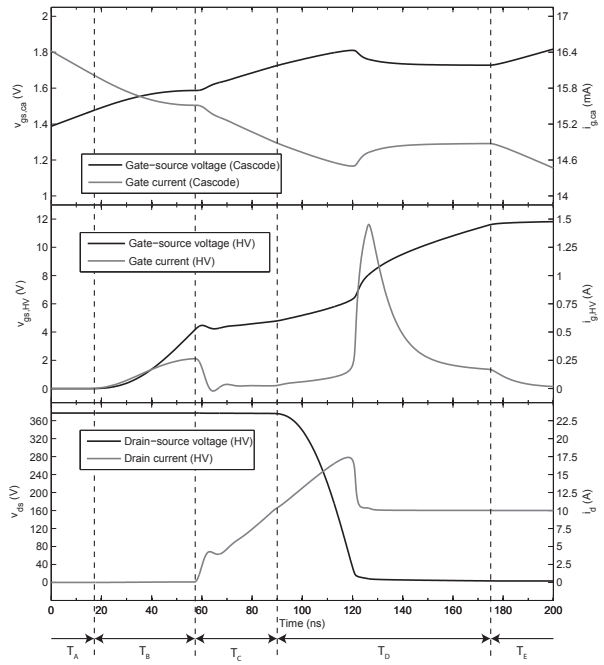

Figure 6. Simulated switching waveforms for the cascode driver circuit in a clamped inductive switching application. The timebase is annotated with the intervals corresponding to figures 3 and 4

Plateaus in the cascode MOSFET gate-source voltage are visible at beginning at approximately 40ns and 120ns, which fall within corresponding periods T_B and T_D respectively in Figure 3. It should be noted that the rate of change of gate-source voltage on the high-voltage MOSFET during these periods is largely linear, absent of the exponential decay that is present in a conventional resistor-fed gate drive circuit.

The Miller plateau has also been eliminated from the gate-source voltage of the high-voltage MOSFET. This plateau would usually be present during the fall in drain-source voltage during interval T_D (from approximately 90-175ns).

The change in drain current of the high-voltage MOSFET is also largely linear over interval T_C. A peak overshoot of approxmately 7.5A above the load current is observed at 120ns. It should be noted that this curent is not reverse recovery, but the current required to discarge the junction capacitance of the SiC Schottky diode and the high-side RC snubber. The Schottky diode does not undergo reverse recovery and hence the drain voltage begins to transition as soon as the high-voltage MOSFET supports the entirety of the load current. During the transition of the drain voltage, however, additional current is required to charge the Schottky diode capacitance.

The initial rapid increase in drain current may be attributed to the operating point of the cascode MOSFET at the time at which the high-voltage MOSFET begins to conduct the load current. As the proportion of the load current through the high-voltage MOSFET increases, there is a subsequent decrease in current available to charge the high-voltage MOSFET gate (as the current through the cascode MOSFET remains approximately the same). During this period the drain current of the high-voltage MOSFET increases until it exceeds that of the cascode MOSFET, causing the gate of the high-voltage MOSFET to be slightly discharged until the drain current of the high-voltage MOSFET is reduced below that of the cascode MOSFET. This can be observed by the slight dip in the high-voltage MOSFET gate-source voltage in Figure 6 at t=68ns. The cascode MOSFET then controls the rate of change of current through both devices.

The total simulated switching time is approximately 60ns with the high-voltage MOSFET full enhanced in under 120ns. It should be noted that the drive current delivered to the high-voltage MOSFET are not unreasonably high, with a peak gate current of approximately 1.5A delivered to the gate at approximately 128ns (due to the rapid non-linear increase in the parasitic capacitance of the high-voltage MOSFET).

5. Experimental results

The cascode driver was implemented in hardware (see fig. 9) using the same configuration of devices as was simulated in the previous section. Due to physical constraints it was necessary in the hardware prototype to drive the high-voltage MOSFET in the high-side position and place the SiC Schottky diode in the low-side position. Measurements were then referenced to the half-bridge output rather than the bottom of the bus. Care was taken to ensure that stray capacitances to ground were minimised. A 0.1Ω current sense resistor as introduced between the high- and low-side devices to measure the current.

An inductor was used to provide the load current during the switching transient and double-pulse switching pattern was used to investigate the turn-on switching transients of the cascode MOSFET driver. The prototype was tested under the same operating conditions as specified in the simulation. Figure 7 shows the captured waveforms of the double-pulse test.

Due to the high rates of change of current, the voltage measured across the current sense resistor includes a high contribution from the sense resistor stray inductance which is proportional to di/dt rather than the current. To reconstruct the true current a first-order low pass filter is applied to the measured

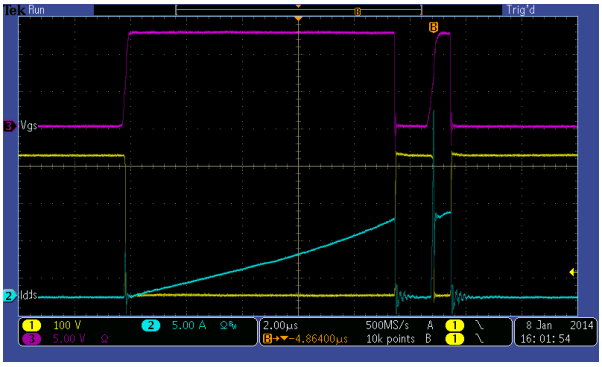

Figure 7. Experimental double pulse switching waveforms for the cascode driver. Shown are drain-source voltage of the HV-cascode pair (CH1, 100V/div), drain current of the HV MOSFET (CH2, 5A/div) and gate-source voltage of the HV MOSFET (CH3, 5V/div).

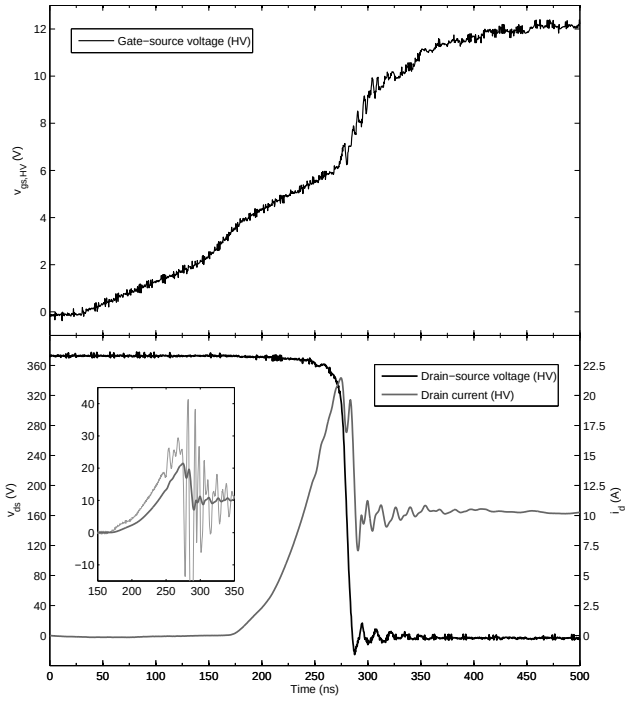

Figure 8. Experimental turn-on waveforms for the cascode driver. The inset shows the filtered current (dark) overlaid on the raw current shunt measurement (light).

voltage across the current shunt, which is tuned assuming a series inductance of 2nH, based on geometric considerations. The raw measured and filtered currents are presented in the inset of Figure 8 for comparison.

Experimental drain-source voltage, drain current and gate-source voltages are presented in Figure 8. The features of the waveforms compare well with the simulated waveforms. The total switching time for the experimental prototype was longer than in the simulation (approximately 125ns compared with 60ns) which is likely attributed to the presence of stray inductances in the prototype not modelled by the simulation.

Three distinct intervals are visible in the gate-source voltage waveform, the shape of which corresponds well with the simulation. No Miller plateau is evident as expected.

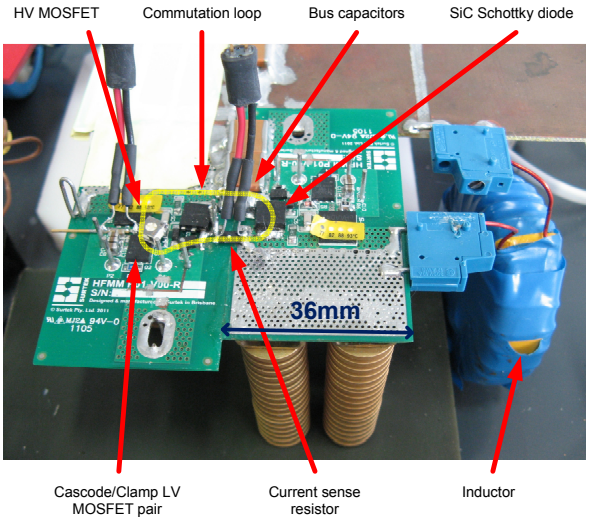

Figure 9. Experimental prototype of the cascode MOSFET gate driver showing key components and the load current commutation loop.

Acknowledgements

This work was supported in part by Surtek Pty Ltd.

References

[1] N. Mohan, T. M. Undeland, W. P. Robbins. *Power electronics: converters, applications and design*, 3rd edition, (John Wiley & Sons, Hoboken, 2003).

[2] Z. Zhiliang, F. Jizhen, L. Yan-Fei, P. C. Sen. "Discontinuous-current-source drivers for high-frequency power MOSFETs", *Power Electronics, IEEE Transactions on*, **25(7)**, pp. 1863–1876, (2010).

[3] J. Fu, Z. Zhang, Y. F. Liu, P. Sen, L. Ge. "A new high efficiency current source driver with bipolar gate voltage", *Power Electronics, IEEE Transactions on*, **27(2)**, pp. 985–997, (2012).

[4] Y. Zhihua, Y. Sheng, L. Yan-Fei. "A new dual-channel resonant gate drive circuit for low gate drive loss and low switching loss", *Power Electronics, IEEE Transactions on*, **23(3)**, pp. 1574–1583, (2008).

[5] Z. Zhiliang, W. Eberle, Y. Zhihua, L. Yan-Fei, P. C. Sen. "Optimal design of resonant gate driver for buck converter based on a new analytical loss model", *Power Electronics, IEEE Transactions on*, **23(2)**, pp. 653–666, (2008).

[6] J. L. Duarte, J. Rozenboom, T. Peijnenburg, H. Kemkens. "Simulating a BJT-MOSFET cascode-connected power switch suitable for resonant converters", *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, pp. 893–900 vol2., (1992).

[7] S. Buonomo, S. Musumeci, R. Pagano, C. Porto, A. Raciti, R. Scollo. "Driving a new monolithic cascode device in a DC-DC converter application", *Industrial Electronics, IEEE Transactions on*, **55(6)**, pp. 2439–2449, (2008).

[8] T. McNutt, V. Veliadis, E. Stewart, H. Hearne, J. Reichl, P. Oda, S. Van Campen, J. Ostop, C. R. Clarke. "Silicon carbide JFET cascode switch for power conditioning applications", *Vehicle Power and Propulsion, 2005 IEEE Conference*, pp. 499–506, (2005).

[9] J. Biela, D. Aggeler, D. Bortis, J. W. Kolar. "5kV/200ns pulsed power switch based on a SiC-JFET super cascode", *IEEE International Power Modulators and High Voltage Conference, Proceedings of the 2008*, pp. 358–361, (2008).