BICMOS MILLIMETRE-WAVE LOW-NOISE AMPLIFIER

by

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SUMMARY

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Keywords: Coplanar waveguide, distributed elements, interdigital capacitor, impedance matching, low-noise amplifier, mathematical model, microstrip transmission lines, millimeter-wave, passive component.

A radio frequency (RF) signal at the receiver of a wireless subsystem contains noise. In order to attain a good signal-to-noise ratio (SNR), the signal power in the RF signal must be higher than the noise present in the RF signal of the receiver. The low-noise amplifier (LNA) is a significant component in the analogue RF subsystem required to achieve a good SNR. In this research, a cascode with T-Type microstrip transmission line (MTL) topology, was put-forward for the realisation of LNA at millimetre-wave (mm-wave) frequencies. This topology was proposed after an exhaustive study of LNA configurations obtainable in published works. From extensive studies, it became clear

that existing approaches and configurations used in the narrowband and ultra-wideband LNA yield unsatisfactory results when they are applied to mm-wave LNAs. Similarly, existing mm-wave LNA designs have certain drawbacks. One such drawback is the existing designs trade-off gain, noise figure (NF) or bandwidth. The formulated mathematical model gave insight into the newly proposed approach. Detailed equations for noise, gain and input matching were derived and optimised to ensure maximum gain and minimum NF. Thereafter, the model was validated via simulation, fabrication, and characterisation of the prototyped passive networks. The different stages of the mm-wave LNA were also prototyped by modelling the input matching network (IMN), interstage matching network (IMS), output matching network (OMN) along with the microstrip to coplanar wave (MTL-to-CPW) transition in CST MWS.

Simulation results and measurement of each stage consisting of the T-type MTL topology were recorded. Thereafter, these were simulated with the active component of the circuit and the simulated *S*-parameters were compared to the measurement results as obtained from the fabricated prototypes. The simulated results of the mm-wave LNA at 56 GHz to 64 GHz using the Global Foundries' (GF) 8HP process indicated a gain of 20.0 dB and an associated NF of 6.2 dB, while retaining an input return loss, S_{11}, below -13 dB. The power consumption of the LNA was 45.37 mW and finite estate of 4.41 mm^2. The prototyped passive was simulated with CST MWS using high-resistivity silicon as substrate. Further integration with LNA will be the object of further investigation.

The decoupling capacitor was also modelled as an interdigitated capacitor (IDT) along with coplanar-to-microstrip line transition (CPW-to-MTL). The ground was designed around the CPW-to-MTL and the IDT. This passive structure arrangement was the template for the IMN, IMS and OMN. The measurement result from each of the passive structures was discussed in detail. However, only the OMN was deployed in the AWR microwave office (MWO) schematic that showed the LNA circuit. An S_{21} value of 9.22 dB at 57.88 GHz, S_{22} value of -6.22 dB at 57.96 GHz, S_{11} of -15.71 dB at 57.84 and an NF of 6.22 dB at 58 GHz was observed after the simulation in AWR MWO.

Even though the measured S_{11} matched the simulated response, the same could not be said about the gain, S_{21}, as it dropped slightly. The reduction in gain can be attributed to a few factors. Firstly, the ground-signal-ground platform used along with the MTL-to-CPW transition introduces a large amount of substrate parasitics, which reduces the gain. Even though the MTL-to-CPW transition was meant to translate the impedance of the MTL to that of the CPW, the matching impedance did not change. The series resistance and inductance effect increased considerably. The NF also increased above the simulated value.

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Remember, "..... ***Your Labour in the Lord is not in Vain.***"

LIST OF ABBREVIATIONS

ADS	Advanced design system
BiCMOS	Bipolar complementary metal-oxide semiconductor
BJT	Bipolar junction transistor
BW	Bandwidth
CAD	Computer-aided design
CB	Common-base
CBE	Collector-base-emitter
CBEBC	Collector-base-emitter-base-collector
CC	Cascode
CE	Common-emitter
CMOS	Complementary metal oxide semiconductor
CPW	Coplanar waveguide
CS	Common-source
DC	Direct current
DE	Differential-ended
DUT	Device under test
DRC	Design rule check
EDA	Electronic design automation
EM	Electromagnetic
FEM	Finite element method
GaAs	Gallium arsenide
GFET	Graphene FET
GBW	Gain-bandwidth product
GND	Ground
GSG	Ground-signal-ground
HBT	Heterojunction bipolar transistor
HEMT	High electron mobility transistor
HiCUM	High-current model
IC	Integrated circuit
IDT	Interdigitated capacitor

IEEE	Institute of Electrical and Electronic Engineers, Inc.
IIP3	Third-order input-referred intercept point
IMN	Input matching network
IMS	Interstage matching network
IMT	Institute for Research & Development in Microtechnologies ("IMT-Bucharest")
IoE	Internet of everything
IoT	Internet of things
LNA	Low-noise amplifier
LVS	Layout versus schematic
MATLAB	Matrix laboratory
MIM	Metal–insulator–metal
mm-wave	Millimeter wave
MMIC	Monolithic microwave integrated circuit
MTF	Mean time to failure
MTL	Microstrip transmission line
MTL-to-CPW	Microstrip-to-coplanar wave
MWO	Microwave office
MWS	Microwave suite
NDA	Non-disclosure agreement
NF	Noise figure
NFmin	Minimum noise figure
OMN	Output matching network
PCB	Printed circuit board
PEC	Perfect electrical conductor
Q-factor	Quality factor
RF	Radio frequency
RLC	Resistance-inductor-capacitor
RLGC	Resistance-inductor-conductance-capacitor
SE	Single-ended
Si	Silicon
SNIM	Simultaneous noise and input matching
SNR	Signal-to-noise ratio

SoC	System-on-chip
SOLT	Short-open-load-thru
S-parameters	Scattering parameters
TEM	Transverse electromagnetic
TL	Transmission line
VCO	voltage-controlled oscillator
VNA	Vector network analyser

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CHAPTER 1: INTRODUCTION

1. CHAPTER OVERVIEW

This thesis presents the design, simulation, prototyping, and measurement of an advanced silicon-germanium hetero-junction bipolar (SiGe HBT) bipolar complementary metal oxide semiconductor (BiCMOS) low-noise amplifier (LNA) at the millimetre-wave (mm-wave) frequency range. During this process, the broadband noise, direct current (DC) and radio frequency (RF) performance of the LNA at room temperature was observed. This chapter gives a quick rundown on the context and purpose of the research and identifies clear research questions to be investigated. The rationale for this research work is discussed while the objective and aims of the work are used to justify the impact of this work to the existing field of knowledge.

1.1 BACKGROUND OF RESEARCH

Millimetre-wave (mm-wave) systems have been an active research topic in the last decade and significant progress has been made with using this frequency band for new and unique technological development around the world. Wireless communication systems such as 5G cellular at 30-40 GHz; Institute of Electrical and Electronic Engineers (IEEE) standard IEEE 802.11ad for wireless local area network (WLAN) at 55-65 GHz, and wireless backhaul at E-band (71-76 GHz, 81-86 GHz) operate at a significantly higher data rate because of the large bandwidth availability. The achievable bandwidth for IEEE 802.11ad varies across the continents of the world. In South Africa, the allocated frequency band is between 57 GHz to 64 GHz [1], which can be utilised for wireless data communication. One key restraint for mm-wave systems is the limited transmitted distance.

For a given amount of power, a short wavelength corresponds to a proportionally short transmission distance. The transmission distance is also determined by the atmospheric absorption spectrum. A pictorial overview of the mm-wave and the attenuation values can be found in [2]. An oxygen molecule resonates at 60 GHz and creates an atmospheric

absorption peak of 9 dB/km, making this frequency suitable only for short-range wireless communications, e.g. Gbps wireless USB or streaming video, hence avoiding interference with neighbouring devices. The specified oxygen absorption loss is advantageous for links that operate below 100 metres [3]. Thus, the constraint becomes a strength at 60 GHz. A notable response of signal at 60 GHz is that it does not penetrate solid materials but ensures that densely packed communication links are established. Losses due to the molecules at resonance [4] create high atmospheric losses in proportion to increasing distance. Along with the identified merits comes the opportunity to utilise mm-waves across a significant frequency band.

Frequency bands such as 55-66 GHz; 72-76 GHz; 83-86 GHz; and 95-98 GHz serve and meet the high bandwidth requirements of the different applications requiring frequency between 50 and 100 GHz [5]. LNAs play a substantial part in the processing of noise superimposed, low power signals and amplification of a processed signal to a satisfactory level, as depicted in Figure 1.1.

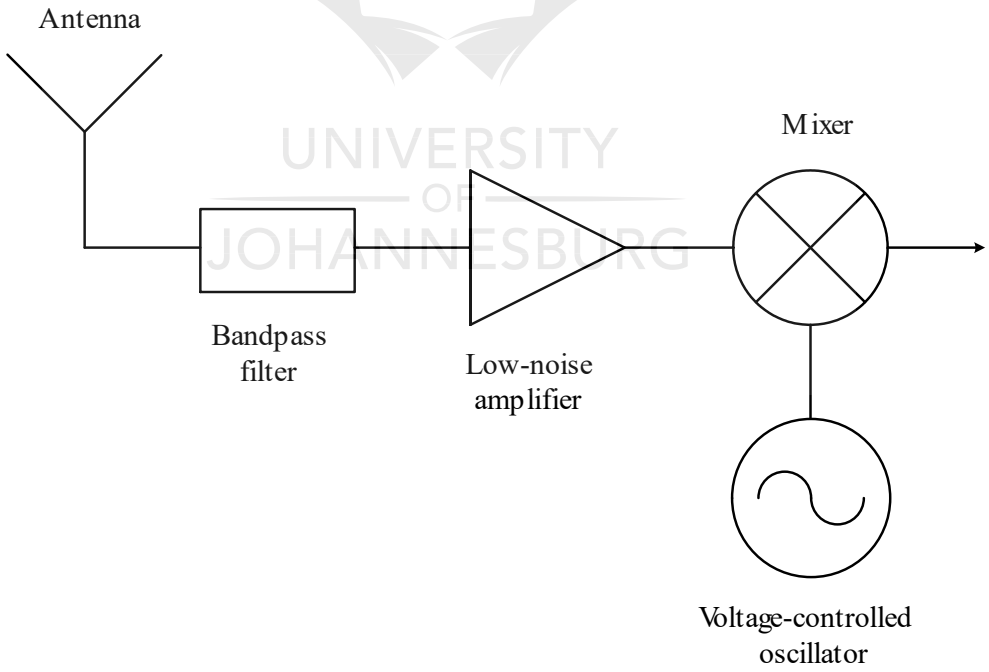

Figure 1.1: Block representation of a superheterodyne receiver.

In Figure 1.1, noise from a signal received from an antenna is passed to a bandpass filter in which the desired information is selected before further processing is carried out.

Thereafter, the selected signal is applied to the LNA, which reduces the noise level of the input signal while ensuring that self-generated noise from within the other LNA stages is lessened. Once this is achieved, the mixer converts the desired signal from the LNA and the output signal from the voltage-controlled oscillator (VCO) into the intermediate frequency. The demand for faster, cheaper and energy-efficient integrated circuits (ICs) [6] prevalent in today's electronics and semiconductor technology continues to rise. In an attempt to improve IC performance, transistor feature sizes in ICs are continuously shrinking [7]. This has contributed directly to increased speed, device density, and circuit complexity, as forecast in Moore's law [5]. For the realisation of a compact IC, lumped and distributed elements are used in modelling of LNAs. The advancement in silicon (Si) structures came as a result of the limit to the device scaling used on the Si bipolar junction transistor (Si BJT). However, the scaling of Si BJTs was feasible to the unity gain cut-off frequency, f_T of 20 to 30 GHz. Beyond these limits, it was unachievable.

This gave rise to III-V compound semiconductors. These semiconductors have the advantage of higher frequency, electron mobility, wideband gap, saturation velocities and compositional altering that could meet precise needs in IC design and its applications. In spite of all these advantages, the low level of integration, difficulty in prototyping, lower yield, and higher cost have limited its niche market to light-emitting diodes, photoelectron systems and discrete semiconductor lasers [8]. Most semiconductor devices have a low levels of integration and excessive cost of manufacturing, as highlighted in [9]. Even though the high cost of manufacturing is a recent trend from the year 2000, the need to reduce the manufacturing unit cost and increase the level of integration is at present driving the semiconductor industry to lower technological nodes, such as 28 nm to 22 nm, and currently 14 nm nodes. Thus, foundries involved in high technological nodes are gradually losing foothold in the market [9].

At present, SiGe HBT devices achieve an f_T and maximum oscillation frequency (f_{max}) in excess of 300 and 500 GHz respectively [10], with operable frequencies of over 100 GHz. SiGe HBT [11], [12] offers integration advantages, higher speed, and excellent

microwave noise behaviour, beyond the performance of Si and III-V semiconductor elements.

1.2 HYPOTHESIS AND RESEARCH QUESTIONS

Achieving a low noise figure (NF) in the design of a mm-wave LNA is still a challenging issue for analogue circuit design engineers. Existing topologies [13], such as shunt series coupled common-source (CS) LNA, CS LNA with shunt input, and differential-ended topologies, have been utilised to resolve the NF issue. All the listed approaches are known for their unacceptably high NF. Indeed, this observation is no surprise, as it has been reported in [14] that the source impedance is crucial in minimising the NF of an LNA. The source impedance must be inductive in nature to keep the NF low. The theory was further established by simulation and prototyping [15] of the IC. In the design, the inductor was used at the collector, base, and emitter of the first stage. Despite the reduced NF, the required bandwidth was not met. Another shortcoming is that the performance of passive devices tends to be unpredictable as mm-wave frequencies are approached.

The unexplained and variable nature of disruptive parasitic capacitance and inductance elements in passives limits performance and the chance of reproducing results from experiments. One of the effects is that the impedance magnitude of the passive changes as a higher frequency is approached. As the frequency of the designed circuit increases, the insertion loss from passive components increases, leading to undesirable effects, changing the overall behaviour of the elements in the circuit (distributed effects). Along with this, even when the targeted NF is measured, this comes at a cost of either a low gain or a small bandwidth [16]. Thus, the physical dimension of the components becomes a significant and substantial portion of the wavelength, which is inversely proportional to frequency. It is not consistent with the performance patterns of similar components at a lower frequency [8]. Distributed element matching ensures low circuit losses and better modelling. The microstrip transmission line (MTL) meets the characteristic needs of the mm-wave frequency adequately [9], [17]. The transmission line approach would therefore be used in this work. LNA, a pivotal component of the front-end RF receiver, allows an incoming signal from the antenna in a transceiver system, a combination of

preferred information and unwanted interferer, to be fed into it. The desired signal is known to be the weaker component in the received signal and the LNA is vital to provide gain while ensuring minimum deterioration of the signal-to-noise ratio (SNR).

Research on the design and prototyping of the state-of-the-art V-band LNA (56-64 GHz) was conducted by [11], [12], [18]–[21]. The current approach to designing the 60 GHz LNA includes common-emitter (CE), cascode (CC), differential and a combination of CE and CC topologies. The CE topology is known for its high output impedance due to the high frequency pole at the denominator. It has been used with the shunt feedback technique to improve its gain [22], [23].

The performance of mm-wave LNA obtainable using the CE and CB transistors can be further enhanced by using T-type MTL topology to have a wideband width and flat gain. An analytical approach and measurement of the LNA have shown that the first stage contributes the highest amount of noise to the overall NF. Since the downconverter generates about 10 dB of noise, the LNA serving the DC must achieve a very low noise at 60 GHz and a high gain in comparison to the total noise contribution of the other components. WLAN is central to meeting the demand for more bandwidth required at present in the age of interconnected networks. This demand is not going to reduce over the next decade, as more applications that are developed use the wireless domain. The need for security on any platform using the wireless network cannot be ignored. This is where the mm-wave frequency band becomes the present and future solution to the demand associated with internet of things (IoT). While the WLAN is currently running out of spectrum space, the mm-wave frequency band offers a solution that deals with the demand for bandwidth need for security and opportunity for the re-use of frequency. The mm-wave LNA, a key block in the radio transceiver system, would be needed in the telecommunication block.

Reducing the bias current along the T-topology network with the CE and CC topology (transistor bias current), with inductive emitter degeneration would increase the overall gain of the amplifier circuitry. This would also reduce the NF and improve the input and

output impedance matching of the LNA, thus eliminating signal reflections and losses. The CC and CE topology with T-type MTL topology has proven capable of effective use in the design of an LNA for providing wide bandwidth. However, the LNA considered requires high gain after its implementation.

The use of a T-matching network at the base of a CE transistor and at the IMS has been reported, with the advantages of large bandwidth and good gain. This has further been established as a direct relationship between bandwidth and gain because of the amount of feedback (negative feedback concept) in the IC. A reduction in gain at the expense of the larger bandwidth results in an increase in the NF, especially at the first stage of the CC transistor configuration. It is therefore imperative to deduce a relationship between the gain, NF and the bandwidth such that the sensitivity of any of the listed characteristics due to component value changes would cause the least change in overall gain performance of the IC and ensure a functional broadband mm-wave LNA.

Based on the above discussion, the following hypothesis was conceived:

If the biasing of the CC topology at the first and second stage of the mm-wave LNA, along with the use of the T-matching topology at the input matching network (IMN) and interstage matching network (IMS), can be designed and modelled, then a two-stage LNA functioning at 60 GHz can be optimized to realise a low NF and a high gain.

To test the hypothesis, the following research questions must be answered:

How can it be demonstrated through mathematical modelling that the suggested approach would yield a wideband matching, a low power configuration, high input impedance, minimal NF, and high gain?

Secondly, how can the chosen configuration ensure that a large 3-dB bandwidth is realised along with a high and flat gain while reducing gain and bandwidth trade-offs?

Lastly, how can the linearity and stability of the mm-wave LNA be improved without the introduction of the degeneration MTL?

1.3 JUSTIFICATION OF THE RESEARCH

The extension of wireless frequencies to the mm-wave band offers sufficient bandwidth, which is an increasing requirement of the human populace. The mm-wave frequency is attractive for thermal remote measurement, radiometry, fine resolution remote sensing, medical imaging, and pulse-modulated radar, among many other uses.

The V-band frequency range (40 – 75 GHz), which forms part of the frequency spectrum at the mm-wave band, also contributes to secure satellite absorption and short-range communication. It is known that this aforementioned frequency band is expected to be the core of the 5G network, which is being rolled out. Its significant strength, as seen in strong signal absorption, frequency reuse, wide bandwidth, and a very high data rate, would be required for the rapidly growing IoT and Internet of everything (IoE).

At the heart of the wireless transceiver system is the LNA, which is an essential building unit at the receiver end of every communication system. Its principal role is to boost the signal received while reducing the amount of additional noise introduced into the signal from the LNA. Its NF, gain, and bandwidth are important for the overall functioning of the transceiver system. At any instance of increasing the gain of the LNA, the NF and bandwidth are adversely affected. Wide bandwidth is necessary for systems that require high throughput at short range.

Tables 1.1 and 1.2 list the parameters of the significant and associated work found in works of literature showing the ultra-modern 60 GHz LNA performance. The simulation and measurement results of each design using the CC and T-type MTL topology are shown. For this work, the chosen topology is compared to other LNAs with similar configurations where wider bandwidth and high gain are realised. Wide bandwidth in other research projects is traded off for low NF and high gain. However, the proposed

topology is suitable for applications that require high gain, a low NF and wide bandwidth in the V-band.

1.4 RESEARCH METHODOLOGY

In authenticating the aforementioned hypothesis, the scientific method is applied. The research methodology supports an efficient procedure for the research work, and this is illustrated in Figure 1.2. In addition, different existing topologies that are applicable to LNA at the mm-wave frequency range were highlighted, and the relevant limitations and challenges of the topologies were reported. The review of process technology was combined to also understand and identify the strength and demerits of processes that are commercially available. The significance of using the distributed or the lumped element in the monolithic microwave integrated circuit (MMIC) design space was also captured in terms of its known strength and vulnerabilities associated with each element.

Lumped elements are used relatively because of the parasitics that become dominant at the mm-wave band. The distributed elements with reduced loss also decrease NF in the IC circuit. After checking through relevant literature in identified areas and the feasibility of designing and resolving the gap found in literature, a hypothesis was formulated. A scientific hypothesis predicts what would happen after the design of the experiment. Once the hypothesis statement has been formulated, an experiment must be designed. The experiment is required to prove or invalidate the hypothesis. This is the first proof required before further work can continue. The initial result at this stage only considers an independent variable while taking cognisance of its effect on the dependent variables.

After this, related research questions were drafted. Within this framework, selected techniques, which can be used to answer each research question, were derived. The analytical approach includes firstly using matrix laboratory (MATLAB) to estimate the initial value of S_{11}. Thereafter, mathematical expressions of insertion loss, S_{21} and NF using the small-signal equivalent circuit analysis were derived. As indicated in Figure 1.2, an updated literature review of the challenges and limitations associated with the topology selection, design, prototyping, and characterisation of LNA at mm-waves was

completed. If the estimated value S_{11}, S_{21}, and NF meet the defined design specifications, the full design of the IC schematic can be continued.

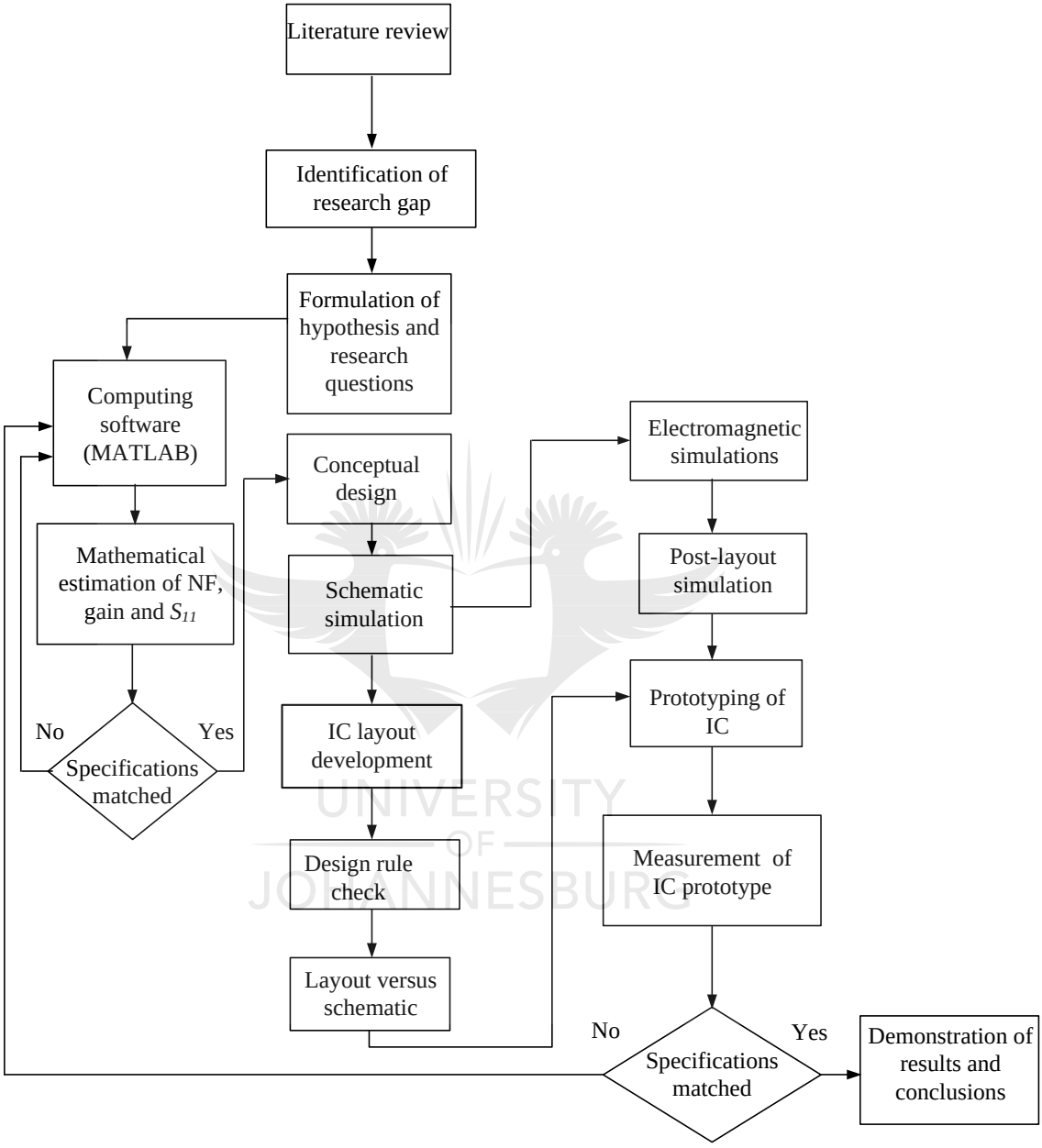

Figure 1.2: Research methodology adopted for this research.

If otherwise, the analytical approach would be re-evaluated. After the full design of the IC schematic is finalised, the first arm of schematic simulation connects to IC layout. The other arm of the schematic simulation links directly to electromagnetic (EM) simulations.

This was due to the limited capacity of the standalone/node-locked license. An in-depth generalisation cannot be established from the design of the experiment, but the initial "guess" will have been substantiated. The operating point of the transistor (Q-point) was selected by using the load line analysis where the collector current was plotted against the collector-emitter voltage (V_{CE}).

Once this had been completed, the schematic model of the circuit was drawn using Keysight Advanced Design System (ADS). Analytical modelling was used when selecting estimated values of the other components of the circuit. A full-wave EM simulation was carried out on the circuit to provide an estimation of parasitics and to allow the co-simulation and co-optimisation of circuit components. Once the desired parameter values were equal to the calculated values, the IC layout was drawn accordingly. With the IC layout completed, a layout versus schematics (LVS) verification process was used to check that the geometry (IC layout) conformed to the rules required for prototyping of the circuit. In the design rule check (DRC), the circuit chip was checked against the design rules before being sent for prototyping. To gain a suitable idea of the performance of the chip, a post-layout simulation was carried out and matched to the simulation results to check for the discrepancy in the actual design. The layout was transformed to a graphic database system file and prototyped using the 130 nm SiGe HBT BiCMOS process provided by MOSIS.

Once prototyping had been completed, measurements were taken. The measurement results were weighed against the simulations results. The measurement results will be documented and analysed. If the measured results and the post-layout simulated results are equivalent, then the hypothesis is viable. Otherwise, a justification and reasons for inconsistencies in the results are presented. At this stage, a theory can only be formed once the learning and building stages have been completed. Even if the hypothesis is invalidated, new evidence will be made available. A justification and reasons for inconsistencies in the results will be presented.

Two prototypes were developed and discussed in this thesis. The design and prototype that uses only the 130 nm BiCMOS collector-base-emitter-base-collector (CBEBC) transistor provided by Globalfoundries (GF) will be discussed throughout this thesis. The second design makes use of a printed circuit board (PCB) that was prototyped at IMT, Bucharest. The same schematic captured in chapter 4 and the topology discussed in this section are used for both prototypes. However, the dimensions of the MTL and the capacitors are different. After the successful design of the mm-wave LNA using ADS Keysight, the extracted parameter of the BiCMOS transistor and the connecting bond pads were transferred to AWR microwave office (MWO). In AWR MWO, the design using an ideal transmission line was used. A bias network, stability unit, balanced input, and output matching network (OMN) are used in the design.

On completing the design in AWR MWO, the transmission lines are modelled in CST microwave studio (CST MWS) using a two-layer PCB. The constituents of the design are the IMN, IMS and the OMN. The *S*-parameters of the IMN, IMS, and OMN are obtained via simulation of each structure. Thereafter, this is imported as a sub-circuit back to AWR MWO. In this design, the decoupling capacitors are also included. After this, the performance evaluation of each stage of the mm-wave LNA is observed. If it is satisfactory, the completed schematic drawing is then simulated in AWR MWO and the results are checked to determine if these meet the goal set in the hypothesis, a large 3-dB bandwidth and high gain while reducing NF. Other parameters observed include S_{11}, and S_{22}. With this completed, the prototyping of the mm-wave LNA can be carried out and the measurement setup for certain parameters using the vector network analyser and connecting wire can be achieved. A silicon substrate, ground made of a perfect electrical conductor (PEC) and aluminium metal, is used in the design of the prototype in the CST MWS. The results are illustrated in chapter 5.

Thus, in this research, a CC topology with the T-type MTL topology was used. CC topology was used to limit the NF of the proposed LNA. CC topology was preferred over CE topology because it reduces Miller capacitance at the input, and it enhances good

input and output isolation. The arrangement of the distributed elements as a T-type topology similarly achieves a much wider bandwidth, competitive gain, and NF.

1.5 DELIMITATION AND ASSUMPTIONS

The following assumptions and delimitations were considered in setting the boundaries of this research work:

For all measurements, a room temperature of 300 kelvin (K) was used. This was assumed because it is very difficult to measure the NF of the LNA accurately. Measuring at a low temperature reveals and increases the sensitivity level of the LNA. Likewise, measuring at room temperature allows the detection of any problem associated with the LNA quickly and easily. Since the ultra-low noise LNA must operate at a temperature below 300 K, such a temperature decrease results in a steady increase in gain, especially as the LNA cools. Moreover, measuring at low temperature allows increased sensitivity of the LNA.

The optimum source admittance, Y_{TOPY} (minimum noise temperature) was assumed to be equivalent to the optimum source impedance. This allowed an increase in the gain of the LNA. Coupled with the fact that the CC topology offered a high gain, the circuit gain would also increase. The gain at the noise temperature should not overtly differ from the gain at the room temperature, 300 K. Slight variability is expected, but not a large shift. Without measurement at other temperatures, one would not know if there is increased electron mobility at this temperature. An innovative circuit model was suggested to minimise variations in the *S*-parameters of the transistors with environmental temperature. It was assumed that when characterising the passives at different temperatures, there would be no variation in measured *S*-parameters despite the change in temperature.

In deriving a mathematical modelling for the LNA, a small-signal transistor model was derived based on the high frequency model. In the thesis, a resistor-inductor-conductance-capacitor (*RLGC*) TL, was modelled as a resistor-inductor-capacitor *(RLC)*

TL. The conductance, *G*, was assumed to be zero. This simplified the model used at the input matching for computing S_{11}. *G* is the conductance shunting the line specified per unit length. The value of *G* affects the geometry of the TL. *G*, which is based on the property of the dielectric, increases as the frequency increases. With *G* not considered in the mathematical model, one has a very useful and good approximation that can be described as a quasi-lossless TL. In this situation, $G = 0$, and *R* is not 0. Equating *G* to zero also results in no consideration of the DC leakage in the TL. The loss tangent used in the simulation is completely ignored.

Since *G* is entirely due to the property of the dielectric, the details of the width, breadth, and height for the dielectric are ignored in this estimation. Likewise, *G* is needed in determining the actual power loss of the TL. Thus, loss of the TL is not modelled. In this case, one assumes that the dielectric is ideal ($G = 0$). Another implication of this is that the loss of the TL would increase when the post-layout (EM simulation of the IC) is carried out, as well as when the prototype of the IC is completed.

Since the mm-wave design methodology encompasses interconnect modelling, which is virtually treated as a TL, if the length increases beyond 250 µm, it must be characterised in EM simulation software. The degradation evident in the interconnect system results in undesired signal coupling and resonances on the interconnect models as a result of the resistance and the interconnect inductance. However, in this circuit layout, the assumption is that the interconnect length is made considerably shorter in the layout. If the interconnect is longer than 250 µm, the desired goals of the hypothesis would not be met.

1.6 CONTRIBUTIONS

This dissertation outlines a few noteworthy contributions to the art of LNA design and prototyping at 60 GHz. The contributions are as follows:

The proposed technique was chosen following an exhaustive literature survey on existing LNA configuration at mm-waves in which the excellent performance and shortcomings

of each approach are highlighted in Table 1.1 and Table 1.2. Most existing mm-wave LNA configurations do not optimise all LNA parameters simultaneously. From the configuration used in this thesis, it has been shown that minimising NF and maximising gain while ensuring wideband can be obtained simultaneously.

The effect of an MTL on the LNA as a degenerative component for a CE topology was investigated. One of the observations from this simulation is that the MTL does not reduce the stability of the LNA; neither does it reduce the noise significantly. However, a benefit of this is that the gain of the LNA increases by nearly 5 dB.

The exploration of different topologies for the design of LNA was considered. The performance of both the CE and the CC topologies was checked before settling for CC at different stages of the LNA. An observation from this set of trials is that the CC contributes to the gain, while the IMN must be designed such that emphasis is placed on obtaining the minimum noise and reduced gain. Subsequent stages were designed for maximum gain.

A study was done of the "RF" characterisation of SiGe transistors at room temperature in terms of the equivalent circuit, using the *RLGC* model.

The design of a passive network of the mm-wave LNA in the CST MWS suite was successfully carried out. The design for the IMN and the IMS was intended to meet the prerequisite of the LNA. The prototype was designed and measured. The simulated value and the EM models (value) were re-introduced into the simulation to observe any difference.

The design of a two-stage LNA and its prototype was successfully demonstrated in the mm-wave frequency range (i.e. at 60 GHz). During this process, a 9.22 dB gain and a maximum NF of 6.22 dB were realised in the prototyped LNA. The design and drawing of an interdigital capacitor (IDT) at mm-waves that matches the design specification of the capacitor used at each stage were undertaken.

A study and analysis of the noise performance limitation of SiGe HBT were undertaken, considering the gain and predicting achievable system performance.

The IMN, OMN and IMS of the LNA in CST MWS were designed. During this process, the optimisation of each structure was carried out using a substrate thickness of 525 µm, metallic thickness of 1 µm, and ground thickness of 0.4 µm.

The prototyping of the IMN, OMN and IMS at 60 GHz frequency was done. Each matching network consists of CPW-to-MTL, IDT and the open-ended microstrip lines.

1.7 PUBLICATIONS

Part of the findings of this work that has been published in a peer-reviewed journal and international conference is presented. Conference articles published from the research activities include:

M. Fanoro, S. S. Olokede and S. Sinha, "Investigation of the effect of input matching network on 60 GHz low noise amplifier," *2016 IEEE International Semiconductor Conference (CAS)*, October 10-12, 2016, Sinaia, Romania, pp. 71-74.

M. Fanoro, S. S. Olokede and S. Sinha, "A low noise and power consumption, high-gain LNA in 130 nm SiGe BiCMOS using transmission lines" In *Conference Proceedings of 32nd International Union of Radio Science General Assembly and Scientific Symposium (URSI) General Assembly and Scientific Symposium (GASS)*, August 19-26, 2017, Montreal, Canada, pp. 1-4.

M. Fanoro, S. S. Olokede and S. Sinha, "Design of a low noise, low power V-band low noise amplifier in 130 nm SiGe BiCMOS process technology" *2017 IEEE International Semiconductor Conference (CAS)*, October 10-14, 2017, Sinaia, Romania, pp. 275-278.

M. Fanoro, S. S. Olokede and S. Sinha, "Effect of degeneration on a millimeter wave LNA: Application of microstrip transmission lines," *2018 IEEE International Semiconductor Conference (CAS)*, October 10 -12, 2018, Sinaia, pp. 283-286.

The following peer-reviewed journal article, approved by the Thomson Institute for Scientific Information, submitted by the author as part of his research activities, has been published:

M. Fanoro, S. S. Olokede, and S. Sinha. "Investigation of 60 GHz LNA with estimated S_{11} values based on mathematical model and numerical solution." *Romanian Journal for Information Science and Technology (ROMJIST)* vol. 19, no. 3, 2016, pp. 239-254.

Excerpts from the aforementioned articles will appear in parts of this thesis. While the copyright of such work is transferred, where applicable, to the publishers, there is understanding that the thesis avails for non-commercial purpose and thus the work is appropriately referenced. As it's the author's own work, the approach also abides to the fair usage principle.

1.8 OUTLINE OF THE THESIS

This thesis is organised as follows:

Chapter 1 provides a short context to the presented research. It details the motivation for researching this 60 GHz mm-wave LNA and contextualises the research gaps and the research questions to be answered. A sum-up of the research methodology and a statement identifying the research contribution to the existing literature. Thereafter, a list of articles (peer-reviewed) generated from this research is provided.

Chapter 2 focuses on the literature that is available on mm-wave LNAs. A brief discussion is conducted on LNA, the topology, architecture used, as well as the merits and demerits of each approach. In addition, matching network approaches associated with mm-wave LNA are discussed. Particularly, a comparison was made between the CE and

CC configuration, highlighting the benefit of each and its associated weakness. This chapter also addresses issues encountered in the prototyping of mm-wave LNAs. This chapter closes with the proposed LNA topology, the CC and T-type MTL topology, that yield wideband matching, good noise performance, and high gain concurrently for the proposed mm-wave LNA.

Chapter 3 details the step-by-step approach to answering the hypothesis questions. Thereafter, a discussion about the computer-aided design (CAD) tool used in the design and the reason why it was used is provided. The design process of the PCB, measurement setup, and hypothesis acceptance criteria are presented. Thereafter, the function of each item of equipment is highlighted and practical considerations during measurement are discussed.

Chapter 4 covers the circuit design and mathematical analysis of the 60 GHz mm-wave LNA. The detailed mathematical analysis of the IMN, the NF and the gain are shown.

Chapter 5 is devoted to the evaluation of the prototype by comparing the measurement and the simulated result in order to validate the proposed hypothesis. Practical considerations during measurement results are analysed. Inconsistent results obtained during experimentation are also explained.

Chapter 6 details the epilogue and evaluative assessment of this work and prospective expanse for imminent research are mentioned.

1.9 CONCLUSION

In this chapter, a brief compendium of this research thesis was presented. A research gap was identified and an approach to addressing this gap was formulated. The research hypothesis was stated and research questions that would be addressed were mentioned. A brief explanation of the research methodology was introduced. Delimitations and assumptions that were made during this study were presented. Contributions from the

work in terms of research output were emphasised as well. Finally, the breakdown of each chapter in the thesis and the subject matter discussed were listed.

Table 1.1: Simulated and measured results of the LNA designed for this research using the proposed topology compared to state-of-the-art measured LNA results found in literature.

Reference	Journal	Impact factor	Topology	Technology (nm)	BW [GHz]	$/S_{11}/$ [dB]	S_{21} [dB]	$/S_{22}/$ [dB]	NF [dB]	P [mW]	Area [mm^2]
[21]	*Electronics Letters*	1.23[1]	CC transconductance	65/CMOS	16.7	14	14.0 (est.)	17	6.1	9.6	0.59
[24]	*IEEE Microwave and Wireless Components Letters*	2.08[1]	Varactor + CC FET	130/CMOS	N/A[2]	13	13.5	9	6.8	N/A[2]	0.45
[24]	*Electronics Letters*	1.10[1]	CS+CC+SC	90/CMOS	12.5	14	11.4	16	3.88 @ 55.5 GHz	14.1	0.44
[25]	*IEEE Transactions on Microwave Theory and Techniques*	2.81[1]	CC	90/CMOS	15	12 @ 58 GHz	13.2	22 @ 62 GHz	3.78 @ 68.5 GHz	14.4	0.3

[1] https://jcr.incites.thomsonreuters.com [July 2019]

[2] Not Available

Table 1.1: (*Cont'd*) Simulated and measured results of the LNA designed for this research using the proposed topology compared to state-of-the-art measured LNA results found in literature.

Reference	**Journal**	**Impact factor**	**Topology**	**Technology (nm)**	**BW [GHz]**	**$/S_{11}/$ [dB]**	**S_{21} [dB]**	**$/S_{22}/$ [dB]**	**NF [dB]**	**P [mW]**	**Area [mm^2]**
[26]	*IEEE Transactions on Microwave Theory and Techniques*	2.81[1]	Magnetic coupled CC	90 LP/CMOS	17	17 @ 58 GHz	17	22 @ 53 GHz	4.4 @ 59.5 GHz	19.2	0.59
[27]	*IEEE Microwave and Wireless Components Letters*	2.08[1]	Gate inductive + CC	130/CMOS	4.5	28 @ 54 GHz	21	18 @ 54 GHz	7.6 @ 53 GHz	15.1	1.04
[28]	*IEEE Transactions on Microwave Theory and Techniques*	3.176[1]	Triple CC	90 LP/CMOS	N/P[3]	30 @ 56 GHz	12.7	25 @ 65.2 GHz	4.7 @58 GHz	18	0.19
[29]	*IEEE Microwave and Wireless Components Letters*	2.17[1]	Cascaded CS	90/CMOS	6	17	12.5 @ 57 GHz	N/P[3]	5.5 @ 54 GHz	4.4	0.47

[3] Not provided

Table 1.1: (*Cont'd*) Simulated and measured results of the LNA designed for this research using the proposed topology compared to state-of-the-art measured LNA results found in literature.

Reference	**Journal**	**Impact factor**	**Topology**	**Technology (nm)**	**BW [GHz]**	**$/S_{11}/$ [dB]**	**S_{21} [dB]**	**$/S_{22}/$ [dB]**	**NF [dB]**	**P [mW]**	**Area [mm^2]**
[30]	*Cluster Computing*	1.60[1]	CS	180/CMOS	12	12.15	11.29	12.24	1.82	N/A[2]	N/P[3]
[31]	*IEEE Transactions on Microwave Theory and Techniques*	2.81[1]	Transformer feedback + CC	65/CMOS	7.2	17 @ 54 GHz	25.4 @ 54.2 GHz	11	3.8 @ 53.9 GHz	19.8	0.11 (Without pads)
[32]	*Microwave and Optical Technology*	0.948[1]	Cascaded CS + in-stage TL	150/ pHEMT	N/P[3]	N/P[3]	13.5	N/P[3]	5.15 @ 61 GHz	4	NP[3]
[33]	*IEEE Journal of Solid-State Circuits*	4.075[1]	CC with differential-ended	130/ BiCMOS	30	8	25	10	< 7.2	52	0.5
[**This work**]	*Simulated*	N/A	CC+CC+T-MTL	130/ BiCMOS	6	19.8	20	8.5	6.13	32.2	0.4
[**This work**]	*Prototyped OMN*	N/A	CC+CC+T-MTL	130/ BiCMOS	3	15.7	9.21	6.22	6.22	N/A[2]	N/A[2]

[1] https://jcr.incites.thomsonreuters.com [July 2019]

Table 1.2: Summary of journal impact factors and cited *half-life* for literature consisting of comparable work.

Reference	Journal	Impact factor & half-life	Frequency band (GHz)	Contribution to body of literature
[15]	IEEE Journal of Solid-State circuit	4.075/8.5[1]	55-60/60	Development of algorithmic design methodology for mm-wave CMOS LNA and power amplifier.
[20]	*IEEE Microwave and Wireless Components Letters*	2.169/6.6[1]	43-67	Designing a wideband LNA using a gain enhancement shaping method for mm-wave LNAs in the V-band.
[34]	*IEEE Transaction on Microwave Theory and Techniques*	3.176/9.9[1]	54-69	Employing a parasitic insensitive linearisation topology in LNA design at mm-waves.
[11]	*International Journal of Microwave and Wireless Technology*	0.745/2.9[1]	56.6-61.5	Design optimised for low power consumption while ensuring area minimisation of integrated circuit using spiral inductor.
[35]	*Microwave and Optical Technology Letter*	0.95/6.5[1]	55-65	Successful implementation of 60 GHz LNA using commercially available RF-CMOS. The design employs a scalable microstrip TLs model based on EM simulation and available RF transistor.

[1] https://jcr.incites.thomsonreuters.com [July 2019]

Table 1.2: (*Cont'd*) Summary of journal impact factors and cited half-life for literature consisting of comparable work.

Reference	Journal	Impact factor & half-life	Frequency of band (GHz)	Contribution to body of literature
[36]	*Romanian Journal of Information Science and Technology*	0.29/8.4[1]	56 - 64	Mathematical technique to computing the S_{11} of an LNA. A flow chart, which details carefully from one stage to the next the method for designing and analysing the input reflection coefficient, was discussed.

[1] https://jcr.incites.thomsonreuters.com [July 2019]

CHAPTER 2: LITERATURE REVIEW

2. CHAPTER OVERVIEW

The design of an LNA at the mm-wave frequency bands has been particularly challenging for IC design engineers in both the industry and academia. Meeting the expected target in terms of design parameters has been hindered by transistor topology choice, semiconductor design parameters and the material used in prototyping of the IC. In this chapter, diverse transistor topologies used in the design and the prototyping of mm-wave LNA and related issues are discussed. Furthermore, fundamental concepts applied in relation to input and output matching, current process technology, progression in the scaling of transistors, cost implications, and economics of the process will be discussed. The choice of design topology for this work is also discussed in this chapter.

2.1 LOW-NOISE AMPLIFIER

In many cases, the design of an IC involves the integration of all miniaturised components on a single wafer, as well as combining several ICs in a single package (system in package). System-on-chip (SoC) meets the critical need and requirement of cost, performance, compactness and power consumption. The SoC approach is even better suited to measuring equipment used in the mm-wave frequency range. In designing chips, the efficient use of chip area is also important in determining the overall cost of an IC prototype.

An off-chip solution [37] reduces the area and introduces parasitics from the packaging interface, which degrades the overall performance of the IC used in designs compared to an on-chip solution. It is an advantageous approach for implementing discrete components, which are impracticable as an on-chip solution. If the required power and voltage level are higher than those provided on the Si substrate, an off-chip solution is implemented. On-chip inductors are known for large substrate area utilisation and a low quality factor (*Q*-factor), as their sizes do not scale down with advancement in technology, but scales with the frequency [38], [39]. At low frequencies, DC losses prevail. Skin effect at higher frequency increases ohmic loss, and these results to low *Q*-factor. A large substrate area decreases the effective inductance of the inductor. The *Q*-factor of the varactor is dependent on the VCO's *Q*-factor. It decreases as it approaches the mm-wave frequencies, i.e. a *Q*-factor value of between 5 and 7 at 60 GHz is obtainable at a channel length of 130 nm. A large substrate when described

with its schematic representation has a shunt capacitance that represents the electric coupling between the turns and the substrate's group plane. The shunt capacitance introduces a smaller inductance and limits the resonance frequency of the inductor. Substrate thickness decreases effective inductance further. Therefore, at any frequency, the decrease of the inductance is evident.

Inductance is a frequency-dependent effect, becoming more important at higher frequencies as the impedance of inductors increases [40]. When the inductance effect is undesired, it is called a parasitic effect and is often modelled in circuits as a parasitic element. Input resistance of the transistor is increased by utilising inductive emitter degeneration, sacrificing some gain, thus providing unconditional stability as well as simultaneous noise and input matching (SNIM). The emitter of the input transistor must have a return path of low impedance to ground ensuring that gain and input matching is not degraded [41]. Balancing and ensuring that the minimum noise figure (NF_{min}) is close to NF when the IC of a low power device is anticipated [12], [42] are of the utmost importance**.** Even when the desired architecture is selected, it must be selected to be robust enough, having high yield and low sensitivity after prototyping the IC.

Hence, EM simulators are used to determine the effect of parasitics before prototyping. This is essential in the design of wideband LNA at the mm-wave frequencies because interconnect parasitics and parasitic capacitances limit the bandwidth of mm-wave LNA. Some EM simulators are more accurate than others. Trade-offs inaccuracy includes extraction and computational time, computation cost, mesh density and simulation speed, all against simulation accuracy. 3D solvers such as CST MWS and HFSS consider the effect of conductor thickness and resistivity, which is not completely solved using 2.5D EM simulators (sonnet and momentum). 2.5D EM simulators mesh only flat metal surfaces while 3D simulators mesh the entire surface. Even though parasitic extraction is a necessary step, sometimes only parasitic minimisation can be realised. It is therefore important to find the interconnect that contributes most to parasitics in the circuit, since minimising parasitics does not always correspond to an optimised design. However, in some situations, it does correspond to an optimised design.

Once the desired topology has been selected, the balancing of the IMN and OMN is important. Established approaches that ensure proper matching with their different end-goals are highlighted in [43]. Power-constrained SNIM (PCSNIM) [44], power-constrained noise optimisation, SNIM and classical noise matching are a few of the LNA methodologies used at present [12]. To realise a higher gain and wider bandwidth [45], more LNA stages are required and extra power will be consumed. A rise in the number of stages is proportional to the increase in passive and distributed components used on the wafer and substrate area used. The design of each stage must be such that a stage handles the gain while another stage ensures wide bandwidth. Likewise, the design used at each stage must be efficient enough to reach the design goal.

However, the introduction of other techniques such as feedback might affect the overall performance of the IC. It decreases the gain, but it increases the stability and operating bandwidth of the IC. Reduction of the area of the capacitor is another way of reducing parasitics. With the aid of CAD software, the expected capacitance can be estimated. The reduction in capacitance comes at the cost of connectivity. Metals would require re-routing to reduce coupling and parasitic effects in the circuit, which might be possible in a simple circuit, but once a circuit with a dense layout with mixed-signal functionality is being designed, such approach becomes less effective.

Thus, a limited number of stages can be used. The gain for each stage is multiplied to get the overall gain must be beyond the gain of the active device used. The transistor frequency, f_T controls the gain-bandwidth (GBW) product. In LNA where feedback is introduced at different stages, the GBW is virtually independent of the gain at which it is measured. Negative feedback limits the gain of the amplifier but allows for large bandwidth. However, the overall gain must be beyond that the gain of the active device used. The transistor frequency, f_T controls the gain-bandwidth (GBW) product. In LNA where feedback is introduced at different stages, the GBW is virtually independent of the gain at which it is measured. Negative feedback limits the gain of the amplifier but allows for large bandwidth.

2.2 LNA ARCHITECTURE

Topologies are used based on the choice between single-ended (SE), differential-ended (DE) and balanced structure. SE is renowned for its ease and simplicity of design and the small

area used. DE is less sensitive to ground termination and does not require a coupling capacitor. DE reduces second-order distortion while rejecting common-mode noise [13], [47]. The balanced structure is less sensitive to mismatch, possessing good stability and phase linearity. Despite all the merits highlighted for each transistor topology, the SE problem with instability and sensitivity to the ground connection is still inherent. The DE requires two baluns, introducing losses into the LNA designed. Large area and stability issues are also pronounced. Irrespective of the shortcomings of the SE structure, it is widely used in the complete design and prototyping of the LNA. The SE structure including CE and CC [48] transistor topology is widely used. In this work, SE will be used in the implementation of the two-stage mm-wave LNA. The first stage is optimised for low NF and while the second stage, IMS, is optimised for gain and wide bandwidth.

2.3 TRANSISTOR AMPLIFIER TOPOLOGY

LNA design involves the use of different topologies. These include the common-base (CB), CE, CS and CC topologies. The most important points in assessing which topology to use in the design of an IC are the supply voltage, gain, and overall NF. Known advantages of the CC topology are the high frequency of operation, exceptional frequency stability at considerably high gain and high isolation between the input and output terminals. It is also able to nullify Miller amplification, as seen in the CE transistor of the CC topology [11], [49]. A shortcoming of the CC topology is large parasitic capacitance evident in the extremely high frequencies experienced between the input and output node, which contributes to reduced interstage impedance and gain.

CE has a reasonable power gain and smaller NF in comparison to CC, albeit having low gain. Evaluation of each topology or its selective combination (CE, CE+CC, CS+CC) determines which one would give optimal performance [33], [35] based on the proposed design goals, i.e. low NF and high gain. The CE is the driver of the LNA in the single-transistor solution. A CE amplifier offers high voltage gain and the highest power gain. It also has low output impedance, low conductance, and is relatively stable. Miller capacitance, $C_{bc,}$ degrades the overall gain, causing imperfect separation of the output and the input. It can be connected in CC, multistage configuration and a differential pair circuit.

In the CC approach, a CE input stage drives a low-impedance CB stage. CE, however, is easier to implement and has good linearity and output power. CC is identified for its high output impedance and high gain. Thus, with proper network matching, it experiences low loss in comparison with its CE counterpart. Isolation across the input and the output is improved. Nonetheless, at mm-wave frequencies, this topology is more sensitive to parasitics owing to the interconnection of the CE and CB transistors. Therefore, the gain is reduced almost to the equivalent gain value of the CE. Despite this shortcoming at the mm-waves, CC is found to be stable [50].

2.4 INPUT MATCHING OF THE LNA

An IMN in LNA design contributes to the LNA's performance by minimising the NF, maximising gain and ensuring stability. The choice of matching network elements is essential for optimising the NF. Output matching is of negligible importance unless it is important to drive an external filter. The IMN transforms the input impedance, Z_{in} of the driving transistor (transistor at the first stage) to the normalised input impedance, which is set at 50 Ω. An IMN occurs in two forms: a lossy or lossless matching network. Figure 2.1 shows three distinct models that make up the amplifier block diagram.

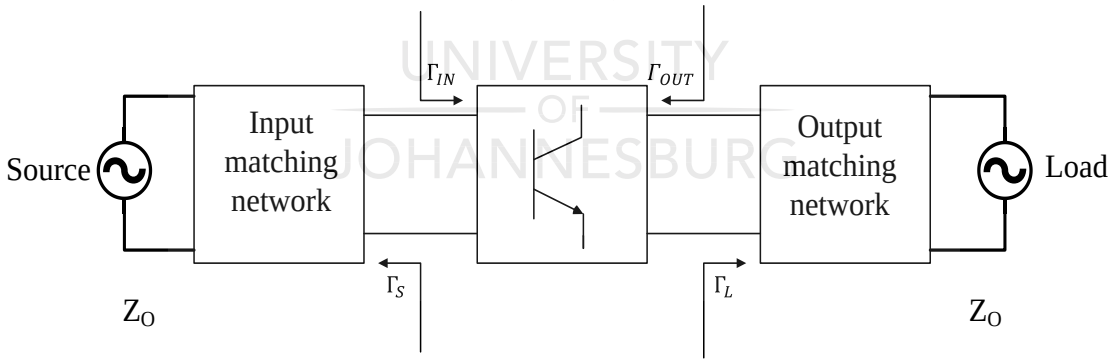

Figure 2.1: Block representation of amplifier circuit.

In Figure 2.1, the reflection coefficients at the input, output, source, and load of the LNA, represented as Γ_{in}, Γ_{out}, Γ_S, and Γ_L respectively, describe the impedance mismatch with respect to a reference impedance, Z_0, for both the source and load of the amplifier circuit. At the core of the block diagram is an active device, which requires biasing for good voltage amplification of the signal through a DC supply. Even though the OMN is of negligible importance, a normalised 50 Ω impedance must be transformed to the desired optimal source impedance, Z_{opt}[16],[46]. Once an LNA consists of more than a single stage, an interstage matching network is added to the design.

In this stage, the input impedance, $Z_{in,}$ is translated to the desired Z_{opt} value at the first stage of the LNA. The addition of the interstage is dependent on the gain performance realised from the first stage (active component). The lossy network (mostly consisting of resistors) is identified for offering flat gain response across a large bandwidth of interest while introducing a large amount of thermal noise and high transmission signal losses into the circuit. A lossless network, which can be used in the lumped or distributed form, is distinct for high gain and unconditional stability. However, the stability comes at the expense of matching to a 50 Ω input impedance.

The existing approach to designing an LNA is articulated well by following the "two-port network theory", where the characteristic impedance varies between 50 and 75 Ω. 50 Ω is widely used because it balances the trade-off between the power-handling capacity and the signal loss per unit length for an air dielectric. The *S*-parameters reveal the quantity of reflected power from one port to another; hence the term "reflection coefficient" was coined.

The simulation and modelling of the behaviour evident in matching network can be expressed in small-signal and large-signal analyses. *K*, the stern stability factor stated in (2.1), must be greater than or equal to 1 to satisfy the stability criterion, while Δ must be less than 1. With these conditions satisfied, the circuit would not oscillate.

$$K = \frac{\Delta}{2|S_{22} \times S_{12}|} \tag{2.1}$$

where Δ is expressed as:$1 + |S_{11}|^2 - |S_{22}|^2 + |S_{11} \times S_{22} - S_{12} \times S_{21}|^2$

where S_{11}, S_{12}, S_{21} and S_{22} are known as input return loss, reverse gain of the port, transducer power gain of the port and output return loss, respectively.

Practical trade-offs such as gain, voltage standing wave ratio [51], stability and bandwidth against NF must also be observed so that the optimum performance of the LNA can be achieved. It is expected that at a high gain, the NF would typically be low. Examples of other parameter trade-offs include current consumption vs. NF, bias current vs. linearity, bias current consumption vs. bandwidth, gain vs. linearity. The Friis equation establishes the relationship between the NF and the gain. The NF of an LNA is defined to a significant

degree by the first stage. Increasing the gain is achieved through the next stages of the LNA. However, it is necessary to ensure that the NF at the first stage is low. This is expressed in (2.2):

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3}{G_1 G_2} + \cdots + \frac{NF_{K-1}}{G_1 G_2 \ldots G_{K-1}} \tag{2.2}$$

In (2.2), *NF*, $NF_{1\ldots n}$ and $G_{1\ldots n}$ are respectively the total NF, NF and available power gain at the *n*-stage in a cascaded system. Another equation that shows the relationship of gain and linearity based on the Friis law reveals the relationship between the gain of the first stage and the input-referred third-order intercept point (IIP3) and it is expressed as:

$$\frac{1}{IIP_{3,TOT}} = \frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} \tag{2.3}$$

where G_1 is the gain of the first stage and $IIP_{3,tot}$, $IIP_{3,1}$, $IIP_{3,2}$ are the total, first and second stage *IIPs*.

2.5 ISSUES ASSOCIATED WITH THE MILLIMETRE-WAVE LNA

2.5.1 *Q*-factor

Distributed and lumped elements used in the design of ICs are distinguished by their *Q*-factor. Common examples of components in the above class are the metal-insulator-metal (MIM), capacitor, inductor, and TL [52]. Although the *Q*-factor of an inductor is relatively smaller than the *Q*-factor of the TL, what is traded off in terms of the *Q*-factor is regained in terms of the area utilised in the IC. A low *Q*-factor apparent in an on-chip inductor is due to the thickness of the metal layer and energy losses in the Si substrate [53]. Similarly, a low *Q*-factor degrades the NF of the LNA. The larger area utilised by the TL is proportionate to the length and the wavelengths. Hence at the mm-waves, wavelength is quite small.

A common example of TL is the MTL, which is recognised for its well-defined return current loops. It can also be routed easily, and it is less sensitive to modelling inaccuracy when compared to lumped elements. From the Smith chart shown in Figure 2.2, a high *Q*-factor is noticeable, especially when the input and output impedance matching, Z_{11}, Z_{22}, are considered respectively.

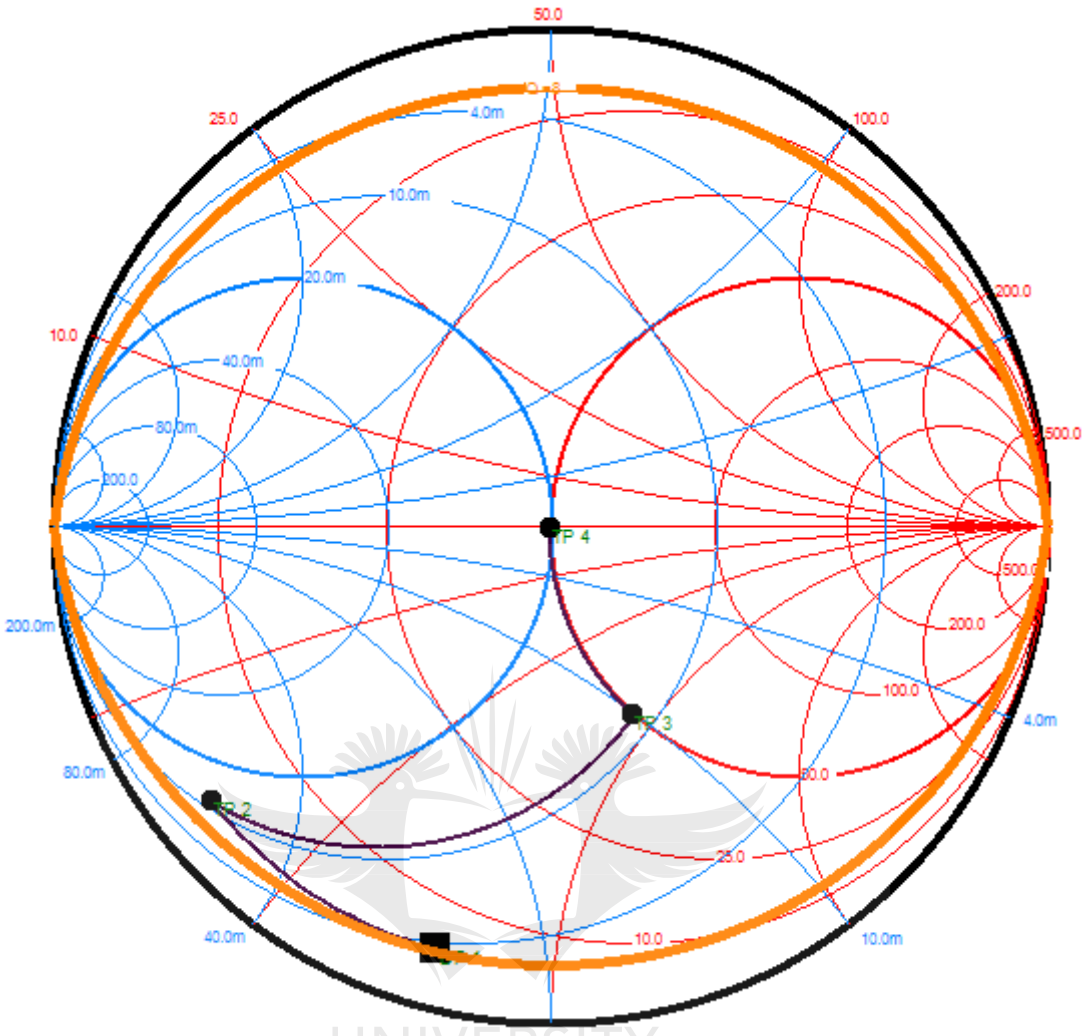

Figure 2.2: Smith chart showing the high Q-factor.

This point on the Smith chart, labelled "TP_1" is equivalent to low impedance, closer to the real line of the Smith chart with constant *Q* showing the *Q*-factor value. This point is matched to characteristic impedance of 50 Ω indicated by "TP_4". The matching requires a shorted MTL, TL and the inductor and this is represented by the movement towards "TP_4". An output matching impedance of high value has a detrimental effect on the gain, as it leads to reduced bandwidth of the designed IC. Increasing the *Q*-factor of passive devices can be realised in circuits by using a multi-stage matching network. However, with a higher *Q*-factor, the sensitivity experienced from component value variations and inherent interconnect/parasitics capacitance become very pronounced. A higher *Q*-factor translates into a narrower bandwidth, and this is undesirable for the mm-wave design, since it is one of the premium attributes of the mm-wave frequency range. Realising a higher *Q*-factor might be impractical because of losses from the Si substrate. These losses are attributed to factors such as substrate conductivity and high frequency capacity effects.

2.5.2 Substrate losses

Substrate losses also reduce the operating frequency of the designed IC. Nevertheless, reduction of energy loss in the lossy substrate improves the overall *Q*-factor of the inductor [53]. An unshielded coplanar waveguide (CPW) is rarely used in the mm-wave frequency range because of its high dielectric constant, about 12. As for MTLs, they are used because of the low loss per unit length. This comes though at the expense of a potential line-to-line coupling. In MTL, the introduction of a floating metal shield has the same effect, reducing energy loss from the lossy substrate significantly. The propagation mode of CPW being quasi-transverse electromagnetic (TEM) contributes to the high capacitance per unit length. It is therefore imperative to find the optimal *Q*-factor that would provide a wider bandwidth.

2.5.3 Parasitics that limit frequency of operation

The performance of the circuit changes significantly because of integrated parasitics. The change in response could be both detrimental and advantageous to the IC being designed. Deviation from the desired peak frequency and frequency response changes are examples of such undesirable changes evident in the circuit. Parasitic capacitance such as base emitter capacitance (C_{be}) and collector base capacitance (C_{bc}) is essential for determining f_{max} as shown in (2.4). The dependent variable of the GBW product of the transistor is described further in (2.5) and (2.6).

$$f_{max} = \sqrt{\frac{f_T}{8\times\pi\times C_{bc}\times R_B}} \tag{2.4}$$

$$GBW_{max} = \frac{g_m}{\pi\times C} \tag{2.5}$$

$$C = C_{bc} + C_{be} \tag{2.6}$$

where C_{bc} is the capacitance across the base and the collector, C_{be} is the capacitance across the base and the emitter; R_B is the resistance across the base; g_m is the transconductance of the transistor and GBW_{max}, the maximum gain-bandwidth product. Parasitics are known to reduce the maximum gain while having an increasing effect on the *NF* of the IC.

2.6 REVIEW OF PROCESS TECHNOLOGY

Process technologies used in manufacturing an IC have evolved significantly. Process steps such as lithography, etching, deposition and oxidation are used in semiconductor processing. The front-end and back-end processing and packaging of IC are very important phases in IC manufacturing. Current state-of-the-art technologies include SiGe HBT BiCMOS [33], SiGe:C, high electron mobility transistor (HEMT) [54], graphene field-effect transistor (GFET), metal-oxide semiconductor field-effect transistor (MOSFET), HBT, SiC, BiCMOS, SiGe HBT [55] and III-V semiconductors such as gallium arsenide (GaAs) [18] and gallium nitride.

GFET [56], a gapless semiconductor, has high strain limits, remarkable optical properties, electronic property, current-carrying capacity and high carrier mobility, which makes it a suitable future candidate in the design of high frequency circuits. It is known for its high f_T and f_{max} of over 100 GHz. Achieving high power gain using GFET is however, difficult. Likewise, impedance matching is another limitation, as the input port reflection coefficient tends towards less than 1. It also demonstrates lower speed compared to other technologies such as n-channel Si-MOSFET [57]. It has been projected that graphene could potentially replace Si. GaAs responds quickly to an electrical signal, making it a material of high electron mobility and high thermal stability. It has a high dielectric constant, which makes it a suitable medium for manufacturing a microstrip. Despite the above, it is much more difficult to manufacture and more expensive when compared to Si-based technologies.

HEMT displays unusual capabilities, showing low NF and high frequency characteristics, which can be useful for varieties of mm-wave amplifiers. A frequency of operation approaching 500 GHz is feasible. Despite this, it is more expensive when compared to Si, when considering manufacturing cost. Furthermore, its low thermal conductivity, substrate fragility and high leakage current are detrimental to its use at mm-wave frequencies. Si-based ICs can achieve the required level of integration at a higher speed, cost and yield than any other semiconductor materials.

III-V semiconductor technologies are made of alloys consisting of group III and V, as seen in the periodic table, i.e. GaN, AlGaN, GaAs and InN. Such alloys possess a much wider range of energy bandgap, high electron mobility and improved output power density, as well as a

lower level of integration compared to the Si-based technologies. Therefore, III-V semiconductor alloys have great potential in high-speed optoelectronics, solar cell development and high power-consuming and low current-consuming RF transceiver front-end applications [58], [59].

Complementary metal-oxide semiconductor (CMOS) technology is a dominant semiconductor technology used in the design and manufacturing of microprocessors, LNA, analogue circuits and ICs. Important advantages of this technology are the high computing power [60] and limited power dissipation during usage [61]. Integration of large, complex functions with higher yields and higher packing density is an added merit of CMOS technology. Low overall cost with large and high-quality production, power saving due to a low supply voltage and ease of integration with a high-speed semiconductor are key advantages of CMOS, which outweigh the disadvantages of low breakdown voltage and the lossy nature of the substrate [62]. However, it lacks the current drive capabilities displayed by BJT technologies. The noise level is an added drawback, as flicker noise is irrelevant at frequencies above 100 MHz, while shot noise increases as the frequency increases. This becomes obvious as its application approaches the mm-wave band.

BJT technologies have evolved over the last decade and their performance has improved when compared to CMOS and HEMT technologies. They offer higher switching speed, high current drive per unit [63], better noise performance, gain, high analogue compatibility and high reliability in severe environmental conditions. CMOS can compete with bipolar devices, since it offers lower power consumption. However, Si/SiGe:C gives better power gain and higher voltage swing [64]. The use of lower scale CMOS (90 nm, 65 nm, 40 nm and as low as 28 nm) technologies with higher unity gain frequencies (f_T, f_{max}) is one way of improving IC performance. However, downsides such as lesser breakdown voltages, diminished linearity [65], and scaling of the back-end metal cannot be avoided. Thus, BiCMOS technology came into existence, which retains the characteristics of both technologies (CMOS and bipolar) in a single chip. It has since evolved into SiGe HBT BiCMOS, which is widely used in IC prototype because of the combined advantages of both technologies. BiCMOS has superior low-current, higher frequency performance and a moderate breakdown voltage; it consumes moderate amounts of power and is optimised for integrated solutions. It

has been developed for 350, 250, 180, 130, 90 nm and, more recently, in 2017 [66], 55 nm SiGe BiCMOS processes.

2.7 PCB MODEL OF MM-WAVE LNA

With a proper choice of PCB material, a good result is expected after the prototype is accomplished. Through this process, low loss from active devices, minimal EM interference, minimal heat effects, and good impedance matching network is ensured. Generally, electrical loss effects limit the performance of MTL and have been studied. In mm-wave design, at least a one to two-layer PCB can be used. A chosen electrical property is D_f, the material loss tangent. The material loss tangent gives a measure of power loss owing to the material used. It varies as frequency increases. A low dielectric constant, D_k, known as the material relative permittivity, ensures rapid signal propagation in built structures. It decreases as frequency increases and it varies across different materials. In the same way, low power dissipation ensures that maximum deliverable power is transferred from ports in the prototype. The combination of D_f and D_k over the bandwidth of the intended application brings about consistent transmission line impedance in prototypes. Insertion loss [67] effects can be classified into three groups:

Dielectric losses are directly linked to signal attenuation. The increase in signal attenuation is directly proportional the frequency of the signal. Conductor losses [68] depend solely on the type of metal used for the transmission lines. Likewise, the increase in dimensions of the MTL increases loss. The material property of the PCB substrate material also plays a significant role in determining the conductor loss.

Radiation losses [69] can be attributed to many factors, such as the type of dielectric material, its thickness and the shapes of MTL structures on substrate. This type of increase in loss approaches the mm-wave frequencies. Highly increased insertion loss, changes in signal phase, and changes in resonant frequency can also be attributed to radiation losses. The number of discontinuities in an MTL circuit must be reduced to minimise radiation losses.
In designing the impedance matching of an LNA, the shape of a transmission-line discontinuity can influence the amount of radiation loss [70]. Sharper edges on junctions cause higher radiation losses than more gradual transitions in step junctions and coupling points, as used for impedance matching in low-noise amplifiers. A careful choice of dielectric

substrate, substrate thickness, and microstrip circuitry geometry can contribute to low insertion loss. The materials for the PCB include copper metal, a silicon substrate and a PEC used as ground.

2.8 130 NM BICMOS TECHNOLOGY PROCESS

130 nm BiCMOS technology process is realised through the integration of the SiGe HBT with the 130 nm CMOS process. The CMOS process benefits from continuous scaling of the technology node, seen clearly as the emitter width is reduced. However, the same cannot be said of the SiGe HBT node, where continuous scaling yields little or no change in the resultant f_T value [61]. The circuit reported in this thesis used the GF 130 nm SiGe BiCMOS technology (8HP), offering options of seven interconnection levels of global metal, with four levels of metal, and metal MQ and analogue metal (LY, AM) [71], with a starting substrate resistivity of between 10 and 20 Ω.cm [72]. The process features include a high-speed SiGe HBT with $f_T/f_{max}/BV_{ceo}$ of 220 GHz/280 GHz /1.8 V. This eight-metal layer back-end-of-line consists of an MIM capacitor and KQ resistors. Apart from the lumped elements, TLs and other distributed passives increase the necessity for EM simulations. The mm-wave technology process using 130 nm SiGe HBT is useful for high-speed and medium-voltage applications. The lines and inter-metal dielectric thicknesses are tuned to minimise attenuation of the signal and high frequency substrate coupling [73], [74].

The SiGe BiCMOS process for 130 nm [75]–[78] is known for its maximum f_T, which typically lies in the same range as a 28 nm RF-CMOS process, as reported in [61]. Thus, at present, SiGe HBT devices achieve f_T and f_{max} in excess of 300 GHz [78], with operable frequencies in excess of 100 GHz. SiGe HBT offers integration advantages, higher speed, excellent microwave noise behaviour, and low $1/f$ noise [76], exceeding the performance of Si and III-V semiconductor elements. The operable frequency of SiGe HBT has remained between 2 and 10 GHz, which is below 20 GHz, the frequency for III-V semiconductors [79]. CMOS technology, however, has a drive for more applications such as WLAN and 10 Gbps data communication. It was a direct shift from continual speed (f_{max}/f_T value) to high digital signal processing content, acceptable power dissipation, low phase noise and lower NF that resulted in SiGe BiCMOS technology. In the development of SiGe HBT, there is an increase of current density as well as higher NF_{min}, compared with low values of current density and lower NF_{min} [61], [73], [80], [81].

2.9 CHALLENGES FACING HIGH-SPEED CIRCUIT DESIGNERS

2.9.1 Power consumption

In the semiconductor industry, it has been difficult to scale the supply voltage of the HBT transistor. The central parameter that causes this is the voltage across the base and emitter junction, V_{BE} is given by:

$$V_{BE} = \frac{KT}{q} \ln \frac{J_c}{J_{co}} \tag{2.7}$$

where K is the Boltzmann's constant with a value of 1.3807×10^{-23}J/K, T is the temperature, q is the electron charge, J_c is the collector current density and J_{co} is the saturated collector current density. An increase in J_c gives rise to an increase in the V_{BE}. Associated with the scaling of the semiconductor process is the increase in f_T, which subsequently results to an equivalent increase in the current density. Thus, V_{BE} of the semiconductor process would likewise increase. In fact, it is as high as 900 mV [82]. The common approach in reducing supply voltages has largely been to reduce the number of transistors stacked in the circuit.

2.9.2 Dynamic range of low power high-speed links

The device breakdown voltage, BV_{ceo} is relevant to all semiconductor devices. High voltage blocking capability is common across all semiconductor technology, especially that used by power semiconductors. Gallium nitride and GaAs have higher BV_{ceo}, hence their wide application in power amplifiers. The Si family devices fall into the lower end of the spectrum with regard to breakdown voltage, which is very low. The merging of CMOS and Bipolar technologies, enhancing higher operational frequency, limits the swing of signal in the process. Technological scaling reduces the noise floor, improving the minimum NF of the transistor effectively. Dynamic voltage scaling, which is directly related to the dynamic range, expresses the variation and trade-off between power and operable frequency in (2.8):

$$P_{dynamic} = \alpha \times C_{Switched} \times V^2 \times f \tag{2.8}$$

where $P_{dynamic}$ is the dynamic power in Watts, $C_{Switched}$ is the capacitance in Farads, V is the voltage in volts and f is the frequency in Hertz. From (2.8), there are essentially four ways of

reducing power consumption $P_{dynamic}$: reducing the capacitive load $C_{Switched}$, reducing the supply voltage V, reducing the switching frequency f, and reducing the switching activity α. This relationship is further described using Figure 2.3.

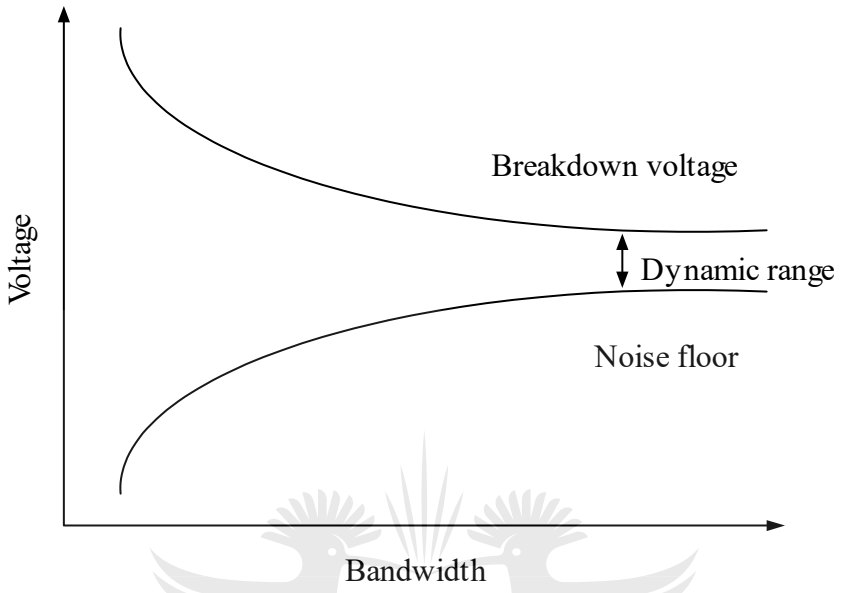

Figure 2.3: Illustration of dynamic range compression at higher bandwidths.

From Figure 2.3, reducing energy consumption means lowering the supply voltage and reducing the number of clock cycles, which is the frequency. Reduced frequency implies a longer time of execution. Increasing the frequency leads to an increase in power since the voltage is proportional to frequency. With increasing data rates, the dynamic range of high-speed serial links is reduced. As the data rate grows beyond 40 Gbps, the internal circuit noise becomes the central aspect of broadband receiver design.

2.9.3 Design cost

Even though the number of transistors per unit wafer is continually increasing, making SiGe BiCMOS a viable option for high-volume production, the further annual shrinking of feature sizes is having a detrimental effect on the semiconductor process. Since the process of shrinking requires a finer lithographic resolution, the cost of wafers has become extremely high. Therefore, the first pass design becomes very important in the prototyping process. Device modelling is the central challenge when the first pass design rate is considered.

2.10 CONCLUSION

In this chapter, issues relating to the LNA, the topologies and applicable architecture were highlighted. The merits and disadvantages of different and recently developed semiconductor processes that have been used in circuit design were also emphasised. Thereafter, details of the 130 nm BiCMOS process were documented. The role of the mm-wave LNA highlighted further in this chapter positions designers in an epoch when continual optimal solution and results regarding the LNA must be produced. The role of the IMN in regard to the NF will dominate the research industry for many years to come. Despite this, it is palpable that the present need is for designing and prototyping an optimal mm-wave LNA that can balance the performance of the NF, gain and wide bandwidth without trading off any of them. This is what this thesis resolves by utilising a CC configuration with a T-Type MTL topology.

CHAPTER 3: RESEARCH METHODOLOGY

3. CHAPTER OVERVIEW

In this chapter, the research hypothesis and mathematical modelling are discussed. Thereafter, a research methodology is developed for the purpose of this research work, to deal systematically with the research hypothesis. The research methodology for the design of the 60 GHz LNA design will be discussed exhaustively. The simulation tools used in this thesis are described, as well as each stage of the design process for which the corresponding tool was deployed. The results from the schematic design and circuit layout of the final IC prototype are further used to corroborate the hypothesis.

A small-signal-equivalent circuit, which represents the RLC relationship of the IMN, is mathematically analysed and verified using the high-current transistor model (HiCUM) in the mm-wave (56-64 GHz) frequency range. This model predicts the high-current operation of the devices. Likewise, since the LNA is intended for amplifying a very weak signal, a small-signal analysis model is required to deliver a close match with measurement data. A flowchart showing the process is presented and explained in this section. Then, the DC and RF characteristics of the 130 nm BiCMOS transistor that will be used for the design of the LNA are reported and the choice of bias voltages and the chosen topology are discussed. Measurement and equipment setup have been described at the end of the chapter.

3.1 DEVICE SPECIFICATIONS

The 130 nm BiCMOS technology process is a technology node offering multi-project wafer program through the MOSIS. The process offers seven metal layers with substrate resistivity of between 11 and 16 Ω.cm. Because of a non-disclosure agreement (NDA), a considerable number of the process parameters that are not available in the public domain have been excluded from this thesis.

The supply voltage of the GF 8HP process allows up to 2.5 V. The metal layers provided are (copper layer) M1, M2, M3, M4, and MQ, while aluminium layers, RF wiring layer, LY and AM form the topmost part in the metallisation stack. Some of the devices used in circuit design, with their central specifications and considerations, are discussed in the following sub-section.

3.1.1 Transmission lines

The 130 nm BiCMOS technology process provides TLs comprising of a top metal layer (AM), with a varying option of MQ and LY metals at the lower layer. The width and the length of the TL can vary up to 25 μm and 1500 μm respectively and its frequency is as high as 200 GHz. In order to use a longer TL, multiple TL are connected in series, yielding a larger inductance with a narrow line width. However, the main decisive factor in respect of the length of a TL is the maximum bandwidth frequency. At low frequencies, longer TLs can be generated and at higher frequencies, shorter TLs can be realised. The desired bandwidth range dictates the length of the TL. The parameters for the TL are given in Table 3.1.

Table 3.1: 130 nm GF 8HP TL parameters.

Specification	Range	Unit
Frequency (bandwidth)	Between 1 and 200 GHz	GHz
Supported lengths	Between 180 and 36 000	μm
Supported widths	up to 25	μm

According to Table 3.1, the maximum frequency for the 130 nm GF 8HP TL is 200 GHz, ensuring at least a length of 180 μm. Stray inductance is reduced in TL by connecting the TL to the ground during simulation. It is necessary to verify that all contacts of the substrate are positioned at a distance of at least 100 μm away from the TL [83], [84]. If the interconnect is shorter than 250 μm, longer Mean time to failure (MTF) is assured, irrespective of its width. For a longer interconnect, a short MTF due to stronger EM condition would be observed.

3.1.2 Capacitors

The 130 nm BiCMOS technology process offers three categories of capacitors. The first is a hyper abrupt varactor, comprising of a thick/thin oxide NFET-in-Nwell MOS capacitor. It consists of a single nitride MIM capacitance, and a dual nitride MIM (DN-MIM) capacitor. In order to compute the desired capacitance, the input parameter for the length and width of the MIM capacitor must be specified. However, in addition to the input parameters, DN-MIM has a switch setting. This determines the number of middle plate (QY) contacts used in any situation. This allows the designer to trade-off capacitor layout density and device *Q*-factor performance within the pcell layout. DN-MIM is also known for its high voltage capabilities.

The aspect ratio controls the value of the width and the length of the MIM capacitor. It is, however, vital to note that the *Q*-factor and the aspect ratio have a particular relationship. For

the best *Q*-factor, the length of the MIM capacitor must be kept short. Since the *Q*-factor is key to this design, the width dimension is larger than the length, thus ensuring that the higher resistance path is as short as possible. Information about available capacitors is given in Table 3.2.

Table 3.2: Capacitances per unit area of 130 nm GF capacitors.

Model	Area capacitance [fF/μm^2]	Bias voltage [V]
HA varactor	*removed (NDA)	1.2 - 1.25
Single MIM capacitor	*removed (NDA)	0
DN-MIM capacitor	*removed (NDA)	0

In Table 3.2, the single nitride MIM capacitor in the 130 nm GF 8HP technology node removes any undesirable RF noise from the DC supplies which can contribute to noise in IC circuitry. The minimal value equation for the capacitance of a MIM capacitor at 298.15 K and 0 V can be estimated as:

$$C_{nom} = \left(C_q \times L \times W\right) + \left(2 \times C_p \times (W + L)\right) \tag{3.1}$$

where C_{nom} is the area capacitance at a definite bias voltage measured in volts, *Cq* and *Cp* are the area capacitance (LY-QY) of MIM and the perimeter term capacitance. The nominal capacitance of MIM capacitor in fF, valued at 298.15 K is presented as:

$$C_{nom} = (C_A \times L \times W) + \left(C_p \times 2(W + L)\right) \tag{3.2}$$

where L and W are the particular length in μm while C_A is the capacitance per unit area. The MIM capacitor is vulnerable to ESD and ESD protection ensures that MIM capacitors are protected.

3.1.3 Bondpads

The 130 nm BiCMOS technology process simulates the effect of the fringing capacitance [85] between the bond pad and the ground plane, in most cases M1. The M1 ground plane offers the lowest impedance shielding from substrate noise, with somewhat higher parasitic

capacitance compared to NS and BB. This model consists of capacitance, a ground plane resistance, a ground plane capacitance, and a diode. The bondpad model and circuit symbol used contain three terminals: the pad, the ground plane, and the substrate. The specifications of the bondpads are provided in Table 3.3.

Table 3.3: 130 nm GF 8HP bondpad specifications.

Model	Oxide area capacitance [fF/µm^2]	Oxide fringe capacitance [fF/µm]
Bondpad over metal	0.0032	0.0336

From Table 3.3, bondpad over metal has a capacitance per area of 0.0032 fF/µm^2. The bondpads were used to connect the IC on the die to the termination point on the package. Similarly, it was also used to test certain points on the IC estate when troubleshooting.

3.1.4 NPN transistors

The 130 nm BiCMOS technology process delivers a high f_T and high breakdown voltage transistor. HiCUM, an advanced, physics-based compact model that supports accurate predictive and statistical models of the bipolar transistor, was used in the design of the GF NPN transistor. The advantage offered by HiCUM [86], a physics-based approach, is the behavioural modelling approach. HiCUM can be used at mm-waves owing to its inherent high speed and high frequency on account of its integration with the CMOS technology. A four-node NPN bipolar transistor was used in the simulation and in the layout. The two different configurations that were available were the CBEBC with collector-base-emitter configurations, both having a single stripe emitter. The emitter width was kept constant at 0.12 µm while the emitter length varied between 0.12 µm and 18 µm. The design specifications for NPN transistors are given in Table 3.4.

Table 3.4: Design specification for NPN transistors.

Specification	Range	Unit
V_{BE}	0.70 - 0.76	V
Beta	100 - 900	-
f_T	180 - 240	GHz

From Table 3.4, the value of V_{BE} ranges between 0.70 and 0.76 while *Beta*, the current gain of the NPN transistor has a maximum value of 900. The frequency, at which the current gain of the transistor falls to 1 is between 180 and 240 GHz.

3.2 MATHEMATICAL MODELLING

Mathematical modelling [87] is the translation of the application area into tractable mathematical formulations. In microelectronics, it involves a proper choice of circuit elements that best approximates the actual behaviour of the mm-wave LNA circuit while following the well-defined rules and identification of underlying assumptions. At the heart of the circuit analysis is the transistor modelling.

Through this modelling, analysing and simplifying of the circuit is possible. With manual calculation, it's almost difficult to analyse circuits with its complex model as a large number of parameters is involved. Through this, scientific understanding, testing of change effects in complex models and decision making around circuit component is made possible. Likewise, the modelling provides insight and guidance required to understanding a complex circuit.

3.3 DESIGN METHODOLOGY FOR A 60 GHZ LOW-NOISE AMPLIFIER

In order to validate the hypothesis, a careful scientific method has to be used in this design. The expected NF, stability, current consumption and optimisation techniques were selected. From Figure 3.1, existing research work on LNA at 60 GHz was studied closely to determine the approach taken and the pitfalls of each process. The expected NF, gain, matching topology and the available electronic design automation (EDA) tools were highlighted.

Once this was completed, the complete mathematical model of the proposed circuit that described the characteristics of the proposed LNA topology was derived. Simulation and optimisation of components were calculated using MATLAB. Characteristics such as the NF and gain were analytically derived from the small-signal analysis. Once the above had been defined and completed, a GF process design kit (PDK) was imported into the selected and available ADS Keysight; its design manual was studied closely. The methodology used in this design is represented in a flow chart in Figure 3.1.

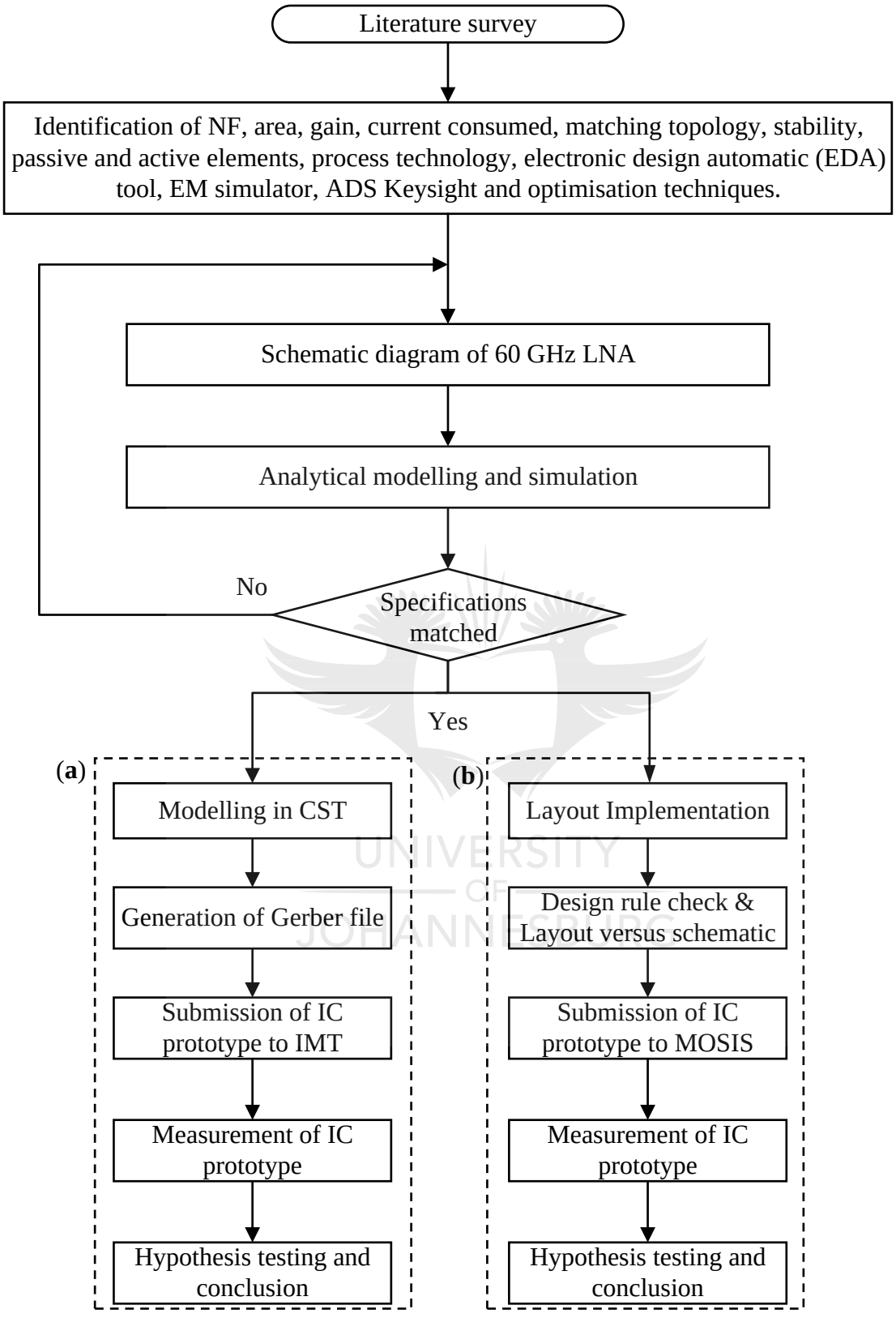

Figure 3.1: Flow chart for design methodology of 60 GHz LNA based on the (**a**) prototype of IC passives in IMT using a single layer metallisation ***(left)*** and (**b**) prototype of complete IC circuitry in MOSIS using GF PDK ***(right)***.

Once this had been done, optimum biasing, device size, input impedance matching, gain optimisation and extension to multistage could be carried out using Keysight's ADS. The implications of each of component value chosen were studied, offering the opportunity of varying the values. The varying of the values is better described as a fine tuning. The accuracy of the calculated results and the simulated results were verified by comparing values. Findings from literature review, simulations, and mathematical modelling give a foresight of the expected result from the prototype. The Q-point was selected by using the load line where the collector current, I_C was plotted against V_{CE}. On completing this, the schematic model of the circuit was drawn and when the simulation results matched the originally defined design specifications, the physical definition (layout) implementation was carried out. With the layout completed, LVS, which is used in checking the geometry of the circuit, was deployed. The layout was compared to the schematic of the chip. In the DRC, the circuit chip was checked against the design rules before being sent for prototyping. A full-wave EM simulation was carried out on the circuit to provide a prediction of parasitics and to allow the co-optimisation of circuit components. The parasitics were also extracted. Once prototyping had been accomplished, measurements were taken. In preparing for testing and measurement, the setup was calibrated according to a well-defined standard. This was used for characterisation and model extraction.

3.4 SIMULATION PACKAGES

Technical packages are required to conduct a carefully designed and controlled experiment, analyse the results from the experiment and draw a meaningful conclusion. Each of these tools gives an estimated value of the parameter to be used. The software programs might not necessarily be the best in the area of use, but the researcher was dependent on what was available. ADS Keysight, a comprehensive design platform, supports the multi-technology simulation based on the system level architecture. It also has dynamic link support [88], which can be used in the GF cadence design environment, where the HSPICE and SPICE netlist are generated. HSPICE and SPICE netlist extraction can also be linked to other EDA platforms. The 2.5D EM simulation capability available within ADS Keysight is preferable for RF designers. Despite this, CST MWS, offers a 3D EM platform for a high-frequency component. A slight drawback of the ADS Keysight platform is the inferior layout suite [89], when compared with the cadence virtuoso layout suite. Modelling and simulation of each phase of the design have been achieved. The precision of the results obtained is not reliant on

only the chosen software, but also on the intellectual capacity and expertise of the software user. Software packages selected in answering the research questions are listed in Table 3.5.

Table 3.5: Software packages used to answer research questions.

Software	Version	Functionality
MATLAB	R2014A version (8.3.0.532) (64-bit)	Mathematical computing
GF 8HP Process Development Kit	*removed (NDA)	DRC, LVS and layer density checks
Agilent Advanced Design System (ADS)	2016.01 version 4 (64-bit)	Schematic composer
CST MWS	2012.06	EM simulation
AWR MWO	2008 version 8.06r build 4290	Schematic composer

ADS Keysight 2016 was used in the design, simulation as well as executing DRC and LVS checks. MATLAB 2014 was used to optimise component values used in the initial estimation of S_{11} and S_{22} parameters while considering the use of lumped elements. The IMN, IMS, and OMN were modelled and simulated in CST MWS to test the performance of the simulated circuit in AWR microwave office (AWR MWO) before prototyping. An illustration that shows the software packages and their function at each research phase is given in Figure 3.2.

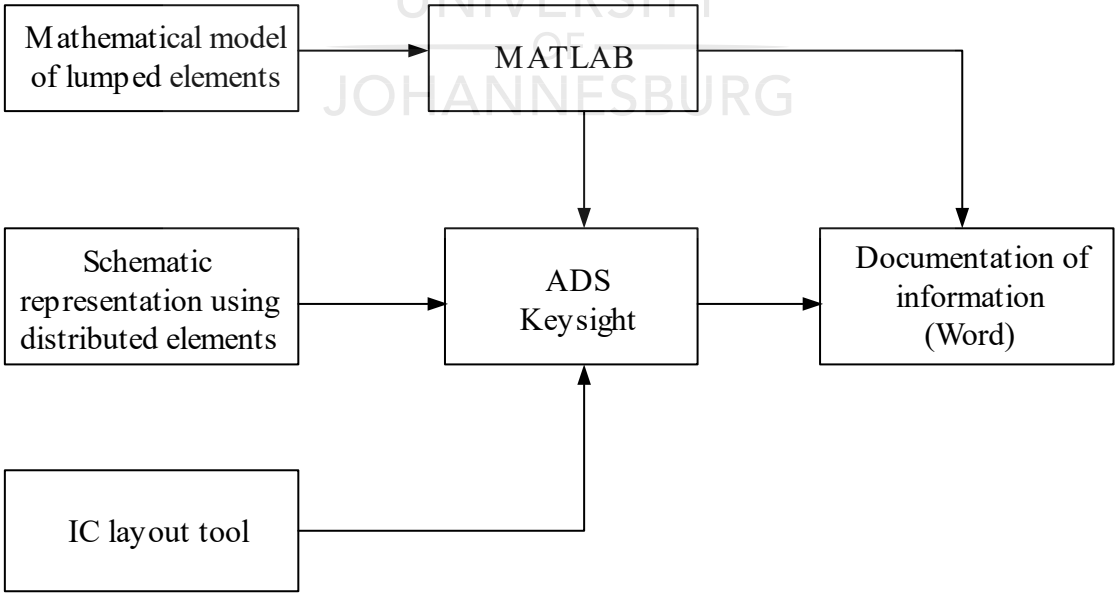

Figure 3.2: Block diagram of software packages.

In Figure 3.2, the blocks diagram describes the different steps taken during this research. These stages include schematic and layout simulations using ADS Keysight and

mathematical modelling of *S*-parameters in MATLAB. The modelling carried out in MATLAB was required to have an estimated value of the *S*-parameters, especially the *S*-parameter at the IMN. Once this is completed, the schematic and layout software programs are used in succession to validate the research hypothesis.

3.5 ELECTROMAGNETIC SIMULATIONS

The outlines of each EM structure were designed in CST MWS through the finite element method (FEM), and the *S*-parameters were acquired to assess the LNA performance, comparing this with the simulated result. CST MWS is a 3D full-wave EM solver suitable for layered media and handling the finite substrate, especially with the 3D models at all frequencies. The behaviour of high frequency components can be determined using the 3D FEM simulator. EM simulation improves the precision and reliability of the electronic simulation

In the next section, a brief description is given of CST MWS, other modules in CST, and its added functionality.

3.6 CST MWS

CST MWS [8], [88] is a 3D full-wave EM software for 3D simulation of high-frequency devices. The efficient computational solution provided by CST MWS is found useful in universities and research institutions. CST has facilities for co-simulation and multi-physics design and analysis. CST Studio Suite includes a collection of other modules among others, CST EM Studio, and CST Physics Studio. This multipurpose software offers a host of solvers, such as a time domain, frequency domain, multilayer and integral equation solver. These solvers are built on a variety of methods, such as the method of moments, finite integration technique and the FEM. The CST MWS uses a mesh system to analyse the 3D models and get the anticipated simulation results.

Modelling is necessary not only for design and optimisation of passive elements but also for analysis and simulation of implemented distributed passive elements and their parasitic effects. Full-wave EM simulation requires resources such as simulation time and processing capability. This method is computationally very expensive, non-economical, and time-consuming in cases where a specialised and dedicated processing capability is not available.

Nevertheless, full-wave EM solvers will be used in the final simulation, evaluation and optimisation processes of this research.

3.7 PASSIVE ELEMENT MODELLING AND DESIGN

Each passive BiCMOS component used in this circuit, including the decoupling IDT capacitor, is modelled individually using CST MWS. Thereafter, the results from CST MWS [90] are transferred into an EDA simulator, AWR MWO along with passive and active components. In this work, all the passive structures of the MTLs are modelled individually to compare the performance at the EDA simulator when the MTL structures are drawn in the 3D EM software. In each group, the T-topologies used in the circuit for the IMN and IMS are compared when used in EDA before prototyping and after this, measurements are taken.

Thereafter, equivalent two-port network models are obtained from the EM-simulation and imported into the EDA simulator. With the described model, the overall RF characteristics are obtained. This is achieved by re-simulating the circuit with its *S*-parameters in ADS Keysight. This approach is reliable because:

1. Inductive and capacitive coupling effects, of the distributed passive components are considered.

2. The material characteristics of each metal used in the stack-up are considered.

3. The high resistivity of the silicon substrate is considered while drawing the MTL in the 3D EM simulator. This high resistivity and the thickness of the silicon oxide isolate the device from the substrate at mm-wave frequencies.

4. The opportunity of optimising the width, length, and gap of the microstrip-to-coplanar waveguide (MTL-to-CPW) transition of the transmission line used in the 3D EM simulation for the MTL to achieve an optimised result is realised.

Figure 3.3 shows the block representation of the mm-wave LNA used in this work.

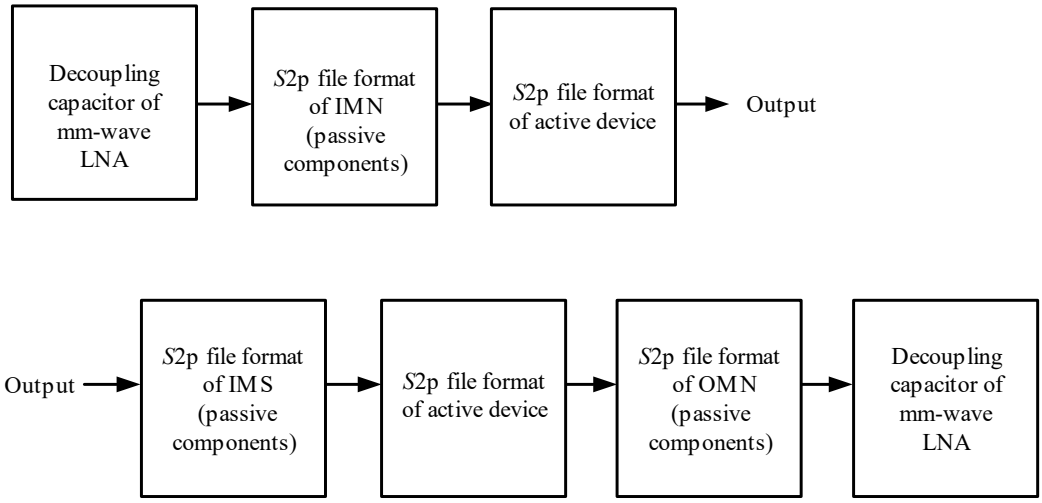

Figure 3.3: Block diagram of the mm-wave LNA.

From Figure 3.3, the decoupling capacitor is used to ensure that no current flows back into the Vector Network Analyser (VNA). After the decoupling capacitor, the IMN passive block made of a T-type MTL topology is modelled and simulated in CST MWS Studio. The first stage of the LNA is completed with the introduction of a CC network in the form of the *S*-parameter. This is only after it has been biased.

The IMS is also added to the mm-wave LNA block to enhance the voltage gain. The second stage of the mm-wave LNA is introduced with the *S*-parameter of the active device, configured in the CC topology and the OMN passive block composed of the T-type MTL topology.

3.8 AWR SCHEMATIC DESIGNS

The circuit schematics were implemented in AWR MWO. The simulation environment allows for fast design verification, and improved efficiency (tuning and optimisation for component parameters to enhance circuit performance). Simulation results acquired with AWR MWO were compared to the model using CST MWS before further steps were taken to prototype the different sections of the circuit.

Each sub-system of the circuit (IMN, IMS, and OMN) was designed independently to permit for an integrated approach, efficient testing, and robust verification process. The optimisation and tuning of component parameters and sizes were done using the AWR MWO and CST MWS.

3.9 HYPOTHESIS ACCEPTANCE CRITERIA

A single prototype was used during the measurement. The prototype was setup on the measurement equipment and evaluated at different points, making contacts with bond pads at a different location, while various bias conditions are evaluated. The objective remains to prove that the prototype can match the specification highlighted in the acceptance criteria shown in Table 3.6, thus validating the hypothesis. Table 3.6 highlights the tests and hypothesis criteria for mm-wave LNA. Based on Table 1.1 and Table 1.2, to make a state-of-the-art prototype, the NF, cut-off frequency, gain, and 3-dB bandwidth must be up to the specified values shown in Table 3.6.

Table 3.6: The test and acceptance criteria for mm-wave LNA.

Tests	**Hypothesis acceptance criteria**
Noise figure test	The NF must be between 5.0 dB and 6.5 dB.
High Frequency test	The cut-off frequency of the active mm-wave LNA should in the mm-wave range (V-band). It must be around 60 GHz (58 - 62 GHz).
Gain and 3-dB bandwidth test	The gain of the mm-wave LNA must be around 20 dB and flat across all the frequency of interest.
Power test	The total DC power dissipated by the mm-wave LNA (maximum achievable power must be in the mW range between 10 – 50 mW).

From Table 3.6, the technical boundaries of the experiments are described, supporting the formulated research hypothesis. It is the necessary guide ensuring the development of the LNA prototype in the mm-wave frequency band.

3.10 MEASUREMENT SETUP

The calibration substrate GBG CS-5 was positioned on the chuck of the on-wafer probe station connection in preparation for the calibration process. Calibration, a necessary procedure that removes the systematic errors associated with the measurement equipment up to the probe tips [59], [63], was carried out. A de-embedding procedure used to remove the effects associated with the on-wafer interconnects that serve as an interface between the

design under test (DUT) and the probes, such as transmission lines, pads, and vias, was also implemented. The calibration structures de-embed the probe from the circuit on the VNA before trying to measure, since at high frequencies the measurement itself becomes problematic and it is necessary to ensure the accuracy of measurements.

The specialised 40 MHz – 65 GHz Anritsu 37397D VNA connected with a frequency extender between 65 and 110 GHz consisting of GSG-100-67A probe needles of 1.85 with a 150 µm pitch was used for this measurement. This is represented in Figure 3.4. The Anritsu 37379D VNA (PM5/Suss MicroTek), depicted in Figure 3.4, is used to measure the *S*-parameters of the passive circuit. Calibration substrate GBG CS-5 was used in the calibration process between 40 MHz and 65 GHz. The on-wafer probe station connection to the Anritsu 37397D VNA depends on the high-performance GSG-100-67A standard probe needle, which is presented in Figure 3.5.

Figure 3.4: Anritsu 37379D VNA.

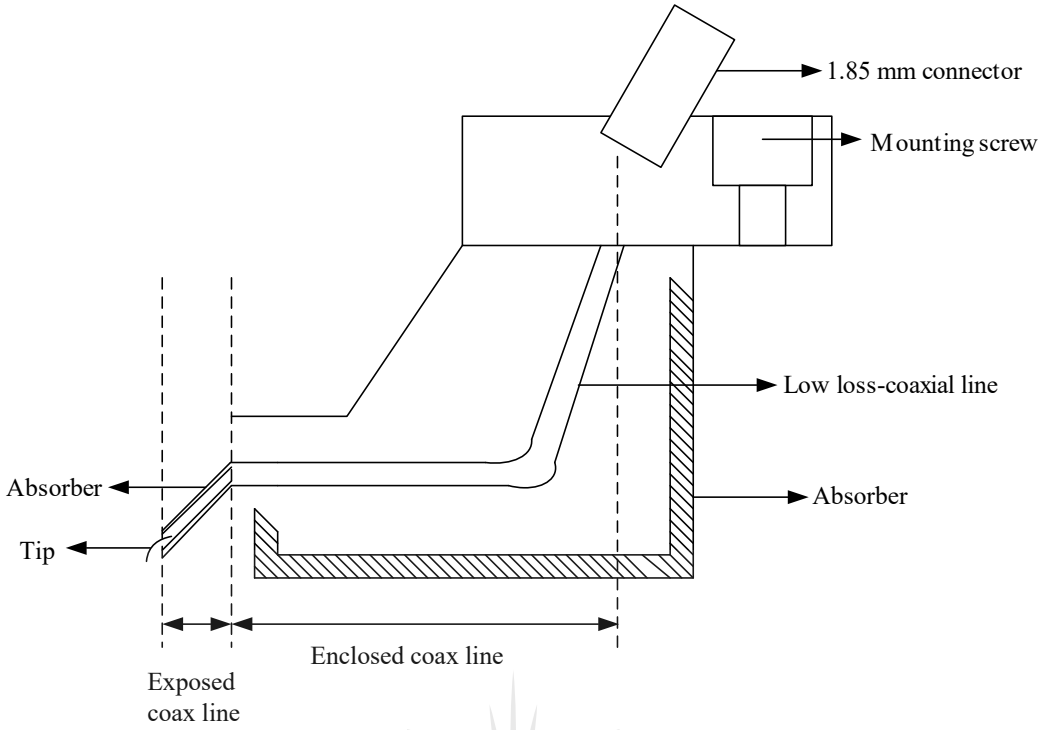

Figure 3.5: GSG-100-67A standard probe needle.

The GSG-100-67A probe needle, shown in Figure 3.5 can be manufactured using Tungsten or beryllium copper. It wears well because of its great hardness and is resistant to fatigue. Tungsten tips last longer than beryllium copper, given the same contact force. Despite this, tungsten's major disadvantage in some probing applications is that it produces highly inconsistent and unrepeatable contact resistance. It has a pitch ranging from 25 to about 1250 µm and can accomplish measurements from 40 MHz to 67 GHz and beyond through careful calibration, using the SOLT method [91]. Associated losses at higher frequency (greater than 67 GHz) can be compensated. The measurement setup is shown in Figure 3.6.

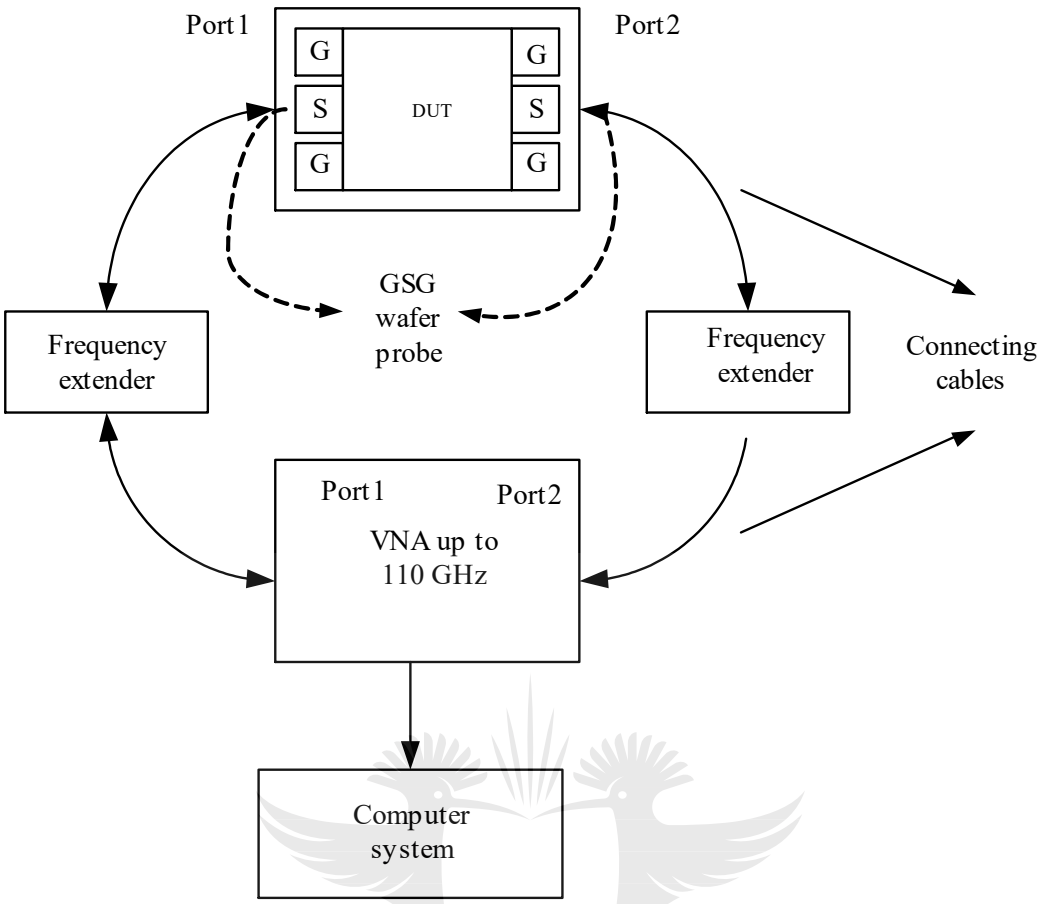

Figure 3.6: A typical measurement setup for on-wafer probing measurements.

This setup included the VNA along with a frequency extender, an on-wafer probe measurement station for DUT, a microscope, and a precision 3-axis XYZ positioner (manual). According to Figure 3.6, the DUT was positioned between the GSG-100-67A standard needle waveguide probes of the Anritsu ME7838A VNA. The positioning of the DUT was aligned through the microscope focused on the calibration substrate and DUT. The wafer chuck is the position where the centred DUT remains fixed, in contact with the microwave ground-signal-ground (GSG) wafer probe. The DUT was secured to a Si substrate with a PEC used as the ground plane. Si is very appealing to the semiconductor industry, as it has high dielectric strength, a relatively wide bandgap, stable insulator, and high temperature stability even up to 1873.15 K. The transmission line for the IMN, IMS, and OMN was made using aluminium.

The probe is connected to the frequency extender, which enables measurement from 65 GHz to 110 GHz. The cable used for the connection between the VNA and probe tips is coaxial cable suitable for frequencies up to 110 GHz, for which the nominal characteristic impedance

is 50 ohms. The losses associated with this described cable are well established. The SOLT calibration allows calibration of the setup in correspondence with the DUT'S ports, hence, considering also cables' and connectors' losses. A computer is used in the control and reading of the VNA. The VNA was configured to measure two-port *S*-parameters. The waveguide probe was attached to one end of a frequency extender. The XYZ positioner was used to ensure that the precision needed to place probe tips on the miniature test point was realised. The PC was used for controlling the prober and running the calibration/measurement software.

3.11 CONCLUSION

In this chapter, the device specifications for a list of components made available through the 130 nm GF design kit were highlighted. The RF characterisation was briefly discussed, paying attention to the IMN and the LNA at each stage. All passive elements were modelled and designed individually. Thereafter, a list of software that would be used in the execution of the design was itemised, stating the function of each and the stage where each item of software would be used was discussed. After this, a brief description of mathematical modelling in relation to microelectronics was discussed, with particular focus on its merit. Mathematical modelling will be discussed in the next chapter. Thereafter, the circuit layout and verification carried out in CST MWS was discussed. Finally, the measurement setup was presented.

CHAPTER 4: SCHEMATIC AND LAYOUT

4. CHAPTER OVERVIEW

This chapter describes the circuit schematic of the mm-wave LNA. The choice of the CC topology is justified again for both stages of the mm-wave LNA. Thereafter, the NF, gain and the input matching analysis are derived to show what parameter/component plays a noteworthy role in the overall performance of the circuit. With this completed, the layout drawing that focused on the whole circuit is discussed, stating the precautions taken and the procedures followed to ensure that the performance of both the simulation and the layout of the mm-wave LNA will be comparable and optimal.

4.1 CIRCUIT SCHEMATICS

The circuit of the LNA at the 60 GHz frequency consists of two stages and it was realised using a 130 nm SiGe BiCMOS process. Similar topology was used in both stages. In the layout, the MTL, tee, MIM capacitor and NPN transistor of a single emitter strip of 0.12 µm were used, at a width of 0.45 µm. The widths of the collector and base were 0.28 µm and 0.40 µm respectively. Transistors Q_1, Q_2, Q_3, and Q_4, used in the first and second stages respectively, had a single emitter finger of width 0.12 µm and corresponding length of 2.5 µm. The CBEBC transistor configuration was used in this design. Transistors Q_3 and Q_4 had a width of 0.12 µm and a length of 10 µm. The motivation for this design choice was to ensure that the desired gain would be realised. Figure 4.1 shows the schematic of the two-stage CC LNA implemented as part of the experimental work.

The first stage of the LNA, as shown in Figure 4.1, consisted of a CC configuration used at the IMN. The CE transistor, Q_1, was used in the input matching along with the T-topology of three MTLs of varying length and a T-type network arrangement. This approach provided for minimal current usage and a low NF by biasing transistor Q_1 at a low voltage, V_{BB1}, of 0.84 V. The bias voltage of V_{BB2} is 0.86 V. The CE transistor in a CC configuration was used without the inductive degeneration because the short stub TL [92] reduced the overall maximum gain and increased the NF. From Figure 4.1, the second stage consists of a CC configuration. For a successful multistage LNA design to transfer an RF signal from the first stage to the second stage, a matching network is required in between. The further advantage includes a minimum NF, satisfactory gain, and improvement in LNA's stability.

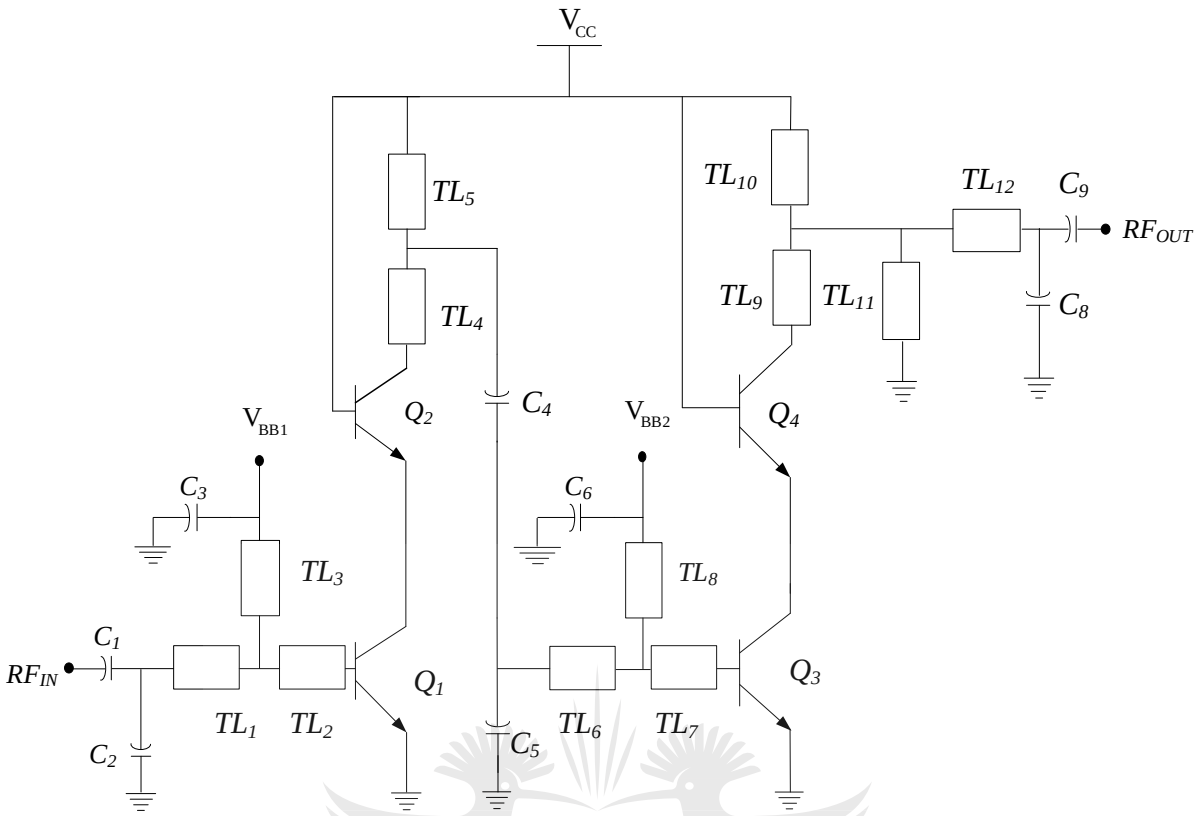

Figure 4.1: Schematic of the V-band LNA.

If this is not designed properly, the signal will be reflected, and this would lead directly to a decrease in gain and certainly affect the stability. The steps used in designing the IMS include simulating and equating on a Smith chart, the impedance of the input and output matching of the amplifier, i.e. the output of the first stage and the input of the second stage. IMS is made of a DC blocking capacitor, capacitor simulating the pad capacitance: C_2 and C_8 and a T-topology consisting of three single-wire MTLs of λ/4 wavelength, biased at 0.86 V. Single-stub tuners of length λ/4 are used in the IMN, IMS, OMN of the LNA. The IMS uses TL_6, TL_7, and TL_8, boosting the gain of the LNA in the process. This arrangement makes up for the discrepancy of the voltage gain, S_{21}, for the first and second stage of the LNA. In this circuit, V_{CC1} and V_{CC2} were both biased at 1.6 V.

4.2 MATHEMATICAL MODELLING OF IMN

The IMN and OMN are vital to the performance of the LNA, as they offer a distinctive function in determining the overall NF of the LNA. A T-topology network consisting of MTLs using a CE configuration [93], along with degenerative component, is used in the IMN of the LNA. An equivalent circuitry is shown in Figure 4.2.

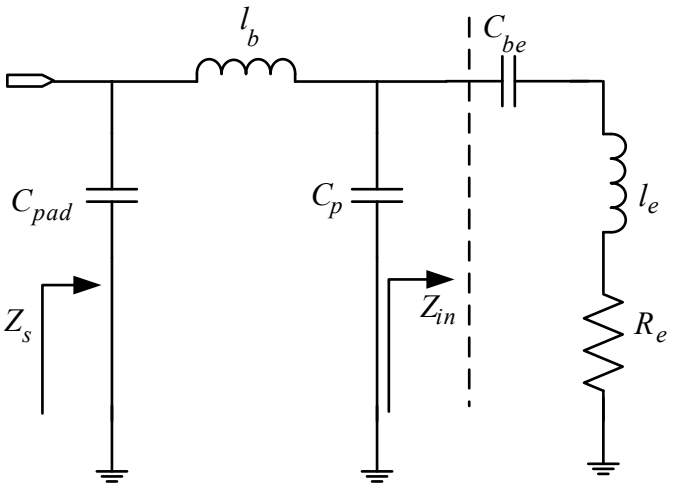

Figure 4.2: Equivalent circuit of the CE topology.

In Figure 4.2, the capacitances C_{pad}, $C_{p,}$ and C_{be}, as well as an inductive component at the emitter and base l_e, l_b and resistive component (R_e), are modelled mathematically to determine the response of the IMN. The resistance, R_e, is associated with the inductor (l_e), balances the real part of the IMN. A parallel connection exists between the pad capacitance (C_{pad}), and the parasitic capacitance in the base-collector junction, C_p. C_{pad} is incorporated as part of the IMN. l_b is an ideal inductor. The following matching conditions, (4.1), and (4.2) must be satisfied:

$$\omega_T \times l_e + r_e \cong R_s \tag{4.1}$$

$$\omega(l_e + l_b) = \frac{1}{\omega(C_{be}+C_{bc})} \tag{4.2}$$

where l_e is the inductor at the transistor's emitter; l_b is the inductor at the transistor's base; R_e is the resistance associated with the inductor; ω_T is the transit frequency; ω_o is the operable frequency; C_{be} is the intrinsic capacitance across the base and emitter junction and C_{bc} is the internal capacitance across the base and collector junction of the transistor. It has been proven from [71] that C_{bc} cannot be ignored when modelling at the mm-wave frequencies. From (4.2), l_e and l_b can be determined, since the value of ω_o has been identified. Figure 4.3 is a flowchart that shows the process of computing the resonant frequency and S_{11}.

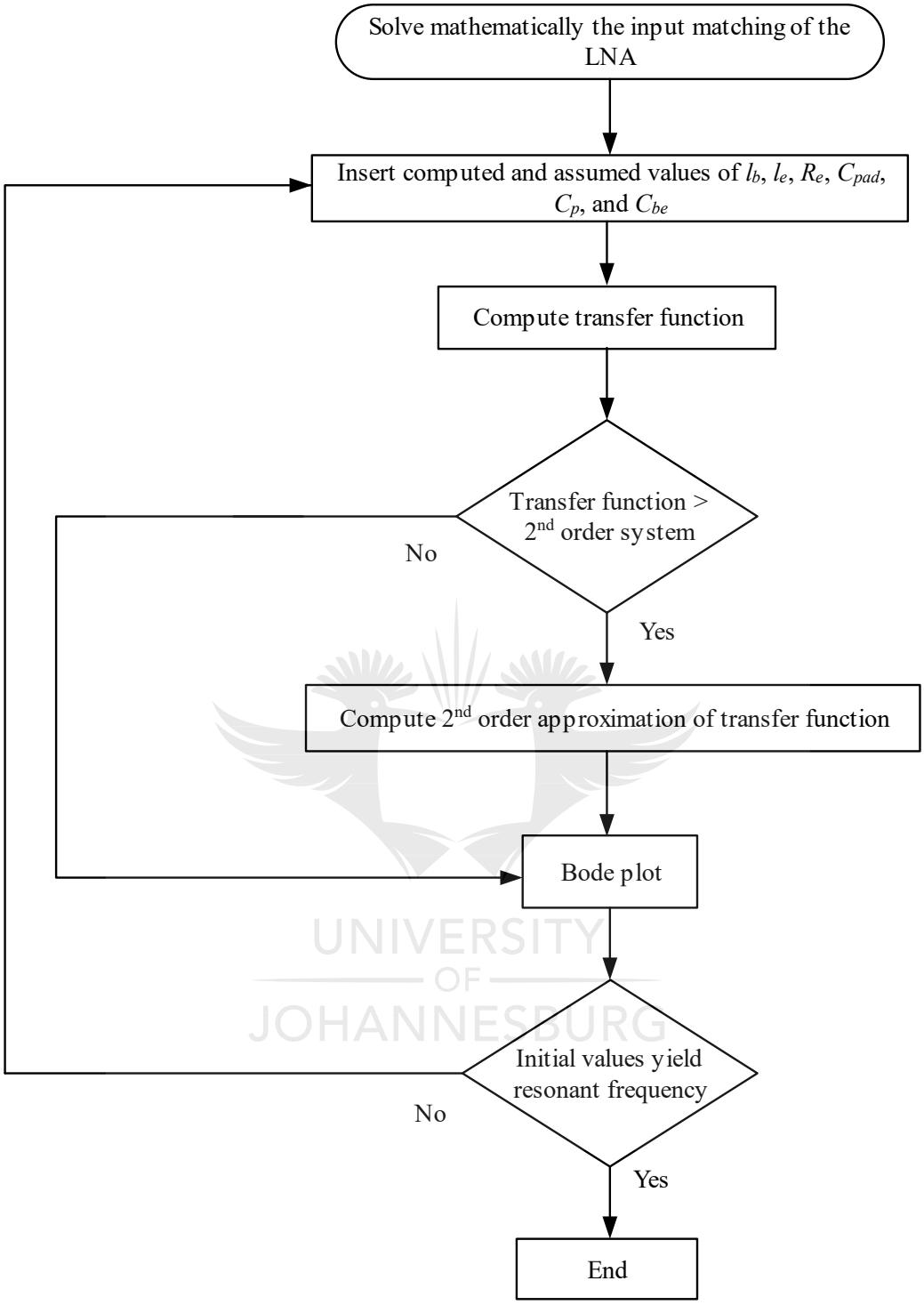

Figure 4.3: Flow chart of IMN.

From Figure 4.3, an initial assumed value used as a starting criterion for the simulation is provided. It is subsequently updated until the desired resonant frequency is computed. The transfer function of the LNA system consists of the coefficient of s, s^2 and higher order is realised. The higher order degrees are used in the estimation of the frequency response. A second order approximation is used to reduce the orders in the systems, and it is resolved using the Taylor's series. The mathematical approximation response to the 2nd order degree

can be expressed as a time invariant model. This can be described further using (4.3) and (4.4).

$$H(s) \approx \frac{b_o}{s^2} \tag{4.3}$$

$$H(s) = \frac{A(s)}{B(s)} = \frac{a_1 s^n + a_2 s^{n-1} + \cdots + a_{n+1}}{b_1 s^m + b_2 s^{m-1} + \cdots + b_{m+1}} \tag{4.4}$$

4.3 MATHEMATICAL ANALYSIS OF GAIN AND NF AT 60 GHZ

In investigating the NF of the mm-wave LNA at the first stage, the CE configuration, of the IMN, is considered. All MTLs were modelled as ideal MTLs during the noise circuit analysis, and the equivalent drawing is depicted in Figure 4.4.

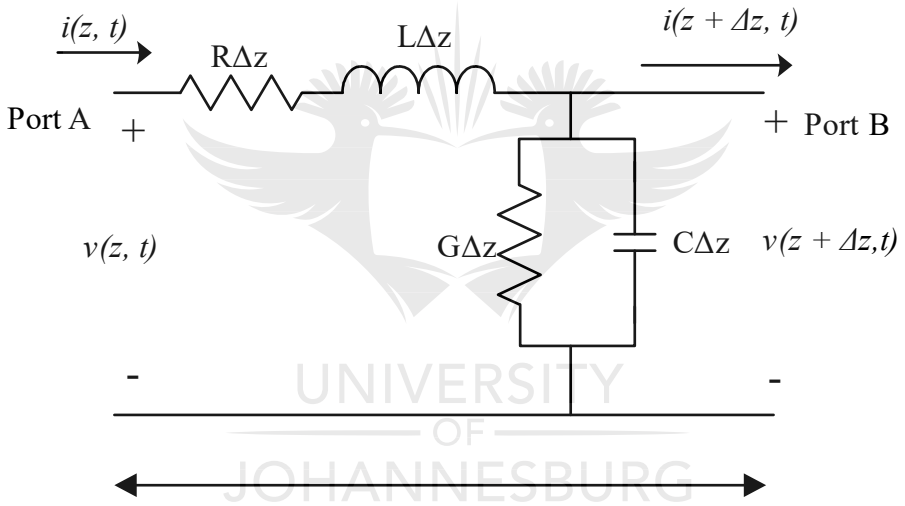

Figure 4.4: An equivalent circuit of an MTL.

In Figure. 4.4, the resistor, *R*, and inductor, *L*, of the MTL are in series with each other, while the capacitor, *C*, is in parallel with the conductance, *G*. All the electrical components are measured per unit length. Based on the values of *RLGC*, an estimated loss per length is introduced into the circuit where an MTL is used. The MTL conductor is assumed to be of zero loss, thus the conductance tends to infinity (zero). Miller's transformation was used, since capacitance across the base and the collector, C_{bc}, was not ignored but transformed, thus making the circuit analysis less complicated.

A small-signal equivalent circuit of the first stage was computed with its input-referred noise components. The circuit in Figure 4.5 is thus reduced to a simple "L" topology. The "L"

topology model was used in the analysis of the CE transistor with a high view of the "T" topology. The equivalent circuit with input-referred noise sources [94] using the CE configuration is described in Figure 4.5.

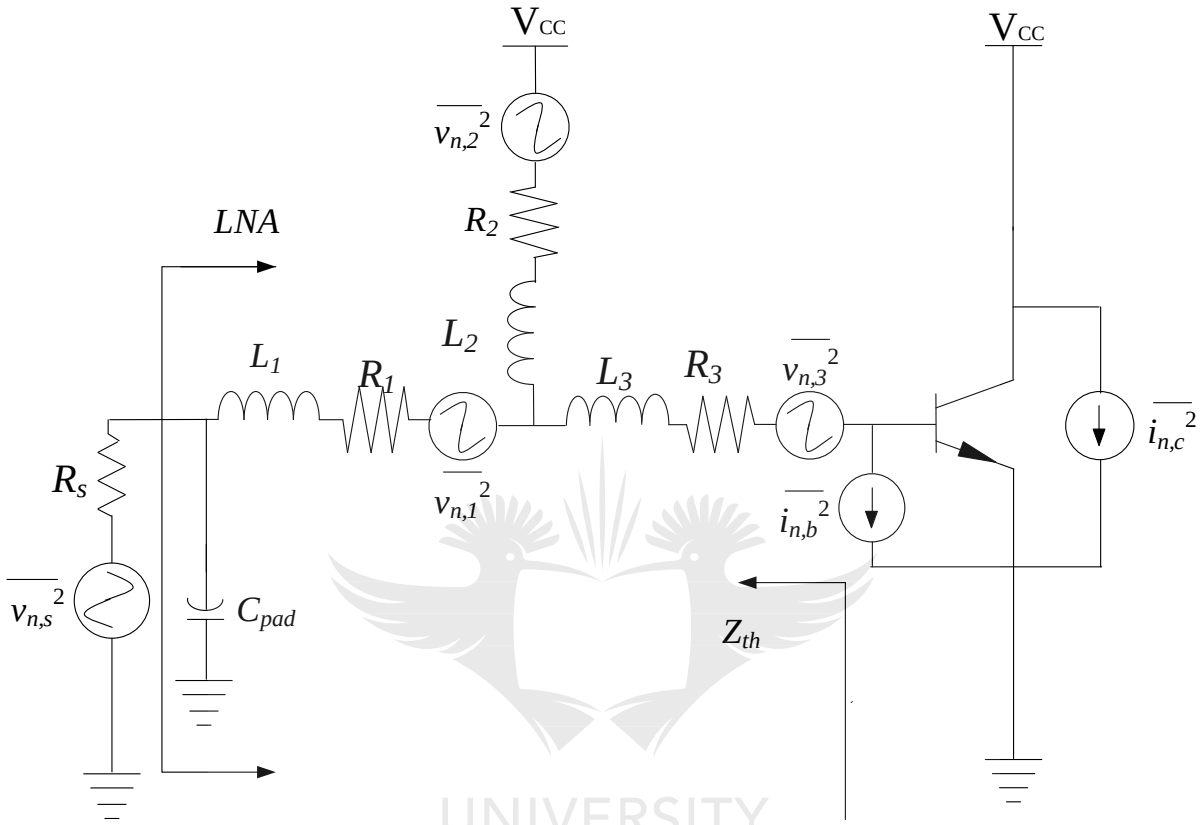

Figure 4.5: Equivalent circuit and noise sources in the 60 GHz LNA for the CE input matching.

Figure 4.5 includes noise sources from the collector and the base of the transistor, and the noise voltage sources due to MTL1 $(\overline{v_{n,1}^2})$, MTL2 $(\overline{v_{n,2}^2})$, and MTL3 $(\overline{v_{n,3}^2})$. In order to simplify the calculation, Thevenin's theorem was used in resolving Thevenin's impedance, Z_{th}, and voltage, V_{th}, before further analysis of the circuit could be completed. Capacitors C_2 and C_4, which are missing in the diagram, were ignored in the mathematical analysis, since current would flow through the pathway of least resistance. An inductor was introduced to cater for the inductance across the two transistors, CE and CB, in the CC topology.

The total NF using the CE configuration is expressed in (4.5) – (4.9):

$$NF = 4K_BT(Z_{th})^2 + 2qI_c\left(\frac{Z_{th}+J_1}{J_3\times ZC_{BC}}\right)\left[\frac{f}{f_T}\right] + 2qI_B\left(\frac{Z_{th}}{\beta^2}\right)(J_2) \tag{4.5}$$

where Z_{th}, J_1, J_2, and J_3 are:

$$Z_{th} = \frac{\left[(R_1+sL_1)\left(sC_1+\frac{1}{R_S}+sC_{pad}\right)+1\right][R_2+sL_2]}{\left(\left[(R_1+sL_1)\left(sC_1+\frac{1}{R_S}+sC_{pad}\right)+1\right]\right)[(1+[R_2+sL_2])(sC_3)]+\left[([R_2+sL_2])\left(sC_1+\frac{1}{R_S}+sC_{pad}\right)\right]} \quad (4.6)$$

$$J_1 = \frac{r_\pi(2sC_{BC}+sC_{BE})+1}{(2sC_{BC}+sC_{BE})} \quad (4.7)$$

$$J_2 = \left(\frac{V_{BE}}{J_1+Z_{th}} + g_m \times V_{BE}\right)(R_4 + sL_4) \quad (4.8)$$

$$J_3 = \frac{(2sC_{BC}+sC_{BE})+\frac{1}{r_\pi}}{(2sC_{BC}+sC_{BE})} \quad (4.9)$$

where Z_{th} is the total impedance when evaluating the impedance from the base of the transistor, R_4 and L_4 are the resistance and inductance of emitter degeneration; C_{be}, C_A and C_{pad}, and r_π are the capacitance related to the base-emitter junction, bondpad, base-collector junction, and the resistance across the base-collector junction respectively. The transconductance of the first transistor is represented by g_{m1}. The gain that can be realised from the circuit in Figure 4.5 can also be computed based on the diagram provided. This is given as:

$$Gain \cong \frac{J_1}{Z_{th}+J_1+\left(\frac{V_{BE}}{Z_{th}+J_1}+g_{m_1}\times(V_{BE})\right)(R_4+sL_4)} \times \left(g_{m_1} \times ZC_{BC}\right) \quad (4.10)$$

In the absence of the MTL degeneration [95] represented by R_4 and L_4, the gain of the LNA increases by some measure. The new expression for gain becomes:

$$Gain \cong \frac{J_1}{Z_{th}+J_1} \times \left(g_{m_1} \times ZC_{BC}\right) \quad (4.11)$$

where ZC_{BC} is the output impedance of the common-emitter transistor.

As for the input impedance, the idea of introducing degeneration, especially of the inductive type, was to increase the input resistance. An additional reason is that it moves the input impedance closer to the optimum reflection coefficient, decreasing the distance between the noise and gain match while ensuring simultaneous matching of gain and noise. However, this

does not apply to the MTL degeneration process. The presence of MTL degeneration at the emitter of the CE transistor tends to increase the NF and decrease the gain of the LNA. Alternatively, without the MTL degeneration, the NF reduces and the gain increases. In this derivation, the impact of Miller's effect on the input matching is included. The input matching, Z_{in}, can be expressed in (4.12):

$$\frac{V_{in}}{I_{in}} = Z_{th} + Z_{pin} + (1+\beta)(R_4 + sL_4) \tag{4.12}$$

where Z_{th} is Thevenin's impedance, Z_{pin} is the resultant impedance of the resistance across the base-emitter, the capacitance across the base-emitter and the Miller effect component. The resistance, R_4, and inductance, L_4, are the degeneration component of the MTL. Bondpads were placed in the simulation design, as this was going to model the external influences encountered when measuring the NF and *S*-parameters. Including bondpads will result in some parasitic capacitances. These can to some extent be reduced by the connected inductive wiring, but the overall effect will still be negative to the performance of the amplifier. It will also have a significant effect on gain and NF.

4.4 DRC AND LVS

With the results achieved, the translation of the LNA schematics to the layout includes the automatic generation of the layout from the schematics. Even though this was the case, there was a need to sort out, for analogue design, the footprint represented in the layout manually. In this design, it was necessary to check that any component used in the schematic could be reproduced in the layout easily, in the process achieving a real near prototype.

Figure 4.6 shows a top view of a complete representation of the LNA schematic. This drawing does not include the bond pad for the LNA testing. Bond pads have a special effect on overall circuit and system performance, especially wherever these are used as access points in the IC. They are commonly used in the IMN, IMS, and OMN of LNA, as well as the power amplifier. When these are introduced, bond wire and package pins are needed in the circuit. The structure of a bond pad includes the metal on the topmost layer, an insulator, oxide and silicon substrate. The effect of bond pad in circuit matching is noticeable both in the IC package and the chip-to-chip connection. A properly matched network would consider the bond pad network and this approach ensures that maximum power transfer is possible,

and the effect of reflection, mismatch and distortion is minimised [96], [97] and if possible, eliminated.

The equivalent representation of bond pad, bond wire and pin is an LC network. The bond pad is represented by the "C", which is capacitance, and the "L" represents the series inductance. Both components have values ranging from the 10^{-9} to the 10^{-15} region, the inductance having the lower value of the two. At millimetre waves, the transmission line must be introduced to account sufficiently for the effect of the bond pads [98]. At high frequency, intrinsic capacitance and inductance effects need to be minimised. Likewise, capacitive and substrate coupling losses [99] are considered in simulation.

The metals for power connection and the ground have also been included. Metal AM was used for the connection to the external power pad that will be used during the measurement and characterisation of the IC. The seven-layer version has two thick top layers, metal layers AM and LY.

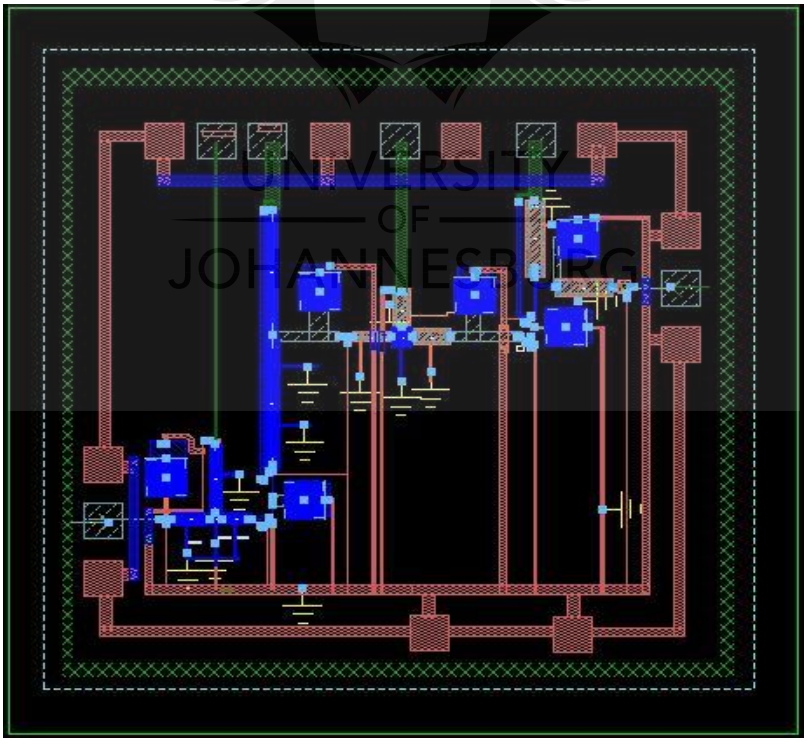

Figure 4.6: Layout for LNA at 60 GHz LNA without bondpad at the RF ports with a dimension of 1768 µm by 1746 µm.

According to Figure 4.6, in connecting some components, such as the MIM capacitor, it was important to add a metal to the lower layer, i.e. the signal layer (layer LY) to connect especially at the T-junction. The idea of merging or extending any metal destroys the property and orientation of the components in the layout. Therefore, traces were used to connect existing metals on the layout. In cases where layer LY was used, vias were added to ensure connectivity for the circuit. This is an innovative technique for limiting the physical length of metal and it is described in [100]. ADS LVS is used as a platform to validate IC layout design before it is submitted to the foundry. Through this process, the synchronisation of the schematic against the layout is verified. Figure 4.7 illustrates the result of the ADS LVS.

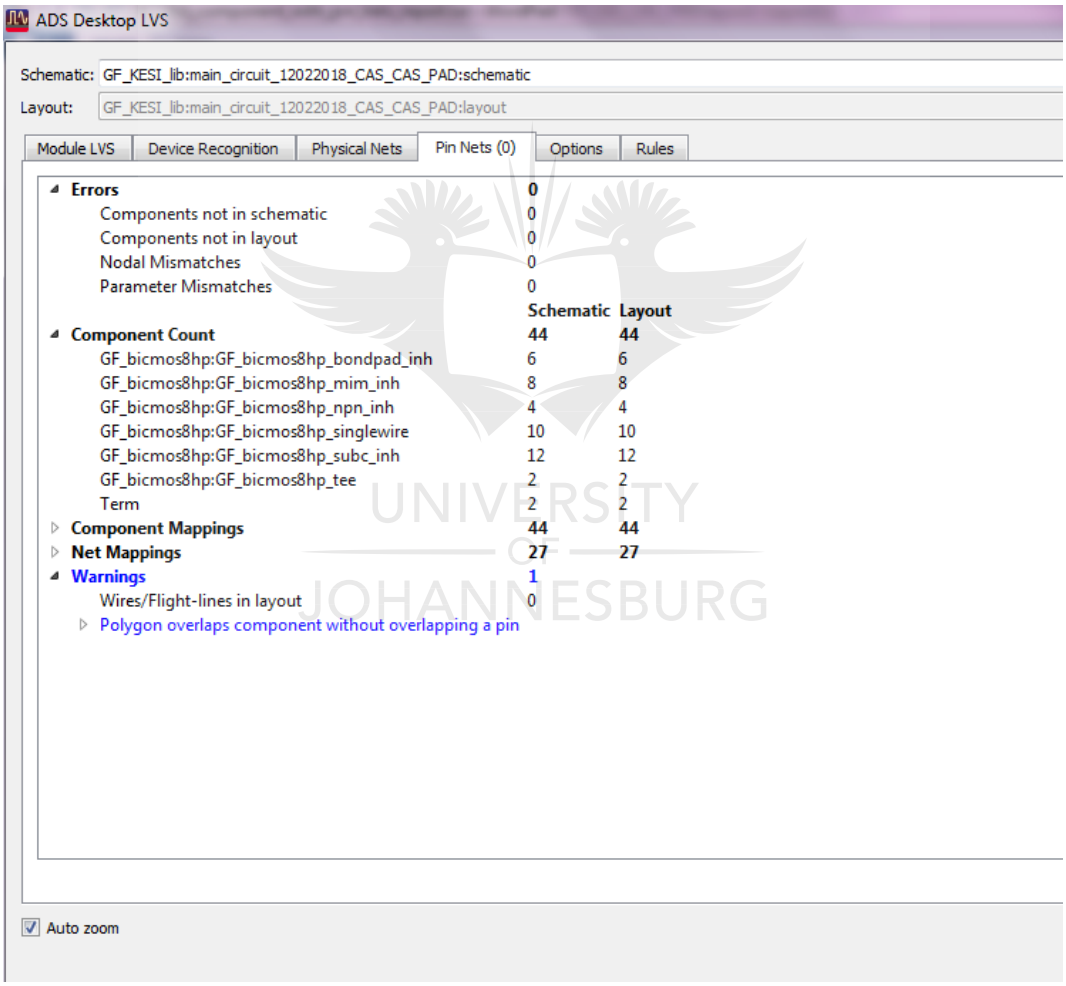

Figure 4.7: Snapshot of the ADS LVS results.

In Figure 4.7, the result of the ADS LVS test is shown. In this, no error was found. Likewise, component mapping and counts were equal when comparing the schematic and the layout. All the schematic and layout components with pins (one-to-one correspondence) were checked.

Through this process, the following can be achieved:

- Detection of missing component, nodal and parameter mismatch.
- Fixing of missing component and component count.

The LVS process can be carried out using the following approaches:

- ADS module LVS.
- ADS device recognition LVS.
- ADS physical LVS.
- ADS pin nets LVS.

In this work, the pin nets' LVS was chosen, since it checks the nodal connectivity and the physical nets that were used. Figure 4.8 depicts the picture of the ADS DRC test and the results.

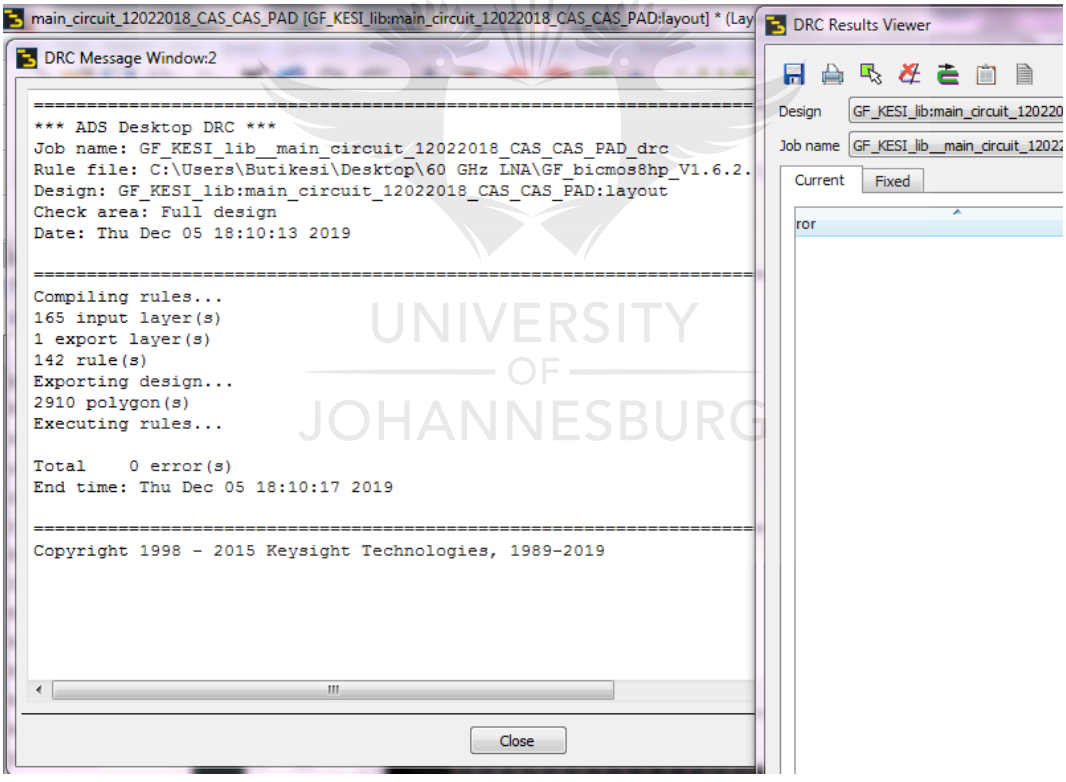

Figure 4.8: Snapshot of the ADS DRC test.

As shown in Figure 4.8, the spacing and width of the metals in their different layers have been complied with, yielding no error. The rules have been applied to the present design and the layout has been found to be consistent with the design rules. The DRC platform allows the layout design to conform to the physical constraints necessary for producing the IC.

Through this, rapid verification and continuous updating of the layout against foundry rules is possible. This is important before taping out of the IC. This limits to the barest minimum any reason for rejection associated with DRC violations from the foundry. Manufacturing grids, minimum width and spacing are some of the custom rules that are checked.

4.5 CONCLUSION

In this chapter, the circuit schematic of the mm-wave LNA was discussed and much attention was turned to the IMN and IMS. Design considerations before and during simulations were also explained. Thereafter, the mathematical analysis of the IMN with regard to the input impedance, NF and the gain was derived. Certain parameter considerations and omissions were explained in detail. The impact of the degenerative MTL was also proven mathematically to have no effect on the stability and the NF, as it did not reduce the NF nor did its absence cause instability in the mm-wave LNA.

CHAPTER 5: SIMULATION AND MEASUREMENT RESULTS

5. CHAPTER OVERVIEW

In this chapter, the 3D-EM modelling of the IMN, IMS and OMN was designed and simulated using CST MWS. Each modelling included the CPW-to-MTL transition, IDT and the MTL. The IDT was designed along with the CPW structure in CST MWS. Thereafter, the MTL for each of the stages of the LNA was also designed. A combination of these passive structures was used in the complete designing, modelling and simulation of the IMN, IMS, and OMN. The process of accomplishing this was shown diagrammatically and discussed, with the geometric parameters used, all presented in tabular format. After the design, the optimisation of the passive structure was carried out. With satisfactory results achieved for each stage, the passive prototype was fabricated and subsequently the *S*-parameters were measured, extracted in *s2p* format as scattering matrix and integrated with active devices in the 60 GHz mm-wave LNA. The simulated and measured passive structures were then compared. The *S*-parameters of each structure were then used in the AWR EDA software to plot the performance of the 60 GHz mm-wave LNA. Thereafter, a comparison of the simulated and the measured prototype was presented, identifying and investigating an uncorrelated result.

5.1 TRANSMISSION LINE DESCRIPTION USING THE EM MODEL

The circuit was simulated using commercially available AWR MWO and CST MWS was used in the design of the passive part of the 60 GHz LNA. The transistor and the distributed elements were simulated and optimised using AWR MWO. After optimising the dimensions of the distributed structures, i.e. MTL, the MTL was EM-modelled and simulated in CST MWS. In this design, the time domain solver is used for the EM simulation. The external boundary of the passive structures, particularly the ground of the structure (corresponding to the coordinate z_{min}), is set as “perfect electric conductor”, in the sense that all tangential electric fields and normal magnetic flues are set to zero. The EM structure requires a transition structure between the CPW line and the MTL, which enhances the de-embedding of the CPW to obtain the *S*-parameters of the MTL alone. The MTL structure of different lengths joined together, constituted as a T-topology, has been modelled and designed in the

standard silicon substrate with a ground made of a PEC, having similar dimensions as the substrate.

A high-resistivity silicon wafer, $k_{dielectric}$ of 11.9 prevents energy leakage through the substrate [101]. MTL is commonly used because of its compact size, low cost and ease of prototyping. This is depicted in Figures 5.1 and 5.2. The microstrip transmission line can be fed by the slot line and CPW [102], [103].

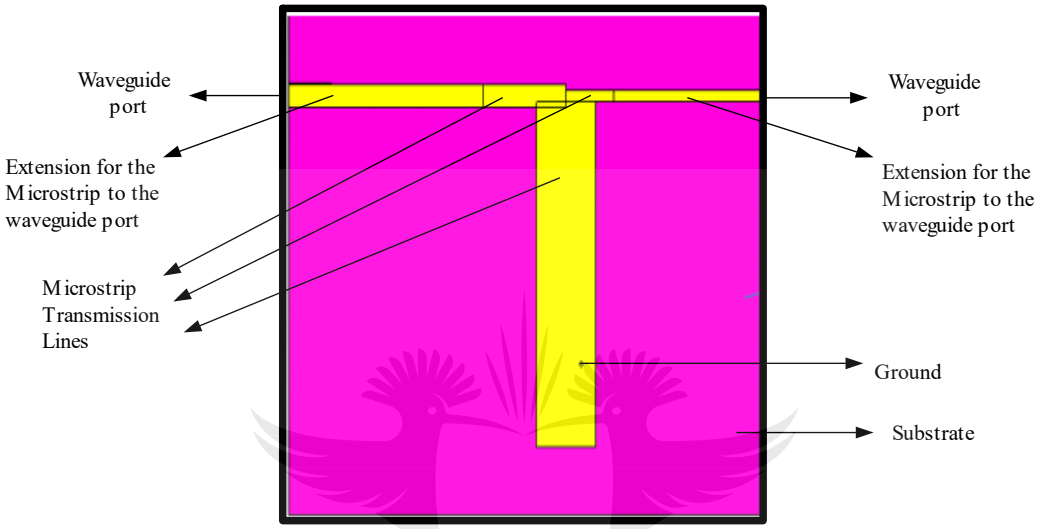

Figure 5.1: Simulated structure of the IMN over a high-resistivity silicon substrate in CST MWS.

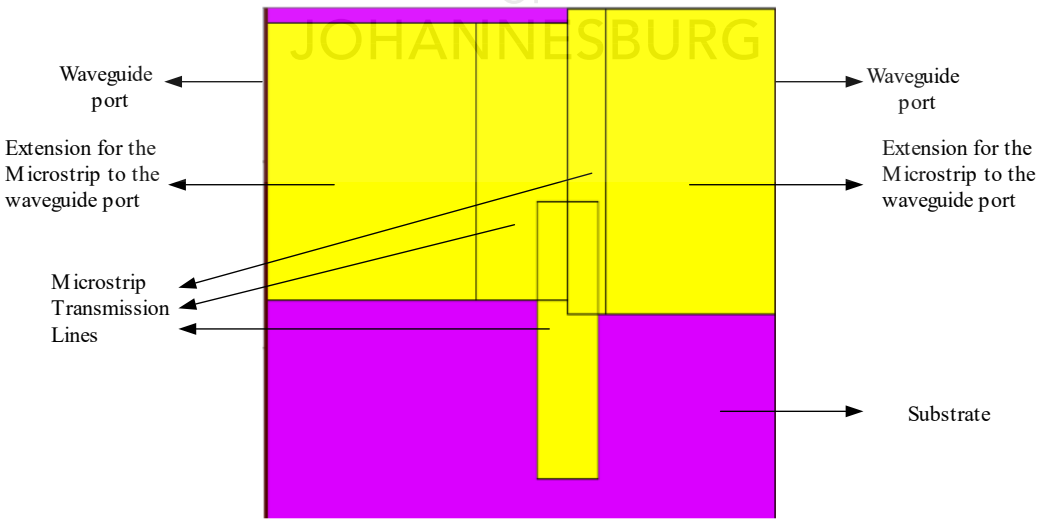

Figure 5.2: Simulated structure of the interstage-matching network over a high-resistivity silicon substrate in CST MWS.

Figures 5.1 and 5.2 show the structures that were simulated in CST MWS. Figure 5.1 describes the model for the IMN, while Figure 5.2 depicts the IMS model simulated in CST MWS. Each structure has a waveguide port, (50 Ω), situated on either side of the structure and with a perpendicular surface to the transmission line on which propagation of modes along the MTL is calculated. The "distance to reference plane" enhances the chance of obtaining accurate data about phase (*S*-parameter de-embedding). A negative value moves the reference plane inwards to the MTL while the positive values extend it in the opposite direction. With the value of "distance to reference plane" being negative, the effect of the extension achieved by adding extra length of MTL was removed from the *S*-parameter values. The transition from a CPW probe pad to an MTL is necessary. The transition used enhances a high level of integration as well as reducing the mismatch and coupling between the MTL and CPW. CPW feed was used. The CPW [104] is the feeding platform in which the side-plane conductor is the ground and the centre strip is the signal line. Vias are not required for connection to the ground, which is common practice in literature.

In order to evaluate these LNA at mm-wave frequencies, MTL-to-CPW [105], [106] transitions are required, since CPW are used, MTL-to-CPW transitions are required for the measurements of *S*-parameters, among others. Figure 5.3 illustrates the MTL-to-CPW transition platform further.

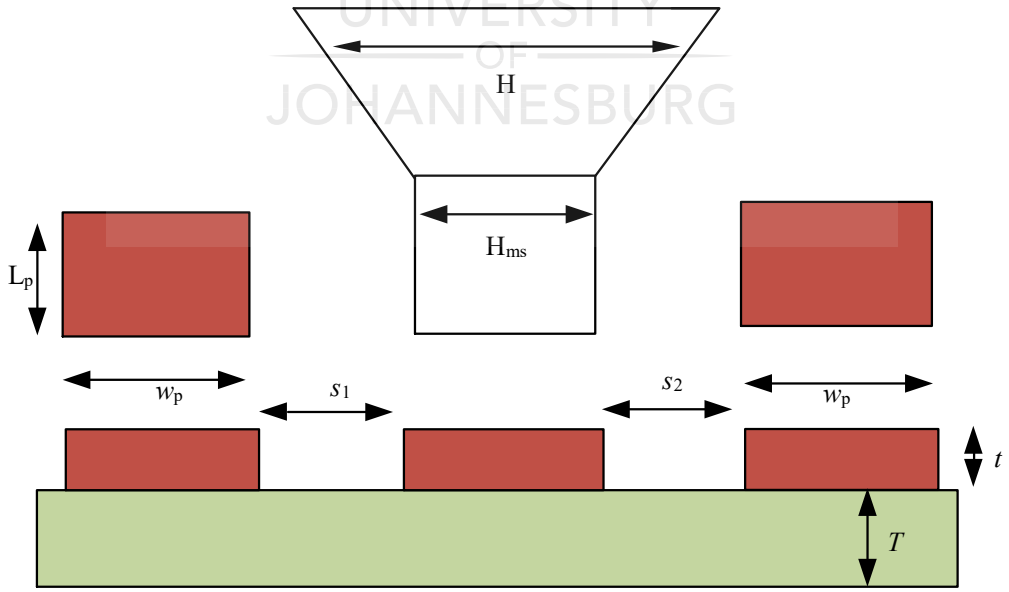

Figure 5.3: Top view and side view of the proposed CPW with ground to be used for the MTL passive structure.

Figure 5.3 shows the geometric dimensions of the MTL-to-CPW transition. Table 5.1 provides the definition of each parameter shown in Figure 5.3. All the parameters used in labelling the figure are described with their meanings and the value for the fixed and variable items are stated.

Table 5.1: Description of the proposed MTL-to-CPW transition.

Parameters	Generic representation	Value(s)
L_p	Length of the ground plane that is not rectangular	Variable
W_p	Width of the ground plane	Variable
H	Width of MTL	Variable
H_{ms}	Width of signal line	100 µm
s_1; s_2	Gap between the signal line and ground plane	60 µm
T	Thickness of substrate	525 µm
t	Thickness of the metal	10 µm
$\mathcal{E}_r$	Resistivity of substrate	11.9

Both ends of the MTL are connected to a waveguide port referenced to a 50 Ω impedance. The waveguide ports are surfaces perpendicular to the MTL on which the modes that can propagate along the transmission lines are calculated [107]. They are introduced to truncate the infinite line associated with the MTL without introducing perturbations. The ports behave like a perfect magnetic conductor with magnetic conductivity of zero (H_t = 0). The quasi-TEM propagation mode is the fundamental mode in open two-conductor-type transmission lines such as MTL and CPW lines. CST MWS allows the rigorous simulation of this mode once the geometry of the structure and of the ports has been well defined. The port of the MTL is checked to ensure that the mode of propagation is the quasi-TEM mode. In this mode, propagation is possible between two mediums: substrate and air with different speeds. A pictorial representation is presented in Figure 5.4.

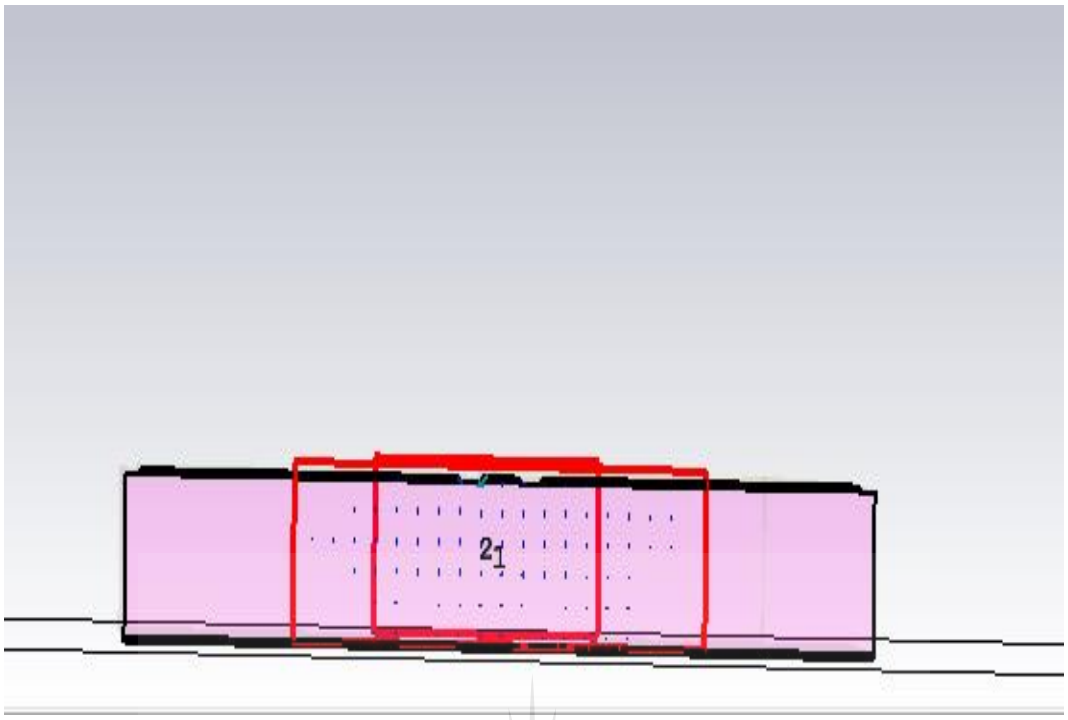

Figure 5.4: Quasi-TEM mode at the waveguide ports.

In Figure 5.4, the fields become zero theoretically at infinity, while the EM fields are perpendicular to the direction of propagation. It was necessary to ensure that no higher order modes could propagate in the port through the port sides. The width of the ground plane labelled as *Wp,* to a value that is far smaller than $\lambda/2$, guards against the propagation of higher order modes [108]. A fundamental mode was chosen for each port. In addition, the boundary of the waveguide is treated with PEC shield against the lossy silicon substrate, achieving extremely low insertion losses and ensuring proper de-embedding to accommodate frequencies at mm-waves. Since the characteristic impedance [109] of a CPW with practical prototype is different from that of the microstrip line designed for the LNA, the transition [102] must match the impedance differences between the MTL and CPW.

Through the transition of MTL-to-CPW, mismatch and coupling of different circuit components are reduced to the minimum. The production cost also decreases significantly. An advantage of using the GSG is that the CPW feed provides easy integration with existing MMIC technology on a single wafer. As is evident from the name, the microstrip line and ground plane of the CPW line share the same plane above the dielectric substrate. It is also easy to design, and it is not difficult to maintain a good matching impedance. A frequency-independent capacitance [110] is yielded through the ground plane defined beneath the substrate.

A substrate of high dielectric constants (i.e. silicon substrate, with an epsilon of 11.9 and an effective epsilon of 6.57) was used in this design. Since the gap around the signal line of the CPW is constant at 60 µm, the gap around the MTL-to-CPW might vary. It might be smaller or bigger than 60 µm, thus changing the behaviour of the MTL and the point of resonance of the matching network.

The impedance calculation was performed by using ADS Keysight. To match impedances between two lines optimally, a Klopfenstein taper [103] is used. Based on the Klopfenstein taper, the taper length should have an initial length of λ/4 to minimise mismatch at the desired frequency range. The taper length can be optimised (reduced or increased) to match the resonance point on the *S*-parameter plot. Table 5.2 shows the relationship between the impedance at the MTL, the width of the MTL, gap, and epsilon for the substrate as provided for IMN, IMS, and OMN.

Table 5.2: Geometric parameters of the proposed CPW structure with GND.

	Port	***Zo* (Ω)**	**Width (µm)**	**Gap (µm)**
IMN	1	56.14	56.02	53
	2	59.26	59.26	32
IMS	1	27.31	742.8	600
	2	25.95	815.1	1200
OMN	1	29.37	666	600
	2	36.10	446.3	410

Table 5.3 provides the dimensions for the substrate and the ground used in this work.

Table 5.3: Dimensions for the substrate and the ground.

	Length (µm)	**Width (µm)**	**Thickness (µm)**
Substrate	2000	2000	525
GND	2000	2000	10

A definite ground enables proper de-embedding up to mm-wave frequencies. The ground plane is defined using PEC. The tapered transition is synthesised with the anticipated impedance difference. The characteristic impedance and the attenuation of the feed line are determined by the dimensions of the centre strip (signal line) and the gap, as well as the dielectric substrate thickness and permittivity [103].

Table 5.4 provides the definition of the main parameters for the IMN, IMS and OMN model using CST MWS.

Table 5.4: Definition of the main parameters for the IMN, IMS and OMN model using CST MWS.

Passive	Width of MTL (µm)	Length of MTL (µm)
MTL1	56.01	262.4
MTL2	187.1	825
MTL3	13.12	27.8
MTL4	742.8	361
MTL5	240.9	970.8
MTL6	815.1	59.47
MTL7	83.4	13.4
MTL8	920	17.1

5.2 DESIGN OF INTERDIGITAL CAPACITOR VIA EM SIMULATION

A commercial off-the-shelf capacitor or a distributed capacitor using commercially available EM software can be used. The commercial off-the-shelf capacitors are cost-effective and have good reliability. A coupling capacitor of small value is required in the LNA design. Despite these advantages, a distributed capacitor using commercially available EM software was used for this LNA design, because of its simplicity in construction, relatively high-quality factor and consistent repeatability. Its application ranges from filters, transducers, and microwave-integrated circuits to tunable devices.

The requirement for the design of the IDT is a closed form expression of the capacitance based on the chosen capacitance value while considering the properties of the substrate. Partial capacitance and a conformal transformation method (Schwartz-Christoffel) are used in evaluating the closed form expression for the capacitance computations. The structure, which

is comb-like, has a capacitance that is dependent on the space and width of the closely coupled digits, the ratio of the thick sensitive layer, and electric field distribution of the interdigital gap, the size of the terminating port and the permittivity of the mediums.

In Figure 5.5, a diagram of an IDT along with a coplanar waveguide (CST MWS top view design and labelling of the CPW and IDT structure.) is shown. The finger of the IDT and the particular length and width of the finger are necessary for realising the desired capacitance. The gap between the IDT fingers and the area of the substrate exposed (not covered by aluminium metal) significantly reduce the losses of the IDT structure. The length, width and height of the CPW taper and the length of the signal line helps to determine the response and the value of the capacitance. The length, breadth, and width of the interdigital fingers also help in determining the total capacitance. The ports of the IDT are matched at 50 Ω with comb-like metal that holds the fingers in position (left and right side respectively), which plays a central role in defining the number of fingers that are used in each IDT.

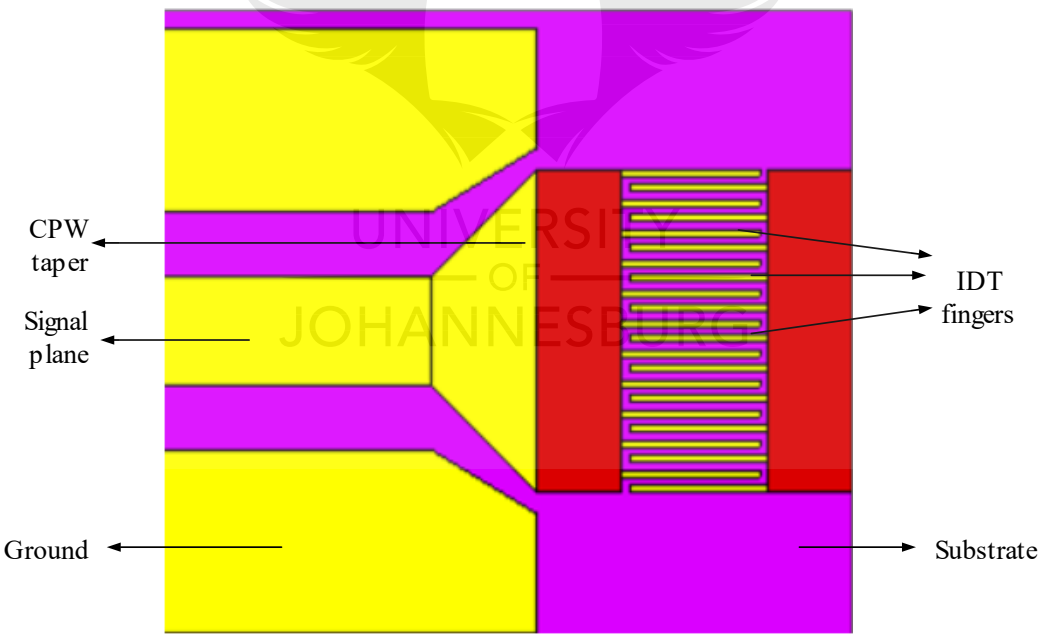

Figure 5.5: Diagram of a coplanar waveguide with an interdigitated capacitor.

In Figure 5.5, the substrate, ground (not labelled beneath the substrate), silicon oxide and the metallisation are used in the design of an IDT. The coplanar line and the microstrip line are joined using the tapering structure. The following parameters can be varied in design to enhance optimised performance:

The finger width and length; the substrate thickness; the gap width of each finger, the overlapping length of the fingers and the impedance of the centre conductor.

Once the IDT has been designed based on the closed form expressions, CST MWS is used for simulation and the *S*-parameters are obtained. These are imported to the ADS Keysight to allow them to be converted to their *Y*-parameters and the capacitance of the structure is then computed. Three capacitors are required in the LNA circuit and these have been designed and analysed based on the above requirements.

- The maximum length of the finger was restricted to 150 µm.
- The gap between subsequent fingers was between 8 and 20 µm.
- The silicon oxide was restricted to a thickness of 0.3 µm.
- The ground was made with a thickness of 0.4 µm
- The total height of the substrate was 525 µm.
- The thickness of the metallisation was 1 µm.

The Table 5.6 gives a complete summary of the IDT capacitors used at the IMN, IMS and OMN.

Table 5.6: Complete description of the IDT capacitor designed for each segment of the LNA.

		Capacitance (pF)	**Length of Finger (µm)**	**Number of Fingers (µm)**	**Width of Fingers (µm)**	**Gap (µm)**
1	IMN	0.07	135	20	7	6
2	IMS	0.7	145	35	6	8
3	OMN	0.15	120	40	5	6

In the CST design, the ground was made of gold with a height of 0.4 µm and the height of the substrate was set at 525 µm. Silicon oxide of 0.3 µm thickness was sandwiched between the metallisation surface and the substrate with *epsilon value* of 3.9 and loss tangent of 0.001. It acts as an insulator, diffusion mask and media for creating a protective layer on the wafer surface. Once the structure was completed, it was joined to the MTL structure designed for the IMN, IMS, and OMN. The result was optimised and then input into AWR MWO to observe the final performance of the LNA.

5.3 RESULT OF AWR MWO SIMULATIONS

Figure 5.6 depicts the simulation result of the mm-wave LNA circuit designed in AWR MWO. The simulation results for the gain and the NF were plotted on the left axis, with a range from -20 dB to 20 dB, while the results for the simulated input and output reflection coefficient, S_{11} and S_{22}, were plotted on the right axis, extending between -20 dB and 0 dB.

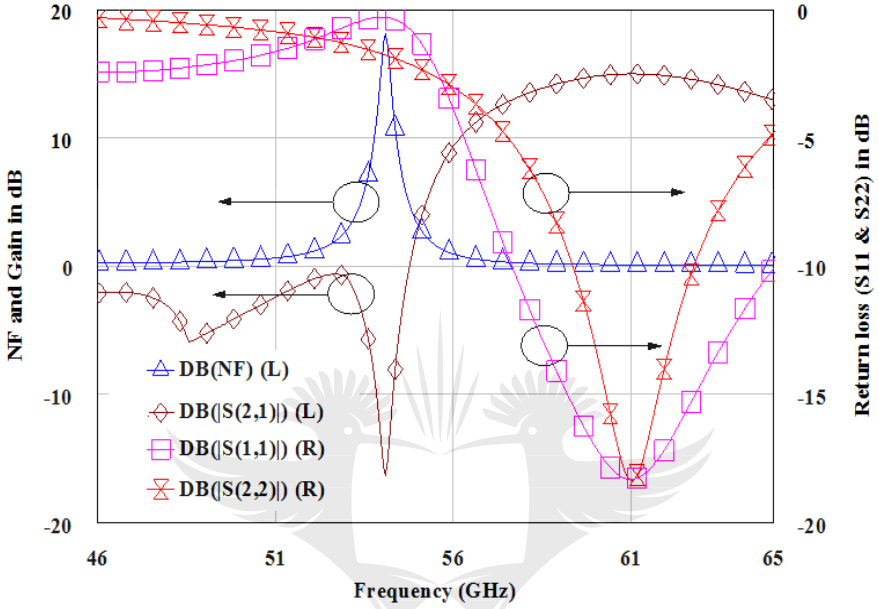

Figure 5.6: Simulated return loss (S_{11} and S_{22}), gain and NF vs. frequency based on AWR simulation of ideal components.

According to Figure 5.6, the results of the simulation showed a gain, S_{21} of 14.82 dB observed at 60 GHz, and a simulated input and output reflection coefficient, S_{11} and S_{22} respectively of less than -17.04 dB and -13.17 dB at 60 GHz respectively. The 3-dB bandwidth covered the entire frequency of interest between 56.93 and 66.18 GHz. The NF of the mm-wave LNA was very low because the *S*-parameter data did not contain the NF. Similarly, the ideal components used in the circuit contributed a minimal amount of noise to the overall NF of the circuit. After introducing the *S*-parameters of the modelled IMN from CST, the gain of the mm-wave LNA dropped by about 45 percent to about 7.57 dB at 64.97 GHz, while at 60 GHz, it had a gain of 7.23 dB. This is displayed in Figure 5.7.

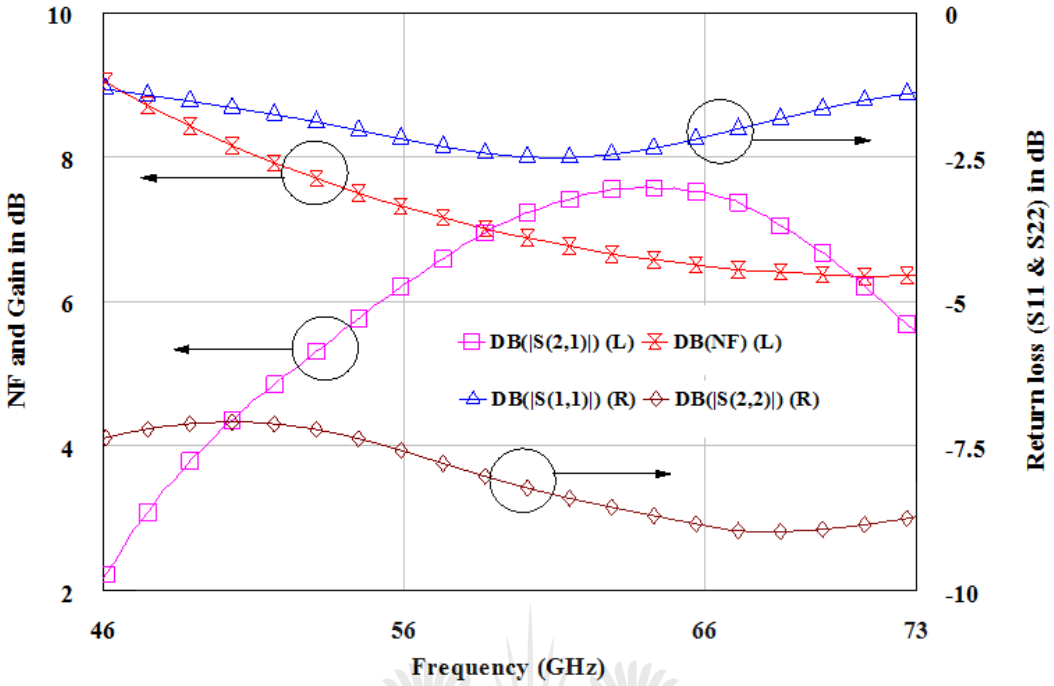

Figure 5.7: Simulated return loss, gain and NF vs. frequency based on AWR.

Additional information provided from Figure 5.7 is as follows: The simulated input reflection coefficient, S_{11}, resonated at 64.8 GHz with more than -6.57 dB, and the output reflection coefficient, S_{22}, resonated at -9.98 dB with a frequency of 67.36 GHz. The NF of the LNA dropped from 6.89 dB at 60.03 GHz to 6.65 dB at 64.8 GHz. The NF improved significantly as it approached the 70 GHz mark, to a value of 6.36 dB. The introduction of the GSG used in the MTL-to-CPW transition enhanced the unsatisfactory performance of the IMN, as it shifted the resonance frequency from 60 GHz to 58.6 GHz.

The shift also affected the S_{11} and S_{22} resonance frequency. The resistive loss affected the overall performance of the modelled IMN as well when re-introduced into AWR MWO. The thickness of the substrate can also contribute to the poor performance of the IMN. A substrate height of 525 µm introduces a large value of capacitance and conductance, a consequence of the dielectric polarisation effect.

5.4 RESULT OF CST MODELLING AND SIMULATIONS

The result presented in this section is for the simulated insertion loss and return loss of the IMN across 45 to 65 GHz (*S*-parameter results of the IMN). The full EM simulation carried out on the structures depicted in Figures 5.1 and 5.2 respectively is presented in Figures 5.8 and 5.9 respectively.

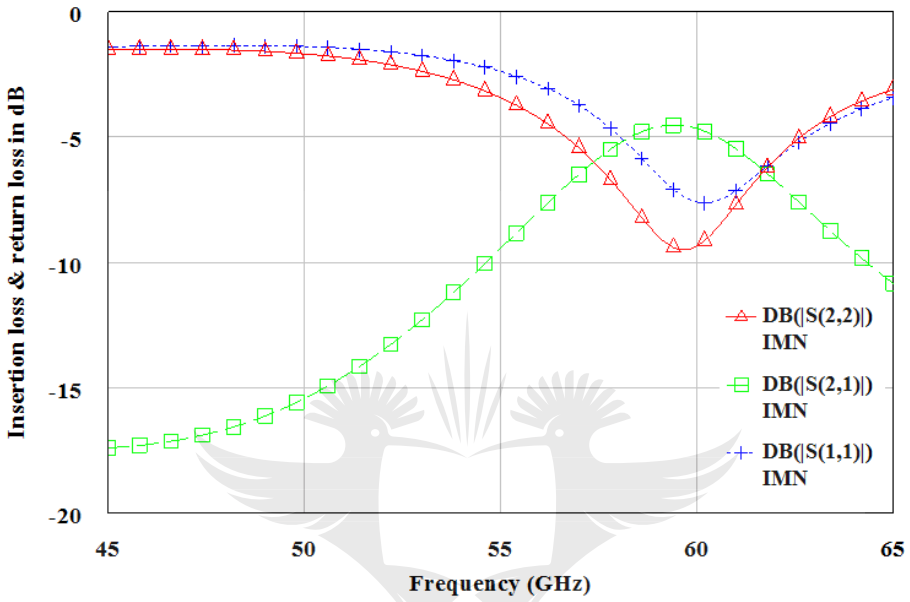

Figure 5.8: Simulated return loss and insertion loss vs. frequency based on the CST MWS modelling for IMN.

Figure 5.8 depicts the *S*-parameter for the IMN. The simulated input reflection coefficient, S_{11} parameter resonates at almost 60 GHz at less than -7.5 dB. For such a high frequency, an S_{21} parameter of -4.3 dB was fairly good and the value of the output reflection coefficient, S_{22}, was well-matched at less than 9.0 dB at the desired frequency range. The insertion loss was lower than 4.3 dB. Figure 5.9 displays the *S*-parameter for the IMS.

The simulated input reflection coefficient, S_{11}, resonated at almost 60 GHz at less than 18 dB. For such a high frequency, an S_{21} parameter of -20 dB was not good, as it had an overall effect on the gain of the mm-wave LNA and a simulated output reflection coefficient, S_{22}, of less than -6.0 dB at 63 GHz was recorded.

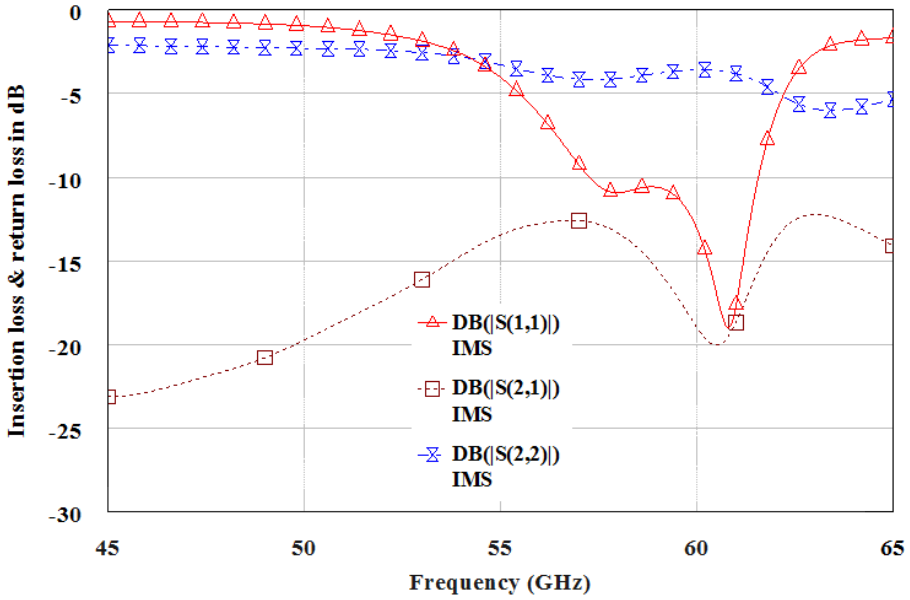

Figure 5.9: Simulated return loss and insertion loss vs. frequency based on the CST MWS modelling for the IMS.

The gain of the IMS contributed to an insertion loss of 20 dB. The high insertion loss can be attributed to the design topology and geometric feature relating to the structure. An additional reason for such a high insertion loss is the amount of power dissipated in the dielectric material. It is expected that for a good voltage gain at the IMS, the insertion loss must be around 2 dB. The distance between the taper and GND pad for both sides of the GSG feed differs. On the left side of the GSG, the gap is 600 µm, while the gap on the right side it is 1200 µm.

Figure 5.10 displays the *S*-parameter for the OMN. The simulated input reflection coefficient, S_{11}, resonates at almost 57.3 GHz at less than 22 dB.

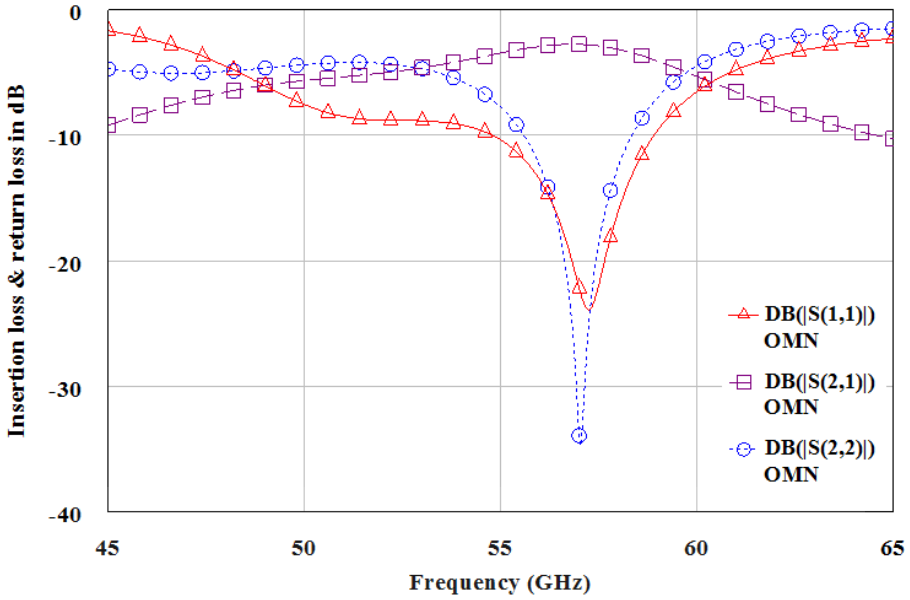

Figure 5.10: Simulated return loss and insertion loss vs. frequency based on the CST MWS modelling for the OMN.

According to Figure 5.10, at such a high frequency, an S_{21} parameter of -2.71 dB is very good, as it has a positive effect on the gain of the mm-wave LNA and the simulated output reflection coefficient, S_{22}, value is well-matched at below -30 dB between 52 GHz and 59 GHz. The gain of OMN contributed to an insertion loss of 2.71 dB.

5.5 MEASUREMENT RESULT OF THE COMPLETE CIRCUIT

VNA measures the inherent RF characteristics of IC circuitry. It is used in the sweeping of amplitudes (magnitude) and phase characteristics, thus providing a complete DUT characterisation. Its optimal performance is only realised through appropriate calibrations and de-embedding techniques. In calibration, the effects relating to cables and adapters used in the measurement process are eliminated. The approach is more mathematical, as error models exposed during calibration can best be described with sets of equations, which consist of known and unknown variables. In resolving the unknown variable, full characterisation of the network error yields additional equations owing to the various load conditions.

The network error correction via VNA calibration can be represented by any measurement parameters, such as the *Z*-parameter, *S*-parameter and the *ABCD*. SOLT, Thru-reflect-line

and thru-reflect-match are examples of the calibration approach that can be used. In this work, SOLT calibration was used with GGB Industries' CS5 calibration. This allows for the direct calibration of the probe tips on the chuck. Thus, all unavoidable errors and losses associated with cabling are eliminated. Once this is completed, measurement procedures as discussed earlier can be implemented. This measurement setup is illustrated in Figure 5.11.

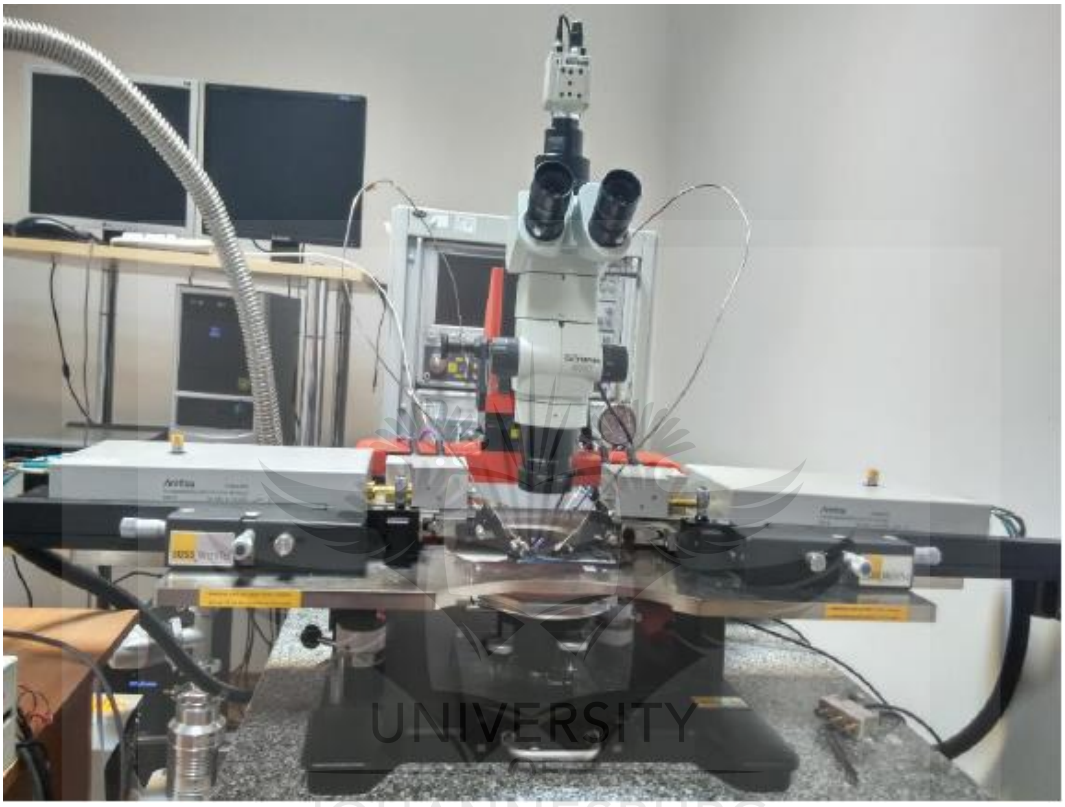

Figure 5.11: Measurement setup for measuring the *S*-parameters of the matching networks.

In Figure 5.11, the complete RF measurement and characterisation of the passive components were verified by using Anristsu 3739D VNA model connected to the SUSS Microtech PM5 probe station for high-frequency on-wafer measurements, built around the SOLT calibration. The Picoprobe 67A GSG probes of 150 µm were used. The probes release sinewaves swept in the frequency domain and the transfer functions are obtained. Two transmission reflection modules were made available between the frequency range of 65 GHz and 110 GHz. The block/side view representation of the millimeter-wave measurement setup is presented in Figure 5.12. From Figure 5.12, the side view of the measurement setup is displayed. The VNA plate is also the chunk where the DUT is placed. The structure from the ground plane to the metallisation is the complete description of the DUT.

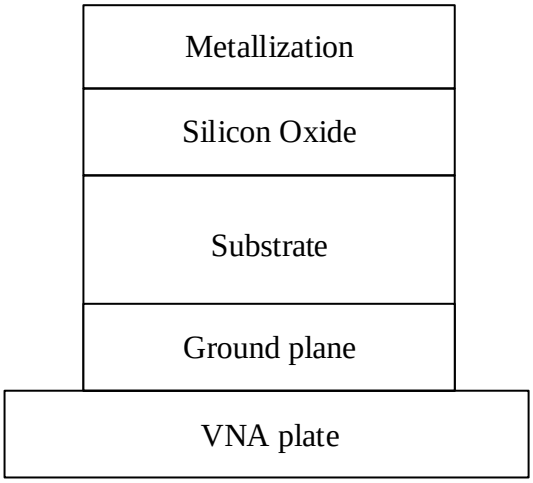

Figure 5.12: Block/side-view of the millimeter wave DUT that was measured.

The calibration exercise was a full two-port calibration. Upon completing the calibration on the VNA, the short was very close to infinity, while the open was very close to zero. The SOLT calibration is defined by *S*-parameter files consisting of transmission line length and corresponding passive elements. The *SHORT, OPEN, LOAD and THRU* is defined based on a frequency dependent inductance, frequency-dependent capacitance, shunt capacitance, a resistance and series inductance, and the frequency-independent losses respectively.

De-embedding, a post-process activity, can be used in removing measurement parasitics that cannot be accounted for during the calibration processes. In fact, a double approach, based on the calibration and de-embedding process, enhances error correction. Calibration allows the shift of the reference point to a location close to the DUT, removing the parasitic effects induced from cables, probes, and internal parasitic to the VNA. De-embedding is the complete abstraction of the electrical performance associated with the test fixture, thus completing the shift of the reference plane.

The fabricated structure of the OMN, IMS, and IMN (consisting of the IDT capacitor, microstrip lines and coplanar waveguide as discussed in this chapter) are depicted in Figure 5.13, Figure 5.14 and Figure 5.15 respectively. In the figures mentioned, an optical and magnified top-view picture of the fabricated DUT is shown. Port 1 is on the right side of the Figures while port 2 is on the left side of the Figure. The probes are denoted by the black tips contacting the port of the structure. The dimensions of the IDT capacitor for the IMN, IMS and OMN are 470 by 418 μm^2, 500 by 534 μm^2 and 290 by 700 μm^2 respectively.

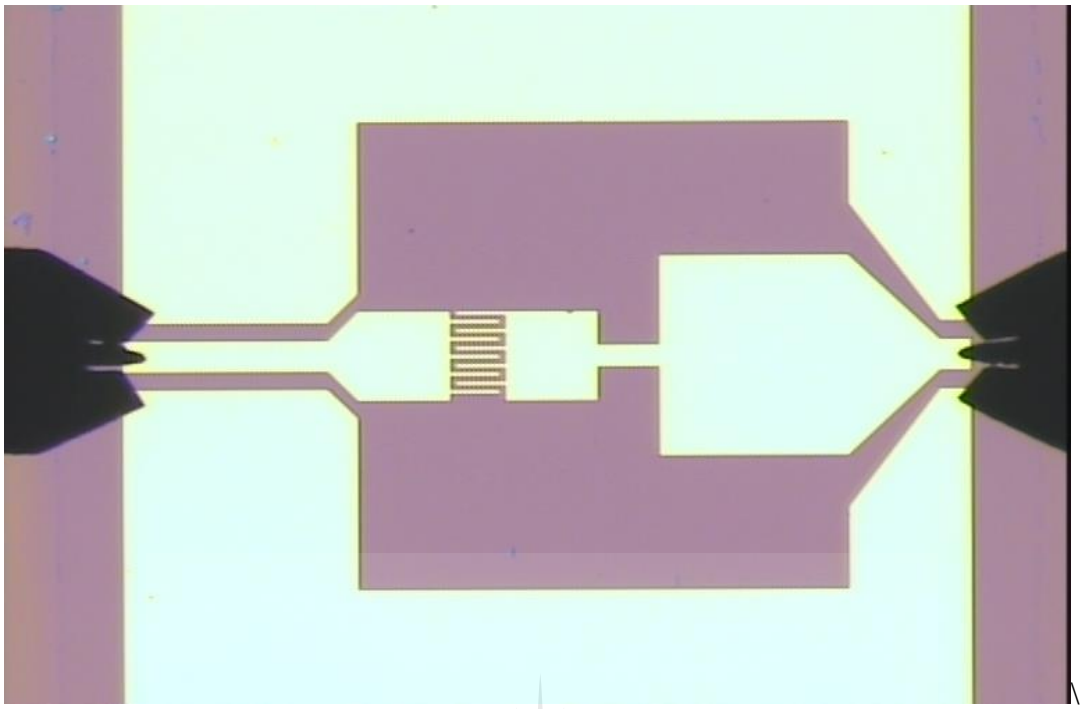

Figure 5.13: Measurement of the OMN with probe positioned on the GSG terminal with a dimension of 2000 µm by 2497 µm.

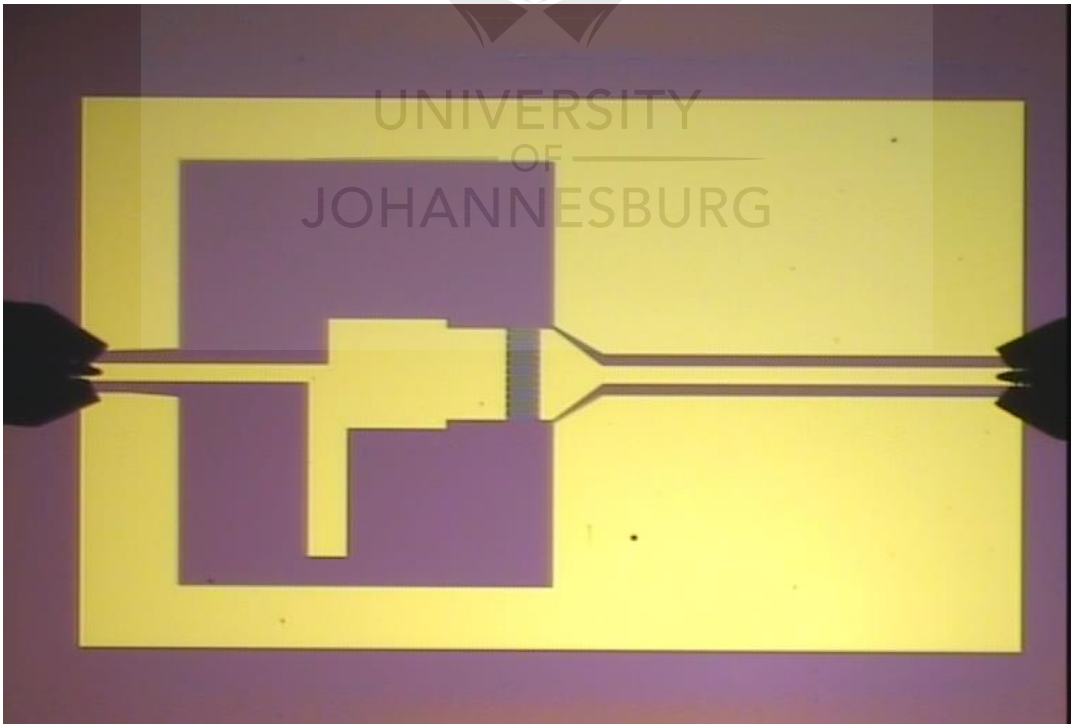

Figure 5.14: Measurement of the IMS with probe positioned on the GSG terminal with a dimension of 2,880 µm by 4,734 µm.

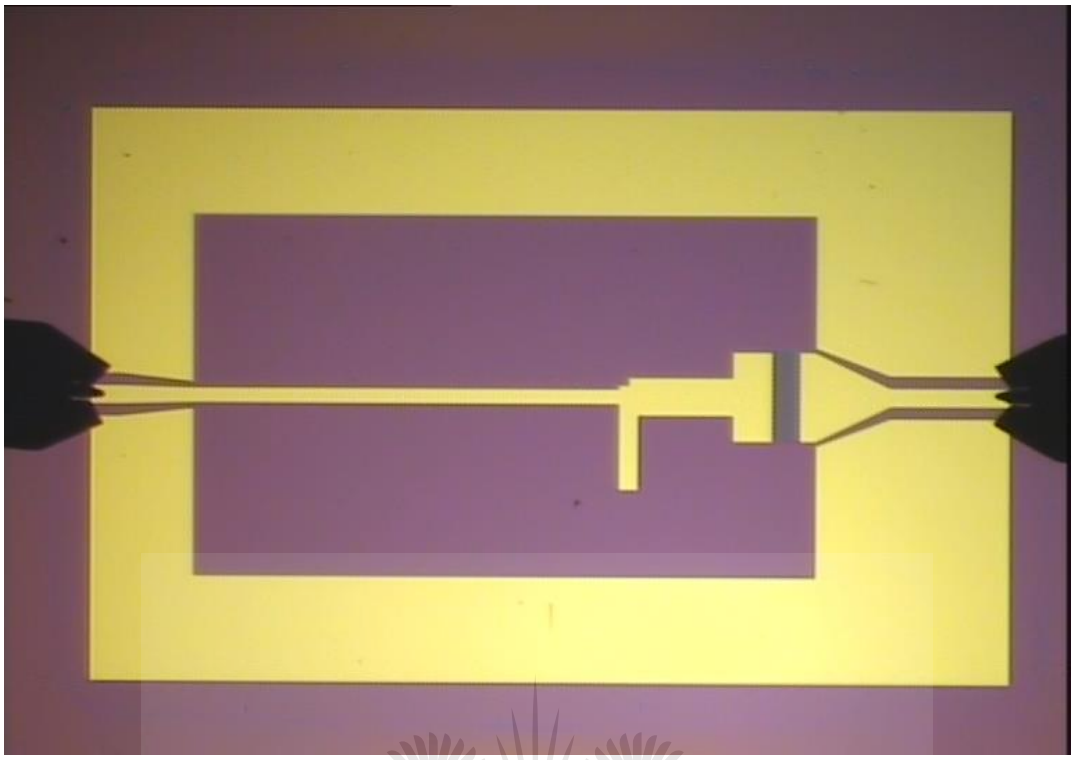

Figure 5.15: Measurement of the IMN with probe positioned on the GSG terminal with a dimension of 2,000 µm by 4,643 µm.

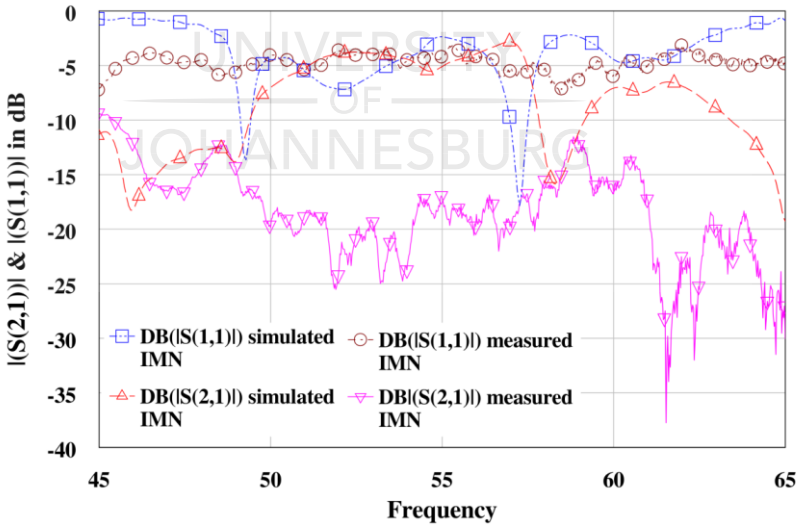

Figure 5.16: Comparison of the simulation and measurement results (S_{11} and S_{21}) of IMN.

With the design, prototyping and measuring of the structure completed, the *S*-parameters of the IMN, IMS and OMN are transferred into AWR MWO. The measured *S*-parameters are

compared to the simulated *S*-parameters in CST MWS. The result is then plotted in Figure 5.16 and the discussion is as follows: In order to assess the performance of the IMN, OMN and IMS, Figure 5.16 focuses on the measured and simulated *S*-parameters (S_{11}, S_{21}) of the IMN for comparison purposes, while Figure 5.17 also provides an explanation of the performance of the S_{22}.

From Figure 5.16, the best performance of the transmission during the simulation was realised at 56.93 GHz with -2.82 dB, while the corresponding return loss around the same frequency was observed at 57.26 GHz with a value of -17.26 dB. This is however not the case when one observes the measured S_{11} and S_{21}. The performance of the return loss was at the best value of -7.45 dB at 58.43 GHz, while at 58.82 GHz transmission of -11.71 dB was measured. In both situations, the performance of the *S*-parameters was distinctly poor. Beyond the 60 GHz mark, the performance was even poorer. An in-depth study of the result is required to examine the factors responsible for these large discrepancies closely. This discrepancy can be attributed to the following:

- Permittivity tolerance of each material used in the prototyping process.
- A closer look at Figure 5.15 gives a picture of the problems associated with the design. The gap between the taper plane and the ground plane was too small. With a smaller gap, the resistance at port 1 of the IDT, is reduced to below 50 **Ω**, resulting in the notably poor result seen in the measured S_{21}.
- The long strip of the microstrip line introduces losses since the long MTL is too narrow and long as it extends to port 2. Consequently, a large loss is seen in S_{12} and S_{21}.
- The fringing field effect evident in the IDT and the proximity effect of metallisation also contributed to the losses in the IMN.

Figure 5.17 shows the difference in the measured and the simulated S_{22} values. Two resonance points were observed in the simulation. The first resonance point was at 57 GHz with an S_{22} value of -17 dB, while the second was observed at 49 GHz with -14 dB. The best performance was seen at 53.5 GHz with a loss of -14 dB for the measured insertion loss. This is however outside the frequency of interest. This observed measured value is better than the simulated transmission at the same frequency. The factor held responsible above for the poor performance of the S_{11}, S_{21} and S_{22} is responsible for the overall poor performance of the

IMN. However, another look at the 57 GHz frequency point shows that the simulated result is better than the measurement result, as the insertion losses are -17 dB and -9 dB, respectively

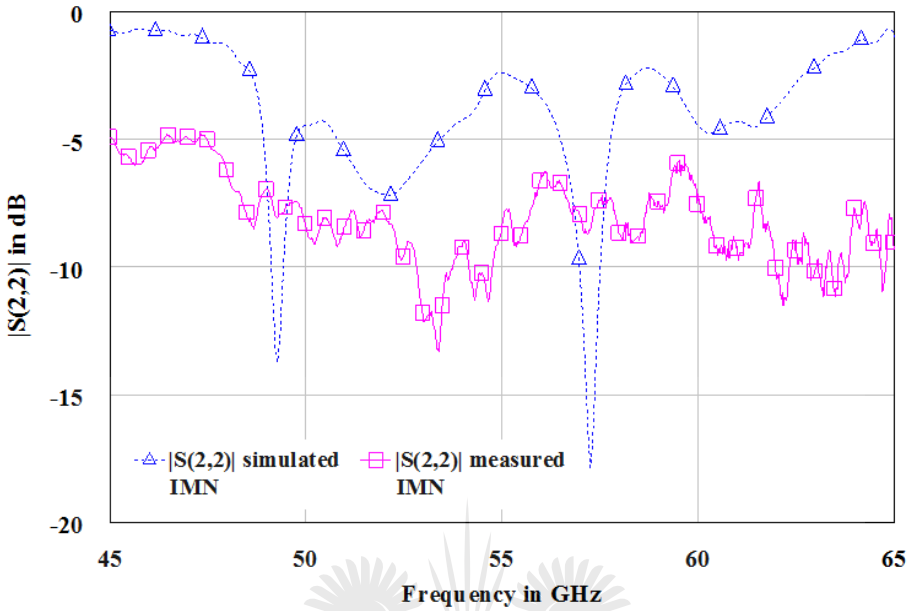

Figure 5.17: Comparison of the simulation and measurement results (S_{22}) of IMN.

In Figure 5.18 and Figure 5.19, the *S*-parameters of the IMS are shown. From the simulation results, it was observed that the best performance of the S_{21} and S_{11} was seen at 56.89 GHz, with an insertion loss of -2.386 dB and a return loss of -14.9 dB at 56.85 GHz respectively. However, a different result was observed when the measurement was taken. The performance of the S_{21} had deteriorated significantly, such that the best result was measured at 55.99 GHz with a forward transmission of -7.62 dB. This also had a significant effect on the return loss, as it became worse at a value of -6.47 dB.

This discrepancy can be seen from the width and the length of one of the MTL used in the design. Significantly long length introduces a large amount of losses to the structure. This could also have been compensated for by widening the width of the same MTL to negate the effect of the narrow MTL. The length of the signal line attached to the transition network is another determining factor in defining the overall performance of the IMS structure. Reducing this length would yield better S_{21} and $S_{11,}$ as seen in the simulation.

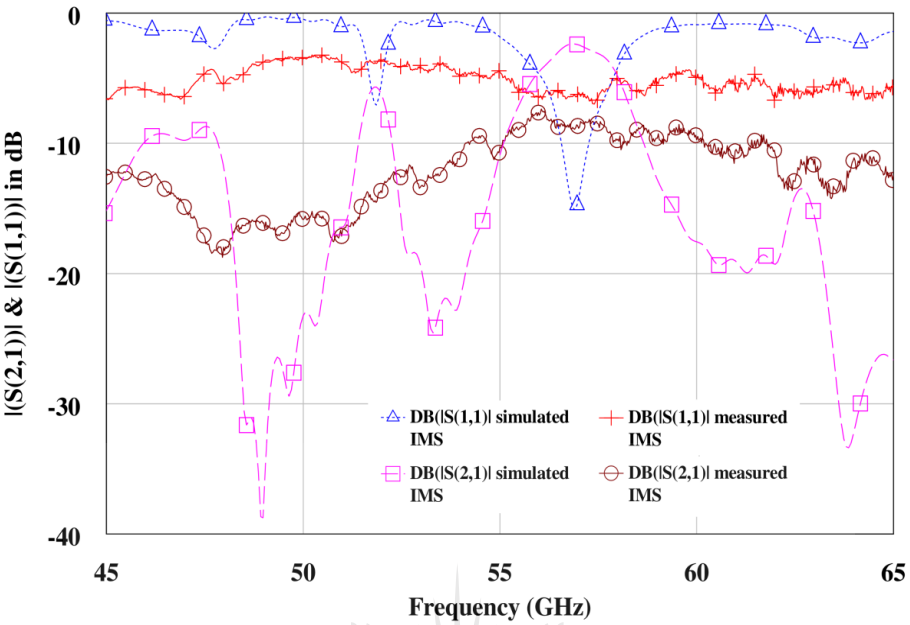

Figure 5.18: Comparison of the simulation and measurement results (S_{11} and S_{21}) of IMS.

There is some level of similarity between the simulated S_{22} and the measured $S_{22,}$ as seen in Figure 5.19. The best performance of the measured S_{22} can be observed between 56 GHz and 62 GHz, averaging between -18 dB and -20 dB. In the simulation, at least two dominant points of S_{22} can be seen, the first at 52 GHz and the second at 57 GHz. The best performance is at a frequency of 57 GHz, with an output reflection coefficient of -15 dB. However, at the same frequency, the measured reflection coefficient is -20 dB. Despite the good performance of S_{22}, the S_{11} and S_{21} performance significantly defines the overall performance of the IMS. The increase in the length of the central pad (signal line) beyond 100 by 100 μm^2 results in an increase in the capacitance of the structure. Thus, the overall capacitance increases, leading to a mismatch between the passive structures.

Figure 5.20 gives a description of the performance of the measured and simulated OMN to be used in the LNA. The S_{21} and S_{11} parameters were considered first before the S_{22} was discussed. The best performance of S_{21} during the simulation using CST MWS was observed at 55 GHz, with an insertion loss of -2.8 dB, while the equivalent performance of S_{11} observed at 56 GHz showed a value of -19.52 dB. The simulated value was good, but with

the measured passive structure of the OMN, discrepancies were observed. The first observation was that the best performance of the OMN was realised at a frequency far from that seen in the simulated result. Values of -6.98 dB and -18.1 dB were realised at 51.54 GHz for the insertion and the return loss respectively.

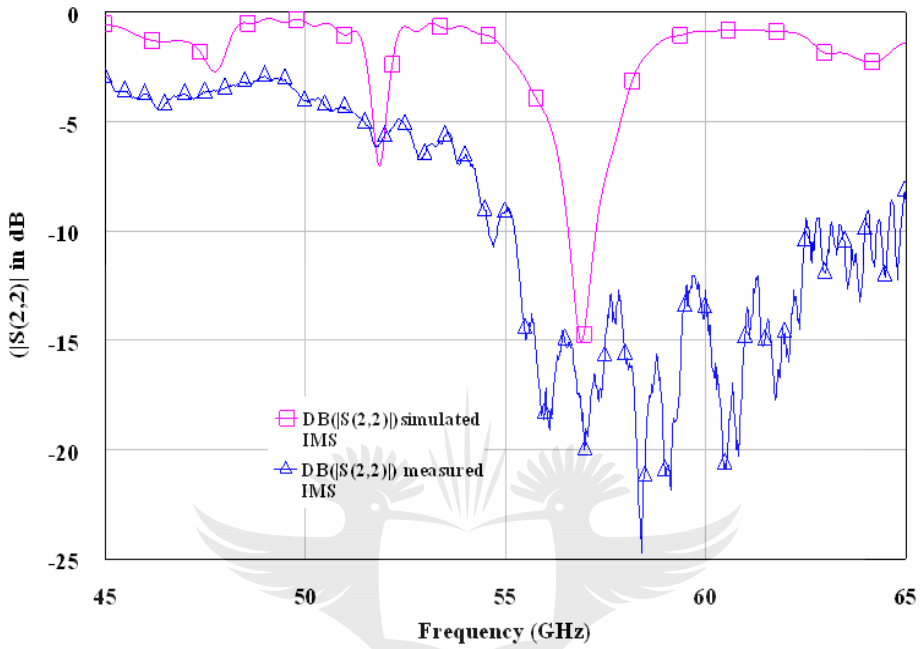

Figure 5.19: Comparison of the simulation and measurement results (S_{22}) of IMS.

Likewise, good measurement performance was observed at 47.23 GHz with an S_{11} value of -15.35 dB and a S_{21} value of -4.34 dB. At the desired frequency (50 – 60 GHz), S_{21} was extremely poor and large losses were seen regarding S_{11}. The second observation was that the S_{11} and S_{21} measured at 55 to 57 GHz were extremely poor. Beyond 57 GHz, S_{11} kept increasing significantly, while S_{21} was decreasing continuously. This can be attributed to the following issues:

- The length of the feeding line (signal line) was seen to be short, hence the significant shift in the resonance point as described in the earlier paragraph. A slight increase in length would result in the shift of the S_{21} and S_{11} of the OMN.
- The width of the microstrip line was observed to be too great. A moderate reduction in the width would create a shift to the desired frequency, while ensuring a good S_{21} and S_{11} of the OMN.

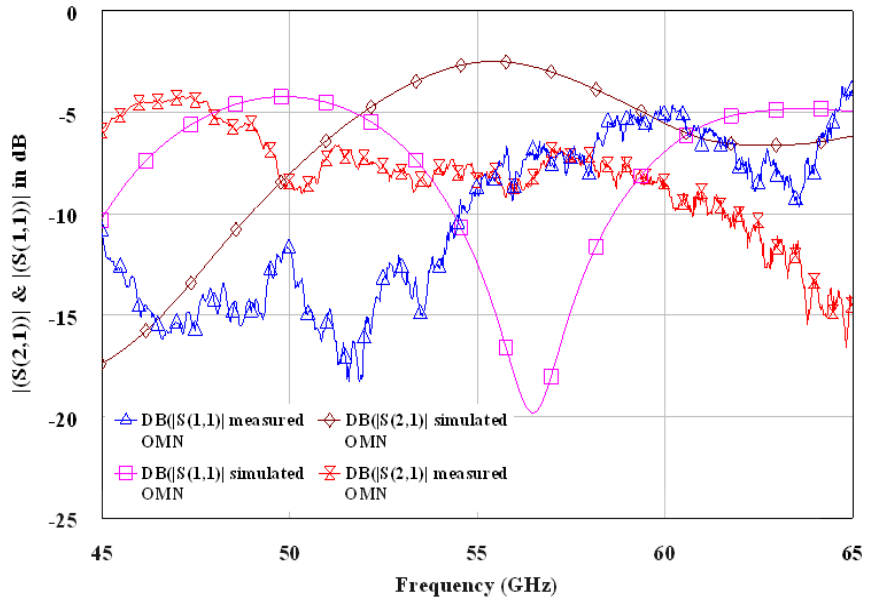

Figure 5.20: Comparison of the simulation and measurement results (S_{11} and S_{21}) of OMN.

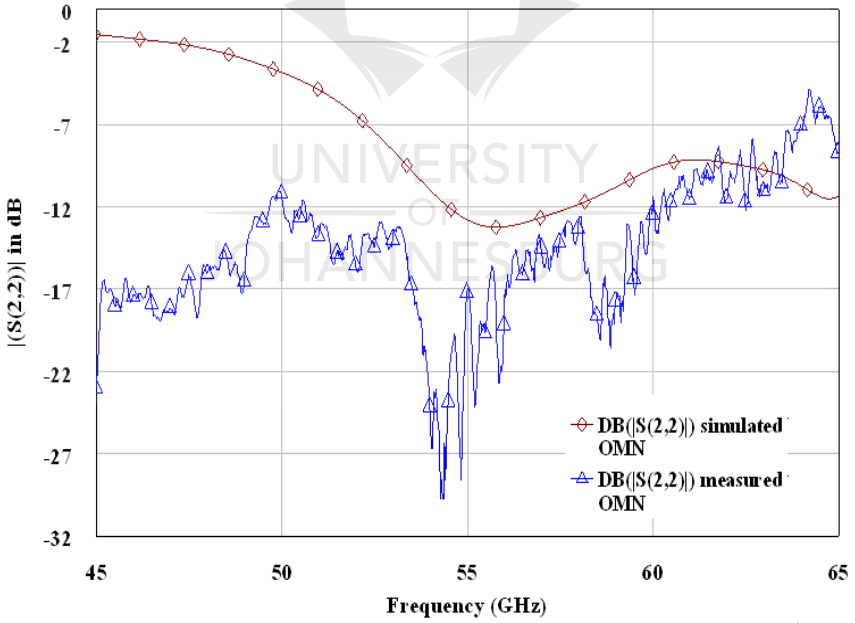

Figure 5.21: Comparison of the simulation and measurement results (S_{22}) of OMN.

Figure 5.21 depicted the output reflection coefficient of the OMN. The simulated value resonates at 55.8 GHz with a S_{22} value of -13.24 dB, while the measurement result shows a

shift in the output reflection coefficient with a value of -29.48 dB at a frequency of 54.32 GHz.

5.6 INTEGRATION OF THE MEASURED PASSIVE COMPONENT WITH ACTIVE DEVICE

The measured components of the LNA at 60 GHz were integrated with the IMN, IMS and OMN. The integration did not yield the desired result. The addition of the measured OMN, IMN and IMS *S*-parameters yielded a very high NF and very poor gain. However, after subsequent simulation of *S*-parameters and verification of the measured passive structure, the OMN was selected to be integrated into the 60 GHz LNA. This yielded a low NF at the desired frequency band. Figure 5.21 provides a complete plot of the S_{21}, S_{22}, S_{11} and the NF on the left and the right axis against the frequency.

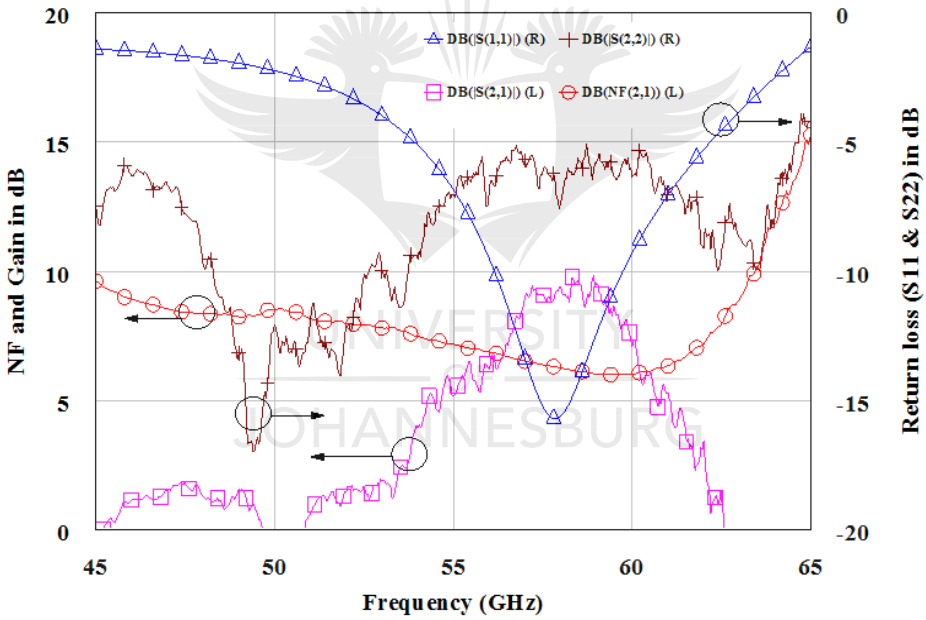

Figure 5.22: Integration of the *S*-parameters of the OMN into the schematic of the LNA layout with active devices.

In Figure 5.22, S_{11} can be observed at 57.84 GHz with a loss value of -15.71 dB, while the maximum value of the gain, S_{21}, is seen at 57.88 GHz with a value of 9.22 dB. The NF value at 58 GHz value was approximately 6.22 dB. However, the best performance occurred at 59.8 GHz, with a value of 5.99 dB. As for the S_{22}, the peak performance at the desired frequency range can be seen at 57.96 GHz with -7.58 dB while at 49.48 GHz, -16.62 dB was realised.

5.7 CONCLUSION

In this chapter, the design of the CPW with MTL and IDT capacitor using CST MWS was described. Thereafter, the advantages of using the MTL-to-CPW platform for measurements were highlighted. A combination of the IDT and CPW-to-MTL was finalised in CST MWS via simulations. Figures and tables that show the parameters and the representation of the modelling of the passive structures used in the mm-wave LNA were depicted. Results from the CST MWS simulation of the IMN, IMS, and OMN were presented.

The simulation results of the mm-wave LNA ideal component were displayed, as well as the result of the mm-wave LNA when the *S*-parameters of the IMN were introduced into AWR MWO. With this completed, the prototype of the IDT and CPW-to-MTL was fabricated at IMT and its characterisation was undertaken. The *S*-parameter of the OMN was then integrated into the AWR MWO EDA simulator along with the active device to observe the performance of the 60 GHz mm-wave LNA.

CHAPTER 6: CONCLUSION

6. CHAPTER OVERVIEW

The summary of this thesis work is presented in this chapter and an evaluative assessment of the research hypothesis is discussed, not excluding the scope, delimitation and postulations made to achieve successful implementation.

6.1 INTRODUCTION

The credibility of the research hypothesis proffered in the first chapter was checked by comparing the simulated and measured results based on the proposed technique. In the first chapter, a circuit consisting of the CC and the T-MTL topology was proposed for the design of the mm-wave LNA. With this circuit, the possibility of achieving a low NF, high gain and a wide bandwidth was put forward, using the configuration mentioned. In addition, the reasoning behind this research and a research procedure that was followed were described.

In the next chapter, the hypothesis was established further through literature reviews on aspects that best describe the area of study. This area includes circuit topology, configuration and architecture, process technology, issues with the mm-wave LNA, IMN and its performance comparison. An extensive discussion of the modelling and design of the mm-wave LNA using CC topology and MTL was also conducted. In chapter 3, the device specifications of each component provided by GF for mm-wave LNA design were provided. Most of the values and dimensions used in the construction of the component could not be published owing to an NDA. Thereafter, a research methodology was developed for the purpose of this research work, to deal systematically with the research hypothesis. Technical software to be used in this study was identified. Thereafter, the circuit layout and verification were implemented in CST MWS. PCB prototyping and measurement were completed.

Thereafter, in chapter 4, a small-signal-equivalent circuit, which represents the *RLGC* relationship of the IMN, was mathematically analysed and verified with expression for the input impedance, gain and NF based on the first stage input matching. In addition to this, with the complete methodology laid out, an approach used to estimate the S_{11} value of 60 GHz LNA was discussed exhaustively, with a flow chart showing each process. A small-signal equivalent circuit, which represented the RLC relationship of the IMN, was

mathematically analysed and verified to compute the $S_{11.}$ Chapter 5 was compiled with the purpose of showing the 3D-EM modelling of the T-topologies across the IMN, IMS and OMN. An IDT was designed and simulated as a decoupling capacitor. This was optimised and combined with the CPW-to-MTL structure designed for the IMN, IMS, and OMN. The process of accomplishing this was shown diagrammatically and discussed with the geometric parameters used, all presented in tabular format. The *S*-parameter of each structure (IMN, OMN, IMS) was used in AWR MWO to plot the performance of the mm-wave LNA. Thereafter, a comparison of the simulated and the measured prototype was presented, identifying and investigating any uncorrelated results.

6.2 CRITICAL EVALUATION OF HYPOTHESIS

Important materials collected from the body of literature made known through this thesis, including the merits and demerits of configuration, practical implementation from the simulation environment and the tuning of component values to the EM modelling of the circuit, as well as observations from this study, are presented in this section.

Incessant growth in the demand for broadband spectrum, coupled with the throughput required by many applications, has made research into the mm-wave frequency band imperative in the last decade. The availability of larger bandwidth also represents a higher data transfer rate, which is very useful for online gaming application as well as high-definition streaming of programs. Irrespective of the above benefits, channels used in the WLAN are typically known for their noise characteristics and interference, which have an undesirable effect on the voltage gain of the wireless transceiver. A significant block in the wireless transceiver is the mm-wave LNA, which has the means to reduce NF and yield high gain. Not only are the NF and gain required by satellite receiver/super heterodyne radio met; a wide bandwidth is available for the network of devices that is at present being taken advantage of on IoT platforms. A low-power wide area network would be required for IoT technologies. A low-power wide area network is designed to complement existing telecommunications networks and link specifically with inhibited IoT devices. The required wide bandwidth and high gain are commonly available at mm-wave frequencies and mm-wave LNA can be used along with existing technology to ensure security and frequency reuse.

Low power consumption, low range and wide bandwidth are additional characteristics that must define the applications and services that meet the need of IoT. A comprehensive and relevant review of literature on mm-wave LNAs was carried out and reported in Chapters 1 and 2. The tables (Table 1.1 and 1.2) focused on the approach, topology, configuration, area, *S*-parameters, NF, and bandwidth of each design. This was compared with similar parameters of simulated and prototyped mm-wave LNA in ADS Keysight, AWR MWO and EM-modelled simulation modelled in CST MWS, as demonstrated in Chapter 5. The summary from the publications reviewed provided an idea that supported the argument, which was verified by observation, i.e. prototyping of the IMN, IMS and OMN and measurement of certain variables of interest, such as *S*-parameters. The result from the measurements was used as the platform for evaluation with the results from articles.

The specific questions to be addressed from this work were listed, with each stating its expected relationship with each parameter variable that needed to be improved. It was evident that the hypothesis was testable. Once this fact had been established, the design of the mm-wave LNA circuit was carried out, using the CC configuration with the T-MTL topology to ascertain that the expectation set by the hypothesis could be achieved at 60 GHz using the 130 nm process. With further optimisation, the set target of parameter variables was met using the EDA software. The first approach involved the use of ideal components in which there was a limit to component values and sizes. Thereafter, once good correlation had been established with the EM model results, particularly the *S*-parameters, a conclusion could be presented.

The methodology (design and procedure) used in this study was described expansively, with the goals of each step outlined, as well as the appropriate software used. Moreover, the rationale for the selection of each EDA, as well as instruments for measurement, was stated clearly, as each instrument met the purpose for which it had been selected. The procedure described in the methodology can be replicated based on the details provided in this work. Parameters such as the thickness of the substrate, capacitance across the base and emitter and capacitance between the base and collector were identified as contributing factors in the mathematical analysis of the IMN.

The hypothesis listed and the enumerated research questions in Chapter 1 were tested and all the results were clearly presented, with graphs, tables and figures to answer the research questions. Each result was discussed in the light of the original hypothesis presented. Results such as the bandwidth, NF and gain were all discussed. These results were consistent with generalisations in literature. Among the many implications of the theoretical and practical results is that in the mm-wave frequency band, degenerative MTL would degrade the gain of the LNA. Similarly, the realisation of a wide bandwidth for the mm-wave LNA implies that the higher data transfer rate required in today's world for application, such as IoT and IoE, is attainable.

6.3 SCOPE AND ASSUMPTIONS

The scope and the assumptions made in this work are as follows:

- The 3D EM modelling of the T-topology structure that constitutes the different stages of the mm-wave LNA was modelled to understand the expected frequency response of the passive (MTL) used in the circuit. The simulation was completed in CST MWS and was prototyped practically. Measurements were taken with the VNA.

- The mathematical model used in predicting the behaviour of the IMN was analysed for gain, NF, and S_{11}. However, the mathematical model was not extended to the 3-dB bandwidth of the IMN. This would have given the estimate of the 3-dB bandwidth frequency, which was finally seen in the AWR MWO and the CST EM simulation results. This can be added to the work to improve its quality.

- The IC layout for the 60 GHz layout was simulated but not realised on the final IC layout because of time constraints and administrative issues concerning the application to MOSIS. However, the prototyping of the IC layout has been scheduled for 2020, which is after the expected submission date of this thesis document.

- Post-layout simulation was not performed to confirm the performance of the proposed IC because of a software license limitation in the ADS EM. Analysis on the parasitic effect (capacitance) could not be carried out, but it was accounted for in all measurements carried out in the work. The post-layout simulation would offer clear

insight into the performance of the mm-wave LNA and the need for optimising and changing some design elements.

6.4 FUTURE WORK AND POSSIBLE IMPROVEMENTS

- EM modelling of the MTL used in the circuit was attempted in CST MWS in collaboration with IMT, Bucharest. Future optimisation of the passive structure can be used to improve the prototyped MTL. Initial measurement results can be used to enhance the modelling of the MTL as an EM component.

- Prototyping of the T-topology showing the IMN, IMS and OMN added to this study along with an off-the-shelf active device would add a significant level of confidence to the results achieved in the scope of this research.

- Post-layout simulation was not carried out owing to a software license limitation. Therefore, EM simulation could be applied further to improve the confidence level associated with the expected and measured results.

- The current strategy of adding a GSG to the MTL tends to push the resonance frequency of the T-topology further away from the desired resonance frequency. Therefore, it would be necessary to find an optimal approach, ensuring that the resonant frequency does not differ from the desired frequency. This is dependent on the physical length of the MTL.

- A substrate of a thickness of 525 µm was used in the CST MWS design and the prototype. The use of other substrate thicknesses can be observed to study the effect of the thickness on the overall performance of the substrate.

- The bandwidth of the 60 GHz LNA was not discussed in detail owing to the limited time available for the analysis of results during the exchange programme in Romania. The prototype of the IMN and IMS and their related *S*-parameters (S_{11} and S_{21}) would require further analysis and optimisation so that the much-desired measurement goal and result can be realised.

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