Design of a Grid-Forming, Multi-Loop Control Scheme for Parallel Connected, Three-Phase Quasi-Z-Source Inverters

by

Adam John Emes

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This thesis was presented

by

Adam John Emes

It was defended on

June 9, 2020

and approved by

Dr. Brandon Grainger, PhD., Assistant Professor, Department of Electrical and Computer Engineering

Dr. Alexis Kwasinski, PhD., Associate Professor, Department of Electrical and Computer Engineering

Dr. Robert Kerestes, PhD., Assistant Professor, Department of Electrical and Computer Engineering

Thesis Advisor: Dr. Brandon Grainger, PhD., Assistant Professor, Department of Electrical and Computer Engineering

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The quasi-Z-source inverter has been the subject of numerous power electronics publications since its invention in the early 2000s. While often applied as an interface for renewable energies such as wind and PV, there is a lack of literature where the qZSI functions in a grid-forming role. The goal of this work is to design and implement a control scheme for a 3-phase qZSI in order to enable it to operate in a grid-forming role. The qZSI is analyzed in great detail and compared to a conventional voltage source inverter scheme that is commonly used in renewable energy interfaces. Literature is presented to demonstrate the need for current programed mode (CPM) control for the dc side of the qZSI, and the control scheme is compared to a common control scheme used for boost converters. Then, recent literature is presented to support why the universal droop control (UDC) scheme was chosen for the ac-side control for this work. After contextualizing the design of the overall qZSI control scheme, the final control scheme is presented, which utilizes CPM indirect control on the dc-side, and UDC on the ac side. The stability and dynamic response of the system is analyzed in detail for the chosen gains and component values.

Through PLECS simulations, the qZSI system presented in this work demonstrated its ability to operate in a grid-forming role and potentially superior performance when compared to conventional VSI systems. While a much more optimized design approach is needed for both the qZSI and VSI to truly compare the two systems, this work demonstrates that the qZSI is more than

capable of operating in a grid-forming role. It handles large step changes in load and input voltage with quick rise times and good damping, and exhibits quick and stable responses when operating in parallel with other inverters. This work concludes with some considerations for future work on this topic.

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Preface

First and foremost, I would like to thank my parents and sister for their support in my academic endeavors. Without them, I never would have pushed myself this far and achieved so much. They set a perfect example and showed me that I can do anything I put my mind to. Thank you to my girlfriend, Eva, for her emotional support throughout the process and always having my back when things got tough.

I would also like to thank all of the professors that helped me throughout my journey, specifically Dr. Brandon Grainger, Dr. Robert Kerestes, and Dr. Alexis Kwasinski. Without their passion for the power industry, I never would have had this incredible opportunity or met so many incredible people. Thank you to everyone in the lab, who were always up for technical discussions and offering help whenever I needed it, and for being excellent friends outside of work.

1.0 Introduction

The goal of this section is to provide context to the work presented in this thesis. The first subsection introduces the quasi-impedance-source inverter (also known as quasi-Z-source inverter or qZSI). The second subsection discusses the need for grid-forming inverters, and why that is an important topic in relation to the qZSI. The introduction concludes by explaining the organization of the rest of the thesis and the content that will be presented.

1.1 Quasi-Z-Source Inverter

First invented in 2003, the Z-source inverter (ZSI) was a novel inverter topology that gained attention for its inherent advantages over traditional inverters [1]. First, the control and types of switches used no longer need to change based on if the inverter is supplied by a voltage or current source. Second, and most importantly, the inverter now has the ability to buck or boost its equivalent dc-link voltage regardless of the input voltage [1]. This makes the ZSI very useful in renewable energy applications because it removes the need for a dc-dc converter to regulate the dc-link voltage [2]. In order to boost the dc-link voltage, the z-source allows a new switching state to be used – a shoot-through state where one or multiple phase legs are shorted [1], [3]. The shoot-through state can be spread symmetrically throughout a standard PWM control, meaning there is minimal modification needed to the switching control of the inverter in order to boost the dc-link voltage [1], [4], [5]. Additionally, because it is no longer detrimental to the system to short any of the phase legs, there is no longer a need for any dead time in the control scheme [6].

There are more than six variations of the z-source network that appear in the literature, each with slight differences in component ratings or control schemes, but ultimately with the same advantages and functionality as the original ZSI [7]. One variation, known as the quasi-z-source (qZSI), is particularly popular due to its nearly identical functionality and control when compared to the original z-source topology, but with the added benefits of continuous input current and less voltage stress on one of the capacitors, reducing component requirements [6]. These benefits are particularly useful in renewable energy applications, thus there is renewed attention on the qZSI for use in wind and photovoltaic (PV) systems [6], [7]. For the application presented in this work, the qZSI has the aforementioned advantages over the ZSI. Thus, this work only focuses on the qZSI topology.

1.2 Motivation

As expected, there are a large number of works on the qZSI regarding control. In recent literature, the focus is not on grid-forming performance, however. There is a lot of work on maximum power point tracking (MPPT) [8], [9], improved voltage regulation [10], [11], increased boost capabilities [12], and improved efficiency [13]. However, there is minimal or zero focus on the ability of the qZSI to function in a grid-forming role. While some works implement a type of droop control on the qZSI, they are still essentially focused on MPPT or voltage regulation [8], [14]. Neither of the mentioned works look at a situation where the qZSI is the primary grid-forming device, or how the qZSI will operate when connected in parallel with other qZSIs. For a device that is expected to continue its gains in popularity, understanding the performance of the qZSI as a grid-forming device is essential – this topic is the focus of this work.

A grid-forming inverter is responsible for providing tight voltage and frequency regulation depending on the real and reactive power being consumed, and capable of operating in parallel with other inverters with the same type of control. Droop control schemes have been applied to inverters in order to allow for stable operation in a grid-forming role. While conventional schemes have been useful thus far, there are shortcomings with conventional schemes when it comes to multiple inverters operating in parallel to one another, and for instances where tight voltage and frequency regulation is required [15], [16]. In order to overcome such shortcomings, a droop control scheme that can work universally with any output impedance, termed a universal droop controller, was proposed in [15] and [16]. For analyzing the performance of the qZSI in a grid-forming role, the universal droop control scheme will be implemented for the ac-side control. In this application, the inverter will essentially function as a swing bus, where the voltage and frequency are regulated to be close to the rated line values, while providing the real and reactive power demanded by the load.

1.3 Thesis Overview

The rest of the thesis will be organized as follows. Section 2.0 will provide a detailed overview of the 3 phase quasi-z-source inverter. First, the choice of qZSI for this work will be justified. Then, the dynamic and steady-state equations will be derived, outlining fundamental expressions for steady-state voltages and currents, as well as transfer functions to be used for modeling the dynamic behavior and stability of the qZSI. The next part provides guidelines on sizing the inductors and capacitors in the qZSI network. The final part of this section briefly

overviews common modulation techniques and control schemes for the qZSI, and which modulation technique and dc-side control scheme was chosen for this work.

Section 3.0 will provide a detailed overview of the universal droop control scheme that is used for the ac-side control of the qZSI in this work. First, the drawbacks of conventional droop control will be explained. Then, a detailed analysis of the dynamic and steady-state equations of the droop controls scheme is presented. Last, the self-synchronization scheme being used for the ac-side control is outlined.

Section 4.0 presents the proposed universal droop controlled qZSI system, the modeling of the system, and the discussion of the simulation results. First, the qZSI and voltage source inverter (VSI) systems are presented and the sizing of the components for each system is discussed in detail. Then, the control gains are chosen after being assessed for stability and desired bandwidths. The qZSI and VSI systems are designed to perform similarly, for a reasonable comparison of the two systems. Finally, the PLECs models of both systems are presented. There are two models for both the qZSI and VSI systems (four models total). The first set of models are a single inverter feeding a load – designed to test responses to a step change in load or input voltage. The second set of models consist of three inverters feeding a load in parallel – designed to test the accurate proportional load sharing between three inverters of different power ratings. For each run, the performance of the qZSI will be compared to the performance of a typical VSI system. This comparison will demonstrate if the qZSI can operate as desired in a grid forming role, and demonstrate any performance differences when compared to the VSI.

Section 5.0 contains the conclusions of the thesis work, and provides some insight on potentially useful future work regarding the universal droop controlled qZSI.

2.0 Overview of 3-phase Quasi-Z-Source Inverter

This section will provide a detailed overview of the 3-phase qZSI. In the first subsection, the various Z-source topologies are presented and compared to the qZSI, with the goal of justifying why the qZSI is best for the application in this work. In the second subsection, the dynamic and steady-state equations for the qZSI are derived. These equations are in turn compared to the equations for the boost converter that will be cascaded with the VSI for a comparison between the two systems. In the third subsection, the equations are derived for choosing the impedance component sizes for both the qZSI and boost converter. The final subsection discusses how the qZSI is typically modulated and controlled, briefly mentioning the control that will be implemented for the boost converter as well.

2.1 Justification for Studying qZSI

Seen in Figure 2.1 is the basic circuit configuration of z-source converters [7]. Note that the z-source network can be used in all power electronic conversion applications, dc/dc, dc/ac (inversion), and ac/dc (rectification). Because this work is focusing on renewable energy applications in ac power grids, the scope of this work is only focused on dc/ac inversion. Also seen in Figure 2.1, is the fact that the source of these z-source converters can be a voltage source or current source. For renewable energy systems such as wind and PV, it is much more common to use voltage source inverters (VSIs) as opposed to current source [2], [6]. Thus, from this point onward, all inverters will be assumed to have a voltage source, unless otherwise stated.

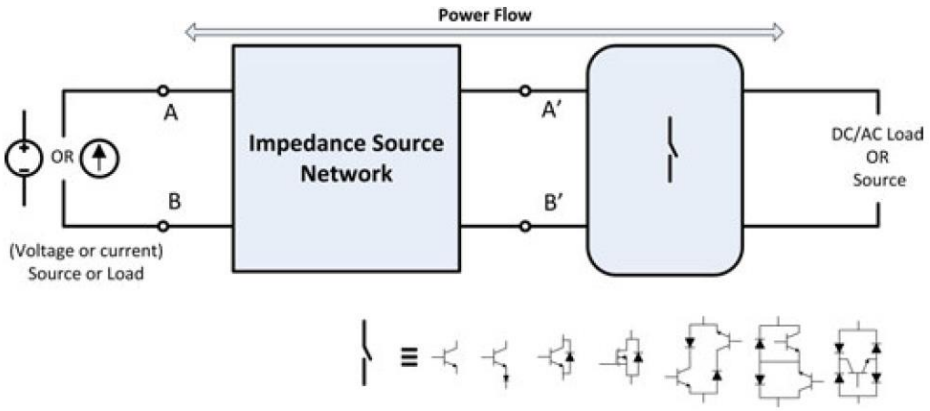


Figure 2.1: General circuit configuration of z-source converters

As seen in Figure 2.2, there is a large variety of z-source configurations, each with slight differences that provide advantages for different applications [7]. While there is no updated list for 2020, it is very likely that there are even more variations than seen in the list. Regardless of which type of impedance source is used in the converter, they all provide a number of advantages over traditional VSIs. The first, most significant advantage is that they all act as a boost stage that can boost the dc input voltage to any desired equivalent dc-link value – given that the source is a voltage source [7]. As is commonly known, VSIs can only produce an output peak voltage that is less than or equal to one half the dc input voltage [1]. Instead of using a separate switch to achieve this boost in voltage, the z-source network makes use of a new state, called a shoot-through state, in the full-bridge network [1]. The shoot-through state, which is defined as when the upper and lower devices in one or multiple phase legs are shorted, is forbidden in VSIs, as it is detrimental to the device. For voltage-source z-source networks, however, shorting the upper and lower devices in one or multiple phase legs allows for a larger equivalent dc-link voltage (V_{pn}) [6]. As mentioned in Section 1, this functionality of the z-source removes the need for dead time in modulation and increases fault tolerance of the device [6]. Thus, z-source inverters can be viewed

as single-stage inverters that can now produce an output voltage peak that is greater than or less than one half the dc input voltage. The derivation of this buck/boost functionality will be shown in the following subsections.

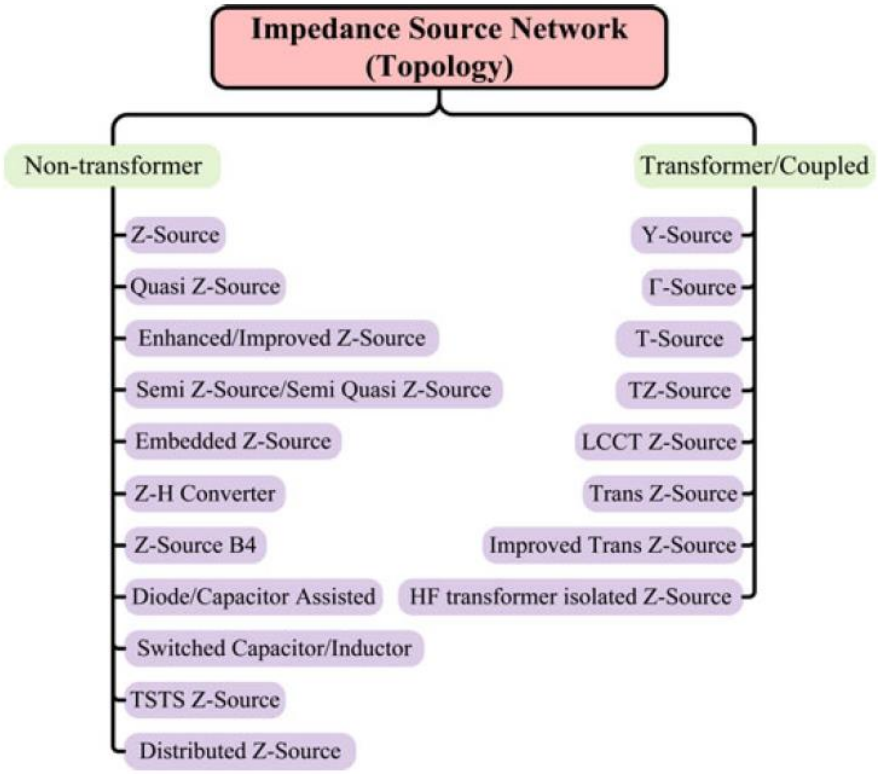
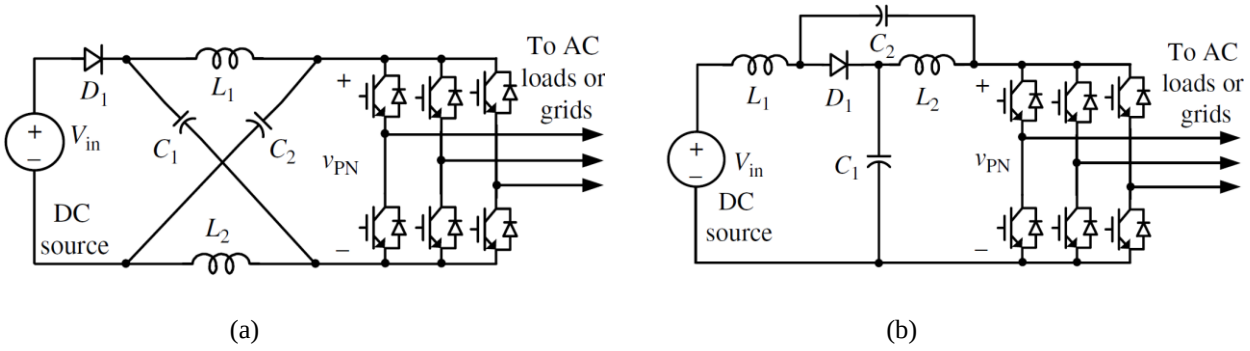


Figure 2.2: Z-source network topologies as of 2013

Of the topologies in Figure 2.2, the Z-source and Quasi-Z-Source are still among the most popular in recent literature. Seen in Figure 2.3 are the diagrams for the 3-phase ZSI and qZSI. While the ZSI and qZSI have very similar functionality, the qZSI has some key advantages that make it a more logical choice for this work. Due to the difference in inductor and diode placement between the two topologies, the qZSI has a continuous dc input current, which significantly reduces stress on the dc source. With a reduction in the input stress, the capacitance for the output

of the PV panels can also be reduced [6]. A second advantage is that the voltage across capacitor C_2 in the qZSI is less than C_1, requiring lower component ratings and leading so less stressful operation. In the ZSI, the capacitors and inductors will have identical steady-state voltages and currents, respectively, meaning they have identical voltage and current stresses and need identical ratings [1]. In the qZSI, the inductors will have identical steady-state currents, however the capacitors will have different voltages, with capacitor C_2 having a significantly lower voltage than C_1 or the capacitors in the ZSI topology [6]. This means that the stress on C_2 is lower, requiring lower ratings and resulting in lower failure rates. Aside from those differences, the control and functionality of the ZSI and qZSI are essentially identical, meaning the qZSI is no more complicated to control and has virtually no disadvantages when compared to the ZSI. For these reasons, qZSI is the converter chosen for study in this work.



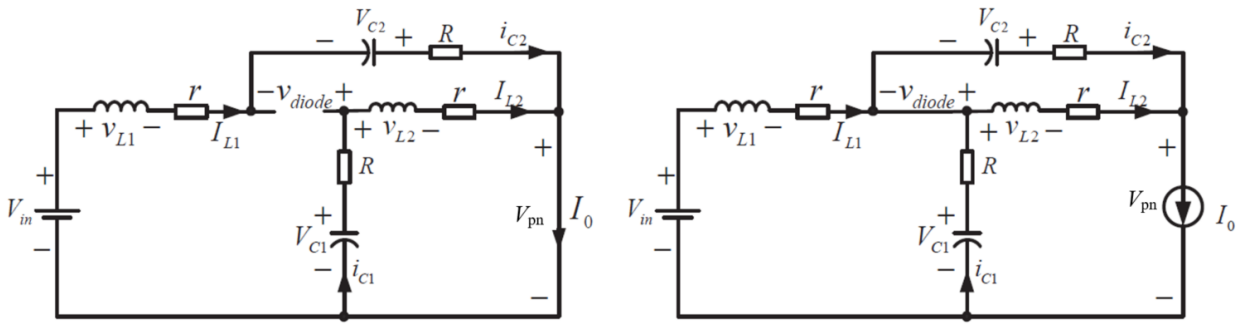
(a) (b)

Figure 2.3: Z-source inverter circuits: (a) ZSI topology; (b) qZSI topology

2.2 Dynamic and Steady-State Equations

2.2.1 Quasi-Z-Source Inverter

In order to derive the mathematical models of the qZSI, two states must be considered [5]. The first state, shown in Figure 2.4 (a), is the shoot-through state. In this state, all switching devices are gated on, shorting each phase leg. In this state, the diode is off and V_{pn} is zero volts. The second state, shown in Figure 2.4 (b), is the non-shoot-through state. This state is when the inverter is feeding the load and switching based on its traditional PWM signal. In this state, the diode is on and V_{pn} is equal to a boosted dc value that is determined by the shoot-through duty cycle. The current I_0 is the dc current that is fed into the full-bridge inverter that feeds the load. Thus, it is also called the load current. Note that equivalent series resistances for the inductors and capacitors are included in the circuit models to ensure an accurate dynamic model of the qZSI.



(a) (b)

Figure 2.4: Equivalent circuit of qZSI: (a) shoot-through state; (b) non-shoot-through state

From the work presented in [5], [17], the dynamic equations for the qZSI in the shoot-through and non-shoot-through states can be written as seen in (2-1) and (2-2), respectively.

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} * \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} \tag{2-1}$$

$$= \begin{bmatrix} -(R+r) & 0 & 0 & 1 \\ 0 & -(R+r) & 1 & 0 \\ 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} * \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} * \begin{bmatrix} v_{in}(t) \\ i_0(t) \end{bmatrix}$$

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} * \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} \tag{2-2}$$

$$= \begin{bmatrix} -(R+r) & 0 & -1 & 0 \\ 0 & -(R+r) & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} * \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 1 & R \\ 0 & R \\ 0 & -1 \\ 0 & -1 \end{bmatrix} * \begin{bmatrix} v_{in}(t) \\ i_0(t) \end{bmatrix}$$

From the dynamic equations, a state-space averaged model can be developed, seen in (2-3). Setting the derivatives equal to zero, the expected steady state values can be found for capacitor voltages (V_{C1} and V_{C2}) and inductor currents (I_{L1} and I_{L2}) – these expressions are seen in (2-4) and (2-5).

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} * \frac{d}{dt} \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix}$$

$$= \begin{bmatrix} -(R+r) & 0 & -(1-D) & D \\ 0 & -(R+r) & D & -(1-D) \\ 1-D & -D & 0 & 0 \\ -D & 1-D & 0 & 0 \end{bmatrix} * \begin{bmatrix} i_{L1}(t) \\ i_{L2}(t) \\ v_{C1}(t) \\ v_{C2}(t) \end{bmatrix} + \begin{bmatrix} 1 & (1-D)R \\ 0 & (1-D)R \\ 0 & -(1-D) \\ 0 & -(1-D) \end{bmatrix} * \begin{bmatrix} v_{in}(t) \\ i_0(t) \end{bmatrix} \tag{2-3}$$

$$\begin{cases} V_{C1} = \dfrac{1-D}{1-2D} V_{in} - V_{22} \\ V_{C2} = \dfrac{D}{1-2D} V_{in} - V_{22}, \quad where\ V_{22} = \dfrac{(1-D)(r+2DR)}{(1-2D)^2} I_0 \end{cases} \tag{2-4}$$

$$I_{L1} = I_{L2} = I_{in} = \frac{1-D}{1-2D} I_0 \cong \frac{P_{in}}{V_{in}} \tag{2-5}$$

For more simplistic steady-state expressions, the parasitic resistances can be ignored (set to 0 Ohms). Note that if the equivalent series resistances are ignored, V_{22} equals 0 V. From Figure 2.4 (b) and equation (2-2), it can be seen that the steady-state peak dc-link voltage is equal to equation (2-6) – when the parasitic resistances are ignored. Because these are just steady-state expressions designed to give an idea of what the steady state voltages and currents should be, it is okay to ignore the parasitic resistances, as they mostly impact the dynamics of the system [6]. An important note here is that the peak dc-link voltage, V_{pn}, can be boosted to any voltage greater than or equal to V_{in}. Accordingly, the duty cycle must remain less than 0.5 to prevent unstable behavior ($V_{pn} \rightarrow \infty$). From the expression for V_{pn}, the average dc-link current, I_0, can be estimated by the expression seen in (2-7) [18]. The peak dc-link voltage, Vpn, can be used to determine the peak output voltage, shown in (2-8).

$$V_{pn} = V_{C1} - v_{L2} = V_{C1} + V_{C2} = \frac{1}{1-2D} V_{in} \tag{2-6}$$

$$P_{out} = V_{pn_{avg}} * I_0 = (1-D) V_{pn} * I_0 = \frac{1-D}{1-2D} V_{in} * I_0$$

$$I_0 = \frac{P_{out}}{V_{in}} \left(\frac{1-2D}{1-D} \right) \tag{2-7}$$

$$v_{o_{pk}} = M * \frac{V_{pn}}{2} \tag{2-8}$$

The work presented in [5] goes further and derives the small-signal state equations, by the following expression:

$$F(X \dot{+} \hat{x}) = \left[(D + \hat{d})A_1 + (1 - D - \hat{d})A_2\right](X + \hat{x}) + \left[(D + \hat{d})B_1 + (1 - D - \hat{d})B_2\right](U + \hat{u})$$

Where F equals the impedance matrix seen in expressions (2-1) to (2-3). Matrices with a subscript of 1 correspond to equation (2-1), for the shoot-through state. Matrices with a subscript of 2 correspond to equation (2-2), for the non-shoot-through state. Last, equations with no subscript correspond to the matrices in equation (2-3). After simplifying and gathering like terms, the above expression can be rewritten as:

$$F\dot{\hat{x}} = A\hat{x} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}$$

Seen in (2-9) are the small-signal state equations derived from the above expression. From the small-signal state equations, the small-signal transfer functions for v_{c1} and i_{l2} can be derived, seen in equations (2-10) through (2-15). These transfer functions are essential for controller design and will be further explored in Sections 2.4 and 4.1, regarding the design of the control scheme.

$$\begin{bmatrix} L_1 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 \\ 0 & 0 & C_1 & 0 \\ 0 & 0 & 0 & C_2 \end{bmatrix} * \frac{d}{dt}\begin{bmatrix} \widehat{i_{L1}}(t) \\ \widehat{i_{L2}}(t) \\ \widehat{v_{C1}}(t) \\ \widehat{v_{C2}}(t) \end{bmatrix}$$
$$= \begin{bmatrix} -(R+r) & 0 & -(1-D) & D \\ 0 & -(R+r) & D & -(1-D) \\ 1-D & -D & 0 & 0 \\ -D & 1-D & 0 & 0 \end{bmatrix} * \begin{bmatrix} \widehat{i_{L1}}(t) \\ \widehat{i_{L2}}(t) \\ \widehat{v_{C1}}(t) \\ \widehat{v_{C2}}(t) \end{bmatrix} + \begin{bmatrix} 1 & (1-D)R \\ 0 & (1-D)R \\ 0 & -(1-D) \\ 0 & -(1-D) \end{bmatrix} * \begin{bmatrix} \widehat{v_{in}}(t) \\ \widehat{i_0}(t) \end{bmatrix} \tag{2-9}$$
$$+ \begin{bmatrix} V_{C1} + V_{C2} + I_0R \\ V_{C1} + V_{C2} - I_0R \\ -I_{L1} - I_{L2} + I_0 \\ -I_{L1} - I_{L2} + I_0 \end{bmatrix} * \hat{d}(t)$$

$$G_{\hat{d}_0}^{\hat{v}_C}(s) = \frac{\hat{v}_C(s)}{\hat{d}_0(s)}\Big|_{\substack{\hat{\imath}_0(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{(V_{C1}+V_{C2}-RI_0)(1-2D_0)+(I_0-I_{L1}-I_{L2})(Ls+r+R)}{LCs^2+C(r+R)s+(1-2D_0)^2} \quad (2\text{-}10)$$

$$G_{\hat{v}_{in}}^{\hat{v}_{C(sum)}}(s) = \frac{\hat{v}_{C(sum)}(s)}{\hat{v}_{in}(s)}\Big|_{\substack{\hat{\imath}_0(s)=0 \\ \hat{d}_0(s)=0}} = \frac{1-2D_0}{LCs^2+C(r+R)s+(1-2D_0)^2} \quad (2\text{-}11)$$

$$G_{\hat{\imath}_0}^{\hat{v}_C}(s) = \frac{\hat{v}_C(s)}{\hat{\imath}_0(s)}\Big|_{\substack{\hat{d}_0(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{R(1-D_0)(1-2D_0)+(1-D_0)(Ls+r+R)}{LCs^2+C(r+R)s+(1-2D_0)^2} \quad (2\text{-}12)$$

$$G_{\hat{d}_0}^{\hat{\imath}_L}(s) = \frac{\hat{\imath}_L(s)}{\hat{d}_0(s)}\Big|_{\substack{\hat{\imath}_0(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{(V_{C1}+V_{C2}-RI_0)Cs+(I_0-I_{L1}-I_{L2})(1-2D_0)}{LCs^2+C(r+R)s+(1-2D_0)^2} \quad (2\text{-}13)$$

$$G_{\hat{v}_{in}}^{\hat{\imath}_{L(sum)}}(s) = \frac{\hat{\imath}_{L(sum)}(s)}{\hat{v}_{in}(s)}\Big|_{\substack{\hat{\imath}_0(s)=0 \\ \hat{d}_0(s)=0}} = \frac{Cs}{LCs^2+C(r+R)s+(1-2D_0)^2} \quad (2\text{-}14)$$

$$G_{\hat{\imath}_0}^{\hat{\imath}_L}(s) = \frac{\hat{\imath}_L(s)}{\hat{\imath}_0(s)}\Big|_{\substack{\hat{d}_0(s)=0 \\ \hat{v}_{in}(s)=0}} = \frac{R(1-D_0)Cs+(1-D_0)(1-2D_0)}{LCs^2+C(r+R)s+(1-2D_0)^2} \quad (2\text{-}15)$$

The transfer functions for v_{C1} and v_{C2}, as well as i_{L1} and i_{L2}, are identical, respectively. Thus only v_C and i_L transfer functions are needed to represent both capacitors and inductors. For the sake of control, it is important to understand the behavior of the control the output transfer functions, (2-10) and (2-13), for different capacitances, inductances, and duty cycles. A very important property of the qZSI can be derived from the denominator of the transfer functions in (2-10) and (2-13) [17]. From the denominator, the natural frequency and damping ratio can be derived, seen in equations (2-16) and (2-17).

$$\omega_n = \frac{1 - 2D_0}{\sqrt{LC}} \tag{2-16}$$

$$\zeta = \frac{r + R}{2(1 - 2D_0)}\sqrt{\frac{C}{L}} \tag{2-17}$$

Figure 2.5 through Figure 2.7 show the trends of poles and zeros for (2-10) for a sweep of inductance, capacitance, and duty cycle, respectively. The steady-state values for duty cycle, inductor current, and output current are 0.225, 8.96 A, and 12.63 A, respectively. The inductance and capacitance, when not being swept, are 1 mH and 400 µF, respectively. The reason for choosing these values will be explained in Section 2.3 and 4.1. For the sweeps, the inductance is swept from 0.5 mH to 3.5 mH, the capacitance is swept from 50 µF to 750 µF, and the duty cycle is swept from 0.05 to 0.40. The arrows represent the direction of the poles and zeros as the chosen parameter increases.

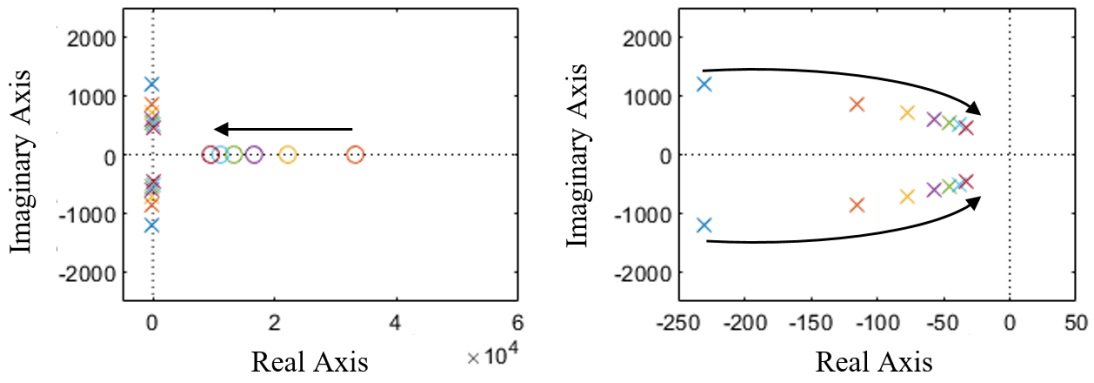


Figure 2.5: Pole-zero plot of $v_C(s)/d_0(s)$, sweep of L, (left) normal, (right) zoomed on poles

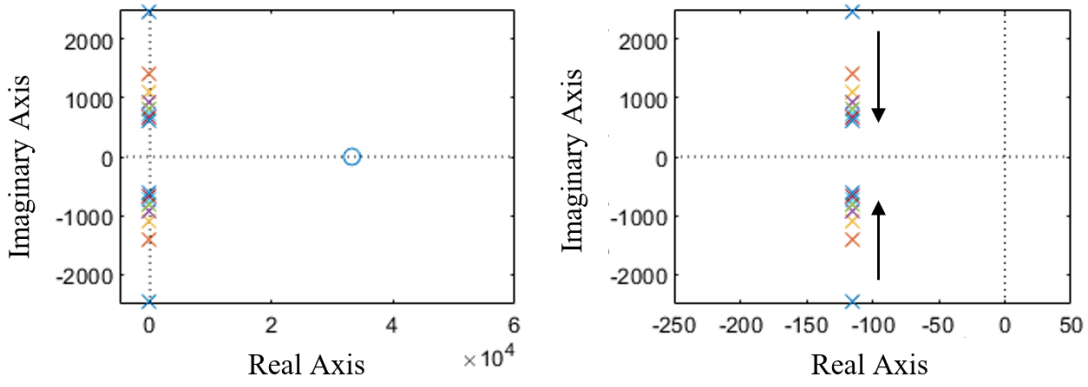


Figure 2.6: Pole-zero plot of $v_C(s)/d_0(s)$, sweep of C, (left) normal, (right) zoomed on poles

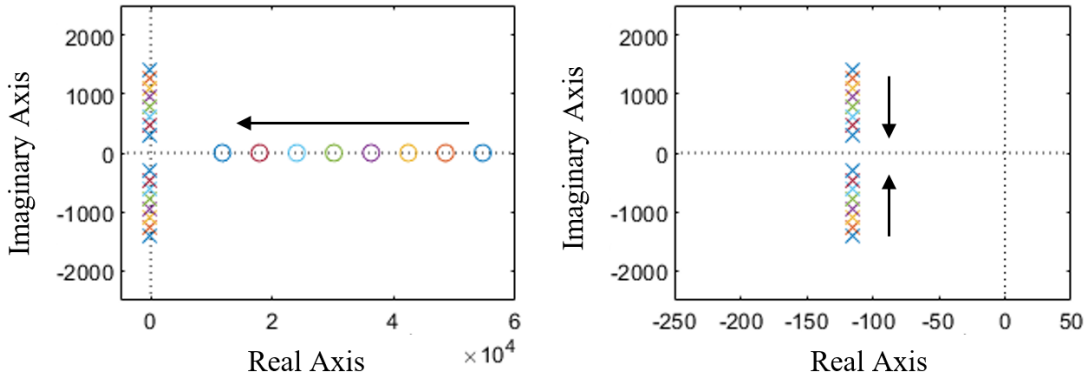


Figure 2.7: Pole-zero plot of $v_C(s)/d_0(s)$, sweep of D_0, (left) normal, (right) zoomed on poles

Figure 2.8 through Figure 2.10 show the trends of poles and zeros for (2-13) with the exact same sweeps as for (2-10). Note that the transfer functions for v_C and i_L have the same denominators, as expected based on linear system theory, and thus the poles are identical for the two sets of plots. The difference between the two transfer functions is seen in the response of the zeros.

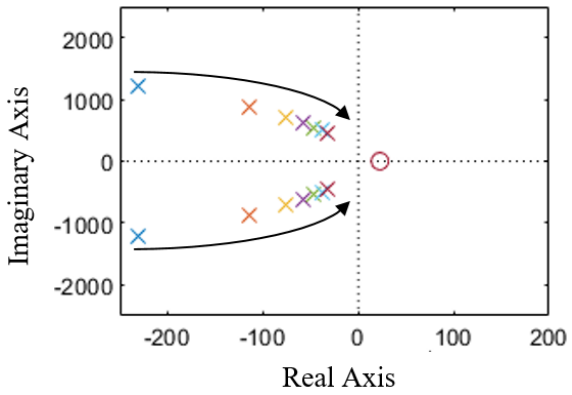


Figure 2.8: Pole-zero plot of $i_L(s)/d_0(s)$, sweep of L

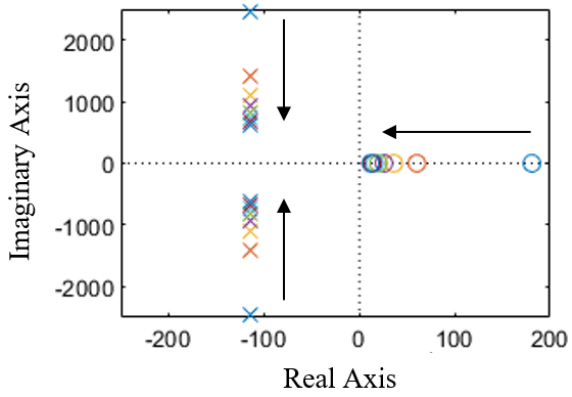


Figure 2.9: Pole-zero plot of $i_L(s)/d_0(s)$, sweep of C

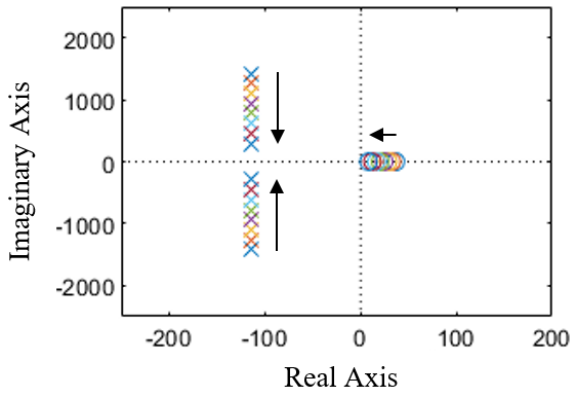


Figure 2.10: Pole-zero plot of $i_L(s)/d_0(s)$, sweep of D

From the pole zero plots, it is clear that there are no unstable poles. However, there is the presence of right half plane zeros for each transfer function regardless of impedance or duty cycle values. Right half plane zeros will result in v_C and i_L decreasing initially after a positive step change to D. Additionally, they represent the presence of non-minimum phase. Though not detrimental to system performance or stability, non-minimum phase requires careful controller design to ensure robust stability [17], [19]. The control of the qZSI can be designed in such a way to overcome such challenges, as will be discussed in detail in Section 2.3. This non-minimum phase effect can also theoretically be reduced by using smaller inductances and capacitances, however the design of those components is not arbitrary and depends on the system parameters, as will be explained in the following subsection.

2.2.2 Boost Converter

Seen in (2-18) is the averaged state-space representation of a boost converter. The expected steady-state inductor current and capacitor voltage can be calculated, seen in (2-19) and (2-20).

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} * \frac{d}{dt}\begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} -r - R(1-D) & -(1-D) \\ 1-D & 0 \end{bmatrix} * \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} + \begin{bmatrix} 1 & (1-D)R \\ 0 & -1 \end{bmatrix}\begin{bmatrix} v_{in}(t) \\ i_0(t) \end{bmatrix} \tag{2-18}$$

$$I_L = \frac{I_0}{1-D_0} \tag{2-19}$$

$$V_C = \frac{I_0((1-D_0)^2R - R(1-D_0) - r) + (1-D_0)V_{in}}{(1-D_0)^2} \tag{2-20}$$

From the work presented in [20], the control to output transfer functions for a basic boost converter, ignoring parasitic resistances, can be derived. Note that in the original text, a term is used to represent the load impedance. However, because the system for this work is feeding an inverter network, the load resistance term has been replaced with:

$$Z_{load} = \frac{V_C}{I_0}$$

The above term represents the equivalent load at the output of the boost converter. The transfer functions are shown in (2-21) and (2-22).

$$G_{\hat{d}_0}^{\hat{v}_{C_b}}(s) = \frac{\hat{v}_{Cb}}{\hat{d}_0} = \frac{V_C}{1-D_0} * \frac{\left(1 - s\left(\frac{LI_0}{(1-D_0)^2 V_C}\right)\right)}{1 + \left(\frac{LI_0}{(1-D_0)^2 V_C}\right)s + \left(\frac{LC}{(1-D_0)^2}\right)s^2} \tag{2-21}$$

$$G_{\hat{d}_0}^{\hat{i}_{L_b}}(s) = \frac{\hat{i}_{Lb}}{\hat{d}_0} = \frac{2I_0}{(1-D_0)^2} * \frac{\left(1 + s\left(\frac{V_C C}{2I_0}\right)\right)}{1 + \left(\frac{LI_0}{(1-D_0)^2 V_C}\right)s + \left(\frac{LC}{(1-D_0)^2}\right)s^2} \tag{2-22}$$

From the transfer functions, the natural frequency and damping ratio can be derived, shown in (2-23) and (2-24), respectively. There are some differences between the qZSI and boost converter. While the qZSI has RHP zero in both the current and voltage transfer functions, the boost converter only has an RHP zero in the voltage transfer function, slightly improving control performance of the inner current loop. With both voltage transfer functions containing RHP zeros, however, the inner current loop of each converter should be used to reduce the impact of the RHP zero or completely eliminate it, as explained in Section 2.4. Second, the damping ratio of the qZSI

is proportional to C:L, while the damping ratio of the boost converter is proportional to L:C. This implied that the boost converter will likely have a much larger damping ratio than the qZSI.

$$\omega_n = \frac{1 - D_0}{\sqrt{LC}} \tag{2-23}$$

$$\zeta = \frac{I_0}{2(1 - D_0)V_C}\sqrt{\frac{L}{C}} \tag{2-24}$$

2.3 Impedance Network Component Design

This section will provide design guidelines for choosing the inductances and capacitances for the qZSI and boost converter for the VSI system.

2.3.1 Quasi-Z-Source Inverter

From all reviewed literature, it is common practice to have the same inductance for both inductor and same capacitance for both capacitors, thus the following derivations apply to sizing both inductors and capacitors [21]. There are also multiple factors to consider when choosing inductance and capacitance values. Typically, to control voltage and current ripples, larger inductances and capacitances are desired. However, seen in (2-16) and (2-17), smaller L and C values result in a higher natural frequency, while a higher ratio of capacitance to inductance results in a larger damping ratio, which are both desired. Thus, there are tradeoffs to consider when sizing the impedance values.

The following derivations will provide insight on how inductances and capacitances should be chosen with regards to desired current and voltage ripples. Because it is best practice to assume worst case voltages or currents across the devices, the parasitic resistances are ignored for these derivations, as they will cause slightly lower voltages and currents. Seen below is a simplified equation for voltage across each inductor:

$$\frac{\Delta I}{\Delta T} L = V_L \rightarrow L = \frac{V_L \Delta T}{\Delta I_L}$$

From (2-1) and (2-2), the maximum inductor voltage can be found between the shoot-through and non-shoot-through intervals:

$$V_L = \begin{cases} V_{C2} + V_{in} = V_{C1}, & shoot - through \\ V_{in} - V_{C1} = -V_{C2}, & non - shoot - through \end{cases}$$

From (2-4), V_{C1} is always greater than V_{C2}, thus the maximum voltage across each inductor is V_{C1} and it occurs during the shoot-through state. Seen in (2-25) is the design equation for each inductor in order to ensure continuous conduction mode (CCM) behavior in the qZSI circuit, where T_{sw} is the switching period, D is the steady-state duty cycle, V_{C1} is the steady-state capacitor voltage, and I_L is the steady-state inductor current.

$$L \geq \frac{V_{C1} D T_{sw}}{\Delta I_L}, \quad for\ CCM: \Delta I_L < 2 * I_L \tag{2-25}$$

A similar procedure to the one outlined above can be used to determine the design equation for the capacitor capacitance. Seen below is the simplified equation for current through each capacitor:

$$\frac{\Delta V}{\Delta T} C = I_C \rightarrow C = \frac{I_C \Delta T}{\Delta V_C}$$

From (2-1) and (2-2), the maximum capacitor current can be found between the shoot-through and non-shoot-through intervals:

$$I_C = \begin{cases} -I_L, & shoot-through \\ I_L - I_0, & non-shoot-through \end{cases}$$

The maximum current through each capacitor is equal to I_L and this occurs during the shoot-through state. Because V_{C2} is less than V_{C1}, the required capacitance for the desired V_{C2} ripple will be larger than that for V_{C1}. Thus, the capacitance should be calculated using the steady-state V_{C2} voltage. This design philosophy, presented in [22], is more conservative than what is presented in [21], which is why it is used in this work. Seen in (2-26) is the design equation for each capacitor, where the variable *y%* is the desired percent ripple of the steady-state C_2 voltage.

$$C \geq \frac{I_L D T_{sw}}{(\mathrm{y}\%)\mathrm{V_{C2}}} \tag{2-26}$$

Based on available literature, common practice is to use a combination of equations (2-16) through (2-26) when picking appropriate inductances and capacitances. The pole zero plots in Figure 2.5 through Figure 2.10 also aid in determining whether the impedance values effectively keep the non-minimum phase effect reduced while meeting the desired performance criteria. Controller performance will be discussed in Section 2.4 and analyzed in great detail in Section 4.2.

2.3.2 Boost Converter

The current and voltage ripple equations for the boost converter look very similar to those of the qZSI. With the differences being in the inductor voltage and capacitor current during each interval. The ripple equations are seen in (2-27) and (2-28). Because the boost converter is one of

the most common and basic power electronics devices, the detailed derivation of the component sizing equations is not presented here.

$$L \geq \frac{V_{in} D_0 T_{sw}}{\Delta I_L}, \quad for\ CCM: \Delta I_L < 2 * I_L \tag{2-27}$$

$$C \geq \frac{I_0 D_0 T_{sw}}{(\mathrm{y}\%)\mathrm{V_C}} \tag{2-28}$$

2.4 Modulation and Control Methods

As expected, there are a variety of techniques proposed in the literature for modulating and controlling the shoot-through ratio of the qZSI [4]. When discussing the modulation techniques, this refers to the switching signals being sent to the inverter, and how they are modified from a traditional VSI in order to incorporate the shoot-through ratio. Sinusoidal pulse-width modulation (SPWM) is among the most simple and widely used techniques, and thus is what will be used for this work. Among the qZSI SPWM schemes, there is simple boost control, maximum-boost control, maximum-constant-boost control, and constant-boost control with third harmonic injection [4]. The simple-boost technique, shown in Figure 2.11, is the most basic of the four, and requires minimal modification to traditional SPWM techniques. The red dashed portion represents the shoot-through periods, where each device in each phase leg is switched on. In this technique, the magnitude of the dc signals V_p and V_n is equal to 1-D, where D is the shoot-through ratio. When the carrier triangular waveform is greater than V_p or less than V_n, the device goes into the shoot-through state. Note that this technique forces the shoot-through ratio to have a maximum

limit of 1-M, where M is the modulation index. In other words, the modulation index must decrease with an increase in the shoot-through ratio, and the device stress is slightly higher than the other modified SPWM methods [4]. The other techniques that were mentioned offer some advantages over the simple-boost PWM, however, they require slightly more complicated control and more modification to the traditional SPWM. For these reasons, the modulation scheme used in this work is the simple-boost PWM, as the goal of this work is not to optimize qZSI performance, but to rather demonstrate its ability to function in a grid forming role when compared to a traditional VSI system. Seen in Table 2.1 is a summary of the expressions in terms of modulation index for maximum shoot-through ratio, boost factor, gain, and voltage stress for simple-boost SPWM.

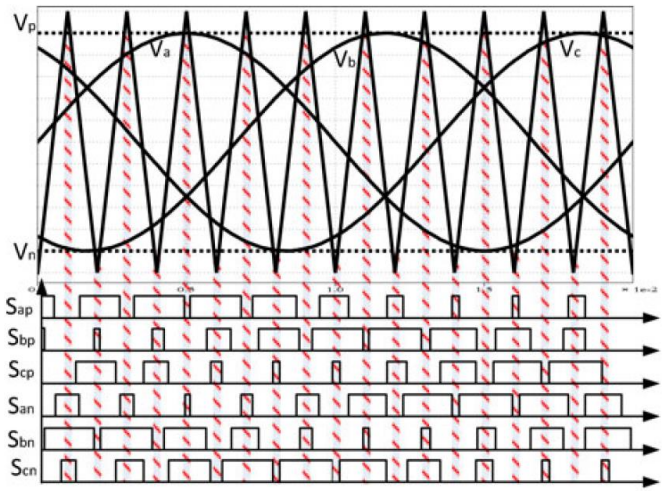


Figure 2.11: Simple-boost control SPWM [4]

Table 2.1: Key expressions for simple-boost SPWM [4]

Parameters	Simple Boost
$\bar{T}_o/T$	$1-M$
Boost Factor (B)	$\frac{1}{2M-1}$
Voltage Gain (G)	$\frac{M}{2M-1}$
Voltage Stress of the Switch	$(2G-1)V_o$
Maximum(M)	1

In order to regulate the dc-link voltage or shoot-through ratio, a control scheme is needed. Similar to the modulation methods, there are a variety of different control techniques that have been applied to the qZSI for regulating its dc-link voltage [4]. There are two main types of control for the qZSI, direct and indirect control. With direct control, the voltage across the inverter bridge is measured directly. While this method simplifies the controller design and may lead to a better transient response, it requires special sensing hardware for determining the peak dc-link voltage Vpn. The dc-link voltage is constantly pulsating between V_{pn} and 0 V, making it difficult to work with as a control signal without additional components [4], [19]. As a result, indirect control methods are more common. With these methods, the capacitor voltage (and sometimes the input voltage) is measured as used to estimate the peak dc-link voltage. A multi-loop controller for the ZSI utilizing this indirect control on the dc-side and standard dq-frame control on the ac side is proposed in [19]. This scheme is shown in Figure 2.12. As previously mentioned, the ac-side control that will be implemented in this work is the universal droop control scheme, not the scheme

shown below. For the dc-side control, however, the design from [19] can be easily applied to the qZSI and is used in this work due to its fairly simplistic design and good performance.

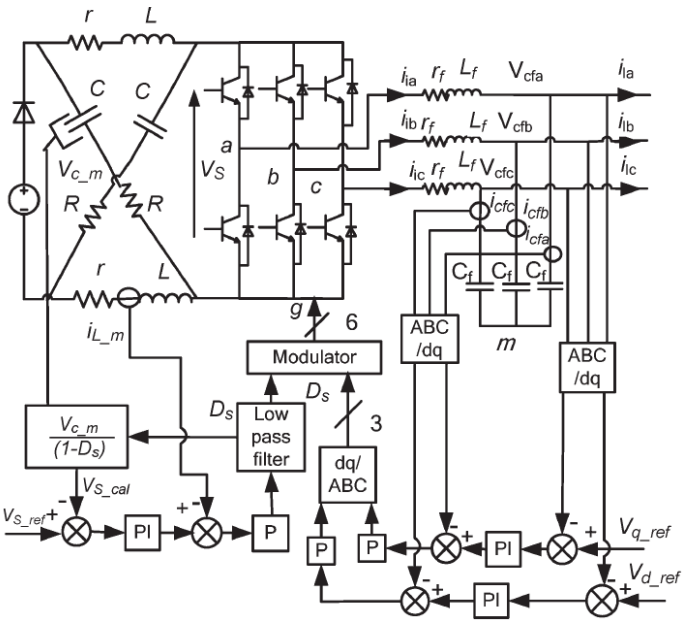


Figure 2.12: Multi-loop controller for ZSI [19]

In order to estimate the peak dc-link voltage from the measured capacitor voltage, equations (2-4) and (2-6) can be used to show:

$$V_{pn} = \frac{V_{C1}}{1 - D}$$

Note that technically the calculation for V_{pn} makes the system non-linear. In order to work around this, the shoot-through ratio, D, must be passed through a low-pass filter with a cut off frequency that is less than the bandwidth of the closed-loop system. Thus, from the perspective of the controller, D is essentially a constant, average value.

As discussed in Section 2.2, there is the presence of a RHP zero in the voltage and current transfer functions of the qZSI network, indicating the presence of non-minimum phase and the

need for careful controller design [19]. This issue is also present in typical boost converters, such as the one that will be used in this work for benchmarking against the qZSI performance. The impact of the RHP zero is reduced and the controller performance is improved by operating in the current programmed mode (CPM) [4], [19]. This method uses the outer voltage loop to generate a reference signal for the inductor current in either the boost converter or qZSI. The reference inductor current is then compared to the measured inductor current (which is identical for both inductors in the qZSI network), and fed through a proportional gain to generate the shoot-through ratio or duty cycle signal. This dual-loop scheme regulates the inductor current during transient events and extends the stability limits of the controller [4].

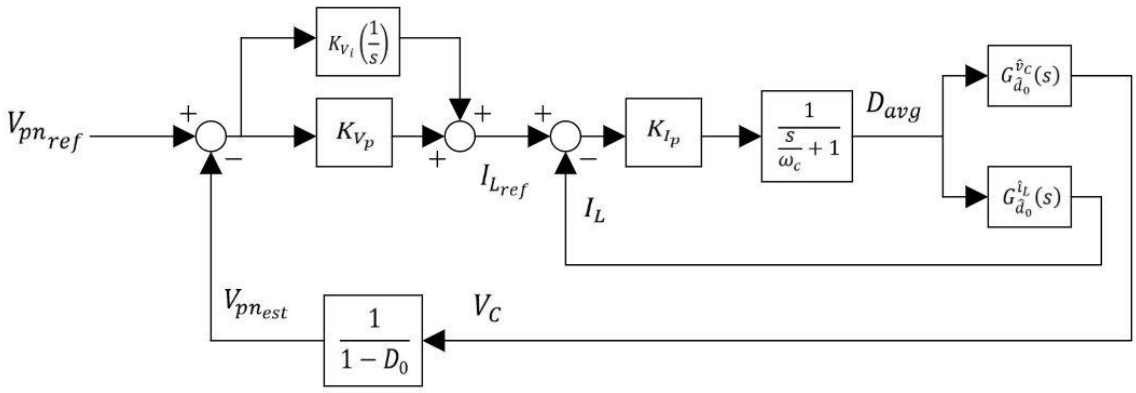


Figure 2.13: Small-signal model of qZSI dc side control system

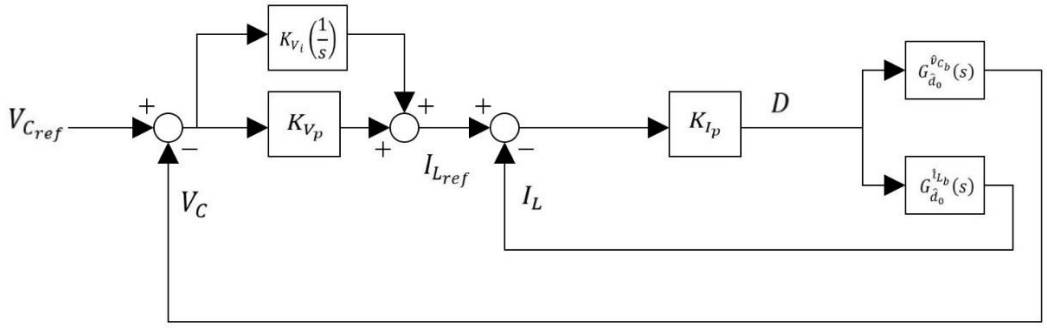


Figure 2.14: Small-signal model of VSI boost converter control system

Seen in Figure 2.13 and Figure 2.14 are the small-signal block diagrams of the qZSI and boost converter dc control schemes. The control for both devices is very similar, with the major difference being that the qZSI requires the shoot-through ratio to pass through a low pass filter in order to effectively estimate the dc-link voltage, while the boost converter dc-link voltage can be directly measured. The closed-loop transfer functions of the qZSI dc control and boost converter dc control can then be derived, shown in (2-29) and (2-30) respectively. These transfer functions will be used in Section 4.2 for assessing the control performance of the qZSI and VSI control schemes, ensuring stability and proper bandwidths.

$$G_{V_{pn_{ref}}}^{V_{pn}}(s) = \frac{\left(\frac{K_{V_i}}{s} + K_{V_p}\right) * G_{I_L} * G_{\hat{d}_0}^{\hat{v}_C} * \frac{1}{1 - D_0}}{1 + \left(\frac{K_{V_i}}{s} + K_{V_p}\right) * G_{I_L} * G_{\hat{d}_0}^{\hat{v}_C} * \frac{1}{1 - D_0}} \tag{2-29}$$

$$G_{V_{C_{b_{ref}}}}^{V_{C_b}}(s) = \frac{\left(\frac{K_{V_i}}{s} + K_{V_p}\right) * G_{I_{L_b}} * G_{\hat{d}_0}^{\hat{v}_{C_b}}}{1 + \left(\frac{K_{V_i}}{s} + K_{V_p}\right) * G_{I_{L_b}} * G_{\hat{d}_0}^{\hat{v}_{C_b}}} \tag{2-30}$$

where:

$$G_{I_L}(s) = \frac{K_{I_p} * G_{LPF}}{1 + K_{I_p} * G_{LPF} * G_{\hat{d}_0}^{\hat{i}_L}}$$

$$G_{I_{L_b}}(s) = \frac{K_{I_p}}{1 + K_{I_p} * G_{\hat{d}_0}^{\hat{i}_{L_b}}}$$

3.0 Universal Droop Control Scheme

The main goal of this section is to provide a detailed overview of the droop control scheme that is applied in this work, as well as the justification for choosing this scheme over other more conventional droop control schemes. In the first part of this section, basic functionality and drawbacks of conventional droop control schemes will be discussed with the goal of contextualizing the need for the universal droop control scheme. The second part of this section will consist of a detailed discussion of the universal droop control scheme. This discussion includes the derivation of the scheme, analysis of the dynamic and steady-state characteristics of the scheme, as well as a self-synchronizing modification that allows inverters to synchronize to the main grid voltage without the use of a phase-locked-loop (PLL).

3.1 Drawbacks of Conventional Droop Control Schemes

Figure 3.1 shows the closed-loop feedback system for a conventional droop control scheme. The control plant is for the conventional droop control scheme is a linearized small-signal representation of equations (3-1) and (3-2).

$$P = \left(\frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o}\right)\cos\theta + \frac{EV_o}{Z_o}\sin\delta\sin\theta \tag{3-1}$$

$$Q = \left(\frac{EV_o}{Z_o}\cos\delta - \frac{V_o^2}{Z_o}\right)\sin\theta - \frac{EV_o}{Z_o}\sin\delta\cos\theta \tag{3-2}$$

These equations represent the real and reactive power delivered from the voltage source (v_r) to the load terminal (v_o), through Z_o. Those variables are displayed in Figure 3.2, the generic model of one phase of a 3-phase inverter [16]. Note that while the work presented in [15], [16], [23] is for a single phase inverter, the analysis is the same for a 3 phase inverter, assuming that the load is balanced. Thus, the reference voltage generated by the droop control scheme for the 3-phase case, will be a 3-phase modulation waveform with equal amplitude and a relative phase difference between the 3 waveforms of 120 degrees.

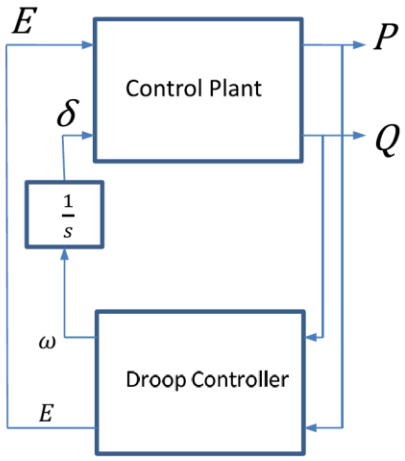


Figure 3.1: Closed-loop feedback system for conventional droop control scheme

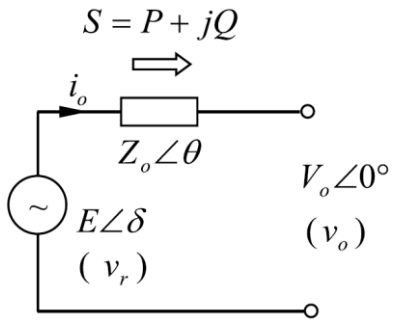


Figure 3.2: Basic model of inverter output

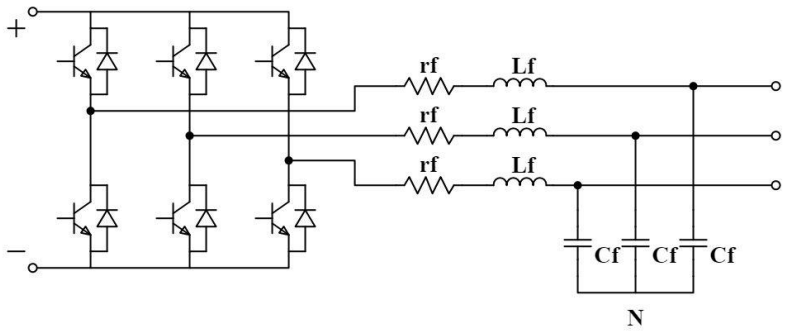


Figure 3.3: 3-phase inverter with LC filter

The output impedance of the inverter, Z_o, is defined at the terminal with the load voltage, v_o, and the filter inductor current, i_o. For an LC filter such as the one presented in Figure 3.3, this equivalent Z_o representation treats the filter capacitor as part of the load [15], [24]. This impedance can be inductive, capacitive, or resistive, and the equations for stable droop operation differ depending on the output impedance [15], [16]. For an LC filter, the impedance will either be purely inductive if the equivalent series resistance is small enough, or of the resistive-inductive (R_L) type if not. The droop controller block seen in Figure 3.1 represents the three major types of conventional droop control schemes. Table 3.1 shows the relationship between output impedance and the required droop controller [16].

Table 3.1: Conventional droop controllers for different output impedances

Inverter type	θ	Input-output/Droop relationship	Droop controller
L-	$\frac{\pi}{2}$	$P \sim \delta$	$E = E^* - nQ$
		$Q \sim E$	$\omega = \omega^* - mP$
R-	$0°$	$P \sim E$	$E = E^* - nP$
		$Q \sim -\delta$	$\omega = \omega^* + mQ$
C-	$-\frac{\pi}{2}$	$P \sim -\delta$	$E = E^* + nQ$
		$Q \sim -E$	$\omega = \omega^* + mP$
R_C-	$(-\frac{\pi}{2}, 0)$	Coupled	Depends on θ
R_L-	$(0, \frac{\pi}{2})$	Coupled	Depends on θ

The requirement of having different control schemes for different output impedances is a major drawback of conventional droop control schemes. Without additional modifications to the control, it is impossible to operate inverters with different output impedances in parallel using conventional droop control schemes. In order to prevent needing different control schemes for inverters that have different output impedances, some literature proposes the concept of using a virtual impedance controller to force the output impedance to appear resistive, capacitive, or inductive [15], [24]. Typically, it is preferable to force the output impedance to appear resistive, as it will not fluctuate with frequency and will reduce harmonic components [15]. The virtual impedance approach is not very practical, however, as it requires exact knowledge of the real angle of the output impedance.

For reasons that will become apparent in Section 3.2, the conventional droop control scheme for a resistive output impedance is the most relevant to the derivation of the universal droop control scheme. Thus, the resistive output impedance droop control scheme, shown in Figure 3.4, will be the focus of the rest of this section.

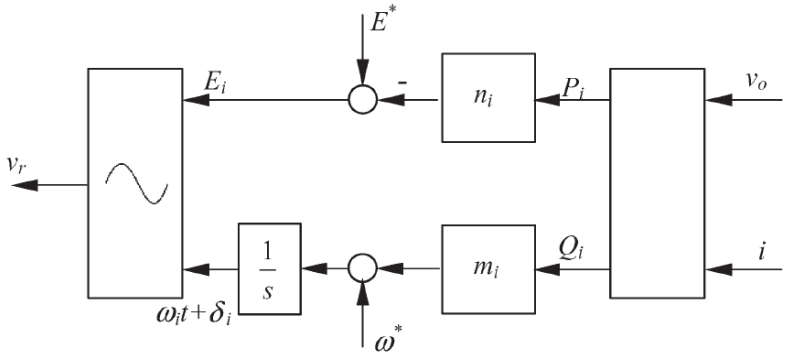


Figure 3.4: Conventional droop control scheme for resistive output impedance

The gains n_i and m_i are determined by the desired voltage drop ratio and frequency boost ratios, respectively. For the conventional control scheme, the voltage drop ratio is equal to $n_i P_i^* / E^*$ (p_{vdrop}) and the frequency boost ratio is equal to $m_i Q_i^* / \omega^*$ (p_{fboost}). An important feature of droop control schemes being used for grid-forming inverters is how they respond when multiple inverters are connected in parallel, shown in Figure 3.5 [15]. Ideally, the inverters should be able to share the load power in proportion to their individual rated powers.

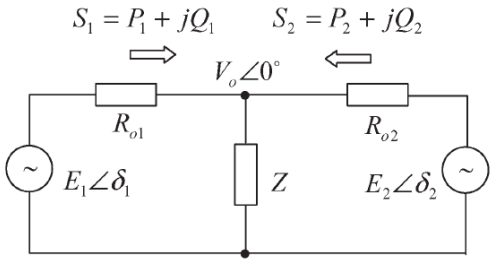


Figure 3.5: Two inverters in parallel with resistive output impedances [15]

In order to ensure this power sharing functionality, there are numerous conditions that must be met. The first condition that must be met is demonstrated below:

$$\left.\begin{aligned} n_1 S_1^* &= n_2 S_2^* \\ m_1 S_1^* &= m_2 S_2^* \end{aligned}\right\} \rightarrow \frac{n_1}{m_1} = \frac{n_2}{m_2}$$

Given that the voltage drop ratio and frequency boost ratio for the two inverters is equal (i.e. $p_{vdrop1}=p_{vdrop2}$, $p_{fboost1}=p_{fboost2}$), the above condition will always be met. An additional condition for accurate real power sharing is that E_1 must be equal to E_2, according to $\Delta P_i = -1/n_i \Delta E_i$. The only way for the two source voltages to be equal is for both inverters to have equal per-unit output impedances [15]. Note that for accurate reactive power sharing, ω_1 must equal ω_2. Because the two inverters are connected to the same output, this condition will be true, always ensuring accurate reactive power sharing between the two inverters in the steady-state. Theoretically, with the same

source voltages, and thus the same per-unit output impedances, the two inverters should also have equal phase angles, δ_1 and δ_2. If the conditions of equal source voltages or phase angles are not met, there will be significant error in the real power sharing of the inverters. In practice, the above conditions are almost impossible to satisfy in reality due to differences in feeder impedances, computational errors and disturbances, and component mismatches [15]. Thus, with conventional droop control schemes it is very difficult to attain accurate real power sharing without the addition of secondary control schemes.

The final major drawback with conventional droop control schemes is their inability to tightly regulate output voltage for changes in load. In conventional droop control schemes, there are two factors that contribute to the drop in voltage with changes in load. The first factor is known as the load effect, which states that as the load increases, the voltage drop across the output impedance Z_o will also increase, reducing the resulting load voltage. The second factor, known as the droop effect, relates to the droop equations displayed in Table 3.1 – specifically the equations for resistive output impedance. The E-P equation shows that as the load power increases, the source voltage, E, will also decrease. While the load effect cannot be compensated for without additional control schemes, the droop effect directly relates to the droop coefficient, n. A smaller n will lead to a smaller voltage drop, however this will also slow down the response of the controller. Thus, similar to the issues with power sharing, it is difficult to attain strong voltage regulation in conventional droop control schemes without additional controllers [15], [16].

3.2 Fundamentals of the Universal Droop Control Scheme

There have been many proposed methods for dealing with the drawbacks of conventional droop control. One proposed method that works specifically well for islanded grids and for accurate proportional load sharing between inverters is the universal droop control scheme (UDC). The first part of this section will discuss the basic properties and advantages of UDC, detailing why it was used for this work. The second part of this section will consider the stability and dynamics of UDC. Finally, this section will conclude with an overview of the self-synchronization scheme that is used with the UDC and implemented for the qZSI control scheme in this work.

3.2.1 Basic Properties and Advantages of the Universal Droop Control Scheme

Seen in Figure 3.6 is the universal droop control scheme that is presented in [16] and [15] and that will be used in this work. This scheme will control the qZSI to properly regulate the output voltage and frequency in a grid forming role, and accurately share real and reactive power when connected in parallel with other inverters.

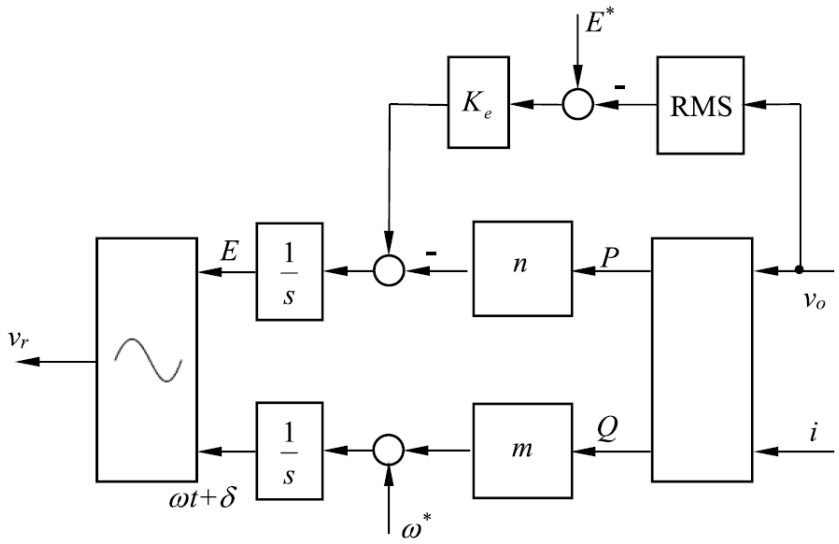


Figure 3.6: Universal droop control scheme proposed in [16]

Compared to the conventional droop control scheme in Figure 3.4, the universal droop control scheme similarly uses P-E and Q-ω control. There are two modifications to the scheme that provide significant advantages over the conventional scheme. First, E^*-V_o is fed back into the system, which will improve voltage regulation capabilities. The amplifying gain, Ke, will eliminate or considerably reduce the effect of mismatched components and computational errors on the overall power sharing capabilities. Second, an integrator is added to integrate the now ΔE values into the RMS reference. This integrator significantly improves the power sharing capabilities of the scheme [16]. Seen in (3-3) and (3-4) are the steady state equations for the universal droop control scheme.

$$\dot{E} = K_e(E^* - V_o) - nP \rightarrow nP = K_e(E^* - V_o)$$

$$V_o = E^* - \frac{n}{K_e}P \tag{3-3}$$

$$\omega = \omega^* + mQ \tag{3-4}$$

With the conventional droop control scheme, only the source voltage, E, could be controlled. As can be seen in (3-3), because the load voltage is fed back into the universal droop control scheme, it is directly regulated instead of the source voltage. Thus, the universal droop controller can compensate voltage drop due to both the load and droop effect, leading to much better voltage regulation capabilities [15], [16]. With the integrator that is now used to determine E, in the steady-state the input to the integrator should be zero. Thus, as shown in the derivation for equation (3-3), the steady state relationship for multiple inverters in parallel can be derived. This steady-state relationship also shows that as long as K_e is equal for each inverter connected in parallel, they will all accurately share real power proportionately to their power ratings. Note that the source voltages, E_1 and E_2, no longer need to be equal in order to have accurate real power sharing, which also means that the accuracy of real power sharing no longer depends on the inverter output impedances [15].

$$n_i P_i = K_e(E^* - V_o) = constant$$

$$n_1 P_1 = n_2 P_2 \rightarrow \frac{n_1}{n_2} = \frac{P_2}{P_1} \tag{3-5}$$

Because there are no modifications to the Q-ω control loop, the frequency relationship explained in Section 3.1 is true for the universal droop control scheme. In the steady-state, ω_1 will

equal ω_2, and thus accurate proportional reactive power sharing will always be achieved. The relationship is similar to that seen in (3-5).

$$m_1 Q_1 = m_2 Q_2 \rightarrow \frac{m_1}{m_2} = \frac{Q_2}{Q_1} \tag{3-6}$$

With the UDC scheme, the voltage drop ratio and frequency boost ratio are now equal to (3-7) and (3-8), respectively. Note that the voltage drop ratio can be described as the percent voltage drop (of the nominal RMS voltage) for 100% change in load real power. The frequency boost ratio can be described as the percent frequency boost (of the nominal line frequency) for 100% change in load reactive power. S_i is the rated apparent power of the given inverter. It can be seen in (3-7) that the voltage drop ratio now depends on both the droop coefficient, n_i, and the gain K_e. Thus, tight voltage regulation can be achieved with a larger droop coefficient – which keeps a reasonably fast response – by choosing a larger K_e value.

$$p_{vdrop} = \frac{n_i S_i}{K_e E^*} \tag{3-7}$$

$$p_{fboost} = \frac{m_i S_i}{\omega^*} \tag{3-8}$$

The only vulnerability that the universal droop scheme now has to error is in the measured load voltage, and reference signal for nominal RMS voltage, E*, and nominal line frequency, ω*. Error in the nominal signals should not be an issue with high quality components, however could lead to significant error in the power sharing if not considered. Error in the load voltage measurement is possible if local voltages are measured for convenience or if the sensors are not

accurate. For simulations this is not typically an issue, but for real applications this should also be considered when implementing this control scheme.

The final main advantage of the universal droop control scheme when compared to conventional droop control schemes is that it will be stable as long as the output impedance of the inverter has an impedance angle, θ, between $-\pi/2$ and $\pi/2$. While the scheme will technically not be stable for an impedance angle equal to $-\pi/2$ or $\pi/2$, there will always be at least a small parasitic resistance in series with the filter inductor or capacitor, forcing the angle to always have a magnitude less than $\pi/2$. The detailed proof of this property of the universal droop control scheme is derived in [16]. Such details are not needed for this work, and thus will not be discussed further.

Given the major advantages of UDC when compared to conventional droop control, especially for inverters operating in parallel and in a grid-forming role, this scheme was chosen for this work to be applied to the qZSI. This control scheme is a good starting point for control that can potentially be applied to the ac control of qZSIs in order to test their behavior when connected in parallel and in islanded microgrid scenarios where they are the primary grid-forming devices. As mentioned in Section 2.4, while there have been some works that apply droop control to the qZSI, there is a clear lack of literature that focuses on the qZSI in a grid-forming role, operating in parallel with other inverters. Additionally, there are no works which specifically implement the UDC with a qZSI and study its performance.

3.2.2 Consideration of Stability and Dynamics

As mentioned in Section 3.1, the control plant of the system can be mostly defined by linearizing equations (3-1) and (3-2) around the respective operating point of the system. The resulting small-signal model of the system is shown in (3-9) and (3-10).

$$\hat{P}(s) = \frac{V_{oe}(cos(\delta_e)\,cos(\theta) + sin(\delta_e)\,sin(\theta))}{Z_0} * \hat{E}(s) + \frac{E_e V_{oe}(-\sin(\delta_e)\,cos(\theta) + \cos(\delta_e)\,sin(\theta))}{Z_0} * \hat{\delta}(s) \tag{3-9}$$

$$\hat{Q}(s) = \frac{V_{oe}(cos(\delta_e)\,sin(\theta) - sin(\delta_e)\,cos\,(\theta))}{Z_0} * \hat{E}(s) - \frac{E_e V_{oe}(sin(\delta_e)\,sin(\theta) + cos(\delta_e)\,cos(\theta))}{Z_0} * \hat{\delta}(s) \tag{3-10}$$

From the linearized model, a characteristic equation can be derived, shown in (3-11). The characteristic equation can be used to ensure that the system contains no unstable poles. The pole-zero plot will be shown in Section 4.2 for the parameters being used in this work.

$$as^4\Delta\delta(s) + bs^3\Delta\delta(s) + cs^2\Delta\delta(s) + ds\Delta\delta(s) + e\Delta\delta(s) = 0 \tag{3-11}$$

where:

$$\begin{aligned} a &= Z_o^2 \\ b &= 2Z_o^2\omega_f \\ c &= Z_o\omega_f(V_{oe}(\cos\delta_e\cos\theta + \sin\delta_e\sin\theta)(n + mE_e) + Z_o\omega_f) \\ d &= Z_o\omega_f^2 V_{oe}(\cos\delta_e\cos\theta + \sin\delta_e\sin\theta)(n + mE_e) \\ e &= mnE_e\omega_f^2 V_{oe}^2 \end{aligned}$$

As explained in Section 2.4, the bandwidths of the dc side and ac side control should be significantly different in order to effectively decouple the two control schemes. The difference in bandwidths ensures that one control scheme will not interact with the other and cause oscillations that prevent the system from settling down to steady-state dc and ac values. In order to determine the bandwidth of the ac-side control, small signal models of the real and reactive power control

loops need to be developed. Seen in Figure 3.7 and Figure 3.8 are the block diagram representations of the real and reactive power droop control loops.

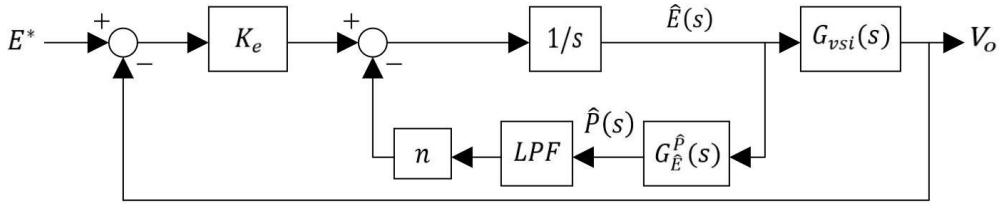


Figure 3.7: Block diagram of UDC real power loop

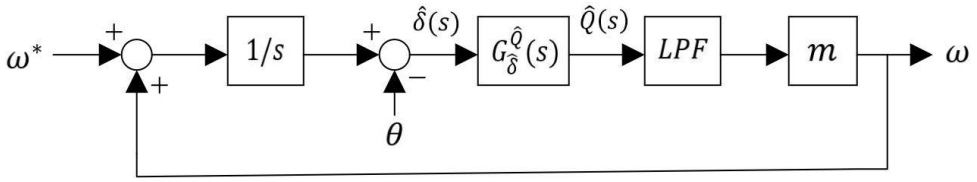


Figure 3.8: Block diagram of UDC reactive power loop

From (3-9) and (3-10), the plant transfer functions seen in the block diagrams are shown below. The transfer functions are standard equations, similar to the real and reactive power equations in (3-1) and (3-2) [16], [25]. Additionally, the method for assessing bandwidth of the droop control scheme presented in this work is similar to the work in [25].

$$G_{\hat{E}}^{\hat{P}}(s) = \frac{V_{oe}(cos(\delta_e)\,cos(\theta) + sin(\delta_e)\,sin(\theta))}{Z_0} \tag{3-12}$$

$$G_{\hat{\delta}}^{\hat{Q}}(s) = -\frac{E_e V_{oe}(sin(\delta_e)\,sin(\theta) + cos(\delta_e)\,cos(\theta))}{Z_0} \tag{3-13}$$

Because the output voltage in addition to the real power is fed back into the real power loop, a second plant model is needed in order to model the output voltage dynamics. From a control standpoint, the filter is what determines the dynamic behavior of the inverter output voltage and the H-bridge and PWM block can be ignored [18]. This model is developed by using a standard plant model for an inverter with an LC filter, shown in Figure 3.9. The most significant harmonic content beyond the 60 Hz fundamental output will occur at the switching frequency of the inverter, which was chosen to be 10 kHz for this work. Thus, the cutoff frequency of the output filter was chosen to be 1 kHz, or one tenth of the switching frequency. The load current, i_{load}, is treated as a disturbance – this is a common practice as it is unrealistic to constantly have an accurate model of the load. For the bode plot analysis in Section 4.2, the load current will be modeled according to the load being used, allowing for a more accurate representation of the AC controller bandwidth when compared to the DC-side controller bandwidth. Because the actual load will be considered in the final modeling of the inverter, the transfer function that considers the load dynamics is derived below.

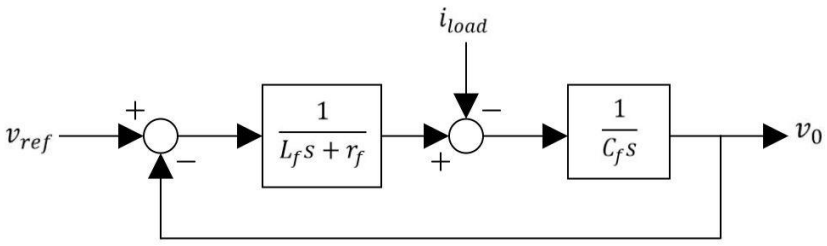


Figure 3.9: Block diagram of inverter output filter

$$Z_{load}(s) = R_{load} + sL_{load}, \qquad X_{C_f} = \frac{1}{sC_f}$$

$$Z_{eq}(s) = X_{C_f}(s) || Z_{load}(s)$$

$$Z_o(s) = R_{L_f} + sL_f$$

$$G_{vsi}(s) = \frac{Z_{eq}(s)}{Z_{eq}(s) + Z_o(s)} \tag{3-14}$$

From the block diagrams in Figure 3.7 and Figure 3.8, the transfer functions for nominal voltage to output voltage and nominal frequency to output frequency can be derived. Seen in (3-15) and (3-16) are the closed-loop transfer functions for the real and reactive power control loops, respectively. Typically, the bandwidth for droop control schemes will be low, as it is simply a reference generator for the plant [25]. Thus, in the analysis presented in Section 4.2, it will be expected that the droop control bandwidth for both the real and reactive power loops should be significantly less than the bandwidth for the dc side control in order to ensure the two schemes are decoupled and thus, operating in a stable condition [19].

$$G_P(s) = \frac{\frac{1}{s}}{1 + n\left(\frac{1}{s}\right) G_{LPF}(s) G_{\hat{E}}^{\hat{P}}(s)}$$

$$G_{\widehat{E^*}}^{\widehat{V_o}}(s) = \frac{\widehat{V_o}(s)}{\widehat{E^*}(s)} = \frac{K_e G_P(s) G_{vsi}(s)}{1 + K_e G_P(s) G_{vsi}(s)} \tag{3-15}$$

$$G_{\widehat{\omega^*}}^{\widehat{\omega}}(s) = \frac{\widehat{\omega}(s)}{\widehat{\omega^*}(s)} = \frac{m\left(\frac{1}{s}\right) G_{\hat{\delta}}^{\hat{Q}}(s) G_{LPF}(s)}{1 - m\left(\frac{1}{s}\right) G_{\hat{\delta}}^{\hat{Q}}(s) G_{LPF}(s)} \tag{3-16}$$

3.2.3 Self-Synchronization Scheme

Before an inverter is connected to the main grid, it is important that the output voltage is synchronized with the grid voltage. Seen in Figure 3.10, modifications were made to the UDC that allow it to operate in different modes from the droop mode presented in Section 3.2.1 [23]. One of the modes of operation is the self-synchronization mode, which synchronizes the inverter with the grid voltage before connecting to the load. This scheme does not require the use of a phase-locked-loop (PLL), which is another advantage over other schemes due to the instability issues that have been presented regarding PLLs [26], [27].

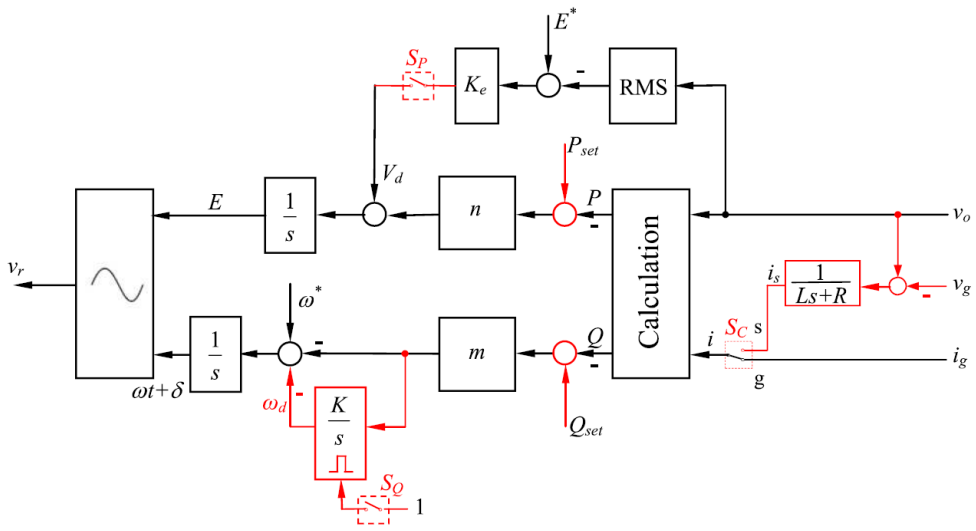


Figure 3.10: Universal droop controller with self-synchronization [23]

The switching signals required to implement each mode are shown in Table 3.2. The only two modes that are implemented in this work are the self-synchronization mode and droop mode (P_D-mode, Q_D-mode). Operation in any of the other modes (P-mode and Q-mode) would be used for situations where the inverter is operating to supply a set amount of real and/or reactive power at the nominal voltage/frequency of the line. This situation would occur for an inverter connected to the main grid, with no need to regulate both the voltage and frequency at the same time.

Table 3.2: Operation modes of modified universal droop controller

Mode	Switch S_C	Switch S_P	Switch S_Q
Self-synchronization mode	s	OFF	OFF
P-mode, Q-mode	g	OFF	OFF
P_D-mode, Q-mode	g	ON	OFF
P-mode, Q_D-mode	g	OFF	ON
P_D-mode, Q_D-mode	g	ON	ON

For convenience, the modified UDC can be represented by the following expressions:

$$\dot{E} = V_d + n(P_{set} - P)$$
$$\omega = \omega^* + \omega_d - m(Q_{set} - Q)$$

Where

$$V_d = \begin{cases} 0, & (S_P = \text{OFF}) \\ K_e(E^* - V_o), & (S_P = \text{ON}) \end{cases}$$
$$\omega_d = \begin{cases} \frac{mK}{s}(Q - Q_{set}), & (S_Q = \text{OFF}) \\ 0, & (S_Q = \text{ON}) \end{cases}$$

For droop mode, S_C is set to ‘g’, S_P and S_Q are ON, and the set values for P and Q are simply 0 W/var. The droop mode allows the inverter to swing to any output powers that are required by the load, while still regulating output voltage and frequency to relatively tight margins.

Thus, an inverter operating in a grid-forming role (similar to a swing bus), will be logically set to droop mode [23].

For self-synchronization mode, S_C is set to 's', S_P and S_Q are OFF, and the set values for P and Q are still 0 W/var. The goal of this mode is to synchronize the inverter to the grid voltage and frequency (v_g and ω_g) before connecting to the grid. When S_P and S_Q are OFF, P and Q are regulated to their reference values, which in this case are both set to zero. In order to force the inverter to start synchronizing with the grid, a virtual impedance is introduced to generate a virtual current measurement into the control scheme. In order to regulate P and Q down to their reference of zero, UDC will inherently attempt to minimize the virtual current (i_s), which is equivalent to regulating v_o to be as close to v_g as possible. Synchronization is achieved once P and Q are regulate to be around zero, and now the inverter can be safely connected to the grid/load [23]. A demonstration of what the inverter voltage looks like as it synchronizes is seen in Figure 3.11 [23]. Additionally, this scheme does not require a PLL, reducing required measurements and improving stability [26], [27].

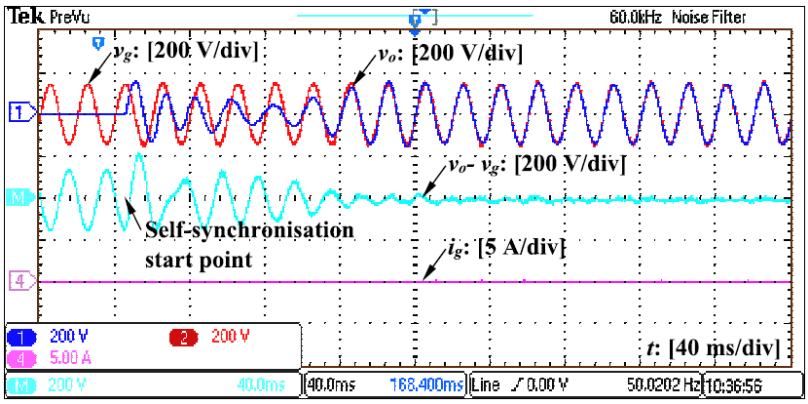


Figure 3.11: Experimental demonstration of self-synchronization scheme [23]

4.0 Proposed Control Scheme for 3-phase Quasi-Z-Source Inverter

The proposed universal droop control scheme for 3-phase qZSIs is presented in this section. First, an overview of the system is presented, now combining the dc and ac sides that were explained in Sections 2.4 and 3.2, respectively. The test cases designed to analyze the performance of the qZSI system compared to the VSI system are outlined in detail. The component design for both the qZSI and VSI boost converter is described, presenting the component values to be used in each simulation model. Then, the selection of control parameters is discussed, with analysis of stability margins and bandwidths for both the dc and ac control schemes. Finally, the results from the PLECS models are presented and discussed in detail.

4.1 System Overview

This subsection will explain the system models being used to demonstrate the performance capabilities of the universal droop controlled 3-phase qZSI, benchmarked against a common VSI system with similar universal droop control.

4.1.1 System Schematics and Test Case Descriptions

Seen in Figure 4.1 is the 3-phase qZSI system that is being studied in this work. For benchmarking its performance, the qZSI system will be compared to a common voltage source

inverter (VSI) scheme for renewable energy systems that has a boost converter on the input to regulate the dc-link voltage [2]. This system is seen in Figure 4.2.

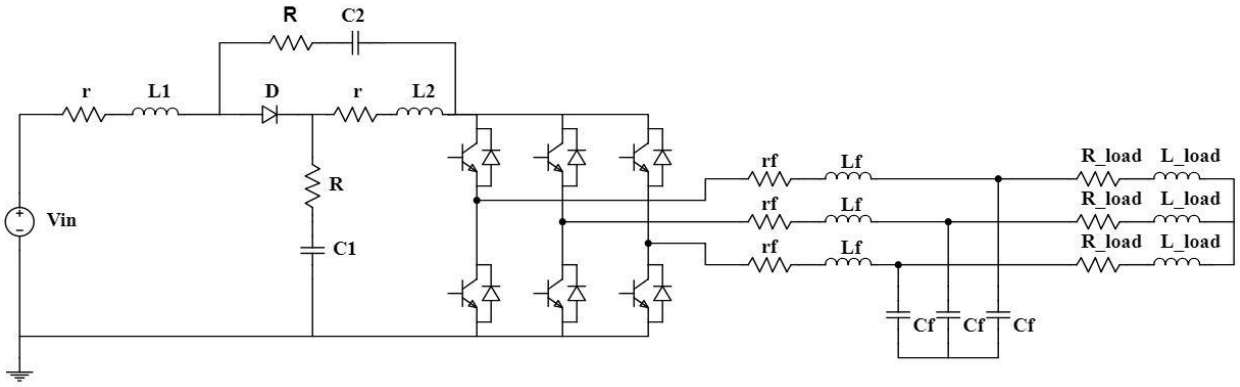


Figure 4.1: qZSI system under study

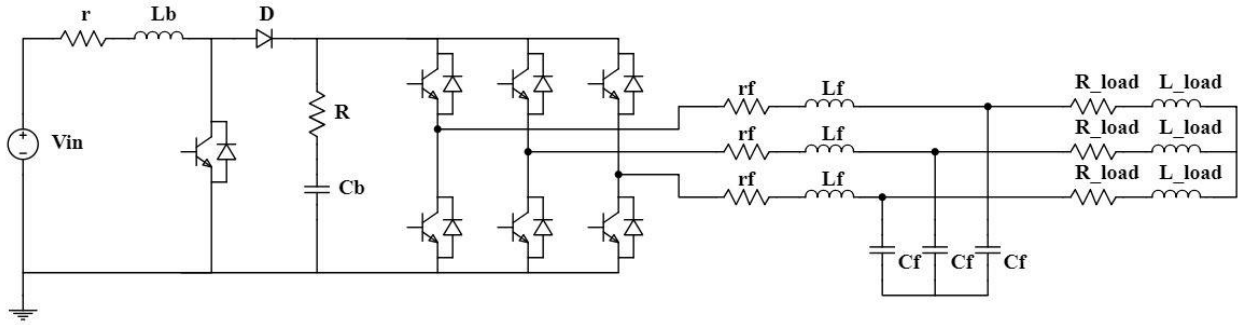


Figure 4.2: VSI system for benchmarking

For testing the performance of the qZSI system, three different scenarios were tested. The first two scenarios are for the single inverter models seen in Figure 4.1 and Figure 4.2. The first test case is a step change in an L-R load from 6.9 kW and 2.6 kvar up to 13.8 kW and 5.2 kvar. This scenario should demonstrate the voltage and frequency regulation capabilities of the universally controlled qZSI, demonstrating that it is able to exhibit grid-forming behavior as well as the VSI system. The second test case is a step change in input voltage from 550 V down to 440

V, representing a sudden voltage sag of 20%. This scenario is designed to demonstrate the ability of the qZSI to handle input voltage disturbances with minimal impact on the AC side. Additionally, it should show that the qZSI performs at least as well as a boost cascaded VSI system, removing the need for an additional switching device – improving efficiency. The single inverter test cases are summarized in Table 4.1.

Table 4.1: Summary of single-inverter test cases

Inverter Rated Power	Test Case Description
15 kVA	100% step change in load: • 6.9 kW, 2.6 kvar → 13.8 kW, 5.2 kvar
15 kVA	20% step change in input voltage: • 550 V → 440 V

The third test case is for a slightly different model, seen in Figure 4.3. This model consists of three inverters feeding an L-R load in parallel. The load is approximately 40 kW and 16 kvar. Each inverter will have different power ratings, which, as explained in Section 3.0, determines how much of the load they will feed. Each inverter is switched on at different times, thus the first inverter to switch on will be rated for 45 kVA, the second inverter will be rated for 30 kVA, and the final inverter to switch on will have a rating of 15 kVA. This scenario is designed to simply demonstrate the fact that the power sharing capabilities of the universal droop control scheme still hold true for the qZSI system. Based on the analysis in Section 3.2.1, the steady state real and reactive powers supplied by each inverter should obey the relationship in (3-5) and (3-6). The power equations can easily be extrapolated for any *i* inverters in parallel. The three inverter test case is summarized in Table 4.2. Due to the inability to operate a boost converter and qZSI

unloaded, a “start-up load” is required in order for the inverters to function properly in self-synchronization mode. How each inverter is powered on and connected in the model will be explained in detail in Section 4.3.2.

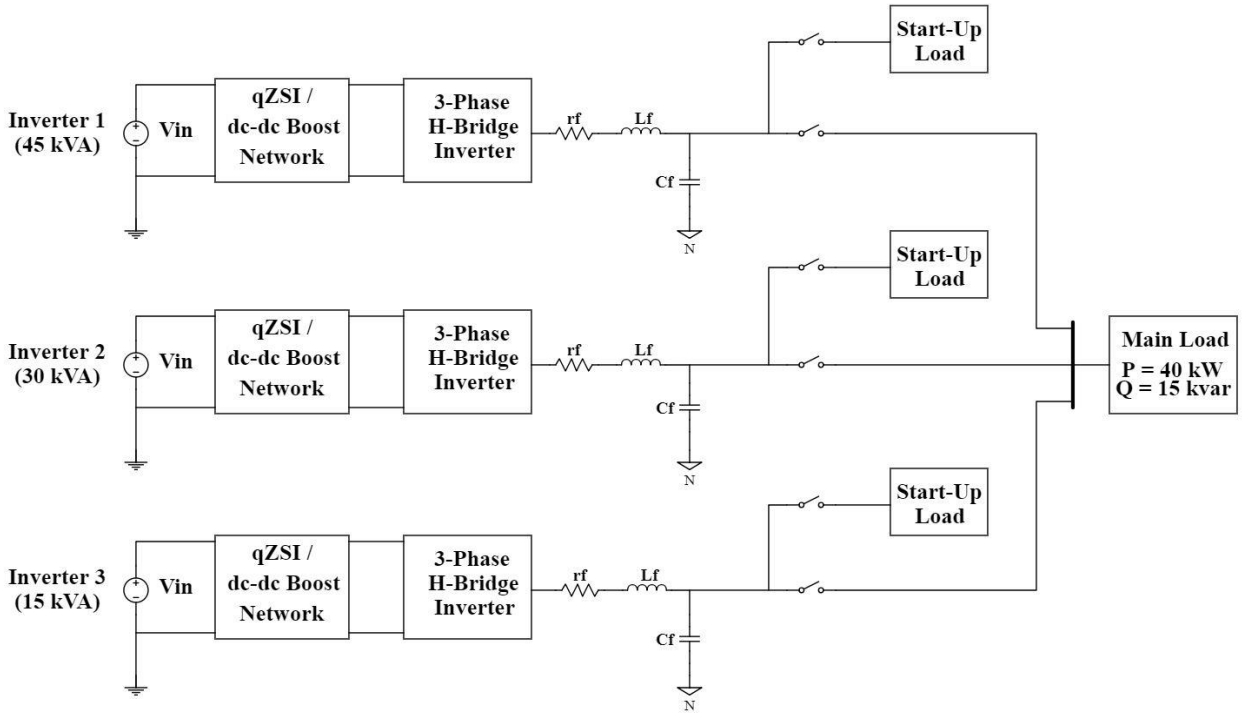


Figure 4.3: Parallel inverter system

Table 4.2: Summary of parallel inverter test case

Inverter 1 Rated Power	Inverter 2 Rated Power	Inverter 3 Rated Power	Test Case Description
45 kVA	30 kVA	15 kVA	3 inverters connected in parallel to a common load: • Load: 42 kW, 16 kvar • Inverter 1 is initially connected to the load, inverter 2 and 3 are disconnected • After inverter 1 reaches steady-state, inverter 2 is connected to the load, inverter 3 is still disconnected • After inverters 1 and 2 reach steady-state, inverter 3 is connected to the load. All three inverters are now feeding the load in parallel

4.1.2 Component Design of qZSI and VSI

For each test case outlined in Section 4.1.1, the range for steady-state inductor currents, capacitor voltages, and duty cycles need to be determined in order to design the qZSI system to work properly in each scenario. For the single inverter model, one design will be made for all scenarios. For the parallel inverter model, each of the three inverters will have different impedance values because they are designed to operate at different output powers.

For both the single inverter and three inverter models, there are similarities in system parameters. For each system, V_{in} was chosen to have a nominal values of 550 V, and the nominal output frequency was 60 Hz. For the single inverter model, the nominal output voltage was chosen to be 230 V_{rms}. For the parallel inverter model, the nominal output voltage was chosen to be 200 V_{rms}. The inverters are feeding an L-R load. In order to produce the desired output voltage with some margin in the duty cycle, the reference for V_{pn} is chosen to be 1000 V for both models. With

these system parameters, equations (2-4) through (2-7) can be used to determine, ignoring the parasitic resistances, the expected steady state parameters of the qZSI system for each test scenario.

For the single inverter model undergoing a step change in V_{in} or load, the expected ranges in steady-state voltages, currents, and duty cycle are shown in Table 4.3. Also shown in this table are the minimum inductances and capacitances needed to meet the design parameters of CCM operation and 5% voltage ripple on V_{C2} – calculated using equations (2-25) and (2-26). With these minimum component values in mind, it is now required to look at the natural frequency and damping ratio of the system to offer further guidance on component sizes. Using equations (2-16) and (2-17), the natural frequency and damping ratio of the system for an inductance of 0.69 mH and capacitance of 51 µF are approximately 3000 rad/s (475 Hz) and 0.056, respectively. While the natural frequency is acceptable, the damping ratio is not. Choosing an inductance of 1 mH and a capacitance of 400 µF give a natural frequency of 695 rad/s (110 Hz) and damping ratio of 0.165. From the controller analysis in Section 4.2, it will be seen that these impedances allow the qZSI to behave acceptably. Additionally, they ensure a RHP zero that is relatively far from the origin, seen in the pole zero plots in Section 2.2.

Table 4.3: Single qZSI model parameter ranges

Parameter	Range for Step Change in V_{in}	Range for Step Change in Load
D	0.225 – 0.280	0.225
V_{C1}	720 – 775 V	775 V
V_{C2}	225 – 280 V	225 V
I_L	12.6 – 15.8 A	12.6 – 25.3 A
I_0	8.96 – 9.65 A	8.96 – 17.93 A
L_{min}	0.69 mH	0.69 mH
C_{min}	32 μF	51 μF
Chosen L	1 mH	
Chosen C	400 μF	

A similar procedure can be used to design the inverters for the parallel inverter model. Seen in Table 4.4 are the expected ranges in inductor and load dc-link current, and minimum component sizes for each inverter in the parallel qZSI inverter model. Because only powers are changing in this model, the duty cycle and capacitor voltages should remain around the same steady state values and are not shown in the table. Similar to the single inverter model, the impedance parameters were chosen based on the current and voltage ripple equations, as well as for a reasonable natural frequency and damping ratio. The capacitances and inductances were chosen to produce a natural frequency and damping ratio similar to those for the single inverter model, since those parameters exhibited acceptable control performance.

Table 4.4: Parallel qZSI model parameter ranges

Parameter	Inverter 1	Inverter 2	Inverter 3
S_{rated}	45 kVA	30 kVA	15 kVA
P_{out}	21 – 42 kW	3 – 17 kW	3 – 7 kW
I_L	38.2 – 76.4 A	5.5 – 30.6 A	5.5 – 12.7 A
I_0	27.1 – 54.2 A	3.9 – 21.7 A	3.9 – 12.7 A
L_{min}	0.23 mH	1.60 mH	1.60 mH
C_{min}	153 µF	61 µF	25 µF
Chosen L	0.5 mH	2 mH	2 mH
Chosen C	300 µF	200 µF	200 µF

The procedure for sizing the components for the boost converter, seen in Figure 4.2, is similar to sizing the qZSI components. As expected, the desired voltage and current ripples help to set minimum values for capacitance and inductance, and then the natural frequency and damping ratio of the system must also be considered. Seen in Table 4.5 are the ranges of different parameters for the boost converter in the single VSI model from Figure 4.2. The test scenarios for the single VSI model are those outlined in Table 4.1. Note that in order to produce 230 Vrms at the output of the inverter, the dc reference of the boost converter was chosen to be 700 V. Plugging the minimum component values into equations (2-23) and (2-24) yields a natural frequency of approximately 8513 rad/s (1355 Hz) and damping ratio of approximately 0.079. While the natural frequency is high, which is desirable, the damping ratio is lower than that of the qZSI. Additionally, it is not best practice to use the minimum derived capacitance. Choosing an inductance of 3 mH and capacitance of 15 µF yield a natural frequency and damping ratio of 2963 rad/s (472 Hz) and 0.1595, respectively. These parameters were chosen because they produce a similar damping ratio

to that of the qZSI, which should provide a good case for benchmarking the qZSI performance. It should be noted that because of the damping ratio depending on L:C instead of C:L, a much smaller capacitance and larger inductance is needed than with the qZSI to achieve the same performance.

Table 4.5: Single VSI model parameter ranges

Parameter	Range for Step Change in V_{in}	Range for Step Change in Load
D	0.214 – 0.371	0.214
V_{Cb}	700 V	700 V
I_L	12.6 – 15.8 A	12.6 – 25.3 A
I_0	9.93 A	9.93 – 19.85 A
L_{min}	0.52 mH	0.47 mH
C_{min}	11 µF	12 µF
Chosen L	3 mH	
Chosen C	15 µF	

Seen in Table 4.6 are the parameter ranges for the parallel VSI model seen in Figure 4.3. Again, because only powers are changing in this model, the duty cycle and capacitor voltages should remain around the same steady state values and are not shown in the table. Similar to the single inverter model, the impedance parameters were chosen based on the current and voltage ripple equations, as well as for a reasonable natural frequency and damping ratio. The capacitances and inductances were chosen to produce a natural frequency and damping ratio similar to those for the single inverter model, since those parameters are expected to exhibit acceptable control performance. Similar to the single inverter case, the inductances for the VSI model are larger than those for the qZSI model, while the capacitances are smaller.

Table 4.6: Parallel VSI model parameter ranges

Parameter	Inverter 1	Inverter 2	Inverter 3
S_{rated}	45 kVA	30 kVA	15 kVA
P_{out}	21 – 42 kW	3 – 17 kW	3 – 7 kW
I_L	38.2 – 76.4 A	5.5 – 30.6 A	5.5 – 12.7 A
I_0	30.0 – 60.0 A	4.3 – 24.0 A	3.9 – 12.7 A
L_{min}	0.15 mH	1.08 mH	1.08 mH
C_{min}	37 µF	15 µF	6 µF
Chosen L	1.5 mH	10 mH	10 mH
Chosen C	50 µF	15 µF	10 µF

4.2 Control Parameter Design

Seen in Figure 4.4 is the qZSI system with the modified universal droop control scheme controlling the ac output, and the indirect control scheme regulating the dc-link voltage. The small-signal representations of the qZSI and VSI dc-side control schemes are seen in Figure 2.13 and Figure 2.14, respectively. As previously discussed, the qZSI control scheme requires passing the shoot-through ratio through a low pass filter in order to preserve linear behavior in the system. A low pass filter is not needed for the boost converter control. Aside from that difference, the two control schemes are very similar, and thus were designed to have similar stability margins and bandwidths.

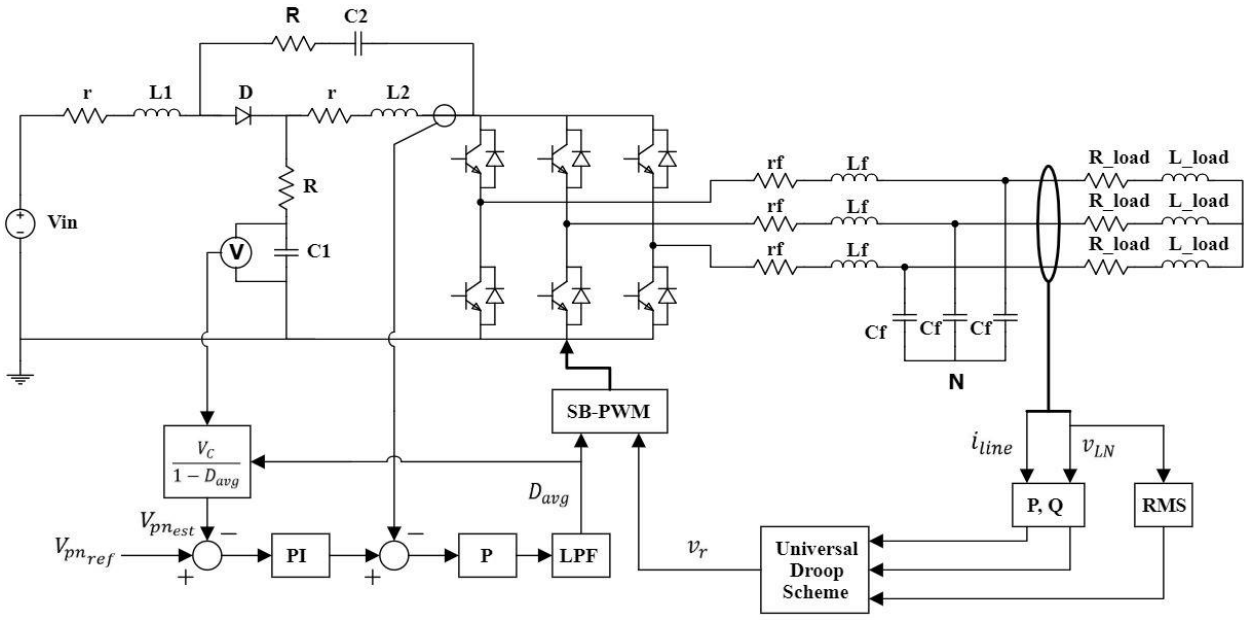


Figure 4.4: qZSI system with full control scheme

Using the transfer functions derived in (2-29) and (2-30), the dc-side control schemes can be analyzed. Seen in Table 4.7, are the chosen gains, the approximate stability margins, and cross-over frequencies for each single inverter model. Seen in Table 4.8, are the chosen gains and corresponding margins and cross over frequencies for each parallel inverter model. Note that these gains were calculated for each test case outlined in Table 4.1 and Table 4.2. There were slight differences in stability margins and cross-over frequencies between the cases, however the differences are so minor that the average of each case is provided. Note that these designs were focused on ensuring that each model is stable, and also ensuring that they have similar bandwidths in order to more accurately benchmark the qZSI with a VSI model.

Table 4.7: Control paramters and stability margins for single inverter models

Parameter	qZSI DC Control	VSI Boost Control
K_{Vi}	12	30
K_{Vp}	0.5	0.1
K_{Ip}	0.01	0.005
ω_c (rad/s)	10	n/a
PM (deg.)	78	109.5
GM (dB)	7	12
ω_{cross} (rad/s)	106	116
f_{cross} (Hz)	16.9	18.5

Table 4.8: Control paramters and stability margins for parallel inverter models

Parameter	qZSI DC Control	VSI Boost Control
K_{Vi}	12	30
K_{Vp}	0.5	0.1
K_{Ip}	0.005	0.0025
ω_c (rad/s)	10	n/a
PM (deg.)	73	98
GM (dB)	9	22
ω_{cross} (rad/s)	60	59
f_{cross} (Hz)	9.5	9.4

Shown in Figure 4.5 and Figure 4.6 are the bode plots for the open-loop and closed-loop dc-side control transfer functions of the qZSI model. Shown in Figure 4.7 and Figure 4.8 are the bode plots for the open-loop and closed-loop dc-side control transfer functions of the VSI boost converter model. It can be seen that their frequency responses are very similar in terms phase

margin and cross over frequency. It is widely understood that a positive, and adequately large phase margin (greater than 60 degrees) is preferred to limit ringing and overshoot in the system response, thus, both system were designed to have phase margins larger than 60 degrees [20]. Overall, the VSI system was more easily designed to have a larger phase margin while maintaining the same bandwidth. It was much more difficult to increase the phase margin of the qZSI without drastically reducing the bandwidth of the qZSI system. Typically, a gain margin greater than 6 dB is considered adequate [20]. Thus, the average gain margin of both systems is larger than 6 dB. Similar to the difference in phase margins, it was easier to achieve higher gain margins with the VSI system without sacrificing bandwidth.

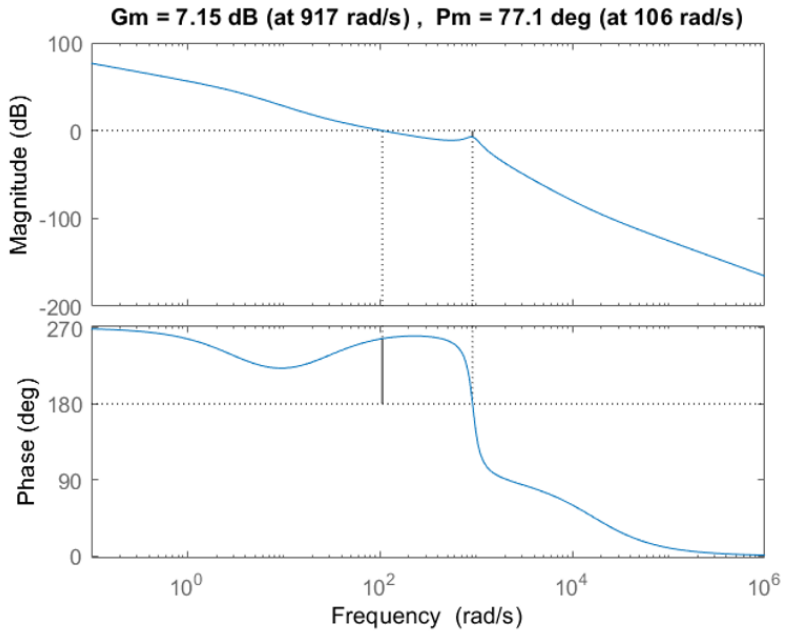


Figure 4.5: Open-loop bode plot of qZSI control system

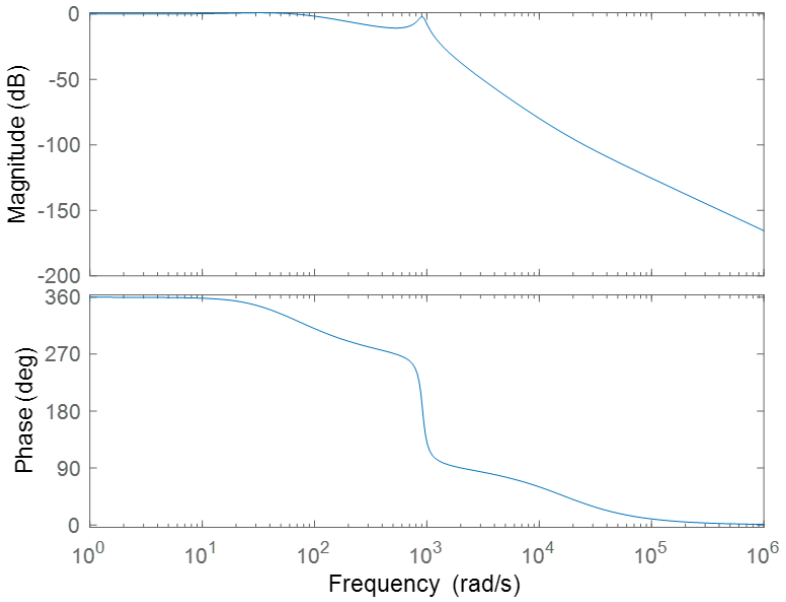


Figure 4.6: Closed-loop bode plot of qZSI control system

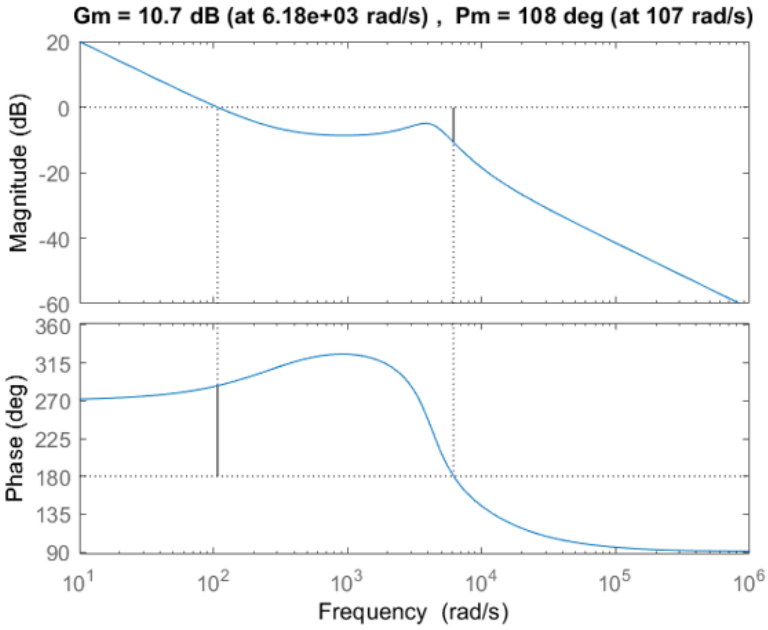


Figure 4.7: Open-loop bode plot of VSI boost converter control system

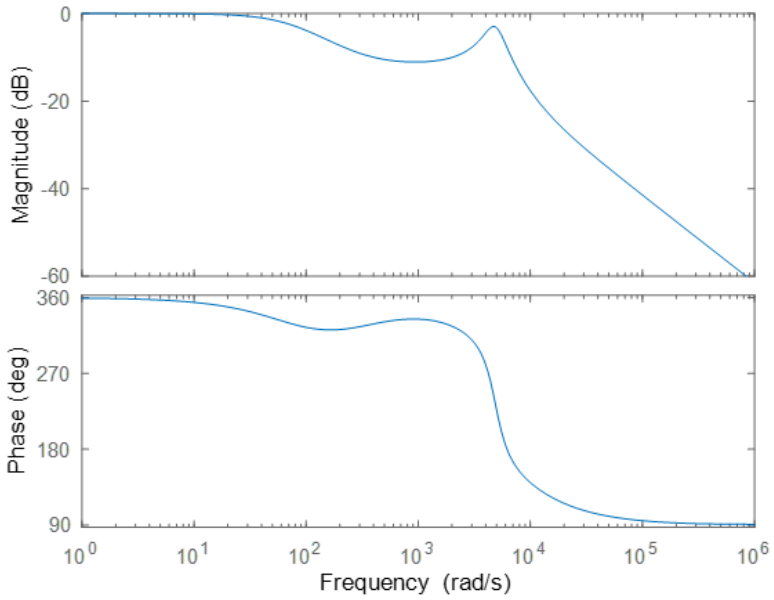


Figure 4.8: Closed-loop bode plot of VSI boost converter control system

Figure 4.9 and Figure 4.10 show the pole zero plots for the closed loop VSI and qZSI systems. The RHP zeros for each system are not shown in the plots, as the RHP zero in each system occur at frequencies between 14000 and 16000 rad/s. At such a large distance away from the origin, the effect of these RHP zeros is minimized [19], [20]. As expected, there are no unstable poles in either system. Another important note is that both systems contain a few zeros that very closely line up with certain poles, reducing the impact of those poles. The location of the poles and zeros of each system can offer some insight on the speed of response and damping of the system in the time domain. It is known that the magnitude of the real part of each pole is inversely related to the settling time of the system. Additionally, the angle of each pole, or the ratio of the imaginary component to the real component, will determine the damping of the system, or percent overshoot [28]. On the other hand, the presence of LHP zeros will speed up the response time, however, as the zeros move further and further away from the origin (the real part increases in magnitude), their impact on the settling time decreases. Thus, looking at the pole zero plots for the qZSI and

VSI systems, the qZSI poles are significantly closer to the origin, potentially indicating a slower response. However, the non-cancelled LHP zero of the qZSI is much closer to the origin than that of the VSI system [28]. Thus, in general, it is hard to make conclusions regarding the speed of response of each system based off of the pole-zero plots. Because the transfer functions of each system are greater than second order, it is also difficult to gain any insight on response times from the transfer functions without additional reduction in the order.

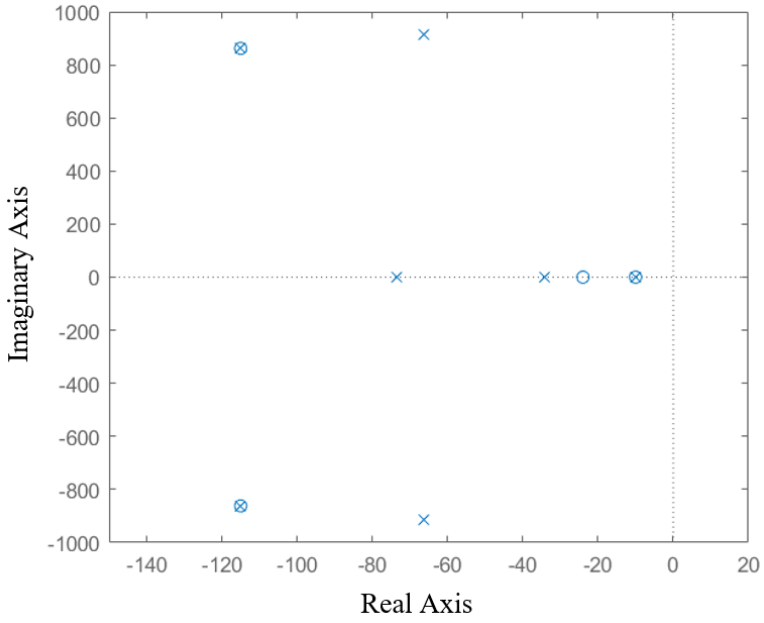


Figure 4.9: Pole-zero plot of closed-loop qZSI control system

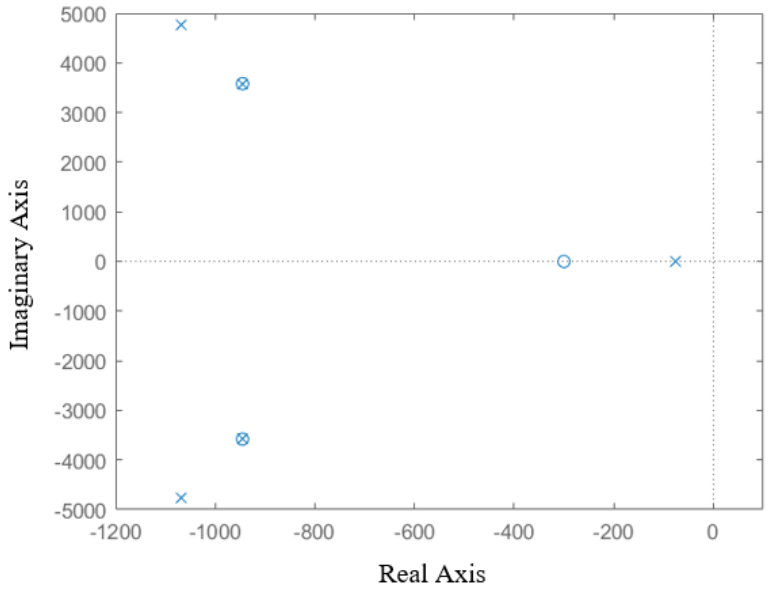


Figure 4.10: Pole-zero plot of closed-loop VSI boost converter control system

As mentioned in Section 2.4, the bandwidth of the ac-side control must be significantly different than the dc-side control in order to limit the interaction between the two control systems and allow the for each control scheme to properly reach their steady-state values independently from the other side [17], [19]. Additionally, it must be confirmed that the ac side control is stable. In order to analyze the bandwidth of the droop control scheme, the small signal models of each control loop, which were derived in (3-15) and (3-16), can be used. In order to ensure that there are no unstable poles of the system, the characteristic equation from (3-11) can be used. Seen in Table 4.9 are the output filter parameters for both the qZSI and VSI systems. The bode plot of the output filter transfer function derived in (3-14) is shown in Figure 4.11. Seen in Table 4.10 are the control parameters for the droop control scheme in the single inverter models. Seen in Table 4.11 are the droop control parameters for the parallel inverter models. Note that these parameters are equal for both the qZSI and VSI systems. For the parallel inverter simulations, the nominal load

voltage was changed to 200 V_{rms}, instead of the 230 V_{rms} that is used in the single inverter runs in order to prevent saturation in the power control loop with such large real power fluctuations.

Table 4.9: Output filter paramters

Parameter	Value
r_f (Ω)	0.3
L_f (mH)	0.55
C_f (μF)	20
ω_{cutoff} (rad/s)	9535
f_{cutoff} (Hz)	1518

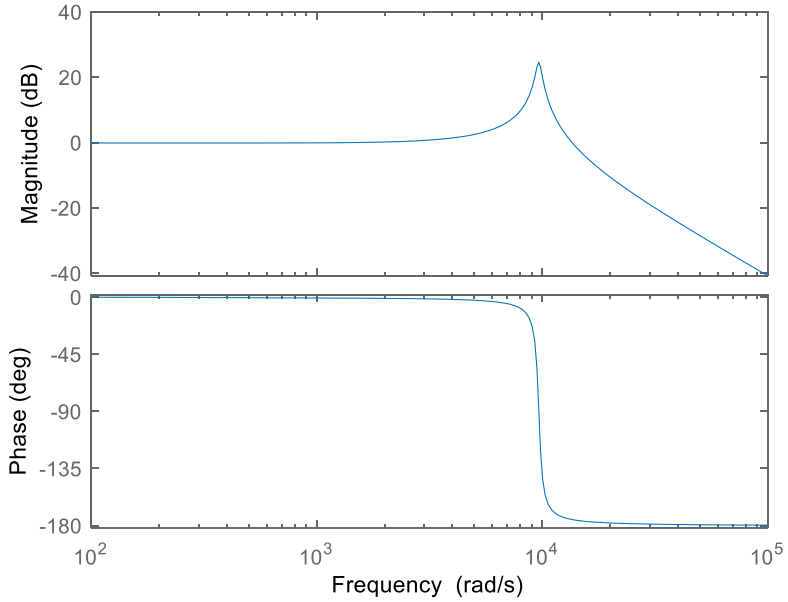


Figure 4.11: Bode plot of output filter

Table 4.10: Droop control paramters for single inverter models

Parameter	Value
p_{vdrop}	0.25 %
p_{fboost}	0.10 %
n	0.0012
m	$2.5133*10^{-5}$
K_e	10

Table 4.11: Droop control paramters for parallel inverter models

Parameter	Value
p_{vdrop}	0.25 %
p_{fboost}	0.10 %
n_1	0.00033
n_2	0.00050
n_3	0.00100
m_1	$7.5398*10^{-5}$
m_2	$3.7699*10^{-5}$
m_3	$2.5133*10^{-5}$
K_e	10

Typically, the bandwidth of droop control schemes are relatively low when compared to the other controllers in the system [25]. Logically, this makes sense as the droop control scheme is essentially a reference generator for the output voltage – these should be resistant to high frequency disturbances that may create a noisy, or oscillating reference. Thus, the goal of this analysis is to demonstrate that the bandwidth of the real and reactive power loops is significantly

smaller than the bandwidth of the dc-side control schemes. Seen in Table 4.12 are the average stability margins and bandwidths of the reactive power and real power control loops for both the single and parallel inverter models. The phase and gain margins for both control loops indicate more than adequate stability margins. When comparing the bandwidths to the dc-side control bandwidths in Table 4.7 and Table 4.8, the bandwidths of the ac-side control are sufficiently less than the bandwidths of the dc-side control. The droop control bandwidths for the single inverter model are less than the dc-side bandwidths by more than a factor of 10 on average. The droop control bandwidths for the parallel inverter model are less than the dc-side bandwidths by more than a factor of 5 on average, due to the smaller bandwidth of the dc-side control for the parallel inverter models. Figure 4.12 through Figure 4.15 show the open-loop and closed-loop bode plots for the real and reactive power loop for the single inverter model, respectively. Note how both control schemes show a steady state frequency and output RMS voltage that is very close to the nominal values, indicating good regulation capabilities.

Table 4.12: Stability margins and bandwidth for droop control scheme

Control Loop	Parameter	Single Inverter Model	Parallel Inverter Model
Reactive Power Loop (ω/ω*)	PM (deg.)	85.9	88.03
	GM (dB)	∞	∞
	CL Bandwidth (rad/s)	9.75	4.51
	CL Bandwidth (Hz)	1.55	0.72
Real Power Loop (Vo/E*)	PM (deg.)	93.4	91.42
	GM (dB)	35.4	42.43
	CL Bandwidth (rad/s)	10.4	9.56
	CL Bandwidth (Hz)	1.66	1.52

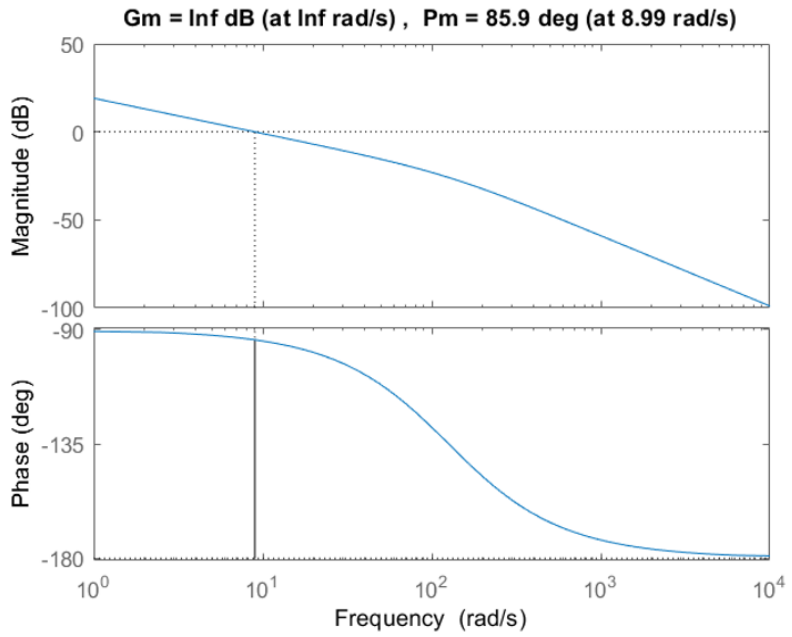


Figure 4.12: Open-loop bode plot of reactive power control loop

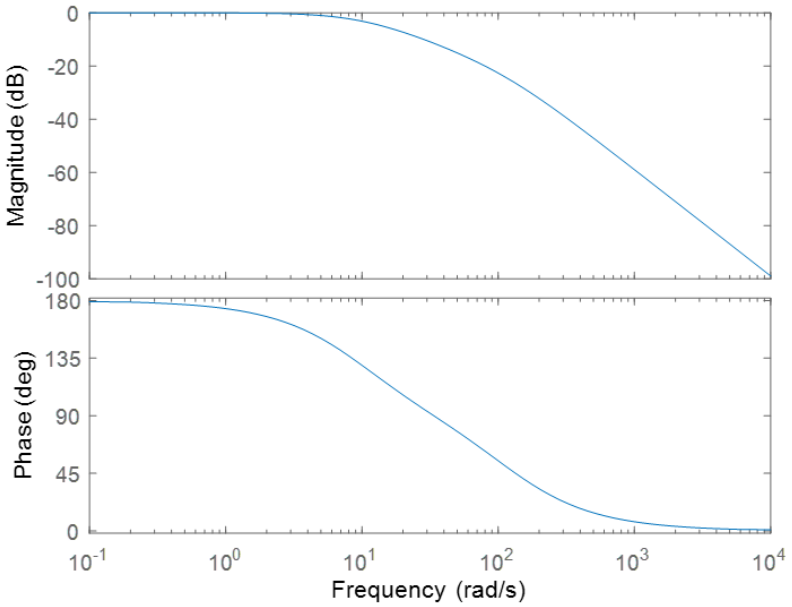


Figure 4.13: Closed-loop bode plot of reactive power control loop

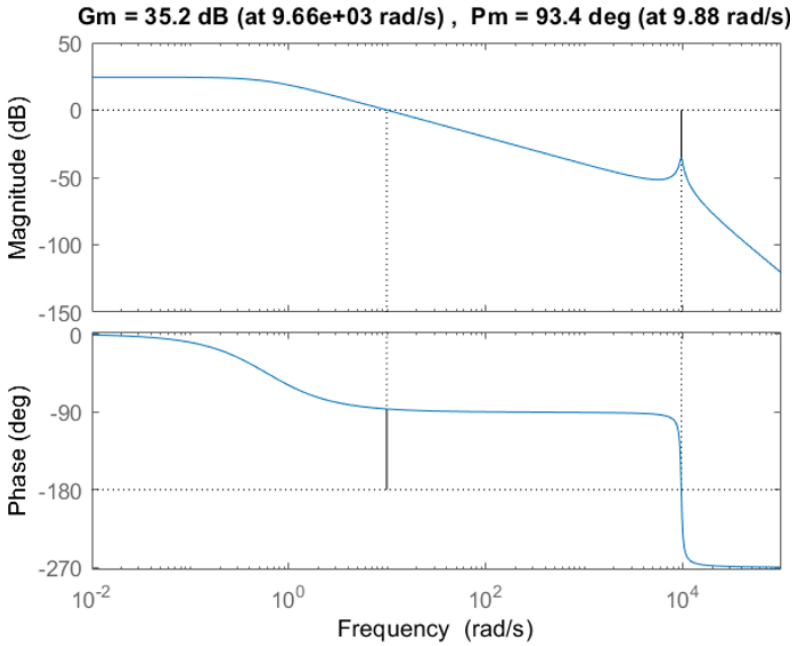


Figure 4.14: Open-loop bode plot of real power control loop

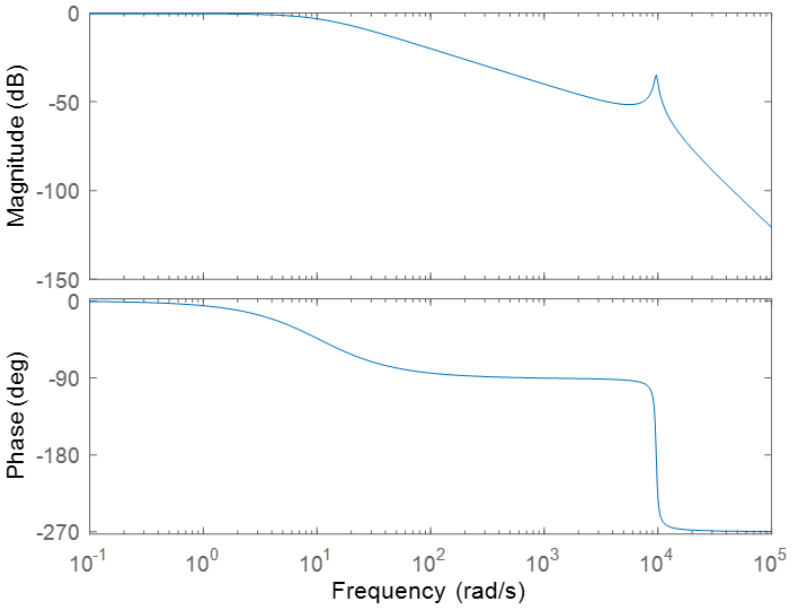


Figure 4.15: Closed-loop bode plot of real power control loop

In order to ensure that there are no RHP poles present in the system, the zeros of the characteristic equation, derived in (3-11), can be calculated. For each simulation scenario, there are no RHP poles present in the droop control scheme. Seen in Figure 4.16 is a plot of the zeros of the characteristic equation for the single inverter models.

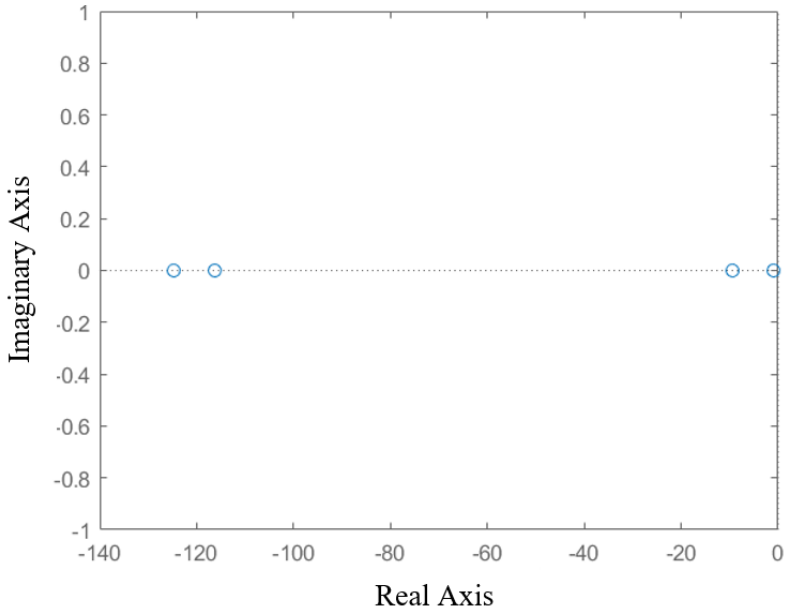


Figure 4.16: Zeros of characteristic equation of droop control scheme

4.3 Simulation Results

After ensuring that the control system is designed to be stable and have proper bandwidths, the scenarios outlined in Table 4.1 and Table 4.2 were simulated in PLECS. There are a total of four models, one single inverter model of the qZSI, one single inverter model of the boost-cascaded VSI, one parallel inverter model of the qZSI, and one parallel inverter model of the boost-cascaded VSI.

4.3.1 Step Changes in Load and DC Input Voltage

As outlined in Table 4.1, two simulations were run for the single inverter models – a step change in load and a step change in input voltage. All of the impedance and control parameters were outlined in the previous sections. Seen in Table 4.13 are the reference parameters for each system. Figure 4.17 through Figure 4.22 show the response of key qZSI and VSI parameters for a 100% step change in load from 6.9 kW and 2.6 kvar to 13.8 kW and 5.2 kvar. At 1 second, when the load was doubled, both systems responded quickly and settled to the new steady state operating state with minimal oscillation or overshoot. In Figure 4.17 and Figure 4.18, it can be seen that the VSI system responded slightly faster than the qZSI, however both responses were overall very similar in terms of rise time and settling time. As exhibited in Figure 4.19 and Figure 4.20, the qZSI regulated voltage and frequency just as well as the VSI system, supporting the conclusion that the qZSI will function well in a grid-forming role. In Figure 4.21, there is minimal impact on the quality of the output voltage for a 100% step change in load, with the qZSI system actually dampening the disturbance slightly better than the VSI system. The better dampening performance is further exhibited in Figure 4.22, where the qZSI dc-link voltage fluctuates by less than 50 V, while the VSI dc-link voltage drops by approximately 75 V before recovering.

Table 4.13: Reference paramters for single inverter models

Parameter	qZSI	VSI System
V_{in}	550 V	
V_{pn} / V_{dc}	1000 V	700 V
ω*	2π60	
E*	230 V_{LN}	
D_{max}	0.3	0.9
M_{max}	0.7	1

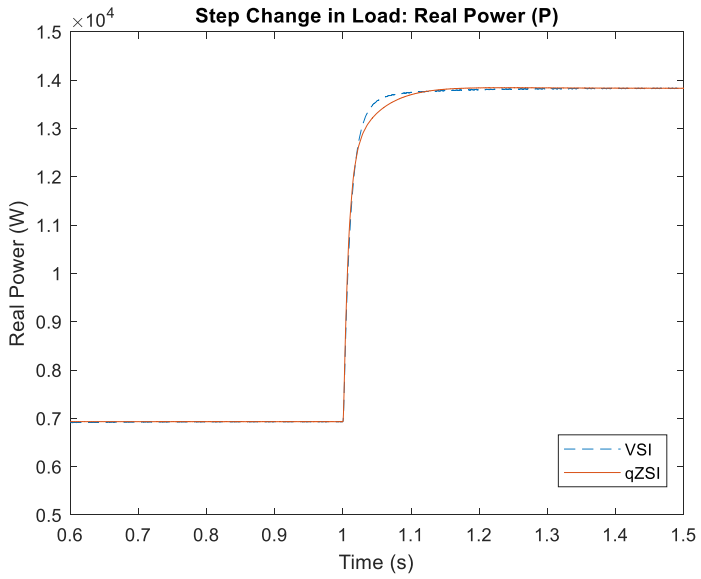


Figure 4.17: Step change in load result, real power

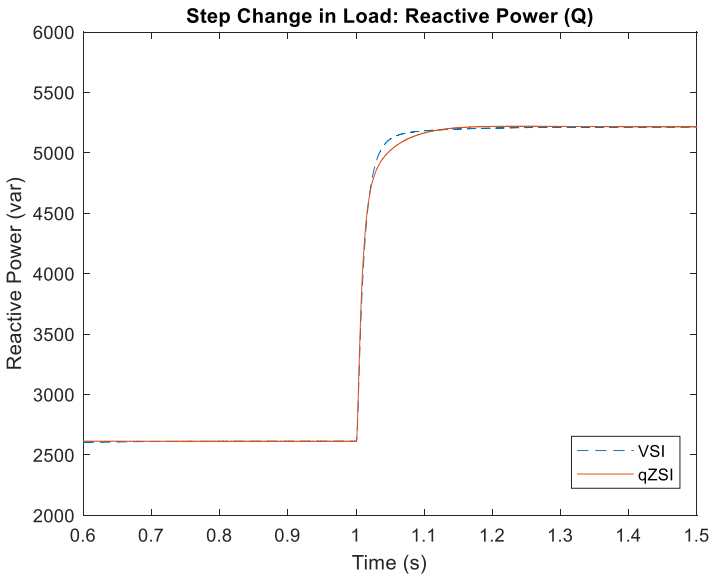


Figure 4.18: Step change in load, reactive power

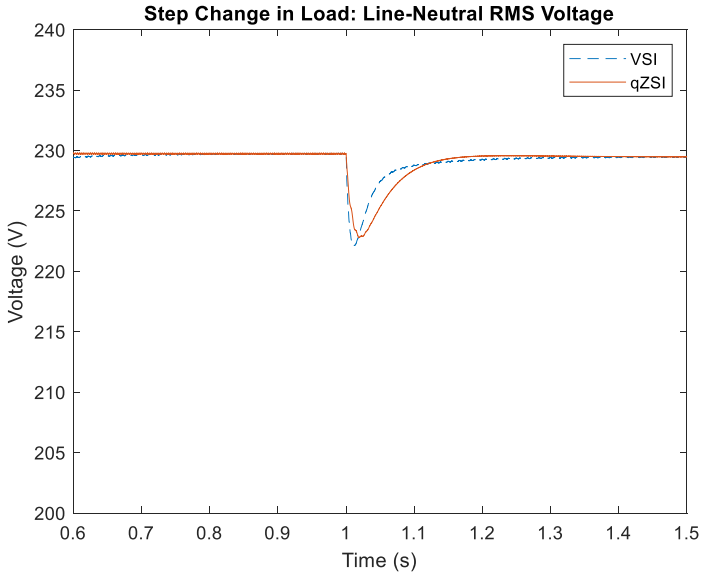


Figure 4.19: Step change in load, L-N RMS voltage

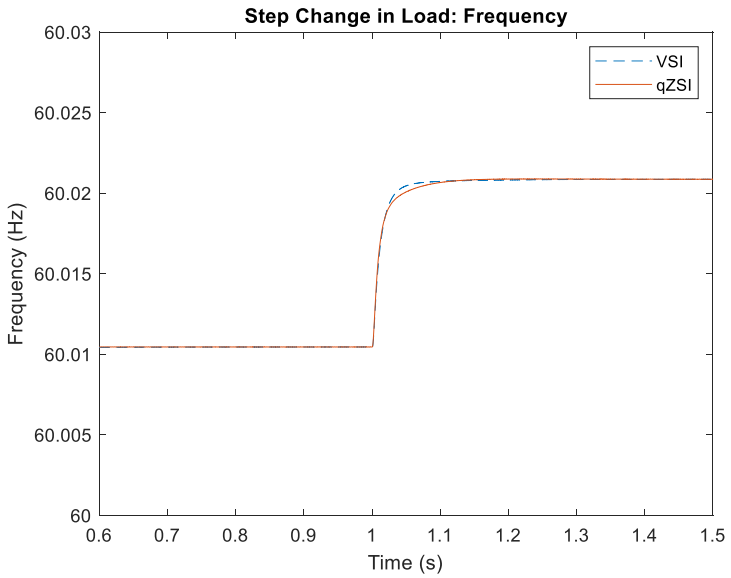


Figure 4.20: Step change in load, line frequency

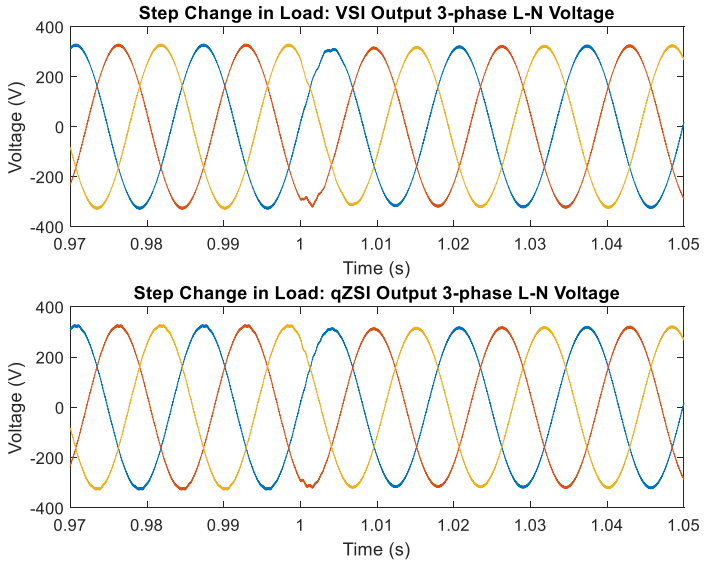


Figure 4.21: Step change in load, (top) VSI L-N voltage, (bottom) qZSI L-N voltage

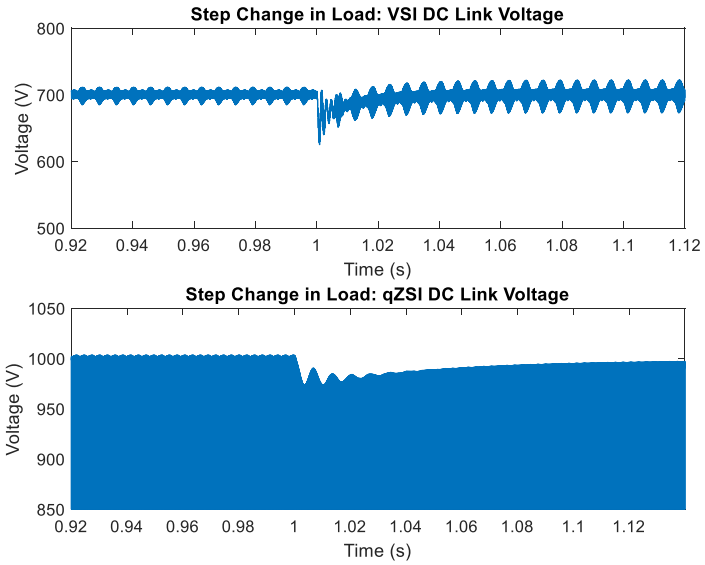


Figure 4.22: Step change in load, (top) VSI dc-link voltage, (bottom) qZSI dc-link voltage

Figure 4.23 through Figure 4.28 show the results for a 20% step change in input voltage from 550 V down to 440 V. As can be seen, there are fluctuations of a few hundred watts and vars immediately after the step change, however the qZSI recovers as quickly as the VSI system and exhibits similar damping. The response of the powers is mirrored by the responses of the L-N RMS output voltage and line frequency, both of which are regulated to the same steady-state value after the transients settle. Comparing the output waveforms and dc-link voltages, the qZSI demonstrates slightly better performance in terms of minimizing the disturbance on the output, and significantly better performance in regulating its dc-link voltage. The dc-link voltage of the VSI system drops by nearly 175 V, while the dc-link voltage of the qZSI drops by just 68 V. While both systems respond quickly, minimizing the impact on the output voltage, the qZSI system exhibits much better damping after the initial step change.

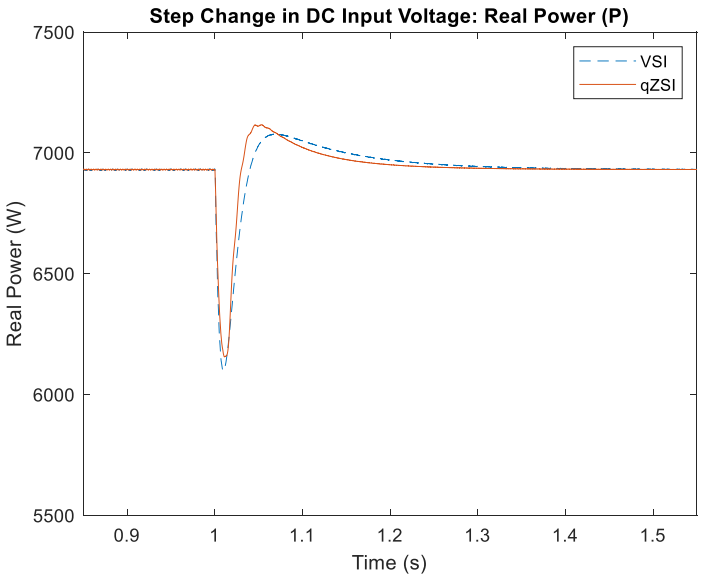


Figure 4.23: Step change in Vin, real power

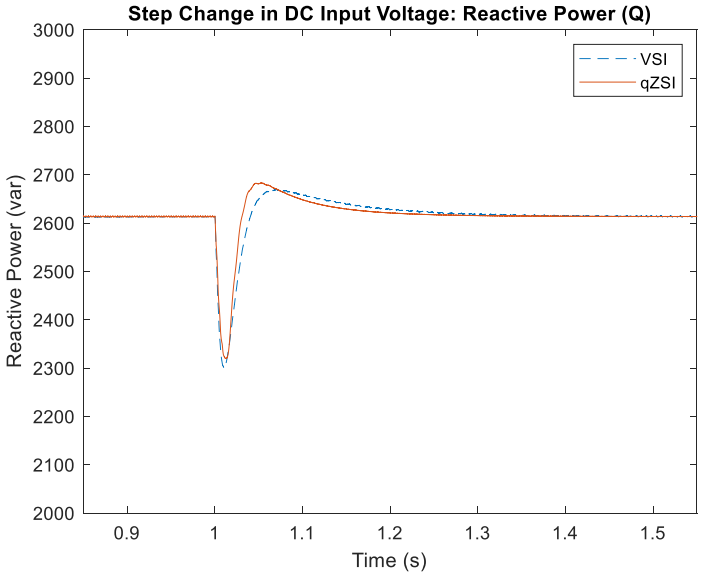


Figure 4.24: Step change in Vin, reactive power

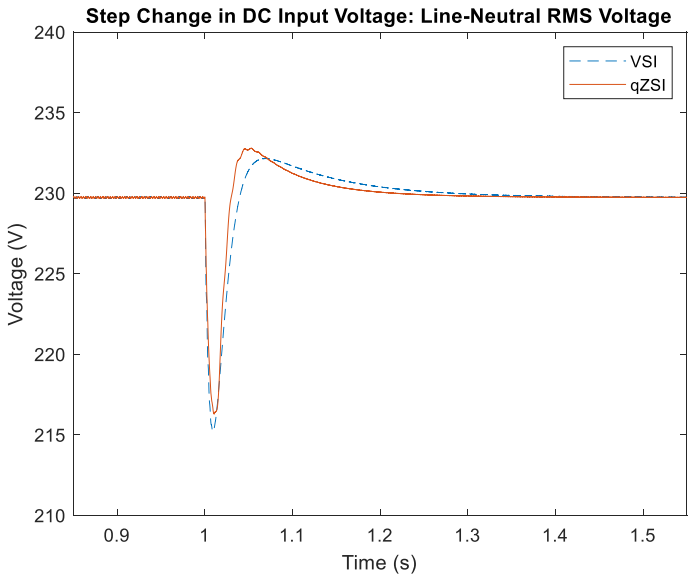


Figure 4.25: Step change in Vin, L-N RMS voltage

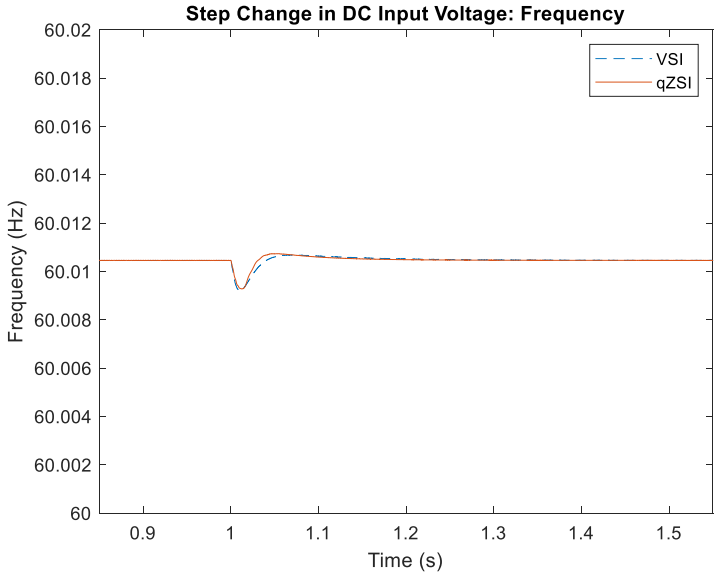


Figure 4.26: Step change in Vin, line frequency

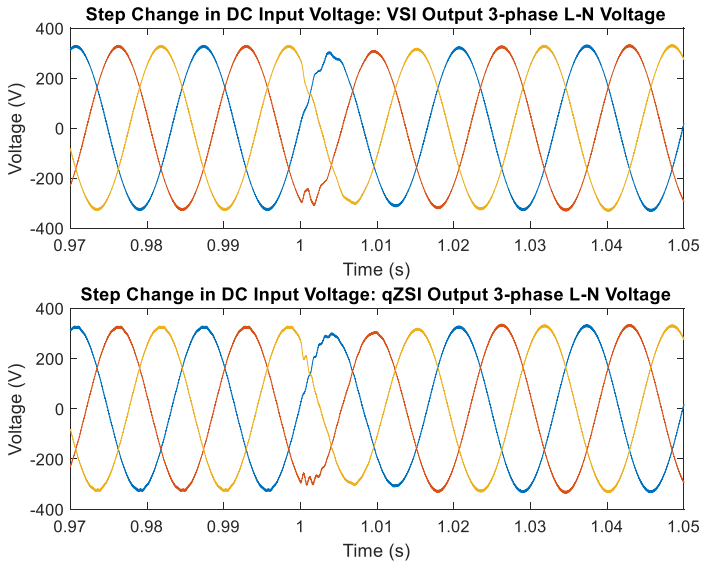


Figure 4.27: Step change in Vin, (top) VSI L-N voltage, (bottom) qZSI L-N voltage

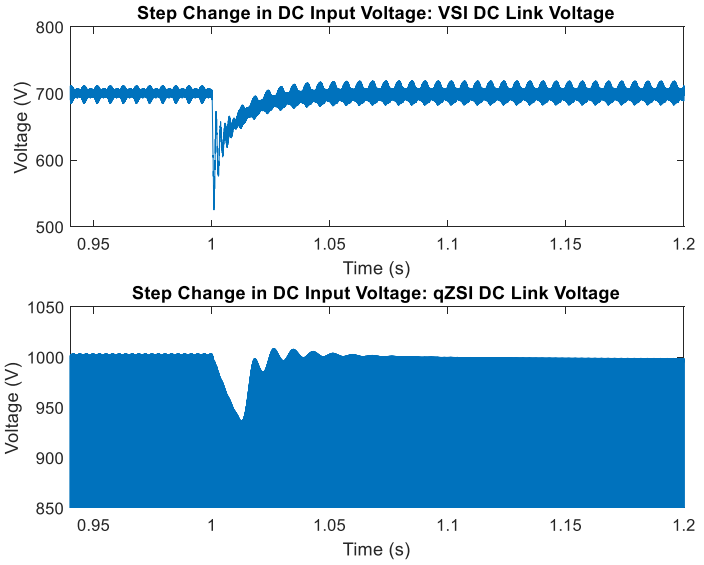


Figure 4.28: Step change in Vin, (top) VSI dc-link voltage, (bottom) qZSI dc-link voltage

4.3.2 Parallel Load Sharing

As outlined in Table 4.2, the parallel inverter models consist of a 42 kW / 16 kvar load. The first inverter, rated for 45 kVA, will be initially powering the load, with inverters 2 and 3 disconnected. At 4 seconds, inverter 2 (30 kVA) is connected to the load and inverters 1 and 2 begin feeding the load in parallel. At 10 seconds, inverter 3 (15 kVA) is connected to the load, at which point all three inverters are feeding the load in parallel. As explained in Section 3.2.1, each inverter should share the load in proportion to their rated powers. The expected steady-state real and reactive powers being fed to the load can be calculated by the following expressions:

$$t < 4\ s \begin{cases} S_1 = S_{load} \\ S_2 = 0 \\ S_3 = 0 \end{cases}$$

$$4\ s < t < 10\ s \begin{cases} S_1 = 1.5S_2 = \left(\frac{1.5}{2.5}\right) S_{load} \\ S_2 = \left(\frac{1}{2.5}\right) S_{load} \\ S_3 = 0 \end{cases}$$

$$10\ s < t \begin{cases} S_1 = 1.5S_2 = \left(\frac{3}{6}\right) S_{load} \\ S_2 = 2S_3 = \left(\frac{2}{6}\right) S_{load} \\ S_3 = \left(\frac{1}{6}\right) S_{load} \end{cases}$$

Seen in Table 4.14 are the reference parameters for each system. Note that the maximum duty cycle and modulation index limits, as well as the rated load voltage are slightly different for the parallel inverter model. These changes were made to prevent saturation in the control scheme, but for future work, the saturation limits of the control scheme or load can be better designed to prevent such changes from being necessary.

Table 4.14: Reference paramters for parallel inverter models

Parameter	qZSI	VSI System
V_{in}	550 V	
V_{pn} / V_{dc}	1000 V	700 V
ω*	2π60	
E*	200 V_{LN}	
D_{max}	0.26	0.9
M_{max}	0.74	1

Seen in Figure 4.29 and Figure 4.30 are the respective VSI and qZSI real and reactive powers for each inverter. Shown in Table 4.15 are the steady-state real and reactive powers for each run, compared to the expected steady state powers.

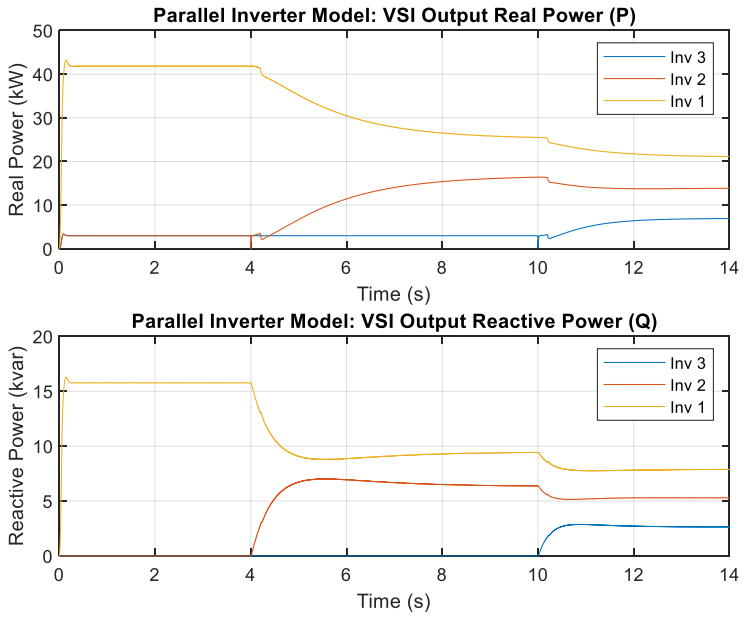


Figure 4.29: VSI power sharing, (top) real power, (bottom) reactive power

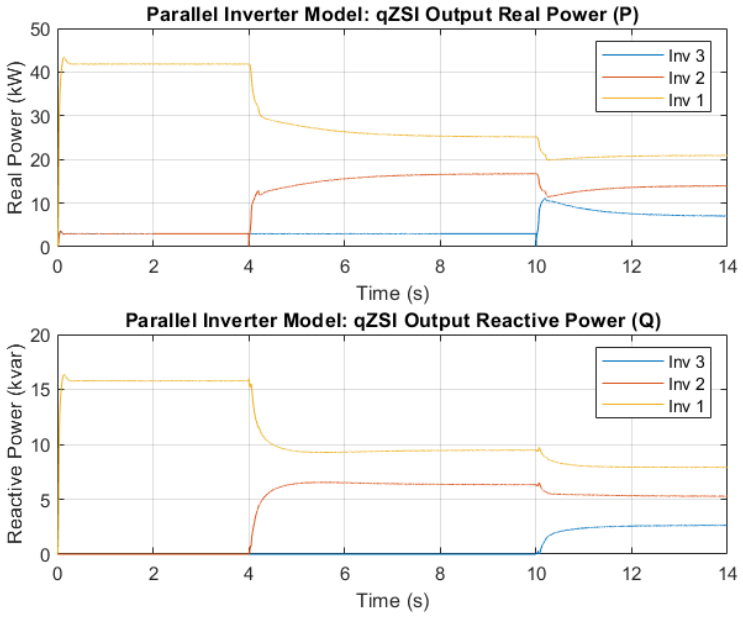


Figure 4.30: qZSI power sharing, (top) real power, (bottom) reactive power

Table 4.15: Steady-state real and reactive powers for parallel inverter models

Time Range	Inverter Number	Expected Powers	qZSI Powers	VSI Powers
0 < t < 4	1	42 kW 16 kvar	41.8 kW 15.8 kvar	41.8 kW 15.8 kvar
	2	0 kW 0 kvar	0 kW 0 kvar	0 kW 0 kvar
	3	0 kW 0 kvar	0 kW 0 kvar	0 kW 0 kvar
4 < t < 10	1	25 kW 9.6 kvar	25.2 kW 9.5 kvar	25.5 kW 9.4 kvar
	2	16.8 kW 6.4 kvar	16.7 kW 6.3 kvar	16.4 kW 6.4 kvar
	3	0 kW 0 kvar	0 kW 0 kvar	0 kW 0 kvar
10 < t	1	21 kW 8 kvar	20.9 kW 7.9 kvar	21.1 kW 7.9 kvar
	2	14 kW 5.3 kvar	13.9 kW 5.3 kvar	13.9 kW 5.3 kvar
	3	7 kW 2.7 kvar	7.1 kW 2.6 kvar	6.9 kW 2.6 kvar

The non-zero real powers seen in inverters 2 and 3 before they are connected to the main load are simply the start-up load that is used because neither the qZSI nor boost-converter can operate unloaded. For this work, inverters 2 and 3 were connected to their start-up loads at t=0 seconds, however in practice they could be connected just a couple seconds before being connected to the main load, to allow for the self-synchronization scheme to reach steady-state. Once the inverter is synchronized with the grid, it can be connected to the load. Note that to prevent any unloaded behavior, the start-up load remains connected to the inverter for 0.2 seconds before being disconnected. The disconnection of the start-up load can be seen in the slight notch in the real powers of each inverter after they are connected to the main load. The start-up procedure for each inverter can be summarized as follows:

1. The first inverter (inverter 1) to feed the load can be directly connected to the load upon start-up
2. The next inverter (inverter 2) to be connected to the main load must first be powered on while only connected to its respective start-up load
3. With both inverters in steady-state inverter 2 should then be set to self-synchronization mode
4. After inverter 2 reaches steady-state, it is synchronized with the output voltage of inverter 1 and can now be connected to the main load
5. Upon connecting inverter 2 to the main load, the start-up load remains connected for a small period of time before being disconnected
6. Repeat steps 2 through 5 for connecting additional inverters in parallel

As can be seen from Figure 4.29 and Figure 4.30, the qZSI and VSI systems reach the expected steady-state real and reactive powers for each inverter at each stage of operation. Unexpectedly, however, there are significant differences in their dynamic responses. The VSI system exhibits a very slow rise time in the real powers of each inverter, while it exhibits some overshoot in the reactive powers. The qZSI system exhibits very quick responses in both the real and reactive powers, showing slight overshoot in the real powers but no overshoot in the reactive powers. This result different from the single inverter model results shown in Section 4.3.1, where both the qZSI and VSI had very similar rise times for real and reactive power. An important detail is that the rise times for the qZSI and VSI parallel models are very similar when all of the inverters are operating independent from one another. The differences become apparent once the inverters begin feeding the same load in parallel.

Because it is extremely difficult to derive mathematical models of parallel inverter systems, it is hard to conclude why the two systems have such drastically different dynamic responses. One explanation could be that parallel operation caused a shift in the poles of each system, resulting in faster or slower responses depending on the location of the shifted poles. This assumption is very difficult to demonstrate analytically, however, as the inverter model in Figure 4.3 would likely require more than ten differential equations to accurately model the system dynamics [29]–[31]. While more simple techniques for analyzing parallel inverter systems were proposed that only use the inverter output impedances and load, these methods only provide insight on the system stability rather than the system dynamics [32]–[35]. Given the complexity of analyzing the dynamics of parallel inverter systems, such an analysis was not performed for this work. In order to analytically demonstrate why the parallel qZSI and VSI systems are performing differently in terms of their dynamics, such an analysis will likely be needed in the future.

5.0 Conclusions

The goal of this work was to design and implement a control scheme for a 3-phase qZSI in order to enable it to operate in a grid-forming role. The qZSI was analyzed in great detail and compared to a conventional boost converter that is commonly used in grid connected inverters. Literature was presented to demonstrate the need for current programed mode control for the dc side of the qZSI, and the control scheme was compared to a common control scheme used for boost converters. Then, recent literature was used to support why the universal droop control scheme was chosen for the ac-side control for this work. After contextualizing the design of the overall qZSI control scheme, the final control scheme was presented. An analytical approach was taken for design of the components and gain parameters. The goal was to design a qZSI system with similar properties to a conventional boost-cascaded VSI system. Thus, the performance of the qZSI system in a grid-forming role could be benchmarked against a conventional device, demonstrating whether the qZSI could operate as a fundamental grid-forming device.

Through PLECS simulations, the qZSI system presented in this work not only demonstrated its ability to operate in a grid-forming role, but also that it may potentially have superior performance to conventional VSI systems operating in the same role. While a much more optimized design approach is needed for both the qZSI and VSI to truly compare the two systems, this work demonstrated that the qZSI is more than capable of operating in a grid-forming role. It handled large step changes in load and input voltage with quick rise times and good damping, and exhibited quick and stable responses when operating in parallel with other inverters. Future work on this topic should focus on developing a detailed dynamic model of the qZSI and VSI parallel

inverter systems, with the goal of analytically explaining the dynamic performance differences between the two systems.

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