Gallium-Nitride Efficacy for High-Reliability Forward Converters in Spacecraft

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Gallium Nitride (GaN) devices show particular promise for space-rated power conversion applications that rely on MOSFET technology whose performance is severely limited by the radiation hardening processes. Though GaN failure mode classification and radiation hardened device variety is limited, the current space-rated selection pool can still yield significant efficiency and power density improvements. However, the context of GaN research is often future oriented such that the application of GaN to common, proven, space-rated converter designs are rare.

The presented work quantifies the performance benefits of market available, space-rated GaN HEMTs over radiation hardened MOSFETs for a synchronous forward converter, which remains an extremely popular topology for isolated, medium power, DC-DC conversion on NASA satellite systems. Two 75-Watt, space-rated forward converters were designed, implemented, and benchmarked, with the power switch technology being the single variable of change. By forming pareto-optimal fronts of the key device metrics, optimal Rad-hard MOSFETs were chosen so that the baseline converter performance was considered best-case.

The frequency limitations of common, available, Rad-hard PWM controllers limited power density in the GaN and Si converters alike, however, efficiency gains proved sizeable. The GaN based converter saw a peak efficiency of 86%, which was a 4.54% improvement over the Si baseline. Detailed efficiency and loss differential plots are presented which show the GaN converter's reduced sensitivity to input voltage. Extreme similarity between the waveforms and functional characteristics of the two converters verified the design of the experiment. Furthermore,

the performance of the baseline Si converter proved very similar to that of a large sampling of space-rated forward converters, making the experimental results have a high degree of utility for manufacturers.

Table of Contents

Preface xi

1.0 Introduction 1

2.0 Design of Experiment 4

3.0 Converter Design 6

3.1 Topology Selection & Specification Justification 6

3.2 Subsystem Design and Component Selection 9

3.2.1 Transformer Design 11

3.2.2 Output Filter Design and Capacitor Dielectric Selection 13

3.2.3 Control Loop Design 14

3.2.4 Isolation Barrier Communication 15

3.2.5 Dead Time Generator 15

3.2.6 Startup-Circuit & Linear Regulator 16

3.2.7 Snubber Network Design & Power Diode Considerations 17

3.2.8 Gate Driver for Si Based Board 19

3.2.9 Omitted Converter Features 19

3.3 Simulation & Design Verification 20

4.0 FET Selection 25

4.1 Si Baseline FET Selection Methodology 25

4.2 FET Loss Calculations used in Selection Process 31

4.2.1 Thermal Considerations 31

4.2.2 Loss Operating Point 32

4.2.3 Conduction Losses..33

4.2.4 Dynamic Losses 33

4.3 Evaluation of Radiation Hardened Optimal Candidates for Q1 35

4.4 Error Bounding the Radiation Hardened Match Selection..................................... 39

4.5 COTS Matching Verification 39

4.6 GaN Device Selection 43

5.0 Results 45

6.0 Discussion... 53

Appendix A Full Schematic References 55

Bibliography 60

List of Tables

Table 1 Forward Converter Design Specifications 7

Table 2 Key Components List.. 11

Table 3 Q1 Losses for Rad-Hard Candidates at Vin=28V, Iout = 3A.................................... 36

Table 4 FET Configurations for Si Forward Converter 40

Table 5 FET Selection Comparison Rad-Hard, COTS, Bounding, eGaN............................. 40

Table 6 Basic Converter Characteristic Comparison.. 50

Table 7 FET/Driver Package Comparison 54

List of Figures

Figure 1 Peak Efficiency of Sampled Forward Converters 4

Figure 2 Synchronous Forward Converter Topology 7

Figure 3 Forward Converter Block Diagram.. 10

Figure 4 Rayco Transformer 12

Figure 5 Slow Start Implementation 14

Figure 6 Adjustable Dead Time Generator 16

Figure 7 Implemented Snubber Networks 18

Figure 8 LTSpice Average Model 21

Figure 9 LTSpice Transient Model 22

Figure 10 Loop Gain/Phase Monte-Carlo Simulation 23

Figure 11 Loop Gain/Phase Analytical Evaluation 23

Figure 12 Transient Simulation Waveform: Output Ripple at Iout = 5A 24

Figure 13 Transient Simulation Waveform: Secondary Switch Node 24

Figure 14 Transient Simulation Waveforms: Startup Signals 24

Figure 15 Total Gate Charge Vs RdsON of IR Rad Hard & COTS FETs Log Scale 26

Figure 16 Output Capacitance Vs RdsON of IR Rad Hard FETs, ... 27

Figure 17 Total Gate Charge Vs RdsON of IR Rad Hard & COTS FETs Linear Scale 29

Figure 18 Qgtotal Vs RdsON of IR Rad Hard FETs Breakdown Voltage Comparison...... 31

Figure 19 Q1 Switch Loss vs Converter Output Current 37

Figure 20 Q1 Switch Loss vs Converter Input Voltage 38

Figure 21 Combined Switch Loss Vs Output Current Comparison 41

Figure 22 Combinaed Switch Loss Vs Input Voltage Comparison....................................... 42

Figure 23 Q1 Switch Loss eGaN Vs Converter Output Current... 44

Figure 24 GaN Based Forward Converter Hardware... 45

Figure 25 Efficiency Plots from the Implemented Converters 46

Figure 26 Loss Differential Between Si Converter (Config. 1) and GaN Converter 47

Figure 27 Switch Node Scope Capture Waveforms.. 51

Figure 28 Transient Response Scope Capture Waveforms... 52

Figure 29 GaN Converter Detailed Schematic Page 1... 56

Figure 30 GaN Converter Detailed Schematic Page 2... 57

Figure 31 Si Converter Detailed Schematic Page 1 58

Figure 32 Si Converter Detailed Schematic Page 2 59

Preface

Thank you to Dr. Brandon Grainger, and Dr. Alan George for advising me during this project and giving the flexibility and encouragement to fully pursue my interests. An additional thank you to Thomas Cook, and all the other graduate students in the NSF Center for Space, High-performance, and Resilient Computing (SHREC).

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A final thank you to my family and friends, without which, I would not have made it this far.

1.0 Introduction

The emerging roll of Gallium Nitride based FETs in power conversion, as seen by the surge in commercially available devices and academic research, is unmistakable. When compared to the highly matured and performance bound Silicon devices, GaN achieves faster slew rates, lower on-resistance, and smaller die sizes [1]. These metrics directly translate to the most critical high-level goals of a power system, namely, efficiency and power density.

Although the benefits of GaN are so fundamental that most power applications could be impacted, space-rated systems are of particular interest for two primary reasons: One, the techniques used to attain radiation hardness for Silicon power switches greatly reduce performance such that space-rated MOSFETs lag commercial devices by nearly an order of magnitude in key metrics like on-resistance and total gate charge. As a result, space-rated power systems are often performance constrained by power switches. Two, GaN's wide band-gap structure has shown inherent efficacy against total ionizing dose (TID) radiation [2][3]. It's conceivable that the performance gap between commercial and future space-rated GaN devices will vastly outperform that of Si. However, even if it doesn't, the step change in GaN switch performance to begin with could lead to a significant increase in power processing capability for space-rated designs.

For all its promise, GaN FET's are still in their infancy, especially within the context of space qualification. Failure mode discovery, classification, and causation is on-going. Where GaN excels in TID radiation, it may be particularly sensitive to Single Event Effects (SEE) [4][2]. Furthermore, GaN FET's have a radically different operating principle and physical structure than MOSFETs. They take advantage of mechanical stresses that induce a piezo electric effect, which then forms a two-dimensional electron gas layer. It's this gas that yields high electron mobility

[1]. It will likely take time for the radiation hardening test methodology to fully adjust to the needs of GaN [2]. That said, research and development efforts by NASA NEPP, ESA, academic research groups, and a select lot of private companies (Freebird, EPC, Renesas, SSDI, Teledyne-e2v) [2] have resulted in promising insights, and a small lot of space-rated low voltage GaN devices.

Of interest is quantifying the utility of market available, space-rated GaN devices for common DC-DC power processing space scenarios. Specifically, how much more performance can GaN give us in pervasive applications if the components used meet radiation hardened standards? Isolated converters that regulate bus voltages for NASA satellite systems are targeted due to their prevalence and medium power requirements, which give the GaN devices a more demanding, but rewarding opportunity over low power, point of load converters. When three of the major radiation hardened switch mode power supply (SMPS) manufactures (Infineon, VPT, Microsemi) were polled for their available isolated converter solutions (TID>100kRads Si, See > 80 MeV-cm2/mg), thirty out of the thirty-nine results used forward converter topologies. The non-pulsating output current and long-withstanding design make it apt for a medium power, high reliability, space-rated supply.

The experimental work in GaN space power conversion is often looking to the future, when radiation hardened control devices can leverage high frequencies, failure mechanisms are further defined, and novel, high efficiency topologies have achieved flight heritage. Moreover, it is rare to find GaN research that is rigorously constrained by the space-rated specifications that drive the research questions in the first place [5][6][7][8][9]. The cases that do conform to the hardware constraints lack in-depth device comparison studies [10][11], for any improvements shown by GaN switches can be easily skewed by the baseline silicon MOSFET selection.

The novelty of this research lies in the practicality of the experimental builds and the corresponding accuracy of the results in both a relative (GaN vs Si) and absolute sense (Implemented Si based converter vs existing Si solutions). Two DC-DC space-rated forward converters were designed, implemented, and benchmarked. One utilizing GaN for power switching, and the other using traditional silicon based MOSFETs. Only available, radiation hardened devices were considered. By holding as many design variables constant as possible across the two converters, a focused and practical study was achieved, centered around the switch technology.

Since minor variations in losses can heavily effect converter efficiency and experiment conclusions, the device selection process was made rigorous by considering pareto-optimal fronts of the key metrics for radiation hardened MOSFETs. Although figure of merit plots that show the on resistance and total gate charge are common in textbook references for commercial devices [1], no equivalent plots to the authors' knowledge exist for their rad-hard counter parts. These are assembled and presented in this paper, and recommended for use whenever matching commercially available switches to rad-hard solutions for economical testing and experimentation. A methodology is proposed and implemented for bounding the error in component matching.

To provide context for this application-based comparison study, section two and three will discuss the design of the experiment and converter, respectively. Section four is devoted to the baseline Si optimal FET selection and commercial off-the-shelf (COTS) part matching process. Sections five and six detail the hardware/performance results and discuss the advantages and drawbacks of using market available GaN FETs for isolated power conversion.

2.0 Design of Experiment

To evaluate the current state of GaN in power processing spacecraft applications, baseline measurements are needed that represent the class of radiation-hardened Silicon MOSFETs.

Slight differences in topology, component selection, PCB layout, and general design processes can lead to a wide range of converter performances. Figure 1 shows a sampling of 19 forward converters from the Hi-Rel/Military, academic, and industry design spaces [6], [8], [10], [12]–[17], [17]–[22], [23, p. 38], [24]. The main takeaway is that efficiency as a representation of performance, has an extremely high degree of variability even within the same topology, and in this example, transformer core reset mechanism.

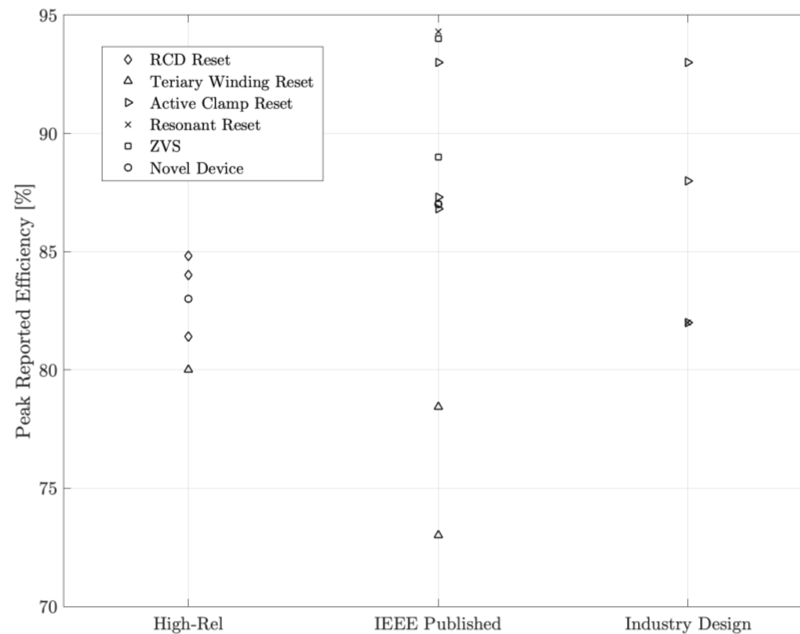


Figure 1 Peak Efficiency of Sampled Forward Converters from Academia and Industry

For this reason, building a single converter using GaN technology and comparing results to existing converters can be misleading.

A fair, head to head comparison requires two converters whose primary design change is the power switch. This philosophy could be taken to the extreme by designing boards that have a selective population scheme for the switch and driver, thereby matching features on a very detailed level. However, contorting the layout, especially the switch nodes, to be flexible in this way would hurt functionality of both designs, and degrade absolute accuracy of the results. While the converters should be matched in terms of components and theory of operation, there are still minor, non-overlapping optimizations that are needed to yield the best performance out of both designs.

The two converters will be first compared and tuned so that their basic functionality is similar. By reusing the same parts and overall design, aside from the power switches, this should require only slight changes to passives so that parameters like switching frequency, dead time, and snubber overshoot are matched. Afterwards, a comparison that details the difference in converter performance will occur. Analytical and experimental loss analysis will primarily focus on the power switches, as other loss modes should be normalized across the two boards. Lossy snubber networks effected by the switch are also of high interest.

For concision, the converter that uses silicon MOSFETs for power switching will be called the Si converter, and the one that uses gallium-nitride HEMTs will be called the GaN converter. The minor differences between the boards are discussed in the convert design section and Appendix A.

3.0 Converter Design

3.1 Topology Selection & Specification Justification

The specifications for the DC-DC converter used in this experiment follow from common requirements found in NASA satellite systems. Solar arrays and their corresponding battery banks provide a main 28V DC bus voltage for many satellites which then requires DC-DC conversion to power spacecraft computing, sensing, actuation, communication, and other critical loads. Isolated converter topologies prevent ground loops and add a layer of protection to the main bus. They are the first stage of conversion and often feed non-isolated point of load (PoL) converters. As stated in the introduction, the forward converter topology dominates market available radiation hardened isolated power supplies, making it a useful platform for this study. Additionally, the increase in GaN power device research in the context of low power PoL converters [25] makes the choice of an isolated, medium power topology more desirable.

Furthermore, since the experiment centers around the effect of an emerging transistor technology, there is no need for a novel or niche converter topology. Choosing a common, well understood topology follows the theme of practicality and generality in this research. That said, the chosen converter should reflect the degree of complexity that is being employed to capture valuable efficiency gains in modern aerospace converters. Also, the risks and lack of flight heritage that make zero voltage/current switching or resonant based converters a rare selection for high-reliability designs will eliminate them as candidates in this experiment.

With these considerations, a synchronously rectified, reset winding forward converter was selected, as shown in Figure 2. The forward converter was chosen over a flyback due to its market

dominance and non-pulsating secondary current, which is desirable for loss mitigation and EMI minimization when entering the medium power regime at low voltage. The synchronous rectification requires significant coordination strategies over the isolation barrier such that the desired complexity requirement is met. The use of a reset winding further separates the converter from a reliance on part parasitics, which aides in consistency and reliability.

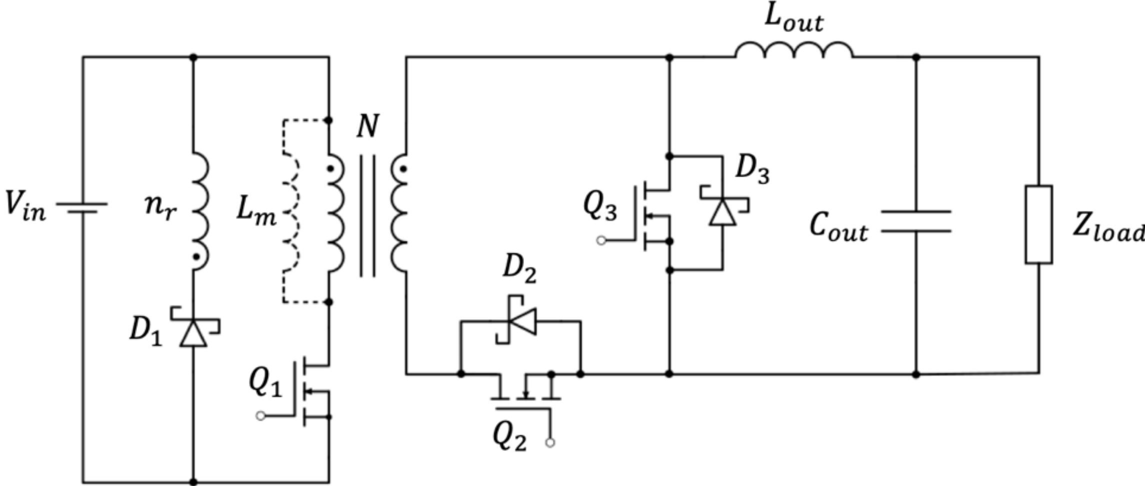


Figure 2 Synchronous Forward Converter Topology with Reset Winding

Table 1 Forward Converter Design Specifications

Parameter	Value
Output Voltage	12.0 ± 5% V
Input Voltage	22-36 V
Output Current	2-6 A
Max Power	72 W
Switching Frequency	300 kHz
TID	100 krad

Shown in Table 1 are the six primary design specifications. The input voltage range is standard for the mentioned 28V bus satellite systems. The maximum power specification was set to push the design into the medium power region.

Switching frequency selection is constrained by PWM controller, maximum duty cycle, and predicted GaN benefits. GaN technology promises an increase in power density without the loss in efficiency that comes with higher switching frequencies in hard switched applications. However, when using radiation hardened PWM controllers, the upper bound on switching frequency typically falls at the 500kHz point. Though there are exceptions for PWM controllers that fit isolated designs including ASIC or FPGA driven solutions, they do not represent the largest class of converters that have obtained flight heritage. Furthermore, the oscillator circuits that set switching frequency within a PWM controller often make a tradeoff for duty cycle. The current source that discharges the externally set RC network for the oscillator is fixed in magnitude such that as switching frequency increases, maximum duty cycle must decrease. For a forward converter, a reduction in maximum duty cycle can lead to an increase in the transformer turns ratio, and a subsequent increase on the peak voltages on the primary and secondary switches, which limits part selection and performance.

The choice of switching frequency is also constrained by the design of the experiment. If too low, then the strengths of GaN may not be seen. If too high, then the claim of a reasonable operating point for the board that uses traditional silicon MOSFETs will disappear due to excess switching losses. The chosen 300kHz specification meets the ability of the PWM controller, while giving the GaN device enough degrees of freedom and the Si MOSFETs a manageable operating point from a loss perspective.

The total ionizing dose specification can be seen as a restriction on all the converter components. This cumulative radiation metric contributes to the lifetime of the converter and is a tenant of space qualification.

3.2 Subsystem Design and Component Selection

Forward converter design methodology can be found in numerous industry application notes and textbook resources [26]. The equations and design decisions detailed in this section are meant to further classify the converter so that the discussion and application of the results have appropriate context. Of particular focus will be the converter features that constrain the three power switches, and the selections constrained by the radiation hardened requirements.

Note that worst-cast calculations, part ageing, and other deratings that effected component selection and converter design stem from NASA EEE-INST-002 specifications.

Shown in Figure 3 and Table 2 is the converter block diagram, and the key components list. Note that this study implements component matching techniques to reduce cost where radiation hardened parts were not donated or were cost prohibitive. That said, many of the final components used in the design were flight rated.

Reference Figures 29-32 for the detailed schematics of both the GaN and Si based forward converter in Appendix A.

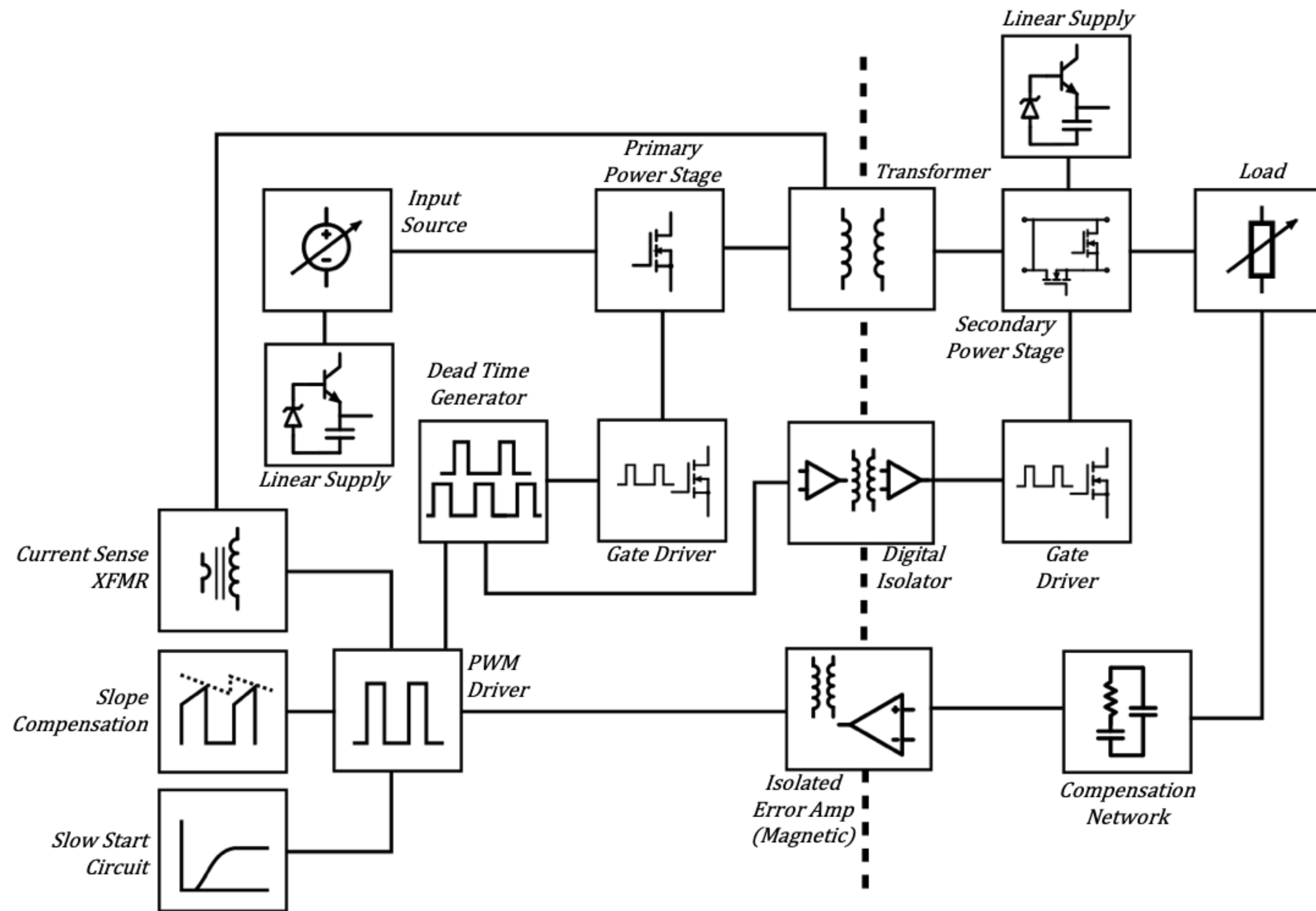


Figure 3 Forward Converter Block Diagram

Table 2 Key Components List

Description	Part Used	Rad-Hard Equivalent
Output Capacitor	AVXTPSD336*025#0100	-
Input Wet Slug Capacitors	T16D227K100EZSS	-
Transformer	5T9087	-
12 V Output Inductor	SRP2313AA-220M	SHILO0906-10R
Current-Mode PWM Controller	UC3845AD	UC1845A-SP
Isolated Error Amplifier	ADuM3190S	-
Digital Isolators	ADuM7442	-
Hex Schmidt Inverter	SN74HC14	SN54AC14-SP
Current Sense XFMR	CS106	-
GaN HEMT Module**	FBS-GAM01-P-C100	-
Power MOSFET Gate Driver*	ISL74422BRH	-
Power MOSFETs*	SQM60N20-35, IRFR24N15D, FDD86250	IRHMS57260SE, IRHNJ67134, NA
Power Schottky Diode	STPS3150U	16YQ150C

* = Exclusive to Si Board, ** = Exclusive to GaN Board, Dash in Rad-Hard Equivalent Categry means Rad-Hard part was used in converter builds

3.2.1 Transformer Design

The turns ratio from primary to secondary (N), and from primary to reset winding (N_r) is set early in the design process due to its effect on output ripple conditions, maximum drain-source voltage levels, and maximum duty cycle.

$$V_{Q1,ds\,max} = V_{in}(1 + N_r) \quad \textbf{3-1}$$

$$V_{Q2,Q3,ds\,max} = V_{in}N \quad \textbf{3-2}$$

$$D_{max} \le \frac{N_r}{2} \quad \textbf{3-3}$$

The majority of single radiation hardened MOSFETs have breakdown drain source voltages from 100V to 250V, which steers an additional constraint. By considering the maximum input voltage, voltage spikes due to leakage inductance, part safety margin, and available parts, the maximum values for N and N_r can be found. The minimum bound for N is derived so that regulation can occur at minimum input voltage with a conservative converter loss estimate. N was set to 2, and N_r to 1.

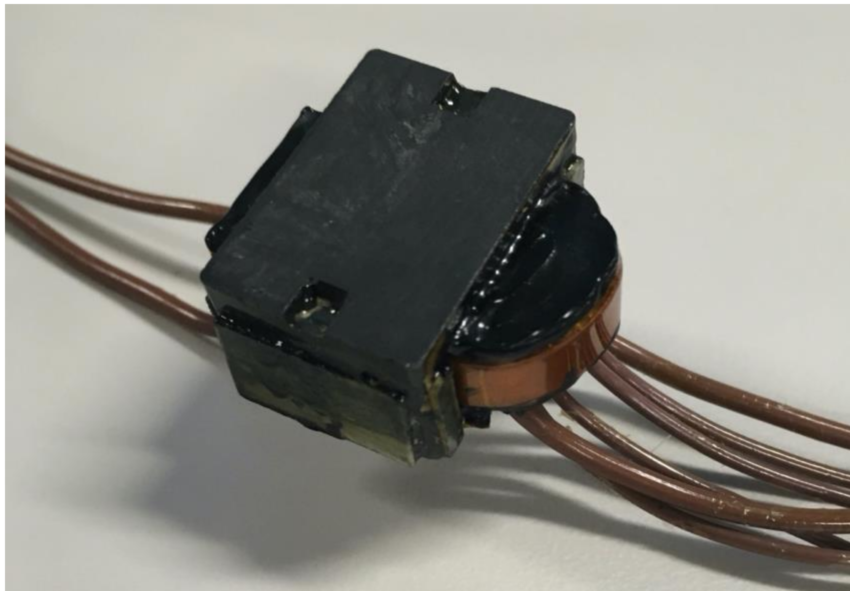


Figure 4 Rayco Transformer Used in Implemented Forward Converters

The transformer design was optimized for the converter specifications by Rayco, an external manufacturer that specializes in aerospace magnetics. The primary, secondary, and reset windings were composed of two, four, and two turns, respectively. An additional winding was included for use as an auxiliary supply if the linear supply scheme was altered in subsequent design stages. Although this winding was not used when the converter was implemented, it does pose a more realistic value for the leakage inductance, whose value increases due to the additional space

constraints. The leakage inductance was found to be 390 nH, and the self-resonant frequency on the primary winding was 2.28 MHz. The inductance seen from the primary was 17.56 uH, and the resistance per turn was roughly 8 $m\Omega$. The transformer was potted, as shown in Figure 4, to account for vibrational aerospace requirements.

3.2.2 Output Filter Design and Capacitor Dielectric Selection

An inductance minimum of $18.8uH$ was found to keep the converter operating in CCM at minimum load condition. A $22uH$ commercial inductor was used to match a space grade part, as seen in Table 2, with equivalent inductance, $\pm 10\%$ DCR, and $\pm 15\%$ rated current.

Eight $33uF$ output capacitors, totaling $264uF$ were specified to achieve a reasonable transient response, and to meet an ESR requirement of $40m\Omega$ to satisfy 50mV of output ripple. AVX TPS series, low ESR tantalum dielectric was selected for the bulk output capacitance due to its high energy density over ceramic types for low voltage applications. Although base metal electrode, and polymer tantalum capacitors have had a surge of recent interest by the aerospace community, MnO2 based tantalum parts remain the modern standard.

Two $220uF$ wet slug capacitors were used on the converter input due to their storage capacity at higher voltage ratings. The large input capacitance is representative of the high bulk values needed for space rated EMI filters. High frequency, and logic level capacitors were composed of ceramic dielectric.

3.2.3 Control Loop Design

Current mode control was selected for its inherent short circuit protection, input disturbance rejection, and elimination of the pole introduced by the output inductor. These benefits reduce component count, and add design simplicity over voltage mode control. To reduce losses from a sense resistor in the primary power loop, a space rated current sense transformer (CS106) was used. A type-2 compensator was implemented with a design specification of 60 degrees of phase margin. A crossover frequency of 5 kHz was selected to maintain the 5% output voltage regulation under a 1 Amp load step under worst case output capacitance.

Slow start and slope compensation circuitry were added to prevent output overshoot during startup and subharmonic oscillation, respectively. The slow start circuit pulls down the COMP pin on the PWM controller to a voltage reference set by an RC network. Once the error amplifier signal reduces, it asserts over the slow start network, as shown in Figure 5. Slope compensation is applied directly to the current sense signal.

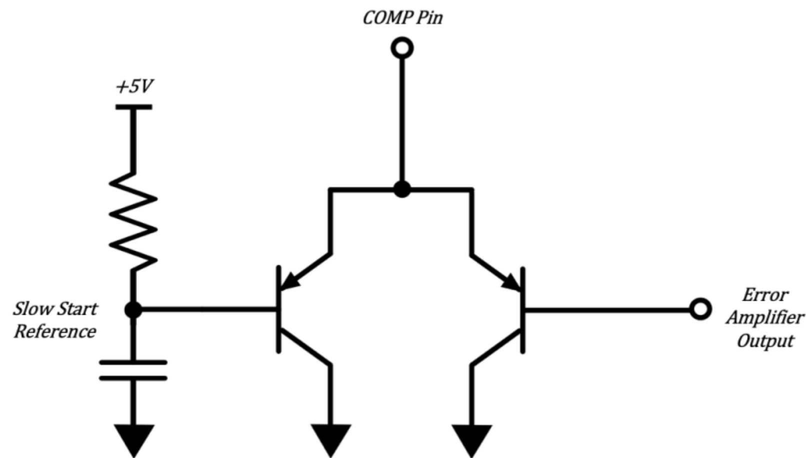


Figure 5 Slow Start Implementation

3.2.4 Isolation Barrier Communication

Radiation hardened parts typically avoid light-based modes of operation that can be easily triggered by single-event upsets in orbit. Correspondingly, the TL431, which pervades the field of switch mode power supply designs, cannot be used as an isolated error amplifier due to its reliance on an optocoupler. The alternative is magnetically operated devices that encode and decode analog error signals over a digital transformer. Both the digital isolator that transmits the synchronous switch command signals, and the isolated error amplifier, operate this way to achieve flight ratings. Note that the error amplifier internal to the PWM controller is bypassed via the COMP pin.

3.2.5 Dead Time Generator

The complexity that synchronous operation adds involves time-sensitive coordination to avoid shoot-through, a high current event through the power switches. This coordination does not solely occur on the secondary side of the transformer. It is the sequencing of Q_1 and Q_3 that can truly cause a shoot-through event. For example, if Q_1 is held off, no energy is transferred through the transformer, and a momentary overlap in the on times of Q_2 and Q_3 will cause a current event limited by the magnetizing inductance of the transformer secondary winding.

A self-driven synchronous scheme is possible, however, they either require their own sensing circuity, safety drawbacks due to maximum gate voltages, or transformer-based drivers that may not match the performance of a dedicated driver IC. Since the hard-switching characteristics are fundamental to this experiment, a dedicated driver is desirable, and self-driven

schemes are rejected. Furthermore, there exists an optimum deadtime for loss minimization, which is difficult to tune for using self-driven circuits.

A dead time generator is used with trim pots for simple dead-time adjustment, and a fixed delay to account for digital isolator and gate drive propagation times, as shown in Figure 6.

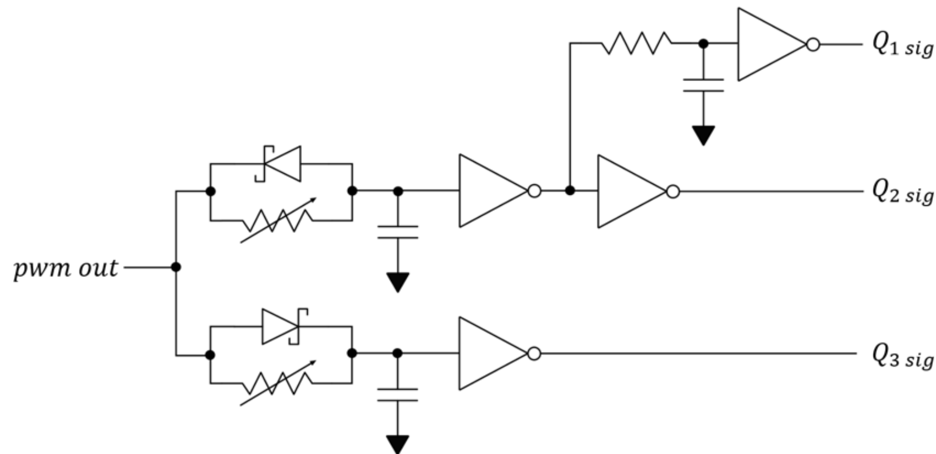


Figure 6 Adjustable Dead Time Generator and Digital Isolator Delay Compensator

3.2.6 Startup-Circuit & Linear Regulator

The primary and secondary sides of the converter require +12V and +5V for logic and gate drive circuits. To simplify the design, use of a bootstrap supply and auxiliary transformer winding were not implemented. The primary side uses two linear regulators from the input voltage bus downstream of each other, while the secondary relies on the output rail for +12V and a single linear regulator to provide +5V.

Since estimates of loss from these regulators can be relatively large, 1.5-2.0 W, dependent on the input voltage, mainly due to FET gate loss, a claim will be made in the discussion section

about absolute converter efficiency in the context of a flight design. Regardless, this loss is matched between the two boards, making relative comparison viable.

3.2.7 Snubber Network Design & Power Diode Considerations

Prior to primary switch $Q1$ turning on, $Q3$'s parallel diode $D3$ is conducting due to the allotted dead time in the system. The moment that $Q1$ does turn on, and energy begins to transfer to the secondary, causing $Q2$'s parallel diode to conduct, there is a momentary overlap in the on time of the diodes. This is primarily caused by the reverse recovery charge needed to fully turn off $D3$. In effect, the leakage inductance seen from the secondary of the transformer becomes energized with a current that diverges from the value of the output inductor. When $D3$ does turn off, the high $\frac{di}{dt}$ seen by the leakage inductance creates a voltage spike on the switch node with a ringing frequency effected by the output capacitances of the diode and switch.

A similar process occurs when $Q1$ turns off and the voltage spikes are able to appear at the drain of $Q1$ and $Q2$. Note that this case is more easily damped as the capacitance on the drain of $Q2$ is larger due to the parallel presence of the inductor.

Without snubber circuits, the voltage transients threaten the part ratings. For this reason, RC snubbers, to be tuned in circuit, were included in the design across each switch. Footprints for an optional RCD clamp snubber were added to the design on the secondary switch node if the reverse recovery event provided an initial current factor that an RC snubber alone couldn't handle. This hybrid approach is employed when the RC network eliminates ringing but not initial overshoot. The snubber circuits are shown in Figure 7.

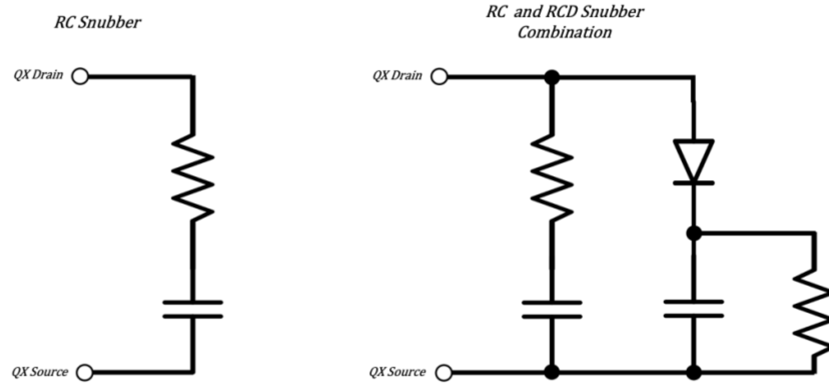


Figure 7 Implemented Snubber Networks on Q1 (RC), Q2 (RC), Q3 (RC and RCD)

Power Schottky diodes are often selected for parallel insertion over synchronous switches due to their reduced forward voltage when compared to the switch's body diode. It is also often claimed that a Schottky's metal junction yields a near zero reverse recovery time. While this is true of the metal junction, high power Schottky devices still exhibit reverse recovery events because of high values of parasitic capacitance and their protective guard ring structure, which is constructed via a PN junction [26].

Since power Schottky diodes $D2$ and $D3$ are critical devices in the power loop, an accurate match to a radiation hardened equivalent must be made when selecting affordable commercial components. The synchronous action will minimize the use of $D2$ and $D3$ such that the detailed approach found in section 4, involving pareto-optimal front formation, will not be used. For the match, we specify equivalent breakdown voltage, $\pm 10\%$ difference on forward voltage, and $\pm$250pF difference on the output capacitance at low bias conditions. Ideally, a reverse recovery time specification would be enacted, as that energizes the lossy snubber events, however, diode manufactures seldom include this information for Schottky diodes. See Table 2 for the selections.

3.2.8 Gate Driver for Si Based Board

As detailed in the FET selection section, the GaN based converter will use an integrated driver-HEMT module such that complexities introduced by layout are greatly reduced. However, the Si based board requires a gate driver such that all radiation hardened single MOSFETs remain as selection candidates. Of principle concern for the driver is radiation hardened status, and high output current capability so that the rise and fall times of $Q1$, $Q2$, and $Q3$ are minimized and the subsequent switching losses are not limited by the driver. As seen in Table 2, the ISL74422BRH was selected, which can deliver 9A of current to the MOSFET gates. Gate resistors will only be used if the FETs have extremely poor voltage overshoot values when tested. The priority will be switching loss minimization so that the Si baseline efficiency results are not degraded.

3.2.9 Omitted Converter Features

The core functionality of a space rated converter was accounted for, however, a few areas that don't impact the desired measurements of the experiment were not realized. For thoroughness, these are listed below:

- Under voltage lockout set-points
- Protection circuits other than inherent current limiting from current mode control
- Temperature / Output telemetry
- PCB size constraints
- Auxiliary winding for efficient logic power supply
- Detailed EMI filter

3.3 Simulation & Design Verification

Two LTspice models were created, one for transient simulation, Figure 8, which included complex component models and full switching events, and the other for control loop verification, Figure 9, which used as an average switch model developed by [26].

Although transient response is not of principle concern for this study, stability verification for steady-state performance was essential. Furthermore, accounting for the poles and offsets introduced by the isolated error amplifier and the PWM controller is a non-trivial task.

Monte Carlo and worst-case simulations were ran over an ac-analysis of the open loop average model with de-rated component values and their datasheet tolerances. This resulted in Figure 10, which was also verified by an analytical transfer function evaluation, developed by [26], as shown in Figure 11.

The transient model in Figure 9 was used to ensure basic converter functionality and verify the schematic design. Although a rigorous modeling process could bring detailed loss estimates and performance characterizations, this study is concerned with the realized hardware. We desire to include the subtle effects that are difficult to capture within simulation, like thermals and layout parasitics. Although GaN transient models are continuously improving, the interplay between the driver, and the faster slew rates that the material allows for, lead to many complexities, including simulation time, and a reliance on board parasitics. Our transient simulations omitted specific FET models, driver models, and passives that incorporated parasitics other than series resistance. The PWM controller, error amplifier, current transformer, dead time generator, snubber networks, and synchronous switches, were however, included. A sample of these simulation results were selected to display the basic functionality, shown in Figure 12, Figure 13, and Figure 14.

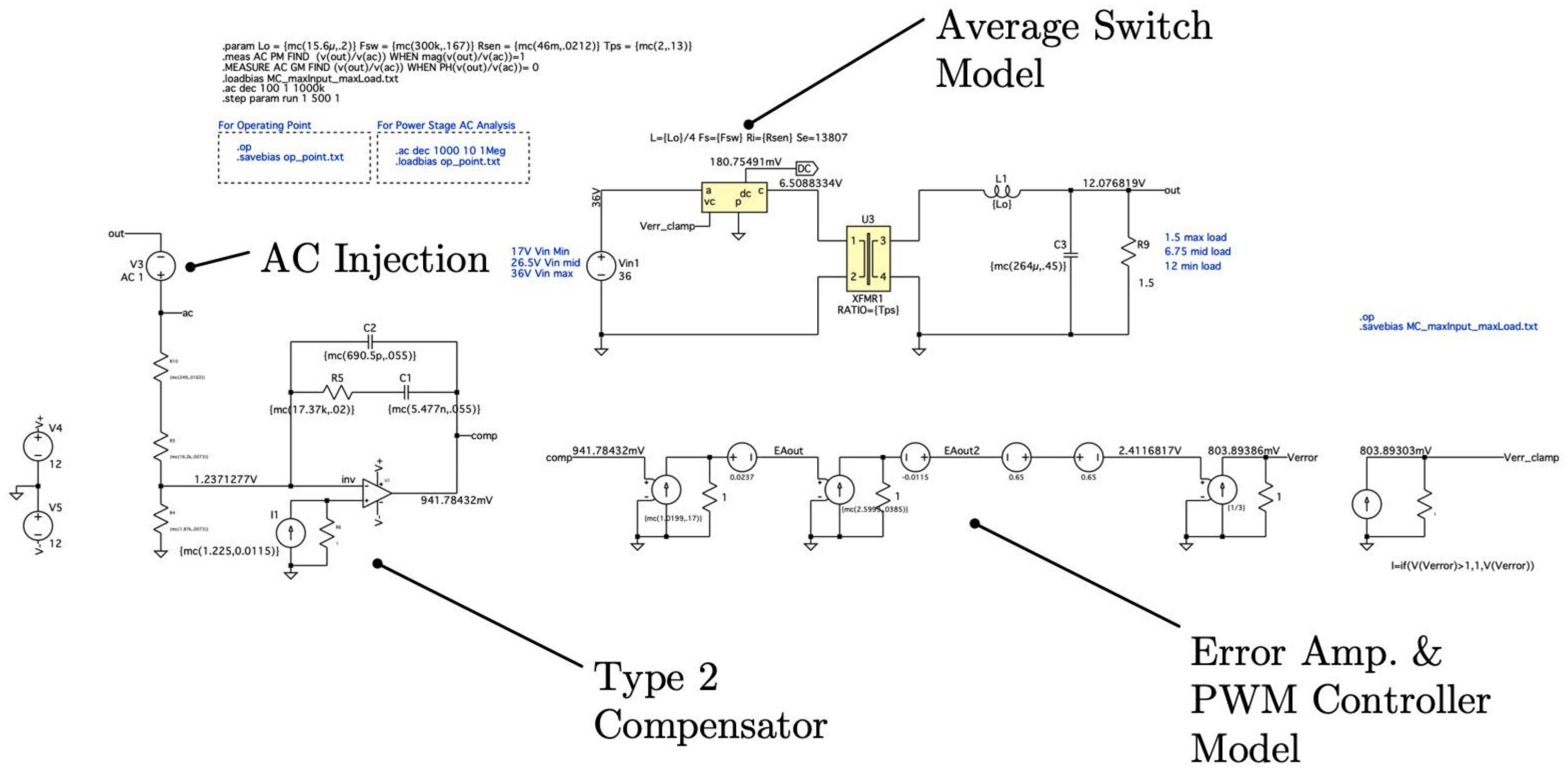


Figure 8 LTSpice Average Model of Forward Converter Used in Control System Design

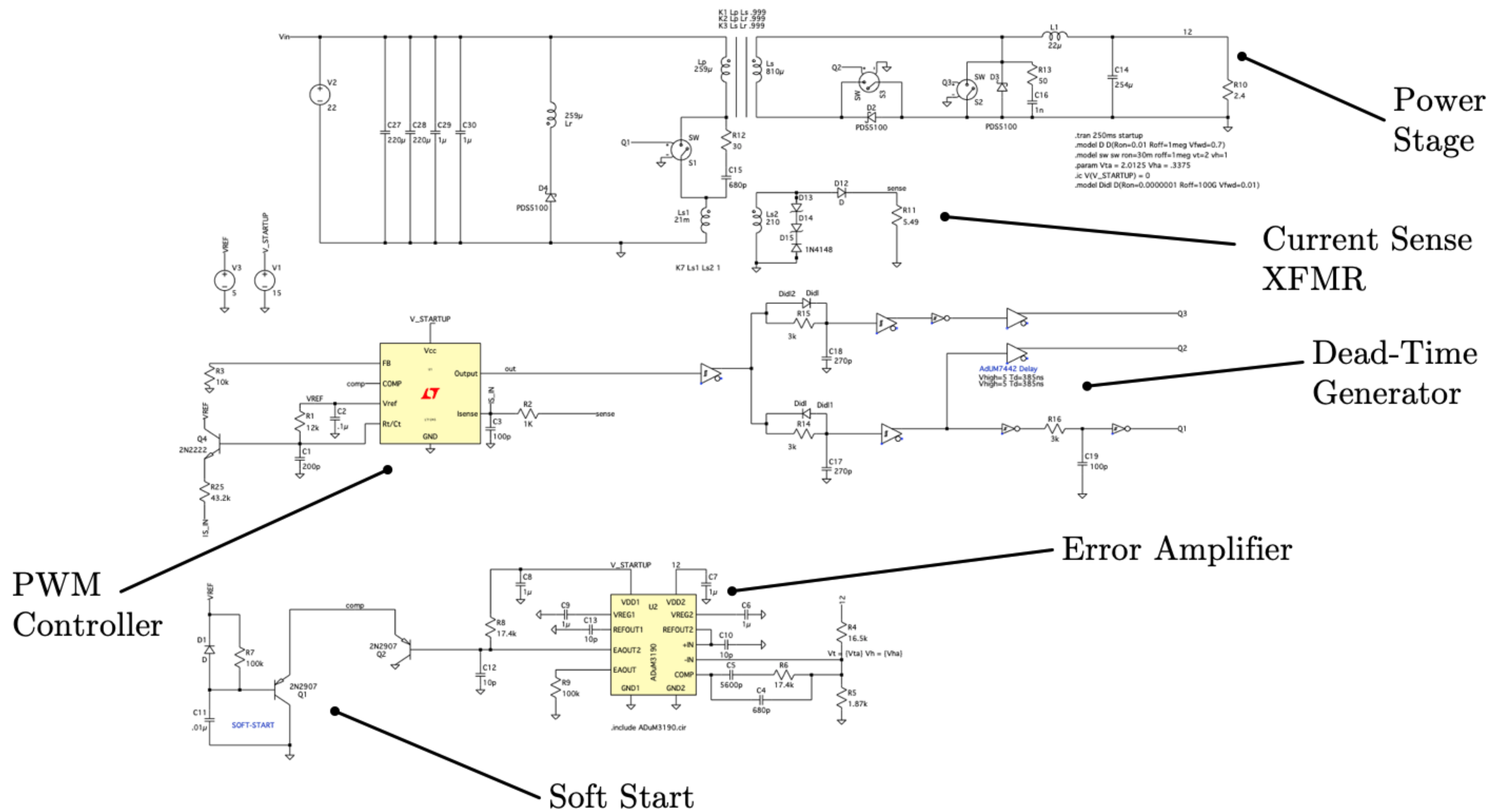


Figure 9 LTSpice Transient Model Used to Verify Basic Converter Functionality

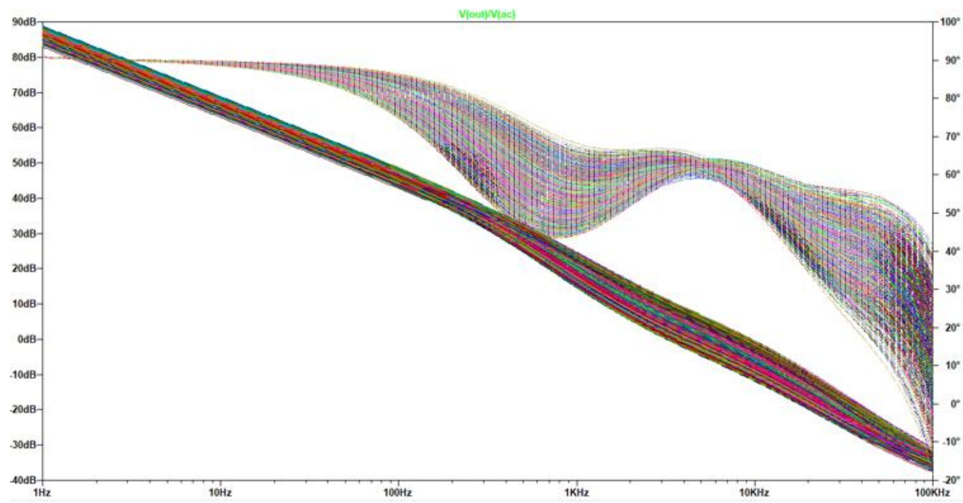


Figure 10 Loop Gain/Phase Monte-Carlo Simulation from Forward Converter LTSpice Average Model

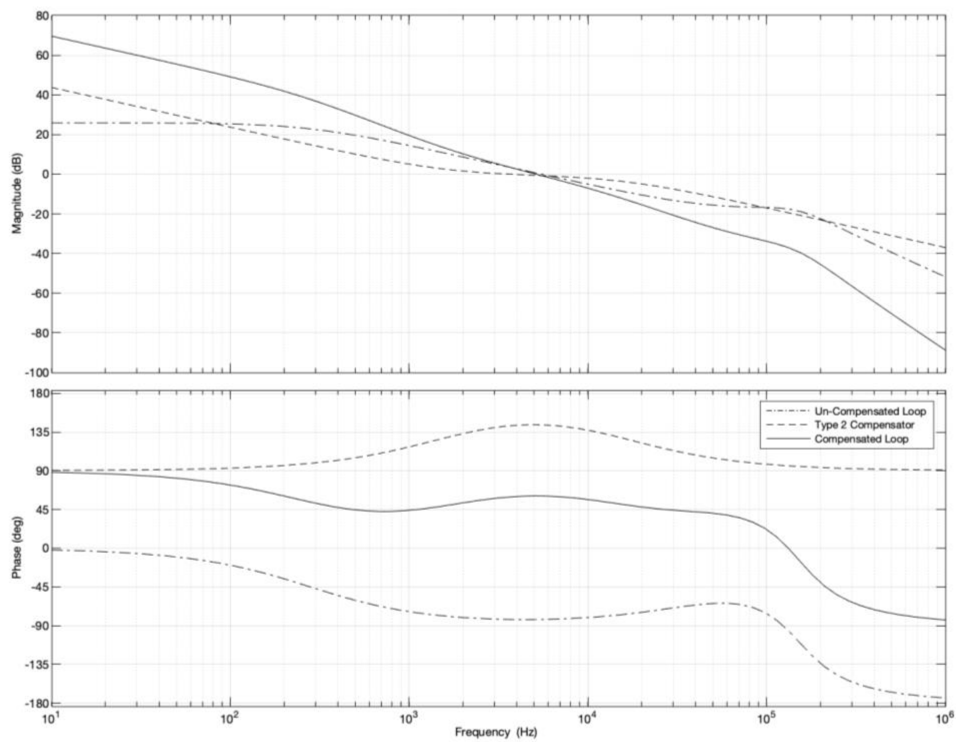


Figure 11 Loop Gain/Phase Analytical Evaluation from Forward Converter Transfer Function

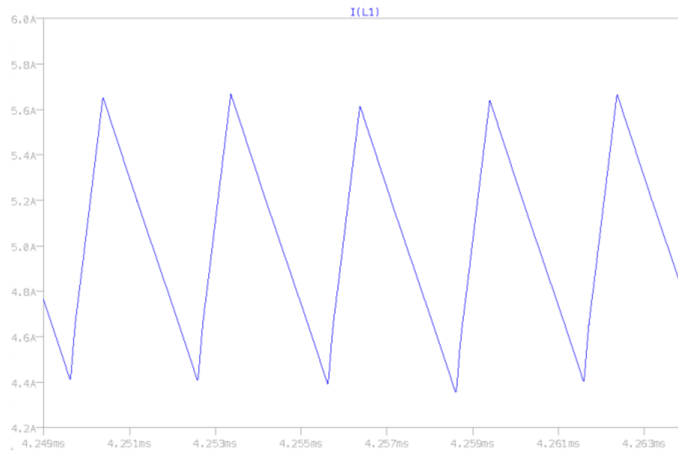


Figure 12 Transient Simulation Waveform: Output Ripple at Iout = 5A

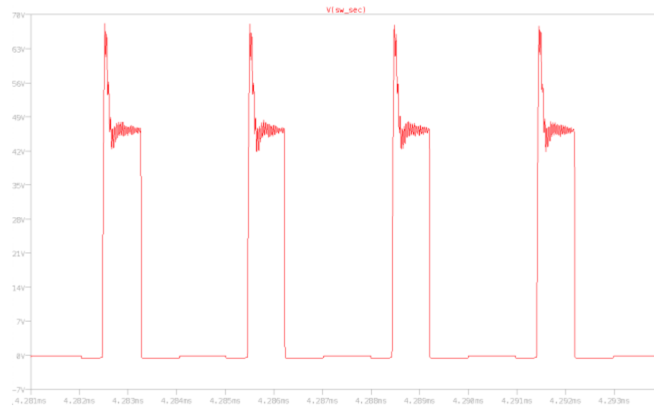


Figure 13 Transient Simulation Waveform: Secondary Switch Node

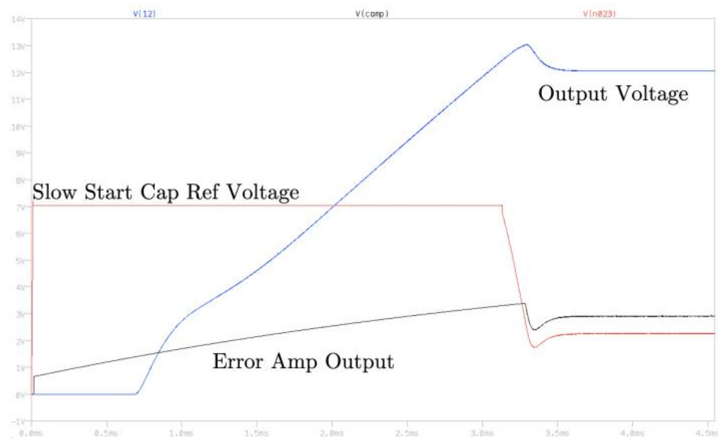


Figure 14 Transient Simulation Waveforms: Startup Signals

4.0 FET Selection

4.1 Si Baseline FET Selection Methodology

The switch used in the Si baseline converter must be an optimal representation of the market available technology for high reliability, space rated components such that the GaN comparison is accurate and fair. Since minor variations in losses can heavily effect converter efficiency, the device selection process must be rigorous. Breakdown voltage, power dissipation, and average/peak drain current specifications initially constrain the selection pool so that converter functionality is ensured. Afterwards, the pareto-optimal front from the $R_{ds(ON)}\ vs\ Q_{g\ total}$ plot for the remaining devices is formed. For high reliability radiation-hardened single MOSFETs, International Rectifier / Infineon are one of the largest manufacturers of power switches for the aerospace community. Though this limits selection options, it allows for an exhaustive analysis of the device dataset. Due to the high cost and lead times of these radiation-hardened MOSFETs, a commercial part will be matched to the optimal flight part, and be used in converter testing. Analytical loss analysis will be reported for both the radiation hardened and COTS components to verify matching quality. That said, not all device parameters will lead to a one-to-one match. To bound the error that comes from part matching, a separate set of components are used whose key characteristics dominate the class of radiation hardened devices. By experimentally testing both sets of matched, and dominant switches, the accuracy of the baseline Si performance can be maintained. We hope this process can serve as a methodology for future affordable part matching in aerospace research.

$R_{ds(ON)} \cdot Q_{g\ total}$ is a common figure of merit for field-effect transistors because it alludes to conduction, switching, and gate loss. Note that the total gate charge is dependent on the operating point of the circuit. While the detailed loss comparison for the chosen devices will calculate $Q_{g\ total}$ for a nominal operating point of the converter, the pareto-optimal front will be formed from datasheet values.

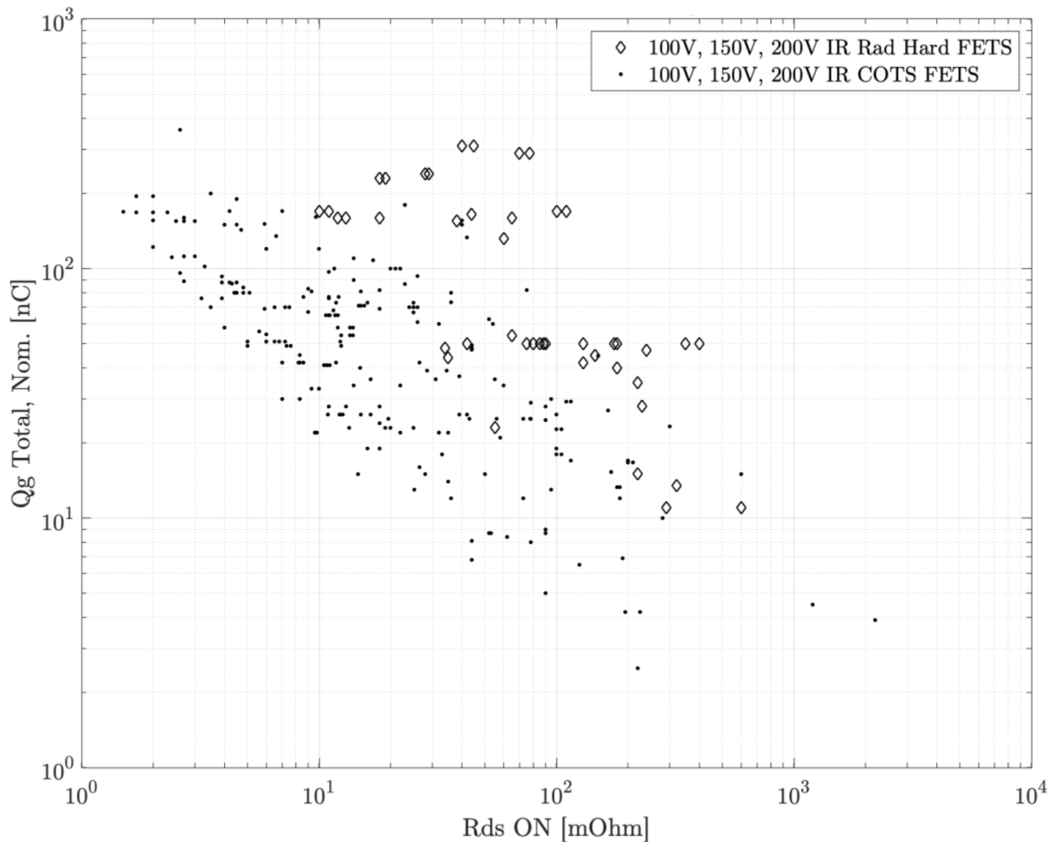


Figure 15 Total Gate Charge Vs RdsON of IR Rad Hard & COTS FETs Log Scale (Nominal Datasheet Qgtotal, RdsON @25C)

To further contextualize and motivate the need for improved radiation hardened power switches, Figure 15 was created. All 76 rad-hard single N-channel Infineon MOSFETs of 100V-200V breakdown voltages are included. To represent trends from the non-rad-hard commercial

sector, all of Infineon's active N-channel MOSFETs of the same breakdown voltages are plotted. The groupings are separated by approximately an order of magnitude on each axis, making the $R_{ds(ON)} \cdot Q_{g\ total}$ F.O.M. differ by a factor of 100. Here lies the opportunity for wide band gap devices who can avoid the performance degrading techniques that yield radiation hardened ratings.

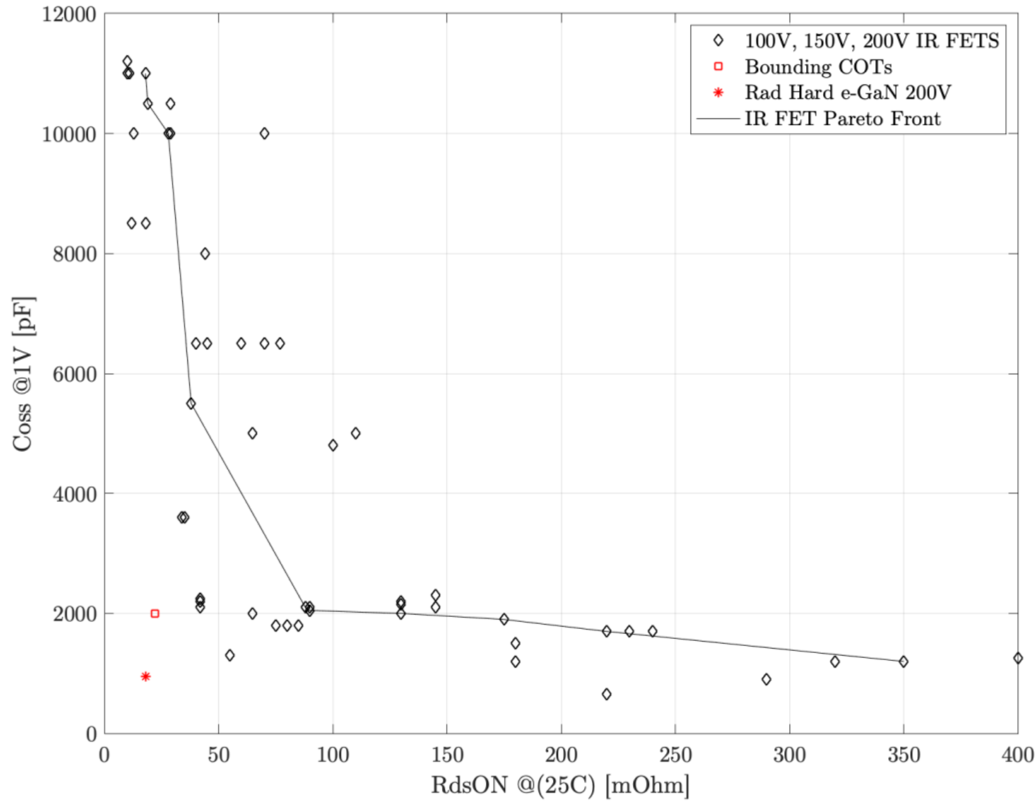


Figure 16 Output Capacitance Vs RdsON of IR Rad Hard FETs, Coss @ Vds = 1V, RdsON @ 25C

Capacitive losses are accounted for by plotting the output capacitance C_{oss} at a single bias point. An effective energy $C_{oss(ER)}$ or charge time $C_{oss(TR)}$ value would be better for device comparison and absolute accuracy, as those metrics account for the C_{oss} nonlinearity over a range of drain-source voltages. Ideally, the capacitive losses could be calculated outright via numerical

integration of C_{oss} for each device. However, the image format of the datasheet plots makes this a work intensive process reserved for after device selection. Plotting at a single bias point, in this case, 1V, to cover the largest magnitudes of the graph, will roughly track the loss mode.

Capacitive losses will be used as a secondary heuristic when finding the representative device. For synchronous switches Q_2 and Q_3, C_{oss} holds a high weight as diode commutation makes switching loss near zero for these devices. Though C_{oss} could be used in a 3-dimensional pareto front, $R_{ds(ON)} \cdot Q_{g\ total}$, will take priority for visual clarity and simplicity. Additionally, $Q_{g\ total}$ trends with C_{oss}.

Devices on the pareto front indicate the 'obvious' initial choices when optimizing for $R_{ds(ON)}, and\ Q_{g\ total}$. No part along that front can improve both $R_{ds(ON)}$ and $Q_{g\ total}$ in comparison to any other part on the front. There must be a tradeoff when comparing that optimal subgroup, known as the non-dominated solutions.

A methodology is still required to select the optimal part from the non-dominated solutions to minimize converter loss. To do this, an analytical approach is taken to calculate the conduction loss, and dynamic losses. Because $R_{ds(ON)}$ directly relates to conduction loss, and $Q_{g\ total}$ to switching loss, total FET loss minimization can be approached by selecting devices that make conduction loss and dynamic loss converge. It is precisely because the pareto-optimal front mimics an inverse relationship that this method is applicable. Since the radiation hardened selection pool is small, using this analytical method to iterate over 2-5 devices can result in a near optimal selection to minimize loss, and to establish a fair comparison for this study. Note that Figure 17 is plotted on a linear-linear scale as opposed to the log-log scale of Figure 15. This is because the final manual, iterative process requires some user intuitions of the tradeoff, which is aided by the linear scaling.

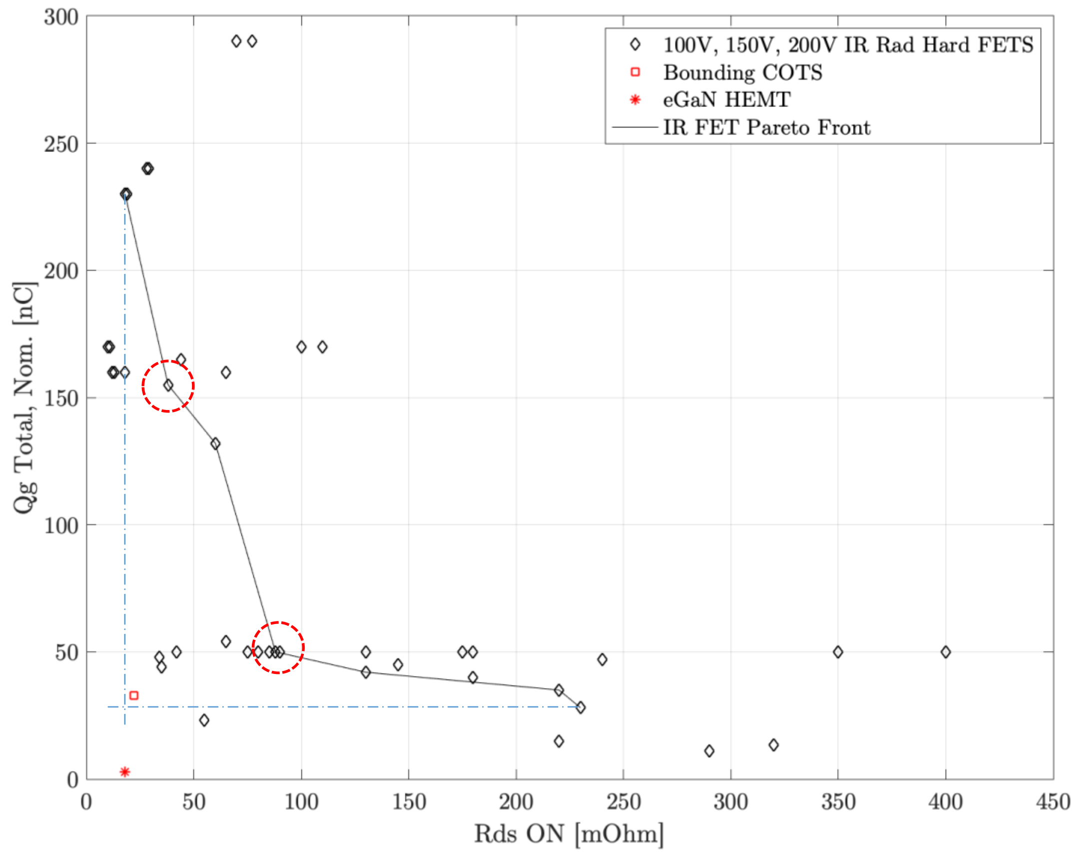


Figure 17 Total Gate Charge Vs RdsON of IR Rad Hard & COTS FETs Linear Scale (Nominal Datasheet Qgtotal, RdsON @25C)

Simulation and initial prototype work proved that voltage spikes from transformer leakage inductance lead to poor safety margin for 100V rated parts. For this reason, the pareto front is made out of only the 150V, and 200V parts. The 100V parts are included as points for reference. Two parts were selected for the analytical converter loss evaluation (circled): IRHNJ67134 (right most), and IRHNS57260SE (left most). Once again, the roughly inverse relationship of $R_{ds(ON)}$ to $Q_{g\ total}$ makes selections closest to the origin a good starting place. It also makes for an

interesting study to compare these two particular parts who make large trade-offs between $R_{ds(ON)}$ and $Q_{g\ total}$.

The synchronous FETs have extremely minor switching losses due to the Schottky diodes roll in commutating, which reduces drain source voltage to that of a diode drop, to ensure dead time. Therefore, it initially seems that minimizing $R_{ds(ON)}$ and taking on additional $Q_{g\ total}$ will be favorable. However, it is these FETs that are greatly aided by Figure 16, the biased C_{oss} $vs\ R_{ds(ON)}$. Moving below 85 $m\Omega$ requires a steep increase in both $Q_{g\ total}$ and C_{oss}. When parts that had over 5000 pF of C_{oss} at 1V were used, snubber losses became heavily load dependent, and the core reset action was significantly delayed. For this reason, the circled part in Figure 17 with the higher on resistance was used (IRHNJ67134) as the basis for part matching of synchronous switches Q_2 and Q_3. The decision for primary FET Q_1 requires the loss analysis discussed in the next section.

Three breakdown voltages (100V, 150V, and 200V), are included in Figure 15, Figure 16, and Figure 17 out of the radiation-hardened IR MOSFETs. This follows from $Q_1's$ requirement to withstand $V_{in}(1 + N_r)$, and $Q_2/Q_3's$ requirement to withstand NV_{in}. Figure 18 plots fit lines for the devices with equal breakdown voltages to illustrate the tradeoff between added safety margin and performance. The general trend of smaller breakdown voltage to increased performance is shown. The factor of improvement for figure of merit $R_{ds(ON)} \cdot Q_{g\ total}$ when moving from 200V to 150V, and 200V to 100V is roughly 1.25 and 2.5 respectively.

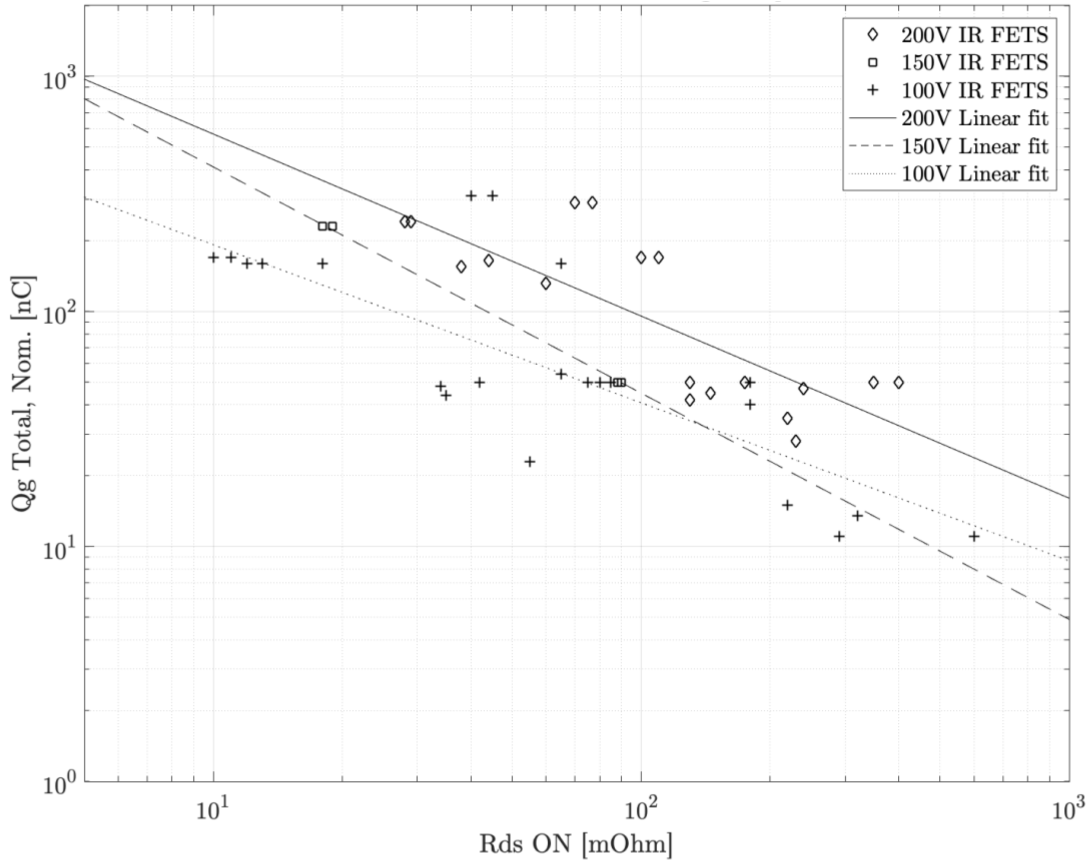


Figure 18 Qgtotal Vs RdsON of IR Rad Hard FETs Breakdown Voltage Comparison (Nominal Datasheet Qgtotal, RdsON @25C)

4.2 FET Loss Calculations used in Selection Process

4.2.1 Thermal Considerations

There is a strong temperature dependence on $R_{ds(ON)}$, and the loss metrics of interest. Iterative methods to solve for both switch power loss and $R_{ds(ON)}$ at the same time have been

shown to be effective [1], in addition to other predictions based on expected temperature rise from the thermal design space [27]. However, the COTS part matching process will prioritize $R_{ds(ON)}$, $Q_{g\ total}$, and C_{oss}, leaving limited options for package types that yield enough degrees of freedom to properly match thermal resistance values. We will reduce error from the thermal differences by trying both match options in circuit from Figure 15, and using the part that results in higher efficiency. Additionally, a second set of results will be obtained for the Si board to create an upper bound on rad-hard Si performance and to bound the error of COTS mismatch.

When choosing the optimal rad-hard part, we will assume a constant junction temperature of 100°C. In this stage of the design, layout and thermals had not yet been defined, making the thermal resistance parameters inaccurate.

4.2.2 Loss Operating Point

Dynamic losses depend on both drain to source voltage and charge transferred over parasitic capacitances, which is a function of drain to source voltage. At high input voltages, drain current reduces, however, the drain to source voltage dominates, and switching, gate, and capacitive losses increase. At low input voltages the duty cycle increases, and conduction losses rise.

Of interest is what operating point(s) take priority in the loss analysis. High output currents will lead to high conduction losses, while high input voltages will lead to high dynamic losses. Priority could be taken at a single nominal operating point, or both the load and input could be varied to check if there is a crossover point between the total loss of the two switch options.

Parts are thought to be balanced for the application when one, the loss remains approximately constant over the input voltage range such that dynamic loss increase matches

conduction loss decrease, and two, the dynamic losses are close to 50% of the conduction losses at a nominal operating point.

4.2.3 Conduction Losses

The typical $R_{ds(ON)}$ value and the normalized $R_{ds(ON)}\ vs\ T_j$ datasheet plot was used to adjust for the 100°C bias point. A nominal operating point of $V_{in} = 28V$ and $I_{out} = 3A$ was selected to calculate the RMS currents. Equations 4-1 to 4-4, from [26], specify the RMS currents used in the conduction loss calculations.

$$I_{rms_Q1} = \frac{\sqrt{D(12I_{out}N)^2 + \left(I_{ripple}N\right)^2}}{2\sqrt{3}} \tag{4-1}$$

$$I_{rms_Q3} = \frac{\sqrt{(1 - D - t_{dead})(12I_{out})^2 + \left(I_{ripple}\right)^2}}{2\sqrt{3}} \tag{4-2}$$

$$I_{rms_Q2} = \frac{\sqrt{(1 - D)(12I_{out})^2 + \left(I_{ripple}\right)^2}}{2\sqrt{3}} \tag{4-3}$$

$$P_{con} = I_{rms_{Qx}}^2 R_{ds(ON)} \tag{4-4}$$

4.2.4 Dynamic Losses

To adjust the pre-biased datasheet values, the methods used in [1] were employed, and are summarized below.

1. Digitize $C_{oss}, C_{iss}, C_{rss}\ vs\ V_{ds}$, and $I_d vs\ V_{gs}$ plots from the datasheet.

2. Record $V_{th}, V_{pl}, Q_{gs}, Q_{gd}, Q_g$ from the datasheet at pre-biased values
3. Integrate C_{rss} numerically to find the charge transferred from the drain to the gate during voltage transition.

$$Q_{GD} = \int_0^{V_{bus}} C_{rss}(V_{ds})dV_{ds} \qquad \textbf{4-5}$$

4. Interpolate I_d vs V_{gs} data at $I_d = N \cdot 3\ A$, to find V_{pl_op}, the plateau voltage at the operating point
5. Find the charge required to reach the threshold of the device by assuming constant $\frac{Q_{gs}}{V_{pl}}$ ratio.

$$Q_{gs_op} = \frac{Q_{gs}}{V_{pl}} V_{pl_op} \qquad \textbf{4-6}$$

6. Calculate Q_{gs2}, the charge required to move from threshold to plateau voltage.

$$Q_{gs2} = Q_{gs_op} - Q_{gs} \qquad \textbf{4-7}$$

7. Calculate switch losses from:

$$P_{on} = \frac{V_{bus} I_{DS} f_{sw} R_{Gon}}{2} [\frac{Q_{gd}}{V_{dr} - V_{pl}} + \frac{Q_{gs2}}{V_{dr} - (\frac{V_{pl} + V_{th}}{2})}] \qquad \textbf{4-8}$$

$$P_{off} = \frac{V_{bus} I_{DS} f_{sw} R_{Gon}}{2} [\frac{Q_{gd}}{V_{pl}} + \frac{Q_{gs2}}{(\frac{V_{pl} + V_{th}}{2})}] \qquad \textbf{4-9}$$

8. Integrate C_{oss} numerically, to find capacitive losses via:

$$P_{oss} = f_{sw} \int_0^{V_{bus}} C_{oss}(V_{ds}) dV_{ds} \quad \textbf{4-10}$$

9. Find the slope of the gate charge Q_g during overdrive, and use it find Q_{g_op}

$$m_{QGslope} = \frac{Q_g - Q_{gs} + Q_{Gd}}{V_{dr} - V_{pl}} \quad \textbf{4-11}$$

$$Q_{g_op} = Q_{gs(op)} + Q_{gd} + m_{QGslope}(V_{dr_op} - V_{pl_op}) \quad \textbf{4-12}$$

10. Calculate gate losses by

$$P_g = Q_{g_op} V_{dr} f_{sw} \quad \textbf{4-13}$$

For Q_1, the V_{ds} values used to calculate both P_{on}/P_{off} and P_{oss} should be limited to V_{in} and not $2V_{in}$, which is tempting to do since the reset winding doubles the voltage on the drain of this FET. However, we can be sure that the FET is off prior to the reset action occurring. In fact, it is solely because the current through Q_1 has diminished that the voltage then doubles. Furthermore, the capacitance loss values of Q_1 shouldn't consider the charge recycled by the reset winding which returns to the converter input source or capacitors. This restricts V_{bus} to V_{in} in the gate loss calculation.

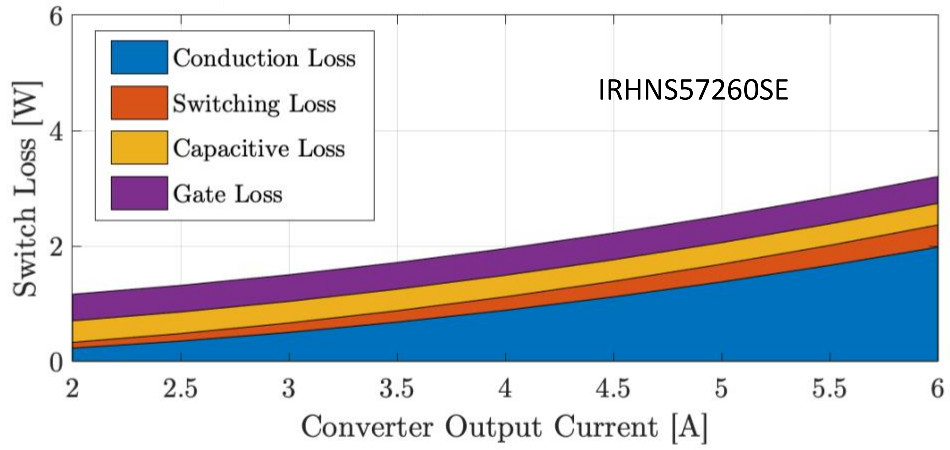
4.3 Evaluation of Radiation Hardened Optimal Candidates for Q1

By performing the loss analysis above on switch position Q_1 the two circled devices from Table 3 can be evaluated.

Table 3 Q1 Losses for Rad-Hard Candidates at Vin=28V, Iout = 3A

Loss Mode	IRHNJ67134	IRHN57260SE
Conduction	1.12	0.50
Switching	0.10	0.16
Capacitive	0.13	0.37
Gate	0.18	0.46
Total	1.54	1.50

The loss at a single, nominal operating point favors the part with lower on resistance, but only slightly. By plotting the loss over the full range of output currents with a fixed input voltage, or vice versa, crossover points can be checked for (Figure 19 and Figure 20). Additionally, we can gain an intuition for the ratio for dynamic losses to conduction losses as the input/output conditions vary. As seen in the plots, for very low load conditions, IRHNS57260SE becomes favorable, however, the part is dominated by conduction losses in the $Q1$ position, especially at high output powers. A similar effect happens when load current is held constant as in Figure 20. The duty cycle decrease leads to a larger effect of conduction losses, so that a crossover occurs at around $V_{in} = 30V$.



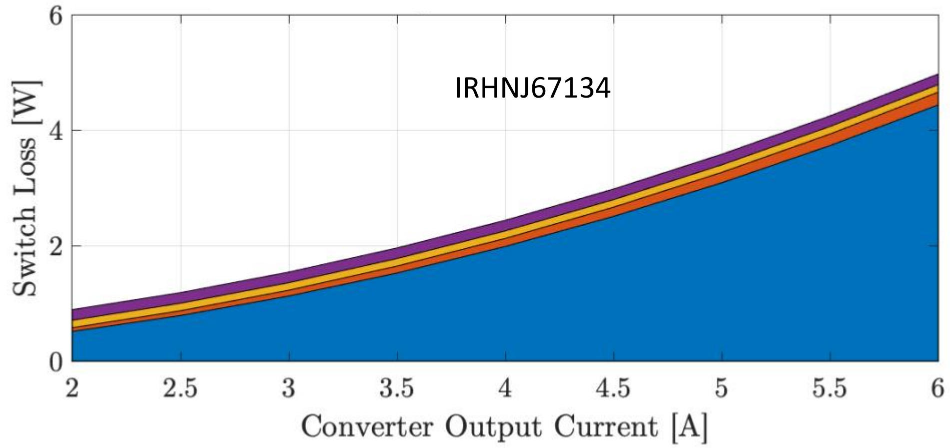


Figure 19 Q1 Switch Loss vs Converter Output Current (IRHNS57260SE & IRHNJ67134), Vin = 28V

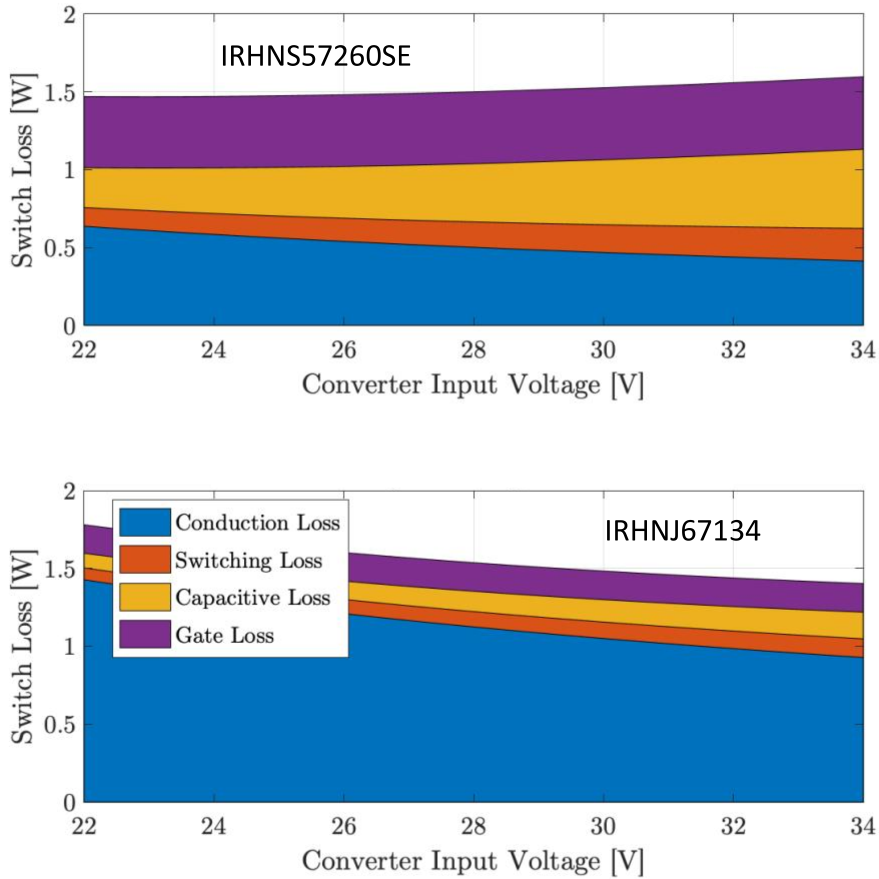


Figure 20 Q1 Switch Loss vs Converter Input Voltage (IRHNS57260SE & IRHNJ67134), Iout = 3A

At high load, the advantage goes to IRHNS57260SE, however, at low load and high input voltage, it goes to IRHNJ67134. Since thermal requirements could constrain the maximum dissipation, IRHNS57260SE is considered the optimal part. Furthermore, for a large range of output current, the dynamic losses approximately match the conduction losses, which indicates a good ratio of $R_{ds(ON)}$ to $Q_{g\ total}$ out of the options on the pareto-optimal front.

For concision, a comparison of the part with the next increase in $R_{ds(ON)}$ is not shown, however the increase in conduction losses led to IRHNJ67134 remaining the optimal selection.

As stated previously, to account for thermal error, both radiation hardened parts will be used as references for COTS matching. Selections are shown in Table 5.

4.4 Error Bounding the Radiation Hardened Match Selection

The vertical and horizontal dotted lines on Figure 17 indicate the globally lowest value of $R_{ds(ON)}$ and $Q_{g\ total}$, respectively, on the pareto optimal front. By choosing a commercial part that is close to the intersection of these lines, we are taking the minimum heuristic loss characteristics from multiple parts. While this approach means that the resulting commercial device doesn't match with any market available radiation hardened equivalent, it does mean that no radiation hardened device can perform better. Therefore, we can put an absolute upper bound on the class of radiation hardened options in terms of efficiency. FDD86250 was the selection for the bounding case, as shown in Table 5.

4.5 COTS Matching Verification

The two devices used to match the radiation hardened selections are shown in Table 5. Note that this table includes two parameters that come from the dynamic loss calculation to be able to equate device parameters at similar operating points instead of datasheet values. $R_{ds(ON)}$ values of the matched components are within 8% of the Rad-hard selections, and $Q_{g\ total}$ within 12.9%.

The three decided upon test configurations for the Si based converter are shown in Table 4. Configuration 1 represents the case where the optimal Si radiation hardened FETs were matched. Configuration 2 is tested to experimentally check for matching errors of configuration 1 by matching Q_1 to the 'runner-up' part from the pareto-optimal front. Configuration 3 marks the performance limit of the available devices.

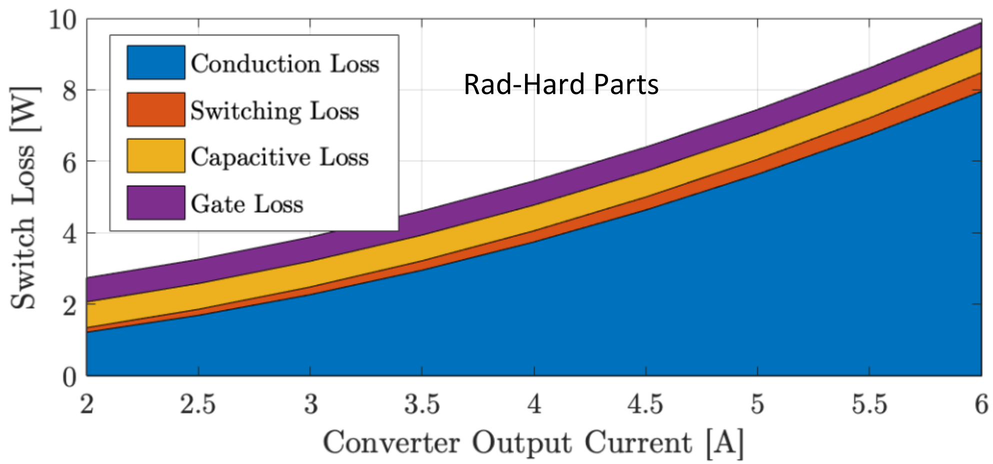
The quality of the matching was judged based on a total switch loss comparison of the selected COTS devices and their hypothesized radiation hardened equivalents. Q_1, Q_2, and Q_3 are all included, and configuration 1 from Table 4 is used as it was predicted optimal during the previous analysis. As seen from Figure 21 and Figure 22, the matching is extremely comparable.

Table 4 FET Configurations for Si Forward Converter

Config.	Q1	Q2	Q3
1	SQM60N20-35	IRFR24N15D	IRFR24N15D
2	IRFR24N15D	IRFR24N15D	IRFR24N15D
3	FDD86250	FDD86250	FDD86250

Table 5 FET Selection Comparison Rad-Hard, COTS, Bounding, eGaN

	Optimal Si Rad Hard MOSFET A (IRHNS57260SE)	COTs matched Si Rad Hard MOSFET A (SQM60N20-35)	Optimal Si Rad Hard MOSFET B (IRHNJ67134)	COT matched Si Rad Hard MOSFET B (IRFR24N15D)	Rad Hard eGaN HEMT Die (FDA20N18X3)	COTs Bounding FET (FDD86250)
$V_{ds(max)}$ (V)	200	200	150	150	200	150
$V_{GS(th\ max)}$ (V)	4.5	3.5	4.0	5.0	1.2	4
$R_{ds(ON\ max)}$ (mΩ)	38.0	35.0	88.0	95.0	25	22
$Q_{gate\ datasheet}$ (nC)	155.0	135.0	50.0	45.0	6	33
E_{oss} (uJ), V_{ds}=56V	1.03	0.59	0.44	0.36	0.53	0.74
$Q_{gate\ op\ nom}$ (nC)	102.60	110.03	40.81	32.07	2.40	56.49



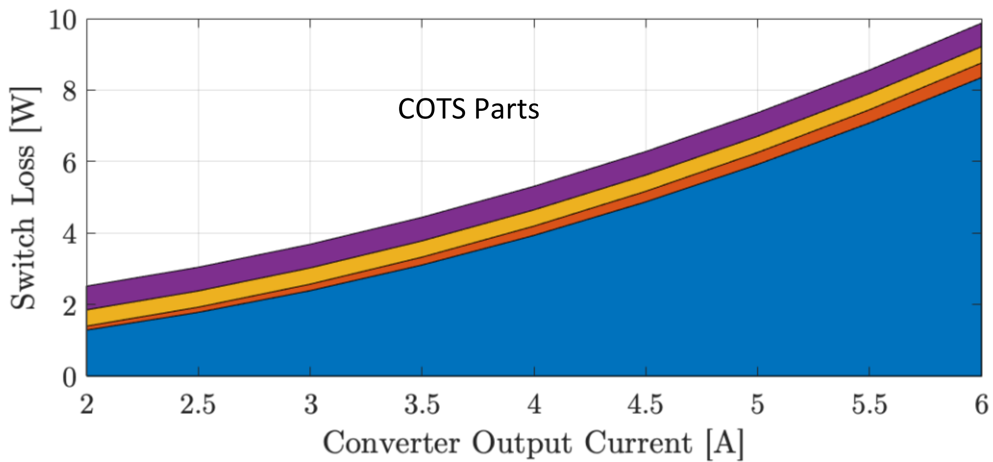
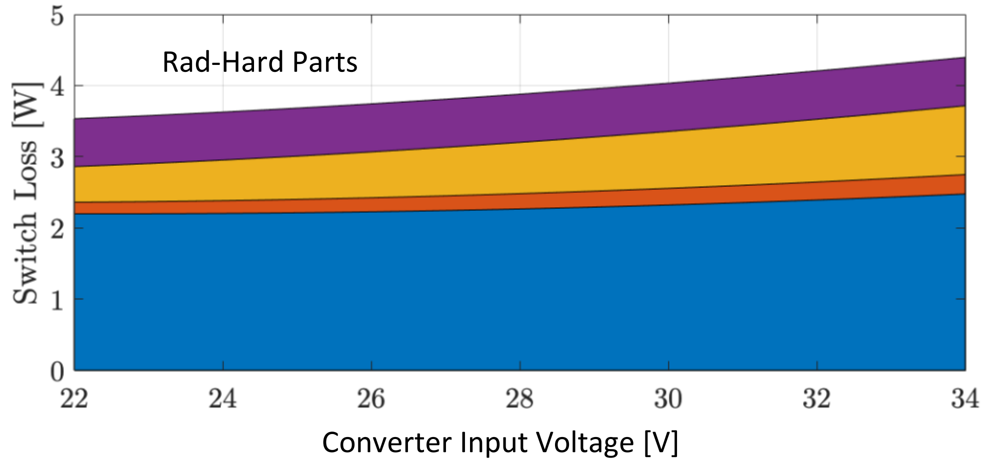


Figure 21 Combined Switch Loss Vs Output Current Comparison (Q1, Q2, Q3) for Optimal Rad-Hard Selections and COTS Matched Selections, Vin = 28V



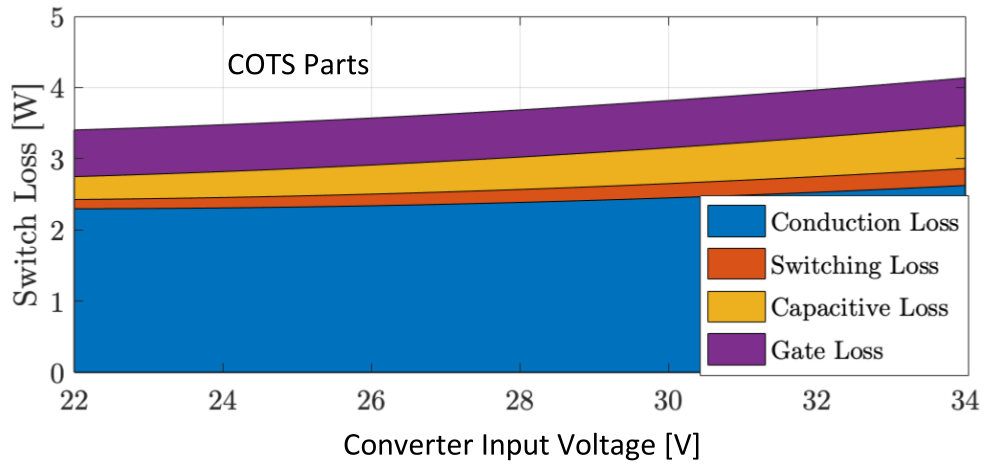


Figure 22 Combinaed Switch Loss Vs Input Voltage Comparison (Q1, Q2, Q3) for Optimal Rad-Hard Selections and COTS Matched Selections, Iout = 3A

4.6 GaN Device Selection

The main drawback of GaN transistors is their drive sensitivity. Low maximum gate voltage paired with GaN's higher voltage and current slew rates can lead to Miller turn-on, voltage spikes on common source inductances, ground bounce, and various other failure modes or performance degrading events [1]. For proper mitigation, proper PCB layout and driver design are essential.

Though the high slew rates must be accounted for in the power loop layouts of the GaN-based converter, it was declared outside the scope of this experiment to optimally coordinate separate space-rated driver and HEMT components. It was therefore desirable to select an integrated module that incorporated both components in the same package, ensuring proper functionality.

Over the past 10 years, there has been a surge of GaN manufacturers in the commercial sector. Although these available devices are proving to have many radiation hardened qualities due to the inherent large band-gap nature of GaN, they don't have the qualification testing for aerospace applications. Despite their use in other aerospace research, they don't fit with the experimental theme of using only components ready to fly today.

For $Q_1, Q_2, and\ Q_3$ it is preferable for switches to fail in the open state. This restricts energy transfer to the secondary of the converter and prevents the synchronous switches from creating a shoot-through event. It is therefore crucial to obtain enhancement mode GaN devices such that the converter failure modes minimize system damage in the event of driver power loss. Since GaN FETs are naturally a depletion mode device, a secondary mechanism is required. The simplest strategy is to employ a cascode Si MOSFET, which is naturally enhancement mode. For

this experiment, we will reject any devices using this mechanism due to its poor performance, and dependence on radiation hardened Si devices.

At the moment, Freebird Semiconductor is the only manufacturer that produces an integrated driver-HEMT module with guaranteed space-borne radiation hardness assurance. Their enhancement mechanism is entirely GaN based. Therefore, the FBS-GAM01-P-C100 Adapter module was chosen which houses the FDA20N18X enhancement mode GaN switch. The module selection was highly constrained by converter maximum requirements, but well represents the selection of available FreeBird GaN HEMTs. It's figure of merit values are plotted in Figure 16 and Figure 17. The same loss analysis was ran on the GaN devices for the Q_1 switch position, resulting in Figure 23.

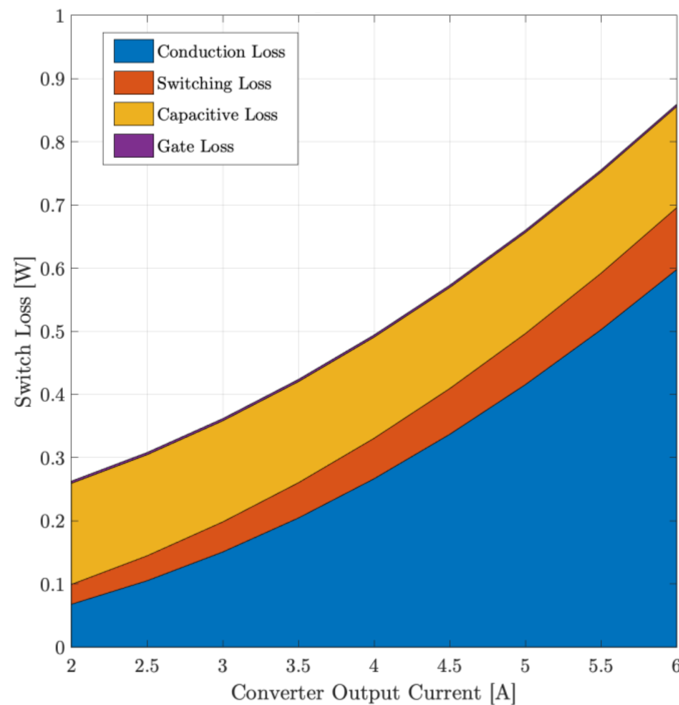


Figure 23 Q1 Switch Loss eGaN Vs Converter Output Current (FDA20N18X3), Vin = 28V

5.0 Results

The two converters were implemented and characterized. Shown in Figure 24 is the GaN based version. Prior to taking key comparison measurements, switching frequency and dead time were tuned to within 1% of 300kHz, and 150 nS, respectively.

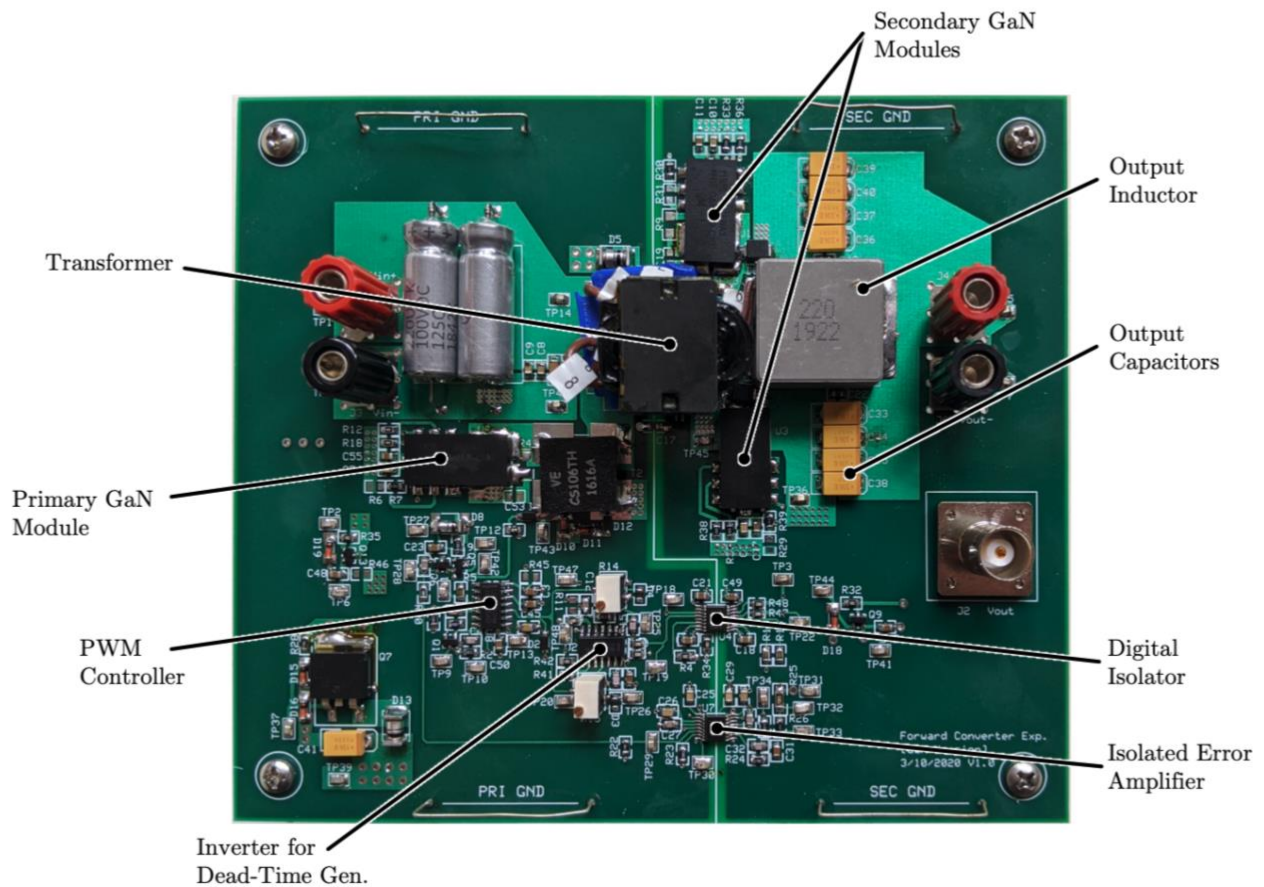
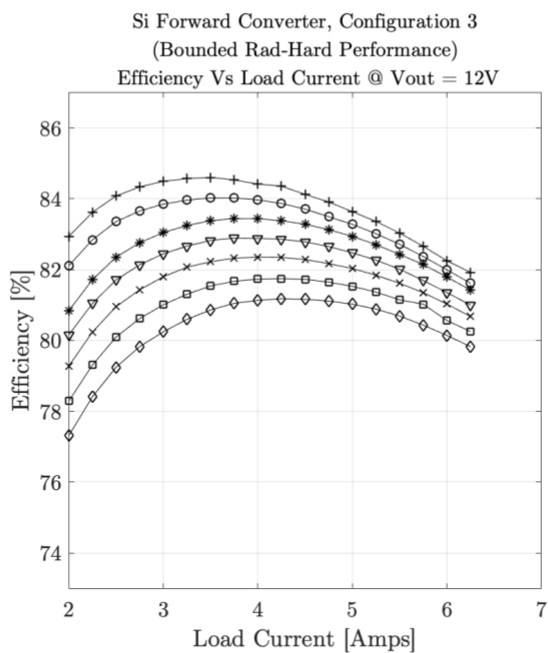
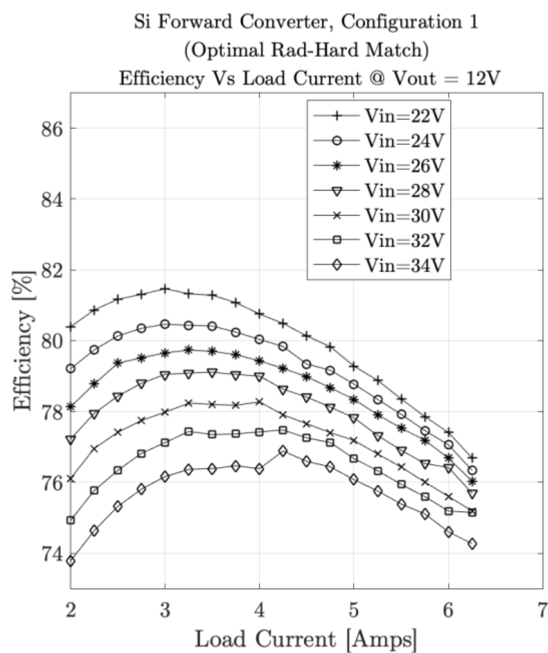


Figure 24 GaN Based Forward Converter Hardware





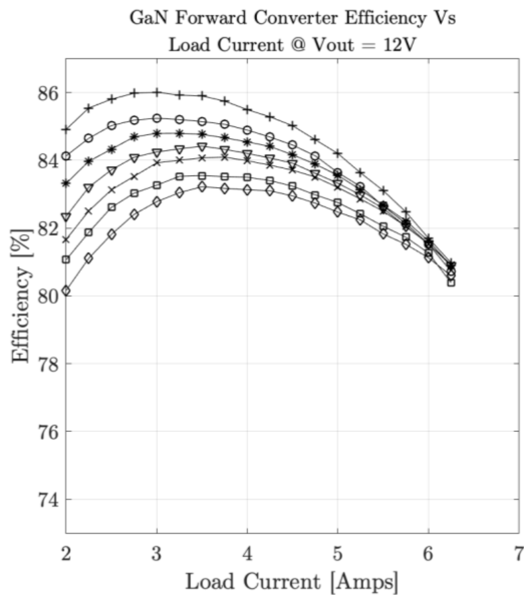


Figure 25 Efficiency Plots from the Implemented Converters

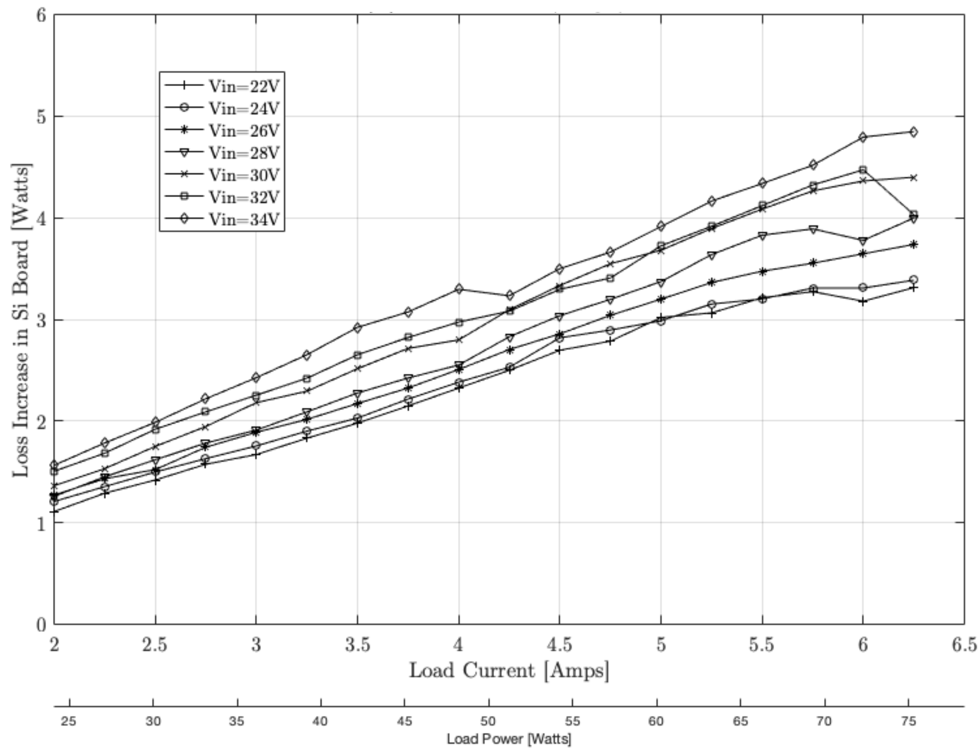


Figure 26 Loss Differential Between Si Converter (Config. 1) and GaN Converter

The converter efficiency plots shown in Figure 25 were captured by using the voltage sense lines of a Rigol DL3021 electronic load and a Tektronix TCP0030A current probe. Input current measurements were taken and averaged by a MSO64, 2.5Ghz, 25GS/s oscilloscope. The converter input supply was a BK precision 9183B.

As predicted by the analytical loss model, configuration 2 for the Si based converter had large losses on Q_1 at output currents of 5A or above. This led to a thermal runaway condition at these power levels, which is why configuration 2 results are omitted from this results section. Its mention is still valuable given that the it proves loss model accuracy.

Configuration 1, which matches the optimal Si FET from the radiation-hardened pareto-optimal front with a commercial device, had a peak efficiency of 81.47%. The GaN converter's peak was 86.01%. Both the Si board under configuration 1, and the GaN board hit peak efficiencies at the minimum input voltage condition, $V_{in} = 22V$ and the 3A load condition, $P_{out} = 36\ W$. Shown in Figure 26 is a graph of the loss differential between these two boards. At high loads the Si converter's relative loss increases significantly. This is an effect of the conduction losses becoming the dominant loss mode in the system, and growing more rapidly in the Si FETs. Thermal effects could have a strong influence here too, as GaN devices have a smaller temperature dependence on $R_{ds(ON)}$, and are likely operating at a smaller junction temperature to begin with. Also seen from Figure 25, is that the relative loss increases with larger input voltages.

The effect of converter sensitivity to input voltage can also be seen from gap size between lines on the efficiency plots. The Si converter (configuration 1) had an average of $-0.35\%\ per\ V_{in}$ and a total efficiency range differential of 7.68%, whereas the GaN board had $-0.2\%\ per\ V_{in}$ and 5.85%, respectively. At high input voltages, the low duty cycle reduces conduction losses in Q_1 and Q_2, but increases them in freewheeling FET Q_3. Additionally, the dynamic losses on Q_1, and Q_3 grow significantly with input voltage. Although snubber losses did grow with both load current and input voltage, the networks were tuned to reduce overshoot to the same level, which required the same capacitor values and slight changes in resistor values, which made snubber losses similar across the two boards.

As seen from Figure 17, the Si FETs used in configuration 3, which yield an absolute bound on predicted rad-hard performance, had an $R_{ds(ON)}$ value very close to the selected eGaN HEMTs. By greatly normalizing the conduction losses, the results of Si configuration 3 give an intuition to the magnitude of dynamic losses occurring in the Si switches. The peak efficiency values differ

by 1.41%, and the mean sensitivity to input voltage is $-0.29\%\, per\, V_{in}$. Remember that configuration 1 uses FETs that don't match with any available radiation hardened part. It is only used as an absolute error bound on the matching process for configuration 1. We expect that using the real radiation hardened plots would produce curves that are much closer to that of configuration 1 than configuration 3.

Another feature of the plots on Figure 25, is the tendency of the GaN converter's efficiency values to converge to a narrow range at high load levels, despite the input voltage. Although this can be seen to a lesser degree in the Si converter plots, it's significantly more pronounced with the GaN devices. In general, the increase in input voltage brings higher dynamic losses. The convergence is due to the ratio between dynamic and conduction losses. For the GaN converter, conduction losses dominated the ratio at higher loads (70.3%) of Q_1, and the separation between input voltage became less influential. The Si converter withheld more of a balance, thereby maintaining some degree of separation. Note that the trend of Figure 26 still holds true in that Si conduction loss rose faster than GaN conduction loss, however, here we are discussing the ratio between the two loss modes in each board.

The switch node waveforms shown in Figure 27 are a testament to the similarity between the two board designs, and the consistency of the voltage spike events caused by transformer leakage, and reverse recovery in the diodes. It was hypothesized that the faster slew rates of the GaN devices would cause the waveforms to significantly diverge, but once the snubber networks were implemented, overshoot and ringing duration had a high degree of similarity. There is a small delay after the voltage spike on the primary switch node, and before the core reset event that causes the primary switch voltage to double. Capacitance from the snubber network, or from components Q_1 or Q_2 / D_1 would contribute to this delay, which is why the selection for Q_2 had a

C_{oss} requirement. Although additional capacitance at the secondary switch node typically reduces the overshoot, it was found that when Q_3 took on large C_{oss} values the overshoot became highly load dependent. This may be due to the added capacitance 'charging' the leakage inductance in a similar way to the diode reverse recovery process when Q_1 closes. After all, a Schottky diode does not have true reverse recovery charge, but undergoes a similar process due to a combination of output capacitance and its ring guard structure. Regardless, this is the origin of the C_{oss} requirement on Q_3, which is mentioned in the FET selection section. For additional waveforms and parameters that compare basic converter functionality see Figure 28 and Table 6.

The only divergent values from table 6 between the two converters came from the load step test, which issued a 2A step at a 0.25 A/uS slew rate. Intuitively, the GaN converter would have a better response given that the energy is more efficiently converted from input to output. However, it is suspected that part variance stacked up in a significant way to make the response worse. Bulk capacitance or the passive values forming the compensation network are prime suspects.

Table 6 Basic Converter Characteristic Comparison

	Si Converter (Configuration 1)	GaN Converter
Output Ripple (mVpp)	25	32
Turn on Rise time (mS)	13	15
Load Step Voltage Sag (mV)	150	200
Overshoot on Q1 (V)	48	41
Overshoot on Q3 (V)	35	39
Duty Cycle at nom op. (%)	26.2	27.6
Dead Time (nS)	149	154

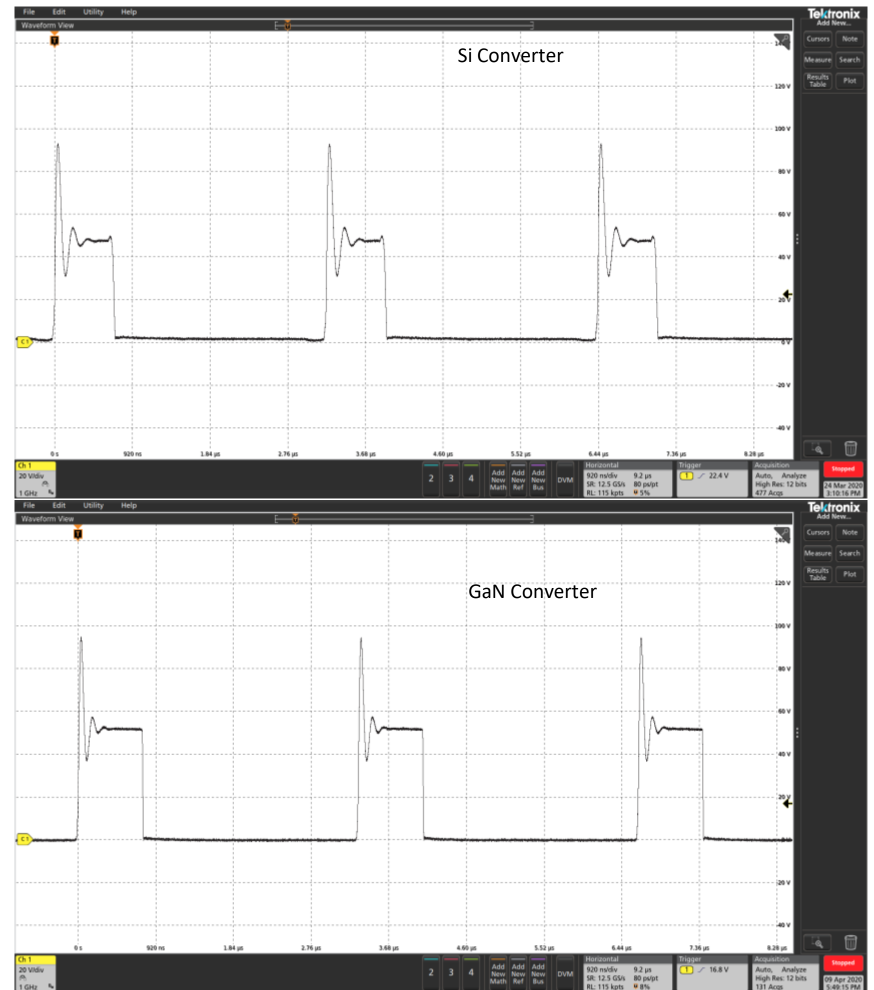
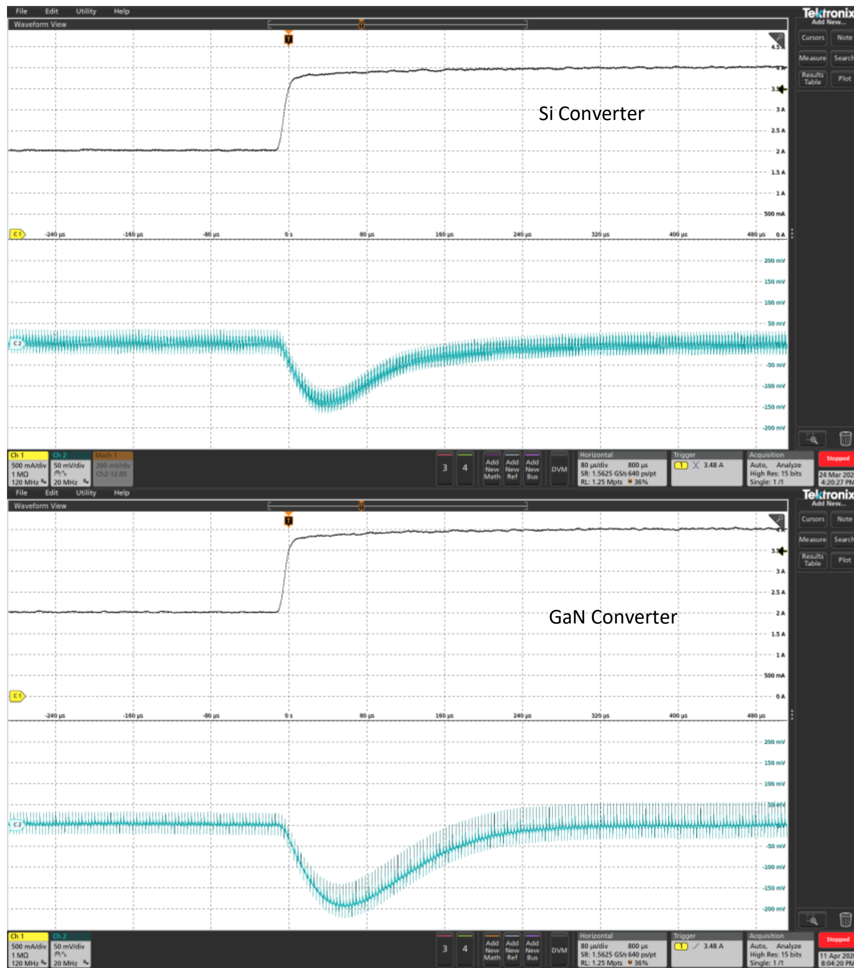


Figure 27 Switch Node Scope Capture Waveforms, Q1 Drain (Left), Q3 Drain (Right)



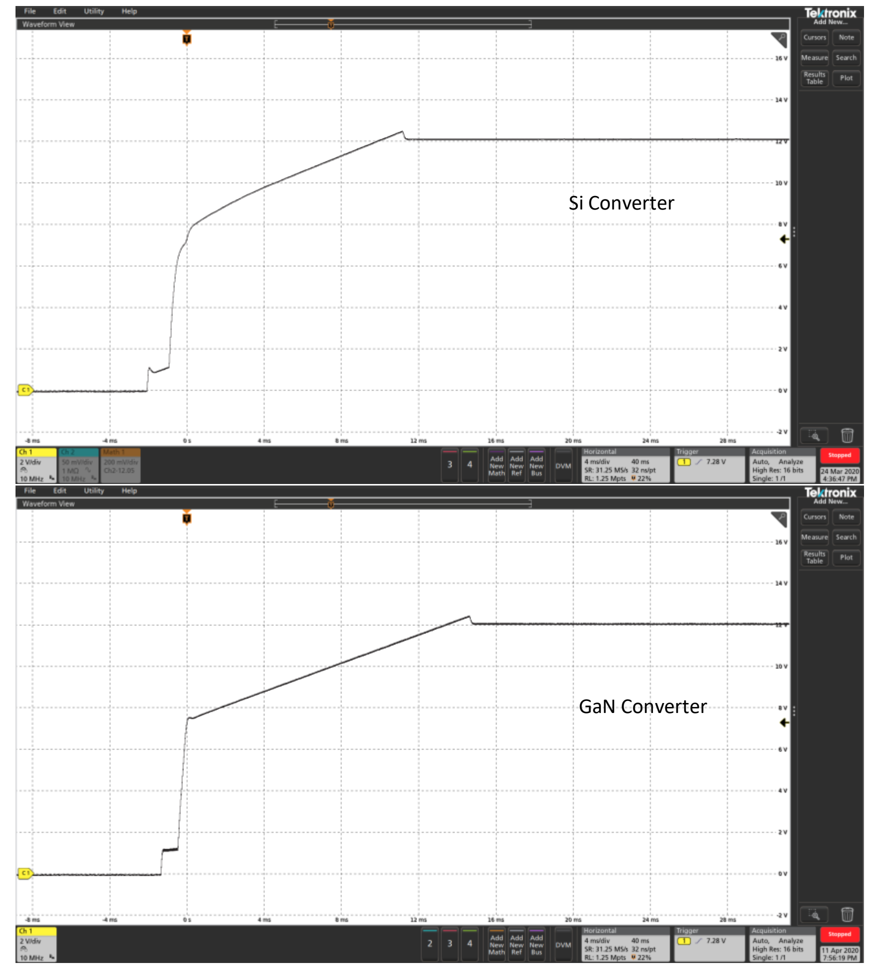


Figure 28 Transient Response Scope Capture Waveforms, Load Step (Left), Startup Output (Right)

6.0 Discussion

The commonality of the forward converter within the scope of purchasable radiation hardened isolated power supply units, made the topology an ideal platform for this study. Although the rigorous FET selection process, including the error bounding methods, lead to a sound baseline Si based converter build, it is still valuable to compare the baseline results to the mentioned purchasable power supplies. As stated in the introduction, when three of the major radiation hardened SMPS manufactures (Infineon, VPT, Microsemi) were polled for their available isolated converter solutions (TID>100kRads Si, See > 80 MeV-cm2/mg), thirty out of the thirty-nine results used forward converter topologies. From those thirty forward converters, the mean efficiency was 81.71% (*Max* = 86%, *Standard Deviation* = 2.39%), with the average maximum output power landing at 45.3W (*Max* = 100W, *Standard Deviation* = 22.15W). The Si based forward converter built in this study achieved a peak efficiency of 81.47% putting it in an extremely comparable position to the market available average, and making the GaN results easily applicable to manufacturers.

The results section has been heavily biased towards the efficiency metric when drawing conclusions from this comparison study. The fundamental reason for this is that power density is largely limited by the radiation hardened PWM controller. GaN's fast edge rates mean high switching frequencies can be achieved, and the size of the power magnetic components can be greatly reduced. However, without a high speed PWM controller, these power density increases won't be seen. The future of space power conversion does point in that direction, but this study is concerned with current standards. Even without the magnetic size reduction, we do see a minor improvement when comparing the board area needed for the Si driver and FETs versus the GaN

integrated module. The package types and sizes can be seen in Table 7. Note that we are considering the optimal Rad-Hard configuration, and not the COTS matched components, where $Q1$ is populated by IRHNS57260SE, and $Q2/Q3$ by IRHNJ67134. The result is 13.65% percent difference in terms of board area between the Si and GaN selections. While this is an improvement, the GaN/driver integration limits the size capability. In the commercial space, GaN FETs from EPC, GaN systems, and many more, showcase very power dense switches. Until more space-rated GaN devices and high-speed PWM controllers become available, power density will always be secondary to efficiency.

Table 7 FET/Driver Package Comparison

	Optimal Si Rad Hard MOSFET A (IRHNS57260SE)	Optimal Si Rad Hard MOSFET B (IRHNJ67134)	Rad Hard Si Gate Driver (ISL7442BRH)	Rad Hard eGaN Module (FBS-GAM01-PC100)
Package Type	SupIR-SMD	SMD .5	CDFP4-F16	Custom
Area in^2	0.376	0.120	0.182	0.285

In conclusion, the GaN based forward converter showed a major improvement in peak efficiency (4.54%), and a tighter efficiency range over the span of input voltages and output currents. This improvement is highly accurate due to the employed methods used to create the baseline measurements, which represented the best-case radiation hardened silicon forward converter.

Appendix A Full Schematic References

On the follow pages are the detailed schematics. Note that there are a few minor differences between the GaN and Si based schematics other than the FET / Driver symbols. The Si based board was built first, and used as a prototype to prove basic forward conversion functionality, so there included optional selective population schemes. The largest difference involves the option to use the auxiliary winding instead of the pure linear regulation strategy for the logic supplies. The supply powered from that winding would have the ability to shut down the linear regulator via the startup circuit shown in Figure 32. Note that the auxiliary winding and the startup circuits were not used when evaluating Si converter performance. A second difference is the location of the current sense transformer. The GaN modules required the FET source node to be directly connected to power ground, making us relocate the current sense transformer to the high side of the switch. All indications by the recorded waveforms showed no difference in performance due to this change. Parallel FET footprints were included on the Si board, but an analysis of this option was never pursued, and a single FET in each position was only ever populated. Finally, there are some minor differences in the dead time generator such that the Si board housed fixed resistor/capacitor SMD component changes instead of the easily adjustable potentiometers, and an AND gate logic chip, which proved to have negligible power dissipation.

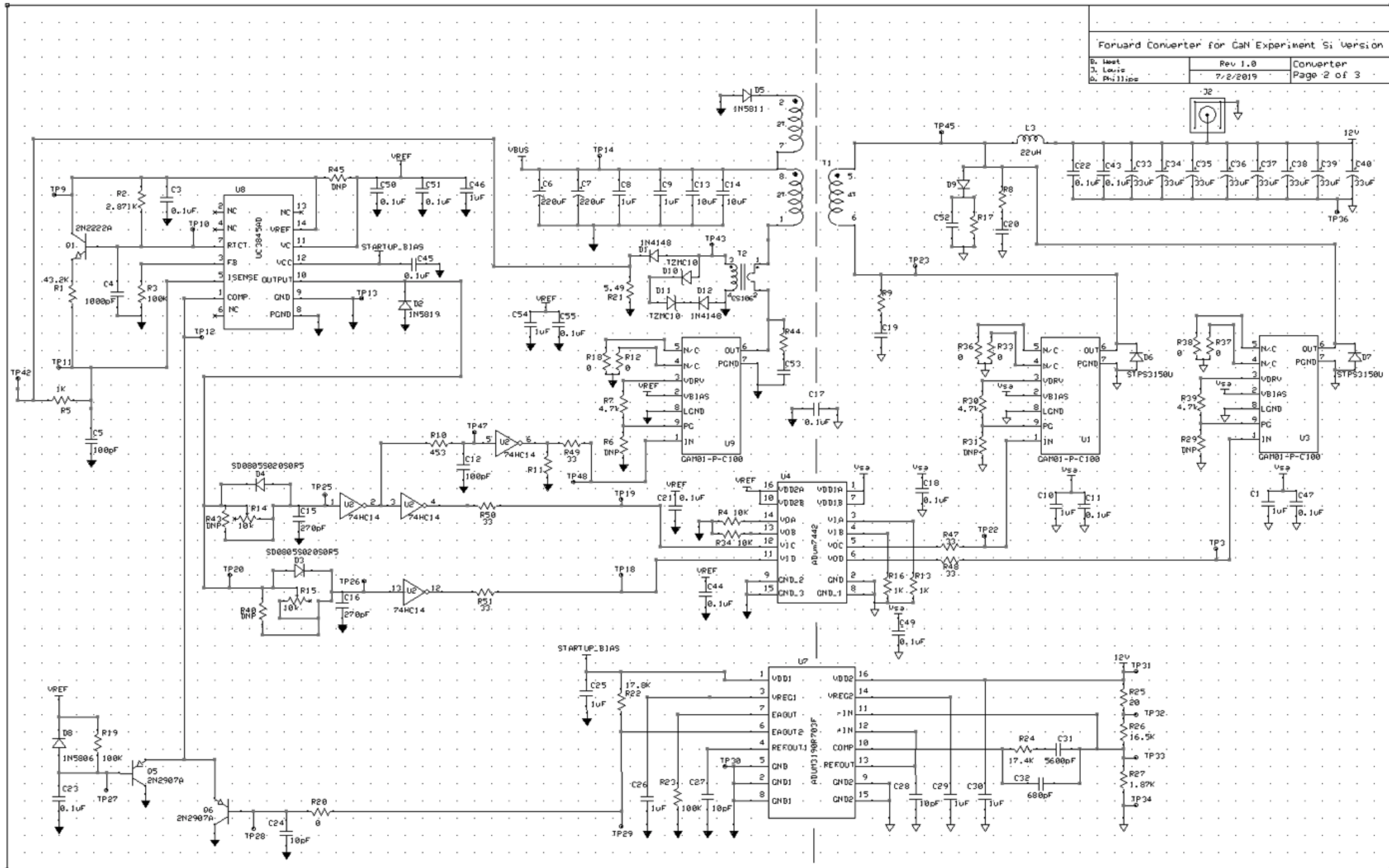
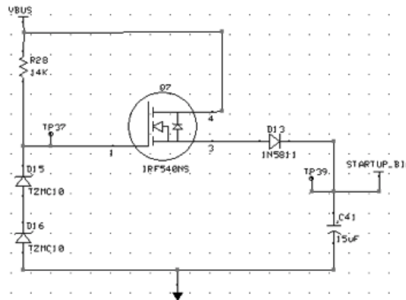


Figure 29 GaN Converter Detailed Schematic Page 1

Forward Converter for GaN Experiment Si Version

B. West J. Lewis A. Phillips	Rev 1.0 7/2/2019	Linear Regs. & Startup Page 3 of 3



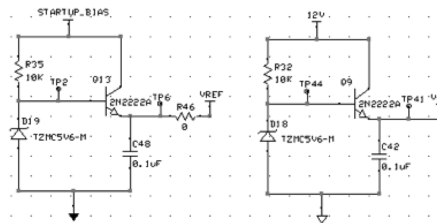


Figure 30 GaN Converter Detailed Schematic Page 2

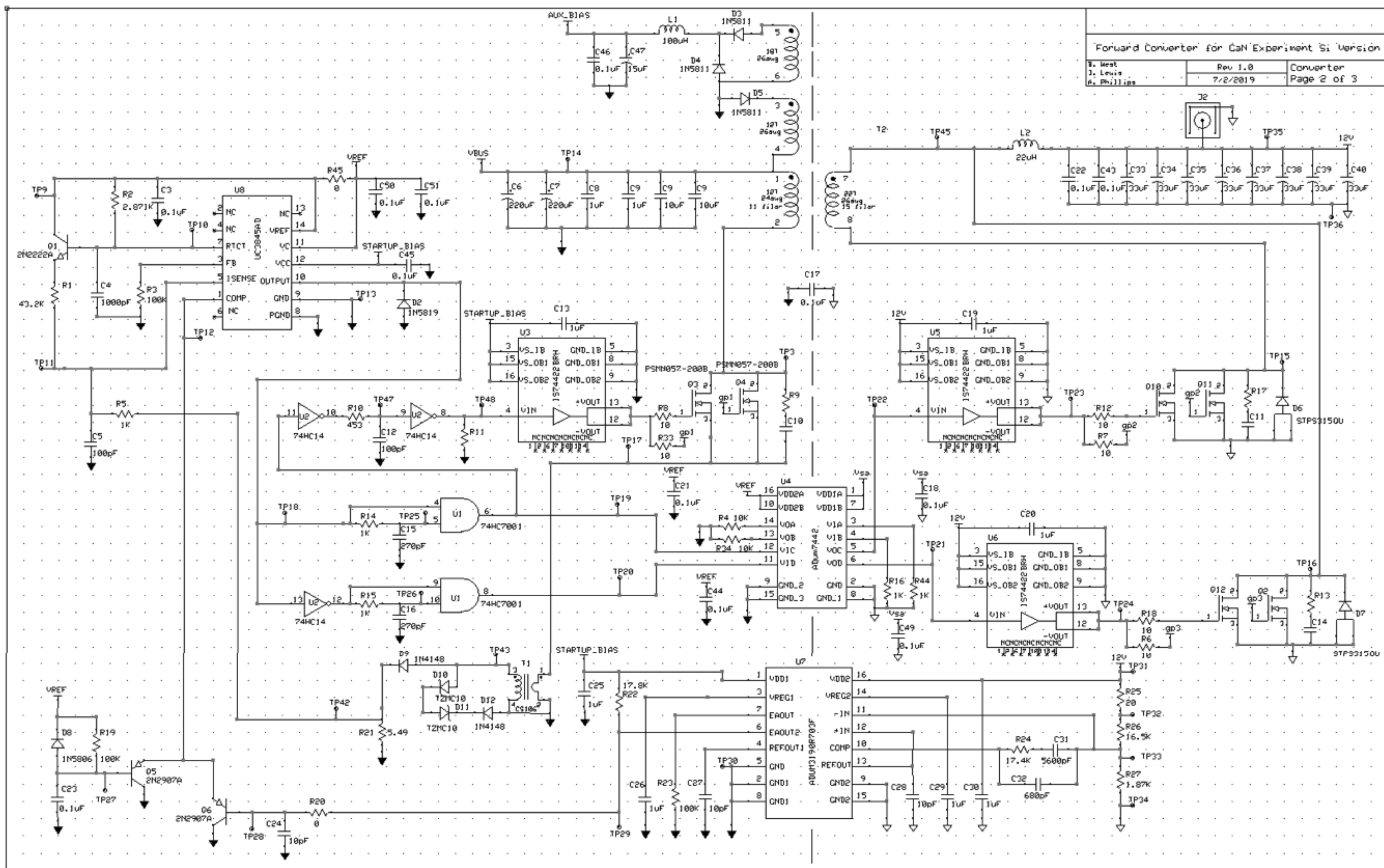
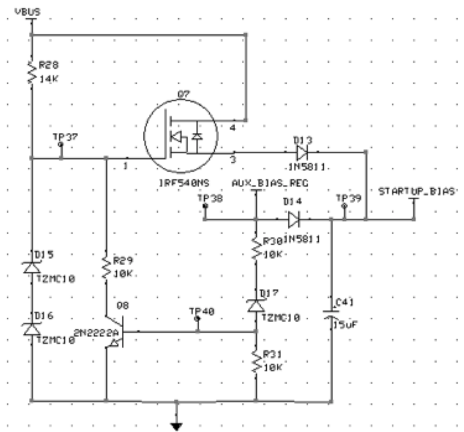


Figure 31 Si Converter Detailed Schematic Page 1

Forward Converter for GaN Experiment Si Version		
B. West J. Lewis A. Phillips	Rev 1.0 7/2/2019	Linear Regs. & Startup Page 3 of 3

STARTUP CIRCUIT



LINEAR REGULATORS

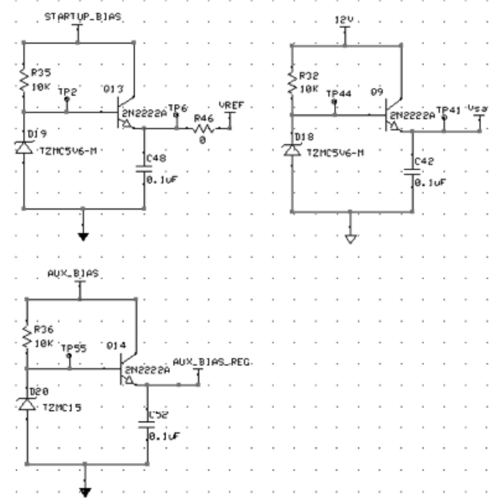


Figure 32 Si Converter Detailed Schematic Page 2

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