A 5.0 GHz ACTIVE INDUCTOR CURRENT CONTROLLED OSCILLATOR

by

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LIST OF SYMBOLS

ω	Resonant frequency , carrier frequency
ω_m	Offset frequency
φ	Phase shift
A_{DC}	DC gain of CMOS transistor
C	Generic capacitance
Cgs	Gate to Source capacitance
Cgd	Gate to Drain capacitance
L	Inductance
Cp	Parallel capacitance
Cs	Series Capacitance
Lp	Parallel Inductance
Ls	Series Inductance
F_t	Frequency of CMOS unit current gain
C_{ox}	Oxide capacitance
P_{RF}	RF power
PN	Phase noise level
Q	Quality factor
Qo	Unloaded quality factor
R	Generic resistance
r_g	Gate resistance
Rp	Parallel Resistance
Rs	Series resistance
r_{ds}	Drain to source resistance
g_m	Transconductance

I_B	Bias current
I_D	DC Drain Current
i_d	AC Drain current
T_d	Delay through delay cell
g_{ds}	Small Signal Output Conductance

LIST OF ABBREVIATIONS

CCO	Current Controlled Oscillator
CMOS	Complementary Metal Oxide Semiconductor
DLL	Delay Locked Loop
FOM	Figure of Merit
GHz	Giga Hertz
LC	Inductance Capacitance
LO	Local Oscillator
MHz	Mega Hertz
MICS	Medical Implantable Communication Service
NMOS	n-channel Metal Oxide Semiconductor
PMOS	p-channel Metal Oxide Semiconductor
PLL	Phase Locked Loop
RLC	Resistance Inductance Capacitance
VCO	Voltage Controlled Oscillator

PENGAYUN TERKAWAL ARUS INDUKTOR AKTIF 5.0 GHz

ABSTRAK

Permintaan untuk komunikasi tanpa-wayar dalam bidang suara dan data telah berkembang pesat. Tahap integrasi sistem pemancar-penerima radio frekuensi (RF) telah menjadi sangat rumit dan usaha untuk menangani hal ini telah meningkat hampir secara eksponen. Komunikasi RF pada masa kini memerlukan sistem yang amat pantas untuk aplikasi-aplikasi laju sperti 4G and 5G, julat penalaan yang lebar bagi pelbagai aplikasi, ralat masa yang minimum dan kos yang rendah. Pengayun memainkan peranan yang mustahak dalam menentukan kualiti sistem perhubungan RF. Kebanyakan pengayun adalah berdasarkan voltan dan dikenali sebagai VCO (Voltage Controlled Oscillator) dan terdiri terutamanya daripada dua jenis, iaitu pengayun tangki LC dan bukan tangki LC. Yang pertama amat baik untuk hingar-fasa yang rendah disebabkan pengunaan induktor pasif. Yang kedua seperti pengayun cincin adalah jauh lebih kecil saiznya daripada tangki LC, dan dengan itu lebih rendah kosnya, tetapi mempunyai hingar-fasa yang lebih tinggi. Walau bagaimanapun, sumber arus menjadi lebih popular dan digunakan dalam pengayun untuk membentuk pengayun terkawal arus (CCO) disebabkan oleh frekuensi yang lebih laju berbanding sumber voltan. Dengan itu, matlamat projek ini adalah untuk mereka pengayun terkawal arus yang boleh menjana frekuensi tengah 5 GHz, julat penalaan 500 MHz dan hingar-fasa yang lebih baik dari -110 dBc/Hz dengan menggunakan induktor aktif. Untuk menzahirkan konsep yang dicadangkan, pengayun cincin 5-peringkat dengan induktor aktif yang dikawal oleh litar mod arus telah direka bentuk dan disimulasi menggunakan teknologi CMOS 180 nm daripada Silterra. Projek ini diteruskan dengan

mengesahkan dan membuat penambahbaikan kepada parameter prestasi asas reka bentuk pengayun tempatan yang menggabungkan laluan dwi lengah, lengah pencong negatif, sumber arus, transistor terganding silang dan induktor aktif. Analisis dilakukan tentang bagaimana transistor terganding silang memainkan peranan dalam mempengaruhi corak operasi frekuensi yang tersendiri. Keputusan simulasi menunjukkan bahawa frekuensi operasi maksima pengayun adalah pada 5.81 GHz. Transistor MOS terganding silang dan induktor aktif dikawal oleh sumber arus telah membantu dalam memperbaiki hingar-fasa dan frekuensi pengayun. Pelbagai keputusan simulasi menunjukkan bahawa julat frekuensi pengayun 5-peringkat ini adalah antara 3.87 GHz hingga 5.81 GHz. Parameter kritikal sesuatu pengayun, iaitu hingar-fasa, ialah -113.2 dBc/Hz pada ofset 1 MHz dengan frekuensi tengah 5.81 GHz. Prestasi reka bentuk baru ini telah meningkat, secara umum, sebanyak 36% bagi frekuensi manakala 8% bagi hingar-fasa, apabila dibandingkan dengan topologi bukan tangki LC. Selain daripada frekuensi dan hingar-fasa, kuasa-keluaran dan saiz reka bentuk ini adalah 9.41 dBm dan 0.22 mm^2 masing-masing. Ini merupakan peningkatan sebanyak 53% bagi kuasa-keluaran dan 33% bagi saiz apabila dibandingkan dengan toplogi bukan tangki LC. Kesimpulannya, reka bentuk ini berjaya mencapai sasaran-sasaran yang telah ditetapkan pada permulaan penyelidikan ini.

A 5.0 GHz ACTIVE INDUCTOR CURRENT CONTROLLED OSCILLATOR

ABSTRACT

The demand for wireless communications in the field of voice and data has rapidly grown. The integration level of Radio Frequency (RF) transceiver systems have become very intricate and efforts to deal with this has risen almost exponentially. Communications nowadays require system with extreme speeds to cater for high speed applications such as 4G and 5G, wider tuning range to cater for variety of applications, minimal timing errors and lower cost. Oscillators play the key role in determining the quality of the RF communications system. Most oscillators are voltage based and known as Voltage Controlled Oscillator (VCO) and comes mainly in two types, which are LC Tank Oscillators and Non LC-Tank Oscillators. The former is very good for lower phase noise due the usage of passive inductor. The latter such as ring oscillators are much smaller in size than LC-Tank, thus lower cost, but exhibit much higher phase noise. However, current sources are becoming more popular and employed in oscillator to form Current Controlled Oscillator (CCO) due to its higher frequency as compared to voltage source. Hence the goal has been put forth to design a CCO that produces 5 GHz center frequency, tuning range of 500 MHz and with phase noise better than -110 dBc/Hz by employing active inductor. To demonstrate the proposed concept, 5-stage ring oscillator with active inductor design controlled by a current-mode circuit, were designed and ran through simulation using 180 nm CMOS technology provided by Silterra. The work proceeds to validate and make improvements to the fundamental performance parameters of a local oscillator design that incorporates dual delay path, negative skewed delay, current source, cross-coupled

transistors and active inductor. Analysis were done on how the cross-coupled transistors play a role in affecting the distinctive frequency operation pattern. Results from the simulation show that the oscillator's maximum frequency obtained without distortion is 5.81 GHz. The cross coupled MOS transistors and active inductor controlled by current source aided well in improving the oscillator's phase noise and frequency. Various simulation results show that the frequency range of this 5-stage oscillator runs between 3.87 GHz to 5.81 GHz. The critical parameter of any oscillator, which is the phase noise, is -113.2 dBc/Hz at 1 MHz offset with a center frequency of 5.81 GHz. The performance of this new design has improved, in general, about 36% on the frequency while 8% on the phase noise as compared with the non-LC Tank topology. Apart from the frequency and phase noise, the output power and size of this design is 9.41 dBm and 0.22 mm^2 respectively. This is an improvement of 53% on the output power and 33% on the size when comparing with the non-LC Tank topology. Conclusively this design has successfully achieved the goals set forth for this research.

CHAPTER ONE

INTRODUCTION

1.0 Background

In this era, most of modern communication systems' timing information, be it in the form of clock signals or oscillator signals, it plays a very critical role in the system's performance. Clock or oscillator signals, in most of such applications, are in fact used to drive sampling circuits or mixers. This is because the instant variations in the sampling, no matter systematic or random are very crucial performance parameters. Local oscillator provides the timing information for some systems. At times the timing information is provided by timing source that is from external source. When this happens, it's critical to minimize the timing errors. This cannot be done without minimizing the noise from the buffering and distribution of clocks in the whole system. Quite a numerous different applications possibly require a clock that is local, having different frequency or different phase. Such requirements can only be delivered by a Phase-Locked-Loop (PLL) or circuits that a very similar to PLL. As explained earlier, minimizing the timing error in such PLL systems should be the primary focus. For this, a very careful attention in understanding all of the noise sources within the PLL and its interacting circuits as a whole is extremely crucial. Due to this very reason, PLL applications are very complex and challenging in achieving superior performance level. Timing error sources are the worst enemy in PLL systems but employing correct techniques will help to alleviate or minimize the issues. PLL is used for data and clock recovery in systems such as disk drive, optical communication and local area networks.

There are also some other systems that use PLL for synthesizing the frequency. These systems include radio receivers and transmitters. Microprocessors, Digital Signal Processors and Network routers are more complex systems in which the clocks are synchronized, primarily to minimize clock-skew, using either a PLL or DLL (Delay-Locked-Loop). Timing errors are often known as timing uncertainty in communication systems and it comes in several types. However, the most important one is the phase noise, also known as timing jitter. It is nothing but the sampling error or more precisely the random variations in the sampling phase of a signal. The source for this phase noise/timing jitter is the 1/f and thermal noise in the active and passive devices that are part of PLL system's components, particularly the voltage-controlled-oscillator (VCO).

Another source for this sampling phase systematic variations is the AC variation that happens in phase. This is called spurious tones. This occurs when signals inject through the other parts of the circuit. Phase shift/drift or frequency offset can be caused by abrupt changes in the substrate. Advanced circuit methods or techniques are often employed to minimize these noise sources. However, the performance of such advanced circuits get limited by thermal noise of the device, which is very fundamental in RF systems. To offset or overcome the noise effect and to boost the optimal performance of RF applications of frequency synthesis, a Low-Phase-Noise oscillator provides the rescue. This kind of oscillator often formed by an external resonator which is nothing but a high quality factor ("Q") varactor tuned LC-tank. Nevertheless, most RF applications are now desiring a conventional oscillator that is fully-monolithic. Monolithic designs integrate a large numbers of transistors built on single semiconductor base material making it much smaller in magnitude but faster and

cheaper of those discrete electronic components. But it brings its own set of issues because the timing errors described above is now more prone to occur and can easily be generated from various means and becomes a bigger threat. The high-Q external resonator that was once the problem solver can no longer now be used. Designing a monolithic oscillator becomes more difficult and complex. New circuit techniques such as using current source instead of voltage source, active inductor as opposed to passive inductor need to be implemented on chip to tackle these problems.

Voltage-controlled delay chain and ring-oscillators are now abundantly available as on-chip for the clock recovery and synthesis applications. These on-chip applications have greatly reduced not only the cost but also the complexity of the systems. However, these applications have very restrictive phase noise requirements and raising questions of these on-chip designs' applicability and performance for RF frequency synthesis. Current-controlled oscillator, on the other hand, has become more attractive due to its faster frequency as compared to voltage controlled (DiClemente and Yaun, 2006). CCO also helps greatly in improving the noise performance due to the steady state flow of current.

This thesis explains the oscillator fundamentals, performance limit due thermal noise in ring-oscillators and their suitability or applicability to RF frequency synthesis systems. It further describes the design techniques and approaches for very low phase noise and/or low timing jitter circuits, which are technically the basis to most RF applications. The dissertation explores the trade-offs at the buffer/delay (Eken and Uyemura, 2004) and/or at the oscillator level that a designer can avail. Even options at PLL level is analyzed in this thesis. The merits of CCO versus the popular VCO are

explained. In addition, this thesis explains the desire of a monolithic oscillator in the frequency synthesizers design in radio receivers. Detailed comparisons of the overall features of the proposed design are made with other designs including those with on-chip LC-tuned circuits (Zito et al., 2012).

1.1 Problems Statements

Looking back at the earlier Section 1.0, it is clear that minimizing the timing errors in RF circuit by improving the noise performance has been a key problem to tackle. Moreover, communications system nowadays require extreme frequency, for example, 3G and 4G. Hence circuits that can provide a high frequency has been a crucial desire as well. Along with high frequencies, lower phase noise is also of a dire need. Using passive inductors to achieve this has been a norm. Works by Chahaboor and Gonoodhi (2017), Elkholy and Entesari, 2017 and Allesandro and Ippolito (2012) are some references that employs huge passive inductors. However, these inductors need to be available in smaller size preferably resulting several nH such that the cost is lower. Unfortunately spiral or passive inductors typically are not small hence alternate to this passive elements are desired. Thus, implementation of active inductors are recommended. Monolithic integration of the CCO with active inductor in place of VCO, could greatly enhance the performance of the oscillator in the aforementioned aspects. Works by Ma et. al (2013) and DiClemente et. al (2008) are some good references on this front.

1.2 Objectives

The objectives of this project are:

- To design an oscillator that operates at 1.8 V and controlled by current source instead of voltage source – making it Current Controlled Oscillator (CCO)
- To design a CCO that produces a high speed oscillation preferably up to 5 GHz
- To design a CCO with a wide tuning range, preferably 500 MHz
- To design a CCO with active inductor instead of passive (spiral) inductor to boost the phase noise, preferably lower than -110 dBc/Hz
- To design a CCO that dissipates very low power preferably lower than 10 mW

1.3 Thesis Scope

This thesis is confined to the following scope:

1. Extensive study of active-inductor and passive-inductor on their advantages and disadvantages with respect to their overall performance, cost and complexity. The success of replacement of an active inductor in lieu of passive inductor. Passive inductors greatly help phase-noise but at the same time comes with distinct disadvantages as previously explained. Active inductor's performance has been very comparable to passive and provides the best of both worlds.

2. A very deep analysis on possible techniques to generate higher and wider operating frequency and range of operating frequency respectively. The deep analysis helps us research through the performance of various techniques and

to settle on one that is most optimum by all means. A thorough comparison on CCO versus VCO will also be provided which is used to eventually to prove that CCO is far better performing design as compared to VCO.

3. The post-layout design and implementation of ring CCO with active inductor. The design will use non LC_tank ring topology using the above mentioned techniques, including issues such as coarse and fine tuning, maximum frequency of operation, and design of high frequency CCOs.
4. A detailed literature and simulation work performed on voltage controlled versus current controlled circuit was also carried out. Simulations were using Cadence HSPICE on Silterra 180 nm process.

1.4 Thesis Outline

This thesis describes the design and analysis of a high frequency oscillator that integrates active inductor for phase noise improvement and current controlled circuit for added frequency and range. Objectives of this work and the scope and outline of this thesis has been explained thus far.

Chapter Two walks us through the fundamentals of an oscillator and the challenges that they come with. It also introduces to the many types of oscillators and their respective challenges. Alongside the challenges, the chapter also gives us a peak on thus far solutions invented and proposed by many well-known scholars for these very challenges.