Asymmetrical Load Resistance Operation of Four Channel DC-DC Buck-Boost Converter

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***Abstract*—In this paper the asymmetrical load resistance operation of a previously proposed five level Buck-Boost converter is examined in discontinuous current conduction mode. The analysed converter has two input and four output channels, providing four identical or different voltage levels at the outputs. Asymmetrical load operation is carried out under steady state conditions. Control characteristics are examined to maintain an operation strategy for the asymmetrical load cases. Several operation points are examined in order to demonstrate two control strategies in which two switching angles or the voltage of the capacitor and the inductor current are the chosen parameters that help to set the required output voltages. Advantages of the proposed strategy for the four channel converter are the soft switching, which help to achieve improved performance and high efficiency. Possible application fields are DC nano-and microgrids and multi-level inverter drives.**

***Index Terms*—multilevel converter, asymmetrical operation, steady state analysis, control strategy, Buck-Boost converter**

I. Introduction

In DC nanogrids, different parts can be connected by several two level converters, however, it is cheaper and easier to realize a smart control strategy by using a multilevel converter instead [1]. On the other hand, multilevel converters can also have disadvantages, such as the complex topology, and the wide number of switches, that also leads to higher switching losses. This made the researches to aim towards developing cheaper, less complex converters, while also reducing the number of switching devices as much as possible.

Multilevel converters can be classified based on different aspects. Two main groups are resonant converters and the converters which consist of transformers, on the other hand the combination of these two are also very common. A three-level LLC (two inductor -one capacitor) series resonant converter allowed wide input/output range under low frequency scale consisting only one magnetic component. It also provided zero voltage switching (ZVS) for the main switches and zero current switching (ZCS) for rectifier diodes [2].

Recently, several multilevel converters were proposed consisting of a transformer which provided both ZVS and ZCS [3]–[5]. Leakage energy of the two transformers was recycled by a special dual DC-DC flyback converter consisting of one active switch only. During the turn-on period, primary windings of the transformers stored energy, that was released through the secondary windings during the turn-off period [6]. The energy of the leakage inductance of the coupled inductor was recycled to allow higher conversion efficiency, while was also supported by minimizing the number of switches to one in [7].

Efficiency of the modular multilevel converters can be improved by implementing a resonant tank to the circuit [8]–[10]. ZVS of the switches and ZCS of the output diode was achieved in a secondary resonance half-bridge converter. In the basic circuit an inductive filter was also included to reduce the output current ripple of the converter [11]. A multi-output current resonant modular converter provided three voltage levels (5V, 10V and 20V) without the intercommunication control between the receiver and the charger for charging electric devices (like laptops and phones) without the use of AC/DC adapters [12].

The proposed converter types however each have their drawbacks. Modular models require large and expensive transformers. Two level converters might operate with harmonic distortion that affects the performance of the load. These harmonics can be reduced by applying filters, or operating at higher frequency shifting the high-frequency harmonic orders. On the other hand increased frequency can lead to increased losses. Using multilevel converters can not

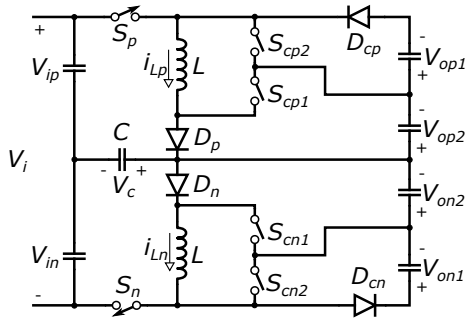

Fig. 1. Topology of the Examined Four Channel Buck-Boost Converter [13]

only decrease the harmonic elements, but they also allow a cheaper and easier smart control strategy for the whole system.

The current paper examines the special asymmetrical operation of a five-level Buck-Boost converter introduced in [13], [14] that allows five producible voltage levels, consisting of only two inductors and one capacitor and six controlled switches. The case of asymmetrical load resistances is investigated, when input and output voltages are symmetrical, furthermore a special control strategy is also proposed. The paper is constructed as follows. Section II explains the operation of the converter briefly. Section III presents the analytical study, Section IV explains the analysis if the load resistances are asymmetrical. Section V proposes a control strategy for this case. Finally, Section VI shows the simulation results which support the theoretical considerations.

II. Topology and Brief Operation

The analysed Buck-Boost converter has a positive, p and a negative, n input channel and four output channels, p_1, p_2, n_2, n_1 (see Fig. 1). There is one controlled switch in both p and n input channels (S_p and S_n). Furthermore, there are two controlled switches S_{cp1}, S_{cp2} and S_{cn1}, S_{cn2} in $p1, p2$ and $n1, n2$ output channels respectively.

Brief operation of the converter is as follows (see Fig. 1 and Fig. 2): First, S_p is turned on ($1p$: $0 < \omega t \leq \alpha_p$, where $\omega = 1/\sqrt{LC}$), sinusoidal current i_{Lp} flows in circuit V_{ip}-S_p-L-D_p-C charging capacitor C from V_{cn} to V_{cp}.
In the next step ($2p$: $\alpha_p < \omega t \leq \alpha_{cp}$), S_{cp_1} is turned on (S_p is turned off), the energy of L supplies the circuit L-S_{cp_1}-V_{op_1}-D_{cp}. Here i_{Lp} is decreasing in a linear way, and there is no current flowing through the capacitor, $i_c = 0$, thus $v_c = V_{cp}$ constant.
Finally, S_{cp_2} is turned on (S_{cp_1} is turned off, $3p$: $\alpha_{cp} < \omega t \leq \alpha_{ep}$), the current flows in circuit L-D_p-V_{op_2}-S_{cp_2}. In DCM at the end of the switching period i_{Lp} becomes zero.
"Protection mode" is an additional operation mode (in both channels), when both diodes D_p and D_{cp} in the positive channel, start conducting if V_{cp}=(V_{ip}+V_{op_1}+V_{op_2}), the current i_{Lp} is flowing in circuit L-D_p-V_{op_2}-V_{op_1}-D_{cp}. This helps to prevent overvoltage across the capacitor terminals.

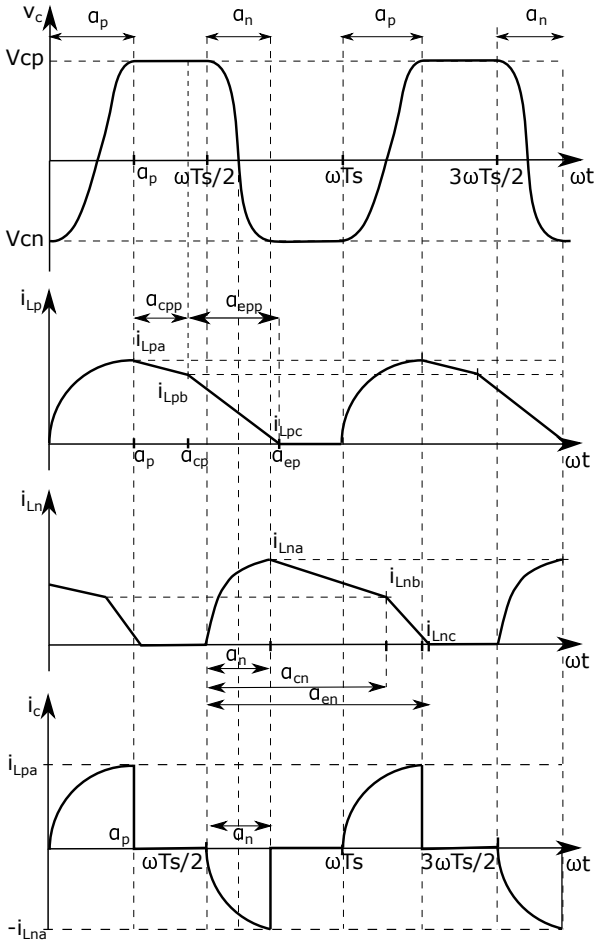

Fig. 2. Time Functions of Inductor and Capacitor Currents and Voltage [13]

Channel n of the converter operates similarly to channel p, shifted by a half period, $\omega T_s/2$, where T_s is the switching time. Further description of the converter operation can be found in [13]. Main advantage of the converter is that it only consists of two inductors and six controlled semiconductor switches, while being able to provide five voltage levels (four different or same voltages and zero). Furthermore, if operating in DCM, zero current switching of S_{cp2} and S_{cn2} is possible that helps to increase the efficiency of the converter.

Output voltages can be controlled by the pulse-widths of the controlled switches and the switching frequency $f_s = 1/T_s$. Switching angles can be calculated as follows: $\alpha_p = \omega t_{p_{on}}$. Duty ratios of the converter can be calculated from the switching angles, e.g.: $D_{Sp}[\%] = 100\alpha_p/360$, $D_{Scp1}[\%] = 100\alpha_{cpp}/360$ where $\alpha_{cpp} = \alpha_{cp} - \alpha_p$. Parameters of channel n can be calculated similarly with the following substitutions: $x_p \leftrightarrow x_n$ (except $v_{cp} \leftrightarrow -v_{cn}$), $x_1 \leftrightarrow x_2$ and $x_2 \leftrightarrow -x_2$.

Positive and negative sequence symmetrical components will also be applied, beside p and n channel variables (they are only introduced for voltages). The positive and negative sequence input voltages respectively are $V_{i1} = (V_{ip} + V_{in})/2$ and $V_{i2} = (V_{ip} - V_{in})/2$, the capacitor voltages in the positive

and negative sequence respectively are $V_{c1} = (V_{cp} - V_{cn})/2$ and $V_{c2} = (V_{cp}+V_{cn})/2$ (here V_{cp} and V_{cn} are the peak values of the capacitor voltages, where $V_{cn} < 0$).

In the provided steady-state case analysis, lossless components, ripple-free in- and output voltages are considered, commutation intervals between the semiconductor switches are neglected. During the analysis, the following per unit parameters will be used: $f_s^* = f_s/f_r$, $R_{p1}^* = R_{p1}/Z$, $R_{p2}^* = R_{p2}/Z$, $V_{c1}^* = V_{c1}/V_{i1}$, $I_{Lpb}^* = I_{Lpb}/I_{Lpa}$, $V_{op1,2}^* = V_{op1}/V_{i1} = V_{op2}/V_{i1}$, where $f_r = 1/(2\pi\sqrt{LC})$ is the resonant frequency and $Z = \sqrt{L/C}$ is the characteristic impedance.

III. Analytical Study

Steady state analysis is carried out on the control variables influencing the power flow between input $p-n$ and output $p_1-p_2-n_2-n_1$ channels. The relation among input and output variables is specified by the equations that describe the energy pulse transferred during one switching period, T_s. The analysis can be found in more detail in [14]. The current of capacitor C can be described by the well-known equation: $i_c = C\frac{dv_c}{dt}$, from where the input energy can be calculated considering that $\frac{1}{T_s}\int_0^{T_s} i_{op1,2}dt = \frac{V_{op1,2}}{R_{p1,2}}$ as follows. The input energy on channel p, w_{ip} is delivered by the current pulse $i_{cp} = i_{Lp}$ in the interval $0 < \omega t \leq \alpha_p$.

$$w_{ip} = V_{ip}\int_0^{\frac{\alpha_p}{\omega}} i_c dt = V_{ip}C(V_{cp} - V_{cn}) = 2CV_{ip}V_{c1} \quad (1)$$

The energy change of capacitor C can be calculated as follows:

$$\Delta w_{cp} = \frac{1}{2}C(V_{cp}^2 - V_{cn}^2) = 2CV_{c1}V_{c2} \quad (2)$$

Considering lossless operation as stated above, the energy stored in inductance L can be calculated by subtracting the energy change Δw_{cp} from the input energy w_{ip}:

$$w_{Lp} = w_{ip} - \Delta w_{cp} = 2CV_{c1}(V_{ip} - V_{c2}) = \frac{1}{2}L(I_{Lpa}^2 - 0) \quad (3)$$

where I_{Lpa} can be seen in Fig. 2.

From here, I_{Lpa} can be expressed as follows:

$$I_{Lpa}^2 = \frac{4CV_{c1}(V_{ip} - V_{c2})}{L} \quad (4)$$

The energy stored in inductance L in the negative channel can be calculated similarly to (3):

$$w_{Ln} = 2CV_{c1}(V_{in} + V_{c2}) \quad (5)$$

By adding $(3)+(5)$, the total energy of the inductances can be expressed:

$$w_L = 4CV_{c1}V_{i1} \quad (6)$$

The ratio of the energy of the inductor in channel p and the total energy of both inductors can be calculated if dividing (3) by (6):

$$\frac{w_{Lp}}{w_L} = \frac{2CV_{c1}(V_{ip} - V_{c2})}{4CV_{c1}V_{i1}} = \frac{1}{2}\frac{V_{ip} - V_{c2}}{V_{i1}} \quad (7)$$

from here capacitor voltage V_{c2} can be expressed:

$$V_{c2} = V_{ip} - \frac{2w_{Lp}}{w_L}V_{i1} \quad (8)$$

The output energy of channels $p1$ and $p2$, w_{op1} and w_{op2} can be calculated as follows. In the time interval $1p$, $0 \leq \omega t \leq \alpha_p$:

$$w_{op_1}^{1p} = 0, \quad w_{op_2}^{1p} = 0 \quad (9)$$

In the time interval $2p$, $\alpha_p \leq \omega t \leq \alpha_{cp}$, using (4) :

$$w_{op_1}^{2p} = \frac{L(I_{Lpa}^2 - I_{Lpb}^2)}{2} = 2CV_{c1}(V_{ip} - V_{c2}) - \frac{LI_{Lpb}^2}{2} \quad (10)$$

$$w_{op_2}^{2p} = 0 \quad (11)$$

Finally, in the time interval $3p$, $\alpha_{cp} \leq \omega t \leq \alpha_{ep}$:

$$w_{op_1}^{3p} = 0, \quad w_{op_2}^{3p} = \frac{1}{2}LI_{Lpb}^2 \quad (12)$$

The energy dissipated on the loads R_{p1} and R_{p2} in the whole period can be calculated by $(9)+(10)+(12)$, $(9)+(11)+(12)$ and substituting (4):

$$w_{op1} = \frac{1}{2}L\left(\frac{4CV_{c1}(V_{ip} - V_{c2})}{L} - I_{Lpb}^2\right) = \frac{V_{op1}^2}{R_{p1}f_s} \quad (13)$$

$$w_{op2} = \frac{1}{2}LI_{Lpb}^2 = \frac{V_{op2}^2}{R_{p2}f_s} \quad (14)$$

The total energy transferred to the outputs in one period can be calculated as follows:

$$w_o = \frac{V_{op1}^2}{R_{p1}f_s} + \frac{V_{op2}^2}{R_{p2}f_s} + \frac{V_{on1}^2}{R_{n1}f_s} + \frac{V_{on2}^2}{R_{n2}f_s} \quad (15)$$

In order to substitute the switching angles, first the voltage of the capacitor is described in function of α_p. Based on the rearrangement of the previously described equation, $dv_c = \frac{1}{C}\int i_c dt$, voltage of the capacitor V_{cp} can be described as follows (see Fig. 1 and Fig. 2 on page 2, Section II):

$$V_{cp} = V_{cn} + \frac{1}{C}\int_0^{\frac{\alpha_p}{\omega}} \frac{V_{ip} - V_{cn}}{Z} sin(\omega t)dt \quad (16)$$

Performing the integral:

$$V_{cp} = V_{cn} + (V_{ip} - V_{cn})(-\cos\alpha_p + 1) \quad (17)$$

from where switching angle α_p can be expressed:

$$\alpha_p = arccos\left(\frac{V_{ip} - V_{cp}}{V_{ip} - V_{cn}}\right) \quad (18)$$

Current value I_{Lpb} can be calculated as follows (see Fig. 2):

$$I_{Lpb} = I_{Lpa} - \frac{1}{L}V_{op1} \cdot \frac{\alpha_{cpp}}{\omega} \quad (19)$$

from where α_{cpp} can be expressed, substituting Z as follows:

$$\alpha_{cpp} = \frac{Z(I_{Lpa} - I_{Lpb})}{V_{op1}} \quad (20)$$

After calculating the switching angles, the required operation point can be set.

IV. Analysis of the Asymmetrical Load Resistances Case

The converter can operate not only in symmetrical conditions but also in case of any parameter deviation between channel p and n. In this paper the effect of asymmetrical load resistances will be discussed. In order to simplify the investigations, $V_{ip} = V_{in}$, $V_{op1} = V_{op2} = V_{on1} = V_{on2} = V_{op1,2}$ are assumed. On the other hand $R_{p1} \neq R_{p2}$ and $R_{n1} \neq R_{n2}$, $R_{p1} = R_{n1}$, $R_{p2} = R_{n2}$ are presumed. In this case several simplifications can be made on the presented $(1) - (20)$ equations. Implementing the symmetrical considerations to $(7) - (15)$, the energy of the outputs in channel p divided by the total output energy is (assuming lossless operation):

$$\frac{w_{op}}{w_o} = \frac{w_{Lp}}{w_L} = \frac{\frac{V_{op1}^2}{f_s R_{p1}} + \frac{V_{op2}^2}{f_s R_{p2}}}{\frac{V_{op1}^2}{f_s R_{p1}} + \frac{V_{op2}^2}{f_s R_{p2}} + \frac{V_{on1}^2}{f_s R_{n1}} + \frac{V_{on2}^2}{f_s R_{n2}}} = \frac{1}{2} \quad (21)$$

Since $w_{Lp} = w_{op}$ and $w_L = w_o$, substituting (21) to (8) results in $V_{c2} = 0$ (due to the symmetrical input voltages $V_{ip} = V_{in} = V_{i1}$).

Choosing I_{Lpb} and V_{c1} parameters to set the output voltages in the first control strategy, output voltage V_{op1} can be expressed from (13), dividing it by I_{Lpa}^2, substituting I_{Lpa}^2 (4) as follows:

$$V_{op1} = \sqrt{2R_{p1} f_s C (V_{ip} - V_{c2}) V_{c1} (1 - \frac{I_{Lpb}^2}{I_{Lpa}^2})} \quad (22)$$

Output voltage V_{op2} can be expressed if dividing (14) by I_{Lpa}^2, and substituting (4) as follows:

$$V_{op2} = \sqrt{2R_{p2} f_s C (V_{ip} - V_{c2}) V_{c1} \frac{I_{Lpb}^2}{I_{Lpa}^2}} \quad (23)$$

Considering $V_{op1} = V_{op2} = V_{on1} = V_{on2} = V_{op1,2}$ and $R_{p1} \neq R_{p2}$, $R_{n1} \neq R_{n2}$, $R_{p1} = R_{n1}$, $R_{p2} = R_{n2}$, substituting per unit values, output voltage in function of the control strategy parameters V_{c1}^* and I_{Lpb}^* can be expressed.

$$V_{op1,2}^* = \sqrt{\frac{V_{c1}^* R_{p1}^* f_s^* (1 - I_{Lpb}^{*2})}{\pi}} = \sqrt{\frac{V_{c1}^* R_{p2}^* f_s^* I_{Lpb}^{*2}}{\pi}} \quad (24)$$

Choosing parameters α_p and α_{cpp} for the second control strategy, these can be expressed as follows:

$$\alpha_p = arccos\left(\frac{1 - V_{c1}*}{1 + V_{c1}*}\right) \quad (25)$$

Substituting per unit values to (20), α_{cpp} is:

$$\alpha_{cpp} = (1 - I_{Lpb}^*) \frac{2\sqrt{V_{c1}^*}}{V_{op1,2}^*} \quad (26)$$

Expressing V_{c1}^* from (25) and I_{Lpb}^* from (26), substituting these to (24), output voltage $V_{op1,2}^*$ can be expressed in function of α_p and α_{cpp} for the second control strategy as follows:

$$V_{op1,2}^* = \frac{4R_{p1}^* f_s^* \alpha_{cpp} \tan\frac{\alpha_p}{2}}{R_{p1}^* f_s^* \alpha_{cpp}^2 + 4\pi} = \frac{-B + \sqrt{B^2 - 4AD}}{2A} \quad (27)$$

where

$$A = 1 - \frac{\alpha_{cpp}^2 R_{p2}^* f_s^*}{4\pi} \quad (28)$$

$$B = \frac{R_{p2}^* f_s^* \alpha_{cpp}}{\pi} \tan\frac{\alpha}{2} \quad (29)$$

$$D = \frac{-R_{p2}^* f_s^*}{\pi} \tan\frac{\alpha_p}{2}^2 \quad (30)$$

The operation gets to protection mode if the capacitor voltage becomes $V_{cp} = V_{ip} + V_{op1} + V_{op2}$ or $V_{cn} = -(V_{in} + V_{on1} + V_{on2})$. If the output voltages are symmetrical, substituting per unit values, protection mode creates the following limit for the capacitor voltage (protection mode needs to be avoided as there the output voltages are not controllable):

$$V_{c1}^* \leq 1 + 2V_{op1,2}^* \quad (31)$$

Furthermore, $I_{Lpb}^* \geq 0$ makes an upper limit also for α_{cpp}, which is denoted by $\alpha_{cpp,max}$ and can be calculated as:

$$\alpha_{cpp,max} = \frac{2\sqrt{V_{c1}^*}}{V_{op1,2}^*} \quad (32)$$

V. Control Strategy for the Examined Operation Cases

In order to create a control strategy for the five level Buck-Boost converter in case of asymmetrical load resistance operation, several control characteristics are examined. The effect of two sets of parameters on the output voltages is analysed: the switching angles α_p, α_{cpp} and the capacitor voltage V_{c1}^*, inductor current I_{Lpb}^*. During the investigations, $f_s^* = 1$ is considered, meaning that $f_s = f_r$, the switching frequency equals to the resonant frequency. From now on, symmetrical operation among p and n and partial asymmetry among p_1 and p_2 channels are considered (as showed earlier in Section IV). Several operation points are marked in the figures with capital letters $(A - H)$, in order to help illustrating the effect of the parameters, see Table I.

TABLE I
Examined Operation Points at Asymmetrical Load Resistances in DCM

	Mode	R_{p1}^*	R_{p2}^*	$V_{op1,2}^*$	I_{Lpb}^*	V_{c1}^*	α_{cpp}	α_p
A	prot.	6	0.9	0.8	0.93	2.57	15.6	115.8
B	sym.	6	6	0.8	0.71	0.67	34.35	78.6
C		1.5	6	0.8	0.45	1.67	102.6	104.7
D		1.5	2	0.8	0.65	2.35	76.2	113.8
E	sym.	6	6	1.5	0.71	2.37	34.4	113.8
F	prot.	6	2.5	1.5	0.85	3.95	25.3	125.6
G	prot.	2.5	6	1.5	0.55	3.97	71.4	126.4
H	prot.	12.5	1.5	1.2	0.33	3.36	9.88	121.9

In Figures 3 to 8, control characteristics of the converter are examined, where continuous lines mark load resistance R^*_{p1}, dashed lines mark R^*_{p2}. The same colours belong to the same resistance level. The green dotted lines indicate the symmetrical operation points in the figures. As during the investigations $V^*_{op1,2}$ is fixed, the border of protection mode belongs to a constant V^*_{c1} value, see (31). This also means that, due to (25), the border of protection mode is at a constant α_p value. The border of protection mode is marked by a black thick line. The other limitation on the $\alpha_p(\alpha_{cpp}, R^*_{p1,2})$ graphs is the maximum value $\alpha_{cpp,max}$, which can be calculated by (32) and is indicated by a black thick line. In all figures, during the whole interval the converter operates in DCM.

Figure 3 shows the effect of load resistance variation in function of the switching angles α_p, α_{cpp} at $V^*_{op1,2} = 0.8$. Operation point A is at the border of protection mode, here $R^*_{p1} = 6$, $R^*_{p2} = 0.9$. The operation point can get out of protection mode by increasing $R^*_{p2} = 0.9$ to $R^*_{p2} = 6$, moving to B, this way the switching loss on S_p can be reduced. To maintain this operation mode, α_{cpp} has to be increased, while α_p decreased. B is a symmetrical operation point, where $R^*_{p1} = R^*_{p2}$. Might the load resistance R^*_{p2} increase further at a constant R^*_{p1}, α_{cpp} reaches its limit. If the load resistance on channel $p2$ remains constant, while R_{p1} decreases, the operation gets to C, both α_{cpp} and α_p need to be increased. Finally, if R^*_{p1} stays constant, might R^*_{p2} decrease, α_{cpp} has to be decreased, while α_p increased (see operation point D).

Figure 4 shows the same cases at $V^*_{op1,2}$, this time in function of parameters V^*_{c1} and I^*_{Lpb}. Here, as DCM operation is examined, the minimum value of $I^*_{Lpb} = 0$. Also, symmetrical points are at a constant $I^*_{Lpb} = 0.71$ as showed in [14]. Starting from operation point C, at a constant R^*_{p1}, the decreasing R^*_{p2} load resistance gets the operation to D, both V^*_{c1} and I^*_{Lpb} parameters need to be increased. Might R_{p2} stay constant, if R^*_{p1} increases, moving from C to B, V^*_{c1} needs to be decreased, I^*_{Lpb} increased. Decreasing R^*_{p1}, while keeping R^*_{p2} constant, the operation can get to protection mode, which however needs to be avoided. A is right at the border of protection mode, where the required symmetrical output voltages can still be maintained.

Figures 5 and 6 show the effect of asymmetrical load resistances, when the output voltage is increased to $V^*_{op1,2} = 1.2$, in function of α_{cpp}, α_p and I^*_{Lpb}, V^*_{c1} respectively. Here the border of protection mode is at a higher α_p (and V^*_{c1}), see (25),(31), as here $V^*_{c1,prot} = 1 + 2V^*_{op1,2} = 3.4$, thus $\alpha^*_{p,prot} = 123°$, compared to Fig. 3 (and Fig. 4), where $V^*_{c1,prot} = 1+2V^*_{op1,2} = 2.6$, thus $\alpha^*_{p,prot} = 116.4°$. Operation point H is right at the border of protection mode, where $R^*_{p1} = 12.5$, $R^*_{p2} = 1.5$. Based on (24) and (27), might the symmetrical output voltage increase at constant load resistances, V^*_{c1} and thus α_p increases as well.

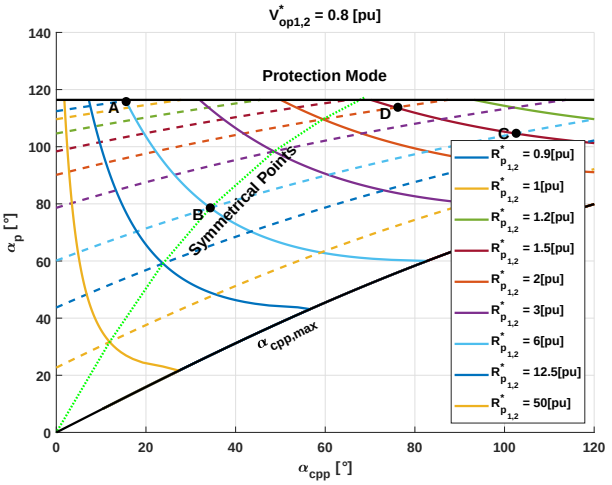

Fig. 3. Operation Characteristics $\alpha_p(\alpha_{cpp}, R^*_{p1,2})$, when $V^*_{op1,2} = 0.8$

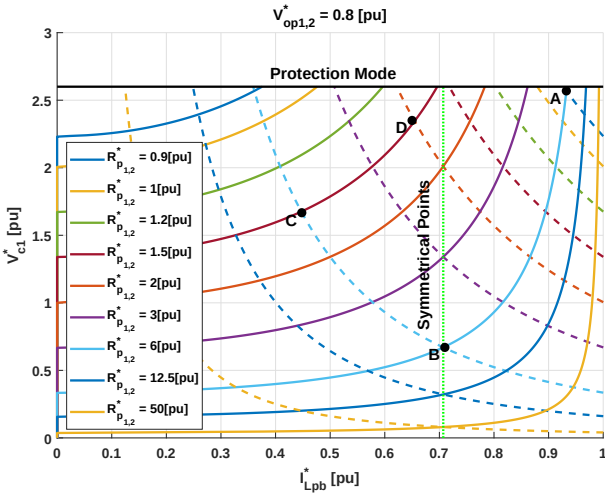

Fig. 4. Operation Characteristics $V^*_{c1}(I^*_{Lpb}, R^*_{p1,2})$, when $V^*_{op1,2} = 0.8$

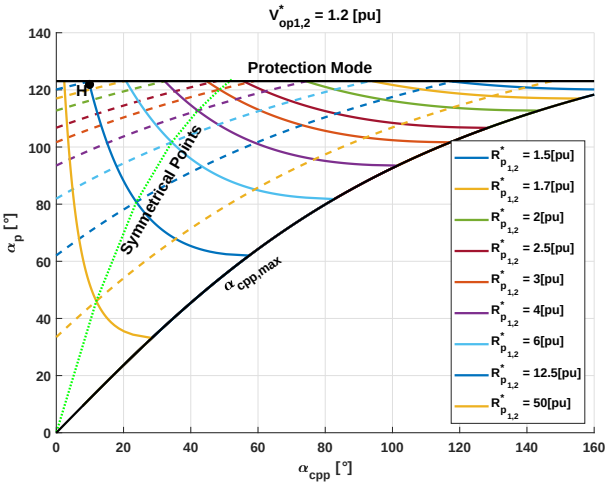

Fig. 5. Operation Characteristics $\alpha_p(\alpha_{cpp}, R^*_{p1,2})$, when $V^*_{op1,2} = 1.2$

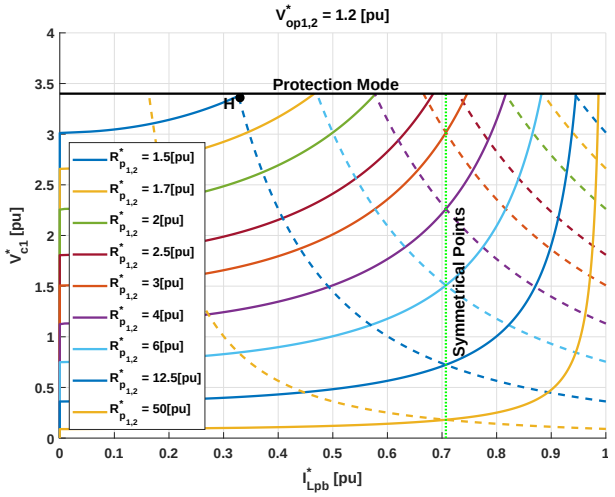

Fig. 6. Operation Characteristics $V^*_{c1}(I^*_{Lpb}, R^*_{p1,2})$, when $V^*_{op1,2} = 1.2$

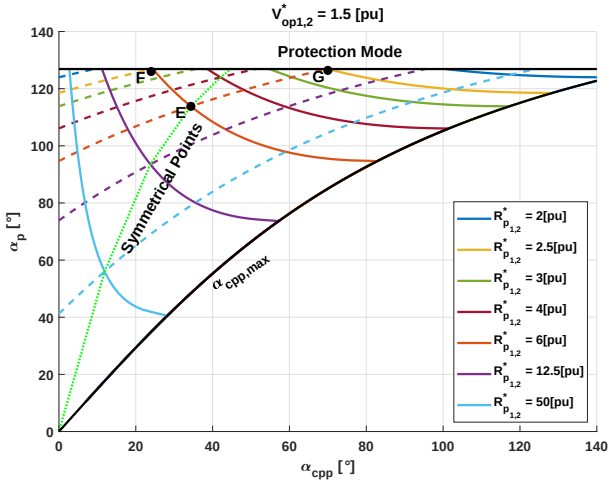

Fig. 7. Operation Characteristics $\alpha_p(\alpha_{cpp}, R^*_{p1,2})$, when $V^*_{op1,2} = 1.5$

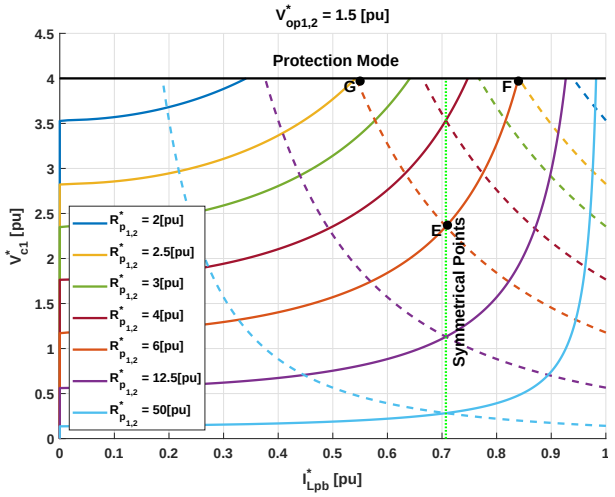

Fig. 8. Operation Characteristics $V^*_{c1}(I^*_{Lpb}, R^*_{p1,2})$, when $V^*_{op1,2} = 1.5$

Finally, Fig. 7 and Fig. 8 show the case of asymmetrical R^*_{p1}, R^*_{p2} load resistances, when the output voltage is increased further to be $V^*_{op1,2} = 1.5$, in function of α_{cpp}, α_p and I^*_{Lpb}, V^*_{c1} respectively. The limit of α_{cpp}, $\alpha_{cpp,max}$ is increasing steeper, than in case of $V^*_{op1,2} = 0.8$. Operation point F is at the border of protection mode, from where however the operation point can move, by increasing load resistance R^*_{p1} at a constant R^*_{p2}. Parameter α_{cpp} has to be increased, α_p need to be decreased, while in case of the V^*_{c1}, I^*_{Lpb} control strategy both parameters need to be decreased to get to E (which is a symmetrical operation point). Might R^*_{p2} stay constant, a decreasing R^*_{p1} can get the operation to protection mode again, which however can be avoided by keeping α_p at the border of protection mode (or $V^*_{c1} = 4$), see operation point G.

VI. Simulation Results

Theoretical considerations were supported by simulations. The simulation model of the converter was built in Matlab Simulink R2018b, based on Fig. 1 (page 2, Section II), assuming ideal circuit components with the following parameters:

- $V_{ip} = V_{in} = 20V, f_r = 50.329kHz$
- $C = 1\mu F, L = 10\mu H, C_i = 10\mu F, C_o = 200\mu F.$

During the simulations, the switching frequency was considered to be equal to the resonant frequency, $f_s = f_r$. Figures 9 to 11 show the time functions of the capacitor voltage, $v_c(t)$, inductor currents $i_{Lp}(t)$ and $i_{Ln}(t)$ of p and n channels and capacitor current $i_c(t)$ in operation points A, E, H respectively (see Table I).

Figure 9 shows operation point A, where the load resistances are asymmetrical, $R_{p1} = 18.9\Omega$, $R_{p2} = 2.8\Omega$, the output voltages are symmetrical $V_{op1} = V_{op2} = 16V$. This operation point is just at the border of protection mode, as here $V_{ip} + V_{op1} + V_{op2} = V_{cp} = 52V$. Here inductor currents i_{Lp} and i_{Ln} reach zero before they would reach the end of the switching time period, thus the operation point is in DCM, ZCS of S_{cp2} (and S_{cn2} is possible). Figure 10 shows operation point E, which is a symmetrical operation point. Here the loads are $R_{p1} = R_{p2} = 18.9\Omega$, the output voltages are $V_{op1} = V_{op2} = 30V$. Finally, Fig. 11 shows the time functions of operation point H, which is right at the border of protection mode. Here the asymmetrical load resistances are $R_{p1} = 39.5\Omega$, $R_{p2} = 4.7\Omega$. Output voltages are symmetrical in this operation point, $V_{op1} = V_{op2} = 24V$. The peak voltage of the capacitor is $V_{cp} = 67.9V$, while $V_{ip} + V_{op1} + V_{op2} = 68V$, consequently this operation point is right at the border of protection mode.

Compared to Fig. 2 (page 2, Section II), it can be concluded that simulation results confirmed the outcome of theoretical analysis.

VII. Conclusion

The operation of a previously proposed five level Buck-Boost converter was investigated at asymmetrical load resistances in discontinuous current conduction mode, steady state

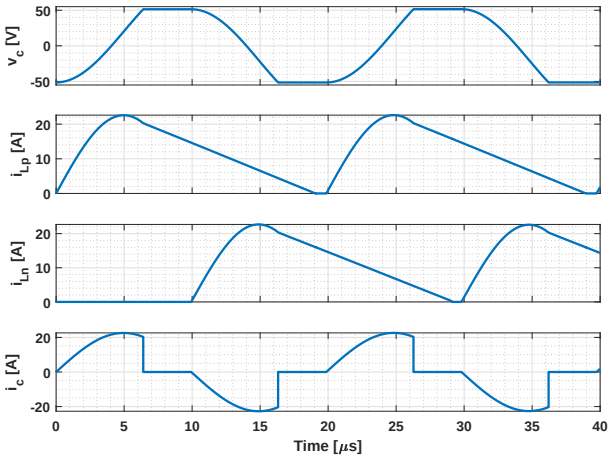

Fig. 9. Time Functions of Inductor and Capacitor Currents and Voltage at Operation Point "A"

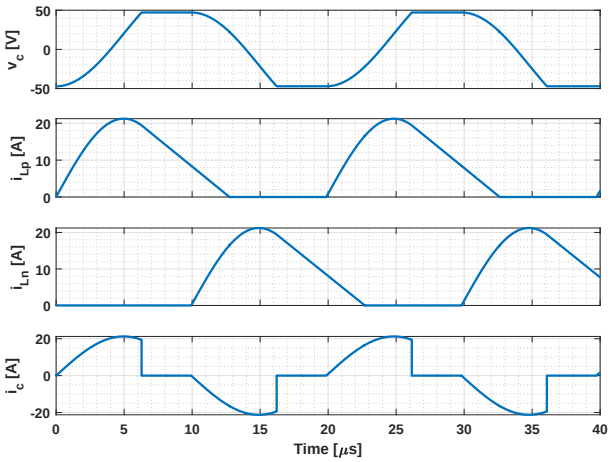

Fig. 10. Time Functions of Inductor and Capacitor Currents and Voltage at Operation Point "E"

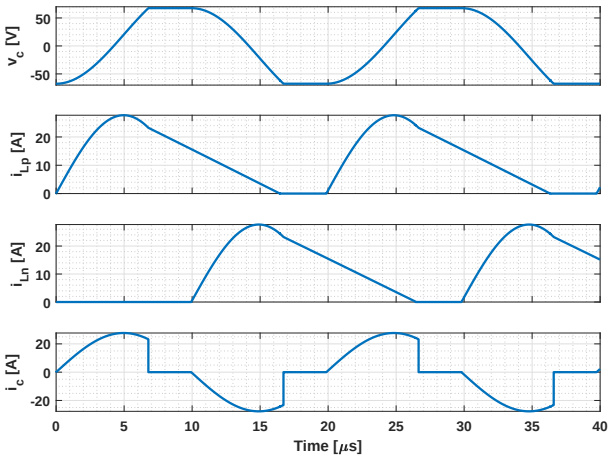

Fig. 11. Time Functions of Inductor and Capacitor Currents and Voltage at Operation Point "H"

conditions. The analytical study was based on the energy equations of the converter, while special, simplified equations were also provided to calculate the required parameters of the operation point. Two different aspects were examined which allowed to set the output voltages of the converter: the switching angles of two controlled switches or the capacitor voltage and the inductor current. These methods were examined in several operation points, both in step up and step down operation. The theoretical results were also supported by Matlab Simulink R2018b simulations which verified the considerations. Possible application fields of the proposed method are DC nano-and microgrids and multilevel inverter drives.

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