Non-unit Protection for HVDC Grids: An Analytical Approach for Wavelet Transform-based Schemes

Vasileios Psaras, *Member, IEEE,* Dimitrios Tzelepis, *Member, IEEE,* Dimitrios Vozikis, *Member, IEEE,* Grain Adam, *Member, IEEE,* Graeme Burt, *Member, IEEE*

***Abstract*—Speed and selectivity of DC fault protection are critical for High-Voltage DC (HVDC) grids and present significant technical and economic challenges. Therefore, this paper proposes a non-unit protection solution that detects and discriminates DC faults based on frequency domain analysis of the transient period of DC faults. The representation of a generic HVDC grid section and the corresponding DC-side fault signatures in the frequency domain form the basis of a generalized approach for analytically designing a protection scheme based on Wavelet Transform (WT). The proposed solution is adaptive within its design stage and offers general applicability and immunity to system changes, while the protection settings are configured for optimized performance. The scheme is validated through offline simulations in PSCAD/EMTDC and the technical feasibility of the algorithm in the real world is demonstrated through the use of real-time digital simulation (using RTDS) and Hardware-in-the-Loop (HIL) testing. Both offline and real-time simulations demonstrate that the scheme is able to detect and discriminate between internal and external faults at a significantly high speed, while remaining sensitive to high impedance faults and robust to external disturbances and outside noise.**

***Index Terms*—DC grid protection, frequency domain analysis, HVDC grids, non-unit protection, wavelet transform.**

I. Introduction

HIGH Voltage DC (HVDC) transmission is widely used for integrating offshore wind farms to mainland AC grids and for interconnecting asynchronous AC zones due to its ability for bulk power transmission over very long distances. HVDC grids are considered as the natural evolution of existing point-to-point transmission links that enable the integration and better utilization of massive amounts of offshore energy. Moreover, they offer a plethora of attractive features such as: enhanced controllability, flexibility and redundancy, improved reliability and security, lower investment costs, etc [1]. However, as with any developing technology, the HVDC grid concept has its challenges, with the requirement for fast and discriminative protection typically being the most prominent.

The electromagnetic phenomena that take place following a DC fault propagate much faster in HVDC grids, with windows for fault detection and interruption being extremely short, typically in the order of a few milliseconds depending on several factors such as size and topology of the DC system and the operating conditions. The requirements of HVDC grid protection become more stringent when only isolation of the faulted area is required, subsequently ensuring overall stability within the HVDC grid and in turn minimal disruption of the transmission output to the AC grid.

The authors are with the Institute for Energy and Environment of the Department of Electronic and Electrical Engineering at the University of Strathclyde, 16 Richmond St, Glasgow G1 1XQ. Scotland, United Kingdom. e-mail: {vasileios.psaras}@strath.ac.uk

In current literature, most proposed HVDC protection schemes are designed based on travelling wave principles that are classified into unit protection and non-unit protection [2]. Unit protection relies on a communication link in order to obtain signal measurements from both ends of the protected feeder. Therefore, the technical feasibility of these methods is greatly compromised in HVDC grids that utilize DC lines of several hundreds of kms, due to prolonged communication delays that inhibit their utilization for primary protection schemes. In [3], the authors achieved a significant reduction in the time delay caused by the communication link but at the expense of installing additional sensors at various points across the lines. Moreover, in [4], the communication is in the same direction as the wave propagation, which results in significant improvement of communication-based methods. However, considering that the fault current rise can be in the range of several kA per ms [5], communication delays can have a detrimental effect on HVDC grid protection.

Non-unit protection techniques typically rely on the placement of series inductors at each end of the transmission medium to define protection boundaries [6]. Series inductors do not only serve as current limiters, but they also behave as a natural boundary filter by damping a range of frequencies of the incident waves, thus influencing the transient voltage and current signatures. This important feature has been exploited to assist DC fault detection and discrimination based on the first incident travelling wave generated by the fault [7]–[10].

Nevertheless, the aforementioned protection algorithms have been designed after extensive time domain simulations to estimate the expected voltage and current signatures and derive the protection thresholds accordingly. Therefore, the designed protection system (accounting for the method and the corresponding thresholds) is only applicable for the system under-test, hence its ability to adapt to different network architectures is challenged. As a result, there are no guarantees that they will perform and operate as designed.

Signal processing techniques, and especially Wavelet Transform (WT) have been widely used in non-unit protection schemes because of their ability to detect the transient components in fault signals [11]–[20]. However, in all these implementations, very limited insight and guidelines have been provided as to how to derive an analytical approach for WT design. In particular, the appropriate wavelet decomposition level, the mother wavelet and the protection thresholds are conventionally determined through extensive offline trial and error simulations.

Several WT-based protection methods based on Discrete Wavelet Transform (DWT) have been proposed in the literature [11]–[16]. However, the effect of the downsampling process

that is an essential element of DWT has not been analyzed in depth. Downsampling leads to loss of information in the high frequency content of the analyzed signal and may result in maloperation of the protection method. In [17], Stationary Wavelet Transform (SWT) which demonstrates time-invariance transformation property has been used on current and voltage measurements to detect DC faults in HVDC grids. Nevertheless, the DC inductor as a boundary element is not considered and hence, selectivity of the method is not ensured.

The shift-sensitivity due to the downsampling process has been considered in [18], where the authors use two adjacent data windows for applying DWT in order to overcome this issue. A 2 ms data window length is used for applying DWT, which is considered relatively long for HVDC grid protection. Moreover, the identification of a critical frequency beyond which the impact of highly resistive internal faults is more pronounced than the impact of external faults has been performed. This is a strong starting point for identifying the lowest suitable decomposition level than can be selected but depending on the sampling frequency of a WT-based method, there might be several levels that satisfy this requirement.

The Real-Time SWT Boundary SWT (RT-BSWT) has been proposed in [19], [20], as an alternative method for avoiding the issues of downsampling. This method results in high speed detection and in reduced computational requirements. Nevertheless, in this method as well, the key WT parameters are mainly selected through trial and error simulations and consequently general applicability is not guaranteed.

To overcome the above limitations, this paper introduces a generalized methodology, specifically tailored for HVDC grid non-unit protection purposes, for flexibly deriving the key parameters of WT-based methods. In contrast with existing approaches, the key parameters of WT are analytically calculated by analyzing the voltage response for key DC fault scenarios in the frequency domain, while avoiding extensive offline simulations. Using this approach, a non-unit protection scheme based on SWT applied on transient voltage measurements is proposed for detecting and discriminating DC faults in HVDC grids. The approach is for each relay separately (within a HVDC grid) and optimized settings for enhanced protection performance are obtained. In this way, general adaptability of the protection scheme to any system configuration and immunity to system changes is ensured.

In Section II, fault voltage travelling waves are represented in the frequency domain and are then used in Section III for optimising the design of the proposed WT-based protection scheme. The enhanced performance of the method is verified by offline simulations in Section IV for an exemplary meshed HVDC grid. Moreover, the technical feasibility of the proposed scheme is demonstrated through real-time simulations in Section V. Finally, conclusions are drawn in Section VI.

II. Frequency Domain Analysis of DC Faults

To facilitate the analysis in this section, a general section of a typical HVDC grid is considered as illustrated in Fig. 1. The grid section comprises of two terminals with Voltage Source Converters (VSCs) that are connected through a cable, while further n and m cables are connected to terminal buses B1 and B2, respectively. The protection zone of relay R is the full length of the DC cable between buses B1 and B2. Based on local measurements, the protective relay should discriminate between a fault at location F_{int} at the remote end of the protected cable (internal fault) from a fault behind the series inductor at location F_{ext} that is right outside the protection zone (external fault). The main difference between the two faults is the presence of the series inductor. The inductor acts as a high impedance element for high frequency components and consequently, the transient voltage frequency response in each fault case is recognizably different. On this basis, the investigation of both faults can reveal significant information for protection design purposes.

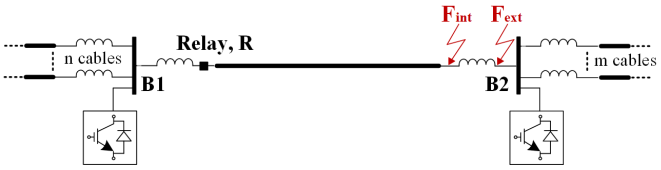


Fig. 1. General section of a HVDC grid.

Owing to the fact that the transient phase of DC faults in HVDC grids is governed by travelling wave phenomena, which are to a great degree frequency dependent, frequency domain analysis can be employed to analyze the frequency response of faults F_{int} and F_{ext}. Towards this aim, common HVDC grid components should be described in the frequency domain, while travelling wave principles have to be taken into account. In the proposed approach, Laplace domain is used to derive the transfer functions of the voltage at the relay location with respect to the fault point accounting both for internal and external faults.

A. Cable and Converter Modelling

Accurate representation of the transmission medium is required for increased fidelity of the frequency domain model and therefore, for the enhanced reliability of the proposed protection scheme design. Distributed parameter frequency dependent model is the most widely-used model for all overhead and underground geometries to adequately describe the current and voltage travelling waves generated by DC faults. The frequency dependent model operates on the principle that the frequency dependence of the medium can be sufficiently described by two matrix transfer functions: i) the propagation function H and ii) the characteristic admittance Y_c, which can be approximated by low order rational functions using weighted vector fitting techniques [21]. Based on this technique, the propagation transfer function is given by

$$H(s) = e^{-s\tau} \sum_{n=1}^{N} \frac{C_n}{s - P_n} \tag{1}$$

where τ is the modal time delay, C_n are the residues, P_n are the poles, and N is the order of the rational function. The required inputs of the model are limited to a set of values of cable series impedance (Z_s) and cable shunt admittance (Y_s) at various frequency points. The characteristic cable impedance (Z_c) is also calculated based on these parameters ($Z_c = \sqrt{Z_s / Y_s}$).

The converter topology considered in this study is the Half-bridge Modular Multilevel Converter (HB-MMC). The fault contribution of HB-MMCs in the early stage of DC faults is governed by the discharge of the distributed capacitance contained in the sub-modules of the converter. The converter impedance is approximated as a series RLC model, and its frequency domain representation is

$$Z_{conv} = R_{eq} + sL_{eq} + 1/sC_{eq} \tag{2}$$

where R_{eq}, L_{eq} and C_{eq} are the converter's equivalent resistance, inductance and capacitance respectively. C_{eq} represents the total capacitance of the inserted sub-modules on all three legs of the converter at the moment the incident wave arrives at the terminal. It is worth noting that the same modelling technique can be applied to other MMC topologies, such as the Full-bridge (FB) or mixed-cell MMCs, since they demonstrate the same behaviour during the transient phase of DC faults.

B. Fault Voltage Wave Representation

To represent the voltage at the measuring point in the frequency domain, the first incident travelling voltage wave generated at the fault location needs to be formulated in the phase domain [6]. The transient voltage at relay R is

$$U_r = \mu_{\beta 1} \cdot H \cdot U'_f \tag{3}$$

where $\mu_{\beta 1}$ is the transmission coefficient at bus B1 and U'_f is the voltage wave at the fault point, and H, which is derived from (1), represents the attenuation experienced by the fault voltage wave after propagating from the fault point. The refraction coefficient describes the fraction of the fault voltage wave that passes through the inductor and is transmitted to the network. For the section shown in Fig. 1, the coefficient is given by $\mu_{\beta 1}$=$2Z_t/(Z_t+Z_c)$ where Z_t is the terminal impedance that is calculated as in (4), assuming that all cables have the same characteristic impedance and the same series inductance.

$$Z_t = Z_{conv} // \frac{(sL + Z_c)}{n} + sL \tag{4}$$

As seen from (3), the voltage at the measuring point is dependent on the fault voltage wave U'_f. When a pole-to-pole fault occurs, the voltage at the fault location falls from the prefault nominal voltage U_{dc} to zero. The Superposition theorem can be applied to derive the voltage at the fault location. Consequently, the fault network, which includes a DC voltage source at the fault location with a value equal to the prefault voltage with reverse polarity (U_f=$-U_{dc}$) is superposed to the prefault network. Fig. 2 displays the equivalent fault-superposed circuit for an internal pole-to-pole fault at F_{int}.

Based on the equivalent circuit depicted in Fig. 2, the fault voltage wave is expressed as

$$U'_{f,int} = \frac{Z_c // sL}{(R_f + 2Z_c // sL)} U_f \tag{5}$$

Using the Superposition theorem in a similar manner for a solid fault at location F_{ext}, the voltage at the fault point is

$$U'_{f,ext} = \frac{Z_c}{2Z_c + 2sL} U_f \tag{6}$$

By substituing (5) and (6) to (3), the transfer function of the ratio of voltages at the relay location and the voltage at the fault point (i.e. U_r/U_f) can be derived for both F_{int} and F_{ext}. The same approach can be followed for deriving the fault voltage waves in the case of pole-to-ground faults.

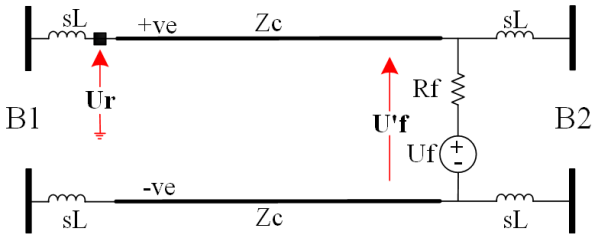


Fig. 2. Equivalent fault-superposed circuit for a resistive internal pole-to-pole fault at the end of protection zone of relay R.

C. Validation of Frequency Domain Analysis

PSCAD detailed simulations of an HVDC grid section are compared against the results provided by the theoretical frequency domain analysis to prove the validity of the calculated transient voltage in each fault case. The cable parameters are adapted from [22], the cable length is set to 200 km, while n, m are set to 2 and 1, respectively. Series inductors with a value of 50 mH are placed at each cable end, while R_{eq}=0.0533 Ω, L_{eq}=0.28 mH and C_{eq}=94.26 μF. The faults occur at t=0 ms.

A step input with a magnitude equal to the prefault pole-to-pole voltage is applied at the fault point (U_f=$-U_{dc}$) and then, inverse Laplace transform is used to obtain a time-domain representation of the transient phase of DC faults. The results of the comparison for solid faults at both locations are shown in Fig. 3. It can be seen, that Frequency Domain Analysis (FDA) demonstrates high accuracy in the transient stage for both faults, thus confirming its suitability as a means of analyzing DC faults in HVDC grids.

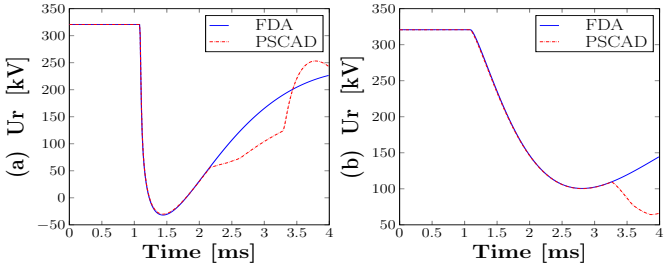


Fig. 3. Validation of frequency domain model against PSCAD for a) an internal solid fault and b) an external solid fault.

In both cases, the fault response deviates from PSCAD simulations, approximately 1.5–2 ms after fault inception. This is attributed to the fact that the analysis does not take into account subsequent travelling waves that arrive due to reflections of the first incident wave or due to travelling waves generated from other events such as breaker tripping or converter blocking actions. Nevertheless, the information contained within the first incident travelling wave is sufficient for protection design. It can be concluded that the model is accurate during the transient period of DC faults, thus providing a time window that is long enough for forming analytical design principles for WT-based fault detection methods.

D. Frequency Response of Transfer Functions

Fig. 4 displays the frequency response in terms of the magnitude of the transfer functions for faults at locations F_{int} and F_{ext} using the same parameters of the previous subsection. It is evident, that in the case of an external solid fault (R_f=0 Ω), the transient voltage attenuates faster in the high frequency region (beyond 200 Hz in this case) than that of a solid internal fault, in which there is a significant high frequency content. The difference in voltage response is caused entirely by the filtering effect of the inductor. This is the main principle of non-unit protection that is used for discrimination between internal and external faults by exploiting the higher magnitude of the high frequency components of voltage.

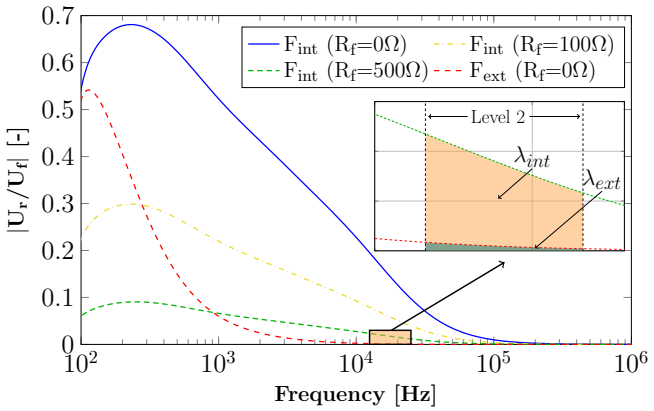


Fig. 4. Transient voltage frequency response in the case of a solid external fault and for various fault resistances of the internal fault.

Fig. 4 also shows the frequency response for highly resistive internal faults at F_{int}. It is evident that as fault resistance increases, the reduction in magnitude of the voltage across the whole bandwidth becomes more prominent. In the low frequency region, the magnitude becomes much smaller than that of the transfer function for the external fault (F_{ext}). Nevertheless, the voltage under highly-resistive internal faults still reveals a higher magnitude in the high frequency region as opposed to the voltage for a solid external fault in which, the magnitude decays faster to zero. Hence, this frequency range can be used for discriminating DC faults.

III. Analytical Design of WT-based HVDC Grid Protection

Due to its time and frequency localization capability, WT can be used to extract the necessary information in specific frequency bands of the transient voltage. As explained in the previous section, the introduction of series inductors, impacts the frequency characteristic of the voltage signatures and hence, the resulting WT outputs (coefficients), thus providing the capability for discriminative fault detection. WT is characterized by a scale parameter (α) and a translation parameter (β). The former determines the size of the window in which WT is performed, while the latter corresponds to the action of shifting the wavelet forward in time while analyzing the entire signal. The WT of a signal $u(t)$ is expressed as

$$WT_{(\alpha,\beta)}u(t) = \int_{-\infty}^{+\infty} u(t)\frac{1}{\sqrt{\alpha}}\psi^*\left(\frac{t-\beta}{\alpha}\right)dt \qquad (7)$$

where ψ^* is the daughter wavelet that is a scaled and shifted version of the mother wavelet function ψ.

DWT can be efficiently implemented based on multiresolution analysis, in which, the signal is passed through successive layers of low-pass and high-pass filters and each layer produces low frequency approximation (A) and high frequency detail coefficients (D). Due to the filtering process at each decomposition level, the frequency bands of A and D coefficients differ. The bands for a signal sampled at 100 kHz are cited in Table I.

TABLE I. Approximation and detail coefficients frequency bands for the first six decomposition levels (100 kHz sampling frequency).

Base signal (fs=100 kHz)	Approximation coefficient frequency band [kHz]	Detail coefficient frequency band [kHz]
1st level	0 – 25	25 – 50
2nd level	0 – 12.5	12.5 – 25
3rd level	0 – 6.25	6.25 – 12.5
4th level	0 – 3.125	3.125 – 6.25
5th level	0 – 1.56	1.56 – 3.125
6th level	0 – 0.78	0.78 – 1.56

One significant drawback of DWT for HVDC grid protection purposes is that the resulting detail coefficients differ depending on the moment the DC fault occurs. This is caused by the downsampling process involved at each decomposition level, which leads to loss of information that is present in the high frequency content. In particular, when analyzing a fault signal with DWT up to level j, the number of different sets of coefficients that can be extracted is 2^j. To overcome this issue, DWT could be applied 2^j times while moving the data window by one sample, as performed in [18]. However, as the decomposition level increases, this solution necessitates extensive calculations.

Alternatively, the problem can be solved by using SWT, which provides the same number of coefficients as the analyzed signal at each decomposition level. This is achieved by upsampling the low-pass and high-pass filters (by means of zero padding), instead of downsampling the analyzed signal as in DWT. SWT is less efficient than DWT and requires additional time to extract the detail coefficients. Nevertheless, when compared to the option of performing DWT 2^j times on the fault signal, the total execution time of SWT becomes equal or smaller, especially as j increases. Therefore, SWT algorithm is considered in this paper to extract the maximum benefit of the method. The detail coefficients using SWT at each level j are obtained through

$$D_j[n] = \sum_{k=0}^{L-1} A_{j-1}[k]h_j[n-k] \qquad (8)$$

where A_j are the approximation coefficients at level j (with initial DC voltage samples representing A_0), n is the sample index and L represents the order of the high-pass filter $h[k]$, which depends on the selected mother wavelet and decomposition level. The rest of the section presents an analytical approach for selecting the decomposition level, the mother wavelet and the protection threshold. Although SWT is used, the process for selecting the parameters is valid for any WT variant. The generalized grid section of Section II with the same parameters is used as an example for the analysis.

A. Selection of Decomposition Level

One of the crucial parameters that needs to be determined when designing a WT-based fault detection and discrimination algorithm, is the wavelet decomposition level. The selection of the level depends on the frequency content of interest of the signal to be processed. It is evident from Table I that depending on the sampling frequency, the frequency bands of wavelet decomposition procedure can be known in advance and hence, the appropriate level can be analytically determined based on the targeted band of frequencies in the signal.

The frequency response of the voltage transfer functions is used to identify the decomposition level (and its corresponding frequency band), in which the impact of a highly-resistive internal fault is more distinctive than that of the external fault. To quantify this impact, the areas underneath the U_r/U_f transfer function are calculated at each level j, for a 500 Ω resistive fault at F_{int} and for a solid fault at F_{ext}, as shown in (9). The areas are denoted as λ^j_{int} and λ^j_{ext}, respectively. Based on (10), the level that maximizes the ratio $\lambda^j_{int}/\lambda^j_{ext}$ is selected.

$$\begin{aligned} \lambda^j_{int} &= \int_{l_j}^{u_j} |U_r/U_f|_{F_{int}^{(R_f=500\Omega)}} df \\ \lambda^j_{ext} &= \int_{l_j}^{u_j} |U_r/U_f|_{F_{ext}^{(R_f=0\Omega)}} df \end{aligned} \tag{9}$$

$$WT_{lvl} = \max_j(\lambda^j_{int}/\lambda^j_{ext}),\ \ for\ 1 \le j \le j^{max} \tag{10}$$

where l_j and u_j are the lower and upper bounds of the j^{th} decomposition level, respectively. Assuming 100 kHz sampling frequency, the level that maximizes the above function is the second wavelet decomposition level (see Fig. 4). The same approach can be followed for any parameters of the HVDC grid section and sampling frequency.

B. Threshold Selection

Non-unit protection methods do not offer inherent selectivity and they require an optimized protection setting to ensure that the maximum protection reach is achieved and that the method remains robust against external faults and other disturbances. FDA can be used for developing a generalized approach for directly calculating the protection threshold, while avoiding extensive electromagnetic transient simulations. A solid external fault is the hardest fault that should be detected and classified by the relay as an external fault for which no action is required. Hence, the voltage response of this fault is used for setting the threshold.

The required protection threshold can be determined analytically by using SWT to analyze the time-domain expression of $U_{r,ext}$, i.e. the derived voltage response for a solid external fault as performed in Section II-C (refer to Fig. 3(b)). According to Wavelet Modulus Maxima (WMM) theory, the threshold is equal to $WMM_{F_{ext}}$, which is the maximum point of the absolute voltage wavelet detail coefficients as shown by

$$WT_{th} = k \cdot WMM_{F_{ext}} = k \cdot max(\ |D_j(U_{r,ext})|\ ) \tag{11}$$

where j is obtained using (10) and k is a reliability factor that offers a safety margin and immunity against external influencing factors such as noise, measurement errors and other disturbances (here, k=5).

C. Wavelet Selection

Selecting the right wavelet is of crucial importance for the successful implementation of WT. In current literature, WT has been widely used, but little insight has been provided as to what procedure should be followed for the determination of the appropriate mother wavelet. There are several factors that shall be considered such as, the nature of the analyzed signal, the computational requirements and the application-related aspects and goals (e.g. time localization of voltage transients in DC fault detection and location applications) [23].

Each wavelet is characterized by its order which is usually indicated in the name of the wavelet, e.g. *dbN* corresponds to a wavelet of the Daubechies family where the order is equal to 2*N*. High order wavelets have greater filter length and are better in localizing singularities in the signal. However, very high wavelet orders smooth the WT coefficients, leading to indistinguishable transients, while also high order filters result in poor time localization properties and increased computational complexity, which hinders the feasibility of WT for real-time applications. Consequently, wavelets with 7-12 filter coefficients are considered for this analysis.

Quantitative approaches have been proposed for choosing the right wavelet such as, the Pearson coefficient [15], the maximum absolute error or the root-mean-square error (RMSE) [24] between the original signal and a reconstructed version of the original signal. However, in the context of this study, none of these methods offered further insight since all the remaining wavelets performed similarly well.

Based on the above discussion and considerations, the appropriate mother wavelets can be limited to a few options, but it is not possible to single out a wavelet that performs sufficiently well for any HVDC grid section. Consequently, an additional criterion is required to obtain the optimum mother wavelet. The criterion proposed in this paper is the assessment of the capability of different mother wavelets in providing enhanced protection margin and resiliency against highly resistive faults. For the generic section of Fig. 1, the WMM for a DC fault at location F_{int} with fault resistance equal to 500 Ω is compared against the corresponding WMM that is obtained for a solid fault at location F_{ext} for all the remaining wavelets. Assuming a set Ψ that comprises of all candidate mother wavelets, the wavelet $\psi \in \Psi$ that exhibits the highest ratio $WMM_{F_{int}}/WMM_{F_{ext}}$ is selected as shown by (12). The final protection threshold is then selected based on the $WMM_{F_{ext}}$ of the best performing wavelet WT_{wav} using (11).

$$WT_{wav} = \left\{ \psi : \max_{\psi} \left(\frac{WMM^{R_f=500\Omega}_{F_{int}}(\psi)}{WMM^{R_f=0\Omega}_{F_{ext}}(\psi)} \right),\ for\ \psi \in \Psi \right\} \tag{12}$$

Using the example of Section II, Table II presents the analytically calculated ratios (for the mother wavelets of set Ψ) obtained through the analytical analysis and the corresponding ratios obtained through time-domain simulations of a detailed model in PSCAD. It is evident, that the analytical approach yields very similar results to those obtained from PSCAD, thus proving the suitability of the approach for designing WT-based HVDC protection schemes without the need for offline simulations.

As seen from Table II, wavelet *sym4* presents the highest ratio and is therefore selected. Even for a very highly-resistive fault (500 Ω), *sym4* demonstrates a WMM that is 21 times higher than the corresponding WMM for the external fault. It is evident that selecting a wavelet based on this criterion maximizes the protection margin of the protection method.

TABLE II. Comparison of $WMM_{F_{int}}/WMM_{F_{ext}}$ ratios obtained using PSCAD simulations and the theoretical approach.

Mother Wavelet	PSCAD	Theoretical
db4	1.591	1.606
db5	14.828	15.061
db6	13.671	13.916
sym4	21.1450	21.640
sym5	18.555	18.802
sym6	19.895	20.603
coif2	14.785	17.704
Bior 1.3	3.7132	3.7506
Bior 1.5	1.1486	1.2271
Bior 2.2	4.6164	5.0302
Bior 2.4	2.4785	2.5088

D. Proposed Protection Scheme

Based on the generalized analysis of the previous sub-sections, a non-unit HVDC protection scheme is proposed which follows a two-stage approach. Fig. 5 shows the overall protection scheme that is employed by each relay. The first stage is a parameterization procedure to select the optimum WT parameters (which is carried out offline) and the second stage is a real-time signal processing process (based on SWT) that is responsible for detecting internal faults.

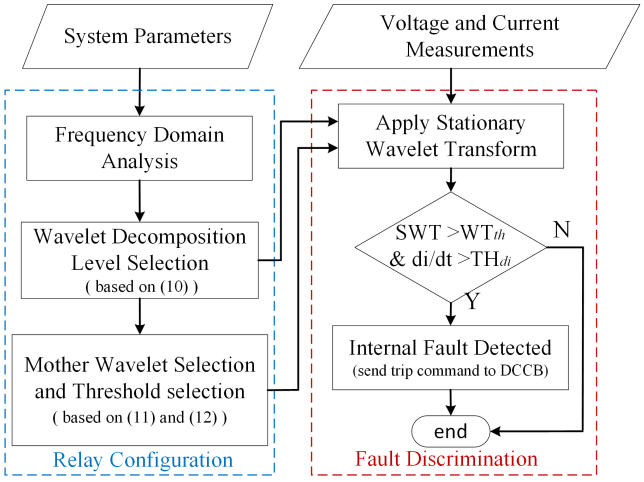


Fig. 5. Flowchart of protection scheme.

1) Relay Configuration Stage: In this stage, the suitable wavelet decomposition level, mother wavelet and protection threshold are derived based on the approach that was previously presented. The determination of SWT parameters is realized locally at each relay location by taking into account the system parameters, namely, the feeder length and geometry, the number of other attached feeders to the same terminal, the converter parameters and the inductive termination. In case there is a change in the system parameters (e.g. equipment replacement, scheduled maintenance, grid expansion), the procedure is re-initiated to reconfigure the relay parameters. In this way, optimized settings for the protection scheme under all circumstances is guaranteed.

2) Fault Discrimination Stage: In the second stage of the protection algorithm, selectivity is ensured by applying SWT on voltage measurements captured by the relay that is placed on the line-side of the series inductor. To guarantee selectivity, protective relays should be placed at each end of a transmission medium at both poles of the HVDC grid. In this way, only the faulted segment can be securely isolated. Since line-side pole voltage does not contain information regarding the direction of the fault, the current derivative *di/dt* is employed to provide directionality (i.e. distinguish between forward and backward faults). Assuming positive current as the current that flows into the feeder, a positive *di/dt* indicates that a fault lies in the forward direction of the protection relay (towards the other end of the DC cable). Consequently, a near-zero threshold TH_{di} on current derivative is used. The calculated parameters from the first stage are utilized by SWT to successfully discriminate between internal and external faults. If the detail coefficients exceed the analytically calculated threshold WT_{th}, then an internal fault is detected. When an internal fault is confirmed, the relay sends a tripping signal to the corresponding DC circuit breaker (DCCB) to isolate the faulted DC line or cable. It should be noted that the fault detection method is designed to be unbound to a specific breaker technology and hence, it is not dependent on DCCB characteristics, such as breaking speed and maximum current breaking capacity.

IV. Simulation Studies

The HVDC grid model illustrated in Fig. 6 is used to validate the performance of the protection scheme. The test system is modelled with the PSCAD/EMTDC simulation tool. The network architecture, converter protection logic, breaker model and cable parameters are adopted from [22]. The network is operating at ±320 kV DC in a symmetric monopolar configuration. All DC links are represented based on the frequency-dependent cable mode available in PSCAD library. The modelling approach for the MMCs is based on average value modelling, with the appropriate modifications to accurately represent the converter behavior during the blocking state [25]. Protective relays with DCCBs are placed at each cable end. DCCBs are modelled as hybrid with an operation time delay of 3 ms. The main parameters of the HVDC grid and the MCCs are summarized in Table III.

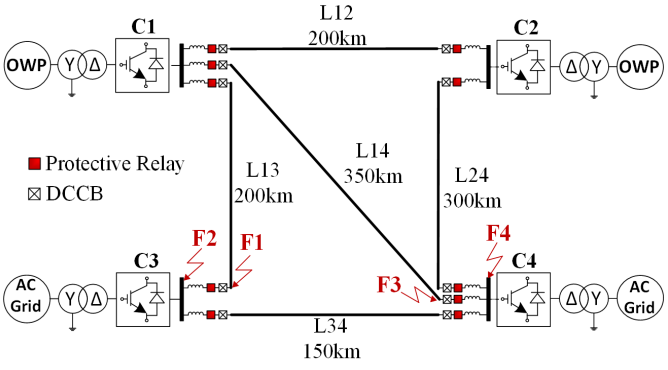


Fig. 6. HVDC grid test system.

TABLE III. System and converter parameters.

Parameter	Value
Nominal DC voltage	± 320 kV
Rated AC (line-to-line) voltage	360 kV
Rated power (C1∼C4)	1000 MVA
Active power setpoint (C1∼C4)	700,700,−800,−600 MW
Reactive power setpoint (C1∼C4)	100,100,−100,−100 MVAr
DC inductors	50 mH
Arm inductance	42 mH
Arm resistance	0.08 Ω
Arm capacitance	31.42 μF

A. Relay Configuration

The relay settings with regards to SWT parameters are calculated based on the approach described in Section III. The sampling frequency is set at 100 kHz. The settings for each protective relay are cited in Table IV (R_{ij} refers to the relay located at the end i of cable L_{ij}).

TABLE IV. Relay configuration settings.

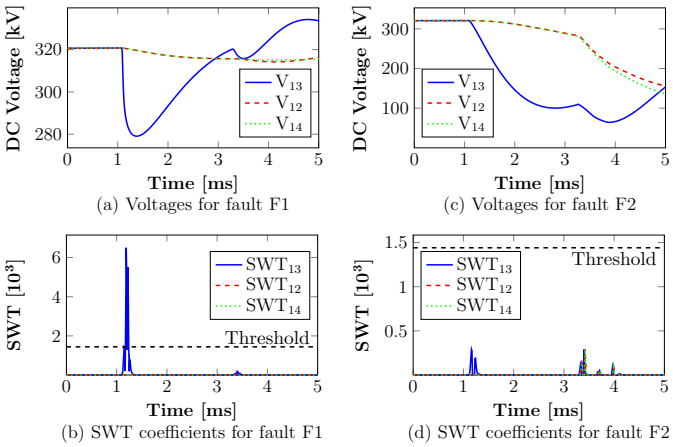
Cable	Relay	Level	Wavelet	Threshold [10^3]
L34	R_{34}	2	sym5	3.750
	R_{43}			3.756
L13	R_{13}	2	sym4	1.441
	R_{31}			1.453
L12	R_{12}	2	sym4	1.457
	R_{21}			1.453
L14	R_{14}	3	db5	2.623
	R_{41}			2.643
L24	R_{24}	3	coif2	3.475
	R_{42}			3.507

Since the cable characteristics, DC inductors and converter parameters of all terminals are the same, the length of the cable and the number of cables connected at the bus adjacent to the relay are the two main factors affecting the relay settings. The relays protecting the shorter cables L12, L13 and L34 use the second level for the calculation of the coefficients. In contrast, longer cables provoke greater attenuation on the high frequency content of the voltage waves and hence, the third decomposition level (lower frequency band) is obtained through (10) and employed by the associated relays. Moreover, several wavelets have been selected using the analytical approach, confirming that it is difficult to choose a single wavelet for all protection relays. In the simulation studies, the SWT detail coefficients calculated by relay R_{ij} are denoted as SWT_{ij}. A SWT detail coefficient is calculated every time a DC voltage measurement is received using (8). The required number of voltage samples for the calculation of each coefficient varies depending on the selected decomposition level and mother wavelet. For instance, 16 samples are required by relays of cable L13 that use wavelet *sym*4 at level j=2.

B. Verification of the Proposed Method

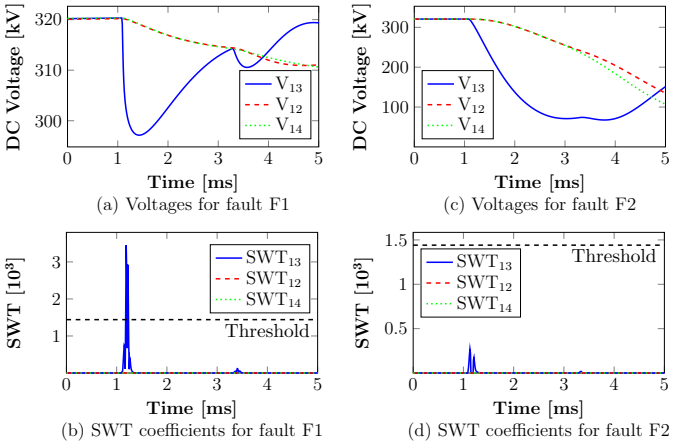
This subsection validates the performance of the protection scheme and its effectiveness in discriminating between internal and external faults. An internal fault is applied at the end of cable L13 (location F1 in Fig. 6), and a solid external fault is applied at location F2. All faults occur at t=0 ms.

1) Pole-to-pole (PTP) faults: Fig. 7 shows the results for PTP faults at fault locations F1 and F2. The fault resistance of the faults is 500 Ω and 0.01 Ω, respectively. In both cases, after approximately 1.1 ms (due to the time it takes for the travelling wave to reach relay R_{13}) the DC voltage starts to fall (Fig. 7(a) and 7(c)). In Fig. 7(b), SWT_{13}, the wavelet coefficients of the DC voltage for fault F1 demonstrate a WMM of 6.23 10^3, which clearly exceeds the calculated threshold, approximately 120 μs after the fault wave reaches the relay location. Hence, an internal fault is detected at very high speed and a trip signal is sent to the associated DCCB. Moreover, the wavelet coefficients calculated by the rest relays of the terminal (R_{12} and R_{14}) are also shown in the same figure for comparison. It is evident that there is no visible change in magnitude of the coefficients. On the contrary, SWT_{13} for the external fault at F2 (Fig. 7(d)) has a maximum WMM of 0.288 10^3, which is well below the threshold and therefore, no trip signal is generated. Moreover, for fault F2, converter protection is activated around 3.3 ms, nevertheless, the generated SWT coefficients at this instance are well below the threshold.



(a) Voltages for fault F1 (c) Voltages for fault F2
(b) SWT coefficients for fault F1 (d) SWT coefficients for fault F2

Fig. 7. Waveforms during PTP faults at locations F1 (R_f=500 Ω) and F2 (R_f=0.01 Ω).



(a) Voltages for fault F1 (c) Voltages for fault F2
(b) SWT coefficients for fault F1 (d) SWT coefficients for fault F2

Fig. 8. Waveforms during PTG faults at locations F1 (R_f=500 Ω) and F2 (R_f=0.01 Ω).

2) Pole-to-ground (PTG) faults: A positive PTG fault is applied at fault locations F1 (Fig. 8(a) and 8(b)) and F2

(Fig. 8(c) and 8(d)) with the same fault resistances as in the previous scenario. For a PTG fault at F1 the derived wavelet coefficients SWT_{13} are smaller in magnitude compared to those for a PTP fault. Nevertheless, the coefficients reach a value of 3.45 10^3, thus exceeding the threshold and an internal fault is detected almost instantaneously (in less than 150 μs). Hence, the proposed method can successfully detect internal PTG faults with weaker fault transients. For fault F2 the coefficients do not exhibit any significant change (WMM of 0.268 10^3) and no DC fault is detected. In this study also, there is no detectable change in the magnitude of SWT_{12} and SWT_{14}.

C. Influence of Fault Resistance

Fig. 9(a) compares the WMM of SWT coefficients calculated by R_{13} for PTP and PTG DC faults at location F1 against the selected threshold to demonstrate the sensitivity of the protection system. The results indicate that as fault resistance increases, the magnitude of SWT coefficients diminishes due to greater attenuation of the fault voltage wave. However, even a PTG DC fault with R_f=1000 Ω can be successfully discriminated from a solid fault at F2. The same analysis is performed for cable L14 for an internal fault at F3 and external fault at F4 (Fig. 9(b)). The incident voltage wave experiences higher attenuation due to the greater length of L14, resulting in smaller SWT coefficients as calculated by R_{14}. Consequently, the maximum fault resistance (for a PTG fault) that can be discriminated is just below 500 Ω. It is promising that even when a conservative reliability factor is used for determining the protection threshold (i.e. k=5), the method still demonstrates enhanced protection margin.

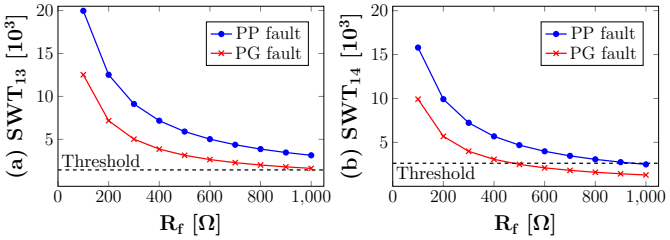


Fig. 9. Maximum SWT coefficient as a function of fault resistance for PTP and PTG faults on cables (a) L13 and (b) L14.

D. Influence of Noise

To demonstrate the performance of the proposed method in a noisy environment, the monitored voltage measurements for the same fault scenarios of the previous subsection are contaminated with artificial white noise to obtain different Signal-to-Noise Ratios (SNR), starting from 50 dB until 5 dB (lower dB values correspond to higher noise level). The WMMs in all cases are presented for relays R_{13} in Fig. 10(a), and R_{14} in Fig. 10(b). In both cases, the SWT coefficients are not affected by noise when SNR is equal or higher than 20 dB. For SNR equal or lower than 15 dB, the impact of noise becomes greater than the impact of the induced transients from the external faults F2 and F4, but still the SWT coefficients do not exceed the selected thresholds. An example is shown in Fig. 11 for SNR=20 dB, where the DC voltage for faults F1 and F3 is zoomed to illustrate the noise impact. It is noteworthy that noise has less impact on the calculated coefficients by R_{14}. This is attributed to the fact that a lower frequency band is assigned to the third level used for the calculation of coefficients SWT_{14} and hence, high frequency noise is filtered out.

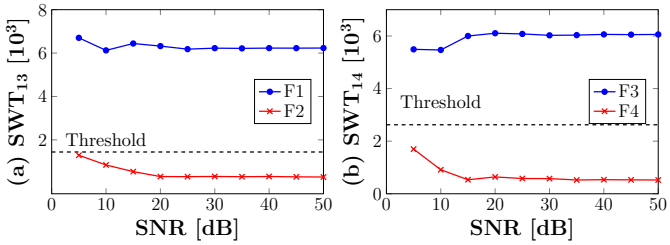


Fig. 10. Maximum SWT coefficients at different noise levels for internal and external PTP faults on cables (a) L13 and (b) L14.

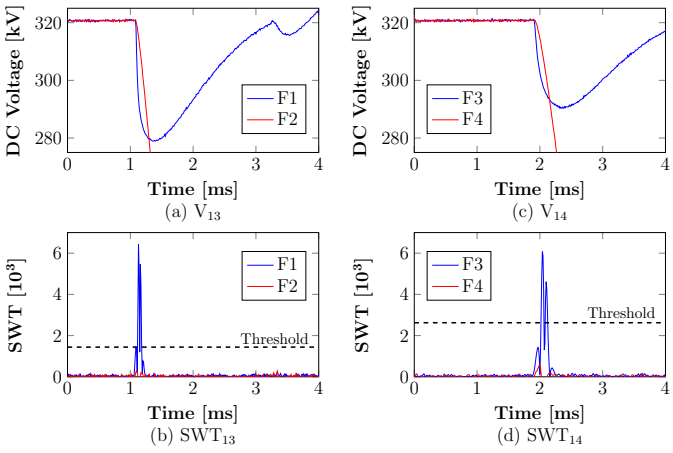


Fig. 11. Voltage profiles and SWT coefficients for SNR=20dB.

E. Influence of Sampling Frequency and ROCOV Comparison

Faults F1 and F2 are repeated for different sampling frequencies to investigate their impact on the proposed method. The same analytical methodology of Section II can be applied for different sampling frequencies, resulting in different frequency bands and calculated thresholds. Table V cites the corresponding thresholds and the WMM_{F1}/WMM_{F2} ratios in each case for sampling frequencies ranging from 10 kHz to 100 kHz. The thresholds are given for a reliability factor k=1. It can be seen that lower sampling frequencies still deliver enough confidence for discriminative DC fault detection.

Moreover, the maximal detectable fault resistance for the internal fault (F1) is cited in Table V for each sampling frequency. The studies are repeated for another voltage-based non-unit protection method for comparison. The selected method for comparison is the Rate of Change of Voltage (ROCOV) that was proposed in [7], and the corresponding maximal detectable fault resistances for all sampling frequencies are also derived and cited in Table V. The same reliability factor (k=5) is used in all cases. It is evident that as sampling frequency decreases, the maximal detectable fault resistance

is reduced. Nevertheless, the proposed method demonstrates significantly improved performance in terms of resiliency to highly resistive DC faults for all sampling rates.

TABLE V. Protection thresholds, WMM_{F1}/WMM_{F2} ratios and comparison with ROCOV for different sampling frequencies.

f [kHz]	10	20	40	60	80	100
Threshold [10^3]	6.72	2.27	0.994	0.612	0.397	0.288
WMM_{F1}/WMM_{F2}	2.68	6	10.46	13.21	17.25	21.64
SWT Max R_F [Ω]	240	629	1128	1551	2044	2259
ROCOV Max R_F[Ω]	55	127	211	271	370	393

F. Robustness of Proposed Method

This subsection investigates the robustness of the method against external disturbances such as, AC faults, active power changes and DCCB operation. The protection scheme should remain idle and not react during these events. A three-phase fault at the AC side of converter C1, a power order change from 800 MW to 0 MW for converter C1 and a trip event of the DCCB next to relay R_{12} are put forward for this analysis. The DC voltage is monitored by R_{13} and the measurements are displayed in Fig. 12(a). The corresponding SWT coefficients are illustrated in Fig. 12(b). The three-phase fault and the power change have minimal impact on the coefficients' magnitude, whereas the DCCB operation provokes a significant spike, which exceeds the corresponding WMM for a fault at F2. Therefore, it is likely that a breaker opening will cause maloperation of the protection. The selected reliability factor (k=5) of the proposed method ensures that a breaker tripping action does not interfere with the fault detection method.

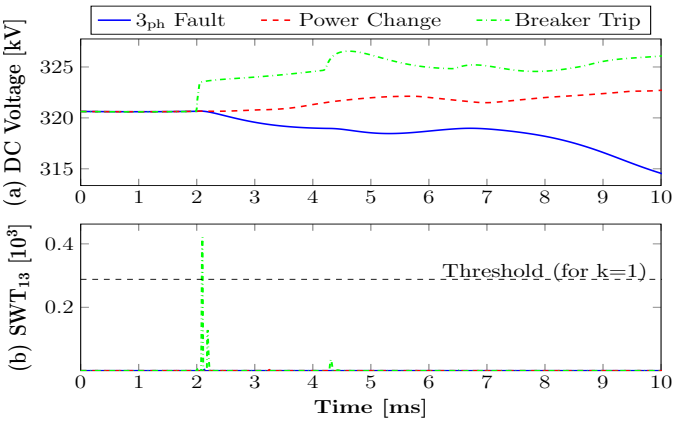


Fig. 12. Waveforms captured by R_{13} during external disturbances: (a) DC voltages and (b) SWT coefficients.

V. Real-Time Validation of the Proposed Method

To further corroborate the results and to evaluate the practical feasibility of the method, a hardware-in-the-loop simulation has been performed. Real-time Digital Simulator (RTDS) has been used in order to represent the behavior of the 4-terminal HVDC grid of Fig. 6. The proposed method has been implemented using the Texas Instruments (TI) TMS320F28379D Digital Signal Processor (DSP) [26]. Fig. 13 shows the arrangement of the test platform.

The DSP receives analog DC voltage measurements at the relay point from an analog output channel provided by the RTDS. The input signals have been scaled down to fit the operating range of the DSP (0–3.3 V). When the DSP detects an internal DC fault, a digital trip signal is generated and sent to a digital input port of the RTDS. The DSP receives the measurements at 100 kHz. Moreover, an analog output channel of DSP is available for monitoring of the SWT coefficients.

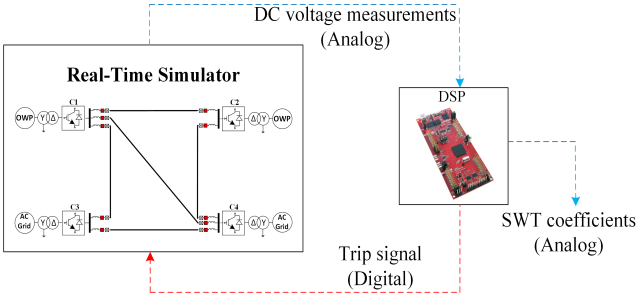


Fig. 13. Test platform arrangement.

For direct comparison with the offline simulations, PTP faults are applied at locations F1 (R_f=500 Ω) and F2 (solid fault). The DSP simulates the operation of Relay R_{13}. Fig. 14 shows the fault voltage profile, the SWT coefficients and the trip signal for the internal fault F1. The SWT coefficients rise significantly above the threshold and hence, a DC fault is successfully discriminated and a trip signal is generated. Similar to the offline simulation, the method operates at very high speed, producing the trip signal 120 μs after the fault wave reaches the terminal.

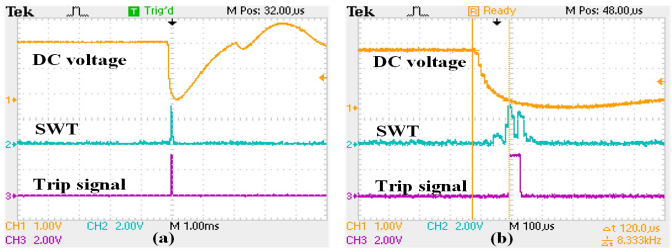


Fig. 14. Real time simulation results for the internal fault F1: a) overall view, b) zoomed view.

To demonstrate the closed-loop operation and the successful coordination of the proposed method with the DCCBs that are embedded within the simulated system, the pole currents i_{dc13p} and i_{dc13n} are shown in Fig. 15(a). The current measurements are obtained through the RSCAD RunTime module of RTDS. For simplicity, the digital trip signal that is generated by the DSP is used to trigger the operation of both positive and negative pole breakers of cable 13. Moreover, the tripping signal (denoted as $BrkTrip$) and the breaker operation signal (denoted as $BrkOp$) are also captured via the RTDS and the results are shown in Fig. 15(b). It can be seen that the fault is detected very early in the fault current rising stage. Subsequently, the DSP trip signal is received by the RTDS resulting in the operation of the breaker (3ms operation time) and in the successful fault current interruption.

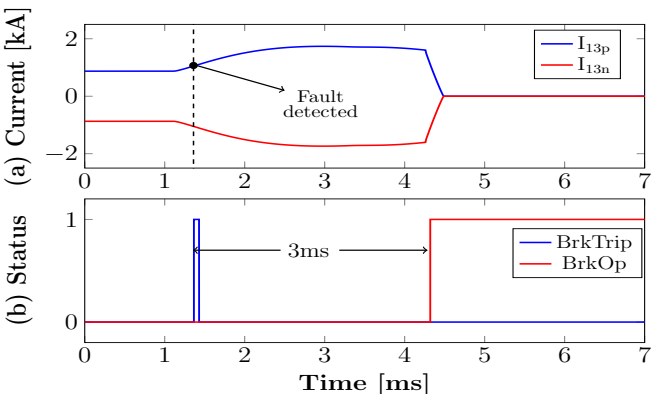


Fig. 15. Fault current signatures during fault detection and interruption process for the internal fault F1.

Fig. 16 presents the results for the external fault F2, where the voltage measurements are contaminated with noise (Fig. 16(a)) in order to test the performance of the method in a noisy environment. Fig. 16(b) demonstrates that the protection method does not react to the external fault, thus validating the capability of the method to selectively detect DC faults.

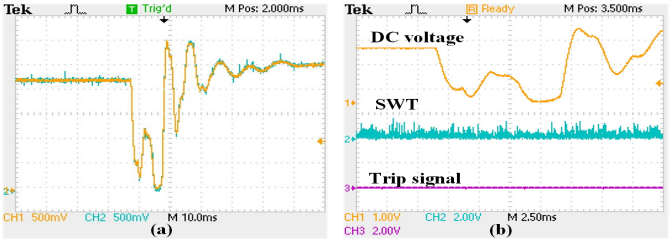


Fig. 16. Real time simulation results for the external fault F2: a) noise impact on measured voltage, b) protection scheme response.

It is worth noting that the algorithm is successfully executed at the relatively high sampling rate of 100 kHz and that no overruns were noticed. The results provide a high level of confidence that the proposed method is effective, practical and cost-effective despite the small available scale for voltage conversion of the deployed hardware and the presence of noise.

VI. Conclusion

In this paper, a non-unit protection scheme for detecting and discriminating DC faults in HVDC grids based on wavelet transform has been proposed. A generalized analytical approach, adaptable to any HVDC grid topology has been developed for deriving the main WT design parameters based on frequency domain analysis, thus avoiding the need for extensive offline simulations. Although proven for symmetrical monopolar systems, the analytical approach for WT-based HVDC grid protection design is also applicable to bipolar systems. In detail, the optimum wavelet decomposition level, mother wavelet and protection threshold are flexibly derived for each relay separately according to the prevailing local system conditions in order to achieve the highest performance of the method. SWT has been proposed amongst the WT variants to maximize the performance of the protection scheme. Offline simulations conducted in PSCAD demonstrated the effectiveness of the proposed method, and it has been found that the scheme can provide fast, reliable and selective protection even against highly-resistive DC faults. Further analysis demonstrated robustness against external disturbances and immunity against noise, while a sensitivity analysis revealed that the method can be executed in lower sampling rates (i.e. 10 kHz). Finally, with the use of a real-time simulator and a low-cost hardware prototype, the practical feasibility of the scheme has been confirmed.

VII. Acknowledgments

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Appendix

All cables are modelled based on the frequency dependent (phase) model of the PSCAD software. Fig. 17 illustrates the cables configuration and Table VI shows the cable parameters.

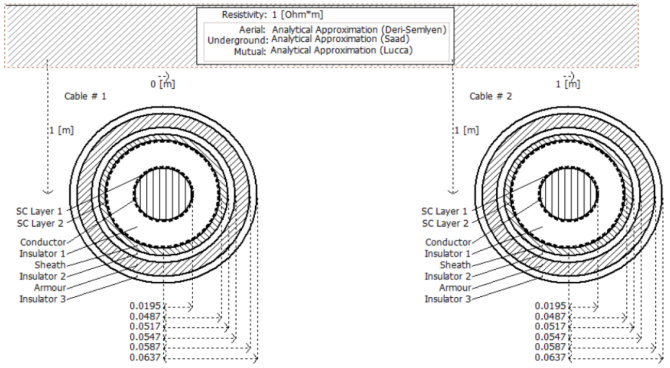

Fig. 17. Cables configuration [22].

TABLE VI. Cable parameters.

Layer	ρ [Ωm]	ϵ_{rel} [-]	μ_{rel} [-]
Core	1.7e-8	-	1
Insulation	-	2.3	1
Sheath	2.2e-7	-	1
Insulation	-	2.3	1
Armour	1.8e-7	-	10
Insulation	-	2.3	1

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