

Automated Nanoscale Absolute Accuracy Alignment System for Transfer Printing

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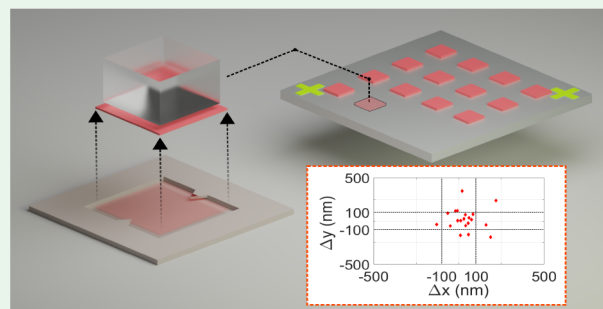


Supporting Information

ABSTRACT: The heterogeneous integration of micro- and nanoscale devices with on-chip circuits and waveguide platforms is a key enabling technology, with wide-ranging applications in areas including telecommunications, quantum information processing, and sensing. Pick and place integration with absolute positional accuracy at the nanoscale has been previously demonstrated for single proof-of-principle devices. However, to enable scaling of this technology for realization of multielement systems or high throughput manufacturing, the integration process must be compatible with automation while retaining nanoscale accuracy. In this work, an automated transfer printing process is realized by using a simple optical microscope, computer vision, and high accuracy translational stage system.

Automatic alignment using a cross-correlation image processing method demonstrates absolute positional accuracy of transfer with an average offset of <40 nm ($3\sigma < 390$ nm) for serial device integration of both thin film silicon membranes and single nanowire devices. Parallel transfer of devices across a 2×2 mm² area is demonstrated with an average offset of <30 nm ($3\sigma < 705$ nm). Rotational accuracy better than 45 mrad is achieved for all device variants. Devices can be selected and placed with high accuracy on a target substrate, both from lithographically defined positions on their native substrate or from a randomly distributed population. These demonstrations pave the way for future scalable manufacturing of heterogeneously integrated chip systems.

KEYWORDS: hybrid integration, microassembly, precision alignment, transfer printing, integrated optics, nanophotonics



1. INTRODUCTION

Historically, integrated photonic chips have been implemented in a wide range of material systems dependent on the application. For example, III–V materials for on-chip laser sources,¹ silicon for large-scale passive signal processing,² or glass for lab-on-a-chip use.³ To realize true single chip systems, it is necessary to integrate multiple materials together, on a common substrate, to cover the required range of functions. Furthermore, the integration process must meet two crucial criteria for future scaling of photonic integrated circuits (PICs): (1) potential for automated, high throughput parallel processing and (2) high accuracy alignment of waveguide devices on different material layers. The integration of electrically pumped diode lasers with silicon photonics has provided much of the early work in this field and is now reaching a significant level of maturity.⁴ The common method of wafer or die bonding onto a prefabricated passive optical chip, followed by fabrication of active optoelectronic devices in situ, meets the required scaling criteria and is suitable for applications requiring the integration of only two materials. However, in applications requiring the integration of multiple materials on a single chip, the requirement to reprocess the full system by using multiple die bonds may be prohibitive,

especially for densely packed layouts. Recent reviews on photonic integrated circuits for quantum optical applications, for example, show both the breadth of function that can be achieved and the need for dense integration of devices from multiple, complementary materials.^{5–7} Similar requirements can be envisaged for all-optical computing and telecommunications applications.^{8–10}

An alternative to die bonding and postprocessing is the use of back-end microassembly techniques. Devices in complementary materials can be fully fabricated on their native substrates and then integrated by using a pick-and-place process. Of the various forms of this technique, transfer printing (TP) is a particularly attractive example.¹¹ Transfer printing allows for both the large-scale transfer of significant numbers of micrometer scale devices on planar,¹² deformable,¹³ and nonplanar substrates¹⁴ and the high precision

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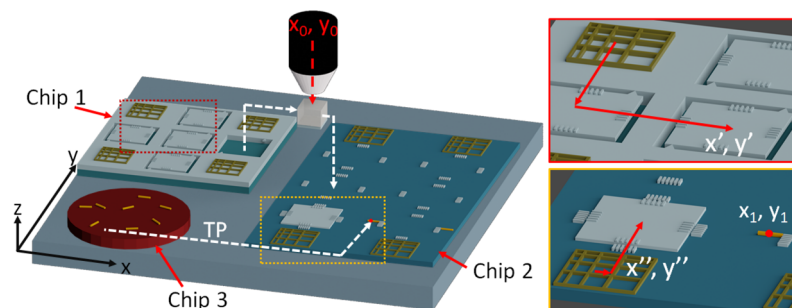


Figure 1. Schematic of the TP setup for the absolute cross-correlation alignment method. Two types of donor chips are shown: one containing lithographically defined registration markers (chip “1”, upper left) and the second with randomly distributed devices (chip “3”, lower left). The receiving chip is shown with lithographically defined registration markers and target patterns (chip “2”, right). The imaging column is situated above the motion stage, with the TP stamp head centered to its FOV (x_0, y_0). Labeled are the local coordinate points of a device-of-interest and its target print position (x', y' ; x'', y'') and the target print position of a NW device (x_1, y_1). Each are calculated from their local coordinate systems and referenced to the global coordinate system.

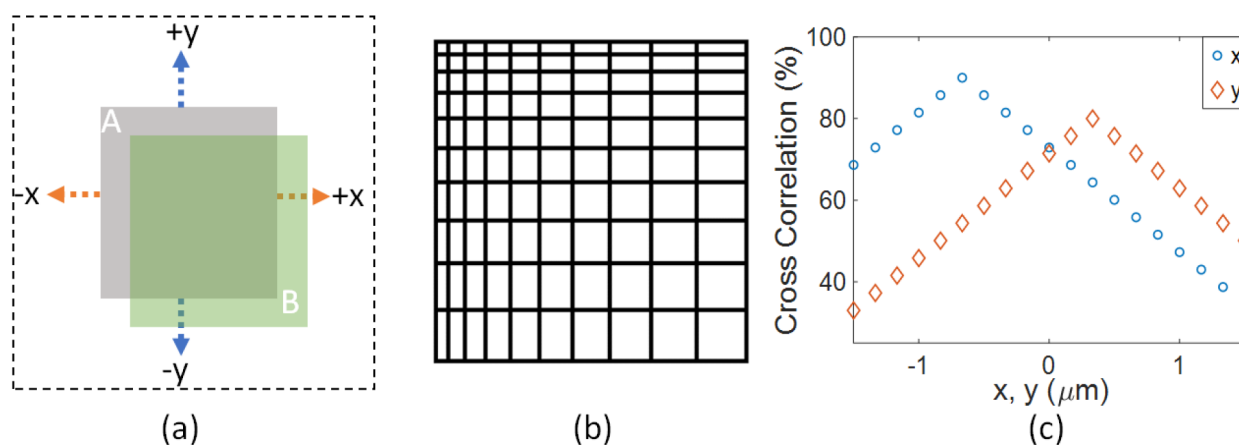


Figure 2. (a) Schematic of the cross-correlation of two objects A and B with a relative lateral displacement within a fixed FOV region. (b) Optimized alignment marker design for optical microscopy cross-correlation. (c) Theoretical plot of cross-correlation as a function of lateral displacement in x and y dimensions.

alignment between prefabricated waveguide devices with cross-sectional dimensions in the hundreds of nanometers range.^{15–17} Current approaches to accurate device alignment depend on either high resolution electron beam imaging systems¹⁸ or skilled user operation of the pick and place tool to assess the overlay marker registration positioning. This limits the throughput and yield of these systems. Complementarily, for systems that can handle large numbers of devices, the optical microscopy-based transfer printing methods based on standard edge detection marker registration alignment produces layer-to-layer alignments with an alignment accuracy currently stated at $\pm 1.5 \mu\text{m}$ (3σ).¹⁹

In this work an automated absolute position measurement technique is presented based on simple optical microscopy imaging. The technique uses cross-correlation imaging that allows for positional registration with an accuracy better than can be achieved using standard edge detection marker registration. This method has been used previously in technologies from single particle analysis,²⁰ fingerprint matching,²¹ and electron-beam lithography, with the potential for nanoscale accurate alignment.^{22,23} Furthermore, as this is an automated technique, many devices can be printed both serially and in parallel using a single alignment step to reference the donor and receiving chips to a common reference grid system. Quantitative results are presented for device

printing accuracy with respect to lateral and rotational errors. The method is demonstrated for serial and parallel printing of devices where they are rigidly connected to their original fabrication layout, allowing the use of lithographically defined registration markers. Furthermore, the method is also used to print devices initially randomly distributed on their native substrate.

2. EXPERIMENTAL SECTION

Accurate Absolute Alignment Technique. In high accuracy microassembly systems, the central problem is to define the positions of components from two separate chips with respect to a global coordinate system. A schematic of the situation is shown in Figure 1. The transfer printing system shows two donor chips and a single receiving chip rigidly bonded to a nanoprecision 5-axis motion stage. An imaging column is located above the stage, with a polydimethylsiloxane (PDMS) stamp used for device printing centered in the imaging field-of-view (FOV) and located between the imaging column and motion stage. Both the column and stamp are rigid elements of the system, with all movement achieved solely by the stage. The relevant TP methods are detailed in the Methods section. In this arrangement it is convenient to define the common coordinate system in terms of x and y (or the system R), corresponding to the rigid surface of the print tool's translation stage in the x – y plane. Chip “1” represents a donor chip where the internal coordinate system, R' , holds between the lithographically

defined registration markers and the devices to be printed. Chip “2” represents the receiving host chip where the devices are to be printed, corresponding to a coordinate system, R' , defined relative to lithographically registered markers on that substrate. Finally, chip “3” corresponds to a case where there is no predefined coordinate system between the substrate and the randomly positioned devices to be picked from its surface. By use of any registration marker alignment process, both R' and R'' can be related to R by locating their registration markers within the field of view (FOV) of the optical microscope rigidly connected to the print tool translation stage base. The accuracy with which this transform can be performed is typically limited by the optical microscope resolution and the edge detection methods used to define the position of the marker relative to the microscope FOV.

In this work an alternative to measuring the effective center of area of registration markers using edge detection techniques is presented. Cross-correlation measures the similarity of an object (A) with a secondary object (B) as a function of their relative displacement,²⁴ as shown in the schematic of Figure 2a. By use of nominally identical objects (A) and (B), the cross-correlation function will have a global maximum where the two objects are exactly overlapped in space. This function can then be used to locate an object, for example a registration marker, in the fixed FOV of the optical microscope. Because this FOV has a fixed relationship to R , defining R' and R'' with respect to the FOV allows definition of a common coordinate system. The advantage of using the cross-correlation method for positional registration of objects is that it is not dependent on detecting edges of objects in the image, but rather on the relationship between the spatial features of the object.

The second object used in the cross-correlation calculation is an ideal virtual object, nominally identical with the on-substrate object. This virtual object is cross-correlated to the imaged object using its relative position to the center of the FOV, referencing the position of the imaged object in this FOV and therefore R . Consequently, the positional accuracy is dependent on the displacement offset resolution of the cross-correlation measurement, i.e., the imaged pixel dimensions, rather than the imaging system's optical resolution. The relative displacement between virtual and real images is achieved by lateral shifts of the virtual marker image within the FOV using iterative pixel offsets in both axes, with the lateral positional offset calculated from the pixel dimension. The pixel dimension is measured by calibrating to an object of known size; in this instance, we use an electron-beam fabricated alignment marker. For the imaging system magnification in use, a pixel size of ~ 160 nm is calculated. Further experimental analysis is provided in the Supporting Information, section 2.1. The cross-correlation procedure for aligning on-chip and virtual marker images is as follows: (1) An on-chip alignment marker is positioned in the center of the FOV by using a standard overlay method and the marker image captured by the imaging system. To minimize any spatial distortions, the markers are imaged through a flat section of the PDMS stamp. Binary thresholding is performed on the captured images prior to the alignment process to improve marker image contrast. (2) The captured image is cross-correlated against a range of virtual marker images, each with a known relative displacement to the center point of the FOV by iterative pixel offsets in the lateral axes. (3) The spatial similarity between the acquired image of the on-chip marker as a function of each virtual marker image is calculated, providing a position of optimum overlap corresponding to pixel number offset. (4) The motion stage's coordinate readings in R are determined for the point of maximum correlation, providing absolute reference for the imaged object. Following the initial manual positioning of the on-chip alignment marker to the center FOV, the calculation and recording of the on-chip coordinate system takes less than a minute to complete. This process can be repeated at intervals during a fabrication session incorporating multiple printing stages, calibrating against any subsequent misalignment as a function of relative drift over time experienced by the motion stages. In our particular system stage drift is less than 50 nm over a 30 min period, allowing for multiple print steps to be performed by using a single alignment step in this period.

This drift can be further reduced through use of optimized translation stages, e.g., stick-slip drives.

Individual substrate rotation is also calculated through the use of multiple alignment markers fabricated on the same sample, with a known single-axis separation. By translating each alignment marker independently to the center point of the FOV by the known separation, the sample-to-stage rotational offset can be calculated by the lateral offset of each marker's relative position in the FOV. The sample-to-stage rotational offset is compensated by the rotational module of the motion stage prior to any device printing. All marker coordinate registration and x - and y -axis motion during transfer printing is computer controlled and fully defined by the cross-correlation alignment procedure, requiring no postalignment user correction to the device pick-up and target print coordinates. The z -direction of movement, enabling device release from the donor chip and placement onto the target receiver chip, is manually controlled by the user once the target x - y coordinates are obtained by software control.

The registration alignment markers here are fabricated in the same lithographic scheme as the donor and receiving devices. For cross-correlation alignment, specific marker properties are required for optimal performance. The calculated cross-correlation, as a function of offset between the imaged and virtual markers, should exhibit a global maxima with few local maxima and a high gradient of correlation reduction as a function of spatial offset. In terms of 2-dimensional spatial pattern, this means creating a wide spatial frequency range using a noncentrosymmetric design.²⁵ Furthermore, the design should also be easily fabricated, with micrometer-scale features providing high contrast and sharply resolved edge information in simple microscopy systems. To meet these criteria, the alignment marker used is an aperiodic grid geometry, shown in Figure 2b, and further detailed in the Supporting Information, section 1.2. Sample autocorrelation functions of this design as a function of relative displacement in the x and y directions are shown in Figure 2c. The correlation peaks do not reach 100% since the initial coarse alignment of the two images includes some offset in both x and y .

Experimental Setup. The printing system employs a 6-axis motion stage for positioning of samples relative to the fixed print head. The motion assembly comprises of three piezo-driven linear stages for the X , Y , and Z motion and two goniometer stages for tip and tilt control with yaw controlled by a rotational stage. All stages employ optical encoders for internal position reference. The individual linear stages are specified at ± 25 nm resolution, with ± 75 nm for vertical movements. The goniometer and rotation stages are accurate to ± 4.36 μ rad. The optical system used to image through the transparent stamp uses a 10 \times PLAN APO long working distance microscope objective with a numerical aperture of 0.3. The optical system is motorized, providing controlled focus and zoom capabilities. The FOV thus obtained can range from 840×620 μm^2 down to 140×110 μm^2 , with the largest available FOV providing an optical resolution below 1 μm . The images are captured by using a 1.4 megapixel sensor CCD camera. The full printing process includes an initial setup time, a fine marker registration process, and the physical pick and placing of devices between substrates. The system setup including sample mounting, coarse alignment, location of markers, and global rotation compensation typically takes around 30 min to complete. The automated fine marker registration process takes less than 1 min to complete, and a single pick and place operation takes around 2 min. This last stage is limited by current requirements for user control over z -directional motion in the pick and place stage and could be significantly improved through automation.

Optical Registration Accuracy. Before carrying out the full microassembly characterization, the resolution of the alignment procedure itself was measured. Two registration markers were fabricated using electron beam lithography on a single substrate with a well-defined separation. The marker-to-marker separation error due to the electron beam process is on the order of a few nanometers. These markers were then registered individually to the global coordinate system using the cross-correlation method. The experimental measurements deviated from the known marker separation by

less than 56 ± 38 nm. This is significantly lower than current optical registration techniques, including the theoretical limit to standard edge detection optical techniques set by the optical imaging setup ~ 160 nm pixel dimension. Full details of the measurement are provided in the Supporting Information, section 2.2.

3. RESULTS AND DISCUSSION

Transfer Printing of Silicon Membranes. To characterize the positional accuracy of the full transfer printing process, thin-film silicon suspended $100 \mu\text{m}^2$ membranes were printed onto a silicon receiving substrate. The procedure was demonstrated for both individual and parallel printing schemes. The alignment of the individual printed devices in both cases is fully analyzed using dedicated vernier scales on the printed membranes and at their respective targeted positions on the receiving chip, as shown schematically in Figure 3a. Each membrane (Figure 3b) and receiving chip

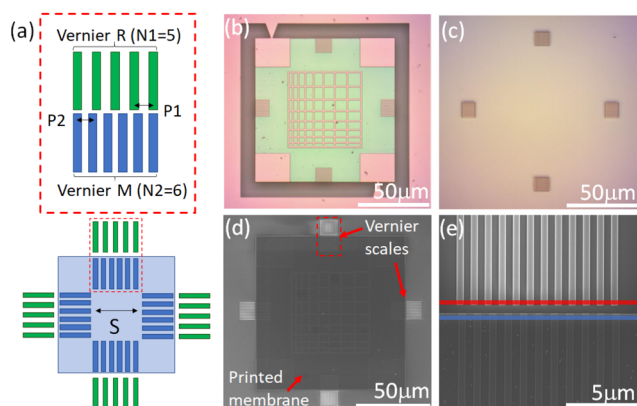


Figure 3. (a) Diagram of vernier scales, showing the grating pitch variation for P_1 and P_2 , number of gratings, and scale separation S . The blue shaded area depicts the printed membrane, containing the half-vernier scale bars. Optical images of the (b) suspended membrane and (c) target receiving substrate vernier scales prior to TP. (d) SEM image of membrane transferred to target SOI substrate with aligned vernier scales. (e) Magnified image of the aligned receiving substrate (upper) and membrane (lower) vernier gratings with colored lines detailing regions of intensity profile analysis.

target position (Figure 3c) has four sets of scale bars on each cardinal face that form half of the vernier scale as shown in Figure 3a. In addition, the silicon membranes have each a unique central registration marker. The silicon membranes and silicon-on-insulator (SOI) receiving chip were fabricated on a SOI wafer comprising a 220 nm thick silicon core and $2 \mu\text{m}$ buried oxide layer. A two-step etch process produces a fully etched silicon membrane with shallow-etched embedded structures. This is followed by an underetch of the buried oxide to fully suspend the membranes, with the fabrication detailed in full in ref 26. The structures on the receiving chip are fully etched into the core silicon layer of the SOI material.

Top-view scanning electron microscope (SEM) images of the transferred devices were captured and analyzed to measure the lateral and rotational accuracy of the printing. An example is shown in Figure 3d, with the magnified image detailing the positional alignment capability of the membrane and target vernier gratings (Figure 3e). SEM imaging of the devices' individual verniers provides information about lateral offsets on each face of the membrane and, taken together, global rotation of the membrane device with respect to its target position. An

intensity profile of the SEM image is used to calculate the centroid of each grating at the positions signified by the blue and red lines in Figure 3e. The overall grating pitch variance between the upper and lower vernier is measured as a function of pixel offset, with the SEM length scale converting pixel number to length in nanometers. The average pixel size with respect to the SEM measurement scale is 10 nm. The measurement resolution is related to the edge detection of the captured SEM images. Full details of this measurement scheme can be found in the Supporting Information, section 3.

Figures 4a,b show plots of the lateral and rotational accuracy data for the individually printed devices, measured for 20 device prints. The red all-dashed area within Figure 4a corresponds to a lateral misalignment below ± 500 nm, while the green dot-dashed area is below ± 100 nm. The percentage of devices that lie within the ± 100 nm region is 55%, with all printed devices situated within the 500 nm region. The measured values are detailed in Table 1, demonstrating results well below the submicrometer level. An absolute alignment accuracy of ± 249 nm (3σ) is achieved for the x -axis and ± 384 nm (3σ) for the y -axis. An average misalignment of 38 nm and rotational offset of ± 6 mrad (3σ) is measured across the full device range.

To demonstrate the scalability of the technique, a 5×5 array of 25 silicon suspended membranes was transferred in a single manipulation. The process uses the same cross-correlation method as the individual device transfer, aligning the membrane array to a complementary array of vernier scales situated on the target SOI chip. With a pitch of 0.5 mm between devices, the effective area of devices printed in parallel was $2 \times 2 \text{ mm}^2$. Figures 4c,d contain plots for lateral and rotational alignment accuracy for the parallel printed devices. Similarly to the individual printing results, the spread of lateral displacement values are centered around zero. Out of all printed devices 36% lie within the 100 nm region, with 91% situated within the ± 500 nm region. Several outlier are exhibited as a result of the magnified effects of tip and tilt within the system across the large printing area. Increased tilt variations cause additional lateral forces during both pickup and placement steps. An overall absolute alignment accuracy of ± 489 nm (3σ) is measured for the x -axis and ± 705 nm (3σ) for the y -axis. The average misalignment is calculated as 30 nm. The rotation is shown to increase slightly from the individual printing with an offset of ± 12 mrad (3σ). For the parallel transfer a success rate of 22 out of 25 printed devices provides a yield of 88%. The main reason for reduction in yield is due to collapse of membrane devices, prior to and during device pickup. The etched membrane thickness is 150 nm, making them extremely flexible and capable of deforming sufficiently to allow contact of their underside surface with the exposed silicon substrate over which they are suspended. Once in contact with the substrate, the membrane cannot be detached from the donor chip. The membrane collapse can be caused by mechanical shock, surface tension effects during the vapor etch, or the mechanical deflection induced when the transfer printing stamp is brought into contact. This would be improved by using stiffer membranes or incorporating a thicker sacrificial etch layer. Cross-correlation alignment of lithographically registered devices is achieved with submicrometer alignment accuracies for both individual device and parallel device printing. The results demonstrate the possible use of the technique as a future wafer-scale device integration technology.

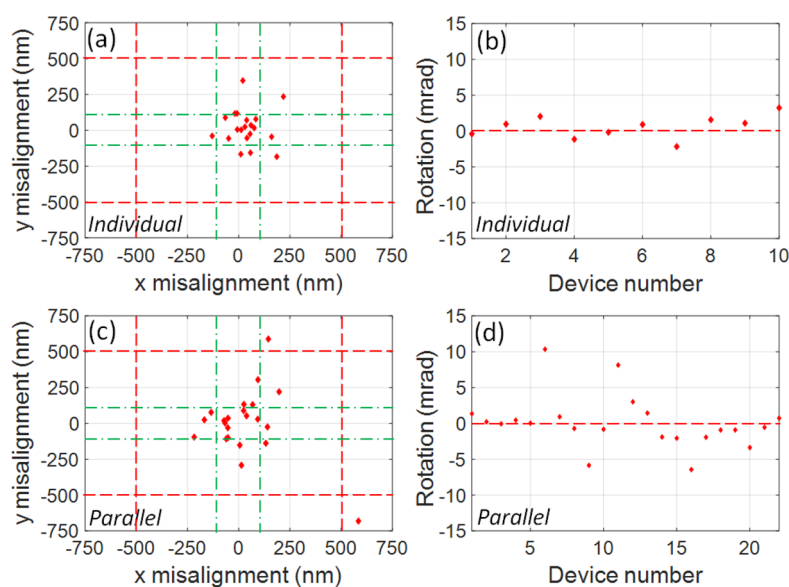


Figure 4. (a, b) Positional accuracy measurements of spatial and rotational misalignment offsets for the individual transferred membrane case. (c, d) Positional accuracy measurements of spatial and rotational misalignment offsets for the parallel transfer case.

Table 1. Lateral and Rotational Alignment Accuracy Results for Both Lithographically Registered and Randomly Distributed Devices

individual membranes	av error	σ	3σ
horizontal (\pm nm)	38	83	249
vertical (\pm nm)	20	128	384
rotational (\pm mrad)	0	2	6
parallel membranes	av error	σ	3σ
horizontal (\pm nm)	30	163	489
vertical (\pm nm)	4	235	705
rotational (\pm mrad)	0	4	12
NW devices	av error	σ	3σ
lateral (\pm nm)	-22	110	328
rotational (\pm mrad)	0	15	45

Transfer Printing of Semiconductor Nanowires. The alignment method can be slightly modified to allow accurate printing of devices whose position on their native substrate is not defined by lithography, for example, collections of nanowire lasers,²⁷ nanopillars, and quantum-dot clusters. In these cases the positional referencing of the donor devices must be made by using the devices themselves as registration markers rather than by using separate structures. The NWs used in this demonstration are bulk InP wires grown on an InP substrate by using a bottom-up approach, reported in ref 28. These have an approximate diameter of 260 nm and lengths between 9 and 11 μ m. To reference the object to the system FOV, a NW device is picked up by the PDMS stamp and imaged by using the optical microscope system. Given the large aspect ratio of the NW device, its centroid can be easily obtained in comparison to a simple line object, which also gives a good estimate of the angle its major axis makes with the FOV coordinate system. Other objects, such as disks, could be treated in a similar way by using appropriate virtual reference objects. The receiving substrate can then be referenced to the global coordinate system, **R**, as before. Finally, the receiving substrate is positioned relative to the fixed centroid location of

the NW to allow printing. Detailed printing and alignment procedures are given in the [Supporting Information](#), section 4.

To estimate the absolute positional accuracy of the technique, 10 NW devices were integrated in a serial process, with target half-vernier scales. High-resolution SEM images were then taken to measure the alignment of the printing. [Figure 5a](#) shows SEM images of a transferred NW device,

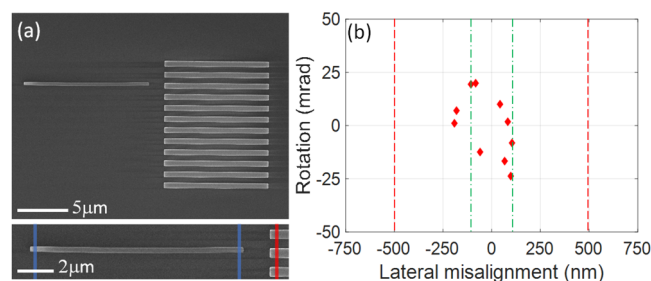


Figure 5. (a) SEM images of a single transfer printed NW device aligned to a vernier scale, with the lower magnified image showing the NW with colored lines detailing regions of intensity profile analysis. (b) Positional accuracy measurements of spatial and rotational misalignment offsets.

aligned to the half-vernier. In this work, only the alignment of the NWs major axis to the target grating lines was carried out. The centroid positions of devices are measured from image intensity profiles at both ends of NWs (blue lines in [Figure 5a](#)) extracted from the SEM images. The centroid coordinate points of the target scales are extracted as before and compared with that of the NW devices. The distance between the two corresponds to the alignment accuracy of the process, with respective pixel dimensions extracted from the image scale bar. [Figure 5b](#) includes the calculated absolute positional and rotational offsets of NW devices integrated with the vernier scale by the aforementioned alignment method. From the plot, it is possible to see that all devices were aligned well within the submicrometer level, with 80% lying within a misalignment range of ± 100 nm. This compared well to the achieved

absolute alignment accuracy of the lithographically registered alignment marker method. The rotational misalignment shows lower accuracy since, in the case of the NWs, the reference object is similar to a line object with one axis from which to measure orientation, further limited by its nanoscale dimensions. As detailed in Table 1, the attainable lateral offset for the NW device TP is ± 328 nm (3σ), with an average misalignment of -22 nm. The rotational accuracy is measured as ± 45 mrad (3σ) across the full NW device range.

4. CONCLUSIONS

In conclusion, we have presented an automated all-optical cross-correlation absolute alignment method with nanoscale accuracy. The method was used to demonstrate the heterogeneous chip-scale integration of both lithographically registered and randomly distributed on-chip devices. A marker-to-marker alignment scheme was implemented to individually integrate fully fabricated suspended membranes across multiple chips. An absolute alignment accuracy of ± 249 nm (3σ) and ± 384 nm (3σ) were achieved for the x - and y -axes respectively, with a rotational accuracy of ± 6 mrad. Alongside this, the parallel printing of a 5×5 array of such membranes over a millimeter-scale range was shown with an absolute alignment accuracy of ± 489 nm (3σ) and ± 705 nm (3σ) for the x - and y -axes respectively, with ± 12 mrad rotational accuracy. Examples of photonic device integration using this methodology have been reported for both vertically assembled passive single-mode and hybrid materials resonators.^{26,29} Furthermore, a second marker-free alignment method demonstrated the integration of submicrometer NW devices. The chip-to-chip integration of individually addressed NW devices with positional and rotational control was achieved with nanoscale absolute accuracies. The measured absolute alignment is ± 328 nm (3σ) with a rotational accuracy of ± 45 mrad. The required print cycle time is dominated by the system setup time and is therefore significant for single device integration. However, this overhead is quickly absorbed when considering scaling the process for high-throughput serial and parallel nanoscale accuracy device processing. This automated alignment system paves the way for the large-scale integration of nanoscale devices in multiple material systems for future optoelectronic systems.

5. METHODS

Micro-Transfer-Printing. Transfer printing of the silicon suspended membranes was performed by using a direct contact approach using no additional surface adhesion promoting layers. A PDMS stamp with a surface area of $100 \times 100 \mu\text{m}^2$ is utilized for printing the suspended membranes. The stamp contains no pyramidal features as utilized by alternative TP processes,³⁰ however, having the pickup and release controlled by careful adhesion control of each contacted surface. The devices are released from their native substrate using a rapid vertical translation of the PDMS stamp head. Once translated to the target print area, the stamp and bonded device are brought into direct contact with the surface. A slow release of the stamp head allows the release and subsequent bonding of the device to the target surface. The relevant cross-correlation alignment between each of the donor and receiving vernier scales was performed prior to transfer.

The NW transfer printing process was performed by using a PDMS stamp head with a surface area of $10 \times 30 \mu\text{m}^2$. The stamp is coarsely aligned with the NW of interest before being brought into contact, with release from the substrate using a rapid vertical translation of the stamp head. The high accuracy alignment to the vernier scales is achieved prior to full contact of the stamp head with the target

surface. This is followed by a slow release transferring the NW to the target substrate with high positional accuracy. The process is detailed fully within ref 31.

Scanning Electron Microscopy (SEM). SEM images were taken by using a field emission SEM (SU8240; Hitachi) at the James Watt Nanofabrication Centre, University of Glasgow. Top-view images were captured without any metal deposition layer to preserve the edge quality of the vernier scale markers.

Data Analysis. We analyzed the data as described in the text and Supporting Information by a Matlab software package using a custom written edge detection and measurement script.

■ ASSOCIATED CONTENT

SI Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsnm.0c02224>.

- (1) Cross-correlation; background theory and outline of the optimized alignment marker design;
- (2) system resolution; imaging system pixel dimension and resolution capability of alignment method;
- (3) vernier measurement procedure; SEM images of membrane vernier structures and theory of measurement technique;
- (4) alignment of randomly distributed on-chip devices with SEM image of NW-vernier integration and description of measurement technique (PDF)

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Author Contributions

J.M., D.J., and B.J.E.G. performed the experiments. J.M. and M.J.S. wrote the manuscript with support from all authors; A.H., M.S., M.D.D., and M.J.S. supervised the project; C.K. fabricated all silicon devices at the James Watt Nanofabrication Centre, University of Glasgow; and M.J.S. conceived of the original idea.

Notes

The authors declare no competing financial interest.

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