Quantifying cell-to-cell variations of a parallel battery module for different pack configurations

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Abstract

Cell-to-cell variations can originate from manufacturing inconsistency or poor design of the battery pack/thermal management system. The potential impact of such variations may limit the energy capacity of the pack, which for electric vehicle applications leads to reduced range, increased degradation along with state of health dispersion within a pack. The latter is known to reduce the accessible energy and the overcharging/discharging of some of the cells within a system, which may cause safety concerns. This study investigates the short-term impact of such effects, which is highly important for designing of an energy storage system. A generic pack model comprising individual cell models is developed in Simscape and validated for a 1s-15p module architecture. The results highlight that a number of cells and interconnection resistance values between the cells are the dominant factors for cell-to-cell variation. A Z shape module architecture show a significant advantage over a ladder configuration due to the reduced impact of interconnection resistance on differential current flow within the module. Current imbalance is significantly higher for a ladder system and its magnitude is not dependent on the module current. Capacity variation does not have a significant impact on the system. By increasing the capacity variation from 9% to 40% the current inhomogeneity increases from 4% to 13%, whilst 25% resistance variation leads to 22% current dispersion. Further, a linear relationship is observed between the current inhomogeneity and thermal gradient (ΔT). A 30℃ ΔT leads to 24% current variation within the module.

Key words: Cell-to-cell variation, Parallel cells, Current imbalance, Battery pack, State of health, Electric vehicle

1 Introduction

The impact of parallel strings of battery cells on pack performance has been neglected for many years and only recently identified as one of the critical areas to be considered [1]. Due to the common voltage of the parallel cells, most studies assume that all parallel cells undergo similar currents. In reality the cell with the lowest capacity or highest resistance within the parallel connection will force the less aged cells (e.g. with lower resistance and higher capacities) to discharge at a much higher current and generate more heat [1]. Multiple factors can cause initial cell-to-cell variations within an energy storage system (ESS) comprising cells connected electrically in parallel. These can be identified as capacity and resistance differences due to manufacturing inconsistencies [2], [3], or parameters within the battery

system, such as variations in interconnection resistance and differences in the capability of the thermal management system [4], [5] leading to temperature gradients within the battery assembly. The initial parameter variations partly affect each other during system operation and even amplify the inhomogeneity at a system level. Such variations force the cells to draw different load currents and result in different states of charge (SoC) and temperature levels among individual cells. This, in turn, results in a further divergence in the electrical loading of each cell and is known to accelerate cell aging and system degradation and negatively affect the available power and energy within the ESS [6].

The manufacturing tolerance of cells is more significant for battery impedances rather than energy capacity [7], [8], [9]. The typical variation is cited to be approximately 25% [10] for internal impedance and 9% for capacity [11], [12]. According to Brand at al. [13] a resistance imbalance is more likely to cause noticeable inhomogeneous current distributions. A 20% difference in impedance of a module comprising two 32 Ah cells can lead to a 40% increase in parallel branch currents which can affect the reliability of the system [4]. Spurrett et al. [14], mentioned that a 10% energy capacity variation among the cells is not sufficient to impose significant imbalances. In another study, Brand et al. [13] connected two cells of the same type with identical internal resistances but with significant difference in capacities of around 30%. They observed that the currents divided equally at the beginning of the discharge, but later a variation of 32% was noticed towards the end of the discharge. The impact of the battery thermal management system and the thermal effect of the neighbouring cells is another issue, which has been ignored in many studies. Fleckenstein et al. [15] cooled three parallel cells differently to reach a temperature variation of 20K. Their results show that the current and SoC difference between the cells during cycling could reach up to 50% and 5.3% respectively. Fleckenstein et al. [15] reported that OCV variation as a result of high load currents might not equalise completely even after a long rest period. SoC inconsistency as well as voltage and resistance can further limit the power availability of a battery pack. The cell with the highest SoC will limit the peak power during charging and the one with the lowest SoC becomes the limiting factor during discharge [16].

Cell-to-cell variations may cause the load current for some cells within a battery pack exceeds their limits and as a result undergo accelerated aging [16]. When considering the degradation of battery packs comprised of parallel strings, a primary research question is whether the initial parameter dispersion of the cells reduces through long-term operation or does the differences between cells diverge further. The degradation process of the battery pack and that of individual cells are correlated, however it is said that the pack capacity degradation rate is generally higher than that of unique cells [17]. Wang at al. [17] tested 4 different battery packs for 100 cycles. They observed that within the first 30 cycles, the capacity degradation of the cells and that of packs were very similar and increased very slowly which was attributed to the initial consistency between the cells. By increasing the number of cycles the degradation rate significantly increased and the cell and the level of pack capacity degradation diverged considerably. Baumann et al. [4] analysed capacity and impedance variations within parallel battery strings with a 2p-6s configuration, both analytically and experimentally. They carried out the experiments on two batches of new and retied BEV battery packs including 1865 and prismatic formats with a capacity of 50 Ah. The nominal capacity and voltage of the pack was 100 Ah and 374 V respectively. The cells were characterised after every 100 cycles. They noticed that aged cells showed a stronger parameter dispersion compared to that of the new cells and the inhomogeneity increased during further aging. Gogoana et al. [10] identified that a 20% difference in internal resistance of the cells in parallel can result in approximately 40% reduction in the lifetime compared to cells with identical resistances. Pastor-Fernández et al [12] achieved different results. They tested four 3Ah parallel-connected cells for 500 charging and discharging cycles. They estimated the state of health (SoH) as either capacity fade (SoH_E) or impedance increase (SoH_P). The initial SoH_E of the cells were

different by up to 40% because of an 8% variation in capacity. Moreover, SoH_P of the cells varied by 45%, due to 30% dispersion in impedance. They observed that SoH_E and SoH_P converged to 10% and 30% respectively by the end of the experiment. From a review of the literature, it is clear that there is still a lack of experimental data on the long-term impact of such scenarios on SoH and pack performance, especially under aggressive drive cycles in which the battery system is cycled through the complete SoC range.

Attribute inconsistency between parallel cells is not typically monitored within the battery management systems (BMS), as the BMS does not have access to the properties of individual cells and the financial cost and resulting complexity of installing a current sensor within each parallel electrical path of the ESS would be prohibitive [6], [12]. Voltage is measured across the parallel connection. Temperature is often only measured at a module level or at strategic locations within the battery assembly. A typical BMS assumes that all the cells connected in parallel have the same SoH and state of charge (SoC) due to their common terminal voltage. This assumption may result in further degradation and over-charging/discharging hazards for individual cells [18], [19]. Therefore, it is of significant interest to understand the current distribution within a parallel string and the topics linked to it such as ESS aging and safety.

There are only a few studies that have examined different imbalanced scenarios, and developed battery pack models based on series-parallel configurations of battery cells, in which each cell is uniquely defined. The authors argue that the number of publications in this area compared to the importance of the topic is low. It is noteworthy that most of the studies tested or simulated packs comprised of 4-10 cells in parallel rather than those used in real world EV applications, in which the number of parallel connected cells may exceed 30 cells within a module, depending on the capacity of the cells. Many of these studies looked at one variable at a time, e.g., capacity, resistance, temperature variation and therefore do not achieve a holistic understanding of the problem. The contribution of this study is to extend the existing literature by modelling a highly parallelised module under real word conditions. This study is novel and addresses some of the most important scenarios which highly impact the overall performance of the system. It highlights the important factors for achieving an optimum design for an ESS, which in turn increase the energy utilisation efficiency, durability and safety of an energy storage system. This will potentially lead to a cost reduction and increase maturity of an ESS. Table 1 presents an overview of the previous studies dealing with parallel-connected cells and the methodology used along with the areas, which have been addressed through their research.

Table 1. An overview of the state of the art in parallel connected cells. R_{cell}, R_{IC}, C, I, T, N_{cell}, pack config, stand for cell resistance, interconnection resistance, capacity, current, temperature, number of cell and pack configuration respectively.

Ref	Exp	Model	Topology	R_{cell}	R_{IC}	C	I	T	SoC	N_{cell}	SoH	Aging	Pack config
[1]	x	x***	2p, 3p, 4p			x				x		x	x
[4]	x		2p 6s	x		x					x	x	
[5]	x	x****	12p 7s	x	x								
[13]	x		2p 1s	x		x	x						
[13]	x	x****	2p 1s			x	x						
[16]	x	x****	2p 1s									x	x
[19]			4p 1s	x	x	x						x	
[20]	x	x**	3p 3s 3s 3p	x	x		x			x	x	x	x

[17]	x	x****	2p 2s 2s 2p	x		x					x	x
[21]	x		3p 1s			x		x			x	
[22]		x*	2p 1s			x		x			x	
[23]	x	x**	2p 4s 4s 2p			x						x
[24]		x****	2p 1s	x		x				x		
[25]		x***	2p 4s		x							
[26]		x***	5p, 10 p		x				x			
[27]	x	x**	8p 1s 8s 1p			x						x
[28]		x***										
[29]	x	x**	2p 1s 3p 1s 2p 2s									
[30]			4p, 10p 4s, 10s	x	x	x						
[31]	x	x**				x	x	x			x	

Cell model: *Electrochemical, **1st order RC, ***2nd order RC, others****

Within this study, a comprehensive model of a battery pack has been developed comprising the electro-thermal coupling of individual cells so that the intrinsic factors affecting cell imbalance can be captured. The impact of cell-to-cell variations within a pack can be predicted, in addition to assessing different topologies of parallel-connected cells. To the author's best knowledge, no other study in the literature has addressed the impact of system configuration on the performance of an ESS so far. A holistic study is presented that addresses manufacturing inconsistencies between cells, thermal gradients within the system and different pack design options (e.g. configuration and interconnection resistance). The impact of each of these is elaborated and the safe operation zone for the module is clarified. In addition, the correlation between the design parameters and system imbalance has been quantified for the first time. Each cell contains a first order equivalentcircuit model (ECM), together with a thermal model operating in the Matlab/Simscape environment. Section 2 presents the structure of the mathematical model. Section 3 presents the model validation. Results and discussion can be found in Section 4, Further work and conclusion are presented in Section 5 and Section 6 respectively.

2 Model Development

2.1 Cell Model: ECM and Thermal Model Formulation

The ECM model is the most common approach for calculating the battery state parameters due to its simplicity, low computation time and accuracy in relation to SoC, voltage and temperature prediction [32]. An ECM model contains several elements, the open circuit voltage (V_{OCV}), internal resistance (R_0) and one or multiple resistor-capacitor (RC) pairs in series, depending on the required accuracy level. In the first RC pair, R_1 is commonly defined as the charge transfer resistance and C_1 represents double layer capacitance [33]. A first-order model formulation for each cell, comprising a single RC pair has been used to define each cell within the module. The schematic of the ECM model configuration is depicted in Figure 1.

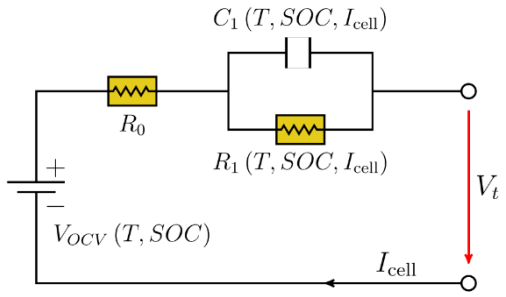


Figure 1. The configuration of a 1st order ECM model containing different elements.

R_0, R_1 and C_1 extracted from the experimental characterisation of the cell at different SoC and temperature levels are collated and implemented into the ECM model as lookup tables. Section 2.1.1 discusses further the model parameterisation process. Derivation of the model equations is defined in many publications and academic texts, for example [19], [34], so only a summary is provided here for completeness. The terminal voltage (V_t) can be calculated as the sum of the voltages over different elements, which includes open circuit voltage (V_{OCV}), voltage over the internal resistance (V_{ohm}) and the sum of the RC pair voltages (V_p) which stands for the polarisation loss as a result of electrochemical reactions [19]. V_{OCV} is derived from measurements and is a function of temperature and SoC. V_t and V_p can be calculated as follows:

$$V_t = V_{OCV} + V_{ohm} + V_p \tag{1}$$

$$\dot{V_p} = -\frac{V_p}{R_1.C_1} + \frac{I_{cell}}{C_1} \tag{2}$$

Battery state of charge (SoC) is governed by ordinary differential equations (ODEs) and is extracted by:

$$\dot{SOC} = \frac{I_{cell}}{36.C_n} \tag{3}$$

Where C_n is the nominal capacity of each cell and is known to be a function of temperature [35]. The model can be solved by writing the equations in state-space form as in the equation below, with SoC and V_p as the state variable and V_t as the response.

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \tag{4}$$

$$\begin{bmatrix} \dot{SOC} \\ \dot{V_p} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_1 C_1} \end{bmatrix} \begin{bmatrix} SOC \\ V_p \end{bmatrix} + \begin{bmatrix} \frac{1}{36C_n} \\ \frac{1}{C_1} \end{bmatrix} I_{cell} \tag{5}$$

$$[V_t] = \begin{bmatrix} \frac{V_{OCV}}{SOC} & 1 \end{bmatrix} \begin{bmatrix} SOC \\ V_p \end{bmatrix} + [R_0] I_{cell}$$

The thermal model is an essential subsystem of any battery model, because it has a significant impact on the internal resistance and other electrochemical parameters of the battery. The generated heat in the battery can be categorised as reversible ($Q_{rev}(W)$) and irreversible heat ($Q_{irrev}(W)$). For the latter, a is dissipated either through natural convection or active cooling [36].

$$Q_{tot} = Q_{rev} + Q_{irrev} + Q_{dis} = -I.T.\frac{\partial V_{OCV}}{\partial T} + R_0.I^2 + h.A.(T_c - T_{cell}) \tag{6}$$

The reversible heat is due to the entropy changes of the battery which are correlated to the U_{OCV} variation by temperature, and is a function of current (I) and cell temperature (T) [37]. The irreversible heat is referred as the generated heat due to the electrochemical reactions within the battery and is proportional to the battery internal resistance $R_0(\Omega)$ and squared current [38]. The dissipated heat ($Q_{dis}(W)$) is the transferred heat to the environment either through natural convention or an active cooling system. $h\ (W/(m^2.K))$ represents the heat transfer coefficient, $A(m^2)$ is the surface area of the cell, T_c stands for either ambient or coolant temperature and T_{cell} represents the surface temperature of the cell at the centre. The temperature of the battery is proportional to the net heat of the cell (Q_{tot}) and is calculated as:

$$Q_{tot} = m_{cell}.C_p.\frac{dT_{cell}}{dt} \tag{7}$$

Where m_{cell} is the mass of the cell (kg), C_p ($\frac{J}{kg.K}$) is the heat capacity of the cell and $\frac{dT}{dt}$ represents the variation of the volumetric temperature of the cell with respect to time. When the cell is under no-load, there is no source of heat generation inside the cell and $h.A.(T_c - T_{cell})$ in eq. 6 reduces to zero. Hence, the heat transfer coefficient can be calculated through equations (8-9).

$$-Ln\left[\frac{(T_{cell}(t)-T_{amb}}{T_0-T_{amb}}\right] = \frac{1}{\tau}t \tag{8}$$

Where T_0 is the cell temperature right after removing the load, T_{amb} is the ambient temperature, t is time and τ is introduced as the thermal constant:

$$\tau = \frac{m_{cell}}{h.A} \tag{9}$$

2.1.1 Model Parameters

The lithium-ion battery used in this study is a 5 Ah cylindrical cell, with an operating voltage of 2.5 – 4.2 V. The nominal resistance of the cell at 25℃ and 50% SoC is 19 – 19.5 mΩ. The normalised R_0, R_1 and C_1 quantified experimentally through standard Hybrid Pulse Power Characterisation (HPPC) tests are displayed in [19], [34]. The process of deriving ECM parameters HPPC experiments is well understood and defined in [19], [34], and will therefore not be repeated here.

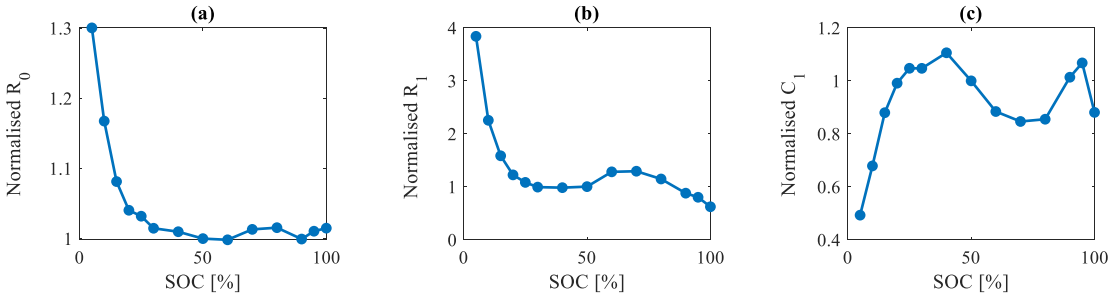


Figure 2. Normalised first order ECM model parameters, a) R_0, b) R_1 and c) C_1 for the 5 Ah cylindrical cell at 25℃.

The thermal properties of the cell are presented in Table 2.

Table 2. Thermal properties of the 5Ah cylindrical cell.

Parameter	Value

$m(kg).\ C_p(J/(kg.K))$	595
Heat transfer coefficient, h $(W/(m^2.K))$	30

2.2 Module Model Derivation

As discussed within [17], the performance of a single cell is not representative of that of the complete pack. Cells within a pack do not operate under similar environmental conditions and there is always deviations between the attributes of the cells in terms of energy capacity, resistance, current and SoC, which may result in different aging rates and performance capabilities. Accurate prediction of the battery current, power capability and battery SoC is key for validity of the model. Aggregating cell models in series and parallel to represent the battery pack model is not sufficiently accurate for modelling of the battery system. The capacity of the pack is usually overestimated through this method and its accuracy further reduces under more dynamic operational conditions [39]. In the current study, the battery pack model contains the model of the individual cell directly connected together in parallel so that the intrinsic cell imbalances are captured [40]. This method is the most promising system level simulation [41]. However due to complexity of the model it is computationally more intensive than the other approaches. The pack model has been developed within the Matlab/Simscape environment and it includes 15 cells in parallel (15p). The cells are connected together via an electric circuit model which is responsible for derivation of the current flows within the module and for representing the interconnection resistance between the cells. Two topologies of module have been derived; a Z and ladder configuration. The schematic of the electrical models are shown in Figure 3.

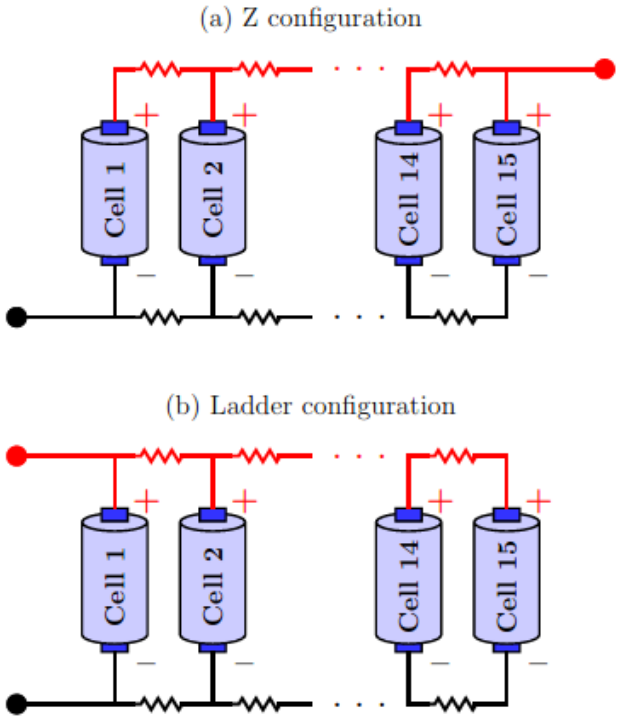
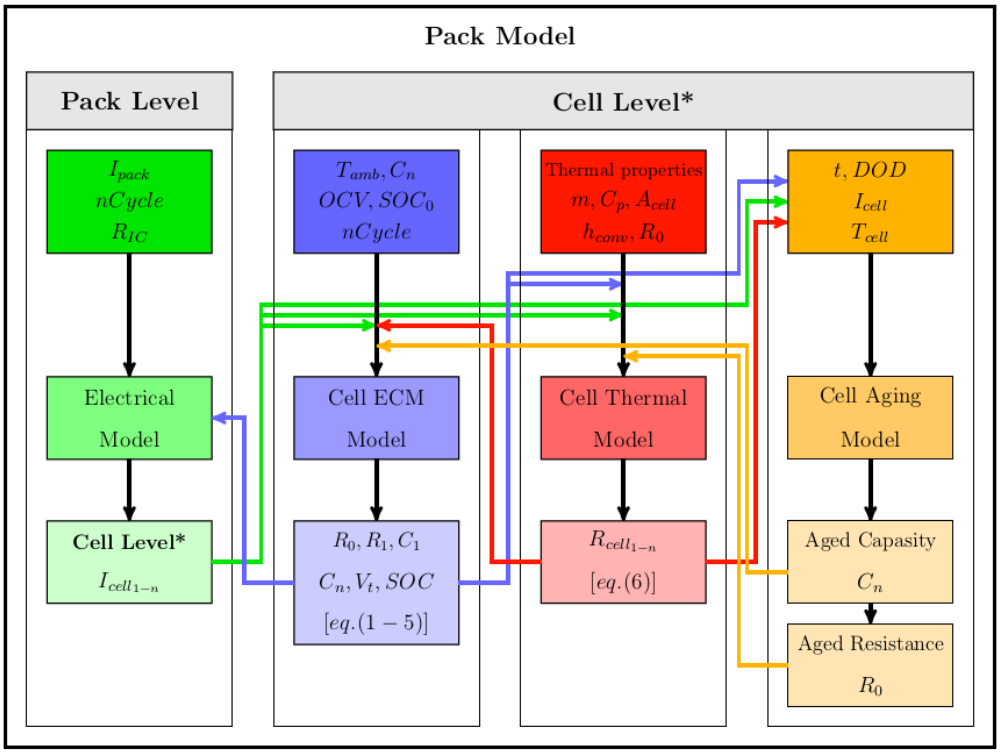


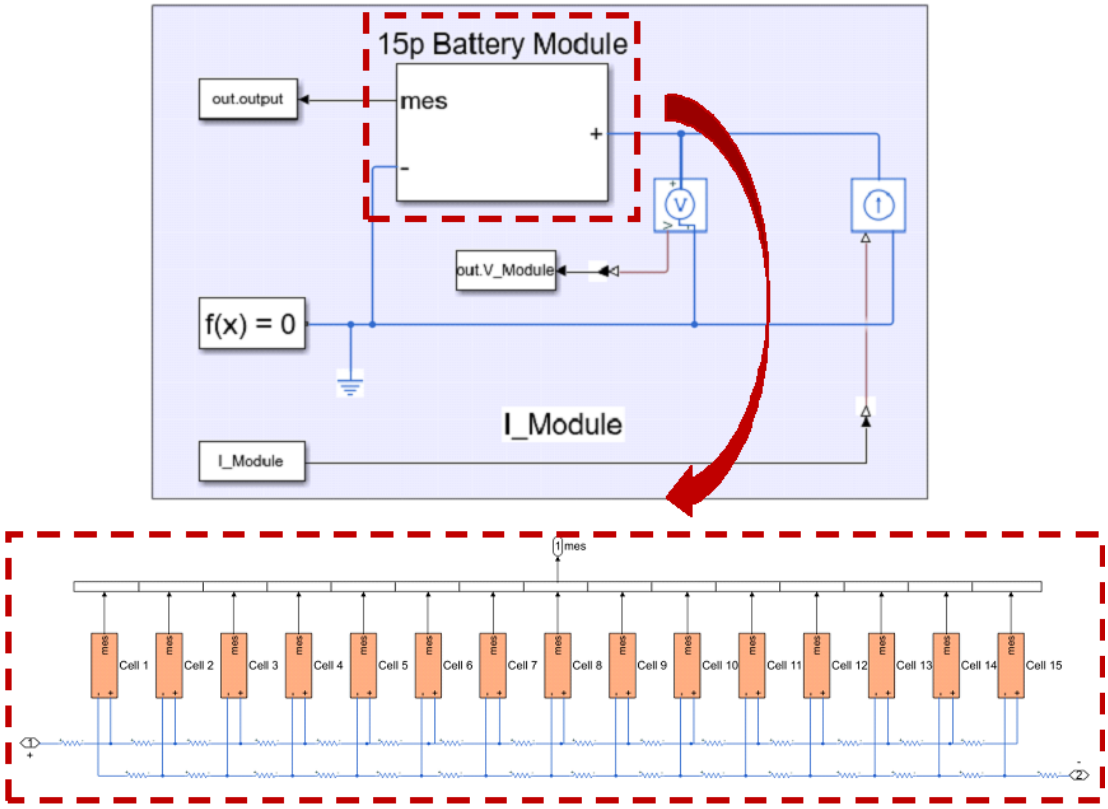
Figure 3. The electrical connection of the cells within the pack, a) baseline with Z shape, b) ladder configuration.

It is noteworthy that the model has been designed to be generic, and it can be applied for any number of cells as well as different cell configurations. The flowchart that defines the execution of the pack model, showing the different computational pathways along with the details of the developed model in Simscape are presented in Figure 4.

(a)


Pack Model
Pack Level
Cell Level*
I_{pack} $nCycle$ R_{IC}
T_{amb}, C_n OCV, SOC_0 $nCycle$
Thermal properties m, C_p, A_{cell} h_{conv}, R_0
t, DOD I_{cell} T_{cell}
Electrical Model
Cell ECM Model
Cell Thermal Model
Cell Aging Model
Cell Level* $I_{cell_{1-n}}$
R_0, R_1, C_1 C_n, V_t, SOC $[eq.(1-5)]$
$R_{cell_{1-n}}$ $[eq.(6)]$
Aged Capasity C_n
Aged Resistance R_0

(b)


15p Battery Module
out.output
mes
+
-
out.V_Module
f(x) = 0
I_Module
I_Module
1 mes
Cell 1
Cell 2
Cell 3
Cell 4
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Cell 10
Cell 11
Cell 12
Cell 13
Cell 14
Cell 15

(c)

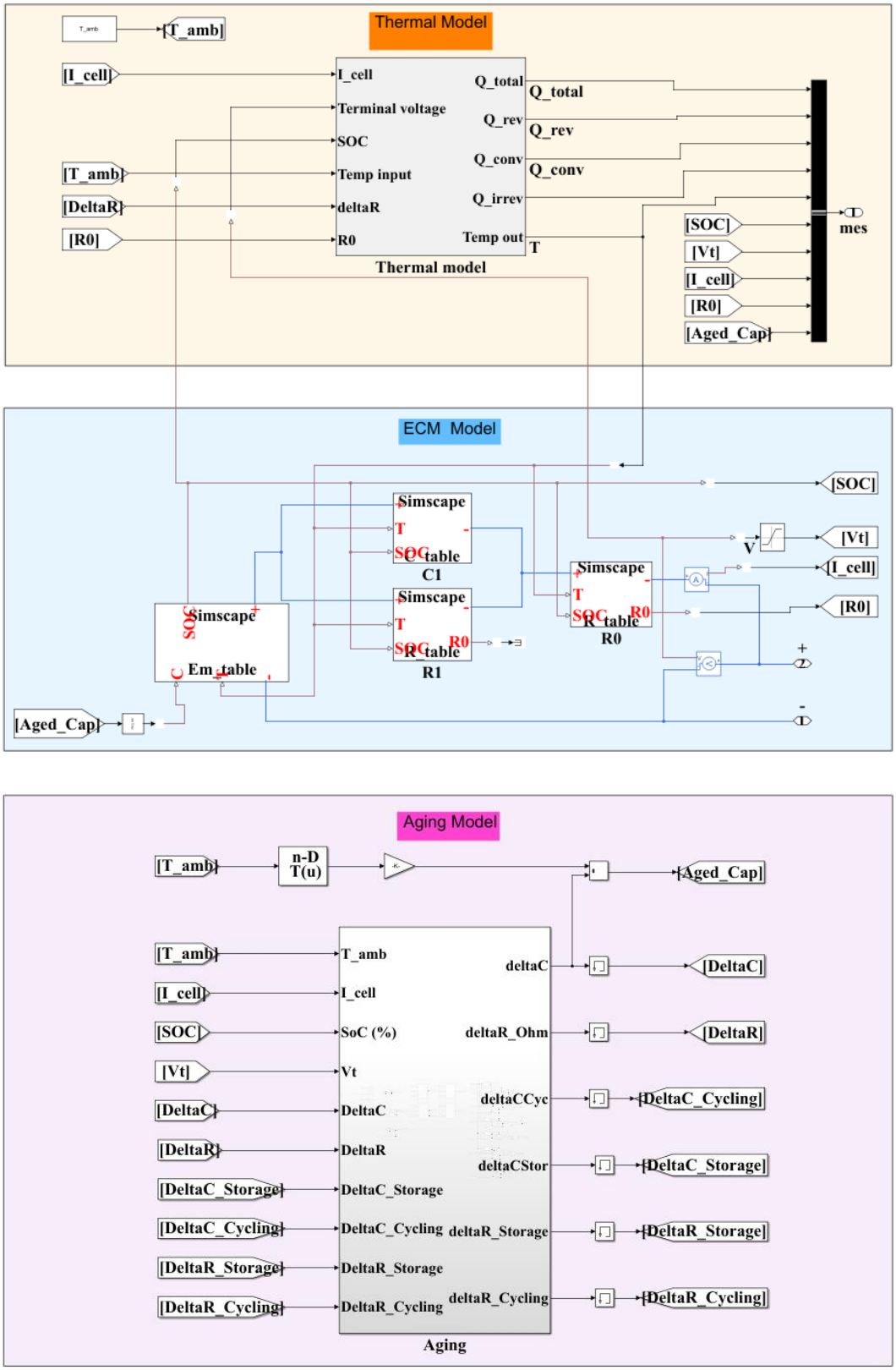


Figure 4. a) The flowchart of the pack model containing the electrical configuration of the pack as well as individual cell models, b) Battery pack model, c) The ECM, thermal and aging model of a single cell in Simscape environment.

The input to the battery pack model is the module current. Depending on the electrical pathway and initial conditions of the cell, the current is distributed between the cells as displayed in Figure 4b. Then the current of each cell goes through the ECM model of its own where its SoC, resistance and terminal voltage are being quantified, Figure 4c. These data are fed back into the thermal model to predict the total heat and surface temperature of the cell whilst the aging model quantifies the capacity fade and increased internal resistance of the cell. The resulting outputs of the thermal model are fed back again to the ECM model. During the simulation the pack model collects the updated resistance values of the individual cells and that is how the current is distributed dynamically within a module.

3 Model Validation

3.1.1 Single cell

The terminal voltage and surface temperature of the underpinning cell model has been validated versus experimental data corresponding to 25℃ ambient temperature, as shown in Figure 5. A good agreement is observed between the experimental and simulation results, with less than 0.1 V peak and 0.08 V RMS error respectively in voltage during cycling and less than 1℃ deviation in surface temperature. It is noteworthy that the temperature measurement corresponds to the surface temperature in the middle of the cell surface recorded by T type thermocouples.

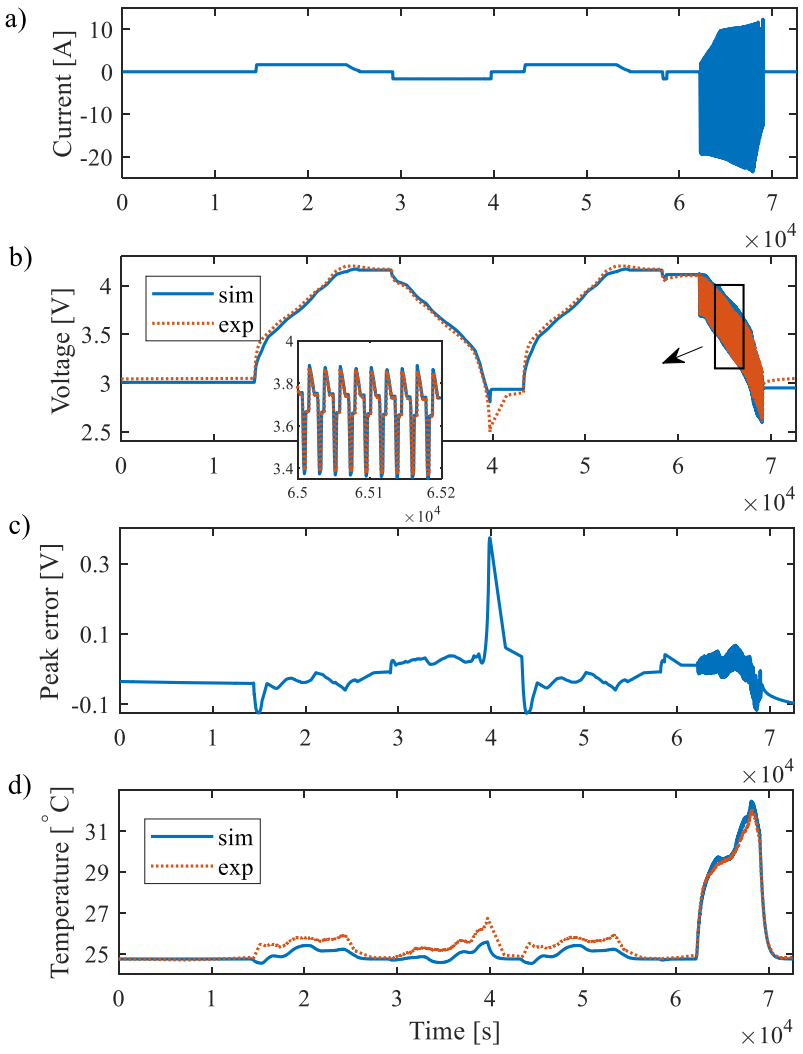


Figure 5. a) applied current, b) Comparison between the simulation and experimental data of the terminal voltage, c) modelling error for voltage ($V_{t,sim} - V_{t,exp}$), d) simulation results for the surface temperature of the cell versus experimental data, for the 5 Ah cylindrical cell at 25℃ ambient temperature.

3.1.2 Module level

The module level validation has been conducted versus previously published data for a 4p module with ladder configuration [19]. Within the [19], the cells were at different SoH conditions as they were aged by 0, 50, 100 and 150 cycles respectively. Hence, the initial capacity and resistance of the cells were different as reported in Table 3.

Table 3. Summary of initial capacity and resistance of the cells [19].

Cell	Aging cycles	1C discharge capacity (Ah)	Internal resistance (mΩ)
Nominal	-	5	19.3
1	0	4.79	18.6
2	50	4.66	20.5
3	100	4.51	23.3
4	150	4.31	25.3

For the experimental work, the wires from each cell were all connected to a common pair of terminals, so there was no unique connection between adjacent cells [19]. Therefore, the interconnection resistance was considered negligible. Using the aforementioned data, the new developed model in this study is validated as shown in Figure 6.

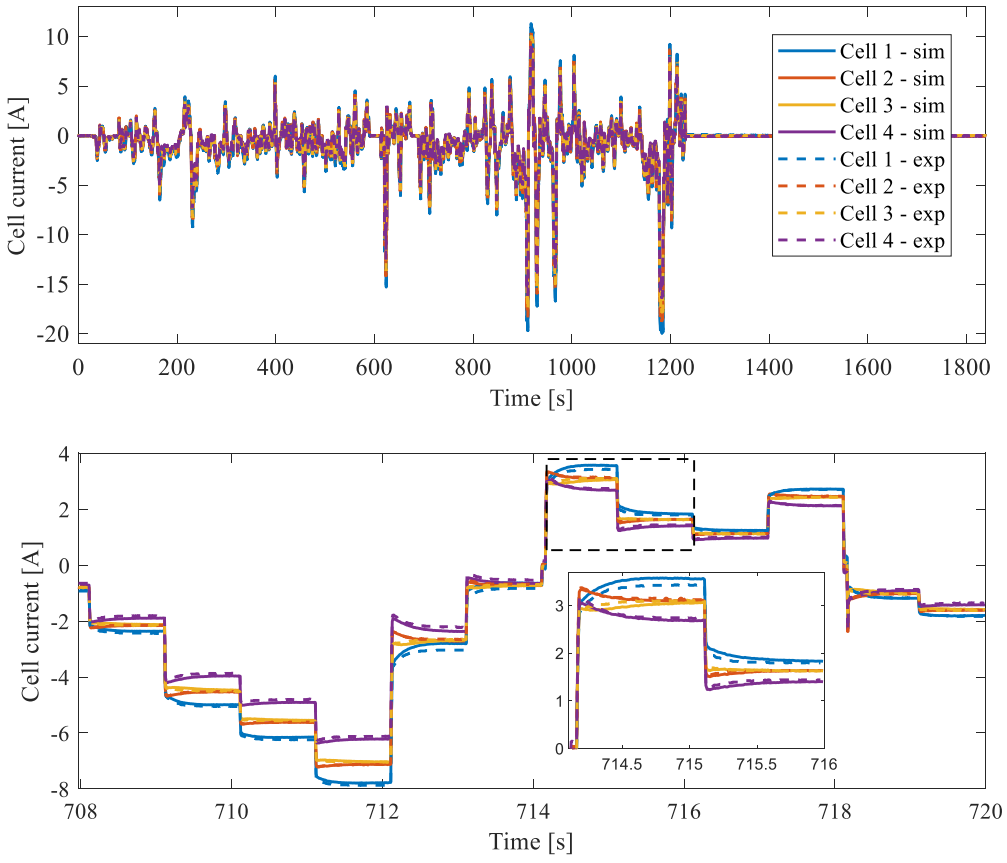


Figure 6. Validation of the module model versus previously published data [19], for a 4p module under a drive cycle with sample rate of 100 Hz and initial SoC of 70%.

The peak simulation error for current of the individual cells in respect to the experimental data is 0.35 A which corresponds well with those of Bruen et al. [19].

4 Results and Discussions

Different case studies are discussed. The main objective is to systematically define an operating window within which the pack is operating safely, moreover, where the unused energy and SoH spread within the pack in minimised. Pack safety is primarily affected by the maximum current and temperature. As the parameter spread within a pack increases, there is a higher chance that some of the individual cells operate under a higher current than the manufacturer's recommendation and will be over charged/discharged. In addition to the safety concern, this condition will limit the useful life of the pack [18], [19]. Hence, an in-depth understanding of the causality between parameter variations as a result cell connection arrangements, cooling design and manufacturing tolerances is vital for optimised system design.

4.1 Pack Configuration

It is well understood that battery pack performance is related to its configuration. However, there has been comparatively little discussion around a comparative analysis of different cell interconnection architectures [17]. In a study by Baronti at al. [42] it was highlighted that battery configurations with modules directly connected in parallel and then assembled in series are more robust against variations of cell capacity through the battery [42]. There are different ways of connecting batteries in parallel. Commonly employed topologies include the Z shape or ladder shape (Figure 3) configurations being the most common approach. This case study evaluates the performance of these two configurations for the same number of cells (e.g. 15p). As discussed within [6], [43], interconnection resistance between the cells can result in a current mismatch. If the sum of electrical interconnection resistances through the current path of each cell differs from one another, the cells will face different current flows [4]. According to [4] the interconnection resistance is typically in the range of $0.08\,m\Omega - 0.318\,m\Omega$ depending on the joining techniques employed. However, in case of a faulty contact, the interconnection resistance can increase significantly (e.g. of the order of $m\Omega$). In case of a faulty interconnection resistance or poor pack design, the cells may not be well balanced under load and over time, this may negatively influence pack performance [5], [6]. In this case study, there is interconnection resistance between each cell and for simplicity it was assumed that all the resistance values are the same. It is noteworthy that in an actual system R_{IC} is dependent on the busbar design and they can slightly vary at different locations of the pack. However as they are at the same order, considering identical values for R_{IC} is a valid assumption [12], [43].. The value varies from 1% to 10% of the nominal internal resistance of the cells, at 25℃ and 50% SoC, having a value of 19.3 mΩ. Hence, R_{IC} therefore varies between 0.193 mΩ and 1.93 mΩ.

The rest of the conditions such as initial capacity, resistance, SoC and thermal boundary conditions have defined to be the same for each cell. A two stage electrical loading profile for the cells is to be employed and contains:

1. Discharging the cells from 96% to 4% SoC (4.125 V – 2.93V), using a current profile derived from an electric vehicle (EV) model for the Artemis Rural Road drive cycle, with maximum charge and discharge rate of 1.8 C and 4 C respectively.
2. The battery will be allowed to equilibrate for one hour at the end of the current profile.

The drive cycle current profile is based on Tesla model S pack size and vehicle parameters [42], [45] in which the cells are substituted by 5 Ah cells.

4.1.1 *Z configuration*

Figure 7 presents the simulation results for the Z configuration of the module design. As it can be seen, $cell_1$ and $cell_{15}$ always receive the highest current, because of the lower resistance through the current path. Conversely, $cell_8$, the one in the middle experiences the lowest current. For $\frac{R_{IC}}{R_{cell}} = 1\%$ ($R_{IC} = 0.193\ m\Omega$), a maximum current variation of 8.6 A is observed when the peak module load current is 300 A, i.e. the average current of 20 A per cell. The normalised current imbalance of the module, θ is defined as:

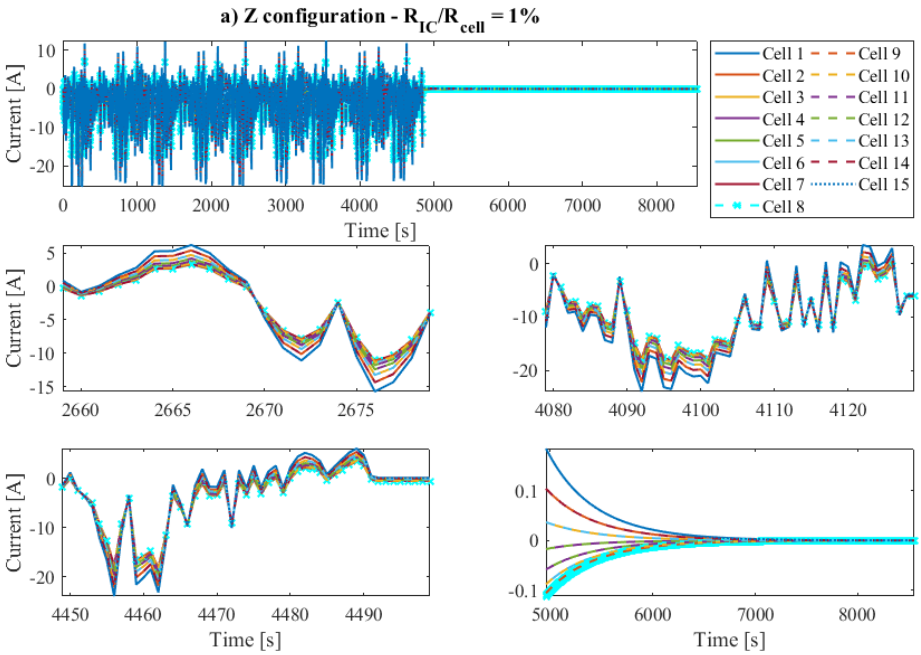
$$\theta = \frac{(I_{cell,max} - I_{cell,min})}{I_{ave}} \times 100 \quad (10)$$

$I_{cell,max}$, $I_{cell,min}$ are the maximum and minimum current of any cell within the module and I_{ave} defines the module current divided by the number of cells. Given $cell_8$ undergoes the lowest current, during the discharge cycle (Artemis Rural Road) it shows the highest SoC. When $cell_1$ is discharged to 4%, the SoC of $Cell_8$ is 5.1%. The SoC of other cells are within the range of 4% - 5.1% which represents a marginal variation of energy balance. However, when the load is removed the cells with a higher SoC charge the cells with a lower SoC. The internal current flow between the cells is within -0.49 A to 0.83 A, see Figure 7, where a negative value defined a cell being discharged. It takes circa 1158 s for the cells to self-balance subject to a final SoC variation of 0.1%.

The unused energy within the pack because the interconnection resistance, ϕ (%) can be calculated as:

$$\phi = \frac{\sum_{n=1}^{N_{cell}} (SoC_{celln} - SoC_{min})}{N_{cell}} \times 100 \quad (11)$$

SoC_{celln} is the SoC of the cells, SoC_{min} represents the lowest SoC within the module and N_{cell} stands for number of cells. For this use case scenario, ϕ is equal to 0.68% which is not deemed to be significant. The maximum temperature difference, ΔT during cycling reaches to 2.3℃. Even though ΔT is not significant, having a subset cells always operating at a higher current and temperature can result in different SoHs during long term operation of the pack [4], [10], [12], [16], [17].



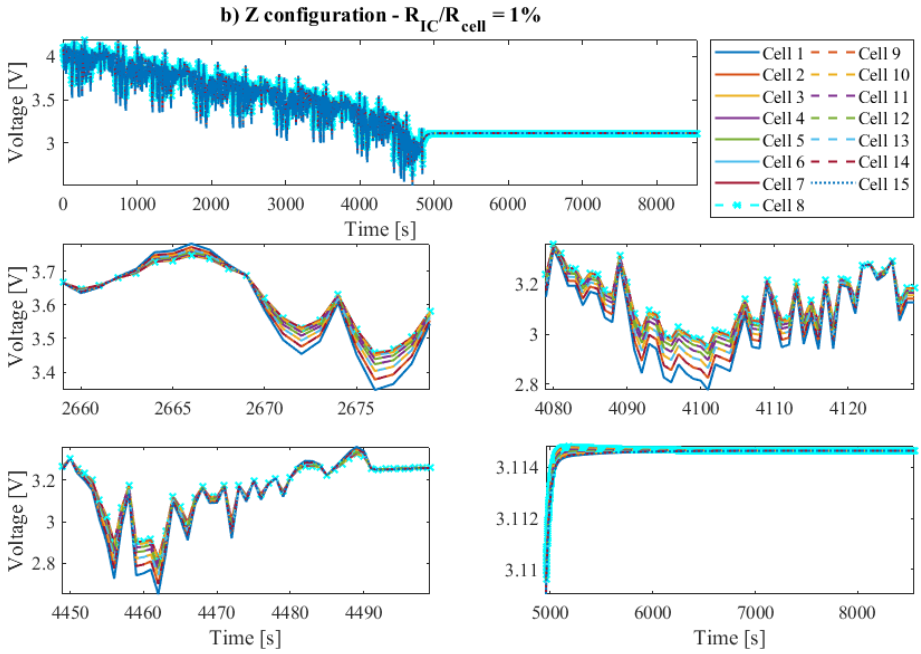


Figure 7. (a) The current imbalance, (b) the voltage variation within the 15p module as a result of interconnection resistance, $R_{IC} = 0.193\ m\Omega$, under Artemis Rural Road, from 96% to 4% SoC.

4.1.2 Ladder configuration

As discussed in Section 4.11, for the Z configuration, the first and the last cells experience the same R_{IC}, due to the symmetry of the design they undergo the highest current whilst the middle cell receives the lowest current. In a ladder configuration the cell closest to the terminal experiences a lower R_{IC} resulting in a higher load current and the furthest cell from the terminal undergoes the lowest current loading. The number of interconnection resistances through the path of current for cells with the highest and lowest currents, i.e. cell 1 and cell 8 in Z configuration are $2 \times R_{IC}$ and $16 \times R_{IC}$ respectively, whilst it is equal to $2 \times R_{IC}$ (for cell 1) and $30 \times R_{IC}$ (for cell 15) in ladder configuration. Consequently, in a ladder system the deviation of currents compared to the average current is much higher. Therefore, I_{max} in ladder is higher than that of Z, and in contrary I_{min} is less. These results are consistent with those published in [6], [46]. As R_{IC} increases the behaviour of the two systems differ more significantly. The summary of the results are presented in Table 4 for different magnitudes of cell interconnection resistance. The values in the columns have been colour-coded, with lightest purple showing the minimum and darkest purple showing the maximum value.

Table 4. A comparison between Z shape and ladder shape configuration for different interconnection resistances, under Artemis Rural Road drive cycle from 96% to 4% SoC.

R_{IC}/R_{cell} (%)	Config	ΔV (V)	I_{max} /I_{min}/ I_{ave} (A)	$I_{balancing}$ (A)	ΔT_{peak} (℃)	θ (%)	ϕ (%)
1	Z shape	0.18	25.4/16.8/20	-0.5 – 0.8	3	43	0.7
	Ladder	0.66	40.7/10.7/20	-2.4 – 4.6	9.8	149	3.5
5	Z shape	0.72	41.2/9.4/20	-3.2 – 5.4	10.3	159	4.3
	Ladder	1.56	86.8/2/20	-4.6 – 27.3	37.6	423	37
10	Z shape	1	54.7/5.2/20	-5.2 – 15.6	17	247	14.5
	Ladder	1.6	118.5/0.5/20	-5.3 – 32	65.4	589	58.6

The results show that for a ladder configuration the peak current is within 1.6 – 2.2 great than that of the Z configuration. Consequently, the variation in SoC and peak temperature is also significantly

higher. Another noticeable result is the higher peak voltage variations in a ladder configuration coming from the aggregated impact of interconnection resistances. The unused energy is represented by ϕ. As highlighted, even for low values of interconnection resistance, (e.g. 1% R_{IC}/R_{cell}), 3.5% of the module energy capacity is unusable for the ladder configuration, whilst in the Z configuration this value reduces to approximately 0.7%. For higher interconnection resistance values, the parameter variations especially current imbalance are deemed unacceptable. Therefore, for increasing safety, lifetime and reliability of the system the interconnection resistance should be minimised. Moreover, a highly parallelised ladder shape system should be avoided. Given the increased current and parameter dispersion within the pack it takes longer for the cells to balance after the electrical load is removed. The balancing time subject to final SoC variation of 0.1%, for Z config is within 1158 – 5536s. Conversely for the ladder configuration, the time required for self-balancing is within a range of 1829 – 12404s depending on the magnitude of the interconnection resistance relative to cell internal resistance.

4.1.3 Faulty resistance

A faulty resistance can occur due to a loose connection of a cell to a busbar or a defective weld. The impact of such a malfunction will be different and depends on the configuration of the pack and location of the fault. Within a Z configuration if the increased R_{IC} is toward the centre of the module, less cells will be affected. Conversely, the closer to the terminals a higher current dispersion is observed. In the case of a ladder configuration, the closer to the terminal the faulty joint occurs, a higher impact is observed. This can be seen in Figure 8. For clarity, only a subset of the figures are displayed. For all cases the R_{IC} is defined as 1% of the R_{cell} (e.g. 0.193 mΩ), with the exception of the faulty connection for which $\frac{R_{IC}}{R_{cell}} = 15\%$, (2.9 mΩ). Wherever there is an increased interconnection resistance, a shift in the voltage is observed in the graph. The same phenomenon is seen in the amplitude of the current and temperature profile of the cells. Some of the cells undergo a significantly higher current, which in turn leads to overcharging/discharging of the cells. For this specific cell, the recommended operating voltage is between 2.5 - 4.2 V. As seen in Figure 8, the voltage of a subset of the cells has exceeded the limit through over discharge which may causes safety concerns. This case study highlights that even one faulty connection can aggravate the performance of the whole system.

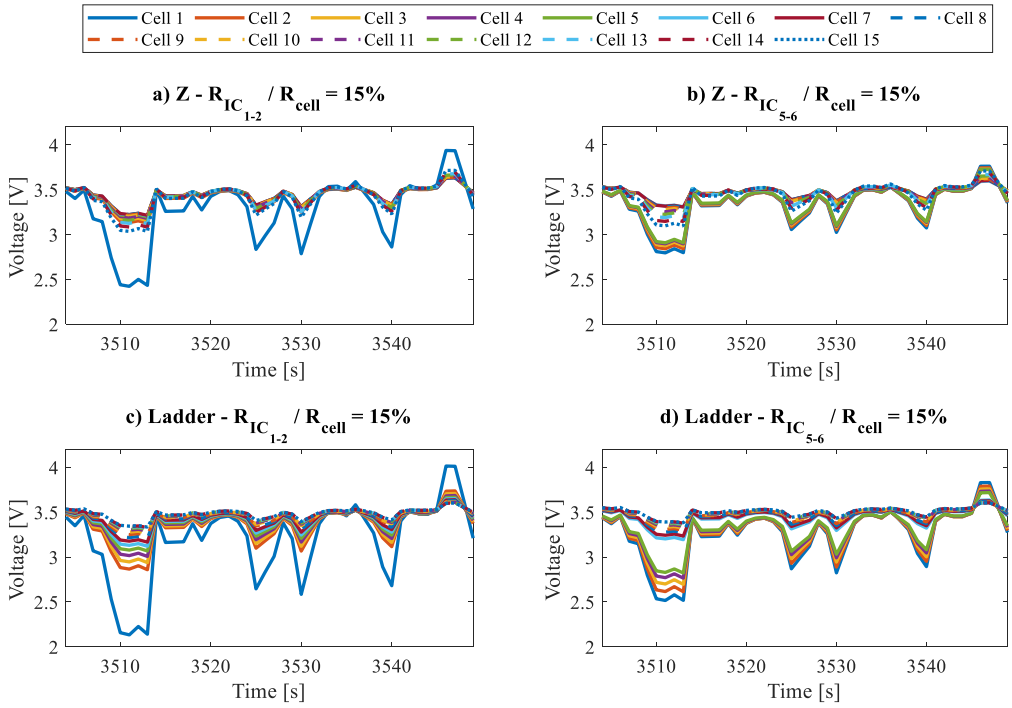


Figure 8. The voltage variation within a module due to an increased interconnection resistance. a) Z configuration, with faulty resistance between cell 1 and cell 2, b) Z with faulty resistance between cell 5 and cell 6, c) ladder configuration, with faulty resistance between cell 1 and cell 2, b) ladder with faulty resistance between cell 5 and cell 6.

4.2 Thermal Gradient within the Pack

One of the key elements and challenges in designing a battery pack is to maintain the battery cells within an optimum temperature range. This is to avoid the uneven degradation of the cells within a pack and to prolong the pack lifetime. Cell temperature has a direct impact on its impedance. The higher the temperature, the lower the impedance and vice versa [25], [26], [27]. A positive feedback coupling exists in which the branch with a lower resistance draws higher current than the others. The resistance mismatch results in uneven current distribution and the effect is amplified as the variations increase further. The cell with the lowest resistance ends up having the highest current which may be outside of its safety zone, also results in a higher degradation rate. Within the literature, a temperature variation of 5℃ between the cells in a pack is often defined as the optimum temperature [47], [48], [49].

4.2.1 Thermal gradient with no interconnection resistance

This case study quantifies the interdependency between the temperature difference of the cells and the resulting cell-to-cell variation in a 15p module. The thermal boundary conditions of the cells is controlled by the convective heat transfer coefficient (h). Cells1-12 have the same value of h = 30 $W/(m^2.K)$, while cells 13-15 are assumed to be insulated with a h value of 0. In reality, the temperature spread can occur due to either degradation of a thermal pad, loose connection between the cells and the cooling plate or improper design of the cooling system. By setting up the aforementioned boundary conditions a peak temperature gradient (dT ℃) of 29.4 ℃ is observed during the cycle. It is noteworthy that in this case study the interconnection resistance between the cells is assumed to be zero, ($R_{IC} = 0$) and the cells have similar capacity and resistance initially. Under these conditions cells1-12 operate similarly under a lower current and cells13-15 behave the same and undergo a higher load current due to a lower resistance [50]. The applied current is derived from an EV travelling over the Artemis Rural

Road drive cycle, where e cells operate between 96% to 4% SoC. For this scenario $I_{cell,max}$ is 23.8 A, $I_{cell,min}$ is 19 A, I_{ave} is 20 A, hence θ is equal to 24%. The current imbalance results in a SoC variation of 1.1% at the end of the discharge. Cell balancing lasts for approximately 814 s and the unused energy of the pack is equal to 0.86%. The correlation between the thermal spread and parameter inconsistency within the module under Artemis Rural Road from 96% to 4% SoC has been summarised in Table 5. ΔT is defined as the peak thermal gradient within the module.

The results show that the peak current and current variation increase by ΔT, however this is mostly the case at higher C-rate, e.g. 4C . If the C-rate is not sufficient, then only a modest current imbalance is driven by the thermal gradient. This has can be seen clearly in Figure 9. Moreover, the generic shape of the cell resistance versus SoC is another important factor to consider. For example, NMC (Nickle manganese cobalt oxide) cells may differ from LFPs (iron phosphate). Also going down to SoC < 20% may have a greater effect given the non-linearity of resistance within this region. Another interesting observation is the linear relationship of ΔT with $I_{cell,max}$, $I_{cell,min}$ and θ. It is noteworthy that in the absence of interconnection resistances, the parameter dispersion of the two configurations (Z and ladder) were similar.

Table 5. The impact of thermal gradient on dispersion of the module parameters in absence of R_{IC}. Cells 1-12 have h of 30 $W/(m^2.K)$, and cells 13-15 have a lower h value.

h (cells 13-15) $(W/(m^2.K))$	ΔT (°C)	R_{IC}/R_{cell}	$I_{cell,max}$ (A)	$I_{cell,min}$ (A)	I_{ave} (A)	θ (%)	ϕ (%)
10	5.6	0	21.2	19.7	20	7.3	0.5
5	11.3	0	22.1	19.5	20	13.1	0.6
0	29.4	0	23.8	19	20	24	0.86

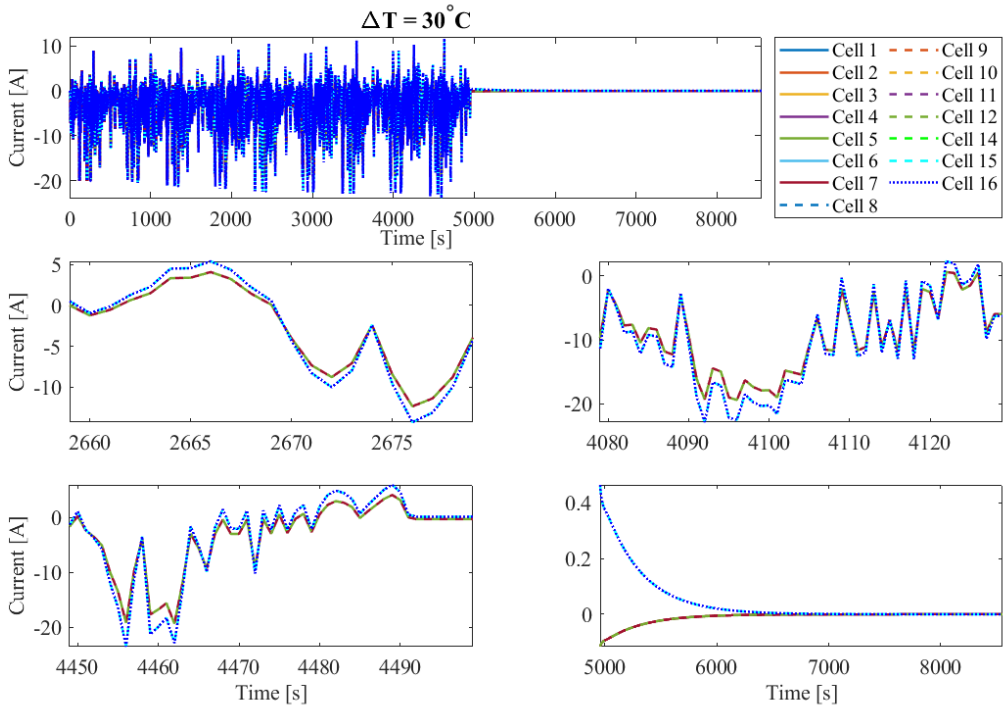


Figure 9. The current variation of the cells within the 15p module at 25°C ambient temperature.

4.2.2 Thermal Gradient combined with interconnection resistance

By combining the thermal gradient with interconnection resistance or any other parameters, the system inhomogeneity is either amplified or moderated. As seen in Table 6, for the ladder case under Artemis Rural Road from 96% to 4% SoC, the interconnection resistance makes the last cells undergo a lower current. The combination of the two factors make the system more uniform. It is noteworthy that the factors may interact with each other in opposite direction so that the inhomogeneity of the system can be aggravated.

Table 6. The impact of thermal gradient on dispersion of the module parameters with Z config, in presence of 1% R_{IC}/R_{cell}. Cells 1-12 have h of 30 $W/(m^2.K)$, and cells 13-15 are insulated.

h (cells 13-15) $(W/(m^2.K))$	ΔT (°C)	R_{IC}/R_{cell}	$I_{cell,max}$ (A)	$I_{cell,min}$ (A)	I_{ave} (A)	θ (%)	ϕ (%)
0	29.4	1	23.8	19	20	24	0.86
	40.7	1	29	16.4	20	63	1.6
	14	1	40.7	10.7	20	150	3.3

4.3 Manufacturing inconsistency

4.3.1 Capacity Variation

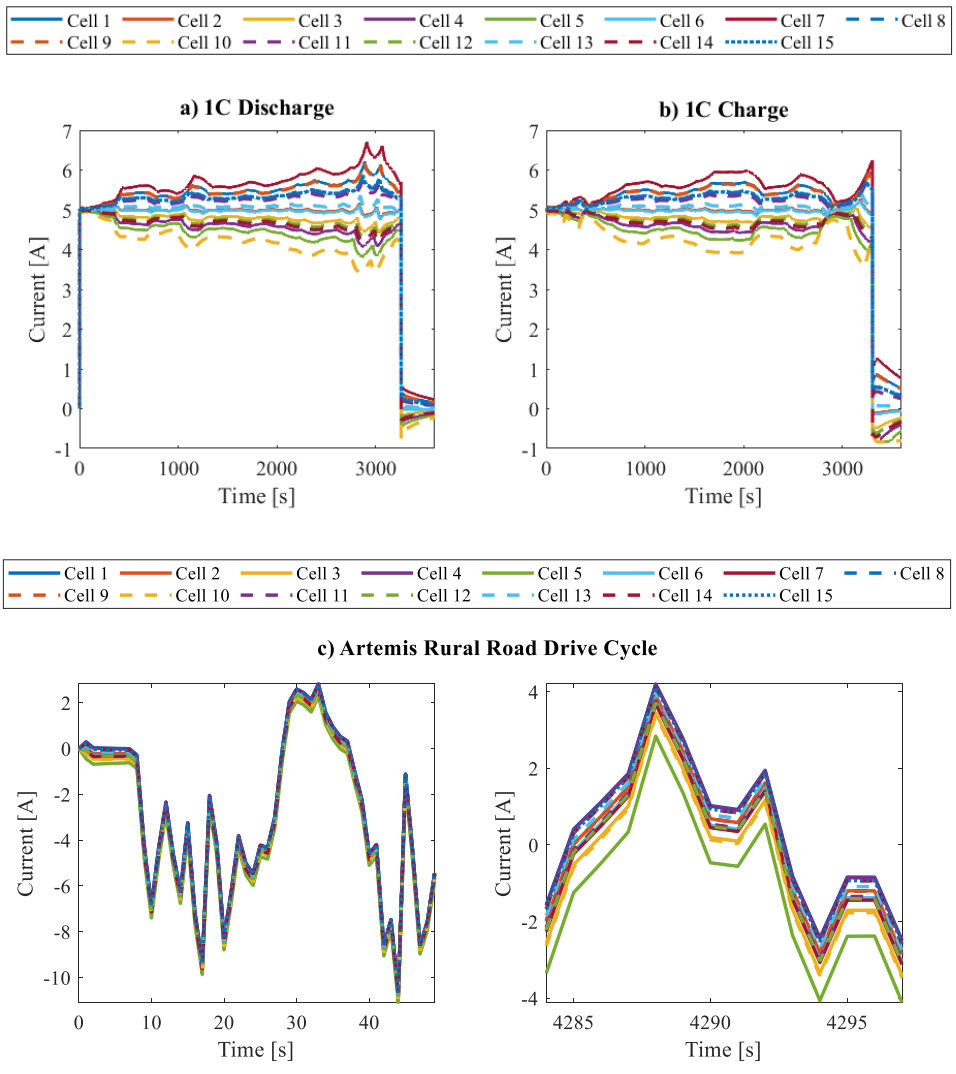
Energy capacity variation is another source of imbalanced behaviour within a parallel string. Cells can have different capacities due to manufacturing processes or it can happen over time, due to different operational conditions leading to variations in SoH. Over-charging or over-discharging of the cells, or being exposed to different environmental temperatures due to poor cooling design, may result in different capacity decay rates among the cells which lead to further imbalanced behaviour. Internal resistance and open circuit voltage (U_{OCV}) are both a function of SoC. When cells with identical internal resistances but different capacities are connected in parallel, normally they draw similar currents at the beginning. A simplified equation for current-voltage relationship of the individual cells is [12], [22]:

$$V_t = V_{OCV} \pm R_{cell}.I_{cell} \quad (12)$$

where V_t and U_{OCV} are terminal voltage and open circuit voltage respectively and R_{cell} represents the internal resistance of the cell and I_{cell} is the current magnitude. In the absence of interconnection resistance, the terminal voltage of each cell is the same. When we apply current at t = 0, the cells have the same SoC, consequently similar currents. For lower capacity cells, the SoC and V_{OCV} change faster, therefore even though they undergo the same current at the beginning, they will end up with different SoCs. In the case of discharge, at next time step, the lower capacity cell has a lower SoC, which results in lower V_{OCV}. In order to keep the same V_t between the cells, i.e. $V_{OCV} - R_{cell}.I_{cell}$, the cells with higher capacities should carry larger currents to compensate for the U_{OCV} variation. In case of charging, cells that have smaller capacities will end up a higher V_{OCV}, hence, undergo a lower current ($V_{OCV} + R_{cell}.I_{cell}$), to balance the SoC and U_{OCV} difference. It is noteworthy that this discussion is valid under the assumption that the resistance of the cells does not change significantly with SoC. From Figure 2(a), this implies that if the initial SoC is below 80%, the resistance variation may outweigh the V_{OCV} effect. The same point is valid for the magnitude of interconnection resistance, due to its significant influence on inhomogeneity of a pack.

A 9% variation in capacities is defined as the typical manufacturing inconsistency [11], [12]. Therefore, in this case study the initial capacities of the cells vary randomly by 9%, with $cell_7$ having the highest and $cell_{10}$ having the lowest capacity whilst the rest of the conditions remains constant. Different load currents were applied to the module, including constant 1C charge and discharge, Artemis drive cycle and a current pulse. The results show that the inhomogeneity of the system because of 9% capacity

variation is not significant, with maximum current variation of 4.3%. By increasing the capacity variation from 9% to 40%, the impact is more evident but still not significant. As shown in Figure 10, for constant 1C charge and discharge $cell_7$ undergoes the highest current and $cell_{10}$ draws the lowest current, as expected. When applying a drive cycle, the results are slightly different. A subset of the results for the Artemis drive cycle is observed in Figure 10c. As seen $cell_7$ carries the largest current during discharge pulses but the lowest during charge. The reason is that when shifting from discharge to charge very fast there is not enough time for relaxation of the cells, hence, the cells conditions will be different. However, if applying a current pulse with 20s rest between charge and discharge, the results are more similar to continuous charge/discharge condition. As seen in Figure 10d, the cell with the largest capacity ($cell_7$), carries the largest current during discharge pulse. But when applying the charge pulse it takes some time before $cell_7$ undergoes the highest current. It means that in terms of aging, when applying a drive cycle, the capacity variation will be less of an issue than applying a constant charge/discharge cycle. Because the highest current drawn by $cell_7$ at discharge pulses will be compensated for during charge. It is noteworthy that this discussion is only valid when there is no interconnection resistance or any other variation source within the module. Figure 10e shows a similar case, pulse current in the presence of 1% interconnection resistance. As seen, the impact of 40% capacity variation is outweighed by the 1% variation in interconnection resistance. Because in Z configuration, the cells in the middle expects the lowest current, $cell_7$ draws the lowest current after $cell_8$.



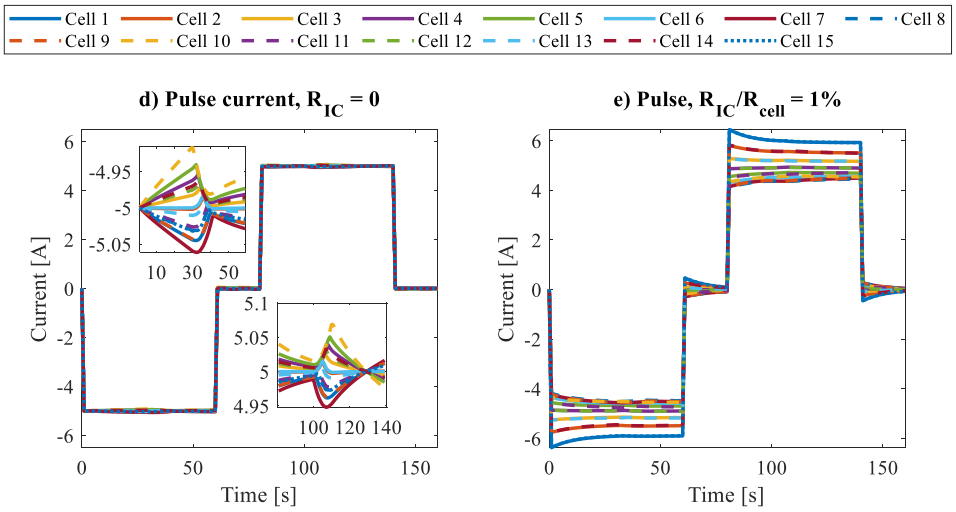


Figure 10. The impact of 40% capacity variation on the 15p module (Z configuration), with $cell_7$ having the highest and $cell1_{10}$ having the lowest capacity, under a) constant 1C discharge from 96%-4% SoC, b) constant 1C charge from 4%-96% SoC, c) Artemis drive cycle from 96%-4% SoC, d) pulse current, e) pulse current in presence of $\frac{R_{IC}}{R_{cell}} = 1\%$. The ambient temperature is 25℃ for all the test cases.

4.3.2 Resistance Variation

Basic electrical theory shows that a parallel connection of two resistances, the current through each branch is quantified by: $I_1 = R_2/R_1.I_2$ [4]. This means that the branch with a lower resistance draws a higher current value. This argument can be extended to a larger number of cells in parallel. Resistance mismatch results in uneven current distribution and the effect is amplified as the variations increase. The cell with the lowest resistance will experience the highest current, which may be outside of the manufacturer's specification for the cell. In this study, the resistance of each cell varies by 25% [11], [12], to account for the potential manufacturing inconsistency. $Cell_{15}$ has the highest and $cell_6$ has the lowest resistance. The results show that for a constant 1C charge and discharge the current flows for each cells diverge initially, as expected from eq. 12. As the charge or discharge proceeds the cells start to balance under load. When a cell reaches toward the end of charge or discharge, the resistance of the cell increases significantly (as shown in Figure 2), hence a turning point in currents is observed. It is noteworthy that resistance curve versus SoC is chemistry dependent and this behaviour may vary from one cell type to another. The variations in current peaks, are most likely caused by the profile of the internal resistance curve of the cells as a function of SoC. The peak current variation during charge is 30%, slightly higher than that of the discharge defined as 23.4%.When applying the Artemis Rural Road drive cycle, $Cell_{15}$ always receives the highest current for both charge and discharge and the peak current variation reaches to 21.8%. Figure 11(d,e), compares the cells response to a 1C charge and discharge pulse with interconnection resistance of 1% R_{cell} and without it. The peak current variation for case (d) is 25.6% which is raised to 44% due to the added impact of interconnection resistance, case (e). The summary of the results in terms of capacity and resistance inconsistencies and their impact on the system performance are summarised in Table 7 and Table 8 respectively.

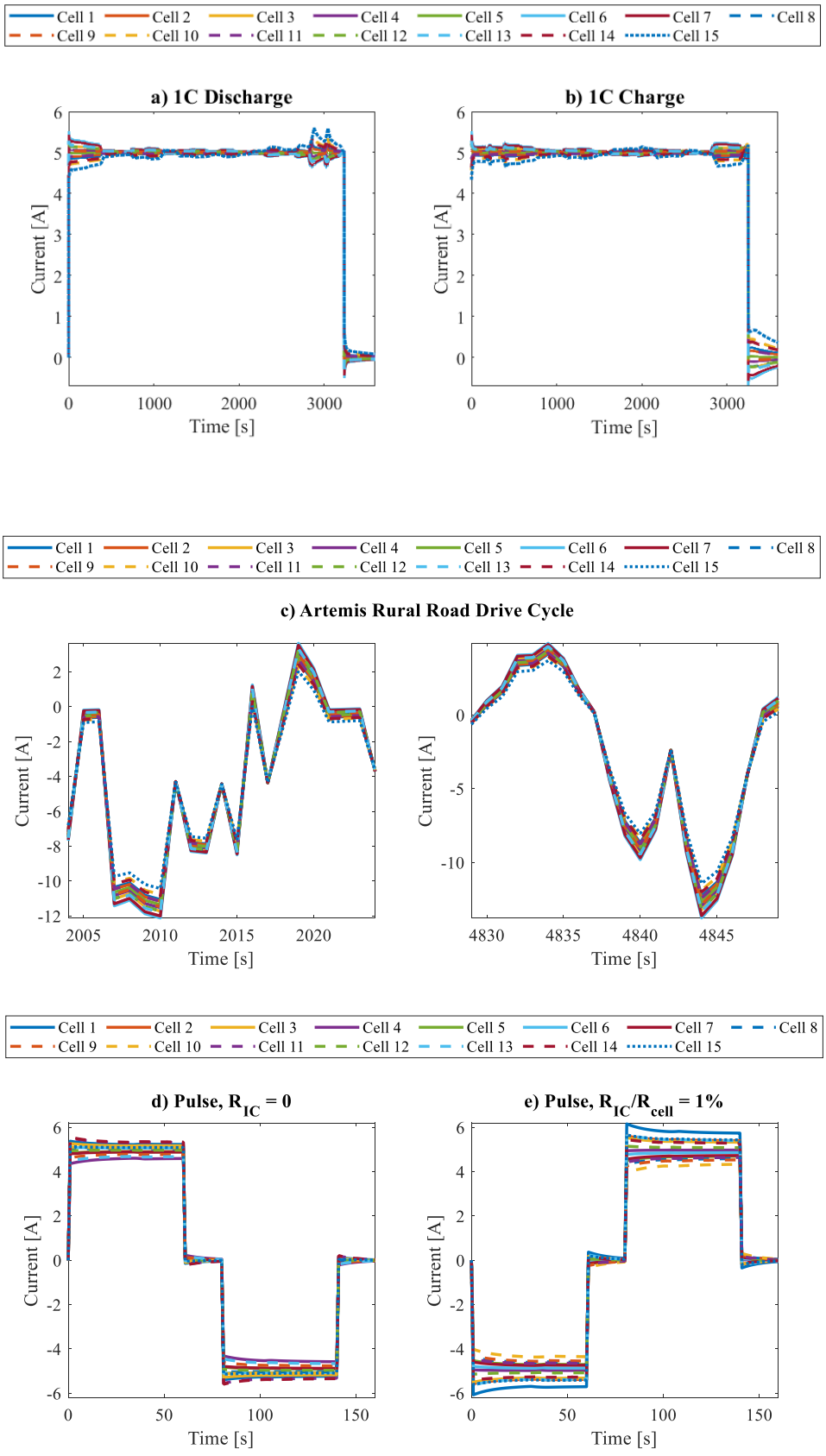


Figure 11. The current response of the individual cells in the 15p module (Z configuration) as a result of 25% internal resistance variation to a) 1C discharge, b)1C charge, c) Artemis Rural Road drive cycle, d) Pulse current,

e) pulse current in presence of interconnection resistance of $\frac{R_{IC}}{R_{cell}} = 1\%$. The initial SoC for charge and discharge is 4% and 96% respectively, moreover, the ambient temperature is 25℃ for all the case studies.

Table 7. Parameters dispersion within a 15p module (Z configuration) as a result of manufacturing inconsistency

ΔC (%)	ΔR_{cell} (%)	R_{IC}/R_{cell} (%)	$I_{cell,max}$ (A)	$I_{cell,min}$ (A)	I_{ave} (A)	θ (%)	ΔT (℃)	ϕ (%)
9	0	0	20.4	19.6	20	4.3	0.3	0.2
40	0	0	21.9	19.2	20	13.3	1.1	1
0	25	0	22.6	17.8	20	24.2	0.3	0.3
0	40	0	30.9	13.3	20	88	0.6	0.8

Table 8. Parameters dispersion within a 15p module (Z configuration) as a result of manufacturing inconsistency together with 1%R_{IC}/R_{cell}

ΔC (%)	ΔR_{cell} (%)	R_{IC}/R_{cell} (%)	$I_{cell,max}$ (A)	$I_{cell,min}$ (A)	I_{ave} (A)	θ (%)	ΔT (℃)	ϕ (%)
9	0	1	25.4	16.9	20	42.5	2.3	0.6
40	0	1	25.4	16.9	20	42.5	2.6	1.1
0	25	1	24.2	16.2	20	40	2.2	0.5
0	40	1	23.7	15.7	20	40	2.2	0.6
9	25	1	24.5	16.6	20	40	2.3	0.5

4.4 Impact of System Design Options

By comparing the results of all the different case studies presented based on their relative impact of current inhomogeneity (θ), it was found that R_{IC}/R_{cell} has the highest impact on the inhomogeneity of a system and the impact of the other parameters can be ranked as below and in Figure 12.

$$R_{IC}/R_{cell} > \Delta R_{cell} > \Delta T > \Delta C$$

It is noteworthy that the base case scenario attributes to a 15p module with Z configuration with no interconnection resistance. Moreover, the initial capacity, resistance and temperature of the cells are considered the same. Hence, there is no variation between the cells in base case scenario. For other case studies only one parameter at the time is varied whilst the others keeps constant. For purpose of this study, the module operates under Artemis Rural Road drive cycle at 25℃ ambient temperature.

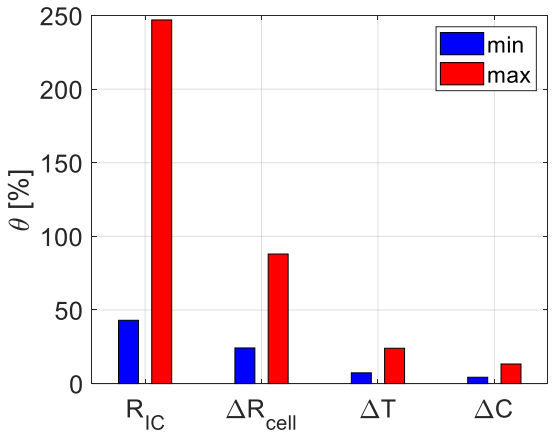


Figure 12. Impact of different parameters on inhomogeneity of the 15p module with Z configuration operating within a defined range of, $\frac{R_{IC}}{R_{cell}} = 1 - 10\%$, $\Delta R_{cell} = 25 - 40\%$, $\Delta T = 5 - 30℃$, $\Delta C = 9 - 40\%$, under Artemis drive cycle at 25℃ ambient temperature.

Figure 13 demonstrates the current imbalance of a system under constant discharge currents of 1C – 3C, as a function of the number of cells within the parallel connection and interconnection resistance for both Z and ladder configurations. The results highlight that there is not a strong correlation between θ and C-rate. Conversely, θ increases considerably as the number of cells varies. Further, current imbalance is significantly higher for ladder and θ is very much dependent on the pack configuration rather than total current. However, it should be noted that despite similar θ value, at different currents, high currents can be much more problematic in terms of pack degradation and safety [51]. For example in the case of ladder configuration with 15 cells and 10% R_{IC}/R_{cell}, the maximum temperature can reach 40 ℃ at the end of discharge when operating under 1C, whilst it is circa 140 ℃ under 3C, which is leading to a potential thermal runaway event. As known at very high temperatures circa 90 ℃, the battery SEI layer starts decomposing and it is normally accompanied by gas and heat release. As the temperature reaches to around 110 ℃, an exothermic reaction starts inside the battery and the rate of temperature increase becomes more violent [52], [53], [54].

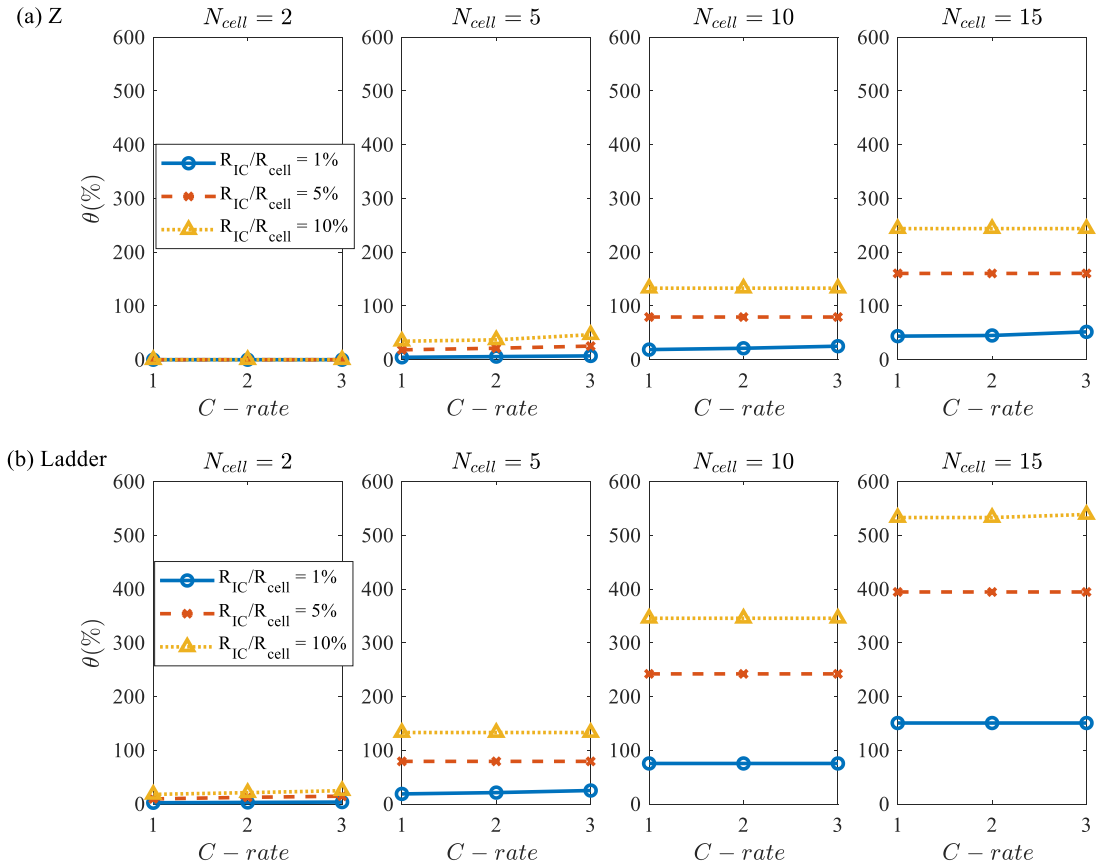


Figure 13. The interdependency between C-rate, length of a parallel string and number of cells on inhomogeneity of the a system for, (a) Z configuration, (b) Ladder configuration.

The correlation between θ and different design parameters (e.g. number of cells in parallel, N_{cell} and interconnection resistance) is quantified through a Multiple regression model in Minitab 19, and presented in eq. 13 and eq. 14 for Z and ladder configurations respectively. The regression model fits

the data very well with R-squared value of 99.7% for θ_Z and 99.05% for θ_{ladder}. The derived equations can be used as guideline for the initial design of a pack topology; knowing the limitations for each cell and the busbar design.

$$\theta_Z(\%) = 6.70 - 0.469\left(\frac{R_{IC}}{R_{cell}}\right) - 4.994N_{cell} - 0.3022\left(\frac{R_{IC}}{R_{cell}}\right)^2 + 0.5115(N_{cell})^2 + 1.5870\left(\frac{R_{IC}}{R_{cell}}\right).N_{cell} \quad (13)$$

$$\theta_{ladder}(\%) = -25.02 + 11.53\left(\frac{R_{IC}}{R_{cell}}\right) + 1.82\,N_{cell} - 1.5768\left(\frac{R_{IC}}{R_{cell}}\right)^2 + 0.387(N_{cell})^2 + 3.449\left(\frac{R_{IC}}{R_{cell}}\right).N_{cell} \quad (14)$$

The operation zones of a parallel string based on design parameters is depicted in Figure 14, where clear regions are defined for (1) ideal operation, (2) increased levels of aging due to the formation of temperature gradients between cells and differential current flow and finally (3) areas of potential safety concern due to individual cells being over charged or discharged. Figure 14, quantifies the potential benefit of the Z-module confirmation vs the alternative ladder cell architecture.

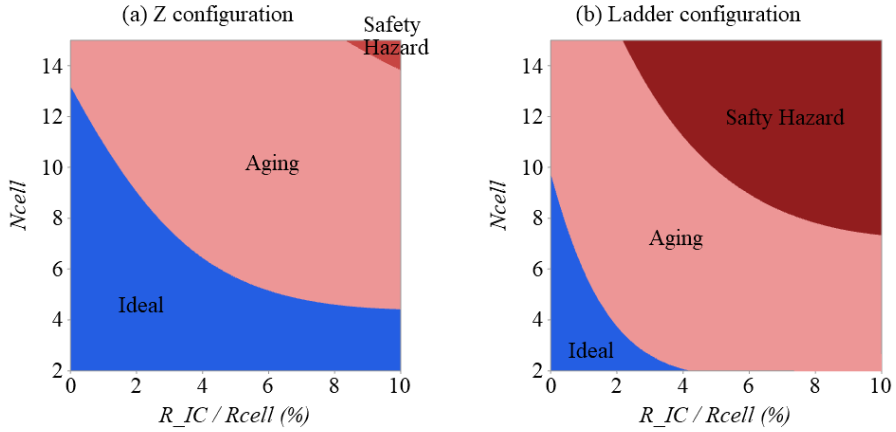


Figure 14. Operational zones as a result of system design for (a) Z configuration and (b) Ladder configuration.

5 Further Work

This work has focused on the short-term impact of cell-to-cell variations and differences in design parameters on the performance of an energy storage system. Further work for this research includes the full validation of the module level simulation for the different uses cases presented. This includes the variations in performance observed and those factors deemed critical for the safe operation of the battery system. The transferability of these design guides, e.g. within Figure 14, should be validated for different cell chemistries that exhibit different OCV and internal resistance profiles relative to SoC and ambient temperature. Moreover, a long-term aging study is required for different module architectures and cells operating within the aging zone defined in Figure 14 to quantify the magnitude and rate of differential aging that may occur between large parallel cell connections to better understand the levels of usable energy and expected life. Finally, it would be interesting to work through designing a balancing strategy in order to eliminate the inconsistency within the system and to maximise its lifetime.

6 Conclusion

Cell-to-cell variations within a parallel module originate from manufacturing inconsistencies or poor pack/thermal management design. Within this study the impact of pack configuration, cell number, interconnection resistance, thermal gradient, cell resistance and energy capacity variations on the level of parameter dispersion were investigated. The pack model comprises individual validated electro-

thermal cell model. The results for a 1s-15p module design highlighted that among all the different factors; the ratio of interconnection resistance to cell resistance has the greatest impact on system performance and potential safety.

Modules with a ladder configuration tend to display a stronger relationship with interconnection resistance due to the aggregated effect of R_{IC} for those cells further from the battery terminals. Conversely, the symmetry in a Z configuration moderates the amplified impact of R_{IC} within a parallel system. In a ladder configuration the cell closest to the terminal ($cell_1$), and the one furthest from the terminal ($cell_{15}$) draw the highest and lowest current respectively. For the Z configuration, the cells closest to both terminals ($cell_1$ ad $cell_{15}$) receive the highest current and the one in the middle ($cell_8$) undergoes the lowest current. Results show that a high interconnection resistance can be recognised from the difference in voltage responses of the cells. Individual voltage responses may therefore be used as a diagnostic tool within the control system to identify and predict the onset of a faulty cell connection.

Results show that temperature gradients do not have a strong impact on the behaviour of a system in the short term. The current inhomogeneity has a linear relationship with ΔT, and increases from 7.3% to 24% as ΔT changes from 5℃ to 30℃. It is noteworthy that only at peak loads the thermal gradient imposes a current variation. The results show that the inhomogeneity on the system as a result of a 9% capacity variation is also not significant, with a maximum current variation of 4.3%. By increasing the capacity variation from 9% to 40%, the impact is more evident but is still not significant. Resistance variation of 25% leads to 21.8% peak current variation within the system and it can boost up to 88% as the resistance dispersion reaches to 40%.

Combining these factors together can amplify the inhomogeneity within the battery system. Within the context of EV operation, the most notable outcome is a reduction in usable energy capacity that will manifest itself as a reduction in range. Increased levels of differential ageing and degradation may be observed when cells are operated for extended periods. Most significant is that for some variations of battery design parameters, safety concerns may be realised due to excessive charge or discharge, none of which would be detectable by the BMS because of its inability to monitor individual cell current and voltages.

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