Development of generic testing strategies for mixed-signal integrated circuits

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Abstract: The paper describes work at the Polytechnic of Huddersfield on SERC/DTI research project IED 2/1/2121 conducted in collaboration with GEC-Plessey Semiconductors, Wolfson Microelectronics, and UMIST. The aim of the work is to develop generic testing strategies for mixed-signal (mixed analogue and digital) integrated circuits. The paper proposes a test structure for mixed-signal ICs, and details the development of a test technique and fault model for the analogue circuit cells encountered in these devices. Results obtained during the evaluation of this technique in simulation are presented, and the ECAD facilities that have contributed to this and other such projects are described.

1 Introduction

The present (1991) ability of semiconductor manufacturers to reliably produce digital application specific integrated circuits (ASICs) containing in excess of 1 000 000 transistors has created major difficulties in IC testability. Successive increases in device complexity have not been matched by corresponding increases in the number of external circuit nodes (device pins), and consequently, in more complex devices, a high proportion of circuit nodes are now 'buried' within the structure of the IC, and are thus rendered inaccessible to a test system.

Testing strategies for complex digital ICs have therefore become dependent on 'structured' generic test schemes that rely on incorporating dedicated test circuitry as part of an IC design in order to provide test access to these buried nodes. Examples of these strategies include built-in-self-test (BIST), and various forms of scan-path analysis.

Analogue ICs are at present much less complex than many digital devices, but analogue testing strategies are also less advanced than those currently employed in digital systems [1]. Noise, nonlinearity, component tolerance effects, and the absence of general fault models for analogue systems have each inhibited the development of analogue testing strategies, and at present no general theory of analogue testability has emerged. Most analogue test schemes therefore rely on various forms of complex functional testing, which are generally inefficient and whose fault coverage is uncertain.

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Mixed-signal ICs, which incorporate both analogue and digital circuitry, are at present attracting a great deal of attention and are rapidly increasing in complexity. These devices offer significant advantages in economy and reliability when compared with assemblies of conventional analogue and digital ICs, and enable complex systems to be fabricated as single devices (e.g. application specific ICs). Mixed-signal ICs, however, present a major disadvantage, in that they are difficult to test using the conventional techniques currently applied to single-mode devices.

It is our view that structured techniques for fault detection in digital circuits are sufficiently well established, and that the major difficulty in current mixed-signal IC test, concerns adequate fault coverage of the analogue cells embedded within these devices. This testability 'barrier' can be considered as arising from the analogue cell testing difficulties previously described, and from the isolation of these cells from adequate control and observation of a test system by intervening digital circuitry.

2 Review of progress

Work at the Polytechnic of Huddersfield commenced with an examination of structured digital test strategies that are capable of meeting the test requirements of the large scale digital systems encountered in current mixed-signal ICs, and which could be modified to provide test access to the embedded analogue circuit cells. A digital scan-path-based testing strategy was selected on the grounds of fault coverage, and on the emergence of an IEEE test standard with which a developed mixed-signal test strategy could also comply.

Scan-path analysis is a widely adopted test technique in which complex digital systems are partitioned by multipurpose registers interconnected by a serial data bus (scan path) dedicated to system testing. Test vectors for each element of a partitioned digital circuit can be loaded, and the response of each element can be extracted by means of the serial data bus or scan path, providing a high degree of fault coverage for the device. The disadvantages of scan-path-based testing include the time penalty incurred in loading test vectors and extracting and analysing the test results, and the increase in device complexity and device area incurred in the incorporation of the scan-path/self-test structure. Test time penalties can however be minimised by specifying a highly optimised set of test vectors generated by automatic test pattern generation (ATPG) software, or by employing deterministic self-test (e.g. BILBO) techniques that combine elements of both BIST and scan-path strategies.

The adoption of a digital scan-path structure for accessing the analogue circuit cells buried within a mixed-signal IC places constraints on the choice of analogue test strategy. The demands made on the limited data capacity scan-path structure by digital cell test vectors and responses require that the analogue test strategy minimises scanpath data loading.

Scan-path loading constraints have resulted in the adoption of an analogue cell test strategy based on the evaluation of the transfer function of the cell under test by transient response techniques. Whereas the original candidates for the analogue cell test strategy included forms of pole-zero matched stimulus [3], and analogue built-in self test (HBIST) [4], transient response testing [2, 5] was selected on the basis of the simplicity of test vector generation, low silicon area overhead, and logic-impulse test vectors which can be propagated directly via the scan path. Transient response analysis is an established technique, in which short duration pulses whose bandwidth exceeds that of the circuit under test, are employed to excite an analogue system. The response of the analogue cell to a transient stimulus contains information which completely specifies its transfer function, and hence its functionality. The choice of transient response testing, therefore offers the advantage of minimal scan-path data loading, simple test vector generation, and the ability to directly propagate 'analogue' test vectors via the scan path, and other digital systems.

3 Interface scan (IS)

The form of the proposed test structure, termed 'interface scan', is depicted in Fig. 1, and consists of a modification of the digital scan-path based techniques previously described, in which special interface scan registers are incorporated into the scan path to provide test access to analogue as distinct from digital circuit cells. In this strategy, the digital systems of the circuit under test are verified by conventional test techniques. Testing of the analogue systems is accomplished by the incorporation of special forms of scan-path register (interface registers) which partition the device under test, and interface the analogue circuit elements to the scan path at selected boundaries between the analogue and digital systems.

The analogue cell test vectors and system responses are transferred via the scan path, and at the boundary of the analogue cells are converted between analogue and digital signal formats by the convertors that exist to interface functional signals between the analogue and digital systems. The need to fabricate signal convertors as part of the test structure is therefore avoided, and the increases in device complexity and silicon area overhead incurred by a scan-path-based test structure are minimised. In smaller mixed-signal devices, or those containing relatively few buried analogue test nodes, analogue multiplexing techniques may also be employed to extract cell responses directly.

The residual area overhead is a function of the number of transitions between the analogue and digital systems that require control and observation, and, where adequate fault coverage can be maintained, can be further reduced by applying the technique to a subset of a devices internal nodes, or by using simplified IS structures to provide a monitor-only facility.

The incorporation of an interface scan structure into a mixed-signal IC provides the ability to monitor and/or control selected circuit nodes at the interface between analogue and digital systems, and, in combination with a digital scan-path-based test strategy, enables the analogue and digital elements of a mixed-signal device to be accessed for test. It is considered that implementation of the technique is best achieved by incorporating the IS structure into the 'background' of the array of analogue cells available to a circuit designer.

4 Results

Device models for bipolar operational amplifiers forming a part of GEC-Plessey Semiconductors DA (2 μm) silicon cell library, were net-listed and simulated on both Apollo and Sun SPARC workstations, using HSPICE as the simulation tool.

The accuracy of these simulations was verified by direct comparison with measurements made on a batch of functional device samples, employing an enhanced Hewlett-Packard analogue ATE system. A high degree of correspondence between measurement and simulation was obtained. Device measurements also enabled the effects of process variations, observed as marginal differences between the transient response of individual devices, to be analysed statistically and expressed in the form of a standard deviation from the mean response of a functional circuit.

The evaluation of transient response testing in simulation, required the development of a suitable circuit-level fault model that was compatible with HSPICE, and capable of reproducing a set of process defects observed in production by GEC-Plessey Semiconductors. The developed model, depicted in Fig. 2, is capable of simulating parametric variations in resistor diffusions, leakage and open-circuit conditions in capacitors, and six discrete transistor defects. The actual fault simulated is

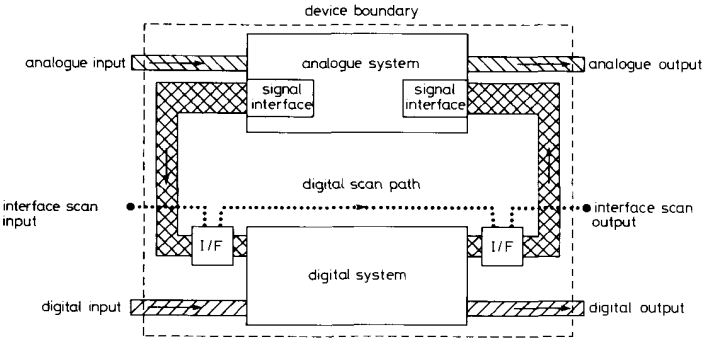

Fig. 1 *Mixed-signal circuit model incorporating interface scan testability*

determined by the state of the switches depicted in this model, and by the fault resistor values. Two fault resistor sets, representing 'out-of-tolerance' and 'catastrophic' models were simulated.

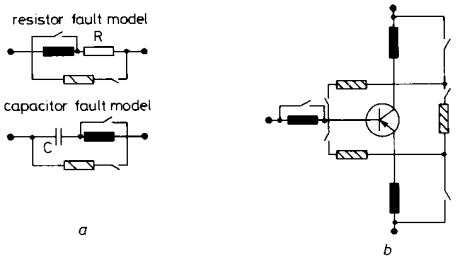

Fig. 2 *Analogue cell fault models*
a Passive component fault models
b Bipolar transistor fault model
leakage resistor model
open-circuit resistor model
short-circuit resistor model
An introduced fault is determined by the states of the depicted switches and by fault resistor values

A total of 196 discrete faults from this model were introduced into net-lists of the GPS 'OPA1' operational amplifier cell, configured as an inverting unity-gain amplifier, and transient response simulations were performed under HSPICE. The transient response obtained in simulation for each fault condition was compared with that obtained from a 'fault-free' circuit simulation, to derive a 'fault-signature'.

The criterion established for the detection of a cell fault condition by transient response analysis is that the amplitude of the fault signature exceeds the standard deviation of the mean fault-free response obtained in measurement by a factor of three. At this measurement threshold, the analogue cell fault coverage obtained by this analysis for 'out-of-tolerance' fault model A exceeds 75%. and that of the 'catastrophic' fault model B exceeds 84% (Fig. 3).

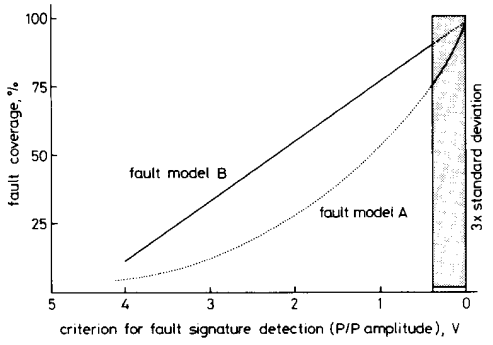

Fig. 3 *Fault coverage as a function of fault signature amplitude*

Recent work has concentrated on the testing of more complex analogue systems. An evaluation of transient response testing of active analogue filter systems, has demonstrated that discrete faults introduced into the operational amplifiers cells comprising these filters are less readily detectable by the elementary signature analysis technique previously described. This result has been anticipated, and is a consequence of the filter overall transfer function being determined by the properties of a feedback network, rather than by the performance of individual operational amplifiers. One consequence of this phenomenon may be that the highly complex analogue systems anticipated in future devices, whose performance is largely dominated by feedback networks, can be considered as possessing a degree of 'tolerance' to noncatastrophic circuit faults. More sophisticated forms of transient signature analysis are, however, currently under development in an attempt to improve the degree of fault coverage in these systems.

5 Future work

Having defined the proposed interface scan test structure, and having evaluated the associated analogue test strategy, the next phase of this project will investigate the further development of the analogue fault models employed to date, and the development of s statistical and/or signal-processing-based tools for analogue fault-signature analysis. Further trials of transient-response-based testing strategies will involve the testing of devices deliberately fabricated with defined fault conditions.

Simulation of the interface scan structure will require recourse to a true mixed-signal simulation environment such as CADENCE, or alternatively VIEWLOGIC, which could be operated in conjunction with a mixed-signal design package developed by GEC-Plessey Semiconductors (Plessey Design Modelling).

6 Conclusions

Interface scan is designed to be a flexible technique that satisfies the general requirements of a mixed-signal analogue cell testing strategy outlined in the introduction of this paper. The ability to partition the circuit under test, and to apply various forms of analogue test strategy via a digital test structure, permits the optimal analogue test technique for the particular types of analogue system to be employed.

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8 References

1 DUHAMEL, P., and RAULT, J.C.: 'Automatic test generation techniques for analogue circuits and systems: a review', *IEEE Trans.*, 1979, **CAS-26**, (7), pp. 411–440
2 EVANS, P.S.A., AL-QUTAYRI, M.A., and SHEPHERD, P.R.: 'On the development of transient response testing techniques for mixed-mode integrated circuits', *J. Semi-Custom I.C.s*, Dec. 1990, pp. 34–37
3 SCHREIBER, H.: 'Fault dictionary based upon stimulus design', *IEEE Trans.*, 1979, **CAS-26**, (7), pp. 529–537
4 OHLETZ, M.J.: 'Hybrid built in self test for mixed analogue/digital integrated circuits'. Proceedings of European Test Conference 1991. Munich, Germany, pp. 307–316
5 EVANS, P.S.A., AL-QUTAYRI, M.A., and SHEPHERD, P.R.: 'A novel method for testing mixed-signal ICs'. Proceedings of European Test Conference, 1991, Munich, Germany, pp. 301–306