Design of sensor electronics for electrical capacitance tomography

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Abstract: The design of the sensor electronics for a tomographic imaging system based on electrical capacitance sensors is described. The performance of the sensor electronics is crucial to the performance of the imaging system. The problems associated with such a measurement process are discussed and solutions to these are described. Test results show that the present design has a resolution of 0.3 femtofarad (For a 12-electrode system imaging an oil/gas flow, this represents a 2% gas void fraction change at the centre of the pipe) with a low noise level of 0.08 fF (rms value), a large dynamic range of 76 dB and a data acquisition speed of 6600 measurements per second. This enables sensors with up to 12 electrodes to be used in a system with a maximum imaging rate of 100 frames per second, and thus provides an improved image resolution over the earlier 8-electrode system and an adequate electrode area to give sufficient measurement sensitivity.

1 Introduction

Electrical capacitance tomography provides a promising technique for imaging industrial multiphase processes [1]. Since the development of the first working model based on an 8-electrode capacitance sensor [2], there has been continual effort to improve the performance of the system and to develop it into an industrial product [3]. Contemporary work with applications to fluidised solids bed processes has also been carried out in the USA [4]. A basic capacitance-based tomographic imaging system (Fig. 1) consists of three parts — the primary sensor, the sensor electronics and an image reconstruction computer. The functions of the sensor electronics include selection of electrode-pair combinations, measurement of capacitances between all possible combination pairs of the electrodes (and by doing so, interrogating different areas in the sensing volume), conversion of measured capacitance values into digital signals and interfacing the data acquisition part with the image reconstruction computer.

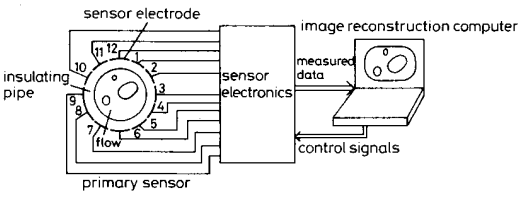

Fig. 1 *Capacitance-based tomographic imaging system*

The spatial resolution of the capacitance tomography system depends primarily on the number of sensor electrodes mounted around the process being imaged. However, given the dimension of the imaging volume, the size of each electrode is reduced as the total number of electrodes increases. This results in a reduction in the sensitivity of capacitance measurement. For a 12-electrode system, for instance, the minimum standing capacitance (between two diagonally separated electrodes when the pipe is empty) is as small as 0.015 pF (when the length of the electrode along the axial direction is 0.1 m), and the measurement resolution required by some applications, e.g. with oil and gas based processes, is often 2% of this standing value (0.3 fF). To resolve such a small capacitance change, the sensor electronics must be designed to provide high sensitivity, high signal-to-noise ratio (SNR) and low baseline drift.

Some requirements for an industrial version of the sensor electronics intended for online imaging of oil/gas flows in oil industry are

(*a*) compatibility with primary sensors with up to 12 electrodes

(*b*) high measurement resolution (0.3 fF, corresponding to a 2% gas void fraction change in the central area of the pipe)

(*c*) low noise level (rms value less than 0.1 fF)

(*d*) low baseline drift

(*e*) wide dynamic range of measurement (from 0.3 fF up to 2 pF)

(*f*) fast data capture rate (capable of capturing all measurement data for one frame of the image in 10 ms)

(*g*) fully software-controlled circuit setting

(*h*) communication capability with image reconstruction computer (a transputer network) located at remote distance up to 250 metres.

The following Sections show how these objectives are achieved.

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2 Capacitance measurement

2.1 The basic capacitance measuring circuit

An essential requirement of the imaging system is that the measuring circuit should measure only the capacitance between the selected pair of electrodes and it should be insensitive to stray capacitances between the measuring electrodes and earth. This implies that a stray-immune capacitance measuring circuit should be used for the measurement. Typical examples of stray-immune circuits are AC ratio-arm bridges with current output and the switched-capacitor charge transfer circuit [5]. The AC bridges operate usually with excitation frequencies lower than 100 kHz, and they are superior to the charge transfer circuit in terms of low baseline drift and high SNR. However, with a switching frequency of up to 2 MHz. the charge transfer circuit can offer a faster data capture rate, and because of its simple circuitry, parallel measurement channels can be used to further increase the speed without a substantial increase in cost and complexity of the circuitry. For more complex circuits based on AC bridges, the use of parallel measurement channels means that each channel will have its own demodulator, and this results in a substantial increase in complexity and cost of the electronics. In considering the requirement for data capture speed and the complexity of the sensor electronics, the charge transfer circuit has been chosen as the basic capacitance measuring circuit, and with an intention to match the performance of the AC bridges, measures have been devised to reduce its baseline drift and noise level (see Sections 2.2 and 3.3).

The principle of the basic measuring circuit can be explained with reference to Fig. 2. One electrode of the

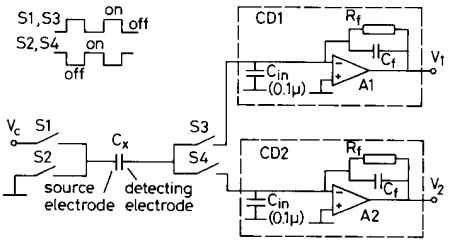

Fig. 2 *Basic capacitance measurement circuit*

unknown capacitance (source electrode) is connected with a pair of CMOS switches, S1 and S2, and another (detecting electrode) is connected with switches S3 and S4. In a typical operating cycle, the switches S1 and S3 are first closed (S2 and S4 open) to charge the unknown capacitance, C_x, to voltage V_c, and the charging current flows into the input (at virtual earth potential) of the current detector CD1 where it is converted into a negative voltage output. In the second half of the cycle, switches S2 and S4 close (S1 and S3 open) to discharge C_x to earth potential. The discharging current flows out of the current detector CD2, producing a positive voltage output. This typical charge/discharge cycle repeats at a frequency, f, and the successive charging and discharging current pulses are averaged in the two current detectors, producing two DC output voltages

$$V_1 = -fV_c R_f C_x + e_1 \quad (1)$$

$$V_2 = fV_c R_f C_x + e_2 \quad (2)$$

where R_f is the value of the feedback resistors of the current detectors, and e_1 and e_2 are output offset voltages of CD1 and CD2 caused mainly by the charge injection effect of the CMOS switches (see Section 2.2). The offset voltages of the operational amplifiers, A1 and A2, have only minor contributions to e_1 and e_2 compared with the charge injection effect. The capacitors C_{in}(0.1 μF) ensure that the virtual earth potentials at the inputs of CD1 and CD2 remain stable during the high speed charge and discharge operation. Since, during the operation, the source electrode is always connected with low impedance supplies (V_c and earth), and the detecting electrode always at virtual earth potential, stray capacitances have virtually no effect on the measurement [6].

The dynamic characteristics of the current detectors are similar to that of a first-order low-pass filter with a time constant T determined by $R_f C_f$. The time constant is so chosen that sufficient attenuation to the switching frequency f is ensured and the bandwidth of the amplifier noise is limited, while the required data capture speed is satisfied.

The differential output voltage, $V_1 - V_2$ is taken as the output signal of the basic circuit. From eqns. 1 and 2,

$$V_2 - V_1 = 2fV_c R_f C_x + e_2 - e_1 \quad (3)$$

Compared with eqn. 1 or 2, eqn. 3 shows that the differential structure has gained two advantages. First, the sensitivity of the measurement has been doubled to $2fV_c R_f$. Secondly, the output offset voltages e_1 and e_2 tend to cancel each other out provided that S3 and S4 have similar charge injection effects and the two operational amplifiers have matched offset voltages (from a dual amplifier package, for instance). Another advantage of this differential structure can be gained when the measurement is applied to fluids carrying electrostatic charges, as in the case of pneumatically conveyed solids. The electrostatic charges induce a noise current flowing into the detecting electrode [7] and produce noise voltages at the detector outputs. Since the fequency of the noise current is much lower (usually less than 100 Hz) than the switching frequency f the noise current flowing into CD1 and CD2 during two successive switching intervals (charge and discharge) can be treated as being of equal amplitude. Therefore the two noise voltages cancel each other out in the differential output.

2.2 The charge injection effect

Charge injection is caused by the feedthrough of gate control signals of semiconductor switches via the gate-channel capacitance [8]. In the circuit shown in Fig. 2, the gate control signals for switches S3 and S4 inject unwanted charge into the current detectors, resulting in offset voltages at their outputs. The offset voltage e_1 (as well as e_2) can be expressed by the following formula:

$$e_1 = fV_h R_f C_1 \quad (4)$$

where V_h is the 'high' level voltage of the gate control signal, C_1 represents the charge injection capacity of switch S3 and is proportional to the value of the gate-channel capacitance. The value of C_1 depends on the physical properties of the switch. From our experience, even the same type of switches from different manufacturers, e.g. the 4066 CMOS switches, can have very different C_1 values, although the typical values specified in their data sheets are the same. The value of C_1 depends also on the voltage level of the signal channel with respect to the supply potentials of the switch (Fig. 3). The injection capacity is lowest when the channel input/output is at the Vss potential, and becomes much higher

when the level is half way between the supplies *Vdd* and *Vss*. In this design, the signal potentials of S3 and S4 are virtual earth and the *Vss* is connected to earth. Therefore

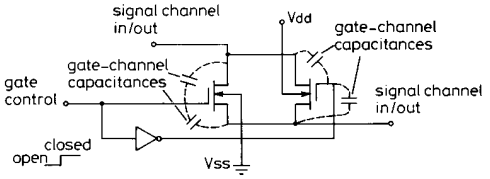

Fig. 3 *Structure of CMOS switches*

for a given pair of S3 and S4, the charge injection is at its lowest.

A test was carried out using the circuit shown in Fig. 2 with the control signals to S1 and S2 disconnected (no charge/discharge operation) so that the output voltages were caused mainly by the charge injection effect of S3 and S4. A MC14066 CMOS switch IC from Motorola was used to provide the switches, S3 and S4, and the value of C_1, worked out from the offset voltage according to eqn. 4, was 0.1 pF. This is equivalent to an unknown capacitance input of 0.1 pF because in this circuit, V_h equals V_c, and combining eqn. 1 with eqn. 4 produces

$$V_1 = -fV_c R_f(C_x - C_1) \quad (5)$$

When the differential output $V_2 - V_1$ was measured, this effect reduced to about 0.03 pF. It was also observed that C_1 was sensitive to temperature change. Over a temperature change of 15°C, the drift measured on the differential output was equivalent to an input capacitance change of 0.005 pF. It was found that the temperature sensitivity of the charge injection capacity contributed most to the baseline drift of the capacitance measuring circuit.

The test results shown above indicate that although the differential structure reduces the output offset voltage caused by the charge injection effect, there is still some 20–30% of this effect remaining. More importantly, the temperature drifts of the charge injection on two different switches can not match each other very well even when the switches are on the same IC chip. Considering the required measurement resolution of 0.3 fF, the baseline drift must be corrected by the arrangement described below.

The idea is to check the baseline regularly and correct the drift by subtracting the baseline from the values measured afterwards. To implement this, a baseline checking mode is incorporated into the circuit operation. In this mode the source electrode is earthed while the switches S3 and S4 remain operational, and the output offset due to the charge injection is measured. Then the measurement is restarted by enabling the charge/discharge control signals connected to S1 and S2, and the offset value obtained in the checking period is subtracted from each measurement value obtained after the check. The time period needed for the checking is short. For a 12-electrode system with 11 measurement channels (see Section 3), the baseline checking needs about 1 ms which is about one tenth of the time required for capturing a complete set of measurement data. The frequency of the checking can be determined arbitrarily. If performed once in a second, approximately 100 frames of imaging data can be obtained between two checking intervals. Considering the length of the measurement mode, the short checking interval will have little influence on the data acquisition process.

3 Overall sensor electronics

3.1 Operating principle

The principle of the sensor electronics is shown by Fig. 4. The circuit is designed to accommodate up to 12 sensor

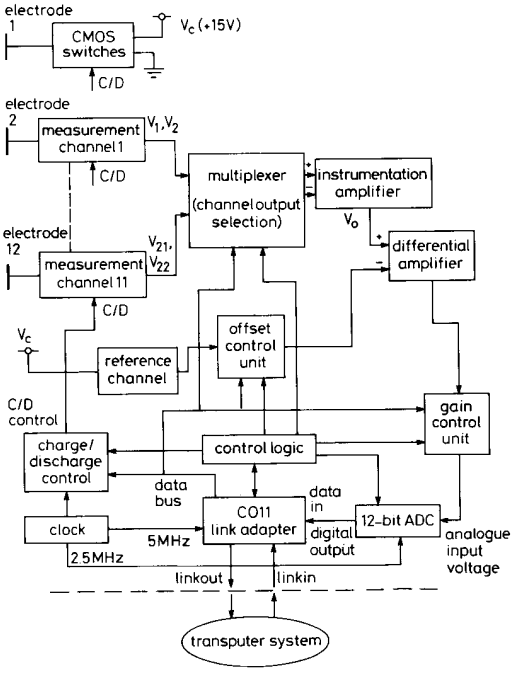

Fig. 4 *Sensor electronics circuit*

electrodes. To increase the overall data capture speed, parallel measurement channels are used. Each measurement channel consists of a 4066 quad CMOS switch and a pair of current detectors. For a 12-electrode system, sensor electrodes 2 to 12 are each connected with such a channel whereas electrode 1 is connected only to a pair of CMOS switches performing charge/discharge functions. The charge/discharge (C/D) control circuit controls the status of the electrodes. Electrodes 2 to 11 can be selected as either the source or detecting electrodes; electrode 1 can be set to either active (source electrode) or idle (earthed), while electrode 12 always works as a detecting electrode. A complete data capture cycle can be explained with reference to Fig. 1. First electrode 1 is selected as the source and electrodes 2 to 12 as the detecting ones. The capacitances between electrode pair 1–2, 1–3, to 1–12 are measured simultaneously. (The source and each of the detecting electrodes as well as the corresponding measurement channel form the measurement circuit shown in Fig. 2.) These parallel measurements are independent because the capacitances are determined from the charge and discharge currents through the detecting electrodes and these are all held at virtual earth potential. The 11 parallel channel outputs are selected one by one by a multiplexer for further amplification and A to D conversion. The amplification and conversion time is short compared with the settling time of the current detector in a

measurement channel whereas the effect of the latter on the overall speed of data acquisition is reduced by the parallel channel approach. In the second step, electrode 2 is selected as the source (electrode 1 set to idle) and electrodes 3 to 12 as the detecting ones. Capacitances between 2–3, 2–4, to 2–12 are measured and converted into digital signals. This process continues until electrode 11 is selected as the source and 12 the detecting one, and the capacitance between electrodes 11 and 12 is measured. Generally for an n-electrode system, the number of independent measurements N is given by the following equation of combination:

$$N = n(n-1)/2 \tag{6}$$

For a 12-electrode system, this number is 66.

3.2 Automatic zero and gain balance

A problem associated with capacitance measurement in the imaging system shown in Fig. 1 is that the standing capacitance values and sensitivity of different electrode pairs can be very different. For instance, for a 12-electrode system, the standing capacitance value (when the pipe is empty) between electrodes 1 and 2 is about 100 times that between 1 and 7, and even for the similar pairs, such as 1–2 and 1–12, the measured standing values may be more or less different owing to manufacturing errors of the electrodes and different charge injection levels of different channels (see Section 2.2). This causes difficulties for the capacitance measuring circuit which has a relatively limited dynamic range. To avoid saturation when measuring the capacitance between adjacent electrodes, the sensitivity of the circuit has to be kept at a value that is too low for measuring the diagonally separated electrodes.

The solution to this problem is to use a programmable reference voltage to balance the different standing values of the measurements (zeros) and a programmable gain amplifier to satisfy the different sensitivity requirements. A calibration procedure has been designed to learn the 66 zeros and required measurement sensitivities (Fig. 5) and it should be performed before the measurement and imaging process. During the calibration, the sensor pipe is first filled with the component of lower permittivity (e.g. air for a gas/liquid two-component process) and the 66 capacitances are measured and stored as the zeros. Then the pipe is filled with the component of higher permittivity and the sensitivity of the circuit is changed for each different measurement to achieve the required output level. The 66 sensitivity values thus obtained are then stored in the transputer system. During the measurement process (Fig. 6), each time after a measurement channel is selected and before the A to D conversion starts, the stored zero and sesitivity values for this particular configuration are sent from the transputer to the offset and gain control units to preset the appropriate zero balance and gain. The offset and gain control units can receive 10 bit digital codes and this allows a fine adjustment of the corresponding parameters.

3.3 Noise

Because of the requirement for a high measurement resolution, the noise level of the circuit becomes critical. Assuming Gaussian noise, its rms value should be at least less than a third of the smallest signal level. (Only 0.3% of the noise readings may exceed the smallest signal).

According to a test carried out on an experimental prototype version of this circuit, the noise voltage at the input of the A to D converter consists of a periodic high frequency content, a wide-band random noise and 50/100 Hz interferences. The fact that the periodic noise has the same frequency as the switching frequency f sugests that it is caused by a layout of the circuit which allows switching current pulses flowing through analogue

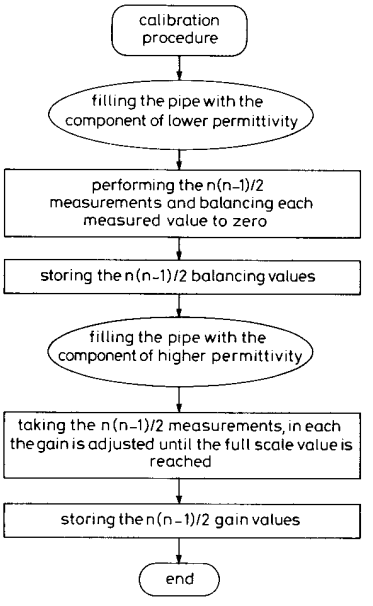

Fig. 5 *Calibration procedure*

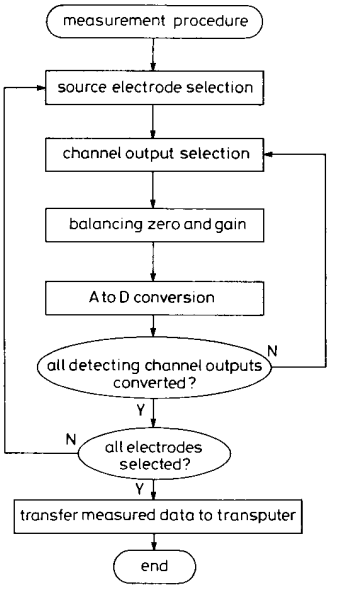

Fig. 6 *Measurement procedure*

ground returns. The random noise signal is generated from the semiconductor devices, in particular the operational amplifiers used to form the first stage current

detectors. The 50/100 Hz interferences come from power supplies and ambient electric fields.

The level of the noise can be much larger than the smallest signal level if the design rules for circuit layout are not adhered to and the right types of operational amplifiers not chosen. The rms value of the noise of the experimental prototype mentioned above was equivalent to an input capacitance of 1 fF. To this the random noise contributes 0.35 fF when operational amplifiers with an e_n (equivalent input noise voltage) of 30 nV/$\sqrt{}$(Hz) at 1 kHz are used for the first stage detectors.

The following measures have been taken in the design to ensure a low noise level:

(*a*) Separate supplies and ground returns are used for the analogue and digital parts respectively, and large area ground planes are used.

(*b*) The bandwidth of the circuit is limited to no more than is needed for achieving the required data capture rate. The overall data acquisition time for one image is given by

$$T_0 = 11T1 + 66(T2 + T3 + Tadc) \quad (\mu s) \tag{7}$$

where $T1$ is the settling time (to 0.1%) of the current detectors, $T2$ the settling time of the intermediate amplifiers, $T3$ the time of communication between the sensor electronics and the transputer system during a measurement and $Tadc$ the A to D conversion time. To trade off the speed and the SNR, $T1$ is chosen as 500 μs and $T2$ 20 μs, whereas $T3 = 20$ μs and $Tadc = 5$ μs are determined by the communication requirement and the specification of the A to D converter. Thus a T_0 of about 8.5 ms (smaller than the required 10 ms) is obtained.

(*c*) Operational amplifiers with very low input noise (<4 nV/$\sqrt{}$(Hz) at 1 kHz) are used for the first stage of the measurement and reference channels.

(*d*) The power supplies to the ICs are properly decoupled.

(*e*) Careful shielding of the circuit is used to reduce internal coupling and external EM interface.

3.4 Interface to the reconstruction computer

As shown in Fig. 4, a CO11 transputer link adaptor (from INMOS) is used to provide an interface between the sensor electronics and the transputer system for image reconstruction. The link adapter is built into the sensor electronics, and is connected with the transputer system via two serial communication links, one input and one output. Control codes from the transputer are converted by the CO11 into parallel outputs, and the parallel output from the A to D converter is converted into a serial output and sent to the transputer system. The functions of the control codes include:

(*a*) selection of operating mode, measurement or baseline checking

(*b*) selection of electrode status (source, detecting or idle)

(*c*) selection of measurement channel outputs for A to D conversion

(*d*) zero balance

(*e*) gain control

(*f*) A to D conversion control

(*g*) switching frequency selection (625 kHz for low sensitivity or 1.25 MHz for high sensitivity of measurement).

The sensor electronics support both electrical and optical fibre links between the transputer system and the CO11. For the standard 10 Mbit/s data communication rate, electrical link cables can be used with a maximum length of 13 metres, whereas optical fibre links can be used over a much longer distance (up to 250 metres). This enables the image reconstruction computer to be placed in a less hostile environment far away from the sensor electronics which are usually mounted on the pipeline.

4 Test results

The sensor electronics shown in Fig. 4 have been constructed on printed circuit boards. Their performance has been tested in the laboratory and the results are given as follows:

4.1 Noise level

Mainly random noise was observed with the PCB version of the electronics, and this was found to have been generated mainly by the first stage detectors. When OP270s ($e_n = 3.8$ nV/$\sqrt{}$(Hz)) from PMI were used for these, the typical rms value of noise voltage measured at the input of the A to D converter was equivalent to an input capacitance of 0.08 fF. It can be observed from the probability density function of the noise (Fig. 7) that the

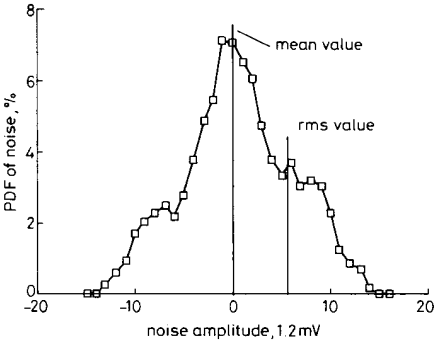

Fig. 7 *Probability density function of the noise*
—□— P.D.F. of noise

peak level of the noise voltage does not exceed 19.3 mV (equivalent to 0.26 fF input capacitance), which is below the minimum signal level (0.3 fF). The ratio of the minimum signal level to the rms value of the noise is 3.8. In a test of an imaging system incorporating the sensor electronics, although some background noise can be observed on the reconstructed image, a plastic rod at the pipe centre occupying 2% of the pipe cross-section can be identified, showing that the SNR is acceptable.

4.2 Baseline drift

The stability of the system incorporating the baseline correction arrangement can be represented by its baseline drift with time and temperature. When the system was placed in a room with a constant temperature (± 1°C change maximum), no apparent baseline drift was observed during a period of 5 hours. However, a temperature drift test is to be carried out in the future.

4.3 Speed

The data acquisition time for obtaining the 66 independent measurements (for reconstructing one image) was measured using the 'timer' function of the transputer. Using a T801 transputer running at 25 MHz as the sensor electronics controller, the resultant time was 10 ms. This is longer than the 8.5 ms estimated using eqn.

7 owing to the fact that the execution time of the Occam instructions on the transputer is not included in eqn. 7.

4.4 Dynamic range

The smallest capacitance change detectable (3.8 times of the rms noise) is 0.3 fF. The maximum input capacitance acceptable is 2 pF. The dynamic range is calculated as

$$D = 20 \log (2/0.0003) = 76.5 \text{ dB}$$

5 Discussion

The sensor electronics described in this paper are suitable for use with capacitance tomographic imaging systems with up to 12 electrodes. The low noise level of 0.08 fF (rms value) enables capacitance changes as small as 0.3 fF to be detected, which is equivalent to a 2% void fraction change in a gas/oil flow in the central area (least sensitive area) of pipe. The automatic zero and gain balance method used in the design provides a 76.5 dB dynamic measurement range. The maximum data capture rate is 100 frames per second.

The measurement resolution of the circuit is mainly limited by the level of noise voltage generated in the circuit. Some possible ways to further improve the SNR in the future are

(*a*) the use of operational amplifiers with lower noise if they become available (preferably dual versions, see Section 2.1)

(*b*) to further increase the switching frequency f. The ratio of the signal to the random noise is proportional to f (because as shown by eqn. 3, the signal level is proportional to f). For instance, an increase in the frequency from the present 1.25 MHz to 1.5 MHz will improve the SNR by 20%. However, the maximum frequency that can be used is limited by the following equation:

$$f_{max} = 0.025/(R_{on} C_s) \quad (8)$$

where R_{on} is the 'on' resistance of the CMOS switches, C_s the stray capacitance between an electrode (including its lead) and the earth. Eqn. 8 implies that the frequency is limited by the settling time needed to fully charge the electrode to V_c (with 0.01% accuracy). In this design, C_s is typically 150 pF, and R_{on} 100 Ω. Therefore the maximum frequency is limited to about 1.7 MHz.

(*c*) to reduce the bandwidth of the sensor electronics when high speed data acquisition is not required. For instance, if only 50 frames imaging data per second is required, the bandwidth of the measuring circuit can be halved, and thus the SNR can be improved by a factor of $\sqrt{(2)}$.

If a further increase in the number of the electrodes, say to 16, is required, or the length of the electrode is to be greatly shortened to reduce the averaging effect along the axial direction, then the present design based on the charge transfer principle may not satisfy the required SNR, and circuits based on the AC bridge techniques may be appropriate. With a bridge, the input capacitance signal would be modulated by a sinusoidal wave, and this would allow bandpass filters to be used before demodulation, to greatly reduce the bandwidth of the random noise. High order bandpass filters and phase sensitive demodulators can be implemented on digital signal processors, which form part of the image reconstruction unit, thus reducing the complexity of the sensor electronics.

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