# Integrated Capacitors for Conductive Lithographic Film Circuits

Paul M. Harrey, Peter S. A. Evans, *Member, IEEE*, and David J. Harrison, *Member, IEEE*

***Abstract*—This paper reports on fabrication of low-value embedded capacitors in conductive lithographic film (CLF) circuit boards. The CLF process is a low-cost and high speed manufacturing technique for flexible circuits and systems. We report on the construction and electrical characteristics of CLF capacitor structures printed onto flexible substrates. These components comprise a single polyester dielectric layer, which separates the printed electrode films. Multilayer circuit boards with printed components and interconnect can be fabricated using this technique.**

***Index Terms*—Conductive lithographic films, embedded capacitors, flexible circuits, integrated passive components, multilayer circuits.**

## I. Introduction

THE demand for increased functionality and miniaturization in electronic products and devices requires the electronics industry to manufacture boards with increased component density. In hand-held product design the aim is to increase functionality through higher levels of integration. As the number of IC's in these products decreases, the quantities of discrete components supporting each IC is on the increase [1], [2].

Increases in component density must be matched by corresponding decreases in package size if similar or more complex products are to be developed without additional product size. Further miniaturization of discrete components is however problematic. Manufacturers are experiencing difficulties with placement and inspection of the smallest size SMT components. The latest generation of component package, "0201" size components measures just 0.5 mm by 0.25 mm and this is proving costly to manufacture and assemble. The 0201 series is more expensive to manufacture than its previous generation and demands highly sophisticated equipment for component placement. Industry sources indicate that the manufacturing cost of current surface-mount components is typically less than the cost of transferring them to a board. Component placement cost can exceed the cost of manufacturing a component by up to four times [1].

In high performance products discrete passive components such as decoupling capacitors may also limit the operating speed of the circuit. The components are typically used to suppress power distribution noise created by the switching of numerous drivers. However, the devices may be large in size and have large parasitics which can reduce their efficiency for decoupling [3].

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### A. Integrated Passive Components

The integration of passive components into the packaging of the circuit board may overcome the problems associated with manufacturing and placing large numbers of small passive components. Integration of passive components into the circuit board packaging may also provide a solution to the speed limiting factors associated with existing discrete component architecture.

Several approaches to the fabrication of integrated components are being explored, advances in ceramic processing such as MCM-C [4], thin film components into flexible MCM-L substrates [5]–[7] and laminate materials in traditional multilayer PCB's [8]. More conventional approaches to passive integration include discrete-like component arrays and integrated networks for specific applications [9].

Discrete capacitors are used in larger numbers and greater density than any other discrete passive component [1]. There is considerable scope for removing a significant proportion of the discrete capacitors found in many electronic devices [1]. It is expected that hand-held products design will drive the implementation of integrated passive components into products.

As yet, there is limited consideration of passive component integration within low-cost flexible electronic circuits. Polymer thick film (PTF) flex circuits are manufactured by printing conductive films onto flexible substrates and are replacing Cu/Kapton circuits in many applications. Products which use PTF circuits include keyboard membranes, vehicle dashboards, telephones, light clusters and smart cards. Printed flexi circuits are typically low-cost, light in weight and low-profile, flexi-circuits can also conform to the curved inner surfaces of many products. Integrating passive components into the substrates of these circuits could offer lower circuit costs, improved reliability and an increase in the areas of application. Unlike surface mount componentry, integral passive components may be located on parts of the circuit which follow curved surfaces or indeed on flexible moving parts of a circuit. The Design Department, Brunel University, has developed the conductive lithographic film (CLF) process, a method of fabricating large-volumes of low-cost flexicircuits. The current objectives of the group are to develop a low-cost approach to fabricating low-cost flexi-circuits with embedded components.

### B. Conductive Lithographic Film Circuits

The conductive lithographic film circuits are fabricated by printing conductive film traces onto the surface of paper-like substrates using the offset lithographic film printing process. Offset lithography, often confused with the circuit-board imaging technique *photolithography* is the process commonly

used to print books, magazines and posters. The process is used on high speed, larger web-fed presses, capable of printing up to 900 m/min [10].

Conductive Lithographic Film circuits were first developed as low-cost and low-environmental impact alternatives to copper-clad FR4 boards and thick-film circuits [11]. CLF circuits have proved suitable for a number of applications, including planar microwave integrated circuits [12], filter structures [13], and switch pads in keyboard matrices [14].

The silver loaded printing inks are engineered to exhibit high conductivity when dried and to be suitable for use with standard printing presses [11]. The ink in its cured state has a thickness of 3–5 $\mu$m. The sheet-resistivity of a cured ink film is dependant on the substrate. The sheet-resistivity of a conductive film printed onto a pulped paper substrate such as Gloss-Art is $\sim .15\ \Omega/\square$.

## II. Embedded Capacitors in CLF Circuits

An emerging area of interest is the integration of passive components within CLF circuits. It is believed that there is a great potential for low-cost flexible circuitry with integrated passive components. A number of approaches to fabrication of integrated capacitor components have been considered.

The simplest type of printed capacitor is the interdigitated capacitor. The components are printed onto the surface of the substrate with standard conductive ink and can form an integral part of circuit interconnect. The component comprises two interdigitated "comb-like" electrodes separated by a fixed gap. The capacitance of the structures is a function of both the number of digits in the electrode and the distance of the gap separating the digits [15]. The interdigitated capacitor may be specified in applications where lumped components are neither cost-effective or suitable. One example is the twin-T analogue filter, a device developed for security documents [13].

Multilayer capacitor structures have been constructed by sequentially printing conductive ink film electrodes and titanium dioxide ink dielectric films. This work required the formulation of suitable dielectric inks containing high proportions of titanium dioxide. Capacitors of this type have been demonstrated in RC timing networks in flexible digital circuit boards. Capacitor structures with dielectric thickness of $\sim$20–25 $\mu$m exhibited capacitance densities of 625 pF/cm$^2$, the relative dielectric constant of the printed films was calculated at 17. Capacitors fabricated with printed ink dielectrics have a limited bending radius, this leads to brittle failure when flexed in a number of samples.

### A. Plastic Dielectric Film Capacitors

Recently, a new method of forming integrated capacitors has been developed. Parallel-plate capacitor can be constructed by printing electrodes either side of a polyester dielectric film. Single layer capacitor components are fabricated by first printing a conductive film on to the surface of the substrate. The substrate is typically 100 $\mu$m and acts as a carrier for the subsequent layers of ink and polyester film. A pre-drilled extruded polyester (PET) film is then registered to the printed substrate beneath and bonded to it to form a single piece. Finally a top electrode is printed onto the over the bottom film to form a parallel–plate construction. Fig. 1 illustrates a single dielectric

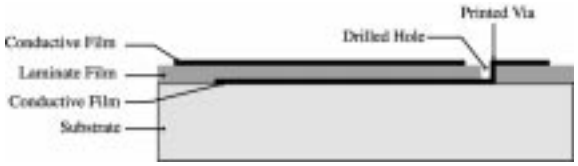


Fig. 1. Single-layer capacitor construction.

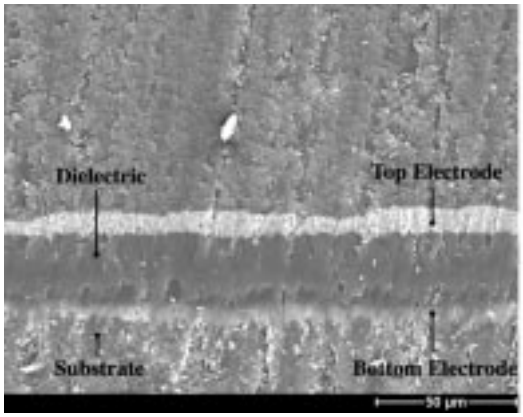


Fig. 2. Electron micrograph of a cross section of a CLF capacitor structure with single dielectric layer ($\times 550$).

layer CLF capacitor construction. The construction method can be extended to form multilayer capacitor structures by further lamination and electrode printing. The completed capacitor, essentially buried within the substrate can be connected to other internal layers and to components on the surface using printed CLF blind vias.

Blind vias are fabricated at the same stage as the circuit's interconnect and capacitor plates are printed. The vias are formed in the structure by drilling the polyester film prior to lamination, holes may be laser drilled or punched out. A conductive ink film is then printed over the edge of the pre-drilled holes in the laminate to connect one conductor plane to another. Fig. 2 is an electron micrograph of a cross-section of a single dielectric CLF capacitor mounted in resin and polished. The micrograph shows that the laminated dielectric film has a thickness of $\sim$26 $\mu$m and appears consistent throughout the section.

*1) Plastic Dielectric Film:* The dielectric film is a commercially available polyester (PET—Polyethylene Terephthalate) extruded film prepared with an adhesive layer on the underside of the film. The adhesive, a low melt copolymer (Polyethylene) is activated at temperatures in excess of 100 °C. When the film is subjected to the elevated temperature, the adhesive melts and allows the polyester film to adhere to the surface on a chosen substrate. The laminate film used in these trials is $\sim$26 $\mu$m thick and consists of a 12 $\mu$m polyester carrier and $\sim$14 $\mu$m of Polyethylene adhesive. A laminating machine is used to bond the dielectric film to the printed substrate. Lamination is achieved when the two are passed through heated rollers under pressure, the rollers ensure a consistent bond over the entire area of the film area.

*2) Fabrication of Capacitor Test Structures for Electrical Testing:* Test structures have been constructed on Teslin substrates. Fig. 3 shows a sample of a Teslin substrate complete with printed capacitors and inductors. The capacitors, fabricated with

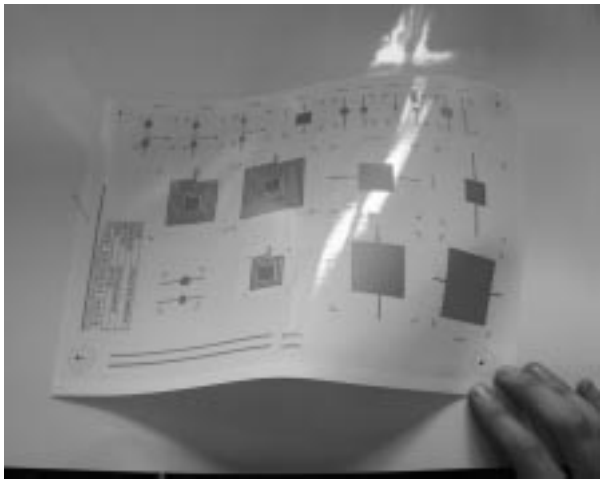

Fig. 3. CLF substrate complete with printed components.

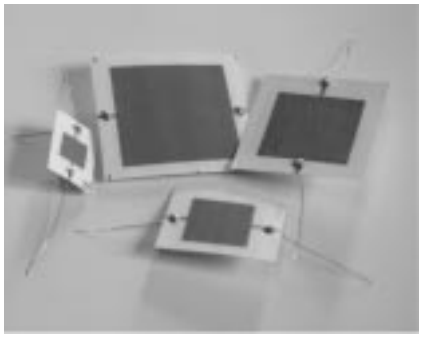

Fig. 4. CLF capacitor test samples.

a single dielectric layer have been printed with plate overlap areas ranging from 1 $mm^2$ to 40 $mm^2$. Examples of cropped test structures are shown in Fig. 4.

## III. Results

Initial electrical tests have been performed on a limited number of test samples of laminate capacitor design. Structures with 10, 20, 30, and 40 $mm^2$ plate overlap areas were included in the tests. Capacitance, Dissipation Factor, Equivalent Series Resistance, Reactance and Impedance were measured using a HP 4284 high precision LCR meter at frequencies up to 1 MHz. Manufactured discrete ceramic disk and polyester film capacitor components were included in the electrical tests for comparison purposes.

### A. Capacitance Density

The capacitance values of the four different plate areas were measured at a frequency of 1 MHz and with 1 Vrms test signal. Table I shows the mean capacitance value of the structures and their capacitance/area (capacitance density). The capacitance density figures shown are for single active layer devices. The capacitance value for a $(10\ mm)^2$ area structure measured 103.3 pF at a test frequency of 1 MHz. Capacitance density is proportional to the number of active layers in the device. 6 nF CLF capacitors have been fabricated with two dielectric layers, the structures had an increased capacitance density of $\sim 208\ pF/cm^2$.

TABLE I
Capacitance of the Four Structures

| Printed Plate Area ($mm^2$) | Mean Cap Value (pF) @ 1MHz | Mean Cap Density ($pF/cm^2$) | Capacitance Tolerance (%) |
|---|---|---|---|
| 10 | 103.3 | 103.3 | -3.6 +5.5 |
| 20 | 401.9 | 100.5 | -3.6 +4.9 |
| 30 | 900.0 | 100 | -3.7 +2.6 |
| 40 | 1580 | 98.75 | -1.96 +2.4 |

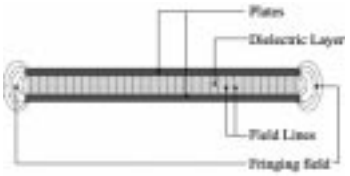


Fig. 5. Fringing field lines in a parallel plate capacitor.

Taking the capacitance values for the four structures and assuming a dielectric thickness of 26 $\mu$m, the relative dielectric constant (K) of the film is calculated at 2.9–3.0 at 1 MHz.

*1) Reduction of Capacitance Density With Increase in Plate Overlap Area:* It has been observed that for an increase in the capacitors printed electrode area there is a disproportional increase in capacitance value. Capacitance values taken from four different sized capacitors show that the capacitance density decreases as the printed electrode overlap area increases. The decrease in capacitance per area is believed to result from a decrease in the ratio of perimeter/area of the electrode and a decrease in the total flux between the electrodes. In addition to the field lines present directly between the two plates of a charged capacitor there is also a peripheral fringing field at the edges of the electrode area, this is illustrated in Fig. 5. The fringing field is believed small in comparison to the field present directly between the electrodes, however it does contribute to the overall capacitance of the device. As the electrode overlap area increases exponentially, the perimeter of the device increases only by a factor of two. It is considered that the fall in capacitance density with an increase in electrode area results from the decrease in fringing field/area of electrode.

### B. Tolerances

Table I shows the capacitor value tolerances achieved for 10 or more samples of each capacitor area size. Tolerances from $-1.96\%$ to $-3.7\%$ and $+2.4\%$ to $+5.5\%$ were achieved. The measurements were made at room temperature (20°C). The initial tolerances achieved are promising and may be improved with subsequent changes in the manufacturing process.

### C. Changes in Capacitance With Frequency

The capacitance value of the devices was measured at test frequencies of 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz, the LCR meter was calibrated at each test frequency A drop in capacitance values with frequency have been observed in all four structures over the frequency range 100 Hz–1 MHz. Fig. 6 shows the capacitance changes for the four structures over the frequency range. It can be seen that the drop in capacitance value

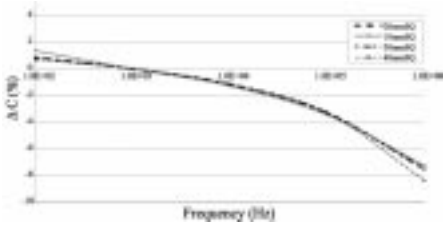

Fig. 6. Capacitance value of CLF capacitors versus frequency.

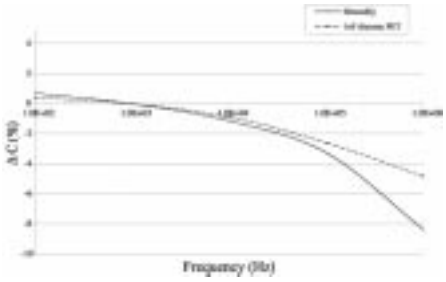

Fig. 7. Capacitance of 0.9 nF CLF device and 1 nF discrete.

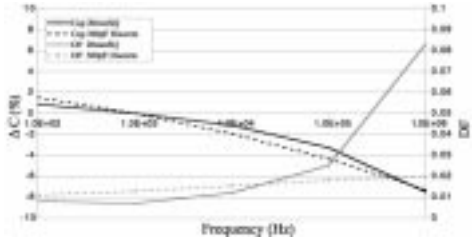

Fig. 8. Capacitance and dissipation factor for a CLF capacitor and a discrete.

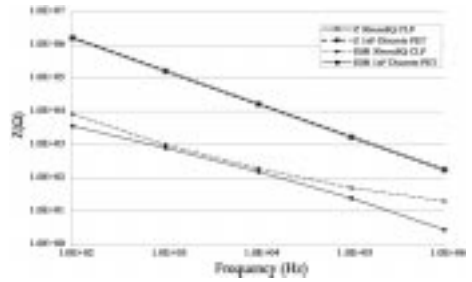

Fig. 9. Impedance and equivalent series resistance.

seems independent of plate area size and a typically a CLF capacitor may lose 8% of its capacitance value over this frequency range.

A drop in capacitance value with frequency is evident in many different types of capacitor, components such as an X7R stable dielectric multilayer ceramic capacitor (MLCC) may lose $\sim 8\%$ of its capacitance over the same frequency range [16]. In order to compare the behavior of the CLF capacitors with existing discrete components, a commercial capacitor was measured simultaneously over the same frequency range. The discrete component measured was a bought-in, low-cost 1 nF metallised polyester film device, (tol' $\pm 10\%$).

Fig. 7 shows the behavior of a 30 mm$^2$ plate area CLF capacitor (900 pF @ 1 MHz) and the measured discrete 1 nF component. It can be seen in Fig. 7 that the CLF and discrete components behave similarly between 100 Hz and 100 kHz. At frequencies above 100 kHz, the CLF structure's capacitance value drops more severely that the commercial component. In the frequency range 1 kHz–1 MHz the CLF printed capacitor and the metallised PET film components lose 8.4% and 4.8% capacitance value respectively. Capacitance measurements taken from CLF capacitors with different plate areas show a similar capacitance value response to frequency.

### *D. Dissipation Factor With Frequency*

Fig. 8 compares the mean change in capacitance and dissipation factor of the printed CLF capacitors with those of ceramic discrete component. The CLF capacitors have a single dielectric layer and a printed plate area of $(20\ \text{mm})^2$ which equates to a mean capacitance value of $\sim 400$ pF. The discrete component is an off the shelf 390 pF ceramic capacitor, the capacitance of this part measured 353 pF at 1 kHz using the LCR meter. The graph shows that the two devices both exhibit a drop in capacitance of $\sim 7\%$ from 1 kHz to 1 MHz.

The dissipation factor *DF* of the CLF printed capacitor and the discrete device is also shown in Fig. 8. The Dissipation Factor of a capacitor is the ratio of the equivalent series resistance (ESR) to capacitive reactance $(Xc)$ and is a function of the operating frequency of the component. In most applications it is desirable to have a low dissipation factor, a higher DF generally means a higher ESR and causes problems with power handling and internal heating

$$DF = \frac{\text{ESR}}{Xc} = 2\pi f CR. \tag{1}$$

Fig. 8 also shows the two different responses of the ceramic discrete and the CLF capacitors, the discrete exhibits a linear increase in DF of 1% to 2% over the frequency range of 100 Hz to 1 MHz. The DF of the CLF device drops marginally from 0.9% at 100 Hz to 0.8% at 1 kHz and rises to 8.4% at 1 MHz.

### *E. 3.5 Impedance and Equivalent Series Resistance*

The complex impedance (Z) characteristics of the CLF components and the 1 nF discrete component have been calculated using the expression in (2) for frequencies up to 1 MHz and are shown in Fig. 9. Although the measured frequency range does not give any information on the resonant frequency of the CLF device, it does suggest that the capacitor has similar characteristics to commercial capacitor devices of similar capacitance value. Included in the graph is the impedance plot of the bought-in 1 nF discrete, it is evident that the 0.9 nF CLF device and the discrete exhibit very similar impedance characteristics at frequencies up to 1 MHz.

The CLF capacitor also exhibits similar impedance responses to devices such as X7R MLCC 1 nF capacitor produced by Syfer Technology [16]

$$\text{Z} = \sqrt{(\text{ESR})^2 + (X)^2}. \tag{2}$$

The graph in Fig. 9 also compares the equivalent series resistance (ESR) of the two devices over the frequency range. ESR is the generic term for a lumped resistance parameter, which includes both dielectric and ohmic losses in a capacitor. At lower operating frequencies (1 kHz) the resistance of a capacitor is

TABLE II
INSULATION RESISTANCE OF CLF CAPACITORS

| Time (s) | $(10\text{mm})^2$ structure | $(20\text{mm})^2$ structure |
|---|---|---|
| | $R_I$ (GΩ) | $R_I$ (GΩ) |
| 30 | 10.11 | 7.46 |
| 60 | 11.97 | 8.46 |
| 120 | 13.36 | 9.79 |
| 180 | 14.86 | *NA* |

dominated by dielectric losses and at higher frequencies skin effect becomes significant and can dominate ESR. In most cases, ESR is an undesirable property that causes power loss in circuits and affects the time constant of the capacitor [17]. The ESR of the bought-in component is generally lower than that of the printed device, it also tends to fall more linearly as the operating frequency rises. The ESR of the printed device could be improved with a change in geometry. The use of multilayer structures with smaller plates will be investigated in the next phase of work.

### *F. 3.6 Leakage Current*

Leakage current measurements were performed on two sets of CLF capacitors, 20 samples of structures with plate areas of $(10\text{ mm})^2$ and $(20\text{ mm})^2$ were prepared and tested. A test voltage of 100 $V_{DC}$ was applied to the devices, a Keithley 617Programmable Electrometer was used to measure the leakage current. The DUT was connected into the circuit and a test potential of 100 $V_{DC}$ was applied. Leakage current measurements were made after a time of 30, 60, 120, and 180 s. Table II shows the mean insulation resistance $(G\Omega)$ for the two structures.

After the dc voltage was initially applied to the test structure, it was noted that the measured leakage current fell over time. Measurements show that the PET film offers a good level of insulation. In total, 60 samples were tested during the trials with no shorted devices reported. Although no voltage breakdown tests have been performed on the devices, ten samples were subjected to voltages of 300 $V_{DC}$ with no evidence of dielectric breakdown.

## IV. CONCLUSION

It has been demonstrated that low-value capacitors can be integrated into flexible CLF circuits using the technique of sequentially printing and laminating PET films to manufacture a multilayer flexible circuit board. Multilayer CLF flexible circuit boards can be manufactured complete with printed capacitors, interconnect and vias in the same operation. The dielectric material (PET) used in the CLF capacitors is a cheap and readily available extruded film manufactured with a heat-activated adhesive film on the underside. Successive pre-drilled films are registered and bonded to the surface of the previous film by passing through two heated rollers under pressure.

A capacitance density of $\sim 103$ pF/cm$^2$ at 1 MHz has been measured for single active layer structure CLF capacitors. It has also been shown that by sequentially printing and laminating additional PET films the capacitance density can be increased. A circuit containing a 10 layer capacitor substrate would give a capacitance density of 1.05 nF/cm$^2$ and have a thickness of $<400\ \mu$m yet still remain flexible.

Measurements of four different size CLF capacitors showed that capacitance and dissipation factor vary with frequency. In comparisons to commercial capacitors, the CLF's performed reasonably. Modifications to the electrode geometry may improve the electrical characteristics of the devices. Future work will compare wider, shorter electrodes with existing designs with square electrode. It is expected that capacitors with the new electrode geometry will have a lower equivalent series resistance (ESR) than existing devices with the same electrode area.

## V. FUTURE WORK

The next phase of work will include high frequency impedance analysis of the capacitors.

Further print runs will incorporate the fabrication of multilayer structures. It is believed that the new structures will offer improved electrical characteristics such as reduced ESR whilst increasing the capacitance density of the devices. It is also planned to produce a working circuit complete with a number of capacitors demonstrated in decoupling, and timing applications.

Evaluation of Solufill® green tape as a dielectric film material in CLF capacitors is underway. The tape, in its unfired state, is flexible and strong enough to be used in the Offset Lithographic printing process. The tape is an ultra-thin, free-standing film containing more than 90% w/w of ceramic powder. It is available with a number of different materials includungX7R, Y5V, and NPO class ceramics. The film supplied by DSM Solutech has been manufactured with a thickness of 11 microns and a K value of 14.5–16.9. The film has been calendered to reduce its porosity and will be coated on one side with a thin film of heat-activated copolymer adhesive to allow it to be bonded to other layers. By fabricating multilayer capacitors with the Solufill material, improved capacitance densities can be achieved. The results of this work will be published at a later date.

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