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Phase-Shifted Full-Bridge Zero Voltage Switching DC-DC Converter Design with MATLAB/Simulink Implementation

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ABSTRACT

Design of phase-shifted full bridge zero voltage switching DC-DC converter has been very challenging due to circuit parasitic effect on the system dynamics. This paper presents steady-state analysis and iterative approach for the systemic design of phase-shifted full bridge DC-DC converter with improved dynamic performance and satisfactory operational requirement in terms of zero-voltage switching range, operating switching frequency and switching resonance. A 3 kW DC-DC converter is designed using the iterative design approach and the system dynamics performance was investigated in the MATLAB/Simulink environment. The converter zero-voltage switching simulation results were satisfactory with 90% efficiency under full load condition.

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1. INTRODUCTION

Phase-shifted full-bridge (PS-FB) DC-DC converter is widely used in high power application due to the advantage of high power handling capability [1], [2]. The conventional full-bridge converter has issues of ringing effect, circulating current, high switching and conduction losses but easily eliminated by employing phase-shifted PWM switching control that allows FET device zero voltage switching (ZVS) [3]. The switching control operation ensures that the converter transformer is connected to the source or shorted for continuous circuit current flow thereby limiting current ringing that might result from transformer leakage inductance. Smooth operation and improved dynamic performance of PS-FB ZVS DC-DC converter require the right choice of component value due to nonlinear operating nature and interdependency of circuit elements. This makes the analytical design of PS-FB ZVS DC-DC converter quite different from other conventional PWM converters. The components are chosen to precision in order to ensure that the circuit parasitics like the transformer leakage inductance, FET device output capacitance and transformer turn ratio are used to the system advantage for improved system dynamics.

The phase-shifted full-bridge ZVS DC-DC converter design, analysis and implementation have been presented in several literatures [4]-[6]. Efforts are being made on efficient circuit design to address most of the prevailing challenges like the loss of ZVS under light load condition, high voltage spike at secondary output rectifier, duty cycle loss, high circulating current and electromagnetic interference. The proffered solutions are mostly based on circuit topology and control techniques modification [7]. Most of the recent proposed modify topologies require auxiliary components to increase the resonant inductance energy for wider ZVS. Addition of auxiliary component like magnetic inductor is presented in [8], transformer design modification in [9] and the addition of passive-active component like capacitors and diode in [10] for

extending the converter ZVS range. Adding auxiliary component has successfully extended PS-FB converter ZVS range but at the expense of voltage ringing and circulating current resulting in high conduction loss. The other trade-off among these solutions are cost and components part increase, increase size and weight, and the implementation complexity. To this effect, switching control scheme was proposed to reduce the switching losses under light load condition when ZVS is lost by the converter lagging leg. The popular control methods include pulse skip mode and a burst mode that mask some of the PWM periods as presented in [11], [12].

This paper presents a systemic approach based on an iterative method for designing PS-FB ZVS DC-DC converter to optimize converter circuit parasitic for achieving improved dynamic performance. A 3 kW 100 kHz high-frequency converter is designed and zero-voltage switching performance investigated in MATLAB/Simulink environment. The simulation results show that the system performed satisfactorily over the design load range with 90% full load efficiency.

2. STEADY-STATE ANALYSIS OF PS-FB ZVS DC-DC CONVERTER

Phase-shifted full bridge ZVS PWM converter is an isolated DC-DC converter with two power conversion stages; the primary DC-AC with a high-frequency isolation transformer and the AC-DC full-wave rectifier providing regulated DC output voltage. The PWM switching control signal offers the advantage of switching all the FET device with ZVS using the junction capacitance and transformer leakage inductance energy. The topology of a full bridge converter is presented in Figure 1 has a leading leg with pair switches S_1, S_2 turned on complimentarily with 50 % duty cycle minus short dead time and same for the lagging leg with switches S_3, S_4. The PWM gating switching control signal to the H-bridge inverter lagging leg is phase shifted with respect to the leading leg as presented in Figure 2.

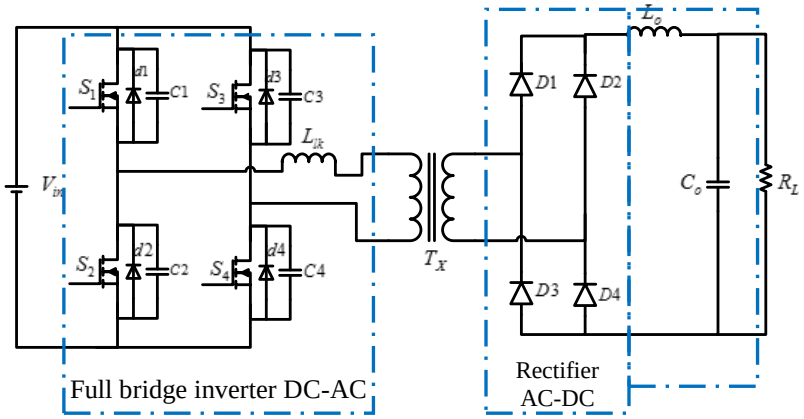


Figure 1. Full bridge DC-DC converter

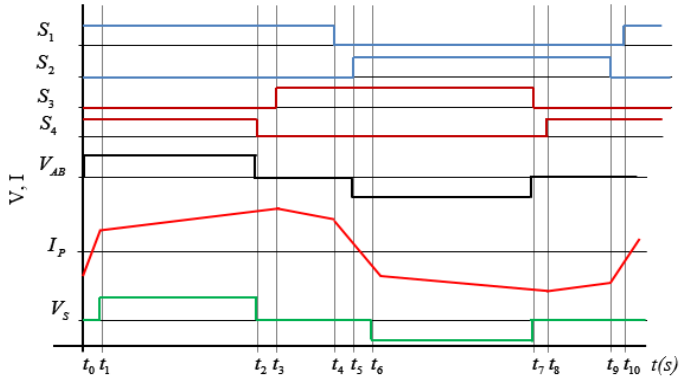


Figure 2. Basic waveform of PS-FB ZVS converter

The voltage gain of ZVS PWM phase-shifted full bridge converter is expressed as:

$$V_o = V_{in} \frac{N_s}{N_p} D_{eff} \quad (1)$$

The duty cycle available at the secondary side of the converter is lower than the primary due to finite slope in the rising and falling edges of the primary current as depicted in Figure 2. The current flow through the leakage inductance does not change instantaneously, the rising and falling edge of the primary current reduces the effective duty cycle available at the transformer secondary side by ΔD [4]. The primary duty cycle D set by the control circuit is given by:

$$D = D_{eff} + \Delta D \quad (2)$$

where, D_{eff} -is the effective duty cycle of transformer secondary voltage and ΔD is the duty cycle loss due to finite slope during rising and falling edges of the primary current.

In order to achieve H-bridge inverter ZVS during operation, the leakage inductance energy (E_L) must be equal or greater than the total capacitive energy of the FET output capacitance and that of the transformer capacitance (E_C). The zero-voltage switching in leading leg with pair switches S_1 and S_2 depends only on leakage inductance energy and the total inductive energy available for ZVS is given by (3):

$$E_{L-A} = E_{Llk} = \frac{1}{2} L_{lk} I_2^2 \quad (3)$$

In the case of legging leg with switches S_3 and S_4, the total energy available for ZVS comprised of transformer magnetizing inductance energy (E_{LM}), leakage inductance energy (E_{Llk}), and the reflected output inductance energy (E_{Lo}). The total inductive energy (E_L) available for ZVS is given by (4) [4]:

$$E_{L-B} = \frac{1}{2} L_M I_{M(pk)} + \frac{1}{2} L_{lk} I_2^2 + \frac{1}{2} L_o \left(\frac{N_p}{N_s} \right)^2 \left(I_{Lo(\max)} \frac{N_s}{N_p} \right)^2 \quad (4)$$

I_2 is the current in the primary when S_4 is in *off*-state and V_{in} is the input voltage, L_M and I_M are magnetizing inductance and current respectively.

The resonance of FET devices switching transition in each pair leg of the H-bridge inverter requires minimum dead time (t_d) to complete the zero-voltage switching transition. The dead-time allows the charging and discharging of the FET (MOSFETs) output capacitance depending on the resonant circuit parameters. The resonant frequency for achieving ZVS in all the four switches is similar and given in (5) [4].

$$f_r = \frac{1}{2\pi \sqrt{L_{lk} C_t}} \quad (5)$$

where, $C_t = 2C_{oss(tr)} + C_{Tx}$

To maintain ZVS, minimum dead time for switching commutation must meet the condition in (6).

$$t_d \geq \frac{\pi}{2} \sqrt{L_{lk} (2C_{oss(tr)} + C_{Tx})} \quad (6)$$

The lagging leg switches would easily achieve the ZVS throughout loading conditions because there is sufficient energy from leakage inductor and output filter inductor for switching. Leading leg ZVS only depend on the transformer leakage inductance energy based on reflected load current which may not be

sufficient under light load to achieve the ZVS. The critical current I_{crit} which is the minimum load current requires to maintain leading leg ZVS is given by (7) [13].

$$I_{crit} = \sqrt{\frac{2}{L_{lk}}\left(\frac{4}{3}C_{oss(tr)}V_{in}{}^2 + \frac{1}{2}C_{Tx}V_{in}{}^2\right)} \quad (7)$$

where C_{Tx} is transformer capacitance and $C_{oss(er)}$ is FET energy stored in the nonlinear drain to source output capacitance, while the ratio 4/3 is the 2 times the $C_{oss(tr)}$ energy. If assumed that the energy stored in the drain to source output capacitance of FET device is linear and the critical current is known, then the critical current I_{crit} can be re-expressed as:

$$I_{crit}{}^2 = \frac{2}{L_{lk}}\frac{1}{2}(2C_{oss(er)} + C_{Tx})V_{in}{}^2 \quad (8)$$

The required leakage inductance value for the ZVS range with critical current I_{crit} is:

$$L_{lk} = \frac{C_t V_{in}{}^2}{I_{crit}{}^2} \quad (9)$$

3. DESIGN AND SIMULINK MODEL OF PS-FB ZVS DC-DC CONVERTER

This section presents a summary of steps for designing PS-FB ZVS DC-DC converter with the iterative method and the MATLAB/Simulink implementation of a 3-kW converter as a case study.

3.1. PS-FB ZVS DC-DC converter design

The two main analytical methods for designing PS-FB ZVS DC-DC converter are the iterative and exhaustive search methods [4]. The PS-FB ZVS DC-DC converter iterative design method ensures that the circuit parameters such as transformer turn ratio, the leakage inductance, the switching frequency and maximum duty cycle are optimized after series of design iterations. The summary of the procedural steps involved in obtaining optimal circuit parameters for converter smooth operation are provided as follows [4].

a. The maximum duty cycle $D_{\max}$ is chosen to be as large as possible to maximize the transformer turn ratio N_p/N_s.
b. The transformer secondary voltage $V_{\sec}$ is chosen to be low such that the voltage stress on the secondary rectifier can be reduced and must satisfy the $V_{\sec} \geq \frac{V_{out}}{D_{\max}}$ condition.
c. The critical current I_{crt} that determines the ZVS range is then calculated.
d. The leakage inductance L_{lk} required for ZVS is calculated using the total switching device and transformer parasitics.
e. Lastly, the operating switching frequency f_s is checked with equation,

$$f_s = \frac{R_L(N_p/N_s)^2}{4L_{lk}}\left[\frac{D_{\max}}{D_{eff}} - 1\right] \quad (10)$$

In this work, a 3 kW rating PS-FB ZVS DC-DC converter is developed based on iterative design technique with ZVS range between 40 % load current to full load. The isolated transformer step-up the 48 V nominal supply to 400 V DC before the output rectification. The converter operates in continues conduction mode (CCM) and the output current ripple is designed for 1.5A. The regulated output voltage is suitable for the DC-AC conversion to a 230V AC to serve local load or grid connection.

The maximum duty $D_{\max}$ is chosen as 0.84 and a ferrite material with low saturation flux density was considered for the transformer magnetic core having a maximum magnetic flux B_{max} of 0.2 T (2000G) and core cross area A_C of 1.5 cm^2. The number of the primary side turns N_p is calculated using (11) and a 5-turn ratio is chosen for the primary turn (N_p). The converter operating supply voltage is between 36 V-60 V with

48 V nominal. The number of transformer secondary turns (N_s) is calculated by (12) using the minimum input voltage and 70-turns was obtained for the transformer secondary side [1], [14], [15].

$$N_p = \frac{V_{in(\min)} D_{\max}}{2B_{\max}(\mathrm{G})\,\mathrm{A}_c(\mathrm{cm})^2\, f_s(\mathrm{Hz})}.10^8 \quad (11)$$

$$N_s = N_p \frac{V_{\sec}}{V_{in(\min)}} \quad (12)$$

3.2. PS-FB ZVS DC-DC converter MATLAB/Simulink model

MATLAB/Simulink model of the PS-FB ZVS DC-DC converter is presented in Figure 3 showing the H-bridge inverter, high-frequency transformer, full wave rectifier and the output filter. The H-bridge inverter has pair MOSFETs on each leg for converting the DC supply voltage to a chopped AC that serves the high-frequency transformer. The switching frequency is 100-kHz to reduce the transformer size for high power density. The MOSFET block has inbuilt parasitic that exhibits switching characteristics closed to the real-FET device. The N-Channel SuperFET FCH043N60 MOSFET is selected with 730 pF effective output capacitance C_{oss}, 37 mΩ *on*-resistance ($R_{DS(on)}$) and all the parameters were configured within the Simulink.

The high-frequency transformer is configured for 1:14 turn ratio as obtained from the design and the full bridge rectifier converts the transformer secondary voltage to 400 V DC voltage before the LC-output filter stage. The load is modelled as resistor while the output inductor ripple current is specified as 20 % of load current and the obtained filter inductor is 466 µH. Also, output voltage ripple current is specified as 1 % of the output voltage and the output filter capacitor is 1.47 µF.

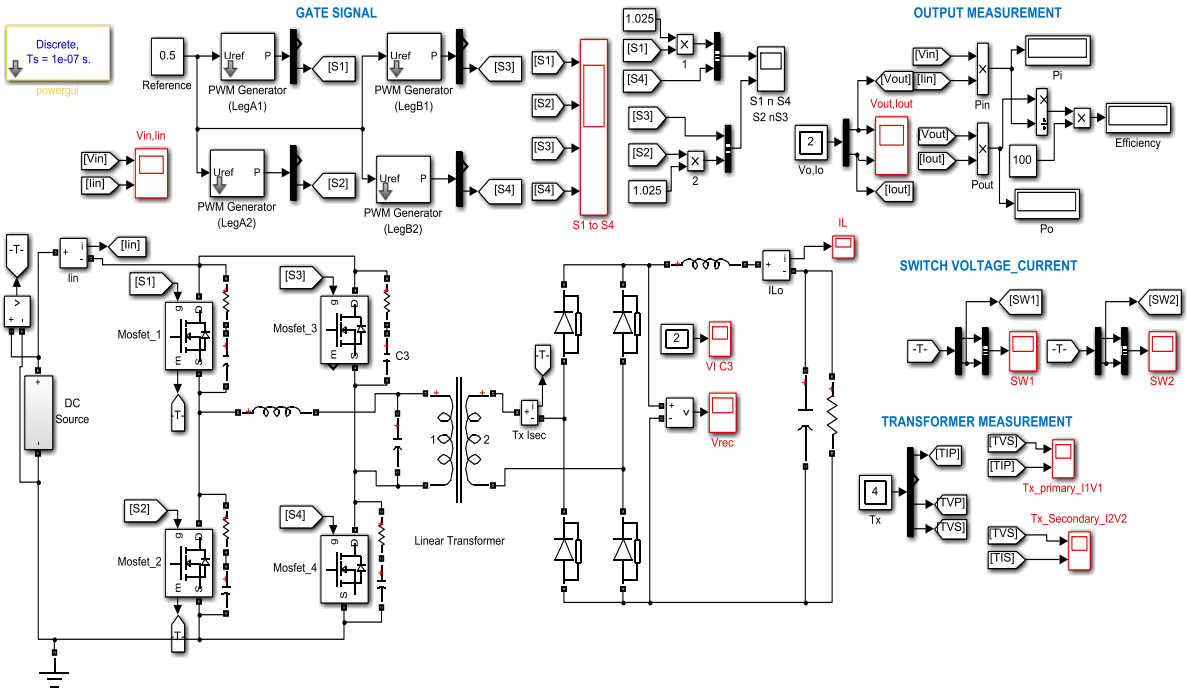


Figure 3. MATLAB/Simulink model of PS-FB ZVS DC-DC converter

4. RESULTS AND ANALYSIS

The PS-FB ZVS DC-DC converter design parameters and the system dynamic performance results for various loading conditions investigated in MATLAB/Simulink environment are presented in this section.

4.1. Converter parameters and DPWM Scheme

Three design iterations were carried out to obtain the converter optimized circuit parameter. The secondary voltage was first chosen as 500 V and the critical load current as 40 % (3 A) of the average full

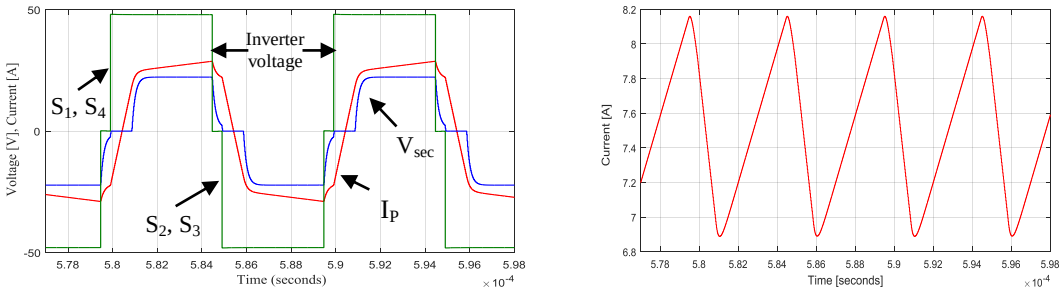
load current. The obtained switching frequency did not satisfy the operational requirement, and this was increased to 550 V and 600 V subsequently. The obtained switching frequency with 500 V, 550 V and 600 V secondary voltage are 35.259 kHz, 70.991 kHz and 97.134 kHz respectively with the latter satisfying the design requirement. The PWM inverter switching gating control signal was generated using a pair of *PWM generator block* as shown in Figure 3. The trailing edge carrier was employed and the phase shift angle between the carrier to each leg of the H-inverter legs under different load currents is presented in Table 1.

Table 1. PWM Carrier Signal Phase-angle

Load current (%)	Leading leg phase angle (º)		Lagging leg phase angle(º)		Phase shift (ϕ º)
	S_1	S_2	S_3	S_4	
100	90	270	285	105	15
80	90	270	293	113	23
60	90	270	302	122	32
40	90	270	305	125	35
15	90	270	315	135	45

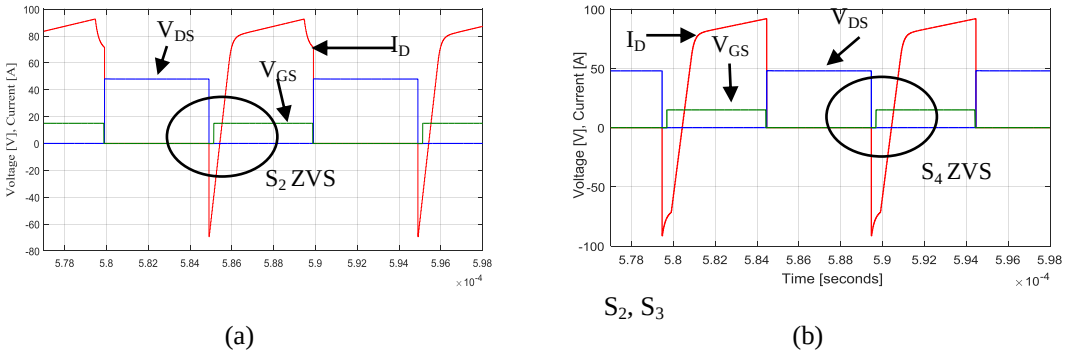
4.2. Full load current ZVS results (7.5 A)

The voltage and current waveform of the inverter, transformer primary and secondary voltage, and load current under full load condition are presented in Figures 4. The inverter voltage waveform switches between + 48 V and – 48 V with short dead time as observed in Figure 4(a). The transformer primary current (I_P) flows in positive direction to reach reflected output inductor current (nL_o) when diagonal switch S_1 and S_4 are in *on*-state condition and flows in the negative direction when diagonal switch S_2 and S_3 are in *on*-state to complete a switching cycle. The load current has a peak-to-peak current of 1.5 A as expected based on the designed ripple value and averaged load current of 7.5 A under full load test as shown in Figure 4(b).



(a) (b)

Figure 4. (a) Inverter voltage, primary current and secondary voltage (b) inductor load current



(a) (b)

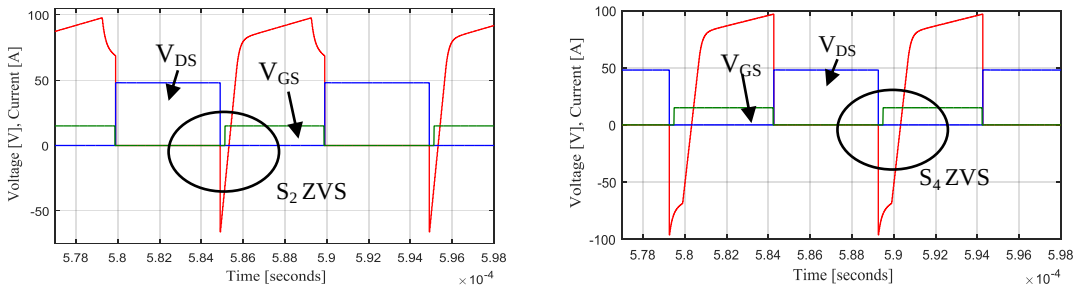
Figure 5. (a) Leading leg MOSFET S_2 and (b) lagging leg MOSFET S_4 Waveform (100%-load)

The switching waveforms for both leading leg switch S_2 and lagging leg switch S_4 under full load current are presented in Figures 5 showing the converter ZVS action. The drain-source voltage (V_{DS}) dropped to zero before the gate-source voltage (V_{GS}) starts rising with ZVS during the turn-*on* transition. The snubber capacitance (C_{GS}) completely discharged from 48 V to 0 V before the MOSFET body diode starts conducting with ZVS reducing the switching losses.

4.3. Converter ZVS results under 80%, 60%, and 40% load current

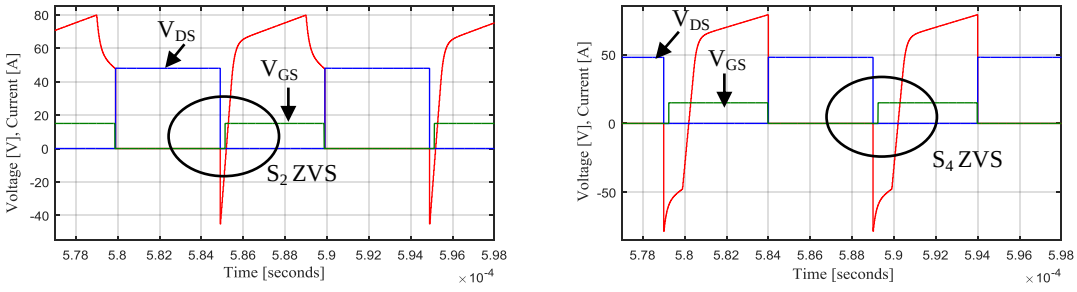
The PS-FB ZVS DC-DC test under 80%, 60%, and 40% load current show that the inverter voltage, transformer primary current and secondary voltage, and load current follows same switching wave pattern as presented in Figure 4. The only difference is the load current value, but ZVS was achieved with reduced switching losses delivering high conversion ratio and efficiency. The voltage and current switching waveform for the leading leg switch S_2 and lagging leg switch S_4 for 80% (6 A), 60% (4.5 A) and 40% (3 A) load currents are presented in Figure 6, Figure 7 and Figure 8 respectively showing the converter ZVS feature.

The V_{DS} dropped to zero before the V_{GS} starts rising with ZVS during the turn-*on* transition. The C_{GS} is completely discharge from 48 V to 0 V before the body diode of the MOSFET starts to conduct thereby ensuring ZVS with significant switching loss reduction. Both the leading leg switch S_2 and lagging switch S_4 conveniently achieved ZVS as presented in Figure 6, Figure 7 and Figure 8(a) and Figure 8(b). The converter was designed for 40% load current under which soft switching is maintained. Figure 8(a) shows the reduced primary current available for ZVS of lagging leg which is an indication that the ZVS will be lost if the load current is further reduced below the 3 A current and the switching losses will become significant.



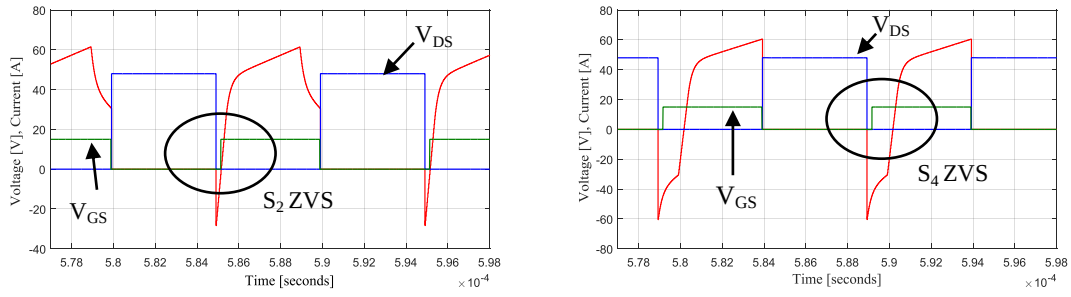
(a) (b)

Figure 6. (a) Leading leg MOSFET S_2 and (b) lagging leg MOSFET S_4 Waveform (80%-load)



(a) (b)

Figure 7. (a) Leading leg MOSFET S_2 and (b) lagging leg MOSFET S_4 Waveform (60%-load)



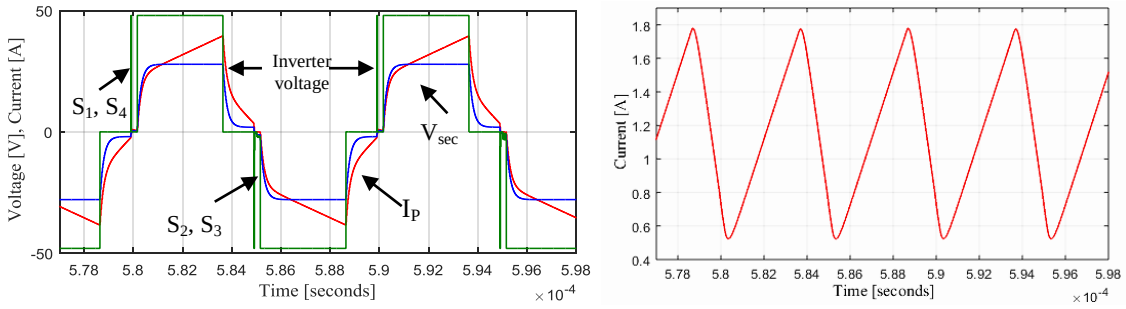
(a) (b)

Figure 8. (a) Leading leg MOSFET S_2 and (b) lagging leg MOSFET S_4 Waveform (40%-load)

4.4. Converter ZVS results under 15% load current

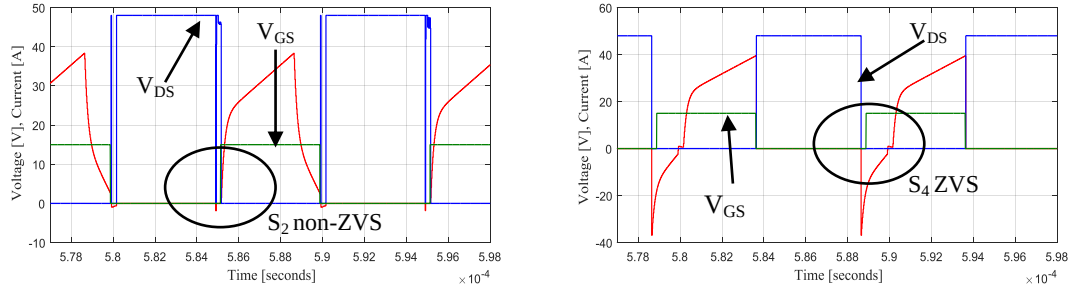
The PS-FB ZVS DC-DC converter load performance was investigated under 15% (1.125 A) load current which is below the 3 A critical load current of soft switching limit. In Figure 9(a), an oscillation or arbitrary switching was observed on the H-bride inverter voltage rising edge due to ZVS loss of the leading leg since the load current is below the critical load current. There are significant switching losses during the turn-on transition which deteriorate the system energy conversion ratio.

At 15% load current, the available energy for the leading leg MOSFET C_{GS} discharge is not sufficient to complete the resonance because the load current is less than critical current. The resonance operation ends when the inverter primary current decreased to zero as indicated in Figure 10(a) and the drain current I_D starts rising while V_{DS} decreases rapidly than it should under resonance transition. Figure 10(b) shows that the lagging leg maintains soft switching since there is sufficient energy from the leakage inductance, magnetizing inductance and reflected output inductance for the MOSFET ZVS.



(a) (b)

Figure 9. (a) Inverter voltage, primary current and secondary voltage (b) inductor load current



(a) (b)

Figure 10. (a) Leading leg MOSFET S_2 and (b) lagging leg MOSFET S_4 Waveform (15%-load)

The converter efficiency under different load conditions is presented in Figure 11. The measured input-output power under 15%, 40%, 60%, 80% and 100% load current are used to compute the system efficiency. The DC-DC converter efficiency between 40% to 100% load currents is almost linear for the soft switching region because the switching losses are minimal owing to ZVS. At rated load current, the PS-FB ZVS DC-DC converter attained 90 % efficiency which is satisfactory based on the designed consideration. At 15% load current, the efficiency drastically dropped due to significant switching loss because the load current is below the critical load current that could sustain leading leg ZVS.

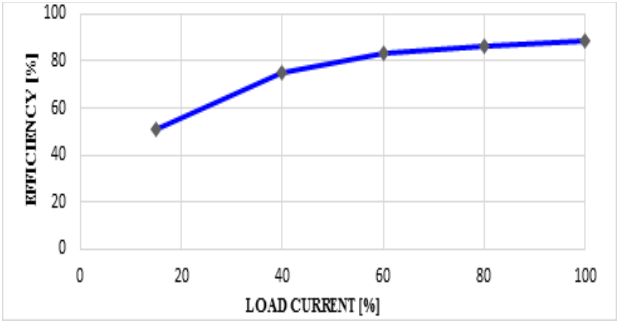


Figure 11. Efficiency against the load current

5. CONCLUSIONS

An iterative method for designing a PS-FB ZVS DC-DC converter has been presented in this paper and the steady-state analysis of the converter enumerated. A 3 kW rating phase-shifted full bridge zero voltage switch converter was designed and model in MATLAB/Simulink environment. The converter zero voltage switching was investigated over the design range and the operational waveforms including the inverter, transformer primary and secondary voltage-current, the load current, and the FET device switching waveforms performed satisfactorily. The system achieved 90% efficiency under full load condition.

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