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Active LC Clamp dv/dt Filter for Voltage Reflection due to Long Cable in Induction Motor Drives

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ABSTRACT

This paper presents an active LC clamped dv/dt filter to mitigate the over voltages appearing across the motor terminals. The over voltages at motor terminal is due to voltage reflection effect of long motor cable connected between high frequency PWM inverter having high dv/dt switching waveforms and ac motor drives. The voltage reflection due to fast switching transients can be reduced by increasing the rise time and fall time of inverter output voltage pulses. The most commonly available mitigating technique is a passive dv/dt filter between inverter and cable. Since, size, cost and losses of passive LC dv/dt filter is more, an active dv/dt filtering technique is used to reduce over voltage at motor terminals. Active LC clamp filtering technique used here consists of a small LC filter designed for a single motor cable length which can be used for any lengths of cable up to 1000m only by changing the active control of the PWM pulses to achieve the desired voltage slope during voltage transition period. The basic principle of active dv/dt filer used here is to charge and discharge the capacitor in the filter with modified PWM pulses to increase the rise time and fall time of output voltage pulses without any extra devices to handle the transient response of the LC filter. Detailed investigation is carried out by simulation using MATLAB-Simulink software with active control of common LC clamp dv/dt filter suitable for various cable lengths ranging from 100 m to 1000 m. Comparative analysis is done with active dv/dt filter designed with a common LC clamp filter and active LC clamp dv/dt filter designed for various cable lengths and also with diode clamped passive dv/dt filter. The results proves the effectiveness of the active common LC dv/dt filter to mitigate the over voltages at motor terminal for cable lengths up to 1000m.

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1. INTRODUCTION

Pulse width Modulated IGBT inverters are widely used in variable speed IMD. The high switching speeds of IGBT with short rise time and fall time leads to high dv/dt in the inverter output voltage pulses. In many industrial applications induction motor and inverter are placed at different locations and hence needs long cables to connect them. The high dv/dt of inverter output pulses with steep rise time through long cables results in voltage doubling at motor terminal due to voltage reflection phenomena [1]-[3]. The over voltages appearing across the motor terminal stresses the motor insulation and finally leads to motor insulation failure.

According to NEMA standard dv/dt of the pulses has to be limited to less than 500V/µs in 460V class of motors. The voltage reflection is dependent on rise time of inverter output pulses, the length of the cable used for interconnecting inverter and motor and surge impedance of motor and cable. If the propagation time is more than half of rise time, then voltage reflection at motor terminal occurs with peak voltage of twice the amplitude of input voltage [1].

The most commonly used mitigating technique for voltage doubling due to voltage reflection is a passive dv/dt filter between the inverter and cable [4]-[8]. The passive dv/dt filter consisting of inductor, capacitor and resistor will increase the rise time and reduce the dv/dt gradient of inverter output voltage pulse. But passive filters with damping resistors have drawback of large power loss. A diode clamped LC filter connected to the neutral of DC link voltage is the best option in terms of reliability and power losses [9]-[11]. But still large filter size, losses in the system and high cost are the draw backs of passive filters.

This paper employs active LC clamp filtering technique to mitigate over voltages at motor terminals by limiting dv/dt of inverter output pulses by increasing rise time of inverter output voltage pulses. This method is the joint effect of small passive LC diode clamped filter and active control of this LC filter by modified PWM pulses. The filter values are designed based on the required voltage transition time and the filter peak current and resonance frequency which is selected well above the switching frequency, hence the size of the inductor becomes small and the filter size is reduced. The required voltage rise time to avoid voltage reflection depends on the length of the cable. In active dv/dt diode clamped LC filter the active filtering is achieved by the combined effort of LC filter and its active control by charging and discharging the capacitor of filter to maintain the motor terminal voltage equal to dc link voltage. The main advantage of this method is small filter that reduces the size and cost of filter. The control of LC filter is done by altering PWM sequence which does not require any extra devices or hardware setup, hence simple, convenient and economical. Simulation is carried out in MATLAB- Simulink platform to validate the performance of the active dv/dt filter designed for various cable lengths with corresponding modified PWM pulses. To standardize the filter size a common filter is designed which is suitable for all the cable lengths ranging from 100m to 1000m and over voltage issue is reduced by only varying the software based switching times and correction pulse control of PWM. A performance comparison is carried out with both approaches and observed that the common filter is much smaller than the passive filter and is suitable for mitigating voltage reflection effect due to various cable lengths and effectiveness of active control is validated. A passive filter had been designed and validated the performance for cable lengths ranging from 100 m to 1000m and was reported in the previous work [10].

2. VOLTAGE REFLECTION THEORY

The IGBT inverter output voltage pulses with short rise time travels along the long cable to reach the motor terminals. These pulses acts like travelling waves through transmission line. The major causes of over voltages at motor terminal are fast rise time of inverter output voltage, length of cable and impedance mismatch between motor and cable characteristics.

The motor impedance is much higher than the characteristic impedance of cable and hence due to impedance mismatch the travelling wave reflects back. If the propagation time is more than half of rise time ($t_p > \frac{t_r}{2}$), the motor terminal voltage will shoot up to double the amplitude of input voltage [2],[12],[13] .Propagation time (t_p) is the time taken by the pulse to reach the other end of the cable. Rise time (t_r) is the time taken by the applied voltage to reach approximately 90% of the desired magnitude of voltage.

The amplitude of reflected voltage wave depends on voltage reflection co-efficient of motor (Γ_m) and is given by equation (1),

$$\Gamma_m = \frac{Z_m - Z_c}{Z_m + Z_c} \quad (1)$$

where,(Z_m) is motor characteristic impedance and (Z_c)is cable characteristic impedance. The peak motor terminal voltage (V_m) given by equation (2),

$$V_m = V_{DC} * (1 + \Gamma_m) \quad (2)$$

The reflection co-efficient (Γ_m) varies with the size of the motor and its value reduces as the size of motor increases. The literature reports that the reflection co-efficient value ranges between 0.65 to 0.95. Hence, over voltages appear at motor terminal due to voltage reflection phenomena. The over voltages can be minimized by increasing the rising and falling times of output voltage pulses.

3. DESIGN OF ACTIVE LC CLAMP DV/DT FILTER

3.1. Design of active LC clamp filter

The basic principle of operation of active dv/dt filter is to generate the required rising and falling voltage slopes by increasing the rise and fall times as shown in Figure 1. It is achieved by the selection of small LC filter and its active control by charging and discharging the filter capacitor to increase the rise time and fall time of the inverter output voltage. The charging and discharging timing sequence is controlled by modifying the PWM pulses. The inductor in the LC filter will limit the charging and discharging current of the inverter and hence control the filter peak current. The main advantage of active dv/dt is that the filter inductor value is very small because in active dv/dt filter, the output transient voltage slope depends only on the LC constant of the circuit. The filter values are designed based on the required rise time of the inverter output voltage and the filter peak current. The filter is designed at high resonant frequency to reduce the size of filter and the neutral of the filter is connected to the midpoint of DC link which helps to reduce the common mode voltages of IMD. Diode clamping is provided to clamp the oscillations of LC filter to the dc link value.

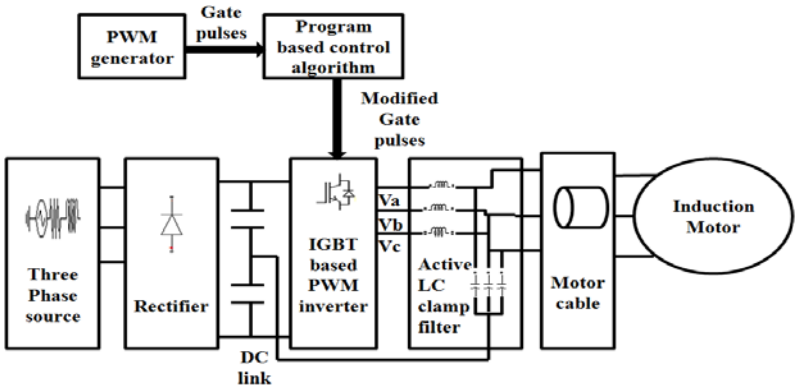

Figure 1. Active LC clamp dv/dt filter topology

Active LC clamp dv/dt filter component values are designed based on rise time of inverter output voltage (t_r). Propagation time increases as the length of the cable increases and is based on equation (3) [4],

$$t_p = \frac{l_c}{v_p} \tag{3}$$

where, l_c –cable length, v_p –propagating wave velocity.

The velocity of propagation of pulse through the cable is considered approximately half of the velocity of light. Rise time (t_r) of under damped second order system is given by equation (4) [14],

$$t_r = \frac{\pi - \tan^{-1}\sqrt{\left(\frac{1-\xi^2}{\xi}\right)}}{\omega_n\sqrt{(1-\xi^2)}} \tag{4}$$

where (ξ) - damping factor which is considered negligible. Hence, rise time

$$t_r = \frac{\pi}{\omega_n} \tag{5}$$

$$\omega_n = \frac{1}{\sqrt{(LC)}} \tag{6}$$

where ω_n is the undamped natural frequency.

The LC filter is designed at resonance frequency which is above the switching frequency that helps to reduce the size of filter. At resonance, energy stored in inductor is equal to energy stored in capacitor [15],

$$\frac{1}{2} * \left(L * I_{fpk}^2\right) = \frac{1}{2} * \left(C * V_{DC}^2\right) \tag{7}$$

$$I_{fpk} = \frac{V_{DC}}{Z_0} \text{ and } Z_0 = \sqrt{\frac{L}{C}}$$

where, I_{fpk} - filter peak current, V_{DC} - DC link voltage.

The filter component values are designed based on above equations. But for industry application designing customized filter for different cable lengths is not advisable. Hence, in this paper small LC filter is designed which can be used for cable lengths ranging from 100m to 1000m by active control of LC filter by appropriate selection of the modified PWM pulses.

From equation (3) to (7) common filter component values are designed as follows,

$$t_p = \frac{l_c}{v_p} = \frac{1000}{1500*10^6} = 6.7*10^{-6} \text{ sec}$$

To avoid voltage reflection phenomena rise time (t_r) of output voltage is selected above twice the wave propagation time.

Using equation (5)

ω_n = 179.18 rad/sec

Using equation (6)

$$LC = 31.14*10^{-12} \quad (8)$$

For filter peak current (I_{fpk}) of 7A and DC link voltage of (V_{DC}) of 565V using equation (7),

$$\frac{1}{2}*(L*7^2) = \frac{1}{2}*(C*565^2)$$

$$\left(\frac{L}{C}\right) = 6514 \quad (9)$$

The minimum inductor and capacitor values required for the active LC clamp dv/dt filter is obtained from equations (8) and (9) and filter inductor value is 450µH and capacitor value is 68.95nF.

3.2. Active control of LC clamp dv/dt filter

LC circuit designed with negligible damping gives oscillations when subjected to inverter output step voltages and the peak amplitude of oscillation goes double as that of step input value. The main objective in active dv/dt filter is to increase the rise time and fall time of inverter output voltage and hence the rate of change in output voltage is reduced during voltage transitions by effectively charging and discharging the filter capacitor. The charging and discharging of capacitor is achieved by modifying the PWM pulses. The step response of un-damped single phase LC filter circuit is given by equation (10),

$$V_{out}(t) = V_{DC}(1 - cos\omega_n t) \quad (10)$$

Inverter voltage pulses are fed to the LC filter for a period of time (t_1) during which the output voltage of the LC filter rises to half the dc- link voltage due to charging of capacitor. When the LC filter output voltage reaches half of dc-link voltage, stop feeding voltage to the LC filter. Keep the switches off for a period of time (t_2) during which capacitor discharges and discharging time period is same as charging time (t_1) . During this discharging time interval the capacitor voltage doubles because of oscillations due to resonance and at the end of discharging time period turn on the switches feeding inverter output voltages to maintain the inverter output voltage level to dc link voltage (V_{DC}). Now the total rise time of the output voltage pulse is increased to $2t_1$ and now no transients will occur as the LC circuit capacitor voltage is same as inverter output voltage. The motor terminal voltage peak will remain at dc link voltage level and no voltage reflection phenomena occur and hence mitigate the voltage doubling effect at motor terminal.

The capacitor charging current flowing through the inductor rises the inductor current which is carrying the load current during t_1 period and during t_2 interval inductor current decreases due to discharging capacitor current. If the current flowing through inductor during charging and discharging is failing to bring back the inductor current to original load current level, then output voltage oscillations can happen. To avoid this overshoot due to oscillations a current correction pulse is required along with charging and discharging timing sequence of PWM pulses. The switching instants are calculated as follows.

The pulse length (t_1) is the time period during which the filter capacitor voltage will reach half of the dc link voltage. The inverter switches are ON during this period and capacitor will get charged to half of the dc link voltage. Hence filter output voltage is given by equation (11),

$$V_{out}(t_1) = \frac{V_{DC}}{2} \quad (11)$$

The capacitor charging time interval is obtained from equation (12),

$$t_1 = \frac{\pi * \sqrt{(LC)}}{3} \quad (12)$$

The capacitor will discharge for a period of time (t_2) during which the output voltage will reach full dc link voltage.

The filter discharging time is same as the charging time (t_2=t_1)and during (t_2) intervel inverter voltage pulses are off.

$$t_2 = t_1 = \frac{\pi * \sqrt{(LC)}}{3} \quad (13)$$

Now the rise time of the output voltage is increased and the rise time is calculated using equation (14).

$$t_r = t_1 + t_2 = \frac{2 * \pi * \sqrt{(LC)}}{3} \quad (14)$$

3.3. Modification of PWM sequence for active control

To mitigate the voltage doubling effect in induction motor drive the rise time of inverter output voltage pulses can be increased by charging and discharging of filter capacitor by the modified PWM pulses. In a two level three phase inverter the upper switches of the inverter leg modulates the rising voltage slope of the corresponding phase and lower switches modulates the falling voltage slope. In active dv/dt filtering, edge modulation has to be done for the voltage step in addition to normal phase voltage modulation at the switching frequency. If load current and initial filter current are considered as zero then PWM modification can be done by providing modified delay pulses based on equations (12) and (13). The capacitor charges or discharges depending on the slope directions, when the filter voltage reached half the total voltage transition, the power switches are turned off and the inductor current goes through the freewheeling diodes of opposite switches. The absolute current decrease at the same rate as it was increased and output voltage of filter continues to increase or decrease depending on the direction of voltage. Then the same power switch is switched on when the current has returned to the same value as it was before the transient and the voltage has reached dc link value.

The above method is good only if the load current and initial filter current is zero. But it is observed that this method has issues when the load current exists. The increase or decrease in load current causes oscillations in output voltage in proportion to the ratio of load current to filter current. Hence the load current creates an error in active dv/dt control explained above. Considering single leg of inverter as shown in Figure 2, during active dv/dt control when the voltage of capacitor reaches half of the dc link voltage, power switches will go off and the filter current will freewheel through the anti-parallel diode of the opposite switch and the current begins to decrease as shown in Figure 3(a)-(d) if the load current is zero. But if load current exists, then depending on the instantaneous values and direction of load current, a current correction pulse is required to bring the load current to its original value. This issue due to load current can overcome by incorporating a current correction pulse along with the PWM pulse modification explained above as shown in Figure 3.

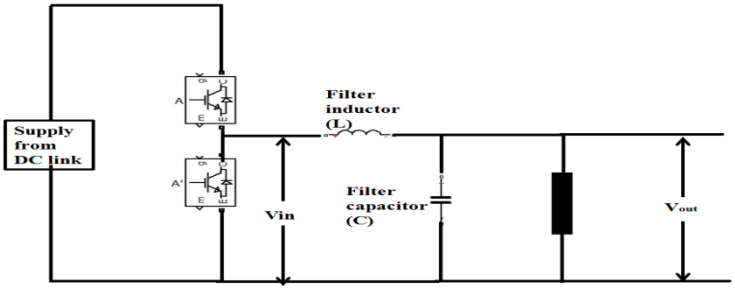

Figure 2. Single leg of the inverter

Case 1a: Rising voltage slope and load current positive

If the load current is positive, the rising voltage slope is not affected and the filter operates normally during freewheeling mode. Only modified PWM pulses are required and no current correction pulses are required. The inductor current is as shown in Figure 3(h) and the PWM pulses to switch A and A' is shown in Figure 3(a)&(b).

Case1b: Falling voltage slope and load current positive

If the load current is positive, the falling voltage slope gets affected because during freewheeling mode the current will not return to the same value as in the beginning of edge modulation Figure 3(h). To bring the inductance current back to initial positive value the switch parallel to the conducting diode needs to be turned on. i.e. upper switch (A) has to be turned on. The appropriate correction pulses to turn on upper switch (A) along with modified PWM pulse sequence is shown in Figure 3(i).

Case 2a: Falling voltage slope and load current negative

If the load current is negative, the falling voltage slope is not affected and the filter operates normally during freewheeling mode. Only modified PWM pulses are required and no current correction pulses are required. The inductor current is as shown in Figure 3(e) and the PWM pulses to switch A and A' is shown in Figure 3(a)&(b).

Case 2b: Rising voltage slope and load current negative

If the load current is negative, the rising voltage slope gets affected because during freewheeling mode the current will not return to the same negative value as in the beginning of edge modulation Figure 3(e). To bring the inductance current back to initial value the switch parallel to the conducting diode needs to be turned on. i.e. lower switch (A') has to be turned on. The appropriate correction pulses to turn on lower switch (A') along with modified PWM pulse sequence is shown in Figure 3(g).

The length of the current correction pulse when load current is between zero and filter peak current can be obtained from equation (15)

$$t_{add} = (\sqrt{LC}) * sin^{-1}(\frac{I_L}{V_{DC}} * \sqrt{\frac{L}{C}}) \quad (15)$$

where I_1 is the instantaneous value of load current. But when load current is greater than filter peak current the current correction pulse width will be half of charging period.

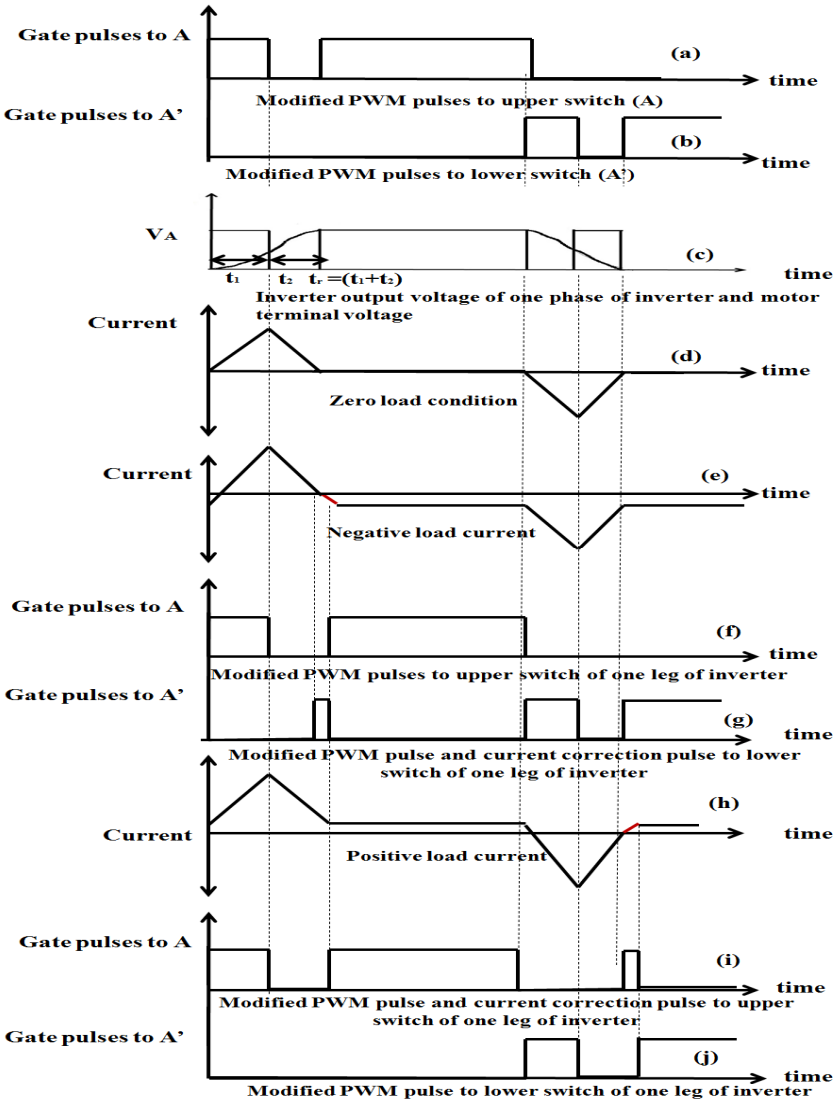

Figure 3. Active dv/dt operation with modified PWM pulses and current correction pulses for one leg of inverter

The algorithm for generation of active dv/dt control with current correction pulses for one leg of inverter is given in Figure 4.

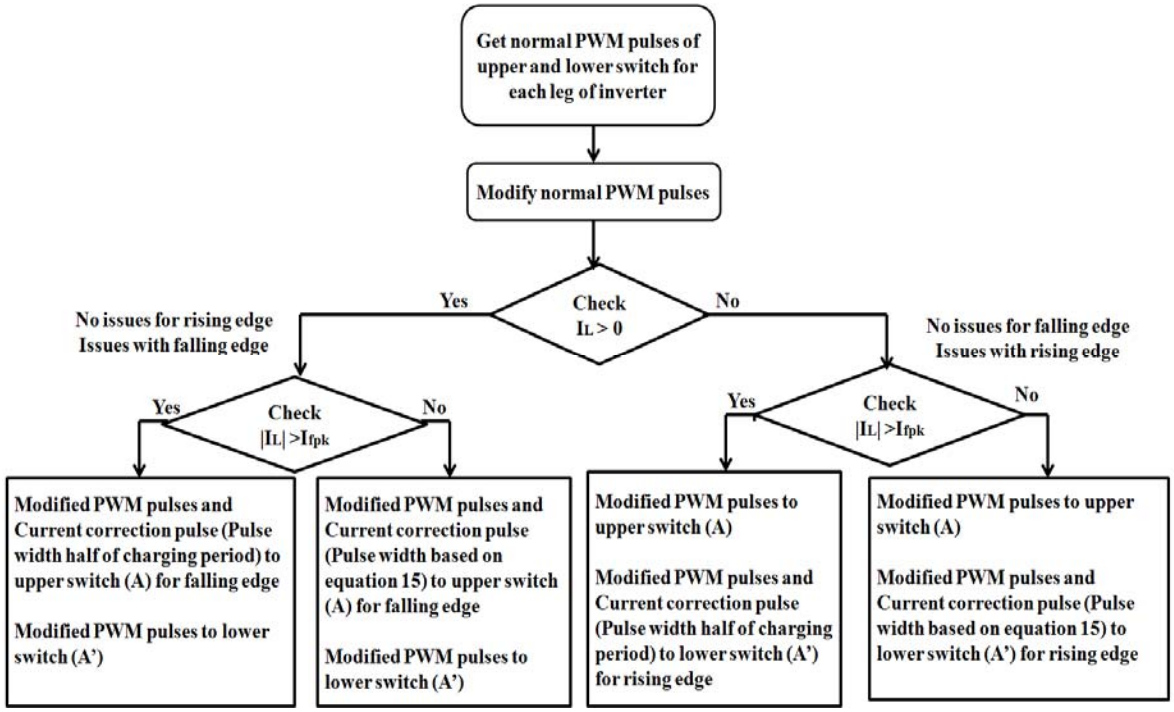

Figure 4. Algorithm for implementation of current correction pulse along with modified PWM pulse sequence for one leg of inverter

Step 1: Normal PWM pulses for upper switch (A) and lower switch (A') for each single leg of inverter is generated by comparing sinusoidal signal with triangular waveform.
Step 2: These normal PWM pulses are modified based on filter capacitor charging and discharging time sequence (t_{ch}, t_{dch}).
Step 3: If load current is positive for rising edge then modified PWM pulses are only required and no need of current correction pulse. But if the load current is negative for rising edge then current correction pulse is required along with PWM modified pulses to lower switch (A') to bring the load current to its original value i.e. to bring inductor current to load current level. Similarly for falling voltage slope if the load current is negative, only modified PWM pulses are required and no correction pulse is required. And if the load current is positive for falling edge then correction pulse along with modified PWM pulse is required to upper switch (A) to bring inductor current to load current level.
Step 4: The width of current correction pulse depends on ratio of load current to filter peak current. If load current (I_L) is less than filter peak current value(I_{fpk}), width of the correction pulse(t_{add}) is calculated as per equation 15. And if load current is greater than filter peak current, width of correction pulse is half of charging period.

4. RESULT AND ANALYSIS

Simulation is carried out in MATLAB-Simulink software to analyze the voltage reflection due to long cable in a 4kW induction motor drive. The cable is modeled based on distributed transmission line model and the cable characteristics required for modeling is selected from Belden cable data sheet of cable part number 29502 multi conductor 1000V UL flexible motor supply cable. The motor parameters and cable parameters are given in Table I and II. Simulation is carried out in induction motor drive with cable model and observed the high voltage at motor terminal side due to voltage reflection phenomena. In the previous part of this work a passive LC diode clamped filter is designed and analyzed its effectiveness by simulation for various cable lengths ranging from 100m to 1000m and reported [10]. In this paper active LC clamped filter is investigated to mitigate the over voltage at motor terminal and to reduce the filter size and hence the cost and losses in the system.

The main advantage of this technique is that the high voltage at motor terminal can be limited to the desired safe limit with active dv/dt filter where the size of filter can be reduced to a great extent by active dv/dt control of the filter without any extra devices or hardware requirement. The rise time of the input

voltage to the motor is increased by the combined effect of small LC filter and the modified PWM pulses with calculated switching times and current correction pulses.

Detailed investigation is carried out to mitigate the voltage reflection effect at motor terminal with LC clamped filter designed for various cable lengths with its active control by modified PWM pulses. To standardize the filter size, a common filter suitable for cable length up to 1000m and its active control by the modified PWM pulses depending on the corresponding length is designed and simulated to validate its performance.

A comparative analysis of performance without filter, with passive LC diode clamped dv/dt filter, active LC diode clamped dv/dt filter for various cable lengths ranging from 100m to 1000m and a common diode clamped LC dv/dt filter with its active control depending on length of cable is given in Table III. The plots showing the above analysis for 100m and 1000m cable are shown in Figure 5 and Figure 6.

Table 1. Motor Specifications

Rated Speed	Rated Torque	Number of poles	Voltage
1430 rpm	26.7 Nm	4	400 V

Table 2. Cable Specifications

Characteristic impedance	80 Ω
Inductance	0.698853 (μH/m)
Capacitance	137.802 (pF/m)
Resistance	8.26812Ω

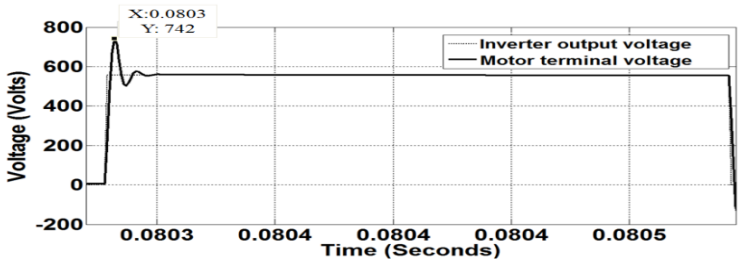

Figure 5a. Simulation result of inverter output voltage and motor terminal voltage for 100m cable length without filter

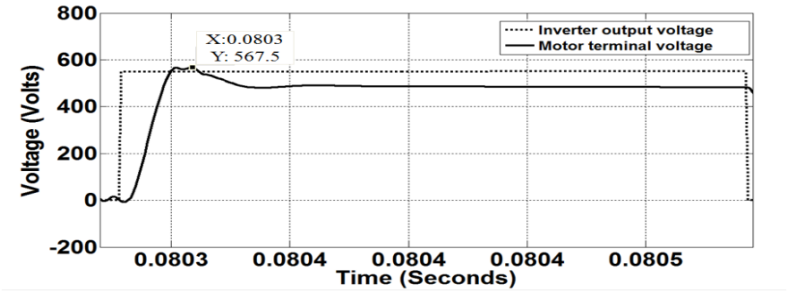

Figure 5b. Simulation result of inverter output voltage and motor terminal voltage for 100m cable length with passive LC clamped dv/dt filter

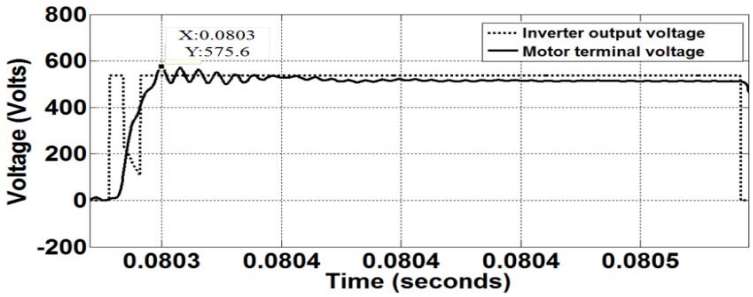

Figure 5c. Simulation result of inverter output voltage and motor terminal voltage for 100m cable length with active LC clamped dv/dt filter

Figure 5(a),(b),(c) shows the line to line voltages of inverter output voltage and motor terminal voltage for a cable length of 100m without filter, with passive dv/dt filter and with active dv/dt filter. The peak value of inverter output voltage is 565V where as the motor terminal voltage is increased to 742V due to voltage reflection due to 100m cable. A passive filter with inductor and capacitor values of 1.8mH and 7.743nF reduced this overvoltage at motor terminal from 742V to 568V. But in active LC clamped dv/dt filter with inductor and capacitor values of 450µH and 68.95nF, the overvoltage at motor terminal is reduced from 742V to 575V. By using active LC dv/dt filter the filter inductor size is reduced to 1/4th as that required for passive filter and it helps to reduce the over voltage in limit and over voltage appearing across motor terminal is only 1.8% with respect to rated value.

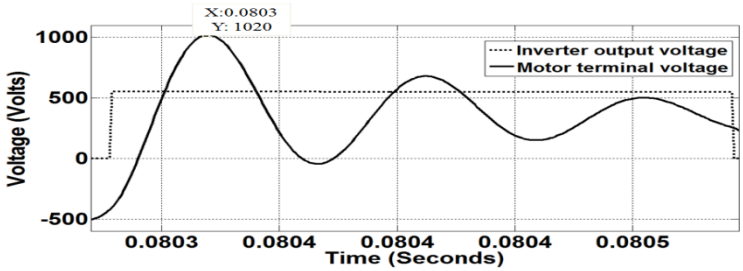

Figure 6a. Simulation result of inverter output voltage and motor terminal voltage for 1000m cable length without filter

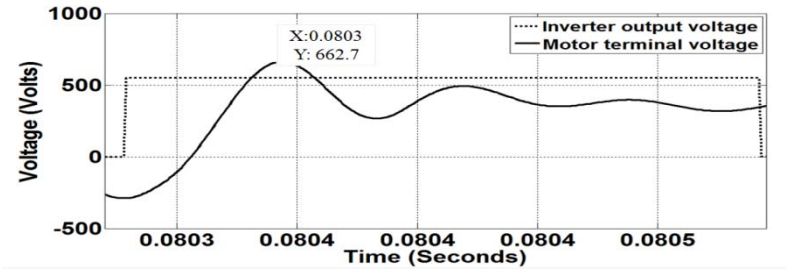

Figure 6b. Simulation result of inverter output voltage and motor terminal voltage for 1000m cable length with passive LC clamped dv/dt filter

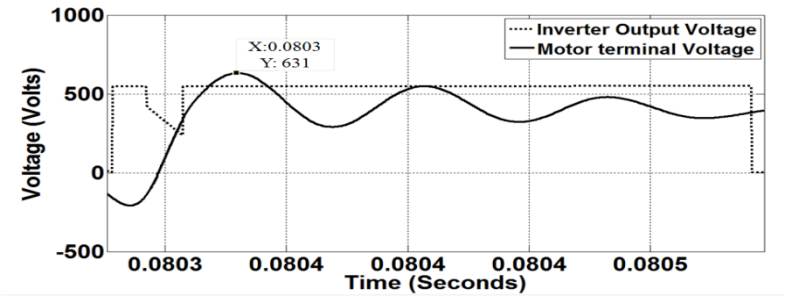

Figure 6c. Simulation result of inverter output voltage and motor terminal voltage for 1000m cable length with active LC clamped dv/dt filter

Figure 6(a),(b),(c) shows the line to line voltages of inverter output voltage and motor terminal voltage for a cable length of 1000m without filter, with passive dv/dt filter and with active dv/dt filter. The peak value of inverter output voltage is 565V where as the motor terminal voltage is increased to 1020V due to voltage reflection. A passive filter with inductor and capacitor values of 1.8mH and 7.743nF reduced this overvoltage at motor terminal from 1020V to 663V. But in active LC clamped dv/dt filter with inductor and capacitor values of 450µH and 68.95nF and the overvoltage at motor terminal is reduced from 1020V to 631V. The size of inductor used in active dv/dt filter is l/4th as that required for passive filter and it reduces the over voltage appearing across motor terminal to less than 10% with respect to rated value.

A comparative analysis for motor terminal voltage in a 4kW induction motor drive with cable model, with cable model and a passive filter, with cable model and active dv/dt filter is given in Table III. The results shows that the over voltages across motor terminal increases up to 81% with various cable lengths ranging from 100m to 1000m. A passive filter with 1.8mH and 7.743nF reduces the over voltages within 15% and and by using active filters with different active LC filters depending on length of cable and a common filter with active control to increase the rise time is observed that it is limiting the over voltages within 15%. This analysis proves the effectiveness of a active dv/dt filter with a small common filter and by active control of its modified PWM pulses is mitigating the voltage reflection phenomena occurring when IMD are interconnected with inverter using long motor cables. Figure 7 shows the comparative graph with motor terminal voltage along Y-axis and length of cable along X-axis. Figure 8 and Figure 9 are the common mode voltage without filter and with active LC clamp filter respectively and it shows that common mode voltage in IMD is improved with active filter.

Table 3. Comparitve analysis of motor terminal voltage

Cable length (m)	Without filter		Passive filter (L-1.8mH, 7.743nF)		Active LC clamp dv/dt filter designed for various cable length		Active LC clamp dv/dt filter designed for all cable length (L-450µH, 68.95nF)	
	Motor terminal voltage (Volts)	Percentage overvoltage above rated voltage (%)	Motor terminal voltage (Volts)	Percentage overvoltage above rated voltage (%)	Motor terminal voltage (Volts)	Percentage overvoltage above rated voltage (%)	Motor terminal voltage (Volts)	Percentage of overvoltage above rated voltage (%)
100	742	31%	568	1%	591	5%	575	2%
200	865	53%	576	2%	630	12%	570	1%
300	885	57%	589	4%	618	9%	600	6%
400	873	55%	598	6%	555	2%	591	5%
500	997	76%	636	13%	570	1%	576	2%
600	884	56%	633	12%	593	5%	592	5%
700	672	19%	648	15%	713	26%	648	15%
800	686	21%	656	16%	670	19%	655	16%
900	825	46%	658	16%	625	11%	637	13%
1000	1020	81%	663	17%	631	12%	631	12%

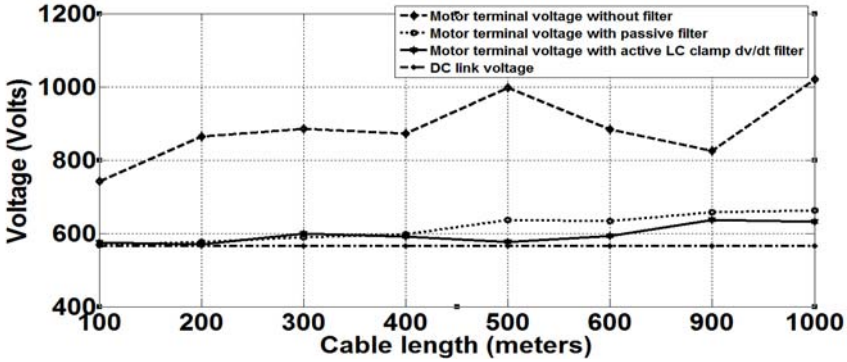

Figure 7. Comparison of motor terminal voltage without filter, with passive filter and with common active LC clamp dv/dt filter

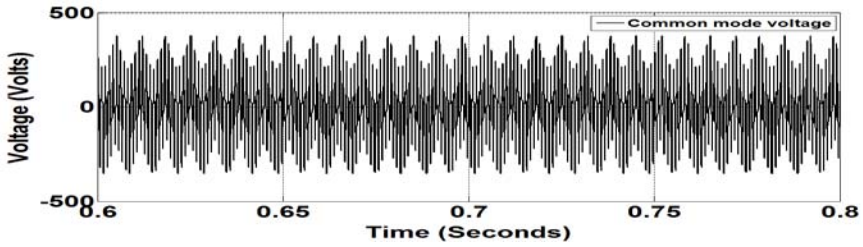

Figure 8. Simulation result of common mode voltage without filter

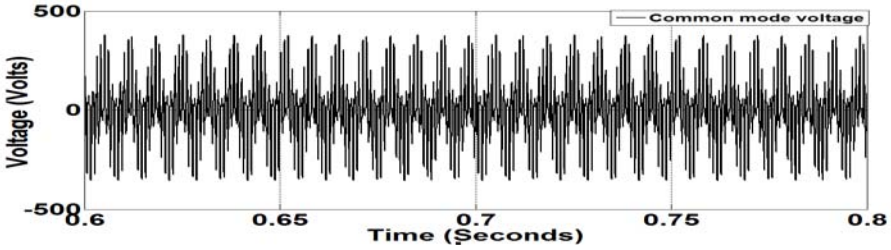

Figure 9. Simulation result of common mode voltage with active LC clamp dv/dt filter

5. CONCLUSION

Simulation is carried out in MATLAB-Simulink software to validate the performance of the active dv/dt filter with a 4kW Induction motor drive. The design of LC filter and the technique used to modify the PWM pulse pattern considering the effect of load current for active control of filter to mitigate voltage doubling effect is presented in this paper.

Simulation is performed with active dv/dt filters whose LC filters are designed based on its corresponding length of cables and its active control algorithm to reduce the over voltages at motor terminal. The results shows satisfactory performance. Instead of using different filters designed based on the length of cables, a common LC dv/dt filter is designed and its active control by modified PWM pulses based on the length of cable is validated by simulation. The results obtained with common LC filter with active control corresponding to length of cable are satisfactory. Thus the results proves that active dv/dt filter can be used with a common filter and the software based active control algorithm can be used to modify the PWM pulses depending on the length of cables.

A comparative analysis of results obtained using passive filter, active dv/dt filter whose LC values are designed based on various cable lengths and common active dv/dt filter suitable for various cable lengths is carried out. The results shows that the over voltages can be limited within 15% with a common active dv/dt filter whose filter inductor size is reduced to 1/4th as that with passive filter. The common LC dv/dt filter with programmable active control of PWM pulses based on the length of cable is a promising solution to mitigate the over voltage issues well within limit at motor terminal.

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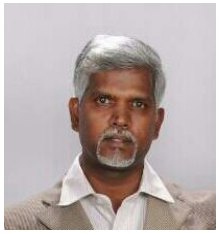

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