Energy-Efficient Start-up Dickson Charge Pump for Batteryless Biomedical Implant Devices

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***Abstract*— This paper presents a power management concept for solar energy harvesting power management using an on-chip switched-capacitor (SC) DC-DC converter for biomedical implantable applications. This design eliminates potential reversion losses caused by the switching scheme. It also mitigates the bottom plate loss by employing the charge recycling technique. Moreover, instead of using a single step clock pulse, the two-step adiabatic charge sharing clock helps reduce the energy drawn from the PV cell by 65%. Furthermore, with the help of clock disabler scheme, the power dissipation has been further reduced by disabling the entire start-up charge pump once the desired reference output voltage was reached. However, due to additional circuitry for the clock disabler, there is a trade-off between power efficiency and power dissipation. The proposed system was implemented and fabricated in a standard 0.18-µm TSMC RF CMOS technology. The proposed converter has achieved a maximum efficiency of 73%.**

Keywords*— *Implantable electronics, Switched Capacitor, Dickson's charge pump, DC-DC converter, Solar power.

I. INTRODUCTION

The amount of useful power that can be scavenged from energy harvesters is strongly dependant on external environmental or human body conditions [1].This can be particularly challenging for implantable biomedical applications that require a constant voltage and current to its electronics components. Consequently, to ensure that power is reliably supplied to an implantable integrated circuits and systems from an unreliable input power source, an effective power management unit or DC-DC converter is required [2,3].

The first integrated switch-capacitor (SC) based DC-DC voltage step-up converter was proposed by Dickson [4]. Later, different versions of the Dickson charge-pump have been demonstrated [5]. Although the Dickson charge pumps has a fast transient responses in comparison to the other charge pumps, they suffer from poor current efficiency. However, there is a scope for improving the Dickson's charge pump topology by mitigating different loss components such as shoot-through current loss, conduction loss and switching loss, which primarily contribute to the power efficiency. The desire solar energy harvested start-up charge pump aim to bridge between the low voltage PV harvested energy into the secondary storage source capacitor. This will then further power the main converter is shown in Fig.1(a). Moreover, the design trade-off of SC converter discussed in [6] and the contribution of this proposed design is depicted in Fig.1(b).

The objective of this design is to achieve a start-up charge pump for the power management system that operates with low input power supplied from a typical crystalline silicon PV cell that is implanted under the skin. The harvested energy from the PV cell is first power managed through an ultra-low-power step up start-up charge pump to convert low input voltage to the meaningful voltage. This is operated with on-chip self-oscillating clock generators [4] and non-overlapped clocks to control the charge sharing clock (CSC) and the charge transfer switches (CTS) of the start-up converter.

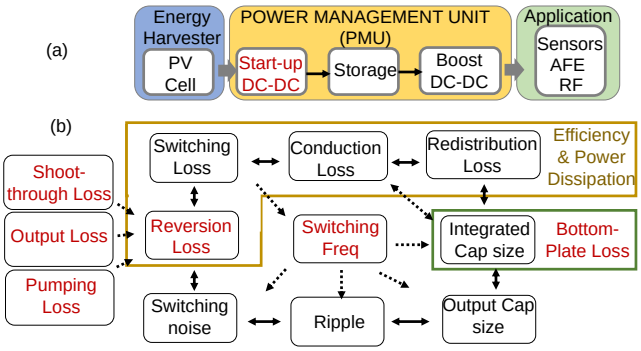

Fig. 1. Illustrating use of (a) start-up charge pump in PMU. (b) SC design trade-off diagram and our contribution highlighted in red.

Proposed clocking scheme operates well with the charge pump and the clock disabler to prevent constant power drawing from the PV cell. Second, the energy output of the start-up charge pump can be stored in a reservoir, ,i.e., a capacitor.

II. PROPOSED CHARGE PUMP DESIGN

A. Design challenges and contributions

In the step-up conversion of the Dickson charge pump, the voltage boosting of voltage goes from left to right across the n-stage charge pumps and the voltage increases at each pumping node.

Challenge and Contribution 1: *Eliminate reverse charge sharing dynamic loss.*

Reverse current paths from the output to the input direction results in output voltage loss and subsequently produce negative contribution in overall power efficiency. Several reverse charge sharing path schemes are discussed in [6,8]. Three types of reversion losses can occur, shown in Fig.2(a). These are (1) **Output loss** that occurs when M2 is accidently ON during the charging process of the charge pump capacitor C and current from load capacitor leaks towards the charge pump instead of sourcing to the load resistor, (2) **pumping loss** occurs when M1 unexpectedly turns on and charge share backward from pumping capacitor towards the supply source, and (3) **shoot-through current loss** or **short circuit loss** happen when both M1 and M2 are ON at the same time, and short circuit the output to input directly.

The two-phase clock-controlled method is typically used, provided that the gate control signals of the CTS are in the diode connection; the gate and the drain of the transistors are connected together, or CTS are bootstrapped by the charge pump's next stage [9]. Let's assume that the standard non-overlapping two phase clocks are used for CSC (CLK1, CLK2) and CTS as illustrated in Fig.2(a, c). For simplicity the

example was given for 2-stages charge pump with NMOS CTS and three arbitrary clock periods (1/2/3) are taken to investigate the operation of the charge pump. When clock signal of Fig.2(b) was applied to the CTC and boosting CSC, as shown in Fig.2(a) in period 2 shoot-through current loss and in period 3, pumping loss occurs.

In the literature [10], a six-phase clock control scheme was proposed to control the crossed-coupled charge pump. In this proposed charge pump, adaption of the original work [10] was utilised and the four-phase clock scheme, shown in Fig.2(c) was used to control the Dickson charge pump converter Moreover, the charge pump design in [10] was designed to operate at 1.8 V input source, whereas this proposed design is for low-voltage solar harvested input source and thus the clock generators are able to work at ultra-low voltages.

A similar investigation can be repeated by employing the proposed clock scheme depicted in Fig.2(c) into the simple Dickson charge pump circuit in Fig.2(a). It was observed that the reversion loss was eliminated at in all three periods.

Challenge and Contribution 2: *Charge recycling to reduce bottom plate parasitic loss.*

The dynamic power loss correlated to the bottom plate parasitic is another major cause for low power efficiency. The charge recycling or charge sharing between bottom layer and substrate parasitic has been studied in [11,12] to minimise the loss.

As illustrated in Fig.2(d), when any of the pumping capacitor was charged, the corresponding bottom parasitic capacitors are also charged to the same magnitude and stored some energy. This process can be considered as the bottom-plate loss during charge sharing. As suggested in Fig.2(d), when the two parasitic capacitors are connected during the operation soft-charging/discharging time (Δt), before the next operation begin, the charged parasitic capacitor (CB1) from the adjacent stage was pre-charged to the neighbour stage parasitic capacitor (CB2) connected across the switch. Therefore, in the next operation when the (C2) was charged to VDD. Thanks to the pre-charged charge recycling action the corresponding parasitic capacitance (CB2) only vary between pre-charged voltage to VDD, instead of a whole amplitude from VDD to the ground as shown in 2(d).

Challenge and Contribution 3: Two-step adiabatic CSC enable charge recycling as well as reduce power dissipation.

Two-step adiabatic (CSC) high impedance capacitive driver was presented in [13,10]. Thanks to the tristate driver two-step charging-discharging was possible. This produces CSC non-overlapped period signal (Δt). According to [10], in contrary to one-step charging the energy dissipation from the source was reduce to three quarter

$$E_{PV} = \frac{3}{4} Q.V_{PV} \quad (1)$$

Challenge and Contribution 4: Automatic clock disabler to reduces the energy dissipation.

The constant power consumption across the start-up charge pump system can change into dynamic consumption if the start-up operation switches to idle mode once the desire voltage is achieved at the storage capacitor. By introducing the clock disabler buffer at the output of the start-up charge pump, which will monitor and examine whether the output voltage threshold is reached to a pre-determined voltage required by the main converter. In previous studies the clock disabler charge pump design is proposed in [14] and integrated into this proposed charge pump design. The output of the clock disabler was linked with the aforementioned clock generators to act as the enable signal for the whole start-up operation and prevent constant energy dissipation from the source.

B. *Proposed control scheme and charge pump*

In the 180nm TSMC RF, native threshold transistor is also available but it is limited only to the NMOS. Upon availability of native threshold transistor for both MOSFET pair in other technologies, the ultra-low input voltage of lower than 450mV can be configured. The proposed start-up design clock control scheme based on the literature [10] is implemented which was designed to prevent the any potential reverse charging for crossed-couple charge pump circuit and operates at 1.8V. The proposed design in Fig.3 uses standard transistors and general purpose transistors are appropriately used to ensure that the charge pump and the clock generators circuits are functional at low input voltage sources. The transistor seizes are chosen through parametric sweep to ensure that the optimal ratio of theirs widths and lengths are set to guarantee the highest VCR and power efficiency.

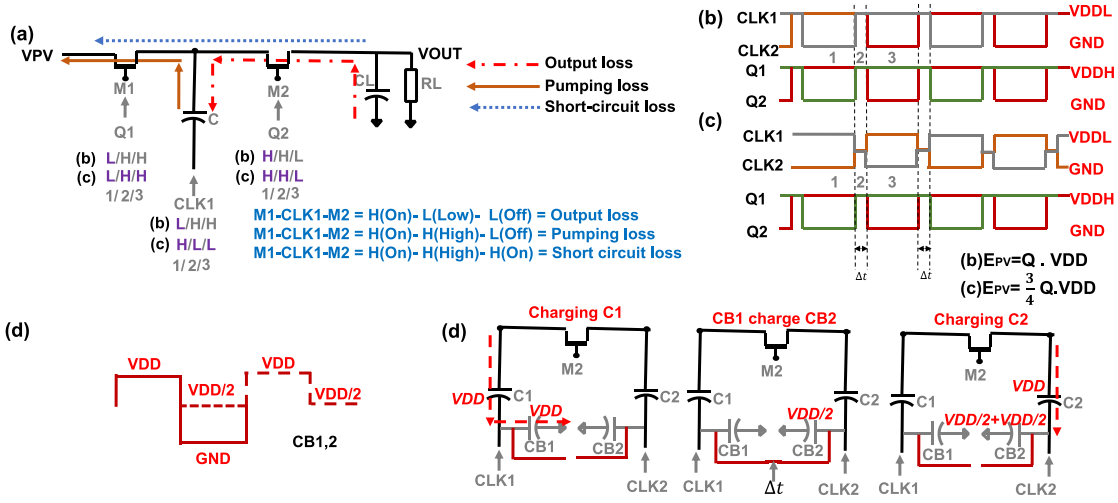

Fig. 2. (a) Problem and challenges of potential reverse charge sharing losses in Dickson's charge pump with (b) standard non-overlapping control clocks (c) proposed controlled signals and (d) explanation of why charge recycled technique can reduce the bottom plate parasitic loss.

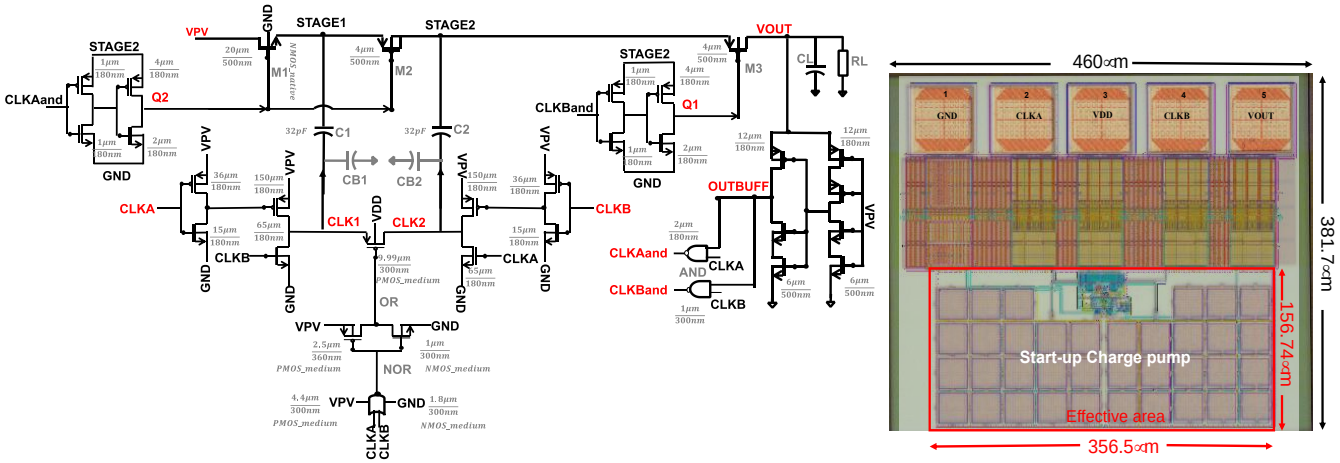

Fig. 3. Proposed circuit implementation of energy saving clock disabler and charge recycled two-step adiabatic CSC controlled charge pump and chip microphotograph (with back annotated layout).

Two charge transfer clock CLK1 and CLK2, which are used primarily for the boosting process are connected to the bottom plate of the top and bottom capacitors respectively. This was implemented through the charge recycling technique as shown in Fig.3.9(a), to ensure that during the transition dead time. Δt, when the two pumping capacitors remain idle, two bottom plates of the both capacitors are connected in parallel by the switch. This switch ON signal was triggered by the OR gate signal configured from CLKA and CLKB. This was due to the fact that when either of pumping capacitor are charged, their correspondent bottom parasitic capacitors are also charged to same magnitude and store some energy. This process can be considered as the bottom plate loss during charge sharing.

By introducing charge sharing in the process, this loss can be minimised. This was done by simply connecting two bottom plate capacitors across the switch and turning it on during the main charge sharing process are in idle state- i.e., Δt time. Therefore, during this period, since the two parasitic capacitors are also intertwined in two different phases, one charged parasitic capacitor share some stored energy to its counterpart capacitor. As a result, when the pumping capacitor charging action was resumed, due to its pre-charged action to parasitic capacitor, charging the discharged parasitic capacitor in the following cycle was minimised and the energy consumption of the associated clock driver was reduced to half.

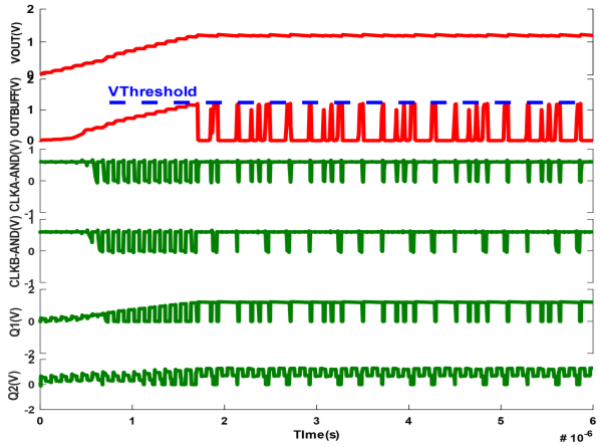

Fig. 4. Demonstrate Output voltage remain stable even when there is working operation of the clock disabler controlled by Outbuff signal.

To reduce the layout complexity and the area consumption, we did not use the deep n-well transistors, fully isolated NMOS does not suffer from the body effect when its bulk is connected to a different potential than ground. As a trade-off, in generating the Q1 and Q2 clock signals, high/low amplitude of the clock Q1 and Q2 has varies between VDDH to GND rather than VDDH to VDD. The implementation is shown in Fig.3.9(b).

The output of two-phase clocks was ANDed together with 'Outbuff' to test whether the start-up charge pump has reached to the desired output voltage. Therefore 'Outbuff' can be regarded as an enable of the 'AND' operation, for which the threshold of the output voltage was set by setting the threshold of the buffer which act as the feedback connected to the output of the start-up's output. As a result, once the threshold of the feedback buffer was aligned with the desired start-up output, the output buffer was low, and the whole 'AND' operation was disabled. When the clock was disabled, the whole start-up operation is deactivated to save energy consumption.

III. POST LAYOUT SIMULATION

This work was implemented in a standard 0.18 µm TSMC RF CMOS technology. The integrated capacitor of 2×20 pF and the output capacitor of 100 pF was used. The 8.8 MHz switching frequency was used for the operation and each pulse was transformed into two step adiabatic.

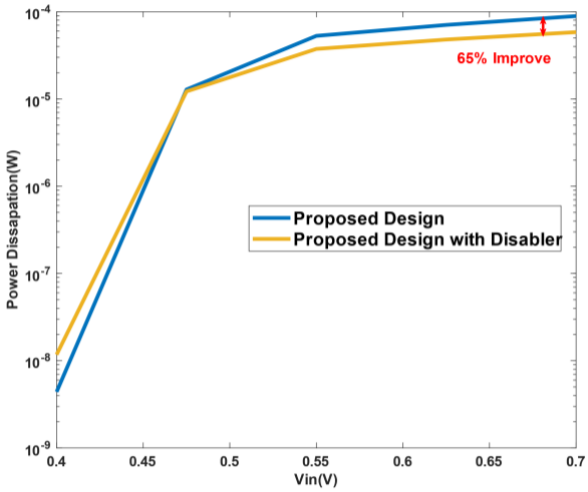

Fig. 5. Load regulation of the proposed charge pump sweeping from 1k-1MΩ.

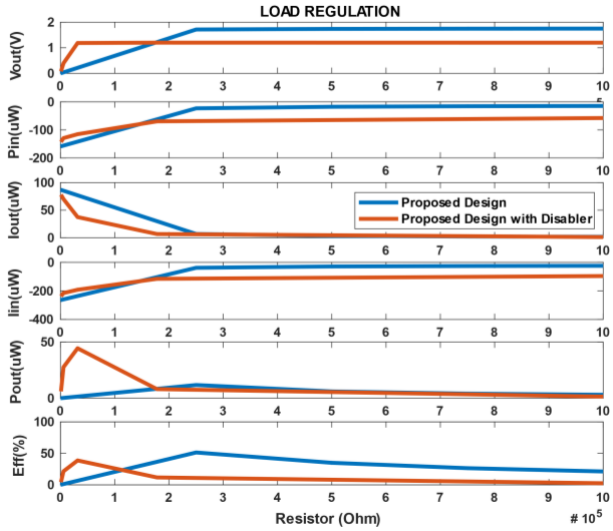

Fig. 6. Load regulation of the proposed charge pump sweeping from 1k-1MΩ.

The Fig.4 demonstrates the operation of the proposed charge pump charge pump with clock disabler scheme where once the output voltage reached to the desire 1 V, the OUTBUFF goes to the idle mode resulting in disabled control clock signals disable and hence stopped charge pump.

The load regulation was tested with a sweeping range of 1 kΩ to 1 MΩ in Fig. 6. As the input voltage increases the Vout also increases. The output power has achieved up to 44.4 µW and 51% end-to-end maximum power efficiency. However, when the clock disabler was added, the efficiency dropped significantly to 38.6%. The energy dissipation; output voltage square overload resistance value ratio, was considered in Fig.5. It demonstrates that the proposed design with the clock disabler design has 65% improvement in energy dissipation. This was due to power loss being dynamic loss from operation control clock disable the converter operation without interrupting the stable Vout as shown in Fig.4.

The line regulation of the converter was demonstrated in Fig.7. This was tested with the optimum load inherit from Fig.6 result to observe the change of the output voltage versus the change of input voltage (between 0.4-0.8 V) to imitate the solar cell open circuit voltages in different lighting conditions. It is noted that the output voltage has achieved up to 1.67 V at 0.7 V input voltage which is within the input voltage range sweep. The output power has achieved up to 89 µW at 73% efficiency. With a clock disabler the efficiency has dropped to 46% with the trade-off of improvement in power dissipation.

V. Conclusion

Thanks to the effective design of a control clock scheme, the reversion losses were prevented resulting in a highly efficient low-powered charge pump converter is accessible to bridge between the solar energy source and the main converter. As it was shown, there is a trade-off between the efficiency and energy dissipation in using the clock disabler circuit.

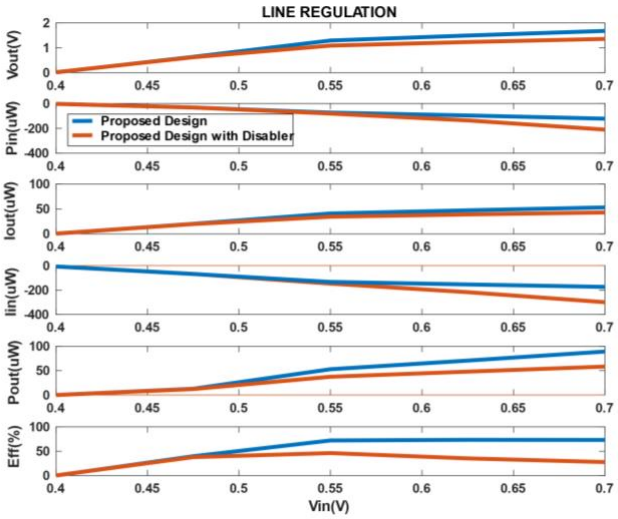

Fig. 7. Line regulation of the proposed charge pump (Yellow) in comparison with proposed charge pump with clock disabler (Red).

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