A Low Noise CMOS Sensor Frontend for a TMR-based Biosensing Platform

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***Abstract*—In this paper, we propose a low noise CMOS frontend for a Point-of-Care (PoC) biosensing platform based on tunnel magnetoresistance (TMR) as sensors. The integration of a low noise and low power integrated circuit (IC) with the TMR sensors reduces power consumption compared to a realization with discrete electronics and, thereby, paves the way towards a portable diagnostic system. The proposed chip uses a DC-coupled fully differential difference amplifier (FDDA) to amplify the minute signals generated by magnetic nanotags (MNTs) that will be used as biomarkers in the target biosensing application. The FDDA features a gain of around 60 dB with a suitable offset calibration scheme to deal with the large DC offsets caused by TMR and/or magnetic field mismatch. The ability to deal with varying DC fields is crucial for a portable setup that is intended to be used in unshielded environments outside the lab. The offset cancellation is achieved by two on-chip current steering DACs that can accommodate TMR resistances between 535 Ω and 4.7 kΩ. The presented chip is manufactured in a 180 nm SOI CMOS technology and features a thermal noise floor of 7 nV/$\sqrt{\text{Hz}}$. It consumes a total of 7.7 mA from a 1.8 V supply.**

I. Introduction

The increasing demand for early disease detection with point of care (PoC) devices has led to strong research efforts in this field. Here, ELISA (Enzyme-linked immunosorbent assay) is currently the gold standard for performing immunoassays and has been investigated since discovered in 1971 [1]. ELISA relies on a highly specific and strong binding between the biomarkers and antibodies. Consequently,In this way, ELISA is capable of detecting and quantifying a large number of different biomarkes with high specificity. However, ELISA also suffers from relatively long incubation timesof a few hours that are needed to achieve the required strong binding conditions. As an alternative to ELISA, biosensing using magnetoresistive (MR) sensors has been gained increasing attention over the past ten to fifteen year. Here, MR-based sensing shows great promise for improving the limit of detection (LoD) beyond that of ELISA. [2]. In this scheme, magnetic nanotags (MNTs) are used as labels to detect a specific biomarker. The different binding process in combination with the improved LoD leads to significantly reduced measurement times of a few minutes compared to several hours that are required for ELISA. Moreover, the MR-based approach is largely immune against background noise due to the intrinsic nonmagnetic nature of the sample, while ELISA suffers from background noise originating from sample autofluorescence. Finally, the MR-based sensing platform can easily integrate multiplexing schemes for an increased throughput without the need for bulky plate readers. While, in principle, any magnetic sensor can be used for magnetic biosensing, most published work focused on the use of giant magnetoresistive (GMR) sensors [3]–[6] due to their good sensitivity [7] and high integration density [3], [4]. More recently, TMR sensors have attracted increasing attention owing to their even better sensitivity, which, however, comes at the expense of an increased 1/f noise floor and a large MR ratio [8]. As it has been shown in [9], the 1/f noise problem can be solved by connecting a large number of TMRs in series. The high MR ratio of TMRs leads to a large susceptibility of the TMR resistance with environmental conditions, which has to be addressed on the system level by an appropriate readout scheme. As a potential solution to this problem, we propose a low-noise custom readout ASIC, which can accommodate large fluctuations and offsets in the TMR sensor.

II. Chip Description

The chip architecture is shown together with a micrograph of the manufactured ASIC in Fig. 1. Any offset generated due to e.g. undesired external magnetic fields or temperature drifts is continuously monitored by the proposed DC-coupled readout scheme. The voltage readout topology is favored to a current readout using a transimpedance amplifier since current biasing results in a spectrally purer output compared to voltage biasing, cf. [10]. This is because the TMR's resistance changes more linear in response to a given magnetic field change than its conductance [4]. The biasing of the TMR and the reference sensor is implemented with chip-integrated current sources. One of the current sources is implemented as an 11 bit binary-weighted DAC to provide a first-order compensation of any offset in the frontend electronics and between the sensor and its reference. A second 5-bit DAC is connected to the output of the first voltage amplification stage. This DAC, therefore, has reduced noise requirements and cancels any residual offset. The first voltage gain stage is realized as a fully-differential difference amplifier (FDDA) with a gain of 50. The FDDA is chosen over a classic three-opamp instrumentation amplifier (IA) due to its improved power efficiency, still providing the required high input impedance [11]. The FDDA is followed by a second gain stage with a gain of 20, which also provides

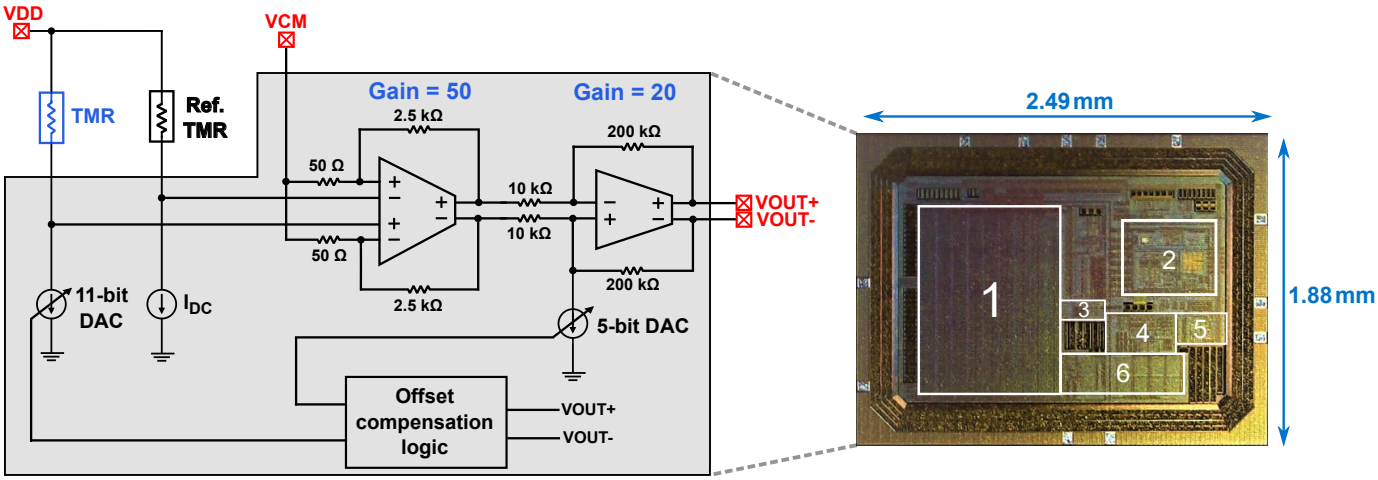

Fig. 1: Overall block diagram of the readout chip and micrograph of the manufactured IC. In the micrograph, (1) is the 11-bit DAC, (2) is the FDDA, (3) is the digital control circuity, (4) is the 5-bit DAC, (5) is the second gain stage, and (6) is the biasing of the reference resistor.

the required driving strength for the following off-chip signal conditioning electronics.

A. Amplifier implementation

Fig. 2 shows detailed schematics of the FDDA. The FDDA is implemented as a compensated Miller OTA with a voltage output stage to drive the resistive feedback. The input stage uses a current reuse scheme to increase the transconductance for a given bias current, and, thereby, the power efficiency for a given speed and noise requirement. [12]. The input differential pairs are designed with a large area to reduce their 1/f noise contribution. Their aspect ratio is chosen for an operation in weak inversion to maximize the $g_\mathrm{m}/I_\mathrm{d}$ ratios of the individual transistors. Finally, the voltage buffer is implemented as a common source stage with MOS diode loads.

B. Sensor biasing

To implement a voltage readout for optimum linearity, the TMR sensors are biased with low-noise current sources. An 11-bit current-mode binary-weighted DAC is used to compensate for any DC offset, e. g. due to mismatch between sensor and reference element, while introducing minimum noise into the system. The noise of the current-mode DAC is critical in this design since it is directly added to the input of the sensor system. The current noise power spectral density (PSD) of a MOS transistor can be modeled as:

$$S_{\Delta I^2_\mathrm{nD}} = 4kT\gamma g_\mathrm{m} + \frac{\mathrm{KF}\cdot g_\mathrm{m}^2}{C^\mathrm{n}_\mathrm{ox}\cdot W\cdot L\cdot f}, \qquad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, γ is the thermal noise excess factor, and g_m is the transconductance of the transistor. We minimized both thermal and flicker noise by choosing an operating point deeply in strong inversion, where the transistor's $g_\mathrm{m}/I_\mathrm{d}$ is minimum. Additionally, we have minimized the second term in eq. 1, the contribution due to the devices flicker noise, by proper device sizing, using sufficiently large devices. Overall, to satisfy both the thermal and the Flicker noise requirements, we used DAC unit elements with an aspect ratio of 850 nm/80 μm.

III. Electrical Characterization

The presented chip has been electrically tested and characterised using a custom-designed evaluation platform, which includes the TMR sensor presented in [9] with a nominal resistance of 830 Ω and a sensitivity of 93 Ω/mT for a biasing current of 1.1 mA. The sensor has dimensions of 6 mm x 4 mm and consists of 1102 TMR sensors connected in series to lower the 1/f noise corner frequency. The sensor is mounted on the PCB using an interposer board. The reference resistance is implemented using an ohmic resistor of nominally equal value. Magnetic fields in the sensitive direction of the TMR sensor are generated using custom-designed Helmholtz coils wound around a 3D-printed holder.

To characterize the fabricated chip, we have measured the input-referred noise and the frequency response of the overall system. The corresponding results are shown in Fig. 3. The measured 1/f corner frequency is 7 kHz. The input-referred thermal noise floor of the entire system consisting of the TMR sensor, biased by the ASIC, and the readout electronics is 9.5 nV/$\sqrt{\mathrm{Hz}}$ which corresponds to a limit of detection of 0.3 nT/$\sqrt{\mathrm{Hz}}$. From the total system noise, we extrapolated an input-referred noise of the ASIC (biasing and readout) of 7 nV/$\sqrt{\mathrm{Hz}}$. The measured AC gain in the passband is 60 dB. The measured 3 dB bandwidth is 500 kHz with a small peaking around 200 kHz. This peaking can easily be compensated in the digital domain. This bandwidth is sufficient to bring the TMR signal outside the 1/f noise region by field modulation [4]. Moreover, we have evaluated the spurious-free dynamic range (SFDR) of the presented chip by applying test signals of different amplitudes to the input. Fig. 4 shows the output spectrum for an input voltage signal with amplitude of 1.35 $\mathrm{mV_{pp}}$ and a frequency of 5 kHz. The measured SFDR is 64 dB.

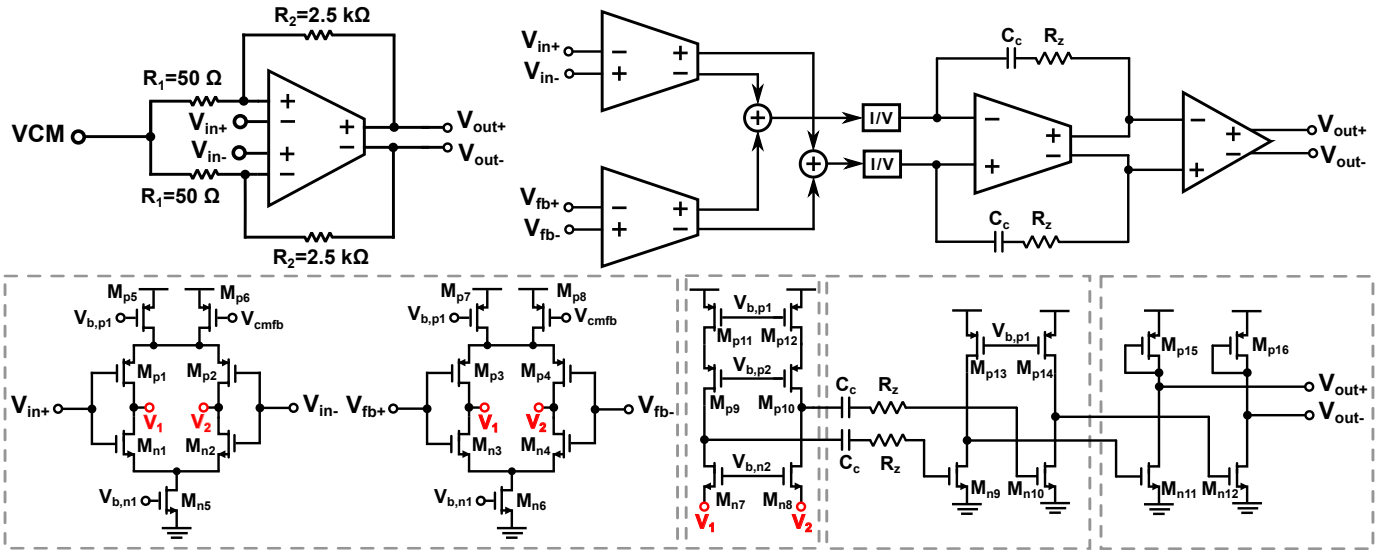

Fig. 2: Block diagram of the implemented FDDA and transistor-level schematics of the building blocks.

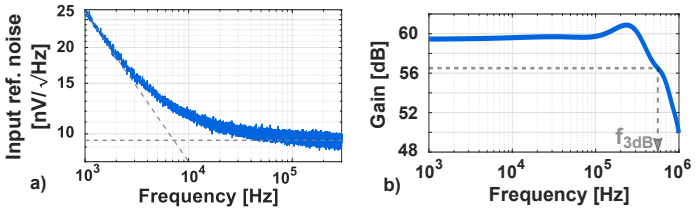

Fig. 3: a) Measured input-referred voltage noise of the biosensing platform. b) Measured AC response of the IC.

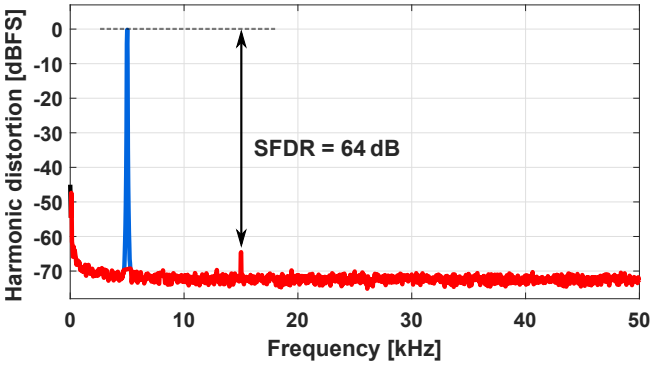

Fig. 4: Measured chip output distortion for a test signal with an amplitude of 1.35 mV_{pp} and a frequency of 5 kHz.

One important feature of the implemented design is its capability to bias largely different sensor resistances. In order to demonstrate this capability, we replaced the TMR by a potentiometer and used a fixed reference resistance of 1 kΩ at the second chip input. Fig. 5 depicts the output voltage offset of the chip for different input resistances after applying the automatic, on-chip offset calibration routine, cf. Fig. 1. According to the figure, the chip can successfully calibrate resistances between 535 Ω and 4.8 kΩ, making the chip compatible with the large process variations of TMRs. Finally,

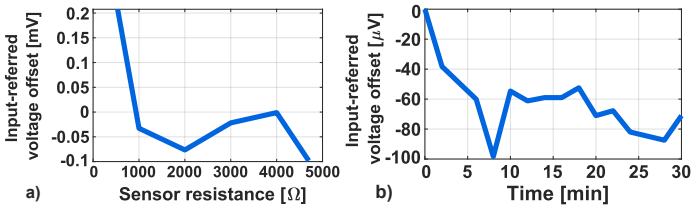

Fig. 5: a) Input-referred voltage offset of the chip for different offsets between sensing and reference resistors. b) Time stability of the input-referred voltage offset.

we also investigated the stability of the chip over time. This is important to ensure that the system is sufficiently stable to avoid calibrations during biosensing measurements, which can take up to several minutes. According to Fig. 5, the chip operates in a stable fashion for at least 30 minutes, which is sufficient for all practical measurement conditions. Here, it is worth mentioning that these experiments have been carried out without any shielding.

IV. Conclusion

In this paper, we have proposed a readout chip for a TMR-based biosensing platform. The chip incorporates coarse and fine low noise current-mode binary weighted DACs to bias the TMR sensor while being able to accommodate the TMR's large MR ratio. The IC provides a total gain of 60 dB, which is sufficient to overcome any noise contribution of subsequent signal conditioning stages. With its small form factor, versatile biasing circuitry, and low-noise performance, the presented frontend ASIC can pave the way towards TMR-based biosensing platforms for high-performance PoC disease detection systems.

Acknowledgment

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