Multi-Sample Differential Protection Scheme in DC Microgrids

Chunpeng Li, *Member, IEEE,* Puran Rakhra, Patrick Norman, Graeme Burt, *Member, IEEE,* Paul Clarkson

Abstract

This paper proposes a novel solution to the issue of protection instability caused by time synchronization error in high-speed differential protection schemes for DC microgrids. DC microgrids provide a more efficient platform to integrate fast-growing renewable energy sources, energy storage systems, and electronic loads. However, the integration of distributed generators (DG) may result in variable fault current magnitude and direction during fault conditions, potentially causing mis-coordination of conventional time graded overcurrent relays. One identified solution to this issue utilizes high-speed differential protection schemes to maintain effective selectivity in DG-dominated DC microgrids. However, as DC short-circuit fault currents are highly transient, microseconds of synchronization error in the measured line currents may cause protection stability issues, whereby mal-operation of relays may occur as a result of faults external to the protected zone. This paper investigates the impact of time synchronization errors for high-speed differential protection in DC distribution systems. It then proposes a multi-sample differential (MSD) scheme that performs multiple differential comparisons over a sampling window to ensure the stability of high-speed differential protection schemes for external faults whilst maintaining sensitivity to internal faults.

Index Terms

DC microgrid protection, Time Synchronization

I. Introduction

The successful deployment of HVDC transmission networks has re-stimulated research and development of MVDC and LVDC distribution systems that provide an efficient platform for the growing power electronic applications industry [1]. Technologies enabled by power electronic interfaces, such as renewable energy sources (RES), energy storage systems (ESS), and electrical vehicles (EV), will form microgrids that can be grid-connected or islanded [2]. Microgrids in general, are particularly beneficial for riding through grid outages and optimizing power dispatch. Employing DC microgrids to integrate such resources, in place of AC systems, offers further advantages in reducing energy losses by decreasing the required number of AC-DC conversion stages [3].

However, new challenges of system protection associated with this next-generation infrastructure need to be considered prior to widespread adoption. Due to the integration of active devices, bi-directional current flows may cause blinding of conventional graded overcurrent protection [4]. Furthermore, DC fault currents increase very rapidly during short-circuit conditions, without zero-crossings. This places demanding speed requirements on the DC protection system to prevent converter damage [5]. Bayati [6] has proposed a comprehensive review of DC microgrid protection. In a system with uncertain current directions, differential protection can sensitively detect the occurrence of short circuit fault in an ultrafast speed. This type of protection method should operate quickly for internal trip-zone faults but must also remain stable for faults outside these trip-zones.

An effective high-speed differential protection scheme for DC distribution networks was first proposed by Fletcher [7] that isolates a short-circuit fault as fast as 7.4 μs within a low-voltage laboratory environment. High-speed signal comparison algorithms have been employed in many other protection schemes in DC distribution networks, including zonal protection [8]

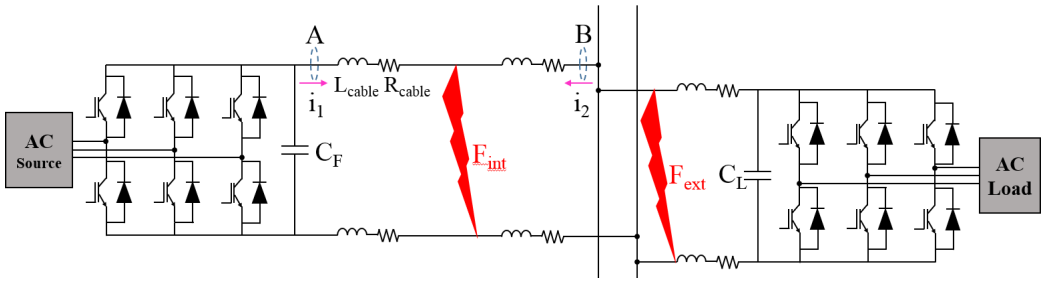

Fig. 1. Equivalent circuit of current differential scheme [7].

and directional protection [9] schemes. These communications-assisted methods provide effective protection selectivity and fast operating speeds, but require very accurate time synchronization measurements for ensuring protection stability [6,10]. For example, as mentioned in [7], a time synchronization error (TSE) as short as 5 μs may create a large current differential error for an external fault, leading to a false-trip condition. Several microseconds TSE may commonly occur in practical implementation, resulting from filtering, A/D conversion, signal propagation, etc. For example, if two 100 kHz ADCs are employed and the sampling is not synchronized, A TSE of up to 5 μs could occur (this is explored in more detail later in the paper). Sub-microsecond time synchronization may be achieved using advanced hardware, but this may cause a high cost when protection devices are widely deployed, which is especially non-economical in distribution networks. As many protection units based on high-speed differential protection [10] may be applied in future large-scale, interconnected DC networks, the protection stability issue caused by TSE may cause multiple false-trips during a fault condition and result in poor system reliability.

This paper proposes a multi-sample differential protection (MSD) method to address the time synchronization error (TSE) on a DC distribution system. This approach employs register-shifted data storage to compare multiple samples and the protection relay will operate only if all the probable comparison results signify an internal fault. When there exists the possibility of an external fault or sudden load change, the protection will not operate to avoid potential false-trip. The method can be applied in radial, teed and multi-terminal structures, and the functionality is realizable using an encapsulated logic circuit to reduce cost. The effectiveness of the MSD method is verified in simulation and validated through experimental demonstration.

II. Impact of Time Synchronization Error to Stability of High-Speed Differential Protection

This section will analyze the impact of TSE on causing protection mal-operation in high-speed differential protection schemes [7], and quantify the current difference error for a number of differential zone configurations.

A. Mathematical Analysis

Fig. 1 illustrates a fundamental differential protection structure that is applied to an example DC network. The relays at A and B will operate when each detects the current difference between its local and remote signals exceeding a predefined threshold. This threshold set-point is selected to tolerate the impact of errors such as distributed capacitance and electromagnetic noise. Accordingly, the current difference can be expressed as

$$\Delta i = i_1(t) + i_2(t - \Delta t), \tag{1}$$

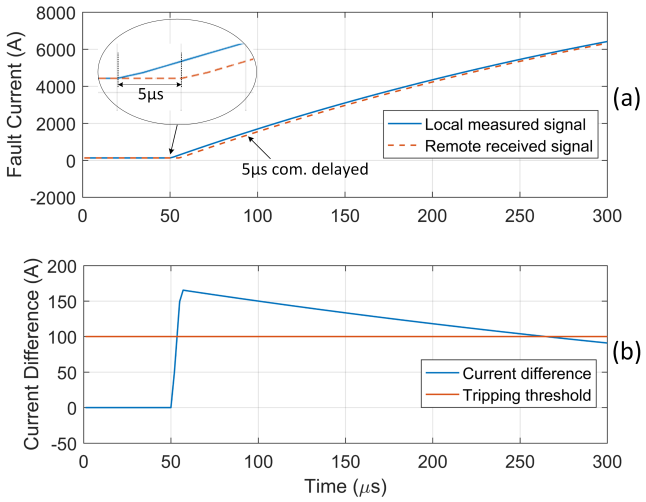

Fig. 2. An example of (a) fault current measurements with communication delay, (b) current difference caused by TSE.

TABLE I
DC MICROGRID NETWORK PARAMETERS [7]

$V_{C_F}(0)$	$i_L(0)$	R/m	L/m	C_F	$C_{F_{ESR}}$	d_{AB}
400 V	125 A	0.64 mΩ	0.34 μH	56 mF	2 mΩ	35 m

where i_1 and i_2 are the current measurements at A and B respectively; t represents the time after the fault occurs; Δt is the time of communication delay from B to A; and Δi is the calculated current difference.

During an internal fault condition, the current difference, Δi, will increase rapidly to reach the predefined trip-threshold, causing the relay to trip. For an external fault condition, the current difference will theoretically be zero and the relay will remain stable. However, where current measurements are not exactly synchronized, a high $\mathrm{d}i/\mathrm{d}t$ from an external fault may result in a large current difference error that causes an undesired trip, causing protection instability issues.

Consider the simulated DC network illustrated in Fig. 1 with circuit parameters shown in Table I. An external fault, F_{ext}, is applied after 50 μs of simulation time, and a communication delay of 5 μs is applied to the remote measurement at point B relative to the local measurement at point A, as shown in Fig. 2 (a). The results of the current differential between these two measurements are presented in Fig. 2 (b). It is clear from this difference calculation that a short-term communication delay may cause a high current difference error during an external fault.

Assuming the tripping threshold is 100 A, this current difference error will be high enough to cause a relay mal-operation. Furthermore, the excessive current difference error may last for several hundred microseconds before it falls lower than the threshold, as indicated in Fig. 2 (b).

The peak value of the current difference error under fault conditions can be quantified in terms of the circuit parameters under the fault condition. In the case of an ideal pole-to-pole short-circuit fault, the fault current response may be represented by a sinusoidal function [11] that can be expressed as

$$i(t) \approx \frac{v_{C_F}(0)}{L\omega_0} \sin(\omega_0 t), \tag{2}$$

where $v_{C_F}(0)$ is the pre-fault voltage of link capacitor; L is the cable inductance from the capacitor to the fault; and ω_0 is the natural frequency of the fault.

Substituting equation (2) into (1), the current difference error shown in Fig. 2 (b) can be expressed as

$$\Delta i(t) = \begin{cases} \frac{v_{C_F}(0)}{L\omega_0}\sin(\omega_0 t) & (t < \Delta t) \\ \frac{v_{C_F}(0)}{L\omega_0}\left[\sin(\omega_0 t) - \sin(\omega_0(t-\Delta t))\right]. & (t \geq \Delta t) \end{cases} \tag{3}$$

Applying the trigonometric equivalence formula

$$\sin\alpha - \sin\beta = 2\sin\frac{\alpha-\beta}{2}\cos\frac{\alpha+\beta}{2}, \tag{4}$$

equation (3) as $t \geq \Delta t$ can be represented as

$$\Delta i(t) = \frac{v_{C_F}(0)}{L\omega_0} \cdot 2\sin\frac{\omega_0\Delta t}{2}\cos\left(\omega_0 t - \frac{\omega_0\Delta t}{2}\right). \quad (t \geq \Delta t) \tag{5}$$

Since $\sin x$ can be approximated to x when $x \ll \pi/2$, the current difference equations in (3) can be simplified to

$$\Delta i(t) = \begin{cases} \frac{v_{C_F}(0)}{L}t & (t < \Delta t) \\ \frac{v_{C_F}(0)}{L}\Delta t \cdot \cos\left(\omega_0 t - \frac{\omega_0\Delta t}{2}\right). & (t \geq \Delta t) \end{cases} \tag{6}$$

From (6) as $t < \Delta t$, Δi will initially develop rapidly and reach its peak at $t = \Delta t$, where the peak value $\Delta i_{\max} \approx \frac{v_{C_F}(0)}{L}\Delta t$. After the peak point, Δi will decay in terms of (6) as $t \geq \Delta t$. Making derivative of equation (6) as $t \geq \Delta t$,

$$\frac{\mathrm{d}\Delta i(t)}{\mathrm{d}t} = -\omega_0\frac{v_{C_F}(0)}{L}\Delta t \cdot \sin\left(\omega_0 t - \frac{\omega_0\Delta t}{2}\right), \quad (t \geq \Delta t) \tag{7}$$

it can be found that the decreasing rate is a very small negative number. Consequently, Δi will decay at a much slower rate than the initial increasing stage of the current difference profile. Accordingly, the high current difference error may last much longer in comparison to the desired high-speed trip-time.

B. Potential Solutions

There are a number of established solutions to this synchronization error, which are summarized and discussed below.

1) Compensation Strategy: Conventional optical fibre based AC differential teleprotection employs IEEE Std C37.94-2017 [12], where the bitstream rate is 2048 kbps $\pm$ 100 ppm. Each data frame is allocated with 256 bits, resulting in a frame rate that is 8000 Hz $\pm$ 100 ppm. Each frame includes a unique 16-bit header to allow the receiver to synchronize the 256-bit frame. That is, each frame is marked with a local timestamp when captured. Then, the frames with the same timestamp are regarded as synchronized regardless of the communication delay. However, microsecond-level accuracy is still rarely achievable because of the clock drift. Due to the 100 ppm error tolerance, the number of frames per second is in the range of 7999.2 to 8000.8. Assuming the local and remote frame rates are 8000 and 8000.5 Hz, the data misalignment can occur, as illustrated in Fig. 3.

In Fig. 3, the frames marked with the same number represent those which share the same header. However, the frames may not correctly synchronize as the accumulation of clock drift will cause an increasingly large TSE. In this example, as each

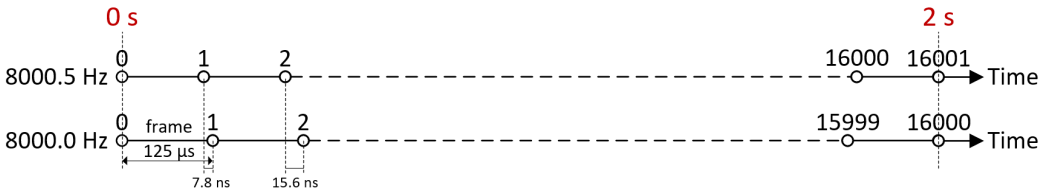

Fig. 3. Explanation of clock drift.

frame will accumulate a 7.8 ns time drift, 641 samples (80.13 ms) will cause a problematic 5 µs TSE. Dealing this issue, the IEC 61850 [13] adopts IEEE C37.118 [14] to transmit synchrophasor information, in which NTP (Network Time Protocol) [15] or Precision Time Protocol (PTP) [16] is employed to calibrate the clock with the Delay Request-Response Mechanism (also known as Ping-Pong method). However, a typical NTP client polls the remote NTP server for calibrating every several minutes so that the target accuracy is few milliseconds [15]. The millisecond-level TSE is tolerable for AC network teleprotection, but DC network may require sub-microsecond accuracy according to the DC fault analysis. However, the implementation of sub-microsecond precision must be supported by advanced hardware, such as PTP, GPS-linked clock [17], and atomic clock [18]. Hence, whilst these technologies are effective in realizing precise time synchronization measurement in HVDC network travelling wave protection, they may be considered as too expensive for a distribution power network.

2) Widen Decision-Making Time-Window: A wider decision-making time-window can be employed to tolerate the impact of time synchronization error. The relay should only trip when all the samples within the time-window exceed the tripping threshold. However, this action will reduce the detection speed during internal fault conditions. From the example shown in Fig. 2, the time-window should be set longer than 200 µs to avoid false-trip during this external fault condition. Hence, this will also result in a minimum 200 µs trip time for internal fault conditions, which may be not acceptable in a high-speed protection scheme.

3) High Threshold Setting: A higher tripping threshold setting could make the protection relays more stable. However, this will also decrease the protection sensitivity for internal high-impedance fault detection. As shown in Fig. 2, the threshold should be set over 200 A to avoid the false-trip, but the protection may fail to detect internal faults with an impedance of higher than 2 Ω.

III. A Novel Time Synchronization Algorithm

To address the issue of protection stability for external faults, a multiple sample differential (MSD) protection scheme is proposed to improve protection stability. This approach employs an one-dimensional array for each current measurement channel which stores a predefined number of previous samples. The differential protection relay compares all the combinations of samples from the arrays, in which at least one correctly aligned comparison exists. During no-fault or external fault conditions, there exists at least one absolute value of combination lower than the preset current threshold. The converse-negative proposition must also be true: only if the absolute values of all combinations exceed the threshold, an internal fault is signified, and the relay must operate immediately. Accordingly, the stability issue caused by TSE can be addressed. This section will introduce the MSD protection scheme, propose the methodology for selecting the size of the array for each measurement channel, and optimize the quantity of required differential calculations to reduce computational overhead.

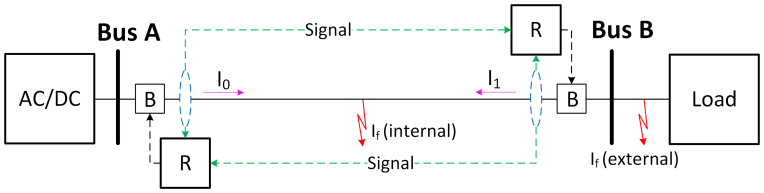

Fig. 4. Differential protection of radial structure.

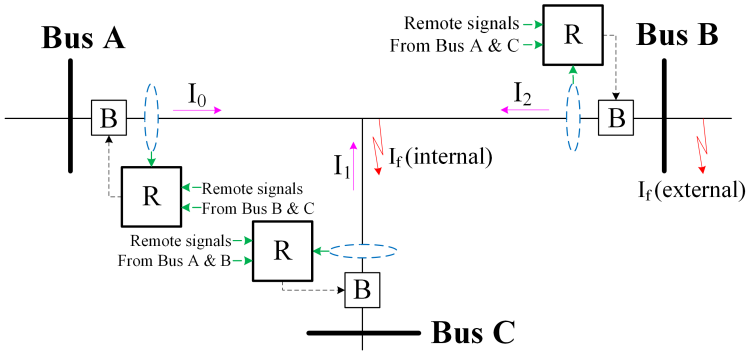

Fig. 5. Differential protection of teed structure.

High-speed differential protection may be applied to three configurations, including radial, teed and multi-terminal circuit structures, as shown in Fig. 4, 5 and 6. Note that in all these cases, at the boundary of the differential zone, the direction of current flow into the zone is defined as positive. Regardless of the circuit structure, differential protection consists of one local measurement and one or more remote measurements. Assuming N_C is the number of measurement channels of any given differential protection structure, $N_C = 2$ represents a radial differential zone, $N_C = 3$ represents a teed differential zone, and $N_C \geq 4$ represents a multi-terminal differential zone structure.

A. Array Size Selection for Measurement Channels

Fig. 7 presents an example of a three-channel relay including one local measurement and two remote measurements with different latencies. This example assumes that the sampling frequency and the maximum speed of the ADC can ensure that the sampling has sufficient resolution and accuracy to capture fast-changing current signals for differential protection. The

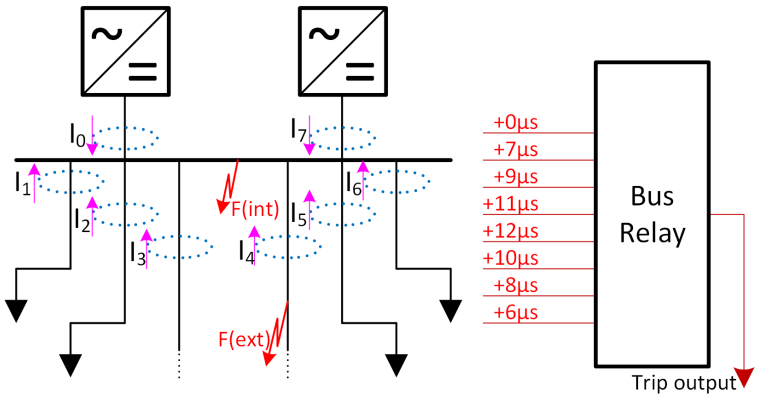

Fig. 6. Differential protection of bus bar.

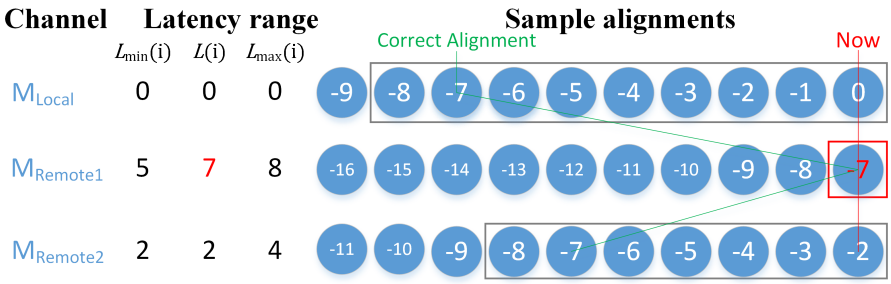

Fig. 7. Example of signal alignment in a three-channel relay.

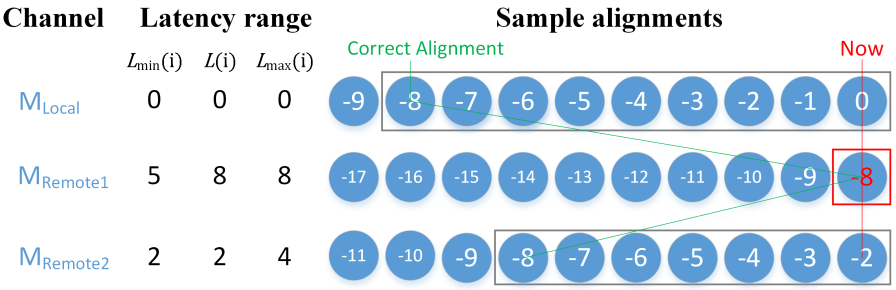

Fig. 8. Array size selection with a FLC.

sample alignments marked with the same number represent the ideally synchronized current samples captured at their local measurements. Note, the numbers presented are the sample number identifiers and not the measured current values. During signal propagation, an undefined latency may occur between the differential relay and its remote measurements according to the communication device specification. An example of latencies is shown in Fig. 7, in which i is the individual measurement channel; $L_{\max}(i)$, $L_{\min}(i)$, and $L(i)$ are the maximum possible, minimum, and actual latencies of each channel with respect to the number of samples.

The selected array size must be wide enough such that at least one set of correctly aligned samples is included. This can be determined by $L_{\max}$ and $L_{\min}$ of each channel. If $L_{\max}$ of a given channel is the greatest compared to the other channels, this channel is known as the latest-channel. However, the latest-channel may be fixed or unfixed depending on its potential latency range. If the latency range of the latest-channel ensures that it is always the most delayed in comparison to all other remote channels, then this channel may be defined as a fixed latest channel (FLC). For example, channel M_{R1} in Fig. 8 has a potential latency range of between 5 and 8 sample delays, whereas M_{R2} has a potential latency range between 2 and 4 sample delays. Accordingly, M_{R1} is guaranteed to always be more delayed than M_{R2}. However, if there is an overlap between the potential latency ranges of measurement channels, the current latest-channel is defined as being an unfixed latest-channel (ULC). As shown in Fig. 9, the latency range of channel M_{R1} is modified between 1 and 8 samples that has overlaps with the latency range of channel M_{R2}. Since channel M_{R1} still has the maximum possible delay ($L_{\max}$) but cannot be guaranteed to always be more delayed than M_{R2}, channel M_{R1} is regarded as an ULC.

By defining the number of samples stored in the array of channel i as $N_S(i)$, only one sample is required to be stored for the FLC. This is because the FLC always provides the global latest sample from all channels, which must be aligned with the local and other remote channels. The latest sample of the FLC defines the size of the array of the other remote measurement

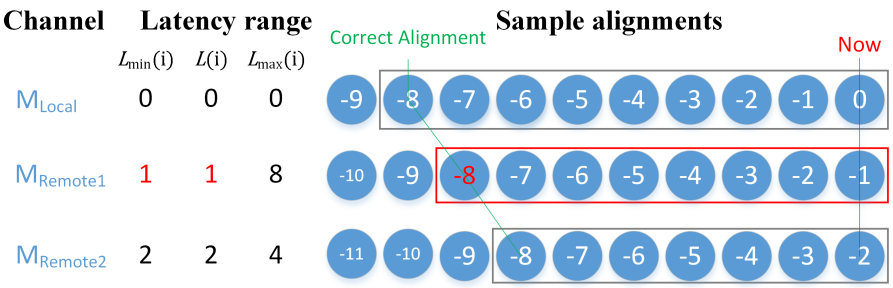

Fig. 9. Array size selection with a ULC.

channels and the local channel required to ensure that the delayed samples are correctly aligned. Considering the case shown in Fig. 8, M_{R1} is a FLC array which includes only one sample in its array. The array size selections for the other channels must ensure the correct alignment of this sample exists. Accordingly, the criteria of array size selection for each non-FLC is defined in terms of the maximum and minimum latency of each channel, such that

$$N_S(i) = L_{\max}(\text{FLC}) - L_{\min}(i) + 1, \tag{8}$$

where $L_{\max}(\text{FLC})$ is the maximum latency of the FLC channel, and $L_{\min}(i)$ is the minimum latency of channel i ($i = 0$ for the local channel).

In the case that channel M_{R1} is a ULC as shown in Fig. 9, the criteria of array size selection must be applied to all the measurement channels including the ULC itself, whereby

$$N_S(i) = L_{\max}(\text{ULC}) - L_{\min}(i) + 1, \tag{9}$$

where $L_{\max}(\text{ULC})$ is the maximum latency of the ULC channel. Fig. 8 and 9 show examples of array size selection with rectangular blocks for both FLC and ULC conditions.

Comparing the two diagrams, in the case of FLC as shown in Fig. 8, the array size of the FLC can be one, because whatever the selected sample is (tagged '-8' to '-5' in this example), this single sample is enough to ensure the existence of the correct alignment with the other two non-FLC channels. In the case of ULC as shown in Fig. 9, the array size of the ULC is selected in terms of equation (9) to ensure the lastest possible simple (tagged '-8' in this example) must be contained in each channel array.

B. Sample Processing for Detecting Internal Faults

After the array size of each channel is selected using equation (8) or (9), the relay should process the measurement signals to determine if an internal fault is detected.

A tapped delay line (TDL) [19] may be employed to update the sample values S_j in each array. The TDL size must be selected to accommodate the array samples in each channel as mentioned above. Fig. 10 illustrates an array of size N_S that stores the latest samples in array positions from S_0 to S_{N_S-1}. When a new sample fills position S_0, the other samples will be transposed forward, and the earliest sample at position S_{N_S-1} is discarded.

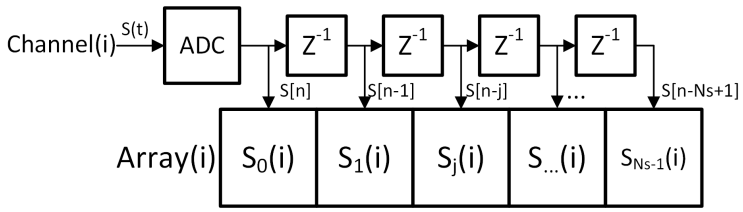

Fig. 10. Tapped delay line of input signal from Channel i.

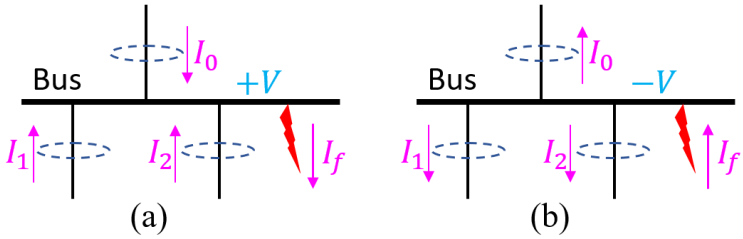

Fig. 11. Types of (a) Current-out fault, (b) Current-in fault.

The principle of fault detection can be derived using contraposition theory: if there is no internal fault, there exists at least one summation of all possible array positions (which hence represents the correct alignment of samples) that is lower than the trip threshold. This is a true statement, so the converse-negative proposition is also true: if all summations exceed the trip threshold, then an internal fault exists. This principle is summarized in Table II , where $S_j(i)$ is the value of the sample at position j in channel i, and THR is the preset current differential trip threshold. Thereby, the operating principle of an internal fault may be expressed as

$$\forall \left| \sum_{i=0}^{N_C-1} S_j(i) \right| > THR. \tag{10}$$

Taking a sample from each channel, the protection relay should calculate the sum of all combinations, and operate if the values of all combinations are out of the range of $(-THR, THR)$.

However, summating all possible combinations of array positions may require considerable computational overhead. The number of combinations, C, may be determined by the array size of each channel, whereby

$$C = \prod_{i=0}^{N_C-1} N_S(i). \tag{11}$$

Consequently, the total number of combinations may be an extremely large number, if the number of channels, N_C, or the array size in each channel, N_S, is large. The example shown in Fig. 9 results in $9 \times 8 \times 7 = 504$ combinations, however the array size in practice may be significantly larger. This may be demanding for the relay processors to realize high-speed operation. Accordingly, it is necessary to reduce the required computational overhead by optimizing the algorithm.

TABLE II
CONTRAPOSITION OF OPERATION PRINCIPLE

If no internal fault,			then $\exists$ $\left\|\sum_{i=0}^{N_C-1} S_j(i)\right\|$	$\leq THR.$
If $\forall$	$\left\|\sum_{i=0}^{N_C-1} S_j(i)\right\|$	$> THR,$	then internal fault detected.	

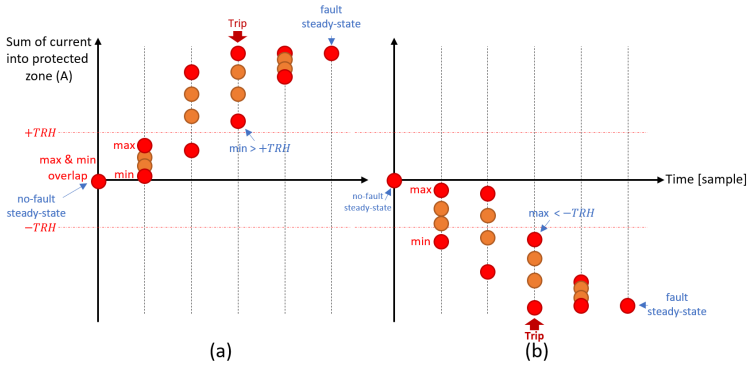

Fig. 12. Illustration of the protection operating conditions: (a) current flow out or (b) current flow in.

Considering a single DC line, differential faults can be categorized as either current-out or current-in variants, as shown in Fig. 11. During the current-out fault conditions (Fig. 11 (a)) where the net current is positive, the protection relay should operate immediately when all summed combinations are greater than a preset positive threshold. Similarly, during current-in fault conditions (Fig. 11 (b)), the relay should operate when all summed combinations are lower than a preset negative threshold. These have been further illustrated in Fig. 12. When the measured currents are changing rapidly, the values of the sample combinations may be in a range due to the effect of communication delay. When the currents are steady-state, all the combinations will settle to the same value. If the relay detects all the combinations are out of the threshold limitations, an internal fault can be confirmed.

Thereby, the operating principle in (10) can be simplified and described in terms of these two conditions, whereby the selection of critical values (maxima and minima) takes place prior to the summation of computations, such that

$$\sum_{i=0}^{N_C-1} \min_{i,\, j=0\rightarrow N_S-1} \{S_j(i)\} > THR, \tag{12}$$

or

$$\sum_{i=0}^{N_C-1} \max_{i,\, j=0\rightarrow N_S-1} \{S_j(i)\} < -THR. \tag{13}$$

Consequently, the simplified operating principle requires the separate selection of the critical value of each array, followed by the summation to compare with the preset current threshold. This optimized algorithm can dramatically reduce the computational overhead.

The logic flow chart of this optimized MSD protection algorithm is illustrated in Fig. 13. At every sampling instance, the local and remote measurement signals are fed into a TDL via an ADC and stored as an array of a pre-assigned length as defined by equation (8) and (9). The maximum and minimum values from each array are selected and summed. According to (12) and (13), the protection relay should operate when either the sum of maxima is lower than the negative current threshold, or the sum of minima is higher than the positive current threshold.

Considering hardware implementation, the function described in Fig. 13 can be designed with Field Programmable Gate Array (FPGA), and eventually encapsulated into an Application-Specific Integrated Circuit (ASIC) that can be mass-produced. Compared with processors, the use of logic circuits can realize faster operation speed and lower costs [20].

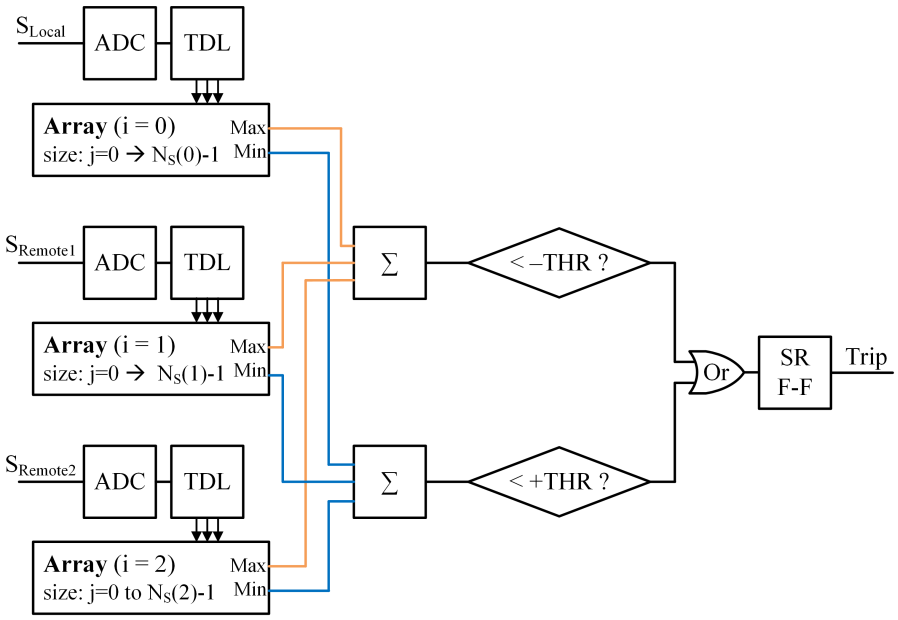

Fig. 13. Protection algorithm of high-speed differential protection mitigating TSE.

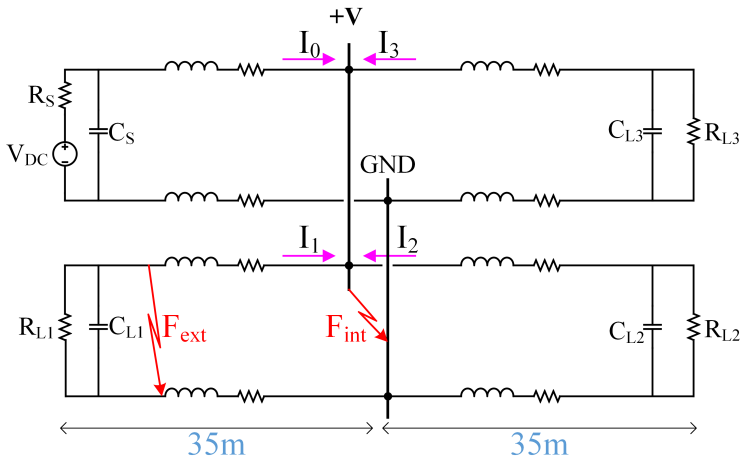

Fig. 14. Circuit configuration of bus protection.

Additionally, the use of the sample array provides more tolerance of accidental sampling errors. In this manner, the threshold (THR) does not need to be set high to overcome the impact of current difference caused by TSE as mentioned in Fig. 2 (b). The THR setting only needs to consider the persistent noise to ensure protection stability.

C. Hardware Requirements

The MSD method purposes to improve the reliability of high-speed DC differential protection, where a high measurement sampling frequency must be employed, e.g., 1 MHz [7]. In the low-frequency applications such as AC differential protection, the conventional time compensation method can be utilized to address the issue of time synchronization error.

The employed communication-links between relays must ensure the latency is maintained below a known upper limit. The delay request-response mechanism may be applied to calibrate the clock and prevent accumulated latency as explained in Section II.B.1. However, in the case of communication failure/loss, the differential protection can no longer effectively protect

TABLE III
ELEMENT PARAMETERS

V_{DC}	R_S [21]	C_S & C_{L123}	$RL_{each\ line}$ [7]
1	0.02 Ω	56 mF	11.2 mΩ, 5.95 μH
R_{L123}	I_{n123}	$R_{F_{int}}$	$R_{F_{ext}}$
3 Ω	0.33	1 Ω	1 mΩ

TABLE IV
LATENCIES OF EACH CHANNEL AND ARRAY SIZE SELECTION

Channel Number (I_i)	Min Latency	Ave Latency	Max Latency	**Array Size Selection (N_S) for the Channel**
I_0	0	0	0	**9**
I_1	30 μs	35 μs	40 μs	**1**
I_2	20 μs	25 μs	30 μs	**5**
I_3	10 μs	15 μs	20 μs	**7**

the network. The differential relays may trip during current disturbances to ensure network safety.

Additionally, the MSD method requires valid current transducers with constrained measurement errors. The maximum noise-level must be known so that the tripping threshold can be specified to tolerate the error. However, in the case that a very high noise-level exists, an excessively high tripping threshold setting may adversely affect the protection sensitivity.

IV. ALGORITHM VALIDATION WITH SIMULATION

To verify the effectiveness of the proposed method, a multi-terminal bus-bar protection scheme is considered. Fig. 14 illustrates a model of a simplified DC power network, constructed within the MATLAB/Simulink environment, used for this case study. A DC supply provides power to three active loads through the four-terminal bus-bar with internal and external fault cases considered. A comparison between uncompensated high-speed differential and MSD protection is undertaken to demonstrate the improvement of protection stability for external faults.

The DC source shown in Fig. 14 is representative of a grid-connected voltage source converter. At the demand side, paralleled RC loads are employed to represent active loads, which may include converter-interfaced renewable energy resources, or energy storage systems. To validate the sensitivity of the MSD protection algorithm, a low-resistance external fault and a high-resistance internal fault are injected sequentially into the network.

As shown in Table III, the details of circuit parameters are referred from [7] and [21], the voltage and current are normalized to unity, and the nominal current is evenly distributed to the three loads. The internal fault resistance is set high to validate protection sensitivity and the external fault resistance is set low to validate protection stability.

To implement the differential protection relay for the bus-bar, the current signals from all four channels are sent to a central relay with different latencies. An example of latencies of the current measurements are shown in Table IV. Since I_1 is the FLC, the array size of I_1 is 1. Assuming the sampling time, T_S, is equal to 5 μs. The array size (N_S) selections for other channels as defined by (8) are also presented in Table IV.

The MSD algorithm is evaluated in simulation to validate the performance for external and internal faults on the network, as shown in Fig. 14. The stability and sensitivity of this method is then compared to conventional uncompensated high-speed

differential protection.

A. Validation Results

The current responses of the four measurement channels for an external fault condition are shown in Fig. 15 (a). Fig. 15 (b) shows the uncompensated sum of all 4 channels using a conventional differential protection scheme. The current differential, Δi, exceeds the current threshold (TRH set as ± 0.1 of load current) in 25 μs, and then falls below the threshold after 1.23 ms. Therefore, conventional high-speed differential protection may cause a false-trip during external fault conditions. Fig. 15 (c) shows the maximum and minimum sums from the MSD protection algorithm shown in Fig. 13. It is evident that the 'maxSum' trace never breaches the '$-TRH$' boundary and the 'minSum' trace never exceeds the '$+TRH$' boundary. Accordingly, the MSD protection method will avoid a false-trip for external fault conditions.

For an internal fault condition, the current response from each channel is shown in Fig. 16 (a). Using a conventional high-speed differential protection method, the protection relay will detect the fault as fast as 5 μs as shown in Fig. 16 (b). However, using the MSD method, the fault can effectively be detected but with a reduced speed of 40 μs as indicated in Fig. 16 (c). Though the fault detection time using the MSD method is 35 μs longer than the conventional high-speed differential method, it can address the instability issue and be effective in ensuring sensitivity to internal faults, compared to the method of widening the fault detection time-window.

Therefore, the simulation results validate that the MSD method is effective in addressing the instability issue caused by communication delay during external fault conditions, whilst maintaining effective sensitivity during internal fault conditions for realizing high-speed DC differential protection.

B. Discussion

The MSD method offers significantly better protection sensitivity compared with the other methods mentioned in Section II.B. Using a wider decision-making time-window to address the protection instability issue, a window longer than 1.2 ms must be selected to avoid a false-trip under the external fault condition, as shown in Fig. 15 (b). However, this will result in an equivalent time delay in detecting an internal fault. Using the MSD method, the relay will remain stable during the external condition, and reacts as fast as 40 μs in detecting the internal fault, as shown in Fig. 16 (c).

Comparing with the method that increases the trip threshold, it must be selected as high as 1.2 times of the load current to avoid the false-trip in Fig. 15 (b). However, during the low-resistance internal fault condition, this will cause a delay in detection and a higher fault current for the breaker to trip. This may require a higher breaker rating and lead to greater damage caused at the location of the fault. Additionally, the MSD method does not require a high threshold setting to deal with the TSE, but only needs a very low threshold to deal with EM noise, cable capacitance, and ADC rounding error.

V. Experimental Validation

A. Experimental Setup

To verify the effectiveness of the proposed MSD method, an experiment was conducted on a low-voltage electrical DC network test-bench shown in Fig. 17. A corresponding schematic diagram is illustrated in Fig. 18. This system consists of

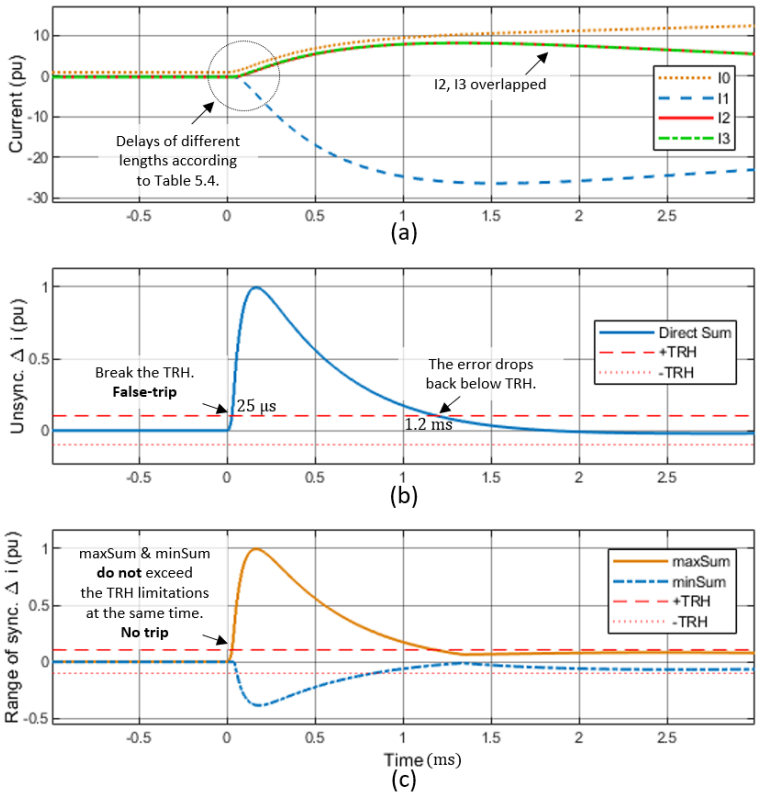

Fig. 15. Simulation results for an external fault condition with (a) current response of all measurement channels, (b) direct sum of unsynchronized currents using conventional method, (c) maximum and minimum sum using MSD method.

TABLE V
METHODOLOGY OF ALGORITHM TESTING

Protection Zone	Operation Switches	Fault Type	
		Internal	External
Branch A	A1 & A2	A_F	C_F
Bus BB	A2, B2 & C2	BB_F	C_F

three DC feeders using inductors to represent distribution lines, and is equipped with voltage and current measurements, and solid-state protection switches devices at each feeder terminal. Short-circuit faults may be applied at each feeder or on the interconnecting busbar.

The experimental methodology is presented in Table V, whereby faults applied to Branch A and Bus BB will be investigated respectively to represent two-terminal and three-terminal zones. In each case, internal and external faults are applied to observe the behavior of both protection methods. For each test, a capacitor located at Bus A representative of the filter of a PEC (charged to 20 V) is discharged through the fault. A short-circuit fault is applied at the corresponding network positions in Table V. The energy stored in the capacitor will consequently release fault current through the shorted path, which can be measured using Hall-effect current sensors. The current measurement signals are conditioned to provide different latencies to evaluate both methods. The trip signals from both methods are digital outputs and are observed using an oscilloscope. The oscilloscope also measures the capacitor voltage and in-feeding current at Bus A without any delay.

To implement virtual communication delays and differential protection algorithms, two separate FPGA-based controllers

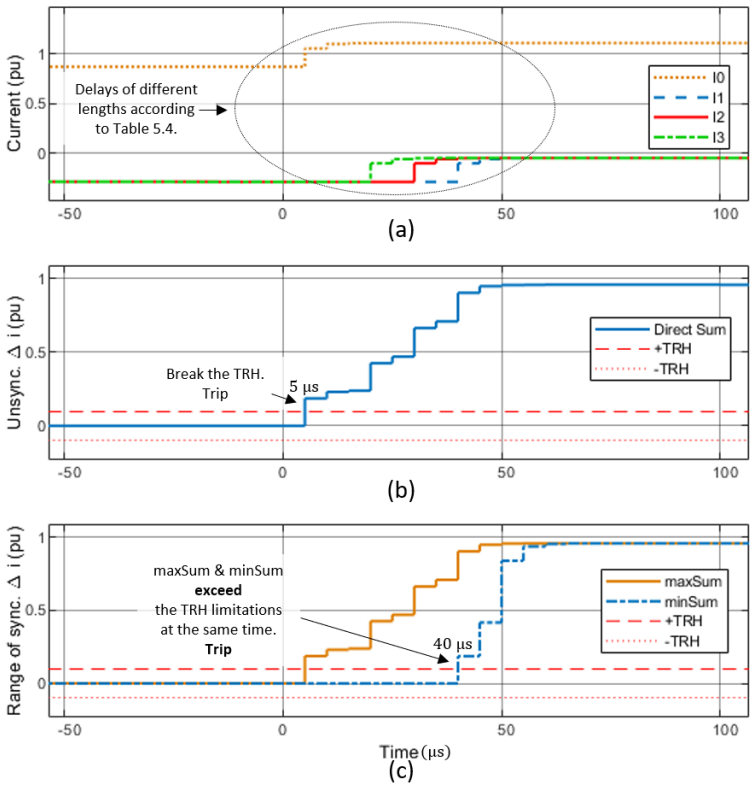

Fig. 16. Simulation results for an internal fault condition with (a) current response of all measurement channels, (b) direct sum of unsynchronized currents using conventional method, (c) maximum and minimum sum using MSD method.

TABLE VI
DETAILS OF EXPERIMENTAL HARDWARE

	Function	Hardware	Experiment Test Settings
1	Power supply	Adjustable DC power supply [22], 0 - 30 V	Set to 20 V constant voltage
2	Capacitor	Aluminium electrolytic capacitor, 2200 µF, 100 Vdc , EPCOS [23]	Charge to 20 V
3	Disconnect supply prior to fault	Semikron SKM 111AR MOSFET [24]	100 V, 200 A nominal (600 A max)
4	Current measurement	LEM HAS 200-S [25]	50 A/V measurement ratio
5	Voltage measurement	LEM LV 25-P [26]	5.7 V/V measurement ratio
6	Representative cable inductor	Murata 15222c	2.2 µH ±20%, 4.2 mΩ
7	Representative load	Panel mount fixed resistor	6.6 Ω
8	FPGA controller 1	NI cRio-9014 [27]	Loop time = 10 µs
9	FPGA controller 2	NI cRio-9024 [27]	Loop time = 15 µs
10	Analogue input	NI 9223 [27]	Loop time corresponding to FPGA target
11	Analogue output	NI 9269 [27]	
12	Digital I/O	NI 9401 [27]	
13	Signal capture	Tektronix OSC MSO 2004B	1 GS/s/channel

are employed. The current measurement signals at the boundaries of protection zone are sent to FPGA controller 1, which is programmed to generate identical delayed signals as outputs. These delayed signals are wired to FPGA controller 2, which is programmed with the multi-sample and conventional high-speed differential protection methods running concurrently. Both trip signals are output for observation, but only one is selected to actuate the corresponding operation switches shown in Table V. Details of experimental hardware are listed in Table VI.

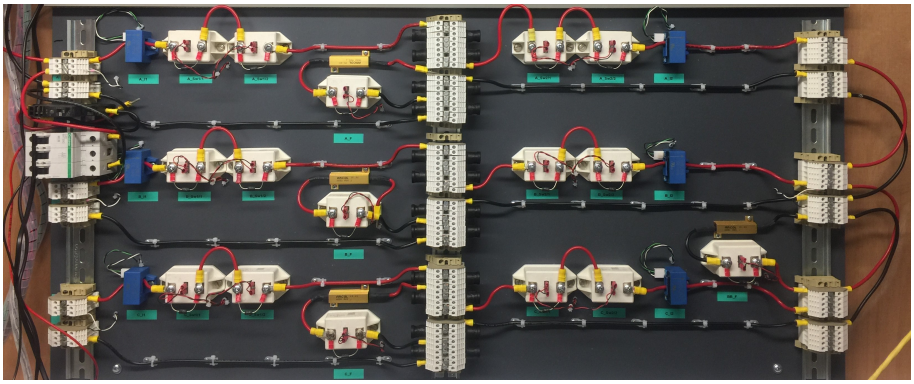

Fig. 17. Illustration of hardware for algorithm testing.

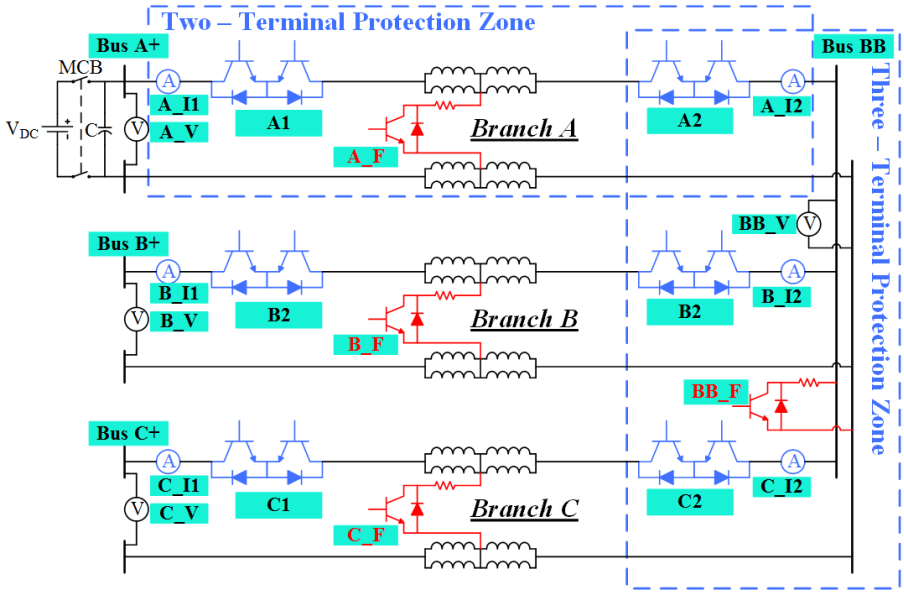

Fig. 18. Primary electrical layout of DC network.

B. Hardware Implementation of Signal Delay

The delay function in FPGA controller 1 is implemented using the circular buffer as shown in Fig. 19, where the latest samples are written successively whilst the output sample reads the register behind with a fixed delay interval representing each channel delay. Latencies of 0, 30, 60 μs are deployed to three measurement channels. As the loop time is set to 10 μs, the delay intervals are set to 0, 3, 6 respectively.

However, due to hardware limitations, the output signals may not deliver perfectly precise latencies. Accordingly, a testing experiment was conducted to inspect processing latency errors. A signal generator is used to provide a saw-tooth waveform that is sampled synchronously by three ADCs. As shown in Fig. 20, the processing delay results in an additional 10 to 20 μs delay greater than the assigned latencies, which must also be considered while assigning the parameters of the MSD protection method. The three measurement channels are allocated as local, remote 1 and remote 2 channels with total latencies displayed in Table VII.

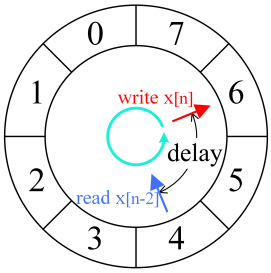

Fig. 19. Circular buffer implementation for delay line.

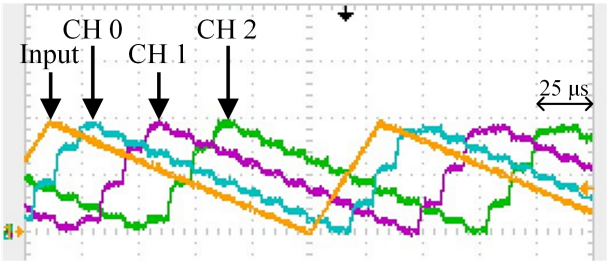

Fig. 20. Waveform of delayed signals.

C. Hardware Implementation of Protection Algorithms

Two independent loops are programmed in FPGA controller 2 to compare the performance of conventional differential protection and the proposed MSD protection method. Since the loop time of FPGA controller 2 is 15 µs, the delayed signals from FPGA controller 1 can be represented in terms of number of samples as indicated in Table VII. These ranges can be used to calculate the N_S setting (the number of samples stored in the array of each channel) according to equation (8). Table VII also shows the derived N_S settings for both two-terminal and three-terminal cases. As the latency ranges have no overlap, the N_S setting of the FLC can be assigned to one. Note that the non-optimized N_S setting for the FLC would normally be 3.

1) Two-Terminal Structure: The results of two-terminal radial protection are shown in Fig. 21. It is clear from Fig. 21 (a) and Fig. 21 (b) that both methods react quickly to the internal fault. The conventional differential protection method reacts in 35 µs, and the MSD protection method reacts in 110 µs. However, for external fault conditions, as shown in Fig. 21 (c) and Fig. 21 (d), the conventional method causes a false-trip whilst the MSD method remains stable to the external fault.

2) Three-Terminal Structure: Similarly, the results of three-terminal teed protection are shown in Fig. 22. Fig. 22 (a) and Fig. 22 (b) show that both methods react quickly to the internal fault. The conventional differential protection method reacts

TABLE VII
LATENCY OF EACH CHANNEL

	Latency produced by FPGA 1	Resulted latency in FPGA 2 (number of samples)	N_S setting (the two-term. case)	N_S setting (the three-term. case)
Local (Channel 0)	10-20 µs	0 - 2 samples	5	7
Remote1 (Channel 1)	40-50 µs	2 - 4 samples	1	3
Remote2 (Channel 2)	70-80 µs	4 - 6 samples	-	1

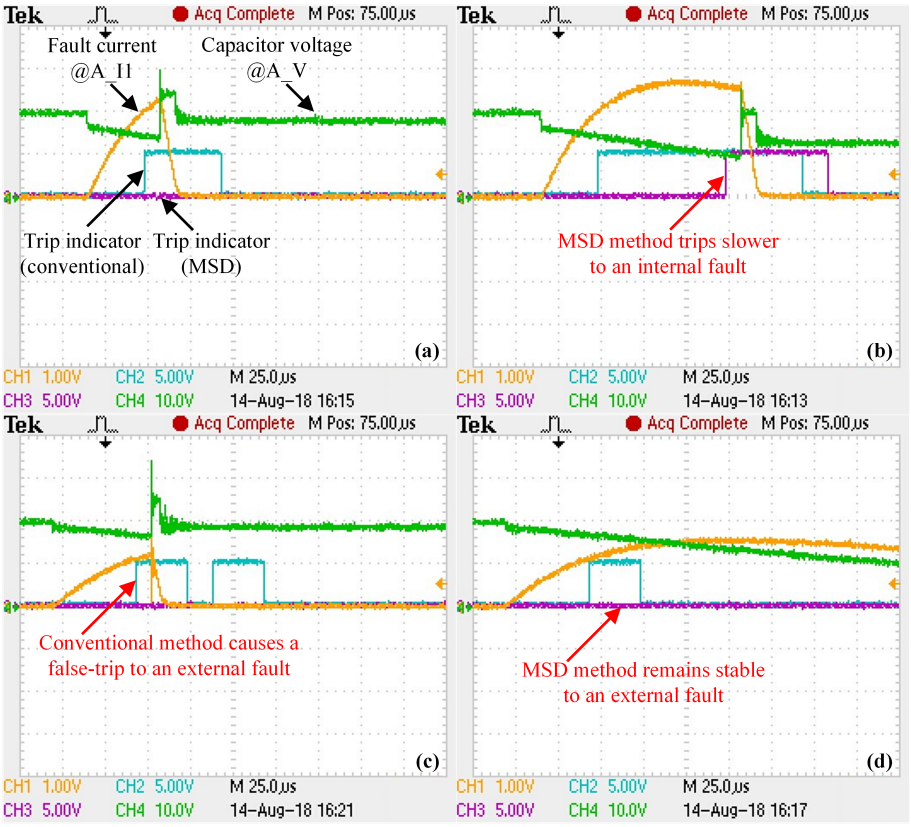

Fig. 21. Experimental results of two-terminal differential protection with (a) internal fault using conventional method, (b) internal fault using MSD method, (c) external fault using conventional method, (d) external fault using MSD method.

in 50 µs, while the MSD protection method is slightly slower at 160 µs. However, similar to the two-terminal radial case, for the external fault condition, the conventional method causes a false-trip whilst the MSD method remains stable as shown in Fig. 22 (c) and Fig. 22 (d).

From the results of both cases, the MSD method provides better protection stability than using conventional differential protection. Although the trip-time for internal fault conditions is increased, sensitivity to internal faults remains sufficient with detection speeds within the sub-millisecond range.

VI. Discussion on Application Scenarios

Based on the simulation and experimental results, the MSD protection scheme can effectively trip the faults in the internal zone but remain untripped during external-zone fault conditions. The performance in radial, three-terminal and four-terminal structures has been validated. DC microgrids usually have a complex multi-terminal structure and the current direction is uncertain, which brings difficulties in fault location. The MSD scheme can be suitably used to protect the distribution lines in DC microgrid regardless of the complexity. Additionally, there are some potential derived applications in which MSD protection scheme may also be applied.

A. Large-scale PV generation

The MSD protection method can be extrapolated to a large PV system as shown in Fig. 23 [28]. Because of the variable intensity of light in one day, the output current of the PV boards may substantially change, which may cause challenges in

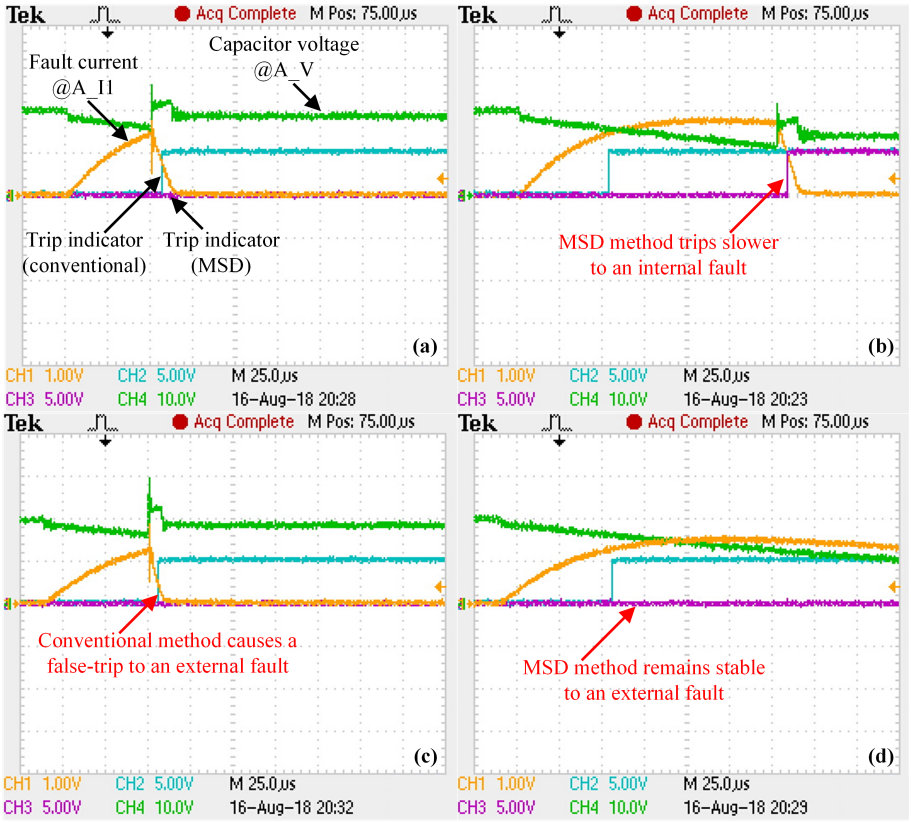

Fig. 22. Experimental results of three-terminal differential protection with (a) internal fault using conventional method, (b) internal fault using MSD method, (c) external fault using conventional method, (d) external fault using MSD method.

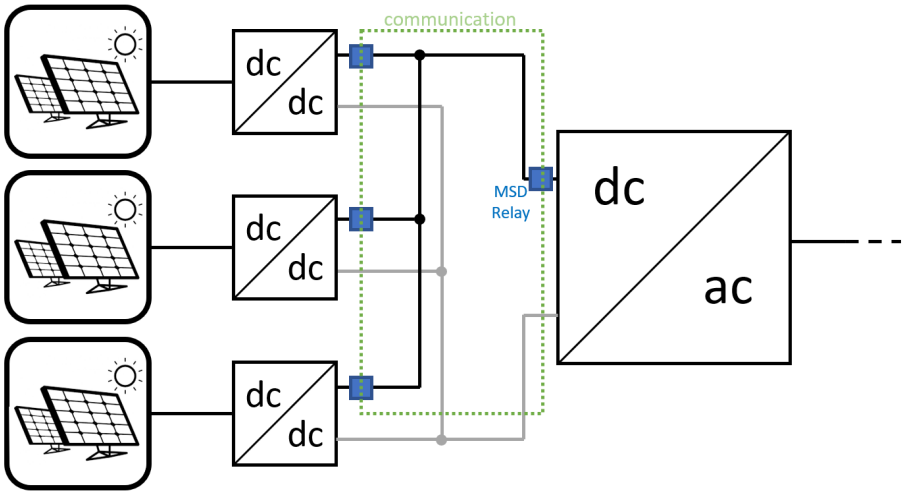

Fig. 23. Schematic diagram of MSD protection in large-scale PV system.

detecting overcurrent faults with high resistance. Failure to detect such faults may result in heat accumulation and a fire hazard. The MSD method can effectively detect any current leakage from the protected zone regardless of the fault resistance. The protection speed of differential protection is fast, and the MSD protection method improves this further to prevent mal-operation during external faults or sudden load changes.

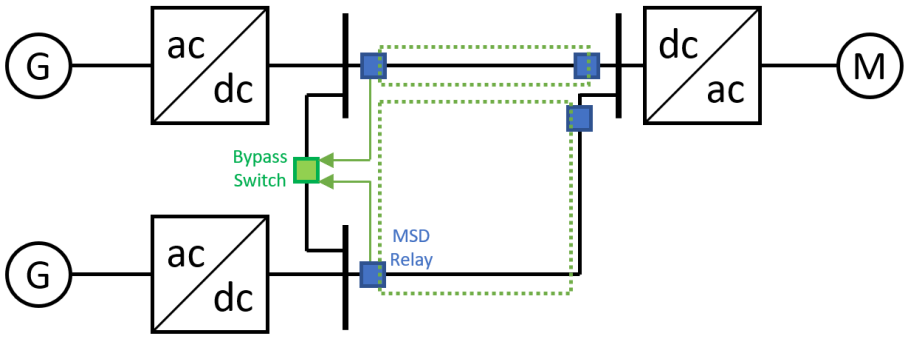

Fig. 24. Schematic diagram of MSD protection in more electric aircraft system.

B. Future More Electric Aircraft System

Future more electric aircraft system may adopt an AC-DC-AC structure to deliver power from generators to the motors or other converter-fed electronic loads, as shown in Fig. 24 [29]. Concerning the DC zone, a differential protection strategy can be employed to isolate any short-circuit faults quickly and switch to the redundant branch to sustain the power supply to the critical load. The MSD protection scheme may be utilized to ensure the relays do not operate during a sudden motor power change.

C. HVDC Power Transmission Line

The MSD method may also be extrapolated to the protection of HVDC transmission lines, where differential protection is a commonly-used protection method [30]. However, an additional challenge in HVDC systems is that the distributed capacitance of transmission line may cause current difference errors in addition to the time delay issues considered in this paper [31,32]. Hence, higher current threshold settings may be required. The application of MSD in HVDC networks hence still requires further consideration, but this is the focus of on-going research efforts by the authors.

VII. Conclusion

This paper proposed an MSD protection method to address the instability issue caused by the time synchronization error of high-speed differential protection schemes in DC microgrids. It was shown that even a microsecond-level TSE will result in a false-trip for external fault conditions. Furthermore, the current difference error caused by TSE may remain high for a long period, which signifies that widening the decision-making time-window may not address the resultant false-trip scenario. The MSD method realizes reliable internal fault detection whilst guaranteeing the stability for external fault conditions when considering latency ranges from multiple measurement channels. Both experimental and simulation results are demonstrated to validate the effectiveness of the MSD method. Taking a four-terminal circuit node as an example, the simulation results illustrate the detailed operating process of the MSD algorithm and the distinguishing between internal and external zone faults. Whilst the hardware demonstration of the MSD algorithm on two- and three-terminal networks prevents direct comparison with the simulated performance on a four-terminal network, the key features of TSE-accommodation and protection restraint are consistent with the simulation results presented, providing confidence in the operation of MSD for all higher-order multi-terminal networks.

Accordingly, MSD protection will enable the rollout of large-scale DC power systems that fundamentally require highly-discriminative and reliable protection for them to be a viable solution for future distribution systems.

ACKNOWLEDGEMENT

The authors would like to thank National Physical Laboratory, UK, for providing financial support to conduct this research.

REFERENCES

[1] T. Dragicevic, X. Lu, J. Vasquez, and J. Guerrero, "DC microgrids—part I: a review of control strategies and stabilization techniques," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4876-4891, 2016.

[2] J. A. Peas Lopes, C. L. Moreira, and A. G. Madureira, "Defining control strategies for microgrids islanded operation," *IEEE Trans. Power Syst.*, vol. 21, no. 2, pp. 916–924, May 2006.

[3] T. Dragicevic, J. Vasquez, J. M. Guerrero, D. Skrlec, "Advanced LVDC electrical power architectures and microgrids: a step toward a new generation of power distribution networks," *IEEE Electrif. Mag.*, vol. 2, no. 1, pp. 54-65, Mar 2014.

[4] P. Rakhra, P. Norman, S. Fletcher, S. Galloway, G. Burt, "Evaluation of the impact of high bandwidth energy storage systems on DC protection," *IEEE Transactions on Power Del.*, vol. 31, no. 2, pp. 586-595, Apr 2016.

[5] J. Yang, J. Fletcher, J. OReilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3827-3837, Oct 2012.

[6] N. Bayati, A. Hajizadeh and M. Soltani, "Protection in DC microgrids: a comparative review," in *IET Smart Grid*, vol. 1, no. 3, pp. 66-75, Oct 2018.

[7] S. Fletcher, P. Norman, K. Fong, S. Galloway, G. Burt, "High-speed differential protection for smart DC distribution system," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2610-2617, Sep 2014.

[8] M. Monadi, C. Gavriluta, A. Luna, J. I. Candela, P. Rodriguez, "Centralized protection strategy for medium voltage DC microgrids," *IEEE Trans. Power Del.*, vol. 32, no. 1, pp. 430-440, Feb 2017.

[9] A. Emhemed, G. Burt, "An advanced protection scheme for enabling an LVDC last mile distribution network," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2602-2609, Jul 2014.

[10] C. Li, P. Rakhra, P. Norman, G. Burt, P. Clarkson., "Metrology requirements of state-of-the-art protection schemes for DC microgrids," *IET the Journal of Engineering*, vol. 2018, no. 15,pp. 987-992, Oct 2018.

[11] S. Fletcher, "Protection of physically compact multi-terminal DC power systems," *Ph.D. dissertation*, Dept. Elect. Eng., Strathclyde Univ., Glasgow, UK, 2013.

[12] IEEE Standard for N times 64 kbps Optical Fiber Interfaces between Teleprotection and Multiplexer Equipment, IEEE Std C37.94-2017, 2017.

[13] Use of IEC 61850 to transmit synchrophasor information according to IEEE C37.118, IEC TR 61850-90-5:2012, 2012.

[14] IEEE Standard for Synchrophasor Data Transfer for Power Systems, IEEE Std C37.118.2-2011, 2011.

[15] Network Time Protocol, NTP Release 4.2.8p3, 2015.

[16] Precision Time Protocol, IEEE 1588-2008, 2008.

[17] D. Tzelepis et al., "Centralised busbar differential and wavelet-based line protection system for multi-terminal direct current grids, with practical IEC-61869-compliant measurements," *IET Generation, Transmission & Distribution*, vol. 12, no. 14, pp. 3578-3586, 2018.

[18] L. Zhan, Y. Liu, W. Yao, J. Zhao and Y. Liu, "Utilization of chip-scale atomic clock for synchrophasor measurements," in *IEEE Trans. on Power Del.*, vol. 31, no. 5, pp. 2299-2300, 2016.

[19] J. Y. Won, S. I. Kwon, H. S. Yoon, G. B. Ko, J. Son and J. S. Lee, "Dual-phase tapped-delay-line time-to-digital converter with on-the-fly calibration implemented in 40 nm FPGA," in *IEEE Trans. on Biomedical Circuits and Systems*, vol. 10, no. 1, pp. 231-242, Feb. 2016.

[20] K. Parnell, and R. Bryner, "Comparing and contrasting FPGA and microprocessor system design and development", Xilinx WP213 (v1.1) [Online], 2004. Available: https://pdfs.semanticscholar.org/3822/8702298b6210c829c1bc34288b289bbf005f.pdf

[21] Vision, Maintenance-Free Rechargeable Sealed Lead Acid Battery Datasheet, [Online]. Available: www.vision-batt.eu/sites/default/files/public/docs/products/manuals/CP1280H.pdf

[22] Velleman, Adjustable DC power supply – PS3020, [Online], Available: www.esr.co.uk/manuals/461-555.pdf

[23] TDK, Aluminum electrolytic capacitor, [Online]. Available: www.mouser.co.uk/datasheet/2/400/B41456_B41458-1219979.pdf

[24] Semikron, Power MOSFET Modules – Semitrans TM M1 SKM 111AR Datasheet, [Online]. Available: www.gdrectifiers.co.uk/uploads/SEMIKRON_DataSheet_SKM_111_AR_.pdf

[25] LEM, Current Transducer-HAS 200-S Datasheet, [Online]. Available: https://www.lem.com/sites/default/files/products_datasheets/has_200-s_sp105.pdf

[26] LEM, Voltage Transducer-LV 25-P Datasheet, [Online]. Available: https://www.lem.com/sites/default/files/products_datasheets/lv_25-p.pdf

[27] National Instruments, Intelligent Real-Time Embedded Controller for CompactRIO on FPGA Chassis and I/O modules, [Online]. Available: www.ni.com/pdf/manuals

[28] C. A. Rojas, S. Kouro, M. A. Perez and J. Echeverria, "DC–DC MMC for HVdc Grid Interface of Utility-Scale Photovoltaic Conversion Systems," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 352-362, Jan. 2018.

[29] M. Flynn, C. E. Jones, P. J. Norman and G. M. Burt, "A Fault Management-Oriented Early-Design Framework for Electrical Propulsion Aircraft," in *IEEE Transactions on Transportation Electrification*, vol. 5, no. 2, pp. 465-478, June 2019.

[30] H. Takeda, H. Ayakawa, M. Tsumenaga and M. Sanpei, "New protection method for HVDC lines including cables," in *IEEE Transactions on Power Delivery*, vol. 10, no. 4, pp. 2035-2039, Oct. 1995.

[31] N. Johannesson and S. Norrga, "Estimation of travelling wave arrival time in longitudinal differential protections for multi-terminal HVDC systems," in *The Journal of Engineering*, vol. 2018, no. 15, pp. 1007-1011, Oct 2018.

[32] S. Gao, Q. Liu and G. Song, "Current differential protection principle of HVDC transmission system," in *IET Generation, Transmission & Distribution*, vol. 11, no. 5, pp. 1286-1292, Mar 2017.