Investigations of Perspective Materials for Aggressively Scaled Gate Stacks and Contact Structures of MOS devices

Von der Fakultät für Mathematik, Naturwissenschaften und Informatik
der Brandenburgischen Technischen Universität Cottbus

zur Erlangung des akademischen Grades

Doktor der Naturwissenschaften
(Dr. rer. nat.)

genehmigte Dissertation

vorgelegt von

Dipl.-Phys.

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geboren am 2. November, 1974 in Kiew, Ukraine

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Tag der mündlichen Prüfung: 29. November 2002

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Chapter I

Introduction

Modern microelectronics is a rapidly developing field which is predominantly based on the complementary metal-oxide-semiconductor (CMOS) technology [1]. The fundamental element of all CMOS integrated circuits (ICs) is the metal-oxide-semiconductor (MOS) transistor [2]. Currently there is a market-driven trend of improving the ICs performance and functionality with a simultaneous decrease in cost. This trend dictates the necessity of further ICs miniaturisation, which in turn leads to shrinking sizes of the MOS transistors [3,4]. While the latter are scaled down, it is important to maintain or improve their gain, switching speed, power dissipation, reliability, operating voltage, etc. This turns out to be possible only if some of the materials traditionally used in the device structures (active and passive) are replaced by new ones with physical properties more suitable for achieving the targeted device parameters. The integration of new materials into the ICs is itself a complex task, since

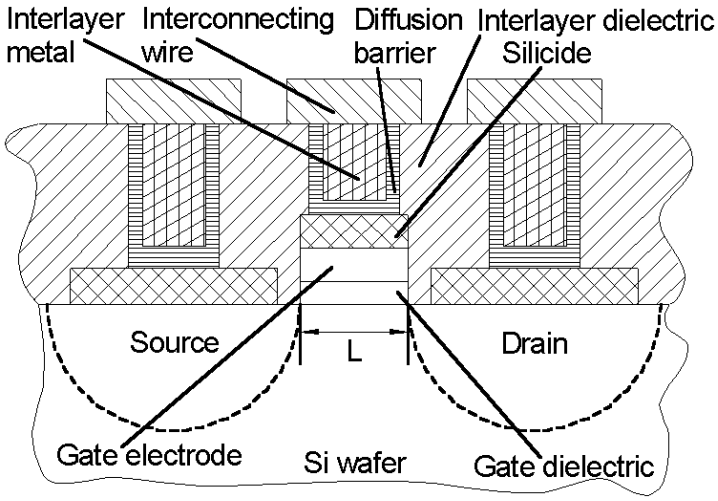


Fig. I.1. The basic structure of the MOS transistor inside of the IC. The transistor consists of source and drain areas in the Si substrate, the gate dielectric (usually SiO_2), and the gate electrode (usually poly-Si). The circuit is formed by interconnecting wires (usually Al) going from one transistor to another. The wires are separated from the substrate by interlayer dielectric (usually SiO_2). The contact between the wire and the transistor consists of silicide (usually WSi_2, $TiSi_2$, or $CoSi_2$), the diffusion barrier (usually TiN or Ti/TiN), and the interlayer metal (usually W).

it requires consideration of numerous issues: deposition procedures, thermal stability, physical properties degradation, etc. As a result a massive analytical effort is usually associated with introduction of new materials into the advanced ICs manufacturing technology.

In order to highlight the issues arising while scaling the MOS transistor it is helpful to consider the basic design of this device, some facts from the theory of its operation and how it is incorporated into the ICs [1-2]. The simplified structure of the transistor inside the IC is shown in fig. I.1. The ICs are manufactured on the Si substrate, which is usually a wafer in (100) orientation. At the front end of production sequence the basic parts of the MOS transistor are created: source and drain regions (the regions of doping opposite to that of a substrate), gate dielectric (traditionally SiO_2) and gate electrode (traditionally poly-Si). Direct contacts to Si parts of the transistor (source, drain and gate) are usually done with silicides (traditionally WSi_2, $TiSi_2$, or $CoSi_2$) in order to obtain contacts with low resistance [5]. The silicide is followed by the layer which serves as a diffusion barrier preventing any diffusion of metal into Si. One of the most widely used barriers is TiN, sometimes in combination with Ti layer [6]. The interconnecting wires are placed on top of the interlayer dielectric (SiO_2) which serves as a "circuit board" inside of which the contact holes are produced. In the case of advanced ultra-large scale integrated (ULSI) circuits there are several layers of wiring and dielectric. The contact holes are filled with the interlayer metal (usually W) and it links the interconnecting wire with the diffusion barrier. Here the chemical vapour deposition (CVD) of W is used because of its high efficiency in filling high aspect ratio holes [6].

Inside of the CMOS digital circuit the sources and drains of transistors belonging to one logical element are connected to gates of transistors from other elements. During switching (from "off" to "on" states or vice versa), the saturated current of one transistor (flowing through the channel - a region of substrate between source and drain) recharges the gate capacitance of another transistor. This saturated value [2] is given by expression:

$$I_{DS} = -Z\mu C_G(V_{GS} - V_T)^2/2L \quad (I.1).$$

Here Z is the width of the channel (in the direction perpendicular to the plane of the drawing in fig. I.1, μ is the carriers mobility inside the channel, C_G is the capacitance

per unit area of the gate electrode, V_{GS} is the voltage between the gate and the source, V_T is the threshold voltage and L is the length of the channel. As it was stated above, during switching between the logical states the saturation current recharges the capacitance C with the time constant $\tau = RC$, where R is the full resistance between the recharging and recharged transistors. The recharged capacitance has two principal contributions: the capacitance of the gate and the parasitic capacitance. It is very desirable to reduce the latter and this is being accomplished through introduction of low-K interlayer dielectrics [7]. The gate capacitance contribution is proportional to C_G, which in its turn should not be reduced since it would lead to lower I_{DS}. The maximum current needed in the process of recharging is V/R, where V is the voltage to/from which the gate is recharged. If $I_{DS}<V/R$, then it would take longer to switch between the logical states than it is expected from the given value of τ, and the speed of circuit operation would be compromised. In practice it always appears that the parasitic capacitance is much larger than the gate capacitance, therefore it is actually better to increase C_G in order to be able to drive larger loads by larger I_{DS}. The classical scaling rule of the MOS transistor requires that all vertical and lateral sizes are decreased proportionally [8]. As miniaturisation of ICs proceeded, C_G was increased by making the gate dielectric ever thinner. It helped to maintain the necessary value of I_{DS}, which according to (I.1) would otherwise drop due to simultaneous decrease of operating voltage. The latter is required by the tendency of making low power consumption devices and to avoid electrical breakdown or excessive power dissipation in ever smaller devices. Up to recent time it was possible to decrease the gate dielectric thickness $t = K/C_G$ (K is the dielectric constant of the given material and is normally small) as much as the value of I_{DS} required. However already for 0.13 μm gate length CMOS technology t reaches 1.5 nm [3-4] and at this thickness the tunnelling through the oxide becomes noticeable [9]. It is still possible to produce functional devices under this condition but only if the tunnelling current is taken into account while designing the circuit [10]. However the power consumption associated with this current will be extremely undesirable for low-power mobile applications [11]. If t is further decreased, the tunnelling current will eventually become so large (it grows exponentially when t is reduced) that the MOS transistor will not function any longer, since there will be no effective insulation between the gate and the channel. It appears that the problem can be solved only if the SiO_2 gate dielectric is replaced with a material having a higher value

of K [12]. In this case the same C_G can be achieved with the physical dielectric thickness $K_{new\ material}/K_{SiO2}$ times larger than it had to be for SiO_2 [13]. Such new materials are called high-K dielectrics and their investigations are of vital importance for enabling further advances in microelectronics [14-18]. If the physical thickness of the gate dielectric can be kept above 2 nm, the tunnelling through it will be effectively eliminated and the gate isolation from the channel will be maintained. That is a desirable scenario of CMOS technology scaling, but it had yet to be realised in practice. There are a number of materials with K higher than $K_{SiO2} \sim 4$, but in order to be considered as gate dielectric candidates they must meet a number of stringent requirements. In particular, a good material must be thermally and chemically stable in contact with silicon and other materials forming the gate stack, have low leakage current, not substantially degrade with time, form a high-quality interface with silicon channel, etc. It turned out a formidable challenge to satisfy all these requirements simultaneously. A known solution, which is already applied for 0.1 micron CMOS technology is a SiO/SiN stacked gate dielectric [19]. In such a structure the tunnelling current is one order of magnitude smaller than in SiO_2 of equivalent electrical thickness. This is however only a temporary relief for the semiconductor industry, since no proven solutions exist for CMOS scaled beyond 0.09 μm gate length [4]. There are however a lot of promising materials which are intensively investigated [14-18]: metal oxides, rare earth oxides, titanates, silicates, aluminates, etc. In the current thesis an evaluation of one of such promising high-K candidates, Pr_2O_3, is described. This material is unique in terms of its fairly high $K \sim 30$, ultra-low leakage current density of 5×10^{-9} A/cm^2 [20-21], and possibility of application in both n- or p-type MOS devices [22], but it was hardly at all investigated in comparison with other rare earth oxides. This prompted a thorough analytical investigation of Pr_2O_3 and its compatibility with the CMOS technology.

Due to the novelty of Pr_2O_3, the only readily available option to deposit it on the Si(100) substrate was by molecular beam epitaxy (MBE). In this way the qualitative difference between Pr_2O_3 and SiO_2 was that the first is crystalline [23-25], while the later is amorphous. In order to produce a crystalline Pr_2O_3 one has to keep the temperature of the substrate in a certain range, giving the deposited molecules enough mobility, but simultaneously preventing their decomposition or chemical reaction with Si. It was possible to grow high quality Pr_2O_3 films on the Si(100) substrate kept at

temperatures between 625°C and 725°C [20]. The crystalline condition of the substrate is an important factor influencing the growth process.

One of the most fundamental properties of any semiconductor surface is its reconstruction. The latter was intensively investigated for the case of the Si(100) surface already for several decades. The undying interest to this subject is fuelled by its ongoing dominant application in the microelectronics production and inability of alternative materials (e.g. III-V compounds) to become a viable replacement. The most widely investigated reconstruction of the Si(100) surface is a 2×1 dimer row structure [26]. This basic structure can have several modifications, namely a 2×n superstructure which arises due to ordering of dimer vacanices [27] and local c(4×2) or p(2×2) periodocities which arise due to dimer buckling [28]. The physical origins of these reconstructions are understood and their exact atomic models are developed, for which an excellent review with a historical perspective was given by Dabrowski and Müssig [29]. Surprisingly, the above-named cases have not exhausted all possible options despite many years of intensive research. It turned out, that some "exotic" (studied and understood to a lesser extent) reconstructions such as c(4×4) [30], c(4×8) [31], and c(8×8) [32] may exist on the Si(100) surface. The atomic models of their structures are not yet firmly agreed on and so are the factors which favour the formation of every particular one. This means that our knowledge of the physical properties of the Si(100) surface is still far from being complete. Understanding these properties in full is desired for further miniaturisation in Si(100)-based microelectronics technologies, thus warranting further studies. Concerning the deposition of high-K Pr_2O_3 films, the Si(100)-c(4×4) reconstruction may be relevant in terms of forming the interface to the high-K dielectric. As thoroughly reviewed in [33], this reconstruction always appears at substrate temperatures between 550°C and 700°C independent of numerous reported preparation procedures, thus substantially overlapping with the temperature window of Pr_2O_3 epitaxy. Obviously the properties of the c(4×4) reconstruction can strongly influence the quality of the epitaxial Pr_2O_3 film, should the substrate find itself in this condition during growth. In particular, the substrate defects may be an aggravating circumstance, especially for ultra thin dielectric films applied in aggressively scaled MOS devices. These defects may lead to a low quality Si/high-K interface, causing all kinds of problems like reduced carriers mobility in the channel, high-K film subjected to electrical breakdown, and unsatisfactory MOS electrical characteristics, thus, making

a high quality interface an extremely important goal [14-15]. According to the previous works of other authors, it is exactly due to a large number of defects is the c(4×4) reconstruction considered a metastable phase on the Si(100) surface (see references in [29,33]). In the meantime, it seemed strange that such kind of phase has a certain characteristic formation temperature and is insensitive to the types of adsorbates (if any) used in the preparation procedure. This controversy requires a revision of the Si(100)-c(4×4) reconstruction models, for which the new insights can be gained from the scanning tunnelling microscopy (STM) investigations. The STM (although quickly approaching its 20th birthday) is still a relatively new and pioneering technique. It is capable of imaging the structure of solid surfaces with atomic resolution, thus being a front-end direct tool for studying the surface reconstructions [34]. The data presented in chapter III of this thesis give a strong hint that the c(4×4) reconstruction is a ground state of the Si(100) surface in the temperature range mentioned above. These data show how to reduce the number of defects on the Si(100)-c(4×4) surface, which may be important for obtaining high quality interfaces with Pr_2O_3 deposited on top of it. The practical need for simulation of interfacial electronic or other properties, and also the fundamental interest in understanding semiconductor surfaces require creation of an adequate atomic model of the c(4×4) reconstruction. As summarised in [33], the previously existed models of other authors contradicted each other, and also they could not account for the new STM images obtained in the present work and shown in chapter III. These images suggest that the c(4×4) structure has a lower symmetry than was previously believed. This fact prompted a suggestion of the new atomic model for the Si(100)-c(4×4) reconstruction which was analysed by semi-empirical total energy calculations [33].

As long as a Pr_2O_3 film is successfully deposited, one of the major concerns is its thermal stability in contact with Si. This corresponds to a traditional MOS transistor scheme (fig. I.1), where the gate dielectric is in contact with a Si(100) substrate underneath and a poly-Si gate electrode above. After transistors themselves are formed, they are inevitably subjected to several thermal treatments (silicidation anneal, dopants drive-in, etc.) belonging to the standard CMOS technology process sequence. A comprehensive study by Hubbard and Scholm [35] was aimed at estimating the thermal stability of all binary oxides in contact with Si on the basis of available thermodynamic data. These data are absent for possible reaction products in the case of Pr_2O_3/Si system,

so the conclusion about thermal stability could not be reached. A more recent experimental infrared spectroscopy investigation by Ono and Katsumata [36] have detected the formation of Si-O-Pr bonds in this system at temperatures between 600°C and 800°C. The scarce information on thermal stability made obvious the need for a comprehensive research of this issue using some direct experimental technique. AES is a standard analytical tool allowing to detect chemical composition with a sensitivity of about 1% or less and lateral resolution about 100 nm or less [34,37]. When combined with ion sputtering it can reach arbitrarily deep layers inside the samples, thus being capable of producing three-dimensional elemental distribution maps. Therefore, AES depth profiling (obtaining elemental distribution as a function of depth) was used in this work to study intermixing of materials in Pr_2O_3/Si(100) and Si/Pr_2O_3/Si(100) structures. The first is of fundamental interest, while the latter is an application relevant model of the MOS capacitor or part of a MOS transistor's gate stack. Chapter IV of the thesis describes the investigations of these structures in the wide temperature range from 600°C to 1200°C both in vacuum and nitrogen environments [38]. It will be shown that the presence of nitrogen at ambient pressure leads to a much higher thermal stability, which is a positive sign because silicidation anneals (discussed in chapter VI) are usually done in this environment. Another interesting phenomenon, which will be demonstrated, is the dependency of the reaction's final product (Pr silicate or Pr silicide) on the initial geometric configuration of Pr_2O_3 and Si. This dependency may be used for an elegant creation of source/drain contacts [39], should Pr silicide be chosen instead of traditional WSi_2, $TiSi_2$, or $CoSi_2$.

The application of Pr_2O_3 as a gate dielectric is targeted for future sub-100 nm MOS transistors. Building the ICs with such transistors will also require making other changes in the traditional set of materials applied in the modern CMOS technology. It is well known that ICs are getting not only smaller, but ever faster as well. This dictates designing logical circuits operating at ever higher frequencies, thus requiring the reduction of time constant τ described above. Lower values of τ can in particular be achieved by making the resistance R smaller all the way from the source or drain of the transistor in one logical element to the gate of transistor in the following logical element [40]. This goal can be achieved by using higher conductivity metal for interconnecting wires and designing lower resistance contacts between the wires and transistors. According to this trend, Cu is being actively introduced instead of Al for the

interconnecting wires [7]. An equally important task is ensuring the low resistance of contacts between wires and transistors under the conditions of shrinking sizes. Contact to the gate is a spatially most constrained location, where traditional WSi_2 or $TiSi_2$ suffer from a severe line width effect (resistivity increase at a size limitation in one or more dimensions). It was proposed to solve this problem by using W/WN_x/poly-Si material combination for the gate stack [41]. This means that any silicide is completely removed from the gate and WN_x barrier between W and Si actually serves to prevent silicidation [42-46]. The transistors with such gate stacks were used in particular for latest generations of dynamic random access memory ICs [47-48]. WN_x was shown to be a good diffusion barrier also in cases when Cu was applied instead of Al for metallization [43-44,46] and when the higk-K material (Ta_2O_5) was applied as a gate dielectric [49]. The ability to grow WN_x films by a CVD technique [43,46,50-51] puts it into a favourable position for application inside of very small contact holes. In the meantime, introducing this material into a real production requires its comprehensive analytic investigation. In particular, analysis of composition inside of the WN_x layers and on the interfaces with W and Si is important for deposition process control and for verifying the effectiveness of WN_x as a diffusion barrier. The results given in chapter V of this thesis are focused on AES depth profiling of the novel W/WN_x/poly-Si and the older WSi_2/poly-Si gate stacks [52]. Under the conditions of shrinking sizes of transistors, the barrier layers are getting ever thinner, thus raising an issue of adequate depth resolution in the Auger depth profiles (ADPs). Therefore, a goal was set to achieve the best possible resolution by using low energy sputtering ions and sample rotation during profiling. This worked perfectly for W/WN_x/poly-Si structures, but preferential sputtering of Si did not allow to improve the depth resolution for WSi_2/poly-Si samples when the latter were rotated. Also it turned out that preferential sputtering of O inside of W/WN_x layers is a reason, why this element is detected better when the analysed sample is rotated during profiling than when it is stationary. Demonstration of these effects is a substantial contribution to the analysis methodology for advanced W/WN_x/poly-Si gate stacks.

The novel sub-100 nm MOS transistors with high-K gate dielectric (e.g. Pr_2O_3) will also need low resistance contacts to source and drain areas [40]. Another very prospective material for making contacts between wires and transistors is $CoSi_2$. It has a very low resistivity (18÷25 μOhm×cm) [5], which is not subject to feature size limitation [53]. $CoSi_2$ contacts can be formed through a convenient self-aligned silicide

(SALICIDE) process [1,54-55] on gate, source and drain of the MOS transistor. Such combination of desirable factors paves the way for universal $CoSi_2$ usage in the latest generations of ICs [7]. During the SALICIDE process an entire Si wafer is covered with SiO_2 which is removed only at contact locations. The layer of Co is blanket deposited over the entire wafer and annealed afterwards. $CoSi_2$ formation proceeds only where Co is in direct contact with Si (where SiO_2 is absent), while no reaction takes place between Co and SiO_2. After annealing, any unreacted Co is etched away selectively, leaving the silicide and SiO_2 intact. Inside the contact holes, $CoSi_2$ is followed by the TiN/Ti diffusion barrier, which separates the silicide from interlayer W. There arises an obvious need to control different stages of contact structure formation. In chapter VI of this thesis a multitechnique analytical investigation of the Co SALICIDE process on source/drain areas is presented. For this purpose, Co was deposited on the Si(100) substrate and annealed at different temperatures to yield three different phases (Co_2Si, CoSi, and $CoSi_2$), which were analysed by AES. Since preferential sputtering of Si during ion irradiation can distort the measured composition (as was shown for WSi_2 in chapter V), it was quantitatively investigated for all three given phases [56]. After the extent of preferential sputtering was firmly established, AES depth profiling could give information about chemical uniformity and spatial distribution of different phases in thin silicide films. This allowed to identify the SALICIDE process parameters (annealing temperature and duration, film thickness, etc.) which are optimal for obtaining the targeted $CoSi_2$ layers. The obtained results were used to calibrate spectroscopic ellipsometry (SE) measurements and thus determine the optical parameters of all three silicide phases. SE [57] is a non-destructive technique for controlling the thickness and composition of thin films, which is preferred in production environment. After AES-assisted calibration, SE alone was able to identify the phases and thickness of corresponding silicide layers. It was then used as a non-destructive technique to control all stages of the SALICIDE process on the CMOS technology pilot line.

The text of the present thesis has the following structure. After the current introductory part, the details of experimental procedures are described in chapter II. All scientific work presented in this thesis is contained in chapters III-VI. The future outlook for the investigations described in chapters III-VI is given in chapter VII. The latter also gives an overview of emerging trends in CMOS technology and how the obtained results may fit into them. Further more, this part of the manuscript attempts to

create a perspective of how the surface science techniques will keep contributing into the continuous scaling of CMOS and once it is finished, how they will enter the realm of nanotechnology and nanoelectronics. The thesis is finalised with the summary of the key scientific results obtained by the author.

Chapter II

Experimental techniques

II.1. Auger electron spectroscopy

Auger electron spectroscopy (AES) is a powerful analytical technique, providing information about the chemical composition of near surface layers of solid bodies [34,37,58]. Physically, it is based on the Auger effect, discovered by P. Auger in 1923. When combined with ion sputtering, AES can obtain a complete three dimensional distribution of chemical elements in the sample of interest. This makes AES extremely valuable for both fundamental and applied research. Nowadays, AES had become a standard analytical tool in every industrial lab within semiconductor, chemical and other industries [59]. It is also a standard surface science technique universally used for basic research by countless groups world-wide.

II.1.a. Physical background of AES

The qualitative principles of AES are quite simple. The first thing, necessary for the Auger effect to occur, is the ionisation of some inner electron level A inside the atom. In practical analysis this is achieved through bombarding the sample by primary electrons, with kinetic energy E_p usually in the range from 3 to 10 keV. Another way of creating the inner vacancy is through the interaction of the atom with X-ray photon. While colliding with atoms, either electrons or photons transfer part of their energy to the electrons occupying inner levels, causing the latter to become ionised. After this, the primary particles become inelastically scattered and the ionisation electrons emerge. The ionised level A can be filled by the weaker bound electron from the occupied level B, freeing the relevant energy difference. The latter can be transferred to the third, yet weaker bound,

electron from level C. Thus, this third electron, called Auger electron, will leave the atom with kinetic energy equal to [60]:

$$E_{K(ABC)} = E_1(A) - E_2(B,C) \quad (II.1).$$

Here $E_1(A)$ is the energy of a single charged isolated ion (the given atom with an electron at level A removed) and $E_2(B,C)$ is the energy of double charged ion (the given atom with electrons at levels B and C removed). The above described process is referred to as Auger effect or Auger transition and is schematically depicted in fig. II.1. Such transitions are

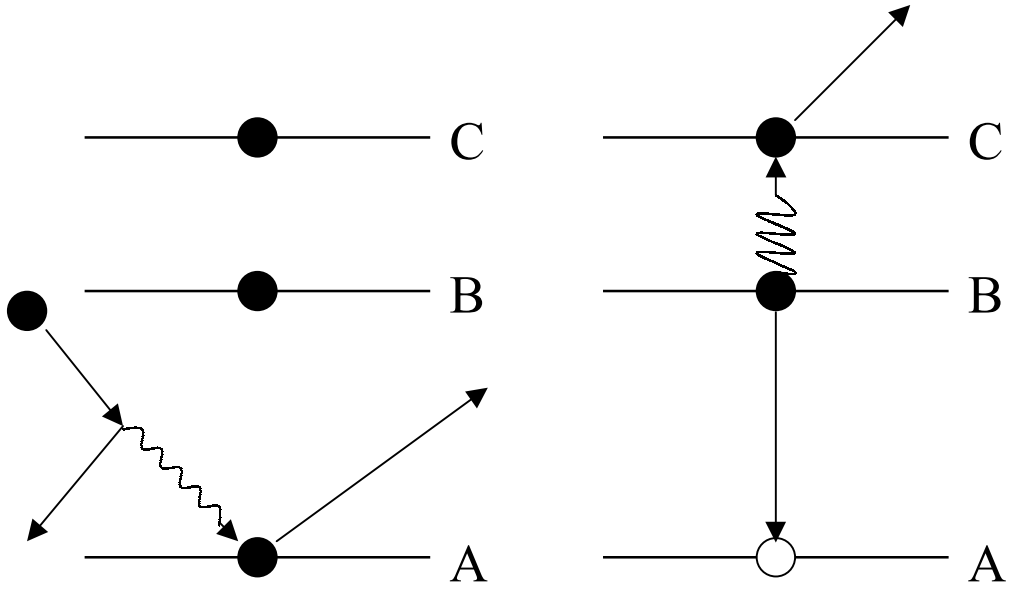


Fig. II.1. Schematic representation of Auger effect excited by collision between the electron and the atom. The primary electron ionises the level A, which is subsequently filled by electron from level B. The released energy is consumed to eject the Auger electron from level C. Filled circles depict electrons and empty circle is an electron vacancy. Straight arrows designate particle trajectories and wavy arrows - energy transfers.

denoted as ABC with actual letters designating the shells, to which involved electrons belong (such as K, L, M.., - in direct correspondence with the electron's principal quantum numbers n = 1, 2, 3...). For example, silicon can be identified by the LMM transition with $E_{Si}(L, M, M) = 92eV$ and oxygen by KLL transition with $E_O(K, L, L) = 503eV$.

It is important to realise that the entire Auger electron emission is essentially a simultaneous quantum-mechanical process, which can only be approximately represented as sequential transitions of electrons between different states (including non-bound state) and energy exchange between them. If such approximation is performed one often uses the electron binding energies instead of ion energies [61]:

$$E_{K(ABC)} = E_{B(Q)}(A) - [E_{B(Q)}(B) + E_{B(Q+1)}(C) + E_{B(Q+1)}(B) + E_{B(Q)}(C)]/2 \quad \text{(II.2)}.$$

Here $E_{B(Q)}(A)$ is the binding energy of the electron at level A in the atom with nuclear charge Q. The first two terms inside the square brackets in equation (II.2) are based on the following reasoning. The binding energy of the electron at level B is subtracted from that at level A, giving the energy released after the first vacancy is filled. This energy is then reduced by the binding energy of the electron at level C, in order to estimate the kinetic energy of Auger electron. Since the electron leaves from level C when there is a vacancy at level B, it is like leaving an atom with a nuclear charge larger by one. In reality one can not distinguish which electron fills the initial vacancy and which is emitted – B or C. That is why an arithmetic mean of energies corresponding to both possibilities is calculated through introducing the third and the fourth terms into the square brackets and dividing the latter by two. Expression (II.2) neglects the interaction between two vacancies left inside the atom after the Auger process has taken place and the difference between the single electron wave functions in the ion and in the neutral atom. There are also other sample specific factors like energy shifts of the electron levels inside the solid body comparative to the free atom or electron energy shifts due to chemical surrounding in compounds, mixtures and alloys comparative to pure chemical elements. Nevertheless it appears that Auger electrons' energies remain more or less constant and characteristic for every chemical element, except helium and hydrogen, always allowing for unambiguous determination of chemical species, which are present in the sample.

II.1.b. Basic realisation of AES

There are a number of ways to ionise the atoms and excite the Auger effect [34]. The most widely spread approach, which is also used in this work, relies on bombarding the sample with primary electrons of certain kinetic energy in the range from 3 to 20 keV. After the Auger electron has left the sample it is necessary to detect this electron and determine its kinetic energy. This is done by an electron energy analyser, which filters out all electrons except with kinetic energy it is tuned to, and by an electron current detector, which counts the electrons (measures their current) after they have passed the analyser. The tuned energy is scanned over a range where Auger energies (Auger spectral lines) are usually found - from ~10 eV to ~2400 eV [62]. As a result, the electron current passing through the analyser is recorded as a function of electron energy I(E). When the analyser is tuned to an energy E, it actually lets the electrons having energies within a certain interval ΔE to go through. The latter always has the finite value and determines the analyser's resolution as

$$r = \Delta E/E \quad \text{(II.3)}.$$

The efficiency of collecting electrons with kinetic energy E is characterised by the analyser's transmission T(E). Further, as the electrons have passed the analyser they are registered by a detector, which in turn has its own sensitivity D(E). One may thus write the following relation between the raw signal I(E) and the energetic distribution N(E) of the electrons entering the analyser:

$$I(E) = \int_{E-0.5\Delta E}^{E+0.5\Delta E} T(E)D(E)N(\varepsilon)d\varepsilon \approx T(E)D(E)\int_{E-0.5\Delta E}^{E+0.5\Delta E} N(\varepsilon)d\varepsilon \approx T(E)D(E)N(E)\Delta E = T(E)D(E)rEN(E) \quad \text{(II.4)}.$$

The values of T(E) and D(E) are in principle dependent on energy, however may be safely considered constant within the measured width of Auger spectral lines, thus being taken out of integration. Since in AES practically all of the information is extracted from narrow

spectral regions encompassing these lines, T(E) and D(E) may be considered as instrumental gain coefficients rather than real functions of energy. Also, the cylindrical mirror electron energy analyser (CMA) has constant r determined by its geometry. Therefore the energy distribution of electrons entering the analyser is measured in the form EN(E), since the measured signal is proportional to this product. Although it is not a problem to obtain a pure N(E) distribution via subsequent computer processing, it is traditionally accepted to use EN(E) for further spectroscopic analysis.

The EN(E) spectrum is a continuous distribution representing the electrons leaving the solid body as a result of irradiation by primary electrons. It has contributions from elastically scattered primary electrons, inelastically scattered primary electrons, secondary electrons and Auger electrons. The contribution from the latter is small comparative to others, so Auger spectral lines appear only as small peaks on the powerful background [63]. This is illustrated by fig. II.2, where the EN(E) spectrum of SiO_2 excited by 10 keV primary electrons is given. Three Auger transitions: Si(LMM), O(KLL) and Si(KLL) are visible together with their satellite structures. In order to eliminate the background and distinguish the Auger peaks better the I(E) raw data are differentiated:

$$dI(E)/dE = T(E)D(E)r[N(E) + EdN(E)/dE] \approx T(E)D(E)rEdN(E)/dE \quad (II.5).$$

The first term in square brackets is neglected, because it is much smaller than the second term in the spectral region approximately above 50 eV - where most of Auger peaks are found. The EdN(E)/dE distribution is called a differentiated spectrum and its example, obtained from data of fig. II.2, is given in fig. II.3.

There are two major characteristics of the peak in the differentiated spectrum as exemplified in fig. II.4 by the Si(KLL) peak, measured on pure Si excited by 10 keV primary electrons. The peak position on the energy scale is assumed to correspond to its most negative value, as shown by the dotted line. This characteristic is used for assigning any particular peak to the corresponding chemical element by comparison with the published or measured peak energies from elemental standards. The intensity of the peak (designated by the double-sided arrow drawn between two horizontal bars) is assumed to be

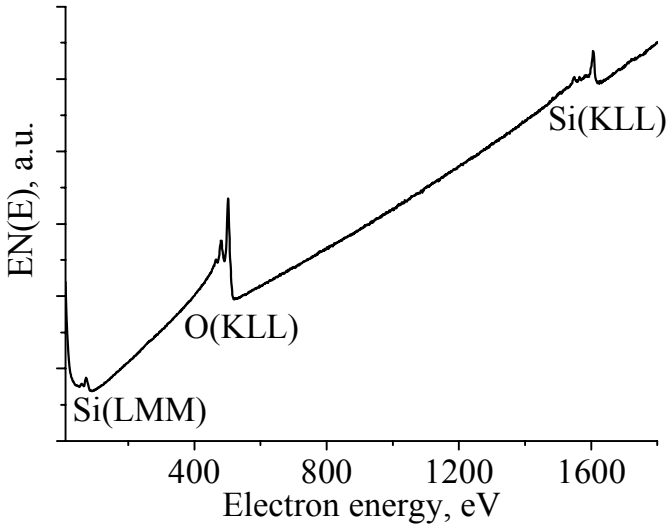


Fig. II.2. An example of EN(E) AES spectrum of SiO_2 excited by 10 keV primary electrons. Three Auger peaks are visible: Si(LMM), O(KLL), and Si(KLL).

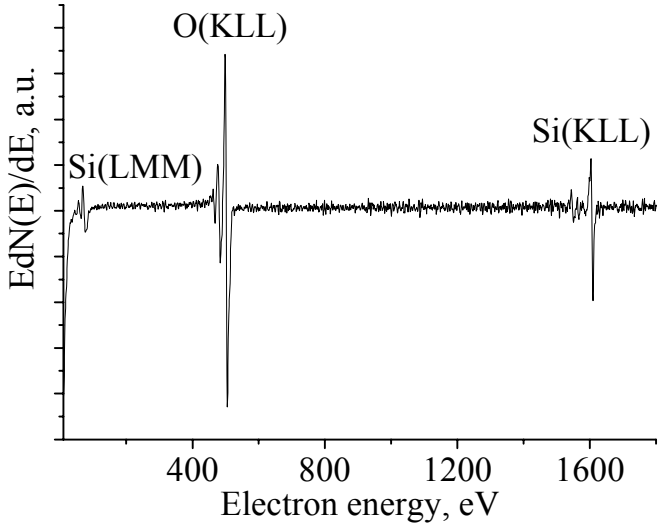


Fig. II.3. A differentiated AES spectrum of SiO_2 (obtained from data of fig. II.2). The background of non-Auger electrons is practically eliminated, leaving the Auger peaks nicely distinguishable.

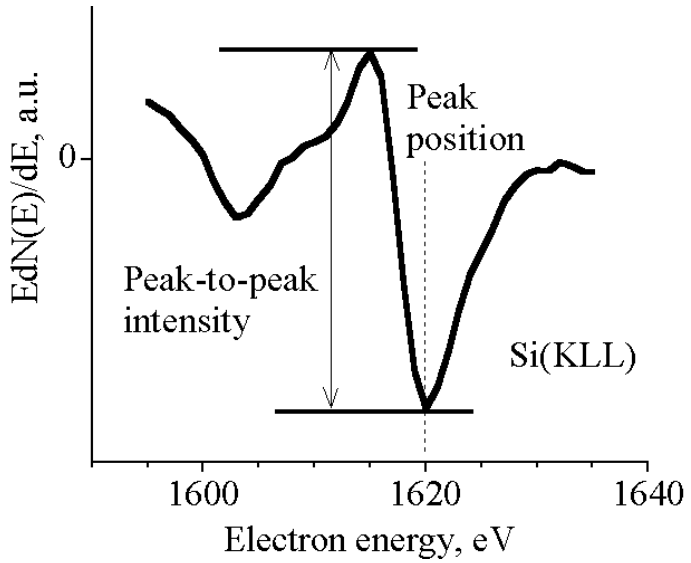


Fig. II.4. Si (KLL) AES peak and its two major characteristics. The peak position is the energy of the lowest signal value in the differentiated spectrum. The intensity is the difference between its highest and lowest values.

a height difference between its most positive and most negative values. This difference is called the peak-to-peak intensity [64] and is used to calculate atomic concentration of the element in the sample, as described in the following section.

II.1.c. Quantitative AES

The principal task of quantitative AES is to determine the atomic concentrations of all elements found in the investigated sample [65]. This is achieved through establishing the correlation between the atomic concentration of some element and the current of Auger electrons corresponding to it. The probability that an atom of a certain sort will be ionised per unit time is a product of the ionising electrons current density ρ_i in the point of atom's location and the ionisation cross-section $\sigma_A(E_p)$ for the core level A, giving rise to the Auger transition ABC. The number of atoms ionised per unit time and per unit depth of volume irradiated by primary electrons is $\rho_i\sigma_A(E_p)C(z)S$, where C(z) is an atomic concentration of the given atoms at a depth z below the surface and S is the surface area on which the primary electron beam is focused. When the primary electrons enter the analysed

sample and travel inside of it, some of them are reflected back, either elastically or inelastically but can still produce ionisation. These electrons are called backscattered electrons and cause the ρ_i to be larger than ρ_p - the current density associated with primary electrons. It is written in the form $\rho_i = \rho_p[1+R(E_p,E_{iA},\alpha)]$, where $R(E_p,E_{iA},\alpha)$ is called the backscattering factor depending on primary electrons energy E_p, ionisation energy E_{iA} of level A and the angle α of primary electrons incidence relative to the surface normal. One can therefore write the number of ionised atoms per unit time and per unit depth as $\rho_p[1+R(E_p,E_{iA},\alpha)]\sigma_A(E_p)C(z)S = I_p[1+R(E_p,E_{iA},\alpha)]\sigma_A(E_p)C(z)\sec\alpha$, where I_p is a primary beam current. The ionised atom will relax through Auger transition ABC and emit the Auger electron into the solid angle of the analyser's entrance aperture with probability P_{ABC}. The electrons originating in the solid body are attenuated exponentially with distance due to various scattering processes as they travel towards the surface. That is why Auger electrons emitted at different depths contribute differently to the stream of electrons departing from the surface. This effect is characterised by the inelastic mean free path $\lambda(E_{K(ABC)})$, which is the average distance that the electron with kinetic energy $E_{K(ABC)}$ will travel before being inelastically scattered. For most of Auger kinetic energies $\lambda(E_{K(ABC)})$ does not exceed 3÷5 nm, thus making AES essentially a surface sensitive technique. In order to get the current $N_{AES}(E_{K(ABC)})$ of Auger electrons from a certain element one should integrate over its concentrations at all depths weighed by appropriate attenuation factor. If β is the angle at which electrons leave the solid body relative to the surface normal, one can write:

$$N_{AES}(E_{K(ABC)}) = I_p[1+R(E_p,E_{iA},\alpha)]\sigma_A(E_p)P_{ABC}\sec\alpha\int_0^\infty C(z)\exp[-z\sec\beta/\lambda(E_{K(ABC)})]dz \quad (II.6).$$

A very important case is the homogeneous sample with concentration C independent on depth. Then the integration can be performed analytically and (II.6) will be transformed into:

$$N_{AES}(E_{K(ABC)}) = I_p[1+R(E_p,E_{iA},\alpha)]\sigma_A(E_p)P_{ABC}\sec\alpha C\cos\beta\lambda(E_{K(ABC)}) \quad (II.7).$$

This expression was used for calibration of spectrometer's sensitivity to any particular element through elemental standards. The total amount of electrons $N(E_{K(ABC)})$ entering the analyser with some particular energy $E_{K(ABC)}$ consists of Auger electrons given by (II.6) and of background electrons $N_{background}(E_{K(ABC)})$ originating from inelastic scattering processes. It has de facto proven impossible to remove the $N_{background}(E_{K(ABC)})$ contribution completely in a well defined and consistent manner. In the simplest (and most widely used) approximation it is considered that the background is a very weak function of energy in comparison with a rapidly changing Auger signal. Thus the $N_{AES}(E_{K(ABC)})$ will be a dominating contribution in the differentiated spectrum (II.5), where $N_{background}(E_{K(ABC)})$ can be neglected. The peak-to-peak intensity I_{ABC} described in the previous section is essentially a peak's energy multiplied by the sum of absolute values of slope on both sides of the peak in N(E) representation. This is exemplified by the O(KLL) peak shown in fig. II.5 in N(E) and EdN(E)/dE representations.

The peak has an asymmetric shape due to characteristic low energy tail on the left side of the peak due to Auger electrons which have lost some of their energy through inelastic collisions. These electrons are not counted in $N_{AES}(E_{K(ABC)})$, since scattering was explicitly taken into account in (II.6) and (II.7) through the parameter $\lambda(E_{K(ABC)})$. The area of the peak can be approximated by two right angle triangles drawn with solid lines on the N(E) plot. The basis of every triangle is equal to W_{ABC}, which characterises the natural peak width (provided the analyser's resolution ΔE is sufficient for not distorting the peak's shape). The hypotenuses are tangent lines to the N(E) curve in the maximum and minimum points of dN(E)/dE. In a simple approximation the area of such triangle (having the dimensionality of the number of electrons) is equal to $N_{AES}(E_{K(ABC)})$ - showing the number of electrons introduced above the background by the peak's presence. This area can be written as $0.5(W_{ABC})^2|dN(E_{max})/dE| + 0.5(W_{ABC})^2|dN(E_{min})/dE| = 0.5(W_{ABC})^2[dN(E_{max})/dE - dN(E_{min})/dE]$. Then using (II.5) one can write:

$$N_{AES}(E_{K(ABC)}) \approx 0.5 I_{ABC}(W_{ABC})^2/T(E_{K(ABC)})D(E_{K(ABC)})rE_{K(ABC)} \quad (II.8).$$

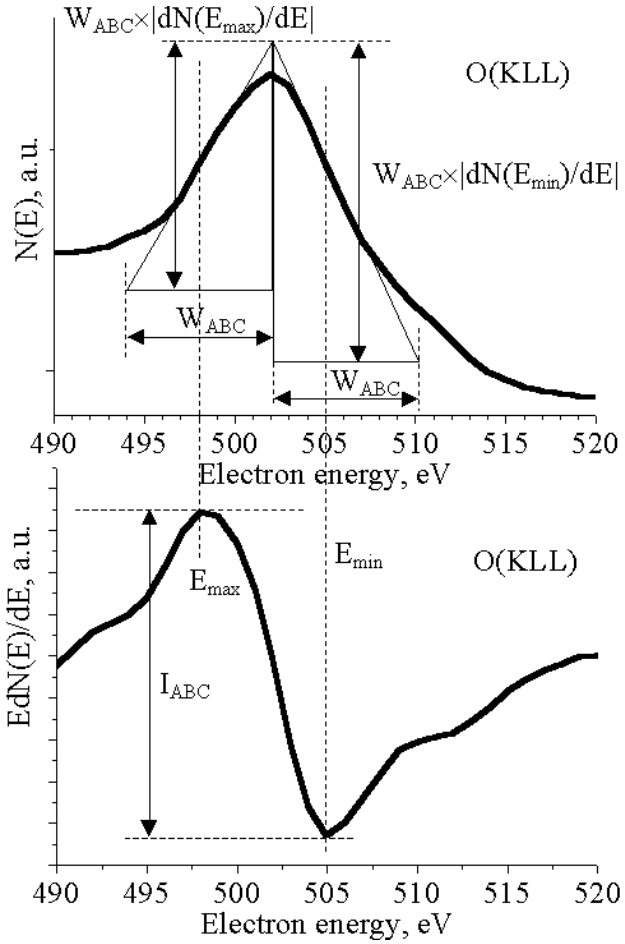


Fig. II.5. Estimation of O (KLL) peak area in the N(E) spectrum and its connection to peak intensity in the EdN(E)/dE spectrum. The intensity is proportional to the number of Auger electrons, which have not lost their energy.

Finally using (II.7) and (II.8) the following relation between the measured peak-to-peak intensity and the elemental concentration in the homogeneous sample can be established:

$$I_{ABC} = C[1+R(E_p,E_{iA},\alpha)] \times$$
$$\times 2I_p\sigma_A(E_p)P_{ABC}\sec\alpha\cos\beta\lambda(E_{K(ABC)})T(E_{K(ABC)})D(E_{K(ABC)})rE_{K(ABC)}/(W_{ABC})^2 \quad \text{(II.9)}.$$

The proportionality coefficient between I_{ABC} and C can be divided into two parts: the instrumental factor $F_{ins} = 2I_p\sec\alpha\cos\beta T(E_{K(ABC)})D(E_{K(ABC)})r$ (containing the quantities which can be changed or vary as experimental parameters for different spectrometers) and

sensitivity factor $S_{ABC}(\text{element}) = [1+R(E_p,E_{iA},\alpha)]\sigma_A(E_p)P_{ABC}\lambda(E_{K(ABC)})E_{K(ABC)}/(W_{ABC})^2$ (containing the quantities which can not be changed and characterise the effectiveness of detecting some particular element with Auger transition ABC). Thus (II.9) can be rewritten as:

$$I_{ABC} = CF_{ins}S_{ABC}(\text{element}) \quad \text{(II.10)}.$$

It is important to note that expressions (II.9-10) are based on (II.7) and therefore valid only for the homogeneous sample. Expression (II.10) was used for quantitative AES analysis throughout the present work. First $F_{ins}S_{ABC}(\text{element})$ products were determined for every element of interest, using homogeneous standards with known concentrations. Whenever possible, pure elemental standards were used (for example metals or silicon), but in the case of gases (oxygen, nitrogen) well defined compounds (like silicon dioxide or silicon nitride) were utilised. Every standard sample was measured together with the Si standard under identical conditions (with equal instrumental factors). Then, all elemental sensitivities were referenced to Si or in other words the ratio of products $F_{ins}S_{ABC}(\text{element})/F_{ins}S_{KLL}(\text{Si}) = S_{ABC}(\text{element})/S_{KLL}(\text{Si})$ were calculated and stored in the processing database. This had an advantage of removing the instrumental factor and extracting the sensitivity factors independent of experimental conditions or instrumental parameters. When the unknown sample was investigated, its chemical composition was represented through partial concentrations C_α expressed in atomic percents - meaning the percentage of atoms of type α among all other species occurring in the sample. According to (II.10) the partial concentration is equal to:

$$C_\alpha = 100\times I_\alpha/[F_{ins}S_\alpha(\Sigma I_\beta/F_{ins}S_\beta)] = 100\times[I_\alpha/S_\alpha]/[\Sigma I_\beta/S_\beta] \equiv$$
$$\equiv 100\times I_\alpha\times[S_\alpha/S_{KLL}(\text{Si})]^{-1}\times[(\Sigma I_\beta/S_\beta)S_{KLL}(\text{Si})]^{-1} \quad \text{(II.11)}.$$

The summation inside of the brackets is done over all elements which are found in the sample and included into the quantification calculation. In (II.11) the first transformation is possible because during measurement of every particular sample the experimental

conditions (and thus instrumental factor) are not changed and the second transformation is a trivial division of denominator and enumerator by $S_{KLL}(Si)$ aimed to make use of the ratios recorded in the processing database. The final form of (II.11) establishes a direct relation between the peak-to-peak intensity I_α of the given Auger transition of element α and its partial concentration inside of the sample. This relation was universally used for quantification of AES data into chemical composition throughout this work.

II.1.d. AES experimental setup

A commercially available "PHI 670 Auger Nanoprobe" system from Perkin Elmer Physical Electronics was used in this work [66]. This system features the Auger spectrometer combined with the scanning electron microscope (SEM) housed in the ultra-high vacuum (UHV) chamber with background pressure in the $10^{-10} \div 10^{-11}$ mbar range. The sample exchange could be conducted via a loadlock without breaking the vacuum in the main chamber. The Schottky thermal field emitter was used as a source of primary electrons. It had a zirconiated single crystal tungsten tip operating at a temperature of 1800°K. The primary electrons were focused on the analysed sample by the electron optics column with the possibility of scanning over the sample's surface. This allowed to operate the column in the SEM mode, which was used for observation of sample's surface and selecting an appropriate part of it for analysis. The kinetic energy of primary electrons could be set anywhere between 0 eV and 20 keV. The AES analysis was performed using 10 keV primary beam at 30° angle of incidence, typically with a current of 100 nA rastered over the area $20 \times 30\ \mu m^2$. The analyser was of cylindrical mirror type (CMA) with the multichannel plate electron detector. The energy range accessible to the given CMA is from 0 eV to 3200 eV and the resolution is better than 0.6% (r = 0.006). AES depth profiling was performed in cycles of interchanged ion sputtering and recording preselected spectral regions, which contained Auger peaks of the elements of interest. During every cycle some layer of sample's material was sputtered away and elemental concentrations were determined on exposed surface. In this way the elemental distributions as a function of depth inside the

sample, or AES depth profiles (ADPs), were obtained. The sputtering was performed by a differentially pumped ion gun, which produced a beam of Ar^+ ions with kinetic energy up to 5 keV. If not stated otherwise, 1 keV energy and ~55° angle of incidence were used. The ion beam was focused and rastered in the sample surface plane over several mm^2 in order to eliminate the crater edge effects on the ADPs.

II.1.e. Related technique: X-ray photoelectron spectroscopy

The X-ray photoelectron spectroscopy (XPS) [63-65] is an analytic technique closely related to above described AES. Both share similar parts of instrumentation, employ similar data evaluation methods, and pursue a similar goal of elemental analysis on surfaces. The XPS is based on the photoeffect, namely a process of atom ionisation by means of photon absorption. The ejected electron is called photoelectron, and measuring its kinetic energy E_{kin} allows for chemical identification of the atom of origin, provided the initial photon energy ω is known. According to the law of energy conservation one can write:

$$\omega + E_A = E_{kin} + E_I \quad \text{(II.12)},$$

where E_A and E_I are the full energies of the atom and the ion respectively. Since the binding energy of the electron $E_B = E_I - E_A$, a well known photoeffect equation is obtained:

$$E_B = \omega - E_{kin} \quad \text{(II.13)}.$$

The binding energy changes only slightly due to atom's surrounding, thus reflecting the specifics of chemical bonding. The chemical state of the atom (e.g. oxidised or not, etc) is more straightforward to interpret than in AES, since only one atomic level is involved, as compared with three in (II.1). Since binding energies are the "fingerprints" of chemical elements, both qualitative and quantitative elemental identification is possible. In this

respect XPS has approximately equal power as AES does. Due to the same reason as AES (see II.1.c), the XPS is also surface sensitive, being able to analyse only a few atomic layers under the specimen surface. An important difference between two techniques is the lateral resolution, or the smallest area which can be analysed. Due to a far better ability to focus electrons than X-rays, a sharply focused primary electron beam is easily produced. This brings a lateral resolution of modern AES spectrometers deep into sub-μm region, while XPS spectrometers reach several dozens of μm at best. Therefore, one can not use the XPS for analysis of chemical composition in device-size areas of modern ICs.

In the present work the XPS analysis was performed using the "PHI Model 5600 MultiTechnique System". In this system the X-ray source, the sample, and the electron energy analyser are housed in the UHV chamber, thus ensuring ultra-clean conditions for chemical analysis. A K_α line of X-ray radiation originating from Al anode due to electron bombardment ($\omega \sim 1486.5$ eV) is used to excite the photoelectron spectrum. The kinetic energy of photoelectrons is measured by spherical capacitor electron energy analyser. When it was necessary to investigate some layer inside the sample at a depth larger than the photoelectrons escape depth, an ion sputtering of sample material was used. This was done with Ar^+ ions having 4 keV kinetic energy and bombarding the sample at an incidence angle of 45° to the surface normal. In this way the sample was gradually eroded, thus exposing deeper layers for chemical analysis.

II.2. Scanning tunnelling microscopy

A scanning tunnelling microscope (STM) is a tool which allows to investigate the surface topography of conducting and semiconducting samples [34,67]. It has an extremely high spatial resolution, namely on the order of 0.1 nm in the surface plane and on the order of 0.001 nm perpendicular to the surface. Due to these parameters it becomes possible to observe the arrangement of individual atoms. The STM was invented in 1982 by G. Binnig and H. Rohrer, for which they were awarded the 1986 Nobel Prize in physics [68]. Now almost 20 years since its creation, the STM is a standard analytical tool for every surface

science lab. Hundreds of both commercial and home-made instruments are used throughout the world for fundamental research, but the application of this technique in an industrial environment is nevertheless extremely limited.

II.2.a. Physical background of STM

The operation of STM is based on the tunnelling effect, which is a manifestation of the wave-particle duality. The tunnelling effect is a process when the quantum particle traverses the region of space where its full energy is smaller than its potential energy. This region of space is called the potential barrier, which is characterised by its shape (spatial configuration of the region) and height (the value of the potential energy). Fig. II.6 shows a one-dimensional barrier between two metal electrodes, separated by the distance d. In the STM terminology these two electrodes are called sample and tip, and are characterised by workfunctions ϕ_s and ϕ_t, and by the electronic densities of states $\rho_s(E)$ and $\rho_t(E)$. The latter are functions of electron's full energy referenced to the Fermi level of each particular electrode. Fig. II.6a corresponds to the situation when no electrical potential difference is applied between the electrodes. In this case the Fermi level E_f has equal positions in the sample and in the tip, therefore electrons do not tunnel between them. Fig. II.6b shows the case when a potential difference V is applied between the tip and the sample. Now the electrons can tunnel from the occupied states of the negatively biased electrode into the equienergetical vacant states of the positively biased electrode. As a result, an electric current, which is called the tunnelling current, is flowing between the tip and the sample. For barrier in fig. II.6 and when the voltage V is applied to the sample the tunneling current is expressed in the following way (m is electron's mass) [69]:

$$I_t \sim \int_0^{eV} \rho_s(E)\rho_t(E-eV)\exp(-2dm^{1/2}h^{-1}[\phi_s + \phi_t + eV - 2E]^{1/2})dE \quad \text{(II.14)}.$$

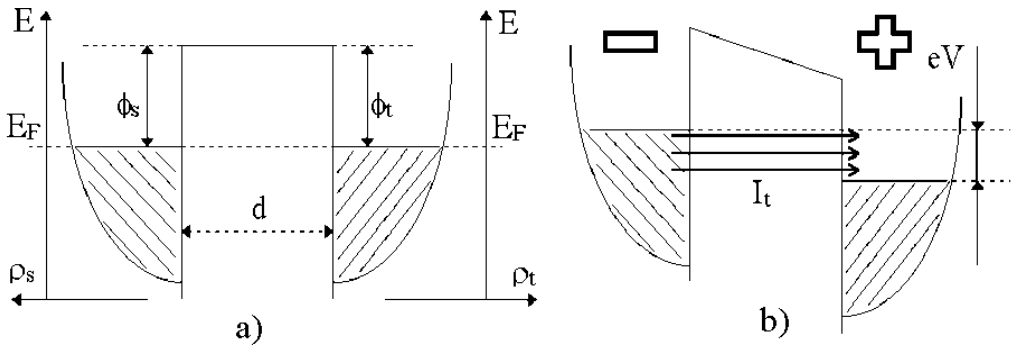


Fig. II.6. A one-dimensional tunnelling barrier between two metal electrodes. a) The case of zero potential difference between the electrodes. The electrons can not tunnel, because no occupied states (cross-hatched areas on the ρ(E) distributions) are energetically aligned with the empty states on the other side of the barrier. b) The case of potential difference V applied between the electrodes. The electrons from occupied states of the negative electrode can tunnel into empty states of the positive electrode.

II.2.b. Principles of STM operation

The schematic structure of STM is shown in fig. II.7 [70]. Usually, the sample (metal or semiconductor) has a relatively flat surface and the tip is an extremely sharp metallic needle (ideally atomically sharp). The tip is attached to a piezoelectric device, called scanner. It is built of piezoelectric crystals covered with metal electrodes, and it is possible to move the tip independently in three orthogonal directions by applying appropriate voltages to different electrodes. The tip is brought into sample's proximity, so that its apex is roughly 1 nm away from the surface. At this distance a measurable I_t will flow between the tip and the sample under a bias voltage of just a few Volts or even lower. When a desired value of I_t is obtained, the tip is moved parallel to the surface (x and y directions) in a raster-like manner by applying corresponding voltage sequences to the scanner. These x(t) and y(t) voltage sequences are supplied independently by the scanning voltage generator. The measured I_t value is fed into the feedback system, which compares it with the pre-set value I_0. According to (II.14), I_t depends exponentially on sample-tip separation d, and it changes very dramatically due to the slightest variations in sample's topography as a function of lateral coordinates z(x,y). When $I_t > I_0$ the feedback system

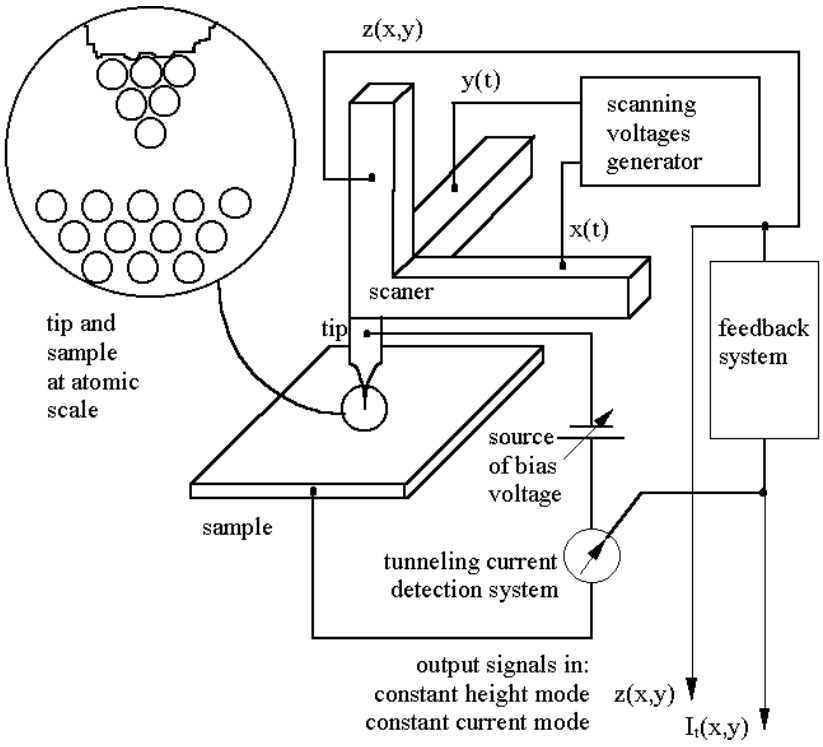


Fig. II.7. Schematic structure of STM. The tip is attached to the piezoelectric scanner, which is being fed by the scanning voltages generator. The tunnelling current is measured in the circuit of the tip, sample, and the bias voltage source. The value of the current controls the response of the feedback system, which adjusts the tip-sample separation.

supplies such a voltage to the scanner, that it retracts the tip from the surface. On the contrary, when $I_t < I_0$ - the tip is moved closer. As a result, the tip-surface separation is kept constant, and the tip's trajectory z(x,y) reflects the surface topography during scanning. When the tip is sharp enough, atomic resolution can be achieved when the surface image is constructed from the z(x,y) map. The described mode of STM operation is called the constant current mode. An alternative way to operate the STM is the so-called constant height mode. Then the tip is rastered along x and y co-ordinates, while its z co-ordinate is kept constant. The information about the surface topography can be obtained as $z(x,y) \sim \ln[I_t(x,y)]$, again due to exponential dependency of I_t on d. In this work all STM experiments were conducted in the constant current mode.

II.2.c. STM experimental setup

A homemade STM system with completely computerised electronic data acquisition was used in this work [71]. It had a maximum scanning range of ~1.5 μm along x and y axes and the same range of z movement. The STM head was mounted on a standard 6-inch conflat-type flange and placed in the UHV chamber with a base pressure of 2×10^{-10} mbar. This chamber also contained the CMA type AES spectrometer, facilities for electron bombardment of samples and tips, and the metal evaporator with quartz microbalance. The tips and samples could be transferred through the load-lock, without breaking vacuum in the main chamber. The tips were formed by electrochemical etching in the NaOH solution using a W wire 0.2 mm in diameter. Such tips were annealed by electron bombardment, usually done with current of several mA and accelerating voltage of 2÷3 kV. Annealing was continued until all W oxide was desorbed and stable tunnelling could be achieved during scanning.

Chapter III

New features in atomic structure of the Si(100)-c(4×4) reconstruction

III.a. The c(4×4) reconstruction of the Si(100) surface

The c(4×4) reconstruction of the Si(100) surface has become an object of intensive research in the recent years [30,33,72-106]. The attention is attracted to it because Si(100) is a technologically important surface in semiconductor industry, while for decades the (2×1) reconstruction seemed to be its lowest energy ground state. Since the early theoretical prediction by Pandey [76], the Si(100)-c(4×4) reconstruction was observed after various treatments of Si(100) samples in ultra-high vacuum (UHV) environment. Reported procedures of obtaining this structure always include annealing in the temperature range of 550°C÷700°C, but differ in species which are admitted to the surface if any. Namely, Wang et al [76], Lin et al [77], Nörenberg et al [78-79], and Miki et al [80] obtained the c(4×4) reconstruction by annealing the Si(100) surface in the UHV background atmosphere, while Ide et al [81], Uhrberg et al [82], and Kato et al [83] used interaction with hydrogen, Men et al [84] - oxygen, Zhang et al [85] - silicon homepitaxy, Goryachko et al [72-73], Miki et al [86], and Wasserfall et al [87] - bismuth, Butz et al [88], Shek [89], and Leifeld et al [90-91] - carbon, Chen et al [92] – fullerenes, Lin [93] - disilane, Shek [89], Kosugi et al [94], Takaoka et al [95], Ikeda et al [96], Stoffel et al [97], and Simon et al [98] - ethylene, Wang et al [99-100] - diborane or decaborane, Moriarty et al [101] - sulphur, Hatayama et al [102] – DMGe, Saranin et al [105] - antimony, Wasserfall et al [III.18] – arsenic or antimony, Sakai et al [106] - carbon and germanium. The formation of the c(4×4) structure in the temperature range mentioned above makes it noteworthy in the light of Pr_2O_3 epitaxy prospects on the Si(100) surface. The latter proceeds in the 625°C÷725°C temperature range [20] and is aimed at achieving a high quality Pr_2O_3/Si(100) interface. Therefore it is desirable to establish an atomic model of the c(4×4) reconstruction and determine whether it is better or not as a substrate for growth than the (2×1) dimer row structure.

No matter of the widest preparation procedure variations, there exists universal agreement about the c(4×4) patterns in STM, LEED or any other technique, whatever is used for surface characterization. This gives grounds to believe, that it is essentially the same Si(100)-c(4×4) structure observed after different sample treatments. No consensus is achieved about the atomic arrangement in this surface structure and what causes it to stabilize in favor of the more familiar Si(100)-2×1 dimer row structure, though carbon is most often recognized as such [78-80,88-92,94-98,103-104]. Consequently, five principally distinctive and competing models with [78,90,98] and without [76,82] carbon are most often used for interpretation of experimental data. The missing dimer model by Wang et al [76] considers the (2×1) dimer rows with dimer vacancies ordered in the c(4×4) manner. Nörenberg et al [78] had proposed a refined missing dimer model where the dimer vacancies are combined with carbon atoms in the 4^{th} subsurface layer. Both models based on dimer vacancies stand in contradiction to the results of Ide et al [81] and Stoffel et al [97], who studied the interaction of the Si(100)-c(4×4) surface with hydrogen. These studies [81,97] strongly suggest that the Si(100)-c(4×4) structure is formed by surface dimers, which hydrogen can break. The mixed ad-dimer model by Uhrberg et al [82] deals with the parallel and perpendicular silicon ad-dimers on the defectless Si(100) surface and gives a good account of all the features observed in the STM images. Leifeld et al [90] had proposed a model of the defectless Si(100) surface, where silicon is substituted by carbon in some surface dimers and subsurface locations. Finally, the most recent model by Simon et al [98] suggests the presence of C in subsurface locations as well as on the surface in the form of Si-C heterodimers (in the ordered mixture with the same amount of Si-Si homodimers). The models by Leifeld et al [90] and Simon et al [98], however, account for only half of the features in STM images which are explained by the mixed ad-dimer model [82].

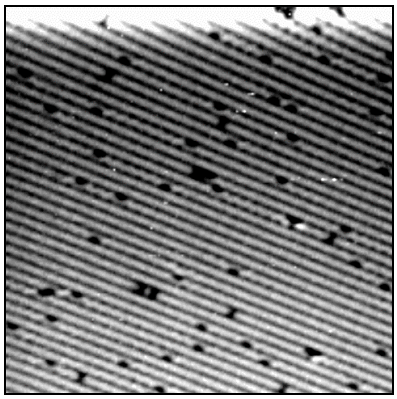
In the present work the Si(100)-c(4×4) reconstruction was encountered while studying the behavior of submonolayer Bi films on the Si(100) surface [72,73,107]. The interaction with Bi was chosen as the technically simplest technique to obtain the c(4×4) reconstruction, since very long annealing times are required to achieve it if no adsorbates are being used [77]. An observed c(4×4) structure turned out to be identical to what other researchers detected [76-102,105-106] and in particular to what Miki et al [86] and Wasserfall et al [87] had seen after the Si(100) surface interacted with Bi. In

the meantime, some evidence [33,74-75] about its behavior and features of STM appearance were not reported by other authors. Moreover, this evidence did not fit into the framework of the known c(4×4) reconstruction models [76,78,82,90,98]. Therefore, the purpose of the current investigation was to analyze possible atomic arrangements on the Si(100) surface, which could be compatible with all experimental data on the Si(100)-c(4×4) reconstruction. As a result, a new atomic model is suggested (named refined mixed ad-dimer model), which will be described below. This model will be discussed in connection with possible stabilization mechanisms of the Si(100)-c(4×4) reconstruction.

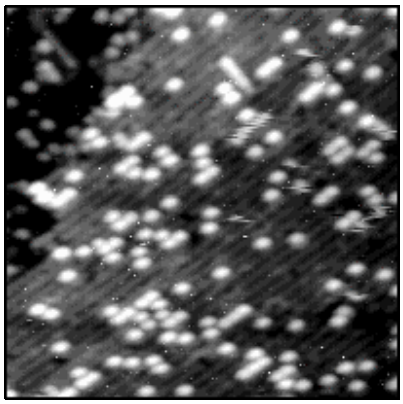
III.b. Interaction of submonolayer Bi films with the Si(100) surface and formation of the c(4×4) reconstruction

The Si(100) samples used in the experiments were phosphor doped (4.5 Ohm×cm) and were prepared by ex-situ rinsing in acetone and hydrofluoric acid immediately before loading into the load lock of the UHV chamber. In-situ they were thermally treated by electron bombardment from the back side in the following stages: outgassing at 650°C for several hours, annealing at 1200°C for one minute, rapid quenching to 900°C and cooling down to room temperature over half of an hour. The base pressure in the chamber did not exceed 2×10^{-10}mbar and it was always kept below 1×10^{-9}mbar during annealing, quenching and cooling the sample. The above described preparation procedure always allowed to obtain the typical Si(100)-2×1 surface, like the one shown in fig. III.1a, and it was characterized by the ratio of peak-to-peak intensities in the differentiated AES spectrum Si(LMM, 92eV)/C(KLL, 272eV) equal to 800÷900. Bi was evaporated on this surface kept at room temperature and the deposited amount was controlled by a quartz micro-balance.

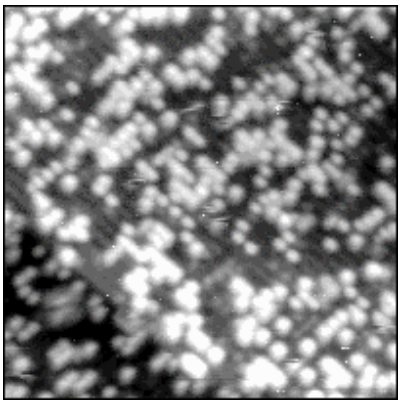
Fig. III.1 displays the images of two submonolayer bismuth coverages: b) θ_{Bi}=0.06ML and c) θ_{Bi}=0.15ML (1ML=6.8×10^{14}atoms/cm^2 - surface atomic density on the Si(100) crystallographic plane). It is immediately seen that bright blobs appear on the background of Si(100)-2×1 reconstructed dimer rows structure. Counting the number of blobs yields half the number of atoms corresponding to the nominal



(a)



(b)

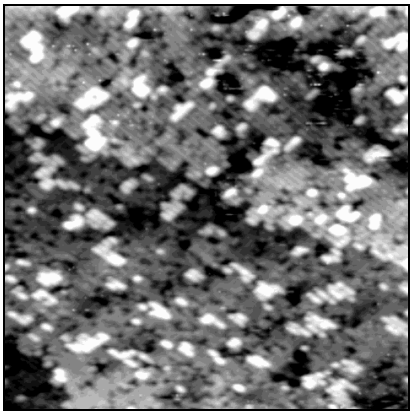


(c)

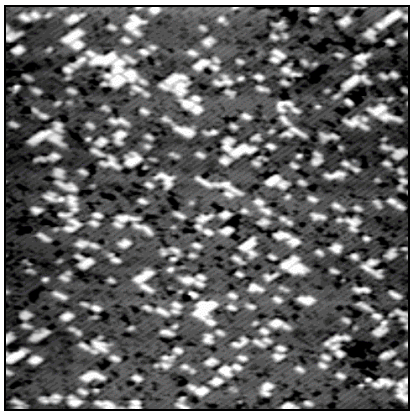
Fig. III.1. a) Clean Si(100)-2×1 surface, 28×28nm^2, U=−1.5V, I=56pA; b-c) Submonolayer Bi films deposited on Si(100)-2×1 at room temperature (bright blobs correspond to Bi dimers), b) 28×28nm^2, U=−1V, I=96pA, θ_{Bi}=0.06ML; c) 28×28nm^2, U=−1.3V, I=96pA, θ_{Bi}=0.15ML.

coverage, thus clearly indicating that each blob corresponds to a single bismuth dimer. Another important observation is that most of the dimers remain unordered [72,107]. There are no large islands (more than several dimers in size) of (2×1) or (2×2) ordered bismuth phases [108], which form when θ_{Bi}≥0.2ML is deposited at room temperature [109-110].

After taking the STM images of as deposited bismuth films, they were annealed at ≈400 ^{0}C for several minutes. The resulting surface morphologies are shown in fig. III.2. One can judge, that bismuth dimers coalesce into squarely shaped islands, thus nucleating an ordered (2×1) phase. This result is in agreement with other works [110-112], where thermally activated ordering of larger Bi amounts into the (2×1) phase was also observed. One can also judge that a substantial amount of vacancy defects are formed in the course of annealing [72,107]. A small number of defects is already present on the initial clean surface (fig. III.1a), appearing as dark holes in the (2×1) reconstructed dimer rows structure. At fig. III.2 the number of defects is several times greater, they are unordered and some of them gather into clusters. Vacancy formation is attributed to the interaction between the Bi atom and the Si atom, which causes the latter to leave its lattice site with higher probability. It is noteworthy that very similar



(a)



(b)

Fig. III.2. The same submonolayer Bi films as in figs. III.1.b-c, but annealed at 400 ^{0}C after deposition. The Bi dimers coalesce into rectangular-shaped islands of the (2×1) adsorbate phase. a) 55×55nm^2, U=–1.5V, I=236pA, θ_{Bi}=0.06ML; b)55×55nm^2, U=–1.5V, I=147pA, θ_{Bi}=0.15ML.

defects were observed in the case of Sb on Si(100)-2×1 [113].

The next stage of investigation was to desorb bismuth from the surface, by heating the sample to ≈600 ^{0}C, and examine its subsequent condition. The overall topography of the silicon surface after this treatment is shown in figs. III.3a-b, where the same area is imaged in occupied and empty states correspondingly. One can see the reconstructed dimer rows structure with numerous vacancies grouped into clusters, not inherent to the starting surface [72,107]. The bright protrusions appearing in the empty states image are not the real adsorbates, since they look like slight depressions in the occupied states. Such objects are known as C-type defects [114] and they always appear on the Si(100)-2×1 surface. In order to investigate the vacancy clusters in more detail, we took the images of another smaller area, containing two large clusters. Its images in the occupied and empty states are given in figs. III.3c-d correspondingly. Because of

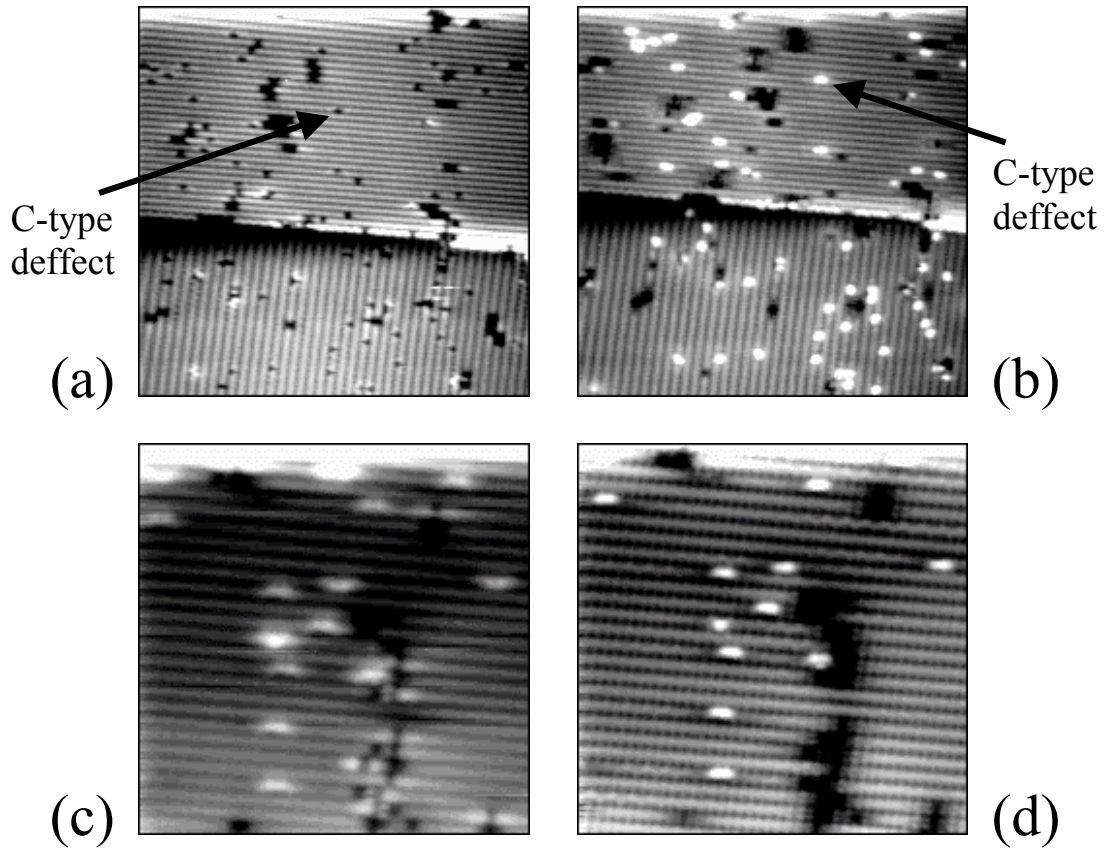
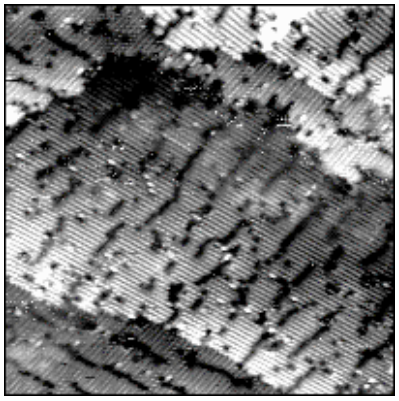


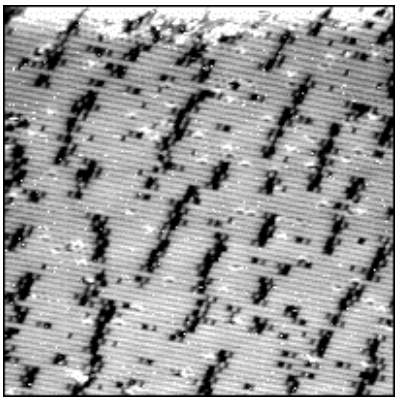
Fig. III.3. Vacancy clusters appear on the Si(100) surface after bismuth desorption (initial Bi coverage 0.09ML). a) 31×31nm^2, U=–1.0V, I=644pA; b) 31×31nm^2, U=1.0V, I=682pA; c) 16×16nm^2, U=–0.8V, I=330pA; d) 16×16nm^2, U=0.6V, I=1396pA.

using low sample bias voltage, C-type defects look like protrusions on both images, but the empty states image is more sharp. The most interesting feature is that vacancy clusters are "filling up", when the bias is switched from positive to negative one. They are characterized by a local density of electronic states, different from the surrounding surface areas, thus causing substantial change in appearance when the tunneling voltage is altered. It is possible that Si, C, or even residual Bi atoms (at coverage below the detection limit of AES) are filling up the vacancies - leading to the observed images.

In contrast to ultra-low initial Bi amounts, thicker films (θ_{Bi}>0.2ML) interact with the Si(100) surface in a qualitatively different way. As an illustration, fig. III.4a shows an image of the sample after 0.69ML of Bi was deposited and desorbed. Now, instead of vacancy clusters, the vacancy lines are formed on the surface, giving rise to the local (2×n) reconstruction [72,107]. It is interesting to compare it with those on the Si(100) surface contaminated by a small amount of Ni, (fig. III.4b). Such contamination



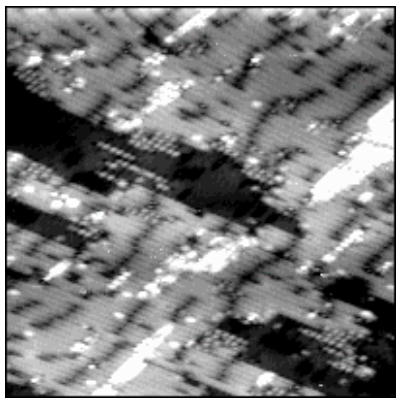
(a)



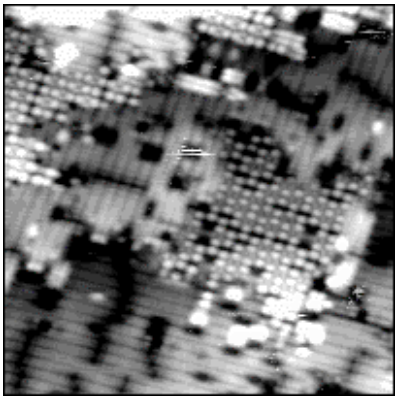
(b)

Fig. III.4. a) Si(100) surface after deposition and thermal desorption of 0.69ML of Bi, 54×54nm^2, U=1.0V, I=60pA. The vacancies are grouped into lines, thus forming a (2×n) structure; b) Comparative image of the Ni-contaminated Si(100) surface; 39×39nm^2, U=–2.0V, I=125pA.

resulted simply from handling the sample with stainless steel tweezers. While the vacancy lines show certain similarity, an important difference is that Ni contamination can not be eliminated by thermal annealing and the sample always displays the (2×n) pattern. At the same time, the (2×n) structure which resulted from Bi preadsorption is



(a)



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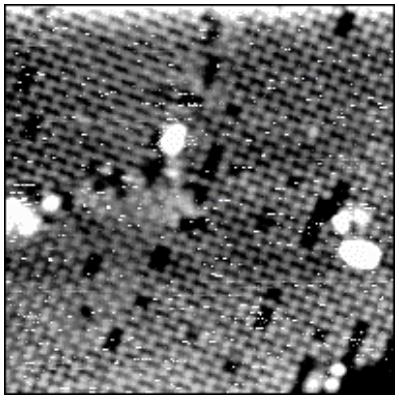

(c)

Fig. III.5. Subsequent stages of Si(100)-2×n→Si(100)-c(4×4) phase transition. The images were taken at 20 ^{0}C in between heating cycles at 600÷700 ^{0}C. a) 40×40nm^2, U=1.5V, I=41pA, nucleation of c(4×4) islands; b) 28×28nm^2, U=1.5V, I=90pA, c(4×4) patches grow in size; c) 28×28nm^2, U=1.0V, I=50pA, c(4×4) reconstruction covers the entire surface.

completely removed after annealing at 1200 ^{0}C, and the initial surface identical to those in fig. III.1a is completely restored.

Finally, if the initial amount of deposited Bi was ≥0.25÷0.3ML, then further annealing at 600÷750 ^{0}C, caused the phase transition between the Si(100)-2×n and the Si(100)-c(4×4) [72-73]. Three subsequent stages of this transition, starting from nucleation of the c(4×4) patches until it covers the entire surface, are shown in fig. III.5a-c. The total annealing time required to complete the transition was no more than half an hour. Comparing this with annealing of initially clean Si(100)-2×1 surface [77], one can judge, that preadsorbition of Bi reduces this time by one order of magnitude. The surface in fig. III.5c was stable to annealing at temperatures up to 750 ^{0}C, and did not show signs of reverse transition into the (2×1) or (2×n) states. However, if heated to 800 ^{0}C, the surface developed a large scale roughness and appeared to be disordered. Annealing the sample at 1200 ^{0}C restored the initial (2×1) structure, like shown in fig. III.1a. When the entire surface was covered with the c(4×4) phase the ratio of intensities Si(LMM, 92eV)/C(KLL, 272eV) was equal to 300. The threefold increase of carbon concentration could not be avoided and was attributed to contamination from the parts of sample holder and manipulator during annealing cycles.

III.c. Previously reported features of the Si(100)-c(4×4) structure

In this work an extensive STM investigation of the Si(100)-c(4×4) structure was performed [33,72-75] and a large amount of images was obtained which are similar to what is widely published in the literature by other authors [77-79,81-82,85-86,88,90-93,98-101]. Figs. III.6a-d show the appearance of the well known c(4×4) structure under different tunneling voltages (all four images show the same location on the surface). In fig. III.7a the registry of the brightness maxima for the empty states image taken at tunneling voltage U_t = 1.0 V (fig. III.6a) is presented. The image consists of pairs of brightness maxima (designated as D maxima [82]) and these pairs form a c(4×4) lattice relative to the unreconstructed Si(100) surface. At U_t = 1.5 V (fig. III.6b) another features appear in the empty states image (designated as C maxima [82]). They are less bright than the D maxima and their relative location is given in fig. III.7b. The C

maxima also form pairs but these pairs are very often missing, thus producing two modifications of the surface lattice: α-c(4×4) – consisting of C and D maxima and β-c(4×4) – consisting of only D maxima. The same two unit cells of different modifications are outlined on the images in figs. III.6a-d. Both modifications have 2mm point group symmetry (second order rotation axis and two mirror planes, shown in fig. III.7a). The filled states images of the c(4×4) structure at U_t = -1.0 V (fig. III.6c) and U_t = -1.5 V (fig. III.6d) are not so sharp as the empty states images. Fig. III.7c shows the registry of the features in the filled states image, consisting of bright A features and less intensive B features [82]. Every A feature corresponds to a pair of C maxima and every B feature is a poorly resolved pair of D maxima. All maxima are of the same brightness within every particular pair with the only possible exclusion of under-compensated surface tilt. The physical equivalence of the maxima within pairs was one of the basic ingredients in existing models of the Si(100)-c(4×4) reconstruction [76,78,82,90,98].

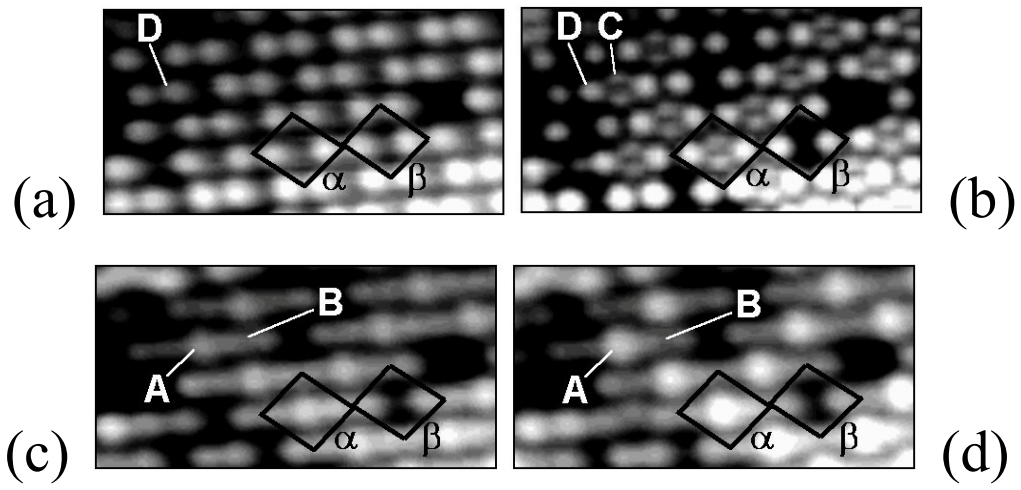

Fig. III.6. Typical STM images of the Si(100)-c(4×4) surface at different tunneling voltages. All images show the same surface area which is 7×3.5nm^2 in size, and the sample bias voltages are: 1.0V (a), 1.5V (b), −1.0V (c), −1.5V (d). The images are slightly distorted due to thermal drift and unequal piezoscanner sensitivity in different directions.

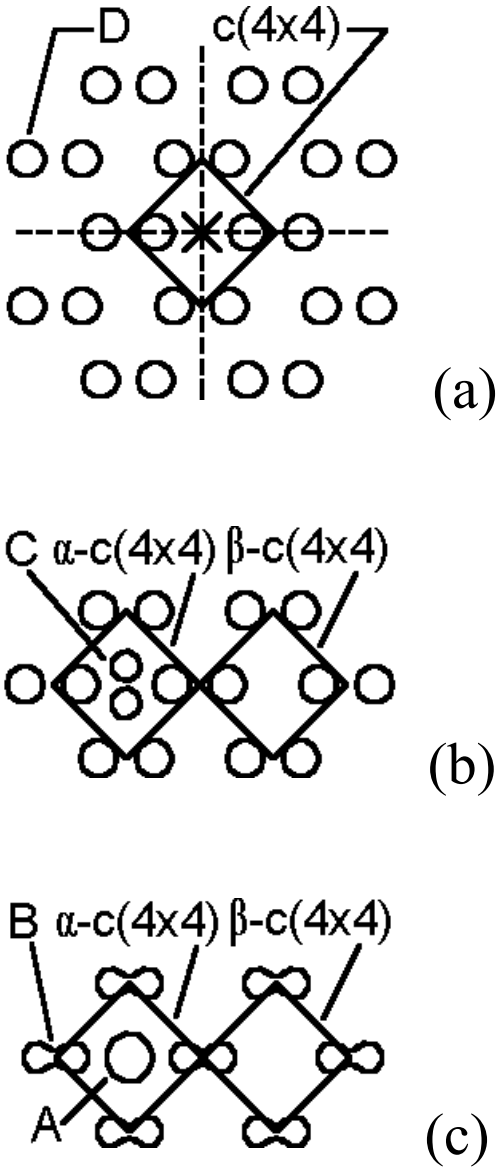

Fig. III.7. The registry of the brightness maxima in empty states STM images from fig. III.6 at 1.0V (a), at 1.5V (b), and in occupied states STM images from fig. III.6 (c). The elements of 2mm point group symmetry are shown in (a): dashed lines are intersections of mirror planes with the plane of the drawing and the cross is the intersection of the second order rotation axis with the plane of the drawing.

III.d. Novel features of the Si(100)-c(4×4) structure

In the following I present STM images of the Si(100)-c(4×4) structure [33,74], which were not previously reported in the literature by other authors. These images show a lattice of different symmetry than described in the previous section. Figs. III.8a-b

show the same area on the Si(100)-c(4×4) surface, with the same two neighboring unit cells being outlined. The empty states image in fig. III.8a (obtained at U_t = 1.0 V) strongly differs from those in figs. III.6a-b, while the filled state image in fig. III.8b (obtained at U_t = -1.7 V) looks similar to the images in figs. III.6c-d. Fig. III.8c shows the registry of intensity maxima in fig. III.8a, which are now of two types D1 (stronger) and D2 (weaker). The maxima form pairs, which are arranged in the c(4×4) lattice, each consisting of one D1 and one D2 maximum. Due to the correlated placement of different maxima inside the pairs, the point group symmetry of the lattice is now 1m –

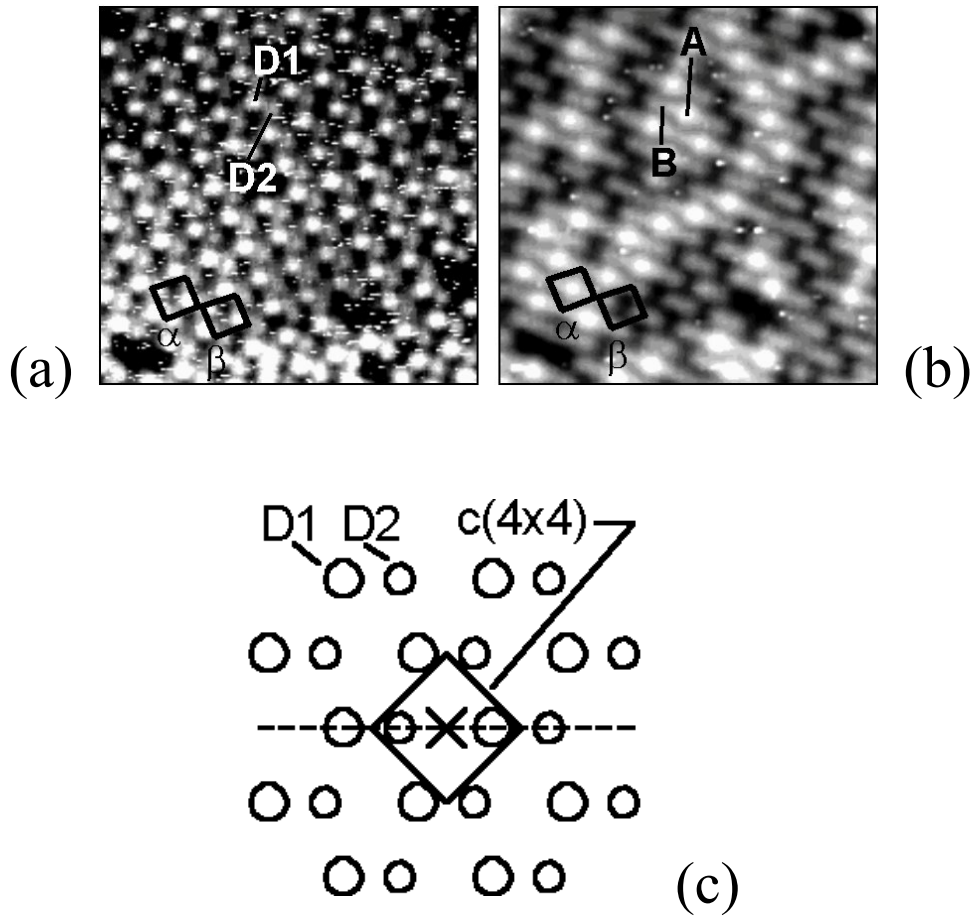

Fig. III.8. STM images of the Si(100)-c(4×4) structure showing lowered symmetry in the empty states. Frames (a-b) have scan size 11×11nm^2 and show the same surface area at different sample bias voltages: 1.0V (a), –1.7V (b). Small white dots and dashes on the image (a) arise due to tip instabilities and electrical interference during the given experiment. The registry of features in frame (a) is given in (c) with the elements of point group symmetry 1m: dashed line is an intersection of mirror plane with the plane of the drawing and the cross is the intersection of the first order rotation axis with the plane of the drawing.

– lower than 2mm as it was for the lattice consisting of only D pairs. The first oder rotation axis and the mirror plane belonging to point group symmetry 1m are indicated in fig. III.8c. The registry of brightness maxima appearing in fig. III.8b is the same as was given in fig. III.7c before, containing A and B features with α and β modifications of the c(4×4) lattice. It is intriguing to observe the similarity of the filled states images in figs. III.8b and III.6c-d and the simultaneous symmetry difference between the empty states images in figs. III.8a and III.6a-b. This requires a check if the orientation of the surface structure relative to the scanning direction can influence the appearance of the empty states image. Figs. III.9a-b show another surface, where the c(4×4) structure had an orientation different by ~90° from that in figs. III.8a-b, while the scanning direction was the same. One can clearly see that the contrast between D1 and D2 maxima remains, thus proving it to be a physical reality. Meanwhile, the empty states image obtained at U_t = 1.0 V (fig. III.9a) does not show the C maxima, which appear only at

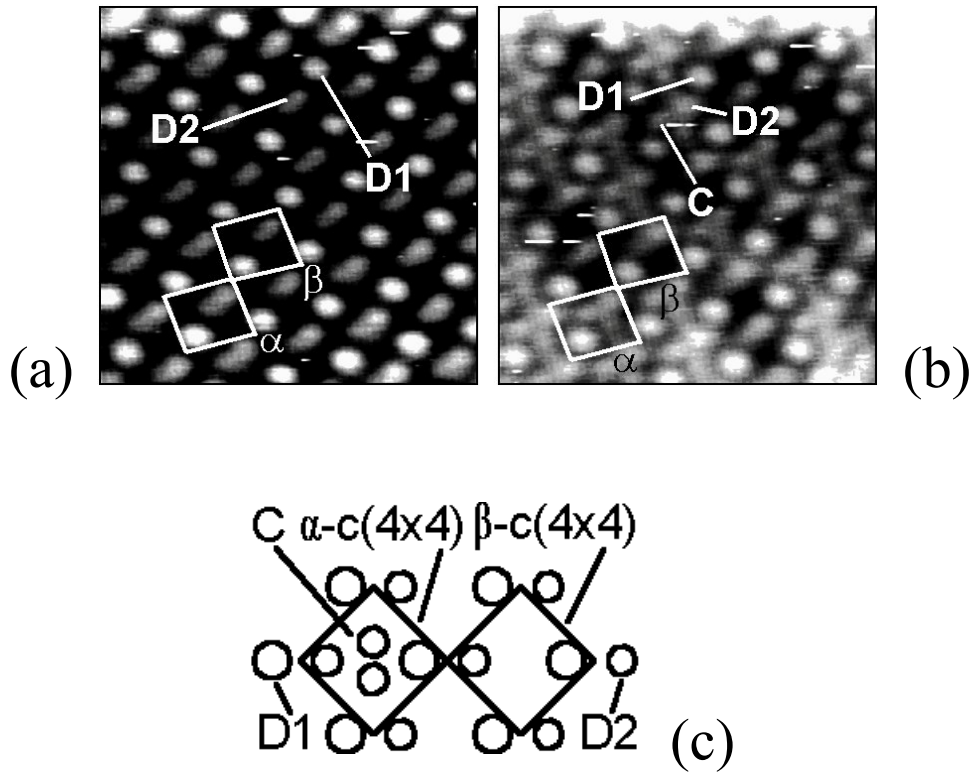

Fig. III.9. STM images of the Si(100)-c(4×4) structure showing lowered symmetry in the empty states. Frames (a-b) show the same area 6×6nm^2 in size at the sample bias voltage of 1.0V (a) and 1.5V (b), with the registry of the brightness maxima at 1.5V given in (c). The STM images are slightly distorted due to thermal drift and unequal piezoscanner sensitivity in different directions.

U_t = 1.5 V (fig. III.9b) – an identical behavior as was observed in figs. III.6a-b. Fig. III.9c contains the registry of the brightness maxima in fig. III.9b. Though the symmetry is lowered as described before, the lattice remains to be c(4×4) with α and β modifications, due to presence or absence of the C pairs. Only the images with the strongest contrast between D1 and D2 are presented in figs. III.8a and III.9a-b, while occasionally the images were obtained with less noticeable contrast in the whole range from the strongest and down to negligible one. Moreover, the same area of the sample could be imaged with or without contrast, depending on the tip condition. These facts along with the unchanging appearance of the filled states images indicate that the images of both symmetries correspond to a single Si(100)-c(4×4) surface structure. One possible scenario is a situation when a physical inequality between D1 and D2 features actually exists but is not always detectable in a certain experimental arrangement. A wave function of the sample's electron system may not be identical in the locations of D1 and D2 maxima. For that to become visible in the STM image, the tunneling current must be different between the tip locations over D1 and D2. The current in its turn is determined by an overlap of tip and sample wave functions. Both are never known exactly, so one can only speculate that some specific configurations of overlapping wave functions produce different currents in D1 and D2 locations, while some others do not.

III.e. Semi-empirical modeling of the Si(100)-c(4×4) structure

In order to understand the cause of D features splitting into D1 and D2 subgroups, a simple modeling of atomic structures consisting of additional Si dimers (Si ad-dimers) on the Si(100) surface was performed [33,74]. Due to the limited scope of calculations the models containing atoms other than Si or involving dimer vacancies were not considered. A semi-empirical MNDO-PM3 method [115] (namely its third parameterized variation of the modified technique with the diatomic overlapping neglected) within the MOPAC code [116] was utilized. The calculations were performed in the restricted Hartree-Fock approximation. The surface was simulated by the clusters of up to 161 silicon atoms with termination by hydrogen atoms at the cluster's boundary [117]. In this way the total energies were calculated for all considered clusters with ad-dimers structures. The latter were compared in terms of

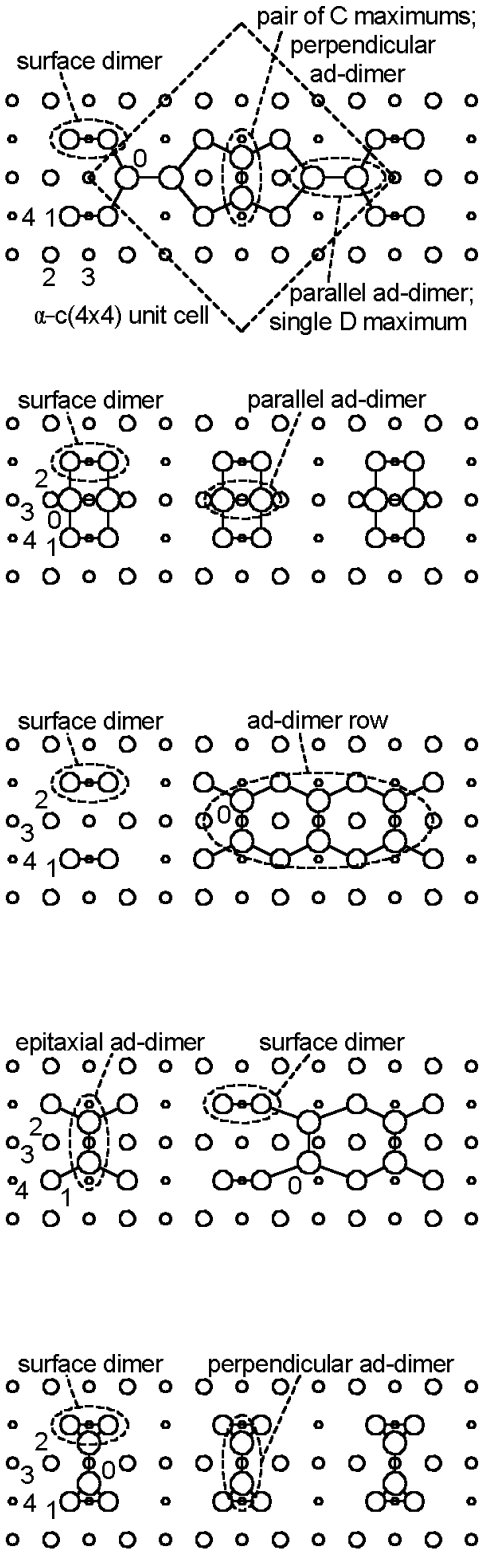

Fig. III.10. Possible silicon ad-dimer structures on the Si(100) surface. The mixed ad-dimer model, α-c(4×4) unit cell, ΔE = –0.08 eV/adatom (a); uniform arrangement of parallel ad-dimers, ΔE = –0.43 eV/adatom (b); continuos ad-dimer row, ΔE = –0.18 eV/adatom (c); ad-dimer row with double dimer vacancy, ΔE = –0.77 eV/adatom (d); uniform arrangement of perpendicular ad-dimers, ΔE = –0.58 eV/adatom (e).

energy **ΔE** calculated as a difference in the binding energies $\mathbf{E_b}$ of ad-dimers' atoms in the structure of interest and in the ideal (2×1) structure formed by the complete monolayer of aditional Si atoms: $\mathbf{\Delta E} = \mathbf{E_b}$(structure of interest) − $\mathbf{E_b}$(2×1). The binding energy was calculated from the following equation: $\mathbf{E_b = (E_t - n \times E_{Si} - E_s)/n}$, where $\mathbf{E_t}$ is the total energy of the cluster simulating the surface with the ad-dimer structure formed by **n** additional Si atoms, each having the total energy $\mathbf{E_{Si}}$ if isolated, and $\mathbf{E_s}$ is the total energy of the cluster simulating the bare surface. In this way **ΔE** is the energy gain of the given structure in comparison with the (2×1) structure. Negative **ΔE** means the energy loss – more negative **ΔE** leads to lower probability that the system will find itself in the given state. Due to the limited computational resources the lateral area of the cluster sufficed to accommodate only one complete c(4×4) unit cell.

Fig. III.10a shows the α-c(4×4) structure according to the mixed ad-dimer model of Uhrberg et al [82], where one perpendicular ad-dimer corresponds to a pair of C type maxima and one parallel ad-dimer corresponds to a single D type maximum. The ad-dimer is considered parallel when its orientation coincides with the surface dimer and perpendicular when they differ by 90°. The Si atoms are represented by open circles with decreasing size indicating position in the deeper atomic layer. The solid lines between the atoms designate chemical bonds, but not all of them are shown for simplicity. The layers are numbered 0 through 4 and the 0^{th} layer consists of atoms forming the ad-dimer structure. These atoms were added to the cluster, which represents the bare surface and was composed of layers 1 through 4. The mixed ad-dimer model corresponds to three ad-dimers added to the cluster (0.75 ML adatoms coverage in the case of completely perfect α-c(4×4) periodicity). Such structure is characterized by ΔE = –0.08 eV/adatom – a very small energy loss in comparison with complete (2×1) reconstructed monolayer of adatoms, for which ΔE = 0 eV/adatom by definition. This energy loss was compared with that of some other structures, which were stable when three ad-dimers were added to the cluster (figs. III.10b-e). Fig. III.10b shows a uniform arrangement of parallel ad-dimers placed on top of the surface dimer rows (ΔE = –0.43 eV/adatom). Other structures consisted of perpendicular ad-dimers, particularly in figs. III.10c-d one observes the nucleation of the next dimerized layer of the Si(100) surface. These structures had values of ΔE = –0.18 eV/adatom for the continuos ad-dimer row (fig. III.10c) and ΔE = –0.77 eV/adatom for the row with a double dimer vacancy (fig.

III.10d). Finally, fig. III.10e shows the uniform arrangement of perpendicular ad-dimers with $\Delta E = -0.58$ eV/adatom. It is clear that the mixed ad-dimer model is energetically strongly favorable over the other dimer arrangements with the same coverage of surface by the adatoms. At the same time, since two parallel ad-dimers are completely symmetric with respect to perpendicular ad-dimer, the mixed ad-dimer model represents the α-c(4×4) structure with point group symmetry 2mm (fig. III.7b-c). Also, the mixed ad-dimer structure was modified by setting unequal initial positions of parallel ad-dimers. Such configurations were not found in any local energy minimum and are unstable. Therefore, the mixed ad-dimer model can not explain the STM images with point group symmetry 1m (figs. III.8a, III.9a-b). Another problematic point is that two atoms of a parallel ad-dimer produce only one D type feature in the STM images. This disagrees with the empty states density contour plot calculated by Uhrberg et al themselves (fig. 6b in [82]), where one distinctly recognizes two density maxima for every parallel ad-dimer. It is hard to realize why they were never resolved, since sufficiently high resolution must have had sometimes occurred, viewing an extensive amount of STM work performed on this system.

As the second step, a possibility of the β-c(4×4) structure, corresponding to parallel ad-dimer model by Uhrberg et al [82], was considered. This model is obtained from the mixed ad-dimer structure by removing the perpendicular ad-dimer from the α-c(4×4) unit cell (figs. III.11a-b). In this case only two parallel ad-dimers are added to the cluster (0.5 ML adatoms coverage in the case of completely perfect β-c(4×4) periodicity). Since Uhrberg et al [82] reported that parallel ad-dimers are buckled, two initial configurations have been tried: with symmetrical (fig. III.11a) and with buckled (fig. III.11b) ad-dimers. Both structures appeared to be in the local energy minimum, but the structure in fig. III.11a was more preferable with $\Delta E = -0.91$ eV/adatom as compared to $\Delta E = -1.21$ eV/adatom for the structure in fig. III.11b. In both cases one parallel ad-dimer corresponds to one D type maximum and the lattice has point group symmetry 2mm, leaving no chance to explain the STM images in figs. III.8-9. The structures in figs. III.11a-b were immediately found unfavorable to placing of both ad-dimers in epitaxial positions with $\Delta E = -0.59$ eV/adatom (fig. III.11c). Thus, it is clear that the β-c(4×4) structure can not exist in the pure form, rather only as a mixture of α-

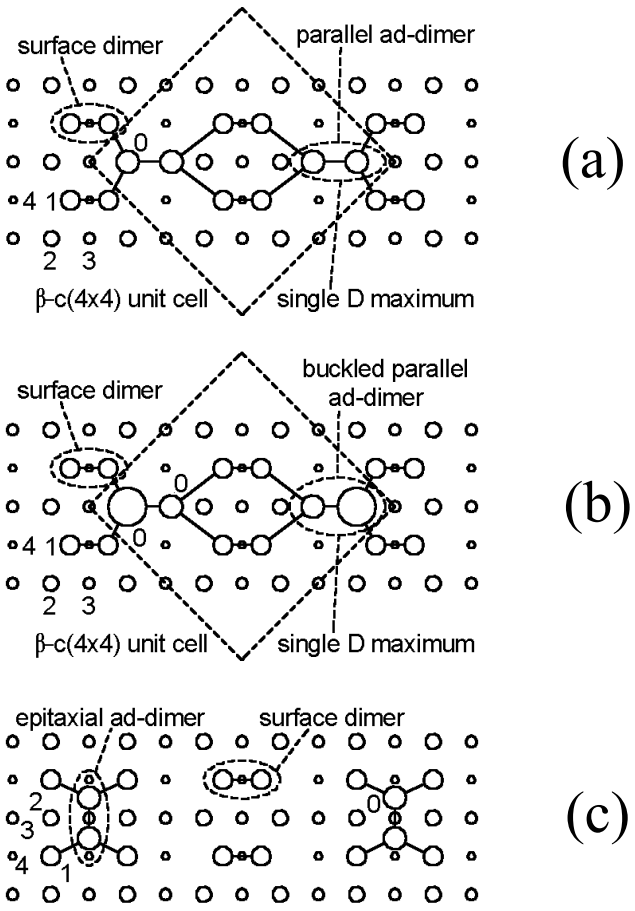

Fig. III.11. Possible silicon ad-dimer structures on the Si(100) surface. Non-buckled parallel ad-dimer model, β-c(4×4) unit cell, ΔE = –0.91 eV/adatom (a); buckled parallel ad-dimer model, β-c(4×4) unit cell, ΔE = –1.21 eV/adatom (b); two ad-dimers in epitaxial positions, ΔE = –0.59 eV/adatom (c).

c(4×4) and β-c(4×4) unit cells – a fact observed experimentally (figs. III.6,8-9).

In the above described models of the Si(100)-c(4×4) surface the objects (ad-dimers in the given case) corresponding to D type features are physically equivalent within the unit cell. That's why it was impossible to explain the STM images of point group symmetry 1m (figs. III.8-9). This prompted a consideration whether the atoms of a parallel ad-dimer can each correspond to a single D type feature [33,74-75] – a possibility pointed out by Ide et al [81] and explicitly suggested by Takaoka et al [95]. In this way the D features may become nonequivalent within pairs due to ad-dimer's buckling. Fig. III.12a shows a suggested refined mixed ad-dimer model [33,74], since its building blocks are still parallel and perpendicular ad-dimers, but arranged in a different manner than in the model of Uhrberg et al [82]. In comparison to the latter, the number

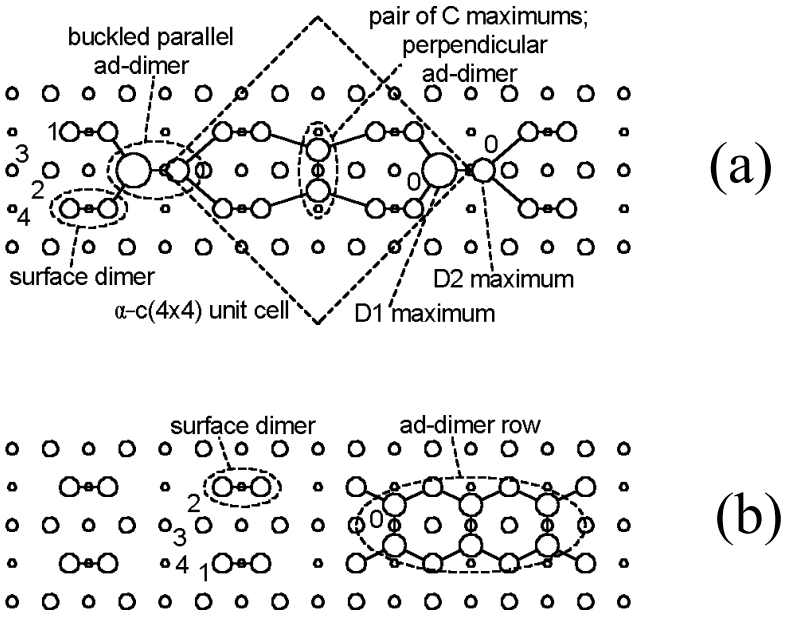

Fig. III.12. Possible silicon ad-dimer structures on the Si(100) surface. Refined mixed ad-dimer model, α-c(4×4) unit cell, ΔE = –1.06 eV/adatom (a); continuos ad-dimer row, ΔE = –0.27 eV/adatom (b).

of parallel ad-dimers is now two times smaller and they are buckled asymmetrically with respect to perpendicular ad-dimers. Comparison of figs. III.9c and III.12a immediately reveals that an STM image similar to fig. III.9b would be produced if the higher atom of a buckled parallel ad-dimer would give rise to D1 maximum and the lower atom to D2 maximum in the empty states. Therefore, a new refined mixed ad-dimer model has point group symmetry 1m to account for the STM images in figs. III.8-9. It corresponds to adatoms coverage equal to 0.5ML (perfect α-4×4 periodicity) and has the value of ΔE = –1.06 eV/adatom. The difference between heights of atoms in the buckled parallel ad-dimer is only 0.01nm. That may explain why D1 and D2 maxima are not always distinguished from one another and the images of point group symmetry 2mm are produced. With a particularly sensitive tip (rarely occurring in practice) D1 and D2 features look different and the symmetry of the lattice is seen as 1m.

It is important to understand the reason for the static buckling of parallel ad-dimers as opposed to dynamic buckling of surface dimers in the (2×1) reconstruction. The former is of primary relevance to the very nature of the refined mixed ad-dimer model. The latter was excellently reviewed with a historical perspective by Dabrowski and Müssig [29]. In the case of the perfect Si(100)-2×1 surface the driving force for

dynamic buckling is the availability of thermal energy which can flip the surface dimer between two stable buckled states (with opposite buckling direction) already at room temperature. Concerning parallel ad-dimers in the Si(100)-c(4×4) structure, we observe all of them buckled in the same direction (within a given atomic terrace). From fig. III.12a it is clear that if both parallel ad-dimers would change the buckling direction, then the structure will find itself in an equally symmetric state. Such change however does not occur, since every parallel ad-dimer belongs to two neighboring unit cells, therefore change in one of them will have to trigger flipping of all ad-dimers on the given terrace. Such correlated flipping seems very improbable due to stochastic nature of thermal fluctuations. On the other hand, the independent flipping of individual ad-dimers would lead to structures of symmetry neither observed in this work nor described in the literature.

The cluster for simulating the refined mixed ad-dimer configuration was larger than in figs. III.10-11, due to increased distance between parallel ad-dimers. Therefore, it was necessary to test a (2×1) ad-dimer row configuration made of three ad-dimers on this cluster, fig. III.12b. Such structure is much more favorable with $\Delta E = -0.27$ eV/adatom, thus representing a major problem for the refined mixed ad-dimer model. Another difficulty is that up to now no stable β-c(4×4) structure was obtained by removing the perpendicular ad-dimer from the refined mixed ad-dimer model. These issues would have to be clarified in the future if this model is really true. In particular it would be helpful to perform ab-initio calculations of total energy for the pure silicon structures presented above and also with inclusion of carbon at some of the atomic sites [103-104]. Such calculations are necessary in order to establish the true atomic structure of the Si(100)-c(4×4) reconstruction and to determine whether impurities play a crucial role in its formation.

III.f. Factors which stabilize the Si(100)-c(4×4) structure

There is no universal agreement about what is responsible for stabilization of the c(4×4) structure instead of the widely occurring (2×1) reconstruction. One simple case is when an element other than Si is adsorbed on the surface in an amount large enough to

create patches of either adsorbate phase or highly defective Si(100)-2×1 phase. These patches may introduce a stress field into the surface layer and in this way stabilize islands of the c(4×4) structure on neighboring areas. Such situations were reported for bismuth by Miki et al [86] and for carbon by Butz et al [88]. In this work the intermediate stages of the (2×1)→c(4×4) phase transition have been observed [72-73]. When both phases coexisted, the (2×1) phase was indeed extremely defective with dimer vacancies grouped into trenches giving rise to the so-called (2×n) structure. However, as the annealing time at 650°C increased, the (2×n) patches disappeared allowing the c(4×4) areas to grow and finally cover the entire surface. This observation indicates that the above discussed stabilization by stress, even if effective, is at least not the only possible stabilization mechanism. When the whole Si(100) surface is in the c(4×4) state, it is natural to search for some impurities possibly responsible for the stabilization. For this particular matter carbon was the mostly studied with perhaps most controversial results. The reported estimates of the carbon amount, which stabilizes the c(4×4) reconstruction are highly inconsistent, ranging from 2.5×10^{18} atoms/cm^3 total bulk concentration [80] to 0.75 ML surface coverage [98]. Remarkably, Men et al [84] had obtained the c(4×4) reconstruction due to interaction with oxygen and found carbon to be detrimental to the structure's stability, seeing it disappear as carbon AES signal becomes detectable. Such a wide contradiction in conclusions suggests that carbon presence does not always stabilizes the given reconstruction, therefore one can not exclude that two different (with and without carbon) c(4×4) structures may exist and still have similar appearance in STM images. It was also necessary to check the Si(100)-c(4×4) surface for bismuth content, since it was involved in the preparation procedure. No trace of it was found with AES, which is not surprising after 30 minutes of annealing well above the bismuth desorption temperature. The influence of bismuth, which might have penetrated into a subsurface region, on the surface structure seems improbable. The retrograde solubility limit of bismuth in silicon is 8×10^{17}cm^{-3} [118] and it is hard to imagine how such a low concentration can affect the reconstruction of the surface. Higher volume concentrations can be achieved by ion implantation of bismuth into silicon [119] and two-dimensional alloying can be achieved by depositing bismuth on the silicon surface amorphized by Ar^+ ion bombardment [120]. Both cases are irrelevant to the employed methodology of obtaining the Si(100)-c(4×4) reconstruction. Another

interesting idea was proposed by Uhrberg et al [82], who outlined the possibility of freezing the density of silicon adatoms, which is not enough to form a complete layer of (2×1) dimer rows. Such a freezing may result from specific preparation conditions of the c(4×4) structure, which are always different from those for the (2×1) structure. From this point of view the Si(100)-c(4×4) structure is regarded as a metastable phase and is observed to be highly defective.

In order to examine a freezing mechanism, the Si(100)-c(4×4) surface was compared after 650 °C annealing which ended with rapid quenching (fig. III.13a) and with slow cooling down (fig. III.13b). As can be seen, the amount of defects dramatically decreases after the slow cooling, thus qualitatively demonstrating the absence of freezing. Recently, Zhao et al [31] have obtained the Si(100)-c(4×8) reconstruction by silicon solid phase epitaxy and found it energetically very unfavorable

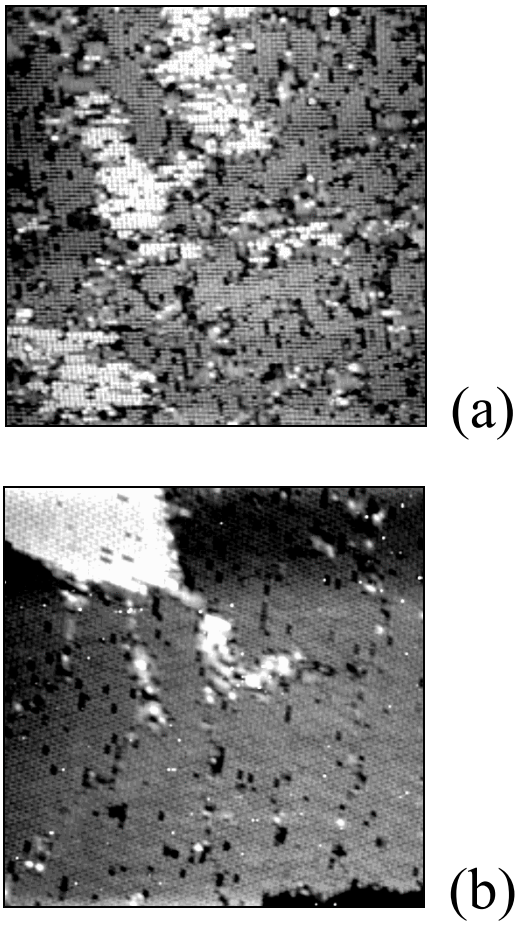

Fig. III.13. STM images of the Si(100)-c(4×4) surfaces obtained by rapid quenching (a) and slow cooling (b) to room temperature after 650 °C annealing. Image sizes are 63×63nm^2 and sample bias voltages are equal to 1.0V.

in comparison with the (2×1) structure. The formation of the c(4×8) structure is attributed to a highly nonequilibrium thermodynamic process as molecular-dynamics simulation suggests. In other words, this structure is formed not due to the global energetic equilibration, but as a result of kinetic pushing (a process of atoms getting high kinetic energy, reaching sites of high potential energy and finally getting trapped there). In the future studies it would be extremely interesting to try this approach in explaining the stability of the Si(100)-c(4×4) reconstruction. At present, however, no single stabilizing factor seems to be an exclusively possible candidate. It can well be that different factors can stabilize the structure in different conditions, but their elucidation will be done in future.

III.g. Summary of the novel features of the Si(100)-c(4×4) reconstruction and the issues relevant to epitaxy on the Si(100) surface

It was found that ultrasmall Bi amounts (θ_{Bi}<0.2ML) adsorb in an unordered phase at 20 ^{0}C and nucleate the ordered (2×1) phase at 400 ^{0}C, simultaneously creating vacancy clusters in the substrate. Deposition and desorption of larger Bi amounts creates substrate vacancies grouped into lines, thus transforming it into the (2×n) condition. Further annealing of such a surface causes a rapid phase transition into the c(4×4) state, which is one order of magnitude faster than without Bi preadsorption. The resulting Si(100)-c(4×4) phase is stable at temperatures below 800 ^{0}C, and does not transform back into the (2×1) phase, unless the Si sample is annealed at 1200 ^{0}C.

The structure and stability of the Si(100)-c(4×4) surface was studied with the STM technique. The new STM images of the c(4×4) structure clearly demonstrate the lattice with point group symmetry 1m in contrast to previously reported 2mm. A series of semiempirical total energy calculations were performed to simulate structures of silicon adatoms on the Si(100) surface. A new refined mixed ad-dimer model of the c(4×4) reconstruction was developed, consisting of equal amounts of perpendicular and parallel ad-dimers, the latter being buckled asymmetrically with respect to the former. Since the buckling is weak, it may not always be detected, thus explaining why the c(4×4) structure of higher symmetry is observed in the majority of experiments.

The AES investigation only adds to a scatter of carbon concentrations reported in the literature for the Si(100)-c(4×4) surface. It seems that the carbon presence is not always responsible for the stabilization of the c(4×4) structure. A possibility of existence of this structure both with and without carbon cannot be ruled out at present. The annealing experiments with different subsequent cooling rates also rule out the freezing mechanism of stabilizing the density of silicon adatoms low enough to form the c(4×4) reconstruction. A more sophisticated theoretical approach (ab-initio total energy calculations) will have to be employed in the future in order to verify the suggested refined mixed ad-dimer model. On the other hand, the molecular dynamics simulations will be very helpful in elucidating the stabilizing factors of the Si(100)-c(4×4) reconstruction.

The prospects of this reconstruction as a substrate for high-K films epitaxy (in particular Pr_2O_3) seem negative on the basis of results presented in this chapter. Such judgement is based on the observation that the Si(100)-c(4×4) surface is always rougher than the Si(100)-2×1 surface. The former is a mixture of α and β phases, thus having intrinsic irregularities, which would most probably degrade the quality of dielectric/Si(100) interface. Even a perfect α-c(4×4) structure (although never observed in pure form) is essentially an uncomplete atomic layer (of various monolayer fraction according to different authors), which is therefore less perfect than an ideal 2×1 reconstruction. A high amount of defects, normally observed on the Si(100)-c(4×4) surface aggravates the situation even further. All factors mentioned above indicate, that it will be reasonable to avoid the formation of the c(4×4) reconstruction during deposition of Pr_2O_3 on the Si(100) substrate. Since such reconstruction appears due to interaction with numerous adsorbates, there was a concern if this will not be the case for Pr_2O_3. One particularly undesirable scenario is when the film covers the substrate, which is half way into the (2×1)→(2×n)→c(4×4) phase transition. As this and other works show, it is the usual sequence leading to c(4×4) phase formation, and the surface quality during transition is even lower than the final Si(100)-c(4×4) surface. All these issues can be of a detrimental nature, especially for ultra-thin dielectric films applied in aggressively scaled MOS devices, where the interfacial quality has a great influence on electrical performance. The STM data of Müssig and coworkers [21,23-25] show that the presence of Pr_2O_3 on the Si(100) surface does not invoke the c(4×4) reconstruction.

During the growth process, the not yet covered surface areas always stay (2×1) reconstructed. This is a positive sign hinting on possibility to create high quality Pr_2O_3-based MOS devices on the Si(100) substrate. However, one should keep in mind that any changes made in the deposition procedure (substrate temperature, vacuum conditions, any additional species, etc) in order to increase quality, productivity, robustness or some physical properties of the film/interface must be checked if they do not invoke a substrate phase transition described above.

Chapter IV

Thermal stability of Pr_2O_3 films grown on Si(100) substrate

IV.a. High-K dielectrics and analysis of Pr_2O_3

The International Technology Roadmap for Semiconductors (ITRS) outlines the need for new materials that can satisfy the stringent requirements of future generations of complementary metal-oxide-semiconductor (CMOS) technology [4]. SiO_2 was used for decades as insulator between the gate electrode and the channel of a metal-oxide-semiconductor (MOS) transistor, but is approaching its applicability limit due to the relatively low dielectric constant "K" [12]. There are a number of new high-K materials and their combinations which are investigated for the desired physical properties and compatibility with the manufacturing technology of advanced integrated circuits (ICs) [14-18]. Recently it has been shown, that Pr_2O_3 is a potential high-K dielectric (with a dielectric constant ~ 30), which could be used in FETs and DRAM capacitors [20-25]. In modern IC production, the FET gates and DRAM capacitors are formed in the middle of the process sequence with several high temperature anneals afterwards. The total thermal exposure must not exceed the maximum allowed "thermal budget" for the dielectric film on the substrate, which guarantees the absence of intermixing between involved materials. Therefore, if Pr_2O_3 is to replace SiO_2 inside of the MOS structures, then the major concern is thermal stability of Pr_2O_3 in contact with Si, on which very little data were previously available [35-36]. The purpose of investigation described in this chapter was an experimental determination of thermal stability limits for the given material system. In the following, results on thermal stability of Pr_2O_3 films against Si out-diffusion from the Si substrate, for uncapped films and films capped with a Si layer [38-39] will be presented. The case of Pr_2O_3/Si(100) is important for the growth process and Si/Pr_2O_3/Si(100) represents the simplest version of the capacitor-type materials combination. The later is of special importance since in modern CMOS technology the material of the gate electrode is usually poly-Si. It will be shown that the thermal stability of Si/Pr_2O_3/Si(100) structure is higher than for the Pr_2O_3/Si(100) structure. They may also have different products of reaction between Pr_2O_3 and Si. During

annealing the Pr_2O_3/Si(100) system always evolves towards the formation of Pr silicate, while the Si/Pr_2O_3/Si(100) system may produce either Pr silicate or Pr silicide, depending on experimental conditions. Since thermal processing is often done in a nitrogen environment, one of the tasks in this work was to compare the outcome of annealing both in vacuum and nitrogen under ambient pressure. It will be shown, that the presence of nitrogen environment permits to avoid silicide formation and also improves the thermal stability of the Si/Pr_2O_3/Si(100) structure with regards to silicate formation.

IV.b. Uncapped film without annealing

A Pr_2O_3 film was deposited on a Si(100) substrate kept at 725°C. The deposition was done under the pressure in the 10^{-8} mbar range by electron beam evaporation from a powder packed ceramic Pr_6O_{11} source. Fig. IV.1a shows the TEM image of an as-deposited, uncapped praseodymium oxide film. Three different regions can be distinguished (from bottom to top): the crystalline Si(100) substrate, the 3 nm thick amorphous interfacial layer (with a bright stripe neighbouring the substrate), and the 10 nm thick crystalline praseodymium oxide. The latter was identified as Pr_2O_3 by X-ray diffraction (XRD) $\theta/2\theta$ scan, which showed a pattern of Pr_2O_3 with manganese oxide structure [23-25]. In fig. IV.1b, one can see the AES depth profile (ADP) of the same structure as in fig. IV.1a. The following transitions were used for quantitative AES analysis: Pr (MNN, 699 eV), O (KLL, 503 eV), Si (KLL, 1619 eV). It was not possible to use the low energy lines of Si and Pr due to their severe overlap. The elemental sensitivity factors of O and Pr were referenced to that of Si using SiO_2 and Pr_2O_3 standards. At the ADP of the as-deposited film the Si substrate, the oxide film and the interface between them can be clearly distinguished. Far from the interface there are non-zero concentrations of Si inside the film and of O and Pr inside the substrate. These concentrations correspond to AES sensitivity limits (or “offset” levels) for the given elements in the given matrixes. In such cases the real concentration may be anywhere

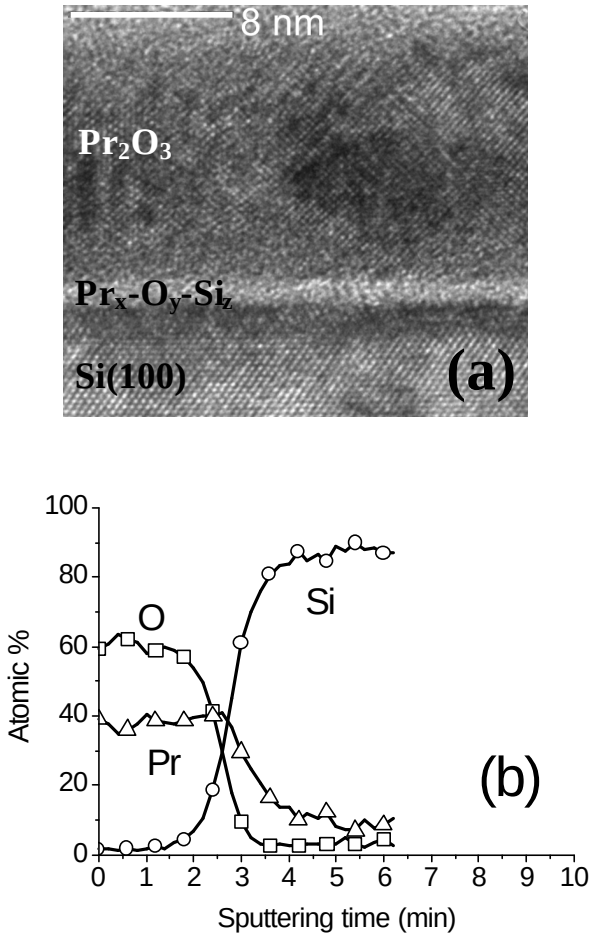

Fig. IV.1. As-deposited Pr_2O_3 film on Si(100) substrate: a) Cross-sectional TEM image, b) Auger depth profile. The Si substrate, the interfacial amorphous silicate layer, and the crystalline Pr_2O_3 film can be distinguished.

between zero and sensitivity limit, and cannot be measured by AES technique. This restriction applies also to all other ADPs presented in this chapter. The ADP in fig. IV.1b shows that O decays faster than Pr along the transition from the film to the substrate. After 4 minutes of sputtering a non-zero Pr signal was detected, but O was already below its "offset" level. This may happen due to faster sputtering of O than Pr in the interface region. As a result, some Pr may still remain in the sample and be registered when the film is already sputtered through during depth profiling.

In order to better understand conditions in the interface between the Pr_2O_3 film and the Si substrate, an XPS analysis of the Pr 3d peak was performed (fig. IV.2a). In the bulk of the film, the structure of the Pr 3d peak with a multiplet splitting into the $3d_{3/2}$ and $3d_{5/2}$ components is evident. Both components show satellites of lower binding energies, as previously reported for Pr_2O_3 [121]. At the interface, the $3d_{3/2}$ and $3d_{5/2}$

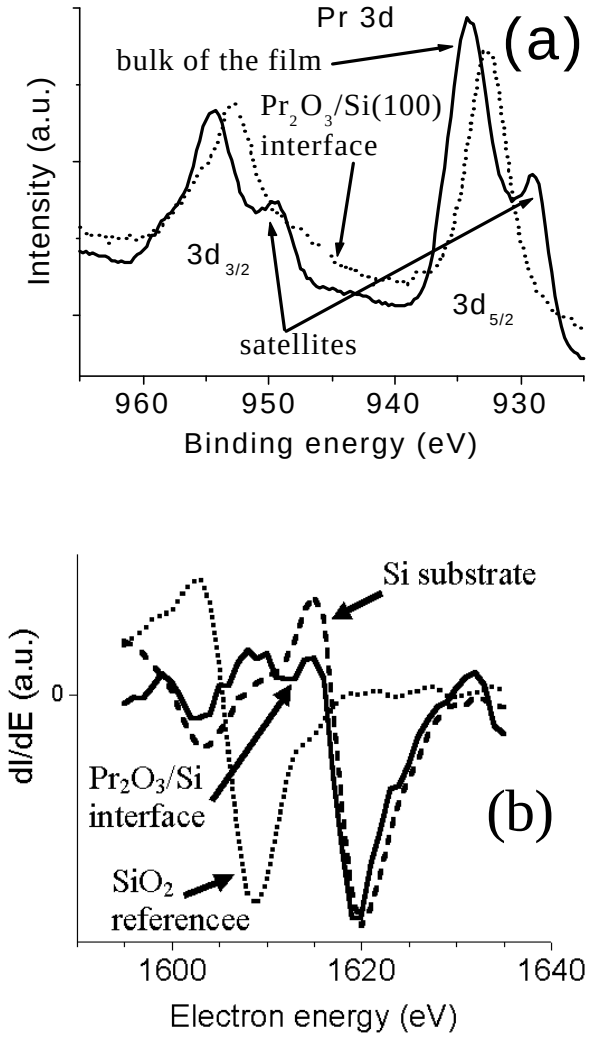

Fig. IV.2. Spectroscopic analysis of as-deposited Pr_2O_3 film on Si(100) substrate: a) XPS Pr 3d peaks (not drawn to scale) obtained in the bulk of the film and at the interface between the film and the substrate; b) AES Si KLL peaks (not drawn to scale) obtained in the interface region, in the pure Si substrate, and in the SiO_2 reference sample.

components without satellites are displayed, meaning that Pr_2O_3 does not exist in this region. The spectrum without satellites may be attributed to metallic Pr [122], but it is not the case here. As will be shown later a Pr_x-O_y-Si_z silicate is formed, which is visible on ADP in fig. IV.1b. There, a layer between the substrate and Pr_2O_3, where all three elements are present, is distinguished. Fig. IV.2b shows the AES KLL peaks of Si on the differentiated spectra obtained: at the interface, deep in the pure Si substrate, and in the reference SiO_2 sample. It is obvious that the Si KLL peak at the interface is an overlap of two contributions: pure and oxidised Si (the latter belonging to silicate).

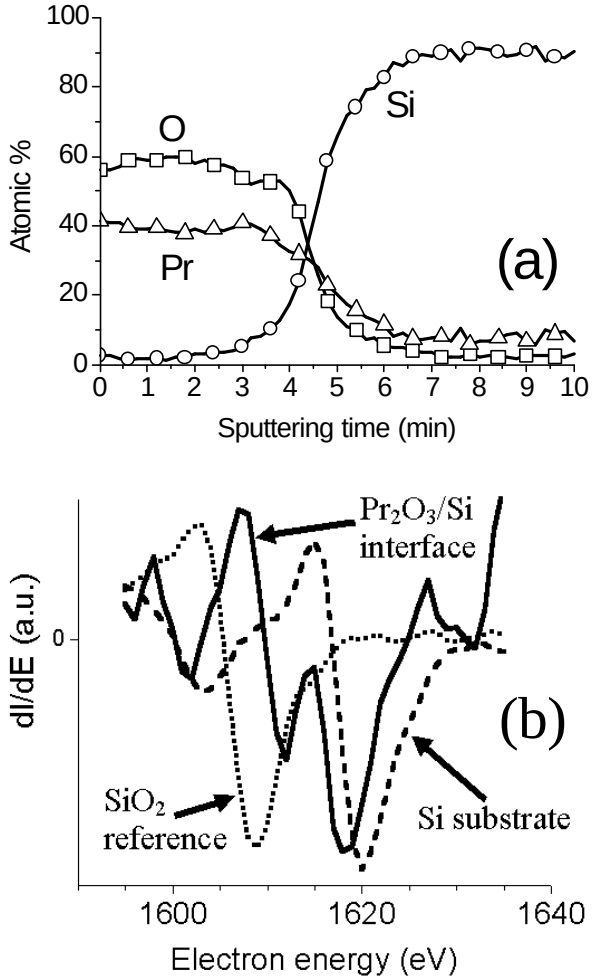

Figure IV.3. The same Pr_2O_3 film as in figs. IV.1-2 after vacuum annealing at 600°C for 3 hours: a) Auger depth profile; b) AES Si KLL peaks (not drawn to scale) obtained in the interface region, in the pure Si substrate, and in the SiO_2 reference sample. The Si diffuses into the interface region, but does not penetrate into the Pr_2O_3 film.

IV.c. 600° C annealing of uncapped film

Fig. IV.3a shows an ADP from the same Pr_2O_3 film as in figs. IV.1-2 but after 600°C annealing (by bringing the back side of the Si wafer into contact with ceramic heat dissipater) for 3 hours under the residual gas pressure of 10^{-6} mbar. Such a high pressure existed due to a large amount of heat emanating from the annealing setup into the parts of the vacuum chamber. After anneal, it takes longer to sputter through the film and the interface region between the film and the substrate. It is convenient to express the thickness of considered layers in equivalent sputtering times needed to remove them.

The interface region is defined to be between the points where the Si concentration is 16% and 84% of the constant substrate level. After 3 hours of annealing (fig. IV.3a), the film and the interface are 70% and 60% thicker than in the as-deposited sample (fig. IV.1b), respectively. The Si AES KLL peak shape analysis in the interface region after 3 hours of annealing again shows an overlap of two contributions: from pure Si and oxidised Si, as shown on the differentiated spectrum in fig. IV.3b. The partial contribution of oxidised Si is much stronger than in fig. IV.2b. The concentration of O in the interfacial layer does not decay across the interface as quickly as in the as-deposited sample (compare figs. IV.1b and IV.3a). Therefore, a Pr_x-O_y-Si_z silicate layer is growing due to 600°C vacuum annealing.

IV.d. 700°C annealing of uncapped film

Fig. IV.4a shows the ADP of the same Pr_2O_3 film as in fig. IV.1-2, but annealed at 700°C for 3 hours in a similar way as described in the previous section. The most important effect of 700°C annealing is a diffusion of Si into the Pr_2O_3 film. Si diffuses through the Pr_2O_3 film and accumulates at the surface. There it reacts with the oxygen available from the residual atmosphere and forms SiO_2. This is confirmed by fig. IV.4b with the AES KLL peaks of Si on the differentiated spectra obtained inside of the film, on the film's surface, in the pure Si substrate, and from the reference SiO_2 sample. The Si KLL peak measured at the surface has practically the same position as the SiO_2 reference. It is clear that the Si, which diffused into the film is oxidised, since its AES KLL Si peak is situated between the pure Si peak and the SiO_2 peak. The thickness of different regions at the ADP in fig. IV.4a is not directly comparable with that of the as-deposited structure, since pure Pr_2O_3 is no longer present. Instead, the total sputtering time, needed to reach the point where the Si concentration rises to 84% of the constant substrate level, may be a relevant parameter. This time increases by 118% after annealing at 700°C for 3 hours (fig. IV.4a) as compared to the as-deposited film (fig. IV.1b). The apparent increase of the film thickness can be understood as a volume increase due to diffusion of additional matter into the film. Noteworthy, this happens at

a temperature lower than the growth temperature. One possible reason for this phenomenon can be a sufficiently long annealing time in the given case.

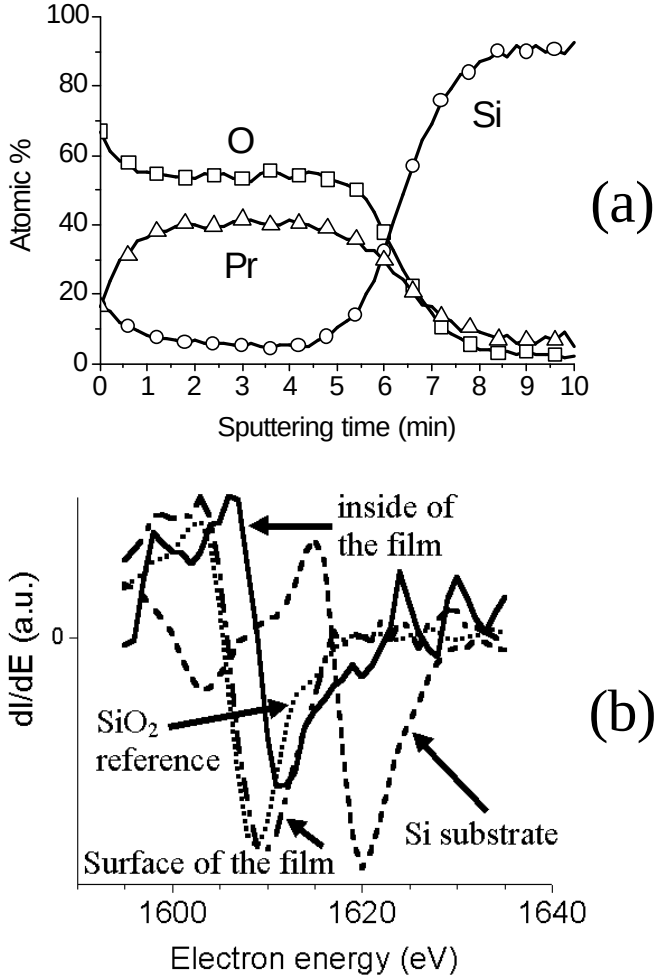

Fig. IV.4. The same Pr_2O_3 film as in figs. IV.1-2 after vacuum annealing at 700°C for 3 hours: a) Auger depth profile; b) AES Si KLL peaks (not drawn to scale) obtained inside of the film, in the pure Si substrate, in the SiO_2 reference sample, and on the film's surface. The Si diffuses into the film, goes through it, and starts to accumulate on the surface in the SiO_2 form.

IV.e. 900°C annealing of uncapped film in an N_2 atmosphere

Annealing at temperatures above 700°C was done in the furnace with N_2 flow under atmospheric pressure, with similar effects on the Pr_2O_3 films as in the case of vacuum annealing. As an example, consider an ADP of the same film as in fig. IV.1,

annealed in an N_2 atmosphere for 30 minutes at 900°C (fig. IV.5a). The TEM image in fig. IV.5b shows a completely different crystalline structure, compared to the as-deposited film (fig. IV.1a). This structure remains to be identified. After annealing, the thickness of the film is 15 nm and the thickness of the interfacial layer is 4 nm, as compared with 10 nm and 3nm, respectively, for the as-deposited sample. As before, Si is oxidised in the bulk of the film, as confirmed by AES and XPS analysis, and the diffused Si starts to accumulate on the surface in the SiO_2 form. For this, the source of O could be impurities in the N_2 flow, which act in a similar manner as residual O during vacuum annealing. Fig. IV.5c shows the XPS spectra of the Pr 3d peak (obtained in a similar way as in fig. IV.2) in the bulk of the film and at the interface between the film and the substrate. The shape of Pr 3d peak at the interface is similar to that for interfacial Pr_x-O_y-Si_z silicate in the as-deposited film (fig. IV.2a). In the bulk of the film, $3d_{3/2}$ and $3d_{5/2}$ components of the peak have low energy satellites, but they are not so intense as in the case of pure Pr_2O_3 (fig. IV.2a). This indicates that Pr_2O_3 exists in the bulk of the film, but it is intermixed with Pr_x-O_y-Si_z silicate, while the latter exists in the pure form at the interface. Thus, a conclusion follows, that due to Si out-diffusion from the substrate, the pure Pr_2O_3 film is transformed into a Pr_2O_3-Pr_x-O_y-Si_z mixture, the structure of which is shown in fig. IV.5b. It is believed that almost the same Pr_2O_3-Pr_x-O_y-Si_z mixture is formed during annealing both in vacuum (fig. IV.4a) and in an N_2 environment (fig. IV.5a). Establishing the exact concentrations of elements in this mixture remains to be done, taking into account matrix effects on elemental sensitivity factors and possible preferential sputtering. These results stand in line with the work of Ono and Katsumata, who investigated the thermal stability of all lanthanide oxides on a Si(100) substrate by infrared spectroscopy [36]. They have found a strong increase in the Si-O-Pr bonds and Si-O-Si bonds, starting at temperatures approximately equal to 700°C, after the 20÷30 nm thick Pr_2O_3 films were annealed in an N_2 environment.

IV.f. Annealing of Pr_2O_3 film capped with Si

There is no doubt about importance of addressing the thermal stability of the application-relevant structure, where the Pr_2O_3 film is sandwiched between the Si(100)

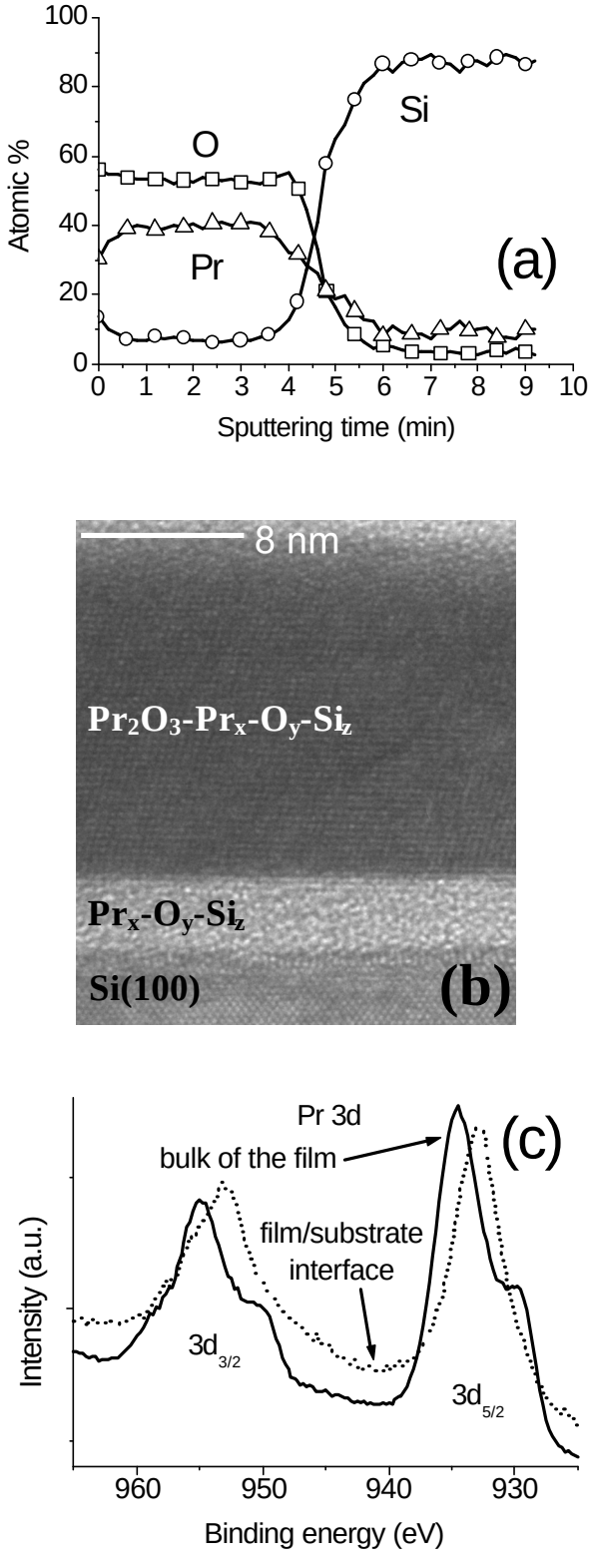

Fig. IV.5. The same Pr_2O_3 film as in figs. IV.1-2 after annealing at 900°C for 30 minutes in the N_2 furnace: a) Auger depth profile; b) high resolution cross-sectional TEM image, c) XPS Pr 3d peaks (not drawn to scale) obtained in the bulk of the film and at the interface between the film and the substrate. The diffusion of Si into the Pr_2O_3 film leads to formation of the Pr_2O_3-Pr_x-O_y-Si_z mixture.

substrate and amorphous Si (a-Si), representing transistor gate or capacitor plate. Both an oxide film and a Si cap were produced by electron beam evaporation. Fig. IV.6 shows the ADP of such a (45nm)a-Si/(40nm)Pr_2O_3/Si(100) structure in the as-deposited state. Just like it was the case for uncapped film (see section IV.b) Pr and O stay below "offset" levels in the substrate and Si is below its "offset" level in the film. Its ADPs

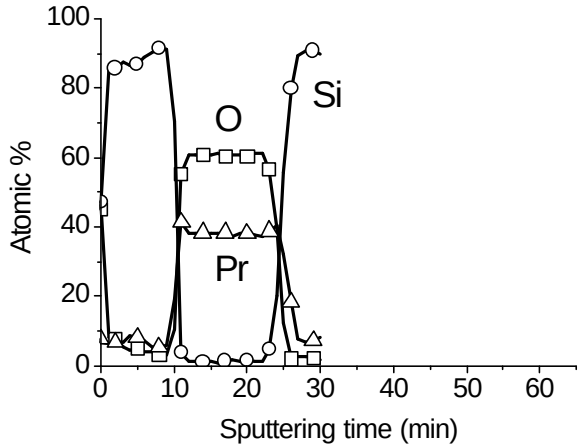

Fig. IV.6. Auger depth profile of the (45nm)Si/(40nm)Pr_2O_3/Si(100) structure. This as-deposited structure represents the simplest capacitor-type materials combination.

after vacuum annealing at 700°C (in a similar way as for uncapped film, see section IV.c) are shown: for 1 hour in fig. IV.7a, for 2 hours in fig. IV.7b, and for 3 hours in fig. IV.7c. As shown in fig. IV.7a, no Si has penetrated into the film and only the interfaces between Pr_2O_3 and Si appear to be slightly broadened. In fig. IV.7b one sees the result of Si cap etching by residual oxygen. This process leads to strong surface roughening [123], which explains why the Pr signal is detected already at the beginning of the ADP. Finally in fig. IV.7c a $PrSi_x$ formation can be observed, as the etching of the cap continues. The true composition of the silicide remains to be determined due to possible influence of preferential sputtering effects.

So far, both capped and uncapped films were not stable under 700°C vacuum annealing. Therefore, it was interesting to compare these films under the influence of annealing in an N_2 environment. For this purpose the effect of such annealing (performed in a similar manner as for uncapped film in section IV.e) in the range from 800°C to 1040°C was examined. Fig. IV.8 shows the same a-Si/Pr_2O_3/Si(100) structure as in fig. IV.6 but after 3 hours of annealing in N_2 at a) 800°C, b) 900°C and c) 1000°C.

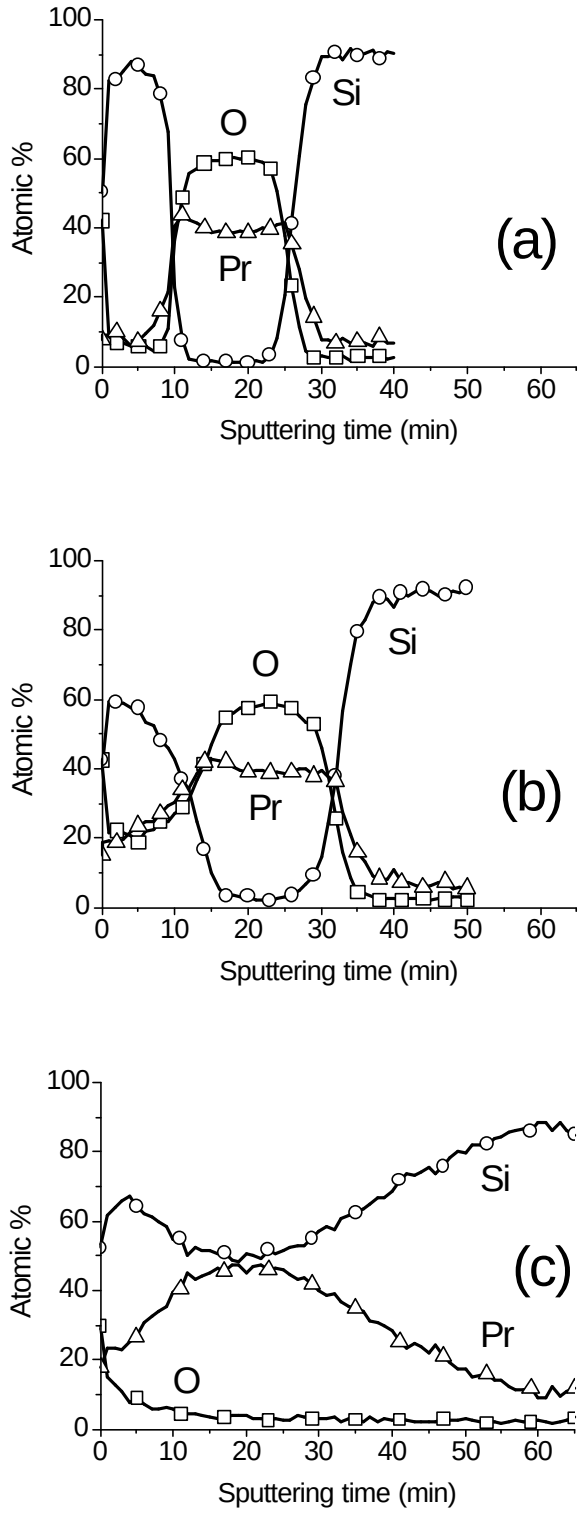

Fig. IV.7. The same Si/Pr_2O_3/Si(100) structure as in fig. IV.6 after vacuum annealing at 700°C. Auger depth profiles of the structure after annealing for: a) 1 hour - the Pr_2O_3 film retains its integrity; b) 2 hours - the etching of cap layer by residual oxygen; c) 3 hours - Pr silicide is formed.

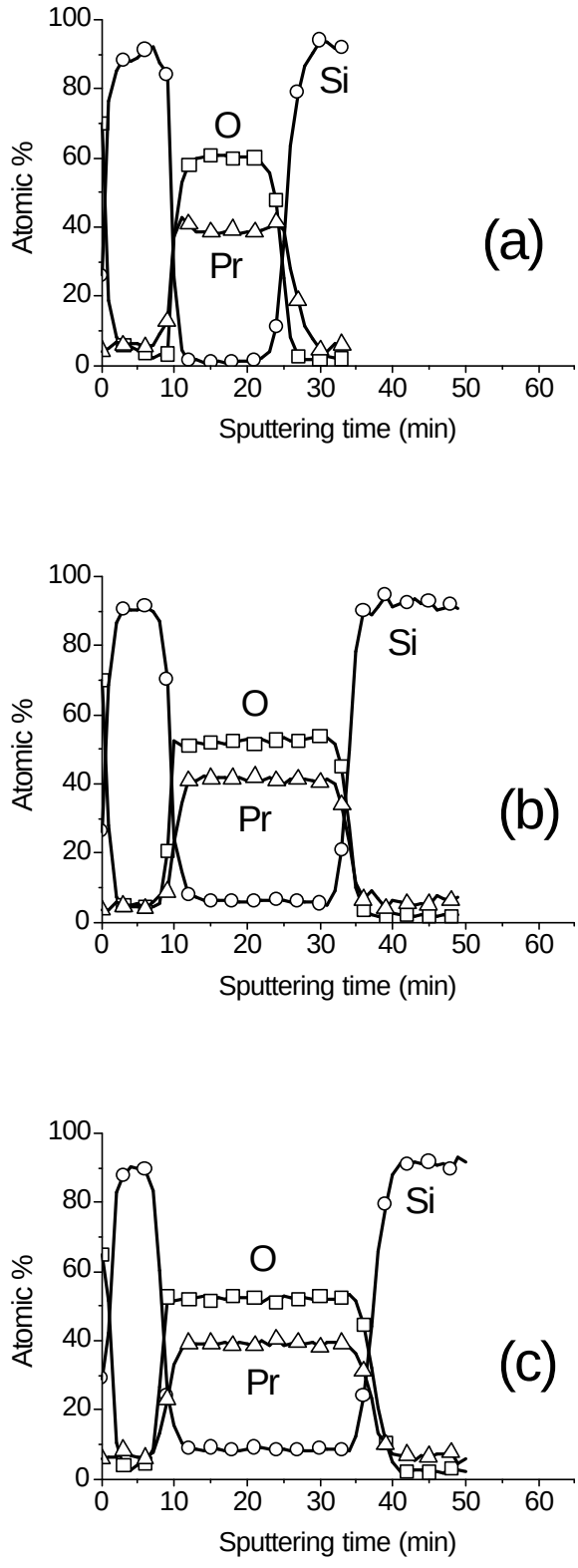

Fig. IV.8. The same $Si/Pr_2O_3/Si(100)$ structure as in fig. IV.6 after annealing in N_2 during 3 hours. Auger depth profile after annealing at: a) 800°C - the Pr_2O_3 film retains its integrity; b) 900°C - the Si diffuses into the film and the Pr_2O_3-Pr_x-O_y-Si_z mixture is formed; c) 1000°C - a similar mixture, but with higher Si content.

In fig. IV.8a not only Si is absent in the film, but its interfaces with cap and substrate are practically identical to the as-deposited case. Both at 900°C and at 1000°C, Si diffuses into the Pr_2O_3 film, and a Pr_2O_3-Pr_x-O_y-Si_z mixture is formed, similar to those as in the case of the uncapped film (figs. IV.4-5). After a 1000°C anneal, the thickness of the Pr_2O_3-Pr_x-O_y-Si_z mixture is larger than after annealing at 900°C. This correlates with higher Si concentration after annealing at higher temperature (figs. IV.8b-c), which means larger amount of in-diffused material and larger volume of the film. It is important to note, that according to a recent report [18], the Pr silicate is also a high-K dielectric. This fact allows to expect that the structures shown in figs. IV.8b-c will also be of an electrode - high-K dielectric - substrate type. Thus the thermal budget of Pr_2O_3-based structures is dramatically increased for the case of annealing in an N_2 environment.

It seems fairly obvious that the presence of nitrogen preserves the Si cap in one way or another. One can speculate, that some kind of stable silicon nitride or oxinitride layer is formed on the sample surface, serving as protective shield against oxidation and etching of the cap. The presence of the latter changes thermodynamics of the system, making it unfavourable for Si to diffuse into the film from the substrate under temperatures of up to 800°C. A theoretical calculation of chemical potential for Si atom inside of both capped and uncapped Pr_2O_3 film will have to be done in the future to support this point of view. Another role of nitrogen is that by preventing the very process of cap etching it eliminates the possibility of Pr silicide formation, which is discussed below in more detail.

IV.g. Formation of $PrSi_x$ layer from capped Pr_2O_3

Finally, it is instructive to focus on the last stages of Si cap etching and $PrSi_x$ formation in the Si/Pr_2O_3/Si(100) structures. For this purpose a structure with 16 nm thick cap and 33 nm thick Pr_2O_3 film was deposited by electron beam evaporation. Fig. IV.9a shows the ADP of this structure in an as-deposited state. The ADPs after vacuum annealing are shown: for 12 minutes in fig. IV.9b and for 1 hour in fig. IV.9c. Since the Si cap was almost 3 times thinner than for the structure in fig. IV.6, it took a very short

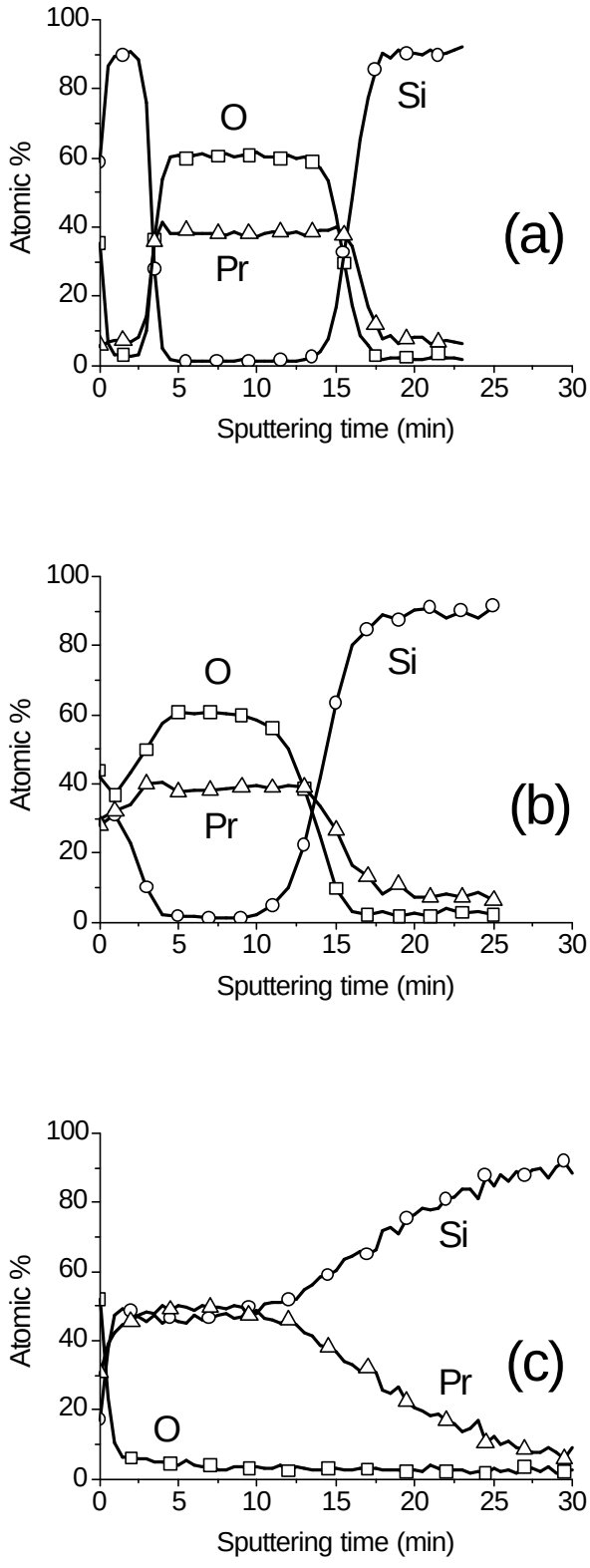

Fig. IV.9. Praseodymium silicide formation in the (16nm)Si/(33nm)Pr_2O_3/Si(100) structure. Auger depth profiles: a) in the as-deposited state; b) after annealing in vacuum at 700°C for 12 minutes - the Si cap is almost etched away; c) after annealing in vacuum at 700°C for 1 hour - the Pr silicide layer is formed.

time for it to be etched away completely (fig. IV.9b). As a last step in the structure's evolution, a silicide film is formed with a very smeared interface to Si(100) substrate (fig. IV.9c). Future work will determine why exactly does the silicide form in the given case and not when the uncapped film is annealed in similar conditions (see section IV.d). At the current moment only a speculative hypothesis can be suggested. According to this, Si reacts with residual oxygen of the vacuum chamber during annealing. As a result volatile SiO molecules are formed and they leave the surface – the Si cap is being etched away. As almost nothing of the cap remains (fig. IV.9b), the system becomes more like an uncapped film (fig. IV.1) where Si outdiffuses from the substrate already at 700°C. Upon reaching the surface it "re-supplies" the almost vanished cap, and so the process of SiO formation goes on, with a thin Si layer being present on top of the sample. In this situation it is probably more favourable for oxygen of Pr_2O_3 to diffuse to the surface and react with remains of the cap (again forming SiO volatile species) than to bind itself into Pr silicate. The final stage of this process will thus be a creation of Pr silicide film. The whole story is too much dependent on a very specific final stage of Si cap etching. In this light, it's no wonder that N_2 environment, which entirely prevents the cap from etching, makes the silicide formation completely impossible.

At this point it was also demonstrated that a higher annealing temperature leads to a Si-rich $PrSi_x$ phase, distinctly different from the one shown above. This phase is seen in fig. IV.10, where the ADP of the silicide film is shown, obtained after the (10nm)Si/(30nm)Pr_2O_3/Si(100) structure was annealed in high vacuum at 900°C for 15 minutes. The transformation of the silicide into Si-richer phase at higher temperatures can be generally observed in other material systems [5,56]. An exact Si content for silicides in figs. IV.9c and IV.10 can not be determined precisely from ADPs alone, due to possible preferential sputtering in compounds where one element is much heavier than Si. Therefore, Rutherford backscattering (RBS) technique or comparative AES of actual and standard praseodimium silicides will be used in future studies, similar to what will be described in chapter V for tungsten silicide [52].

The data presented above complement a comprehensive study by Hubbard and Scholm, who investigated a thermodynamic stability of all binary oxides in contact with Si at 700°C [35]. They could not determine whether the praseodymium silicide

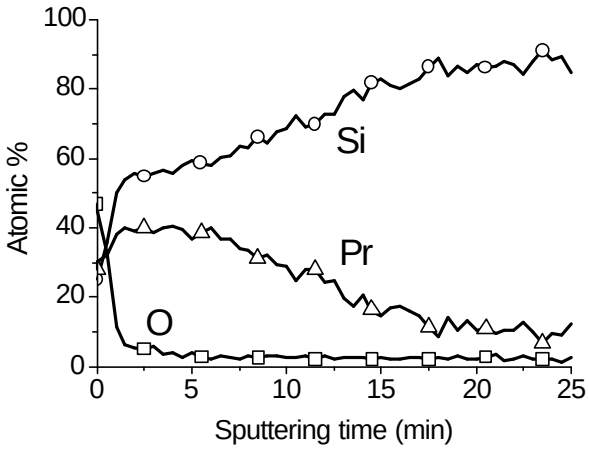

Fig. IV.10. Formation of the Si-rich praseodymium silicide. Auger depth profile after the (10nm)Si/(30nm)Pr_2O_3/Si(100) structure was annealed in high vacuum at 900°C for 15 minutes.

formation was possible, because of unavailability of published thermodynamic data for the reaction products. The current investigation solves this problem experimentally, but demonstrates that either a silicide or a ternary Pr-Si-O compound can be a final product of the reaction, depending on the initial geometric configuration of phases in the Pr_2O_3-Si system.

IV.h. Source/Drain contacts based on $PrSi_x$

In the following it is suggested how the above described silicide formation may be utilised to build a MOS transistor. As it was pointed out in chapter I, different silicides are used for making contacts to Si parts of a transistor. Since $PrSi_x$ can be readily formed from the gate insulator material, a natural idea arises to use this silicide in the contacts to source and drain. The idea is illustrated by fig. IV.11 showing the initial and final stages of source/drain contact creation, respectively [39]. In fig. IV.11a we see a Pr_2O_3 gate dielectric deposited on top of the Si(100) substrate, in which the source and drain regions are already formed by appropriate doping. A 45 nm thick layer of Si (either amorphous or polycrystalline) is deposited on top of the dielectric and selectively thinned (for example by chemical etching through the mask) in the areas

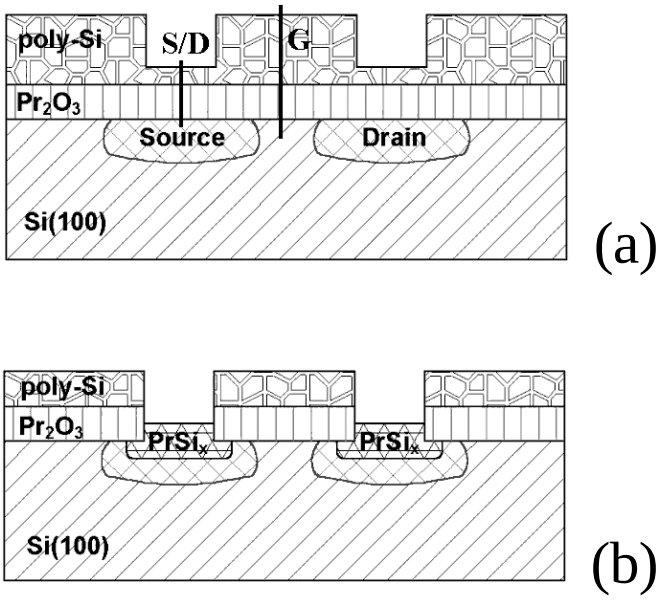

Figure IV.11. Two stages of the proposed process of source/drain contacts formation. a) Cross-sectional view of the as-deposited structure with Si partially etched away in the windows over source and drain areas. b) Cross-sectional view of the transistor structure after vacuum annealing. Pr silicide is formed on source and drain areas.

corresponding to source and drain. The thinning is aimed at leaving only one third or about 15 nm of Si, so that the cross-section S/D (source or drain) corresponds to ADP in fig. IV.9a and cross-section G (gate) to that in fig. IV.6. Annealing such a structure at 700°C for one hour in the vacuum environment of 10^{-6} mbar must yield the silicide at locations where Si overlayer was thinned and leave the dielectric film intact in all other places (fig. IV.11b). After annealing, the cross-section S/D will correspond to ADP in fig. IV.9c and cross-section G to that in fig. IV.7a. Therefore, a strong dependence of Pr_2O_3 thermal stability on the thickness of Si cap allows for an elegant silicidation process for source and drain areas. This has a potential for reducing the total number of process steps in the future CMOS technology that will have Pr_2O_3 as a gate dielectric.

IV.i. Summary of Pr_2O_3 thermal stability

A combined investigation of thermal stability of Pr_2O_3 films grown on Si(100) substrates by AES, XPS, and TEM has discovered a great application potential of these films. At 700°C, out-diffusion of Si from the substrate is so fast that it reaches the surface of a 13 nm thick Pr_2O_3 film in just a few minutes. No diffused Si was found in

unoxidised form inside the Pr_2O_3 films. Instead a Pr_2O_3-Pr_x-O_y-Si_z mixture is formed through partial Pr_2O_3 decomposition. The thermally induced changes in the Pr_2O_3/Si(100) system are qualitatively similar for anneals in vacuum and in N_2. However, the presence of N_2 is crucial for improving the thermal stability of Pr_2O_3 films with an amorphous Si cap. The Si/Pr_2O_3/Si(100) structure is transformed by 700°C vacuum annealing into a film of $PrSi_x$ with a smeared interface to Si(100) substrate. If vacuum annealing is done at 900°C then a Si-richer $PrSi_x$ phase is formed. However, when the capped film is annealed in N_2 it is completely stable at 800°C, only the Pr_2O_3 film is transformed into a crystalline Pr_2O_3-Pr_x-O_y-Si_z mixture at temperatures between 900°C and 1040°C. The $Pr_2O_3 \rightarrow PrSi_x$ transformation may be very convenient for making contacts to source and drain of the MOS transistor, should the latter utilise the Pr_2O_3 as a gate dielectric.

The investigation of thermal stability presented in this chapter hints on the positive prospects of Pr_2O_3 gate dielectric application. The ability of Si/Pr_2O_3/Si(100) structures to survive 800°C annealing in an N_2 environment (needed for $CoSi_2$ formation, see chapter VI) allows the usage of $CoSi_2$ contacts with Pr_2O_3-based MOS transistors. According to data of Osten and coworkers [20], the electrical characteristics of capacitors with Pr_2O_3 dielectric do not change after a rapid thermal annealing for 15 s at 1000°C in an N_2 environment. Therefore Pr_2O_3 high-K material should be compatible with the dopants drive-in annealing. All these facts indicate that Pr_2O_3 can successfully replace the SiO_2 gate dielectric in a standard materials combination of the modern CMOS technology.

Chapter V

Improved AES sputter depth profiling of W/WN_x and WSi_x layers on Si substrates

V.a. W/WN_x and WSi_x layers on Si substrates and their analysis

$W/WN_x/Si$ structures are proposed to be used as gate stacks in future generations of MOS transistors [41,47-48]. This seems to be an elegant solution, while keeping in mind that W remains a mainstream interlayer metal. It is very attractive to use the same basic element for both the actual contact to one of transistor's electrodes and for the interlayer connection. Such approach reduces the number of technological process steps during production, by eliminating the deposition of additional materials, which would be required otherwise (e.g. $W/TiN/TiSi_2/Si$ or $W/TiN/CoSi_2/Si$ structures). The WN_x layer serves as an effective diffusion barrier, which was already proven with Cu metallization and high-K gate dielectric [42-46,49]. This barrier must prevent any reaction between W and Si and also eliminate the penetration of other elements, which may contaminate the MOS transistor. WN_x can also be conveniently deposited by the CVD technique, thus being very appealing for aggressively scaled CMOS technologies [43,46,50,51]. However, successful implementation of this material requires the knowledge of distribution of chemical elements as a function of depth inside the $W/WN_x/Si$ structures. For such measurements Auger depth profiling is a suitable tool, but substantial artifacts can be induced by ion bombardment, including preferential sputtering and surface roughening [124-126]. The former can produce errors in the determination of elemental concentrations, and the latter can degrade the depth resolution of ADPs [127]. In order to get a more precise description of the real distribution of elements inside the sample, the artifacts mentioned above have to be minimised. Since Zalar introduced sample rotation it is associated with decreasing the surface roughness and improving the depth resolution for different systems [128]. But whether such an improvement will take place strongly depends on the preferential sputtering and the crystalline structure of the investigated sample [129].

In the following, the results of AES depth profiling of $W/WN_x/poly\text{-}Si$ structures are presented in comparison with $WSi_x/poly\text{-}Si$ structures [52]. The latter are also of

interest for advanced MOS devices, since large grain sized WSi_x (dubbed NICE WSi_x) could be obtained with resistivity three times lower than the conventionally known value [130]. Both structures were deposited on top of the SiO_2/Si(100) substrate, thus modelling a complete stack of a MOS transistor. The ADPs of these structures were obtained by sputtering the samples with 1 keV and 4 keV Ar^+ ions, both with stationary and rotating (1 rpm) samples. Like expected, using lower energy sputtering helped improve the depth resolution on the ADPs. In the mean time sample rotation did not improve the ADPs of the WSi_x/poly-Si structures, but produced a kind of improvement on the ADPs of the W/WN_x/poly-Si structures, which required careful interpretation. These phenomena will be discussed in this chapter together with their possible explanations.

V.b. W/WN_x films

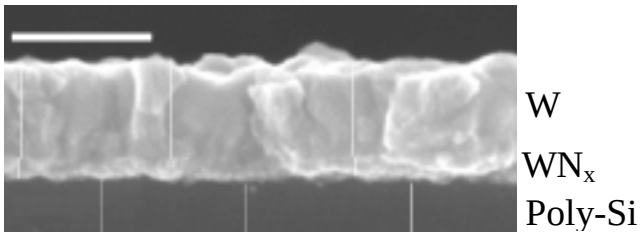

Fig. V.1. SEM image of a typical W/WN_x/Si structure cross-section (the white thick horizontal marker is a 100 nm scale, white vertical lines approximately indicate W, WN_x, and poly-Si regions).

Fig. V.1 shows the SEM image of a typical CVD-deposited W/WN_x film on top of a polysilicon layer. It reveals a roughness of ~10 nm at the WN_x/Si interface. The ADPs of this structure obtained with 1 keV or 4 keV Ar^+ ions and with stationary or rotated sample (figs. V.2-3) show the distributions of O, N, W and Si plotted as function of depth. The following transitions were used for quantitative analysis: N (KLL, 379 eV), O (KLL, 503 eV), Si (KLL, 1619 eV), W (MNN, 1736 eV). Non-zero levels of N and Si in the W film and N, O and W in the Si substrate are observed on all four ADPs (figs. V.2-3). These levels were below AES sensitivity limits (or offset levels) and therefore do not reflect the real concentrations, any of which could be anywhere between zero and the offset level. Composition versus sputtering time was transformed into

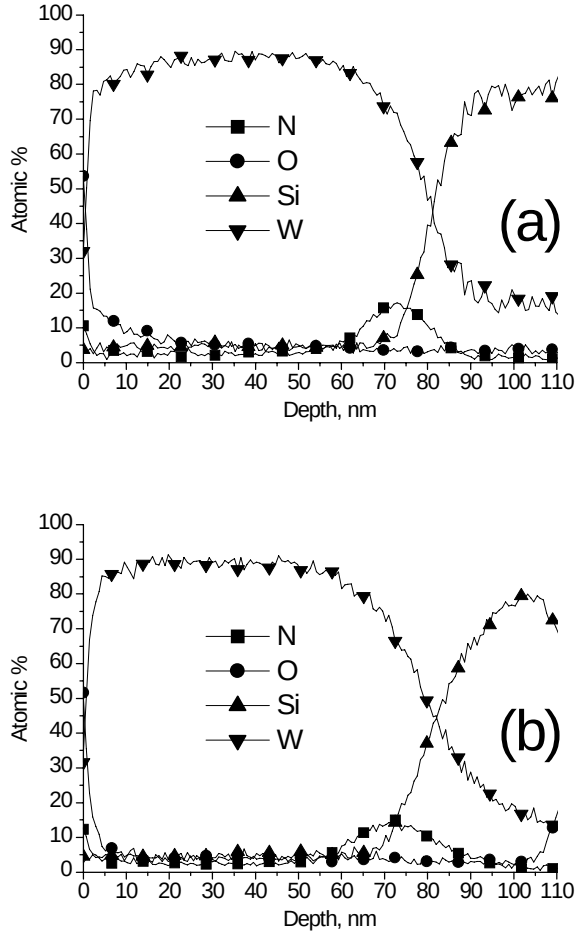

Fig. V.2. ADPs of the structure shown in fig. V.1, obtained when the sample was a) rotated and sputtered with 1 keV Ar^+ ions, b) stationary and sputtered with 1 keV Ar^+ ions. Rotation improves the depth resolution of ADP.

composition versus depth on the basis of the SEM image. Measured interface width, WN_x layer thickness, and the maximum N concentration in this layer are presented in Table V.1 together with corresponding sputtering conditions. The interface width between W/WN_x and Si was assumed to be the distance between the points where Si concentration is 0.9 and 1.1 of the substrate and noise levels, respectively. The thickness of the WN_x layer (enriched layer) was assumed to be the distance between the points where N concentration is half the maximum in this layer. An overview of Table V.1 shows that both rotation and lower ion energy produce sharpening of ADPs if applied separately. The improvement is even stronger when both are combined.

An important observation can be made regarding oxygen profiles presented in figs. V.2-3. The measured O concentration inside the W film was higher when the

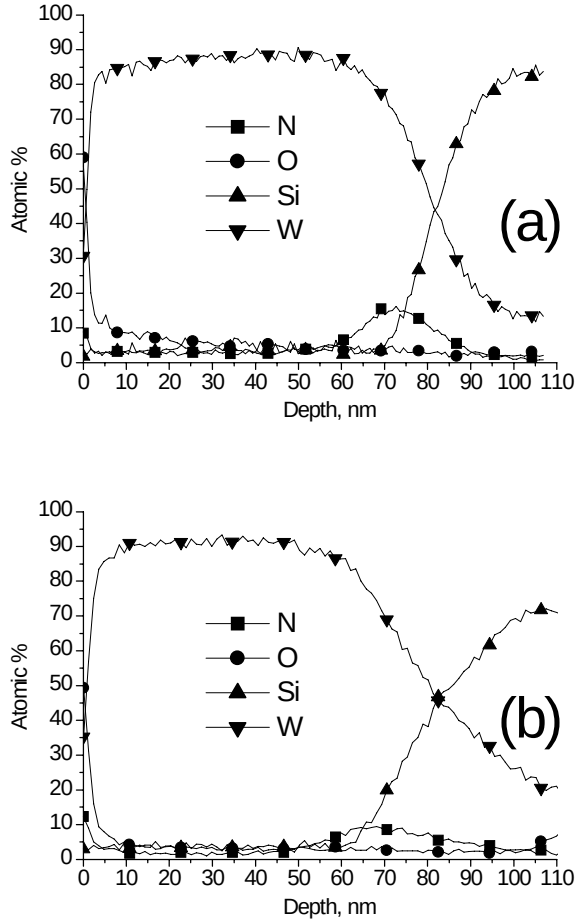

Fig. V.3. ADPs of the structure shown in fig. III.1, obtained when the sample was a) rotated and sputtered with 4 keV Ar^+ ions, b) stationary and sputtered with 4 keV Ar^+ ions. Rotation improves the depth resolution of ADP.

Table V.1

Sputtering condition	W/Si interface width	WN_x thickness	Max. N concentration
Rotated 1 keV Ar^+	18 nm	18 nm	17 %
Stationary 1 keV Ar^+	26 nm	24 nm	15 %
Rotated 4 keV Ar^+	20 nm	21 nm	16 %
Stationary 4 keV Ar^+	39 nm	32 nm	10 %

sample was rotated during analysis, as compared to stationary sample. Fig. V.4 shows an enlarged view of O profiles obtained when the sample was sputtered with 4 keV ions. The difference between these two profiles can be interpreted according to two scenarios: i) There is a thin layer of tungsten oxide on the surface (resulting from sample exposure to ambient environment), and the measured O profile looks sharper when profiling is

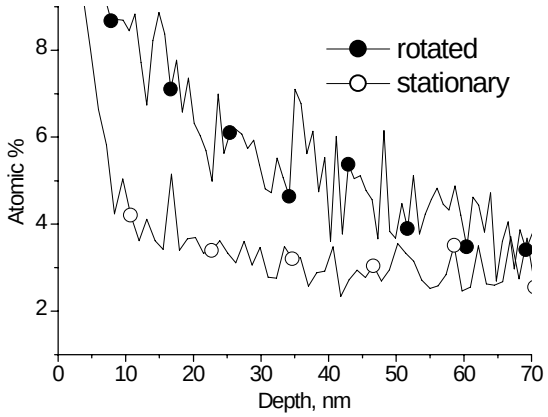

Fig. V.4. Enlarged view of O profiles from fig. V.3. An impression is created that O profile is not sharpened like of other elements, when measured with rotation, but smeared instead.

done on the stationary sample than on rotating one. That would seem rather strange, because for all other elements (W, Si, and N) exactly the opposite is the case. Such a scenario would require an explanation why does sample rotation smear the O profile. ii) O was inherently present (most likely in the form of some tungsten oxide resulting from impurities in the CVD growth) both on the surface and in the bulk of the W film, but could be detected better when the sample is rotated. In other words, the intensity of the O signal is higher when measured on the sample which is rotated during sputtering. In the following the shape of O profiles will be explained after presenting a comparative AES and AFM measurements of another $W/WN_x/Si$ sample.

The ADPs of the W/WN_x film with much smaller N concentration in the enriched layer are shown in fig. V.5. The ADPs of the structure were obtained by sputtering with 4 keV Ar^+ ions of the rotated sample (fig. V.5a) and of the stationary one (fig. V.5b). As it is obvious from figs. V.5a-b, rotation caused a dramatic sharpening of elemental profiles – the interface width (expressed in the sputtering time) is 1.1 min (fig. V.5a) and 2.9 min (fig. V.5b). The enlarged view of O profile for both rotated and stationary samples is given in fig. V.6a, and the same for N in fig. V.6b. An important difference from the previous sample is that the N enriched layer also had an increased O concentration (fig. V.6a). The similarity between the samples in figs. V.1-6 is, that the level of O in the W film appeared higher when profiled with rotation. One can clearly see that the O profile in the enriched layer is sharper for the rotated sample than for the stationary one. Thus, figs. V.5-6 unambiguously prove that sample rotation leads to

sharper elemental profiles of all four elements: W, Si, N, and O, which are present in the $W/WN_x/Si$ structures. Therefore, a correct interpretation of fig. V.4 is not the smearing of O profile. Rather, when the sample is rotated, better measurement conditions exist for detection of O which is present in W.

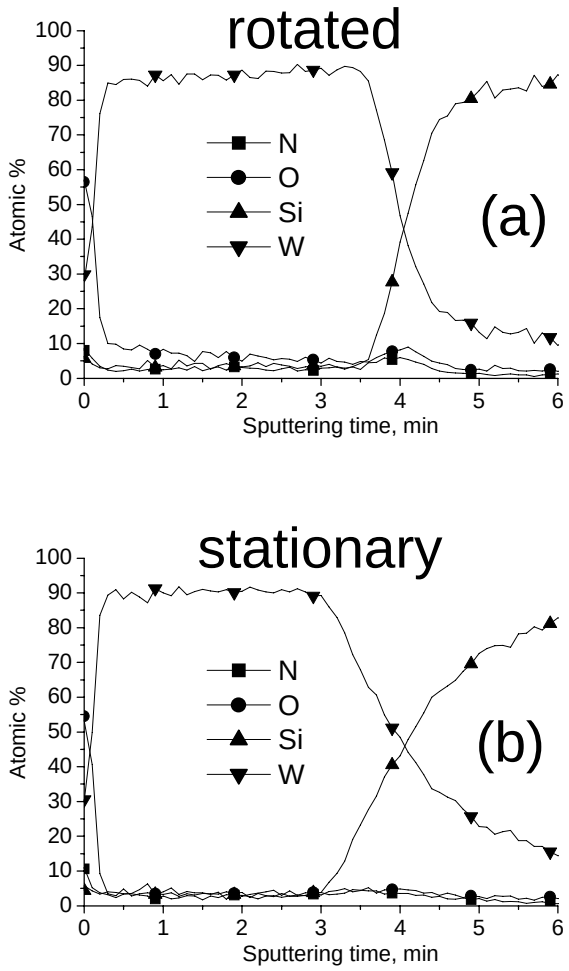

Fig. V.5. ADPs of the $W/WN_x/Si$ structure (N enrichment lower than for sample in figs. V.1-4) obtained with the sample a) rotating and b) stationary; Ar^+ ion energy was equal to 4 keV. Rotation improves the depth resolution of ADP.

A series of AFM images of the same sample as in figs. V.5-6 were obtained after ion sputtering in the same conditions as during depth profiling. The images were taken in an ambient environment using the tapping mode of AFM operation. It is interesting to compare the surface topography after the sputtering reached the interface between the film and the substrate when the sample was rotated (fig. V.7a), and when it was stationary (fig. V.7b). One can see a lower surface roughness in the case of rotation.

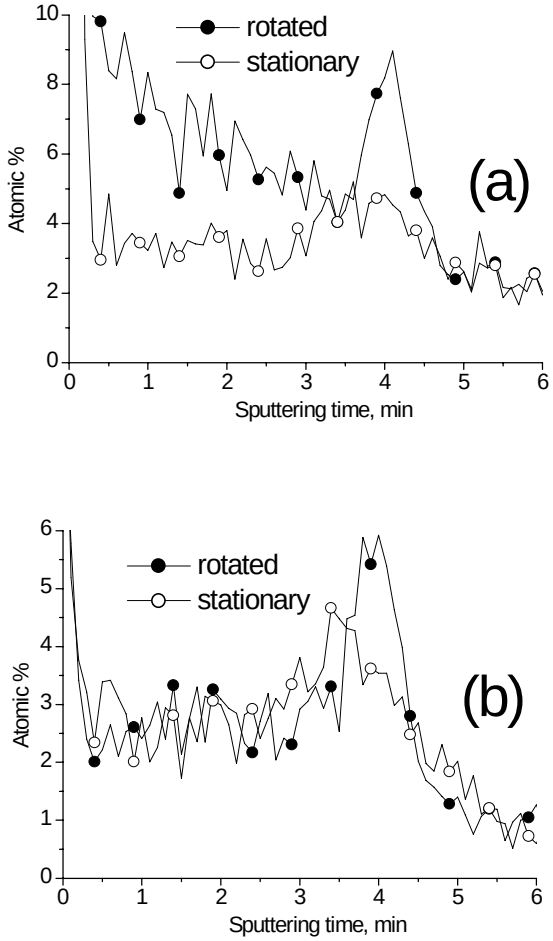

Fig. V.6. Enlarged elemental profiles from fig. V.5. a) O profile, b) N profile. Like the N profile, also the O profile is more sharp when measured with sample rotation. The seemingly smeared initial part of O profile is due to better detection conditions for O when the sample is sputtered with rotation.

This correlates well with a sharpening of ADPs, or equivalently with a depth resolution improvement due to sample rotation. Table V.2 shows a dependence of the surface root-mean-square roughness as a function of sputtering time with and without rotation. Every roughness value was calculated from a separate AFM image and all together they suggest a monotonic increase of roughness with sputtering dose. When the sample is rotated during sputtering this increase is much faster than when the sample is stationary. For rougher surfaces, the AES spectrum stems from species belonging to a wider depth range. Consequently, when the surface is smoother the obtained information is less smeared over the depth. The sharpening of ADPs in figs. V.2a,3a,5a, as compared to ADPs in figs. V.2b,3b,5b can be easily understood in this light. Equivalently the depth profiles have higher depth resolution in the case of rotation than without it.

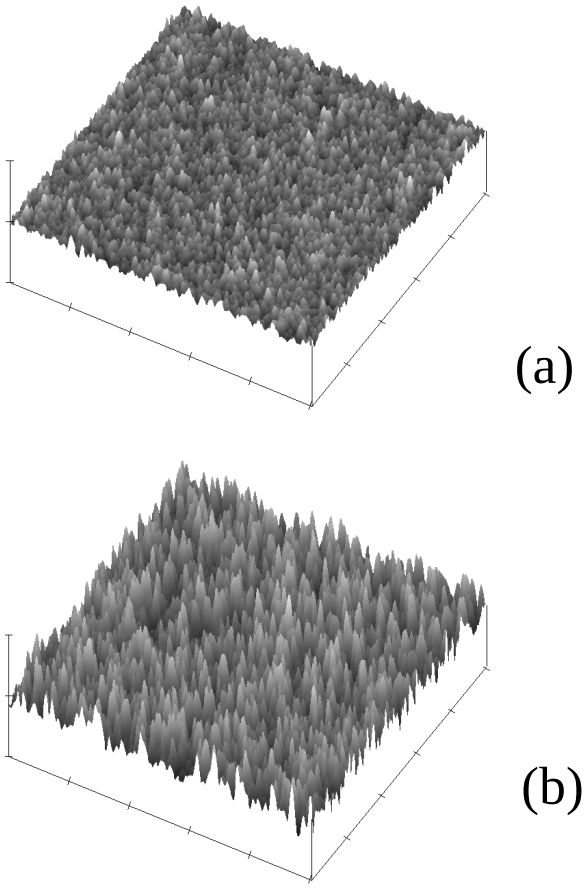

Fig. V.7. AFM images of the W/WN_x film (the same sample as in figs. V.5-6) sputtered with 4 keV Ar^+ ions to the depth of the interface with polysilicon substrate: a) when rotation was applied during sputtering, b) when the sample was stationary; on both images the vertical scale is 50 nm/division, the horizontal scale is 1 μm/division.

Table V.2

Sputtering time, min	RMS roughness (stationary)	RMS roughness (rotated)
1.5 min	3.127 nm	2.127 nm
3 min	6.147 nm	2.203 nm
4.5 nm	8.904 nm	2.736 nm

The definition of depth resolution would require of course a sample with guaranteed atomically sharp interface. Then the measured interface width equals the depth resolution of the technique. The samples investigated in this work do not have atomically sharp interfaces, but provided the sample is identical, a technique of better depth resolution will yield an ADP with sharper interfaces and more pronounced layers of a distinct chemical composition. In the given case a procedure of obtaining ADPs on

rotated samples is a technique with higher depth resolution than the procedure involving stationary samples.

At this point, it only remains to explain an unusual shape of O profiles in fig. V.4. One can speculate that lower O signals in the case of rougher surfaces attributed to stationary samples (figs. V.4,6a) may be due to strong preferential sputtering of O in the unexposed layers (fig. V.8). When a single Ar^+ ion collides with the surface, it creates

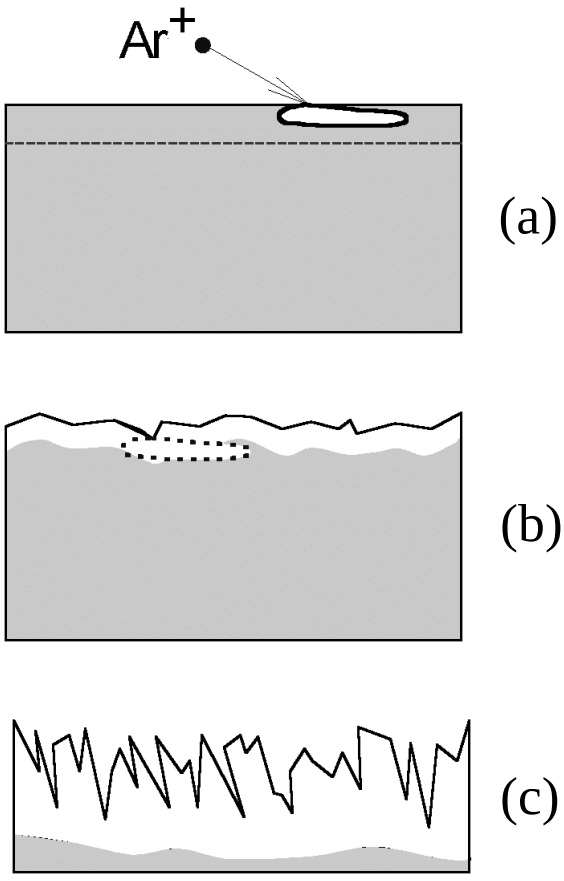

Fig. V.8. Preferential sputtering of O in the unexposed layers. a) Qualitative representation of single ion's impact during sputtering, the area depleted of O is shown in white, Auger electrons escape depth is shown by a broken curve. b) O depletion layer in the case of smooth sputtered surface, O is still present within the Auger electron escape depth. c) O depletion layer in the case of rough sputtered surface, O is already beyond the AES analysis depth.

an irregularly shaped region (shown by white color), which is depleted of O. In fig. V.8a a case is shown when the depth of this region is smaller than the Auger electrons escape depth (designated by a broken curve). When the surface is relatively smooth (while rotated during sputtering) all impinging ions collide with the surface at approximately

the same depth. These collisions result in O depleted layer (shown in white), which is still shallower than the layer from which Auger electrons can escape (fig. V.8b). When the surface is very rough (sputtered without rotation), some impinging ions start their collision cascades at the deepest exposed locations. Assuming that the lateral spread of the cascades is sufficient, the O atoms are removed deeper than the Auger electrons escape depth (fig. V.8c). In this way an O depleted subsurface region is created and it recedes together with the sputtered surface. As a result, the rougher the surface has become – the lower O signal will be detected by AES, which is the situation observed in figs. V.4 and V.6a.

V.c. WSi_x films

The second topic of this chapter was the investigation of WSi_x films on polysilicon substrates. Because of substantial changes induced by heat treatment in the crystalline condition of these films, the as-deposited and heat treated films were separately investigated. Figs. V.9-10 show the ADPs of the CVD as-deposited WSi_x film. The ADP shown in fig. V.9a was obtained with rotated sample sputtered with 1 keV ions, fig. V.9b shows the ADP obtained with a stationary sample and the same ion energy. The same sample was also profiled with 4 keV ions (fig. V.10), producing the ADPs for sputtering with rotation (fig. V.10a) and without it (fig. V.10b). Obviously there is no observable influence of sample rotation on the shape of ADPs. The interface width between WSi_x and Si was assumed to be the distance between the points where Si concentration is 0.9 and 1.1 of the levels in the substrate and the film, respectively. This width of the interface between the silicide and polysilicon is 12 nm (fig. V.9a), 13nm (fig. V.9b), 12 nm (fig. V.10a), and 13 nm (fig. V.10b). Such small differences are insignificant and can be attributed to noise. Thus, it is possible to conclude that rotation does not sharpen the profiles and does not improve the depth resolution in this case. That is usually expected for amorphous material, and the state of the as-deposited WSi_x film was amorphous, as seen on the SEM cross-sectional image in fig. V.11. Lowering the ion energy from 4 keV (figs. V.10) to 1 keV (figs. V.9) has changed the detected Si/W concentrations ratio from 0.49 to 0.39 inside the silicide film. Such values were obtained due to preferential sputtering of Si, as an element with atomic weight lower

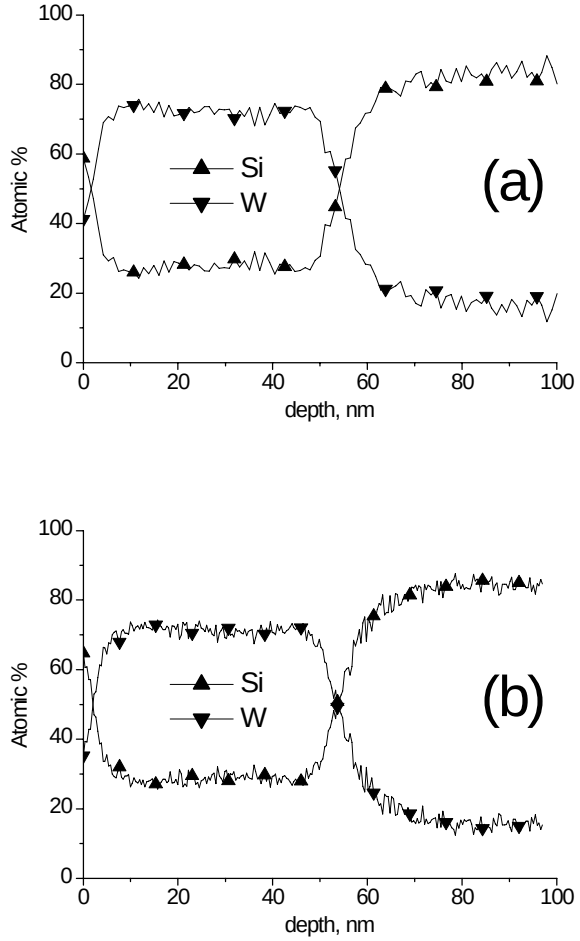

Fig. V.9. ADPs of the as-deposited amorphous WSi_x film on the polysilicon substrate obtained with 1 keV Ar^+ ions, on a) rotated and b) stationary sample. Rotation does not have any significant effect on ADP.

than W [131]. The preferential sputtering was very severe, since the actual Si/W ratio did not deviate from 2 by more than 10 atomic percents. This can be seen at zero depth on the ADPs in figs. V.9-10, i.e. in the points where composition was measured before any sputtering took place. When the sample was sputtered, its surface was gradually depleted of Si until the sputtering yields of Si and W became proportional to their concentrations in the bulk of the film and their surface concentrations stabilised. These stabilised concentrations remained unchanged at a depth between approximately 10 and 50 nm. The stabilised concentration of Si was ~28% (Si/W concentration ratio equal to 0.39) after 1 keV ion bombardment (fig. V.9) and ~33% (Si/W concentration ratio equal to 0.49) after 4 keV ion bombardment (fig. V.10). A comparison was made between these values and the stabilised concentration of Si after 1 keV ion sputtering of the reference WSi_2 sample, the composition of which was confirmed by Rutherford back

scattering (RBS). The 36% (Si/W concentration ratio equal to 0.56) value obtained for the reference sample can assure that the investigated WSi_x film is indeed no more than 10% different from the WSi_2 compound.

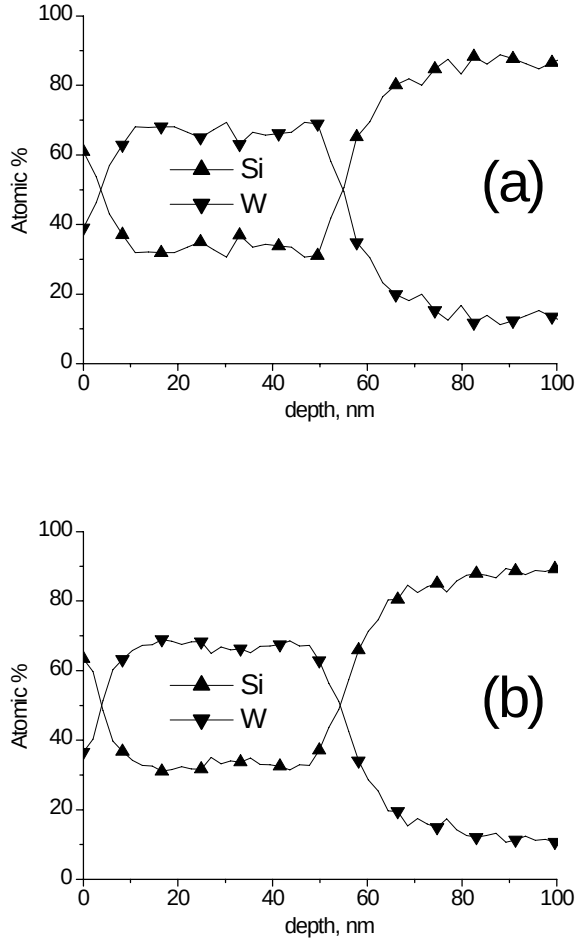

Fig. V.10. ADPs of the as-deposited amorphous WSi_x film on the polysilicon substrate obtained with 4 keV Ar^+ ions, on a) rotated and b) stationary sample. Rotation does not have any significant effect on ADP.

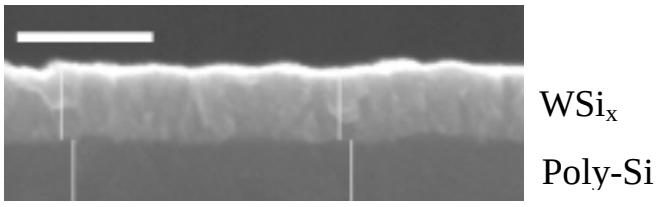

Fig. V.11. SEM micrograph of the film's cross section, whose ADPs are shown in figs. V.9-10 (the white thick horizontal marker is a 100 nm scale, white vertical lines approximately indicate WSi_x and poly-Si regions).

The next point of investigation was the WSi_x sample annealed after deposition. The annealing was performed at 1080°C during 1 minute in the O_2 gas under atmospheric pressure and it simulated one of the steps in CMOS technology process sequence. The stochiometry was close to WSi_2 (again based on comparison with the reference sample mentioned above). Fig. V.12a shows the ADP for rotated sample sputtered with 1 keV Ar^+ ions, fig. V.12b - for stationary sample and 1 keV ions, fig. V.13a - for rotated sample and 4 keV ions, and fig. V.13b - for stationary sample and 4 keV ions. From the profiles in figs. V.12-13, it is obvious that during annealing Si diffuses to the reaction surface and forms a surface layer of silicon oxide together with O available in the process [132]. Another effect of annealing is grain growth in the WSi_x film, so that it becomes polycrystalline, as revealed by SEM image in fig. V.14. At the

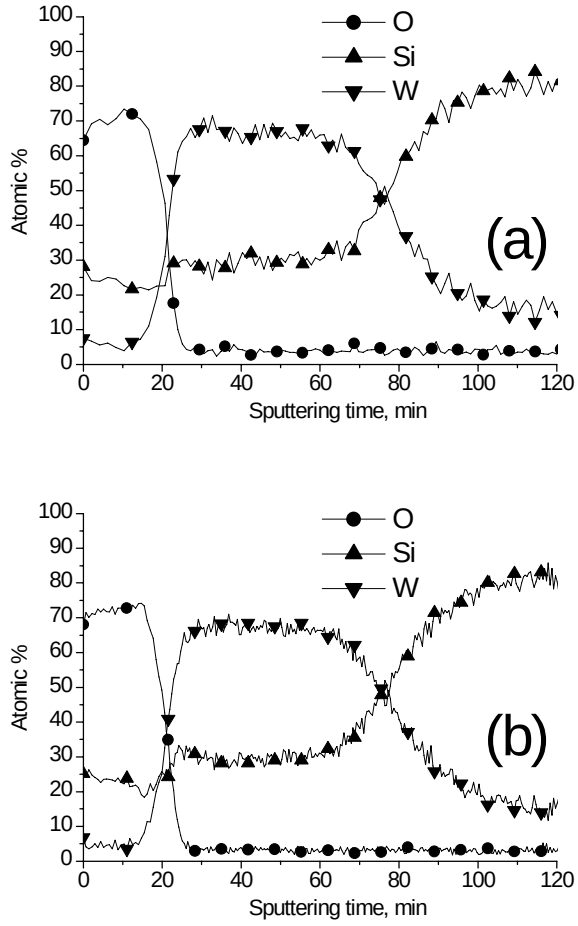

Fig. V.12. ADPs of the polycrystalline WSi_x film on the polysilicon substrate obtained with 1 keV Ar^+ ions when the sample was a) rotating and b) stationary. Rotation does not have any significant effect on ADP.

ADPs in figs. V.12-13 the width of the interface between WSi_x and Si is: 25 nm (fig. V.12a), 27 nm (fig. V.12b), 34 nm (fig. V.13a), and 36 nm (fig. V.13b). It is important to point out that the interface width at ADPs in fig. V.12 is about the interface roughness observed at the SEM image in fig. V.14. Surprisingly, the ADPs of the polycrystalline WSi_x film are practically not influenced by rotation - similar to amorphous film. This opposes intuitive expectation that a significant improvement must come from the more uniform sputtering of the differently oriented crystalline grains when the sample is rotated. The absence of improvement may be caused by preferential sputtering of Si (Si/W concentration ratio is 0.46 in fig. V.12, and 0.53 in fig. V.13). In the process of sputtering, a Si depleted layer is present on the film surface. It moves together with the surface as it recedes, and when the substrate is approached, the presence of such a Si depleted region would smear out an otherwise abrupt interface. This effect may

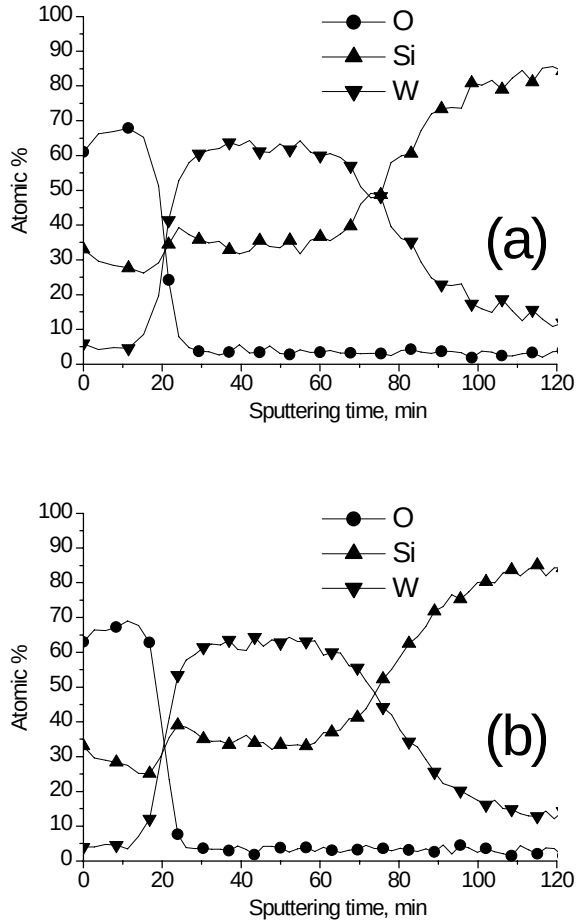

Fig. V.13. ADPs of the polycrystalline WSi_x film on the polysilicon substrate obtained with 4 keV Ar^+ ions when the sample was a) rotating and b) stationary. Rotation does not have any significant effect on ADP.

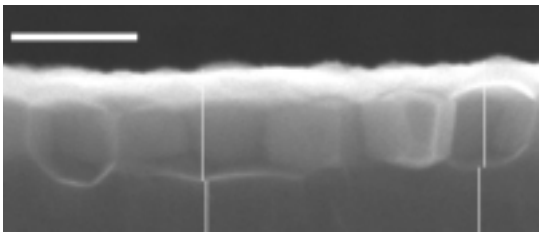

Fig. V.14. SEM micrograph of the film's cross section whose ADPs are shown in figs. V.12-13 (the white thick horizontal marker is a 100 nm scale, white vertical lines approximately indicate silicon oxide plus WSi_x and poly-Si regions).

substantially reduce the depth resolution gain associated with sample rotation. The primary ions of higher energy penetrate deeper into the material, making the depleted layer thicker – a reason why the ADPs in fig. V.13 are more smeared than in fig. V.12. At the same time such a difference between the ADPs in figs. V.9-10 was not found. It is only possible to speculate that in the given ion energy range (1-4 keV) the Si depleted layer in the amorphous WSi_x does not change as the ion energy is varied. The influence of the ion energy on the thickness of this layer is only pronounced in polycrystalline WSi_x. That is why a lower primary ion energy may give a sharper ADP of the polycrystalline WSi_x film on polysilicon substrate. The increased error in elemental concentrations, associated with lower energy sputtering, is not problematic, since the preferential sputtering is very strong in all cases. The true composition of the sample is anyway determined through comparison with standards of known stochiometry. Therefore, it is advantageous to use the ions of lower energy for WSi_x films depth profiling.

V.d. W/WN_x and WSi_x analysis summary

The ADPs of $W/WN_x/Si$ and WSi_x/Si structures are influenced differently by sample rotation during sputtering. The depth resolution of elemental profiles is improved as a result of rotation in $W/WN_x/Si$ structures, but not in the WSi_x/Si structures. The sensitivity to O inside the W/WN_x film is improved when the surface is sputtered and the sample is rotated. The AFM investigation of the $W/WN_x/Si$ structures after sputtering reveals a reduced surface roughness with sample rotation, which leads to better depth resolution and higher O sensitivity. In contrast, the elemental profiles of

WSi_x films, both in amorphous and polycrystalline states (as revealed by SEM), are practically unchanged with or without rotation. This is caused by a Si depletion layer under the sputtered surface, which smears out the transition from silicide to silicon.

Lowering the sputtering ion energy from 4 keV to 1 keV improves the depth resolution in ADPs of $W/WN_x/Si$ structures and in polycrystalline WSi_x / polycrystalline Si structures, but not in ADPs of amorphous WSi_x / polycrystalline Si structures. The surface composition of the WSi_x/Si is altered stronger by 1 keV ions than by 4 keV ions, and a greater error is present in elemental concentrations when the silicide film is profiled with lower energy ions.

These results highlight the potential importance of rotation and careful ion energy selection for measuring and interpreting ADPs of the modern MOS structures.

Chapter VI

Multitechnique control of the Co SALICIDE process

VI.a. Self-aligned silicide process based on Co silicide

$CoSi_2$ is a material of choice for contacts between the Si parts of MOS transistors and metal interconnects in the latest generations of integrated circuits [7]. It has even more room for improvement if a complete silicidation of the gate electrode is performed [133]. This means that the $CoSi_2$/poly-Si gate stack is replaced by a single $CoSi_2$ layer on top of the gate dielectric. The extremely low sheet resistance of such a gate electrode will allow its usage in aggressively scaled MOS devices [53], which will probably utilise a high-K material as a gate dielectric. Thus, $CoSi_2$ is a potential universal contact platform for integration of Pr_2O_3-based MOS transistors. The contacts themselves can be formed by a self-aligned silicide (SALICIDE) process, in which no patterning of deposited Co film is required [1,54-55]. The silicide is produced only at locations, where Co is in direct contact with Si. For this, only one patterning step is necessary on the SiO_2 mask, covering the surface of the Si wafer. The holes in this mask are etched away over the source, drain and/or gates terminals of the MOS transistors. The Co SALICIDE process includes several steps [1,54-55]: i) Deposition of Co with an optional capping layer such as TiN, which is often used for prevention of oxygen contamination during annealing and improving the uniformity of the targeted silicide. ii) First rapid thermal annealing (RTA1), for silicidation of the deposited Co with Si in an N_2 environment. The silicide phase observed after this step is typically CoSi or its mixture with Co_2Si. iii) Wet etching, which selectively removes TiN and non-reacted Co if any. iv) RTA2 at higher temperature in an N_2 environment, which transforms the film from CoSi to $CoSi_2$ with targeted low resistivity.

In order to obtain a high quality $CoSi_2$ film, which is uniform and of targeted thickness, structure, and composition, it is necessary to control every stage of the silicidation process. For this purpose AES is a good tool, which determines the chemical composition and is capable of depth profiling. However, the latter can be complicated by preferential sputtering in Co silicides [VI.5-6], similar to what was described in chapter V

for WSi_x compounds. This drawback is not problematic if the extent of preferential sputtering is known for the given experimental condition. Such knowledge can be achieved through calibration measurement of standard samples, whose composition is well known. After such calibration AES depth profiling can provide information on chemical composition, spatial uniformity and thickness of the Co silicide film. In a production environment a spectroscopic ellipsometry (SE) [57] is mostly convenient for process control as a reliable in-line and non-destructive method that allows mapping of film thickness across Si wafers. However, refractive index (RI) dispersion models for ellipsometric data interpretation are required to provide a determination of Co silicide film thickness and to simulate film reflectivity for optical lithography. These models are created on the basis of SE calibration measurements, done on standard samples, which are confirmed by AES to have a chemically and spatially uniform silicide film. Currently, information on optical constants of thin CoSi films as a function of wavelength is not available in the literature, but it is required to build their dispersion models. Most studied are bulk silicides, in particular $CoSi_2$ [136-144]. The optical constants of CoSi are not widely investigated and only data for 632.8 nm wavelength are presented in the literature [143-144]. Therefore, a chain of calibration measurements (as outlined above) is required to build dispersion models for Co and $CoSi_x$ films and apply these models during production scale SE control of the Co SALICIDE process.

The goal of investigation described in this chapter was to perform reference measurements on Co_2Si, CoSi, and $CoSi_2$ phases for calibration of AES and SE techniques. In the following a quantitative characteristic of preferential sputtering in all three phases by 1 keV Ar^+ ions will be presented [56]. These data allow for correct interpretation of AES depth profiling results. The reference samples were also used for creation of automatic SE thickness measurement procedure and applied on the CMOS technology production line. For this purpose the optical parameters of Co, CoSi, and $CoSi_2$ were measured by SE as a function of wavelength.

VI.b. As-deposited structures (TiN/Co/Si)

Before the as-deposited structures will be analysed it is necessary to consider the AES analysis of TiN capping. The compounds containing both Ti and N represent a certain difficulty for AES, because N KLL peak is superimposed by a component of Ti LMM peak. This overlapping is illustrated in fig. VI.1, where peaks from pure Ti and Si_3N_4 are presented. The LMM peak of Ti is a triplet, in which the component overlapped by N is designated as Ti1. The neighboring component of higher energy (designated as Ti2) is not effected by overlapping. As it was discussed in chapter II, a peak-to-peak intensity is required for every element whose concentration needs to be quantified. For Ti it is of no

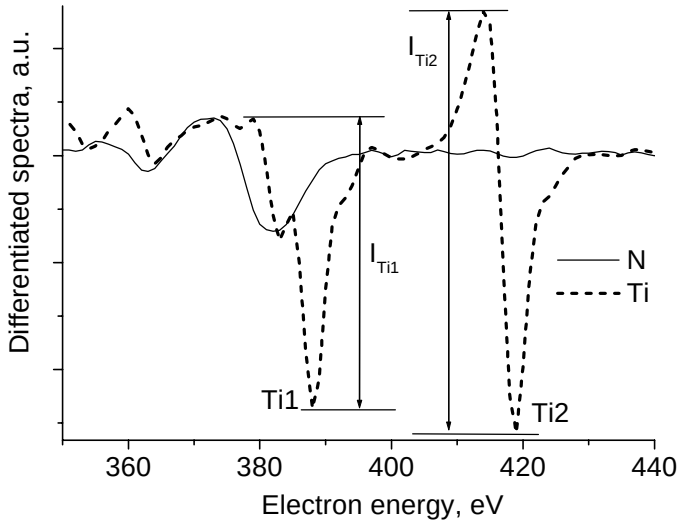

Fig. VI.1. Overlapping of Ti LMM and N KLL peaks in the differentiated AES spectrum. The Ti2 component can be used for measurement of Ti concentration, when N is also present in the sample. The only N KLL peak is completely superimposed by Ti1 component.

difficulty to use the Ti2 component for quantification, but the only N KLL peak is indistinguishable in pure form when Ti is also present in the sample. There are several approaches to solve this problem [145-147], of which the simplest empirical one was employed [147]. The essence of this approach is comparison of measured peak-to-peak intensities for Ti1 and Ti2 in the actual investigated sample. Should any N be present, it will distort the shape of Ti1 component and therefore change its peak-to-peak intensity.

Having a series of calibration samples with a varying ratio C_N/C_{Ti} of N and Ti concentrations, one can obtain an empirical dependence of this ratio on the measured I_{Ti1} and I_{Ti2} intensities. The chemical composition of the calibration samples can be established by an independent technique, for which the XPS is an excellent choice, being able to measure Ti and N concentrations independently. This can be done through measurement of N 1*s* and Ti $2p_{3/2}$ lines (binding energies equal to ~ 397 eV and ~ 455 eV correspondingly). In general the XPS is a very good tool for analysis of laterally uniform TiN layers, i.e. cases when a high lateral resolution is not required. However, analysing modern IC device structures may require resolving chemically distinct areas less than 1 μm in size. In such cases AES technique can be a "front line" analysis tool which provides the necessary lateral resolution on actual samples, while the given AES spectrometer will be calibrated with specially prepared laterally uniform samples of known chemical composition confirmed by XPS. For the spectrometer used in the present work this procedure yielded the ratio of N and Ti concentrations according to the formula:

$$C_N/C_{Ti} = (\alpha I_{Ti1} - I_{Ti2})^2/4I_{Ti2}^2, \text{ where } \alpha \approx 1.5 \quad \text{(VI.1)}.$$

The value of α is essentially a ratio of peak-to-peak intensities I_{Ti2}/I_{Ti1} for the pure titanium weighed by an instrumental factor which reflects the difference in analyser's sensitivity at the energies of Ti1 (388 eV) and Ti2 (419 eV) components.

In the case when elements other than Ti and N are present in the sample, one has to calculate the derived intensity of the N KLL peak, which would have been measured in the absence of overlapping. This derived intensity can be obtained using (II.10) and (VI.1) under the assumption that the Ti2 component is not influenced by contributions from other elements:

$$I_{Nderived} = C_N S_N I_{Ti2}/C_{Ti} S_{Ti2} = S_N(\alpha I_{Ti1} - I_{Ti2})^2/4S_{Ti2} I_{Ti2} \quad \text{(VI.2)}.$$

A thus-derived peak-to-peak intensity can be used along with other intensities to determine the partial concentrations of all relevant elements according to (II.11):

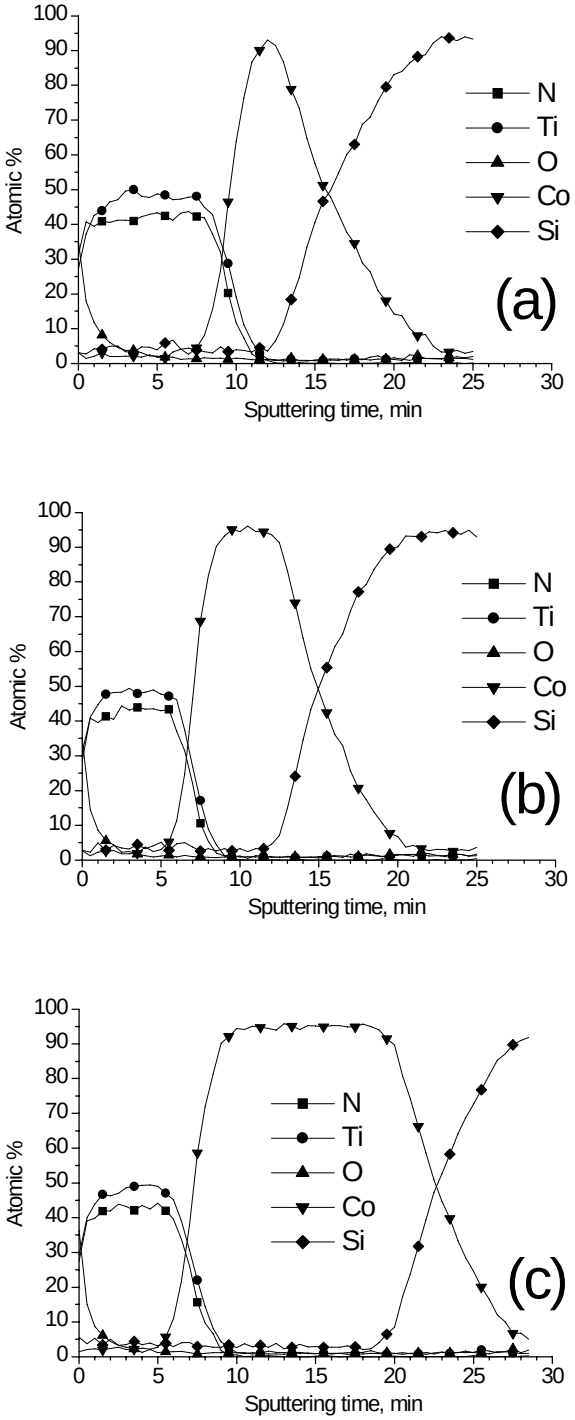

Fig. VI.2. ADPs of the as-deposited structures with initial Co thickness of (a) 10nm, (b) 20 nm, and (c) 35 nm. Every Co film was capped by a 15 nm thick TiN cap layer. Both Co and TiN were deposited by PVD technique.

$$c_N = 100 \times I_{Nderived}/S_N NORM \quad (VI.3a),$$

$$c_{Ti} = 100 \times I_{Ti2}/S_{Ti2} NORM \quad (VI.3b),$$

$$c_X = 100 \times I_X/S_X NORM \quad (VI.3c),$$

$$NORM = I_{Nderived}/S_N + I_{Ti2}/S_{Ti2} + \Sigma I_X/S_X \quad (VI.3d).$$

The following AES transitions were used for a quantification of elements other than N or Ti: Co (LMM), Si (KLL), and O (KLL). The calculation scheme outlined above was used to obtain the ADPs of as-deposited layered structures, shown in figs. VI.2a-c. Co films of 10, 20 and 35 nm nominal thickness were deposited on Si (100) substrates (kept at 200°C) followed by TiN protective cap (15 nm) in the same physical vapour deposition (PVD) chamber.

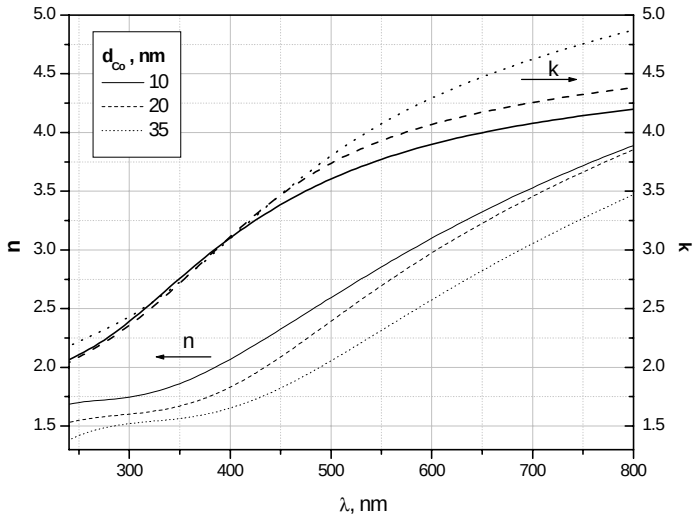

Fig. VI.3. Optical parameters n and k (real and imaginary parts of refractive index) of the Co films with 10, 20, and 35 nm thickness. The difference between optical parameters of different samples may be a result of varying Co film density.

The optical properties of the Co films were measured by SE in the wavelength range of 230-800 nm on an advanced spectroscopic ellipsometer (KLA-TENCOR UV1280). This is a production-oriented, completely automated, small-spot ($14 \times 22 \mu m^2$) tool with a 70° angle of incidence. The refractive index dispersion of the Co films inside of the TiN/Co double-layer stack is shown in fig. VI.3, where the real (n) and imaginary (k) parts are

given as a function of wavelength. An observed dependence of n and k on Co film thickness may be a result of a varying film density, as was previously considered for other metal films [148-149].

VI.c. First silicidation step

The ADP in fig. VI.4 shows the sample with initial 10 nm Co thickness after the RTA1 at 550°C during 30 s. The algorithm for obtaining atomic concentrations was the same as in the previous section. One can see that some Co silicide has been formed,

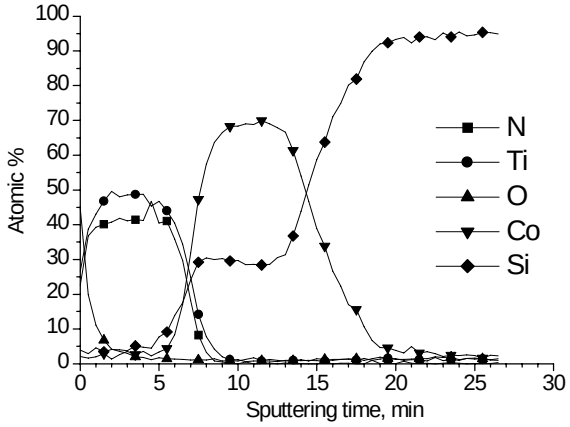

Fig. VI.4. ADP of the structure with 10 nm initial Co thickness after RTA1 at 550°C during 30 s. Si has diffused into the film and Co silicide was formed.

however its exact stochiometry is not readily clear from this ADP due to preferential sputtering. In order to elucidate this issue, one needs to analyse the samples without protective TiN cap. Figs. VI.5a-c show the ADPs of the sample with initial 10 nm of Co after 30s of RTA1 at 435°C, 450°C, and 550°C respectively after the selective etching (performed in $NH_4OH/H_2O_2/H_2O$, which removed TiN and any unreacted Co). The surface concentration in the beginning of ADP is not yet altered by sputtering. It corresponds to stochiometric CoSi in the 550°C sample, but deviates from this value for lower RTA1 temperatures.

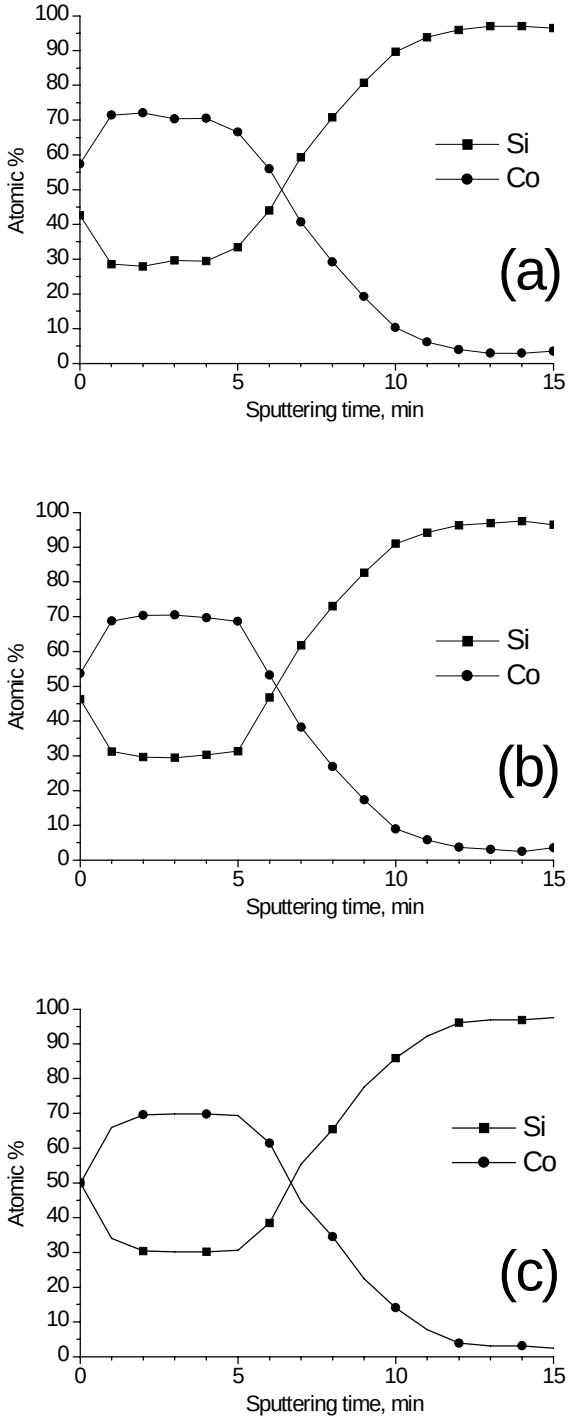

Fig. VI.5. ADPs of the structure with 10 nm initial Co thickness after selective etching, subjected to 30 s of RTA1 at (a) 435℃, (b) 450℃, and (c) 550℃. The bulk of the silicide is identical in all three samples, but its surface composition depends on RTA1 temperature.

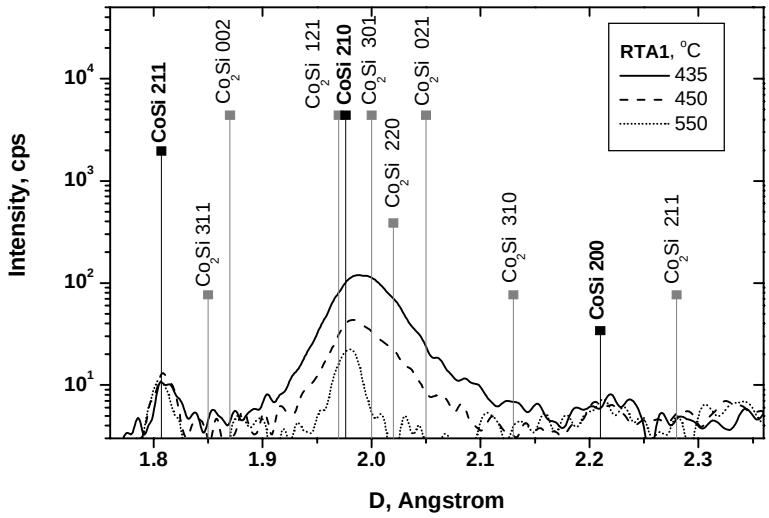

Fig. VI.6. XRD scans of the samples from fig. VI.5 obtained with Cu Kα radiation. A pure CoSi phase is detected in 550°C sample, but a mixture of CoSi and Co_2Si is present in samples with lower RTA1 temperatures.

The crystalline structure of the silicide layers was determined by θ-2θ X-ray diffraction (XRD) scans with Cu Kα radiation, as shown in fig. VI.6. These scans clearly demonstrate pure CoSi peaks in the 550°C sample, but the overlapping of CoSi (210, 211, 200) and Co_2Si (220, 021, 301, 121, 002, 311) peaks for the cases of 435°C and 450°C. This overlapping is most vivid after RTA1 at 435°C (leading to asymmetrical peak shape at ~2Å interlayer spacing), gradually disappearing as the temperature was increased to 550°C. Therefore, the explanation of varying surface concentrations in figs. VI.5a-c is the presence of Co_2Si mixed with CoSi, meaning higher Co content. It happens because not enough Si diffuses at lower temperature from the substrate to the surface in order to form a pure CoSi phase. During depth profiling the elemental concentrations in the near-surface region (accessible to AES) were altered by preferential sputtering of the lighter element. When the balance between depletion and preferential sputtering of Si was achieved, the concentrations were equal to 70% for Co and 30% for Si and remained unchanged over the entire depth of the film till the interface with the substrate. The fact that such "steady" concentrations were practically the same for all three presented samples, means that only CoSi phase existed in the bulk of the films, while only a small fraction of Co_2Si was present on the surface of films with RTA1 at 435°C and 450°C.

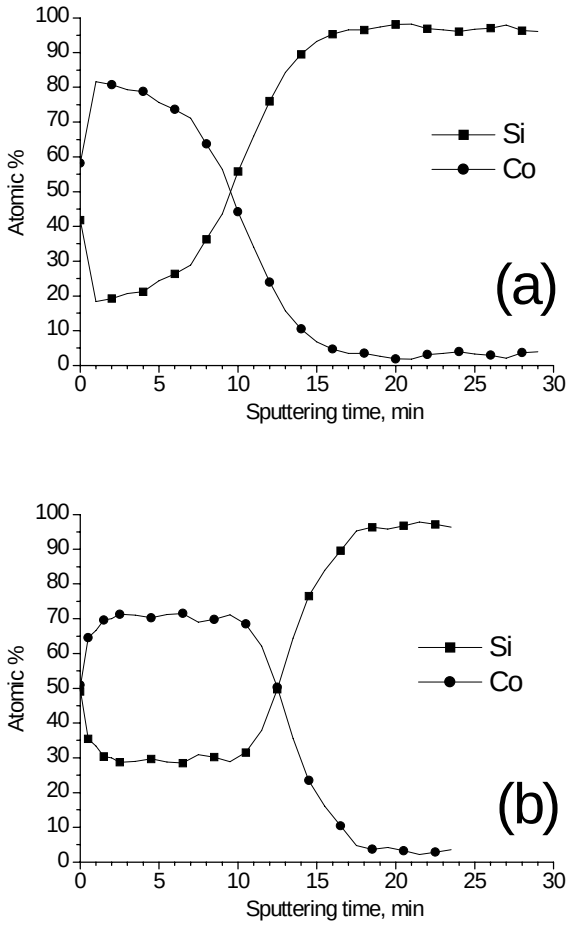

Fig. VI.7. ADPs of the sample with 20 nm initial Co thickness after selective etching, subjected to 30 s of RTA1 at (a) 435℃ and (b) 550℃. Under the same thermal dose of RTA1 at 435℃, the amount of Co_2Si is higher for 20 nm initial Co thickness, than in the case of 10 nm (fig. VI.5.a).

Since the CoSi formation is a diffusion limited process, it was instructive to compare the influence of RTA1 thermal dose on the samples with thicker initial Co films. As an example, figs. VI.7a-b show the ADP of the sample with 20 nm of Co after RTA1 and selective etching. The RTA1 was done for 30 s at 435°C (fig. VI.7a) and at 550°C (fig. VI.7b). The latter sample is attributed to a pure CoSi film, similar to that in fig. VI.5c but with larger thickness. However, the sample after 435°C RTA1 has much higher deviation from the pure CoSi phase than it was for 10 nm of initial Co thickness (figs. VI.5a-b). This is explained by higher Co_2Si content in the thicker film, since less Si has reached its surface

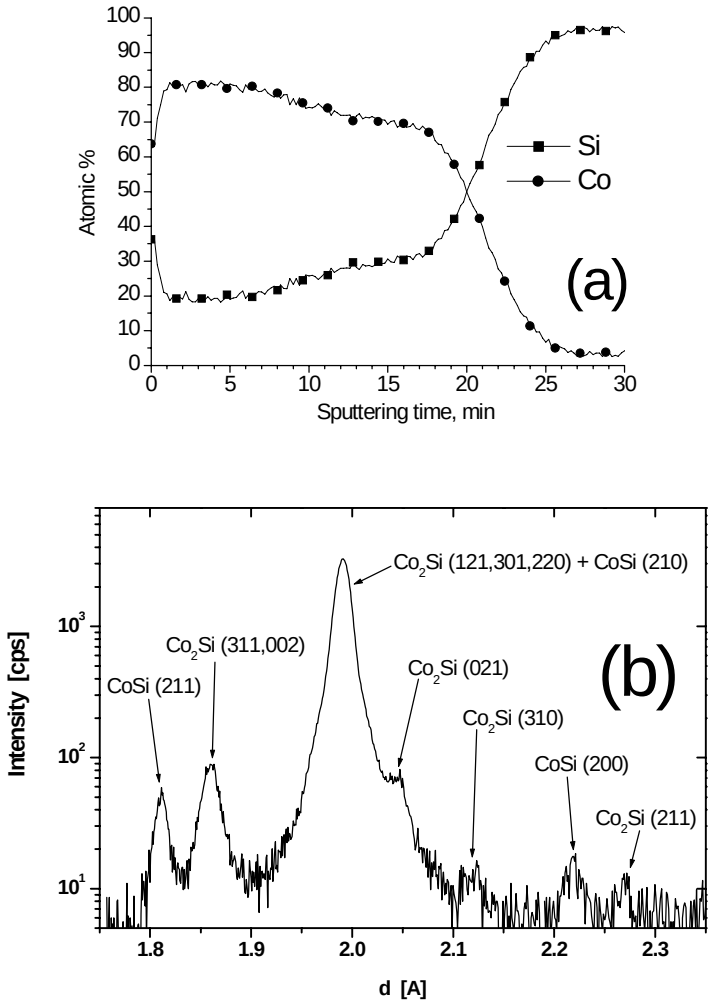

Fig. VI.8. The sample with 35 nm initial Co thickness after 90 s of RTA1 at 465°C and selective etching. (a) ADP; (b) XRD scan by Cu Kα radiation. A pure Co_2Si layer is formed on the film surface and it is thick enough for equilibrium sputtering conditions to be reached.

during the RTA1 with equal thermal dose. It was useful for analysis methodology to obtain the Co_2Si film thick enough for detecting "steady" concentrations during sputtering as it was in the case of CoSi. The ADP of such sample is shown in fig. VI.8a - corresponding to 35 nm initial Co thickness after 90 s of RTA1 at 465°C and selective etching. Here the layer neighbouring the substrate is a familiar CoSi layer with 70%-30% "steady" concentrations. Following is the layer where "steady" concentrations reach the plateau at 80%-20% values. These concentrations are attributed to the steady conditions of Co_2Si

sputtering by 1 keV Ar^+ ions. At the same time, the surface concentrations at the beginning of ADP are very close to the pure Co_2Si stochiometry. The XRD scan in fig. VI.8b confirms this by showing both CoSi and Co_2Si related peaks. Thus, it is clear that a pure Co_2Si layer exists in this sample. From the results presented above it follows that samples with 10 nm initial Co thickness are more suitable for creation of dispersion models of the CoSi phase. The dependencies of the CoSi refractive index (n) and extinction coefficient (k) on the wavelength derived from SE spectra for the case of initial Co thickness of 10 nm, are plotted in fig. VI.9 They were measured in the same manner as in the previous section. The observed difference between the dispersion curves after different RTA1 temperatures, mainly between 435 and 450°C, is a result of the presence of a Co_2Si phase after silicidation at 435°C.

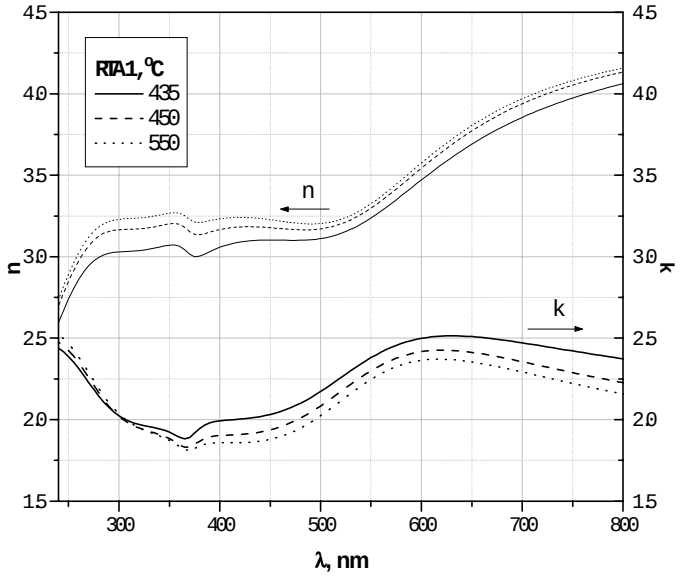

Fig. VI.9. Optical parameters (n and k) vs wavelength of the samples from fig. VI.5. The difference between optical parameters of different samples is due to varying amount of Co_2Si in the surface region.

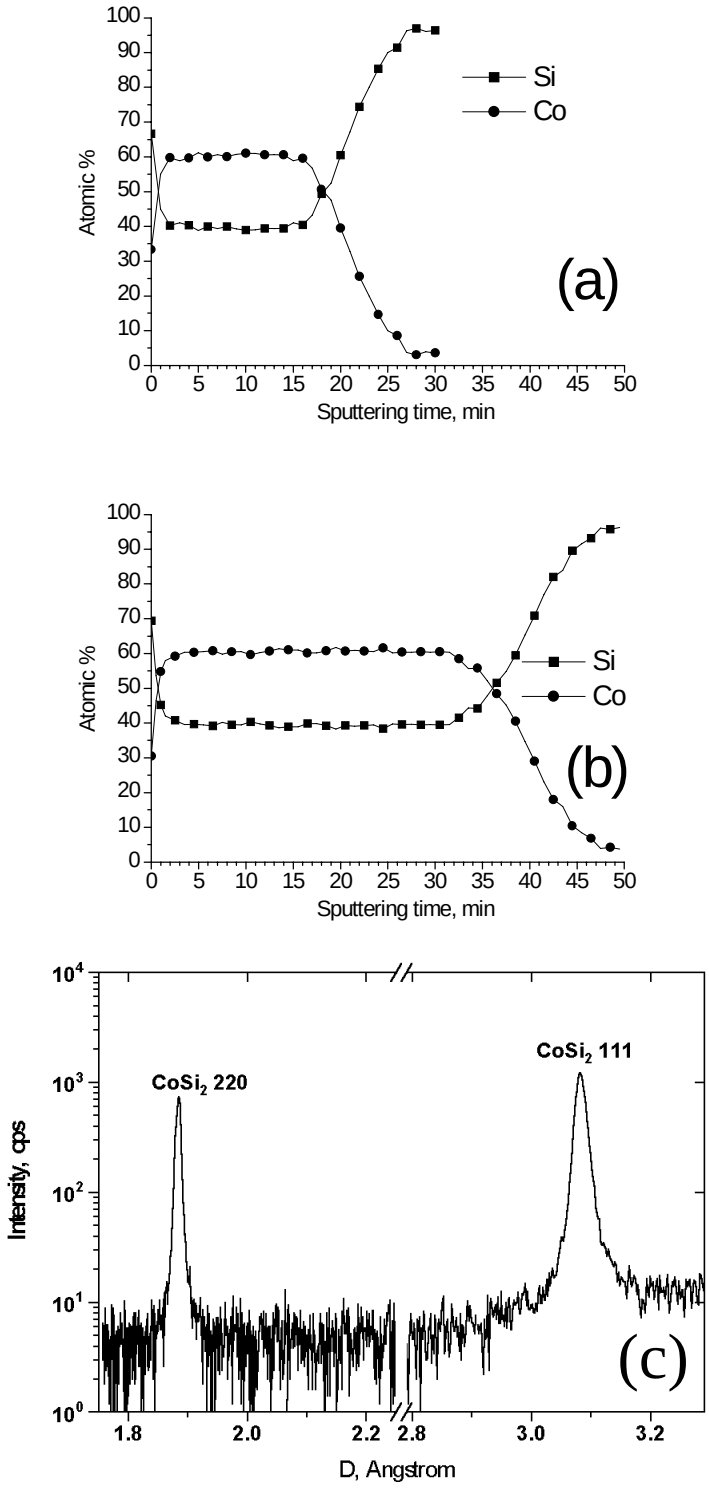

Fig. VI.10. Samples after completion of the last SALICIDE process step. ADPs obtained on samples with initial Co thickness (a) 20 nm, (b) 35 nm. (c) XRD scan of the sample in (b) obtained with Cu Kα radiation. A pure and uniform $CoSi_2$ film is present in both samples.

VI.d. Second silicidation step

The CoSi phase described above was transformed into $CoSi_2$ phase after the RTA2 step. Figs. VI.10a-b show the ADPs of the samples with initial Co thickness of 20 nm and 35 nm respectively. They were subjected to RTA1 at 550°C during 30 s, selective etching and RTA2 at 810°C during 30 s. The XRD analysis confirmed that a pure $CoSi_2$ phase is present in the samples after RTA2. As an example, fig. VI.10c shows the XRD scan of the sample where initial Co thickness was 35 nm. The measured surface concentrations (before sputtering) confirm that the phase is indeed $CoSi_2$. In the steady sputtering conditions the measured concentrations were approximately 60%-40%, as opposed to 70%-30% for CoSi and 80%-20% for Co_2Si. This can be considered as a "fingerprint" of the $CoSi_2$ phase during profiling with 1 keV Ar^+ ions. The refractive index dispersion for $CoSi_2$ phase is shown in fig. VI.11. It was measured in a similar way as in the previous sections using a sample with 35 nm initial Co thickness.

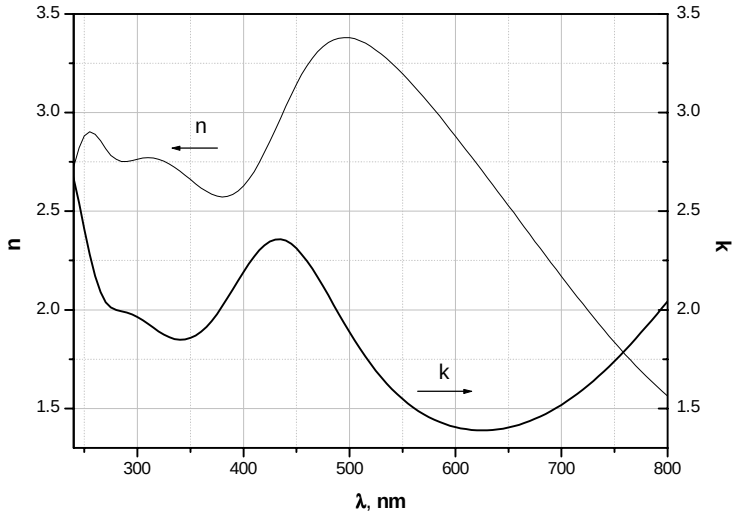

Fig. VI.11. Optical properties (n and k) vs wavelength of the sample from fig. VI.10b. The optical parameters of $CoSi_2$ films (after completion of the SALICIDE process) do not depend on the initial Co layer thickness.

VI.e. Summary of Co SALICIDE process control for industrial wafer processing technology

The obtained refractive index dispersion data for Co, CoSi, and $CoSi_2$ films were used for SE in-line thickness and uniformity determination. Full automatic wafer mapping of 49 points of a 200 mm blanket wafer was performed for each step of the SALICIDE process by SE and four point probe resistance measurement. The average values of film thickness (as measured by SE) D_{SE} and its standard deviations σ_{SE} are presented in the table VI.1, compared with average sheet resistance values Rs and its standard deviations σ_{Rs}.

Table VI.1

Steps of Co SALICIDE process	**D_{SE}, nm**	**σ_D, %**	**Rs, Ohm/sq**	**σ_{Rs}, %**
After Co deposition	10.8	1.5	21.1	1.4
After RTA1 (450 ^oC) and selective etching	18.2	0.8	75.9	0.7
After RTA2 (810 ^oC)	35.1	1.5	5.36	1.4

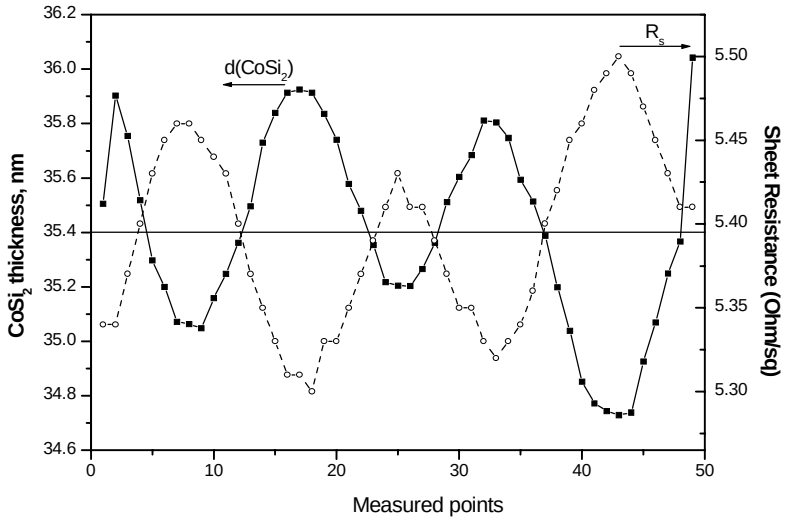

Fig. VI.12. $CoSi_2$ film thickness (measured by SE) and its resistance (measured by four point probe) after the completion of SALICIDE process with initial Co thickness of 10 nm. An excellent out of phase correlation is observed between thickness and resistance.

Finally, fig. VI.12 shows the comparison of SE and sheet resistance values in 49 points along diameter of a 200 mm wafer for 10 nm initial Co thickness after RTA1 (450^{o}C, 30 s) and RTA2 (810^{o}C, 30 s). The average sheet resistance value is 5.395 Ohm/sq and the standard deviation is σ = 1.0%. The average value of the silicide thickness obtained by SE is 35.4 nm and the standard deviation is σ=1.0%. The obtained data show an excellent out of phase correlation of thickness and sheet resistance.

All this proves a high efficiency of the applied SE measurement procedure for in-line thickness uniformity control during SALICIDE process. Also, the data on ion sputtering of Co_2Si, CoSi, and $CoSi_2$ compounds with 1 keV Ar^+ ions allow for unambiguous detection of these $CoSi_x$ phases by altered Co-Si concentrations of 80%-20%, 70%-30%, and 60%-40% respectively. Such information can be readily used in AES investigations of $CoSi_x$ phases without the need for any reference samples.

Chapter VII

Conclusions

VII.a. Outlook

In the following, an attempt will be done to estimate the importance of results described in the previous chapters and their perspectives in the process of further miniaturization in microelectronics. The mainstream of the thesis is investigations of materials, which will enable the miniaturization beyond the 0.1 μm CMOS technology node. In this sense investigation of Pr_2O_3 is a backbone of the entire work, since it deals with a gate dielectric replacement problem, viewed as a major miniaturization challenge in the years to come.

Although new materials are and will be introduced in order to ensure the possibility of further miniaturization, the major material of the modern microelectronics, namely Si(100) substrate, is not likely to be replaced. Therefore, it is reasonable to assume that in the production of mature MOS transistors a Pr_2O_3 gate dielectric will be deposited or grown on the Si(100) surface. The MBE deposition technique used for Pr_2O_3 in this work and also reported by others [18] requires the substrate temperatures somewhere between 600°C and 700°C. It was important to obtain detailed information about surface properties (reconstruction, roughness, defects) in this temperature range. This information is necessary for understanding and simulation of the interfacial region between the high-K dielectric and the substrate, of the film growth, structure and quality, and eventually of the electrical characteristics of Pr_2O_3-based MOS structures. The Si(100)-c(4×4) reconstruction which appears in the given temperature range was found to be an undesirable alternative to the 2×1 structure for Pr_2O_3 epitaxy. This follows from the large number of vacancies observed in this structure and from the presence of two structural modifications: α and β, which are chaotically mixed. These factors make the c(4×4) surface rougher on an atomic scale than the 2×1 surface, while it is desired to make the interface between the gate dielectric and the substrate as smooth as possible. This is especially important for deep sub-μm scaled MOS transistors, where extremely thin dielectric films are used and the

interfacial region has an increasingly large influence on electrical characteristics. Fortunately the presence of Pr_2O_3 on the Si(100) surface does not invoke the c(4×4) reconstruction as many adsorbates do. So, the latter can be safely avoided if extremely long annealing times between 600°C and 700°C are not involved in the deposition procedure. This recommendation stems from the fact that the c(4×4) reconstruction is likely a true equilibrium structure on the Si(100) surface in this temperature range.

The current work makes a substantial contribution into the preparation of Pr_2O_3 for production of real MOS devices. First, it outlines the thermal budget which will be allowed with this high-K dielectric. This thermal budget will have to be taken into account while designing the advanced CMOS production sequence. Of course, the presented results outline the thermal budget only in some certain annealing environments and temperature points. They do not pretend to be exclusively complete and some additional similar measurements may be required to supplement the picture. However, already at this point, two interesting aspects are worth mentioning. They correspond to two possible scenarios of Pr_2O_3 thermal degradation: Pr silicide and Pr silicate formation. As it was shown, the first can be selectively used at desired locations to form contacts to source and drain of the transistor. The second is present at interfaces but can also form in the film under extreme thermal exposures. Since the interfacial layer is effectively a capacitance in series with the main dielectric film, it usually leads to a diminishing of high-K benefits. Fortunately, the Pr silicate is a high-K dielectric itself and viewing its amorphous structure it can be an excellent intermediate layer, which would smooth out the lattice constant mismatch between Pr_2O_3 and Si(100) without compromising the gate capacitance value. Therefore, one can recommend to use the technological thermal budgets, which would limit the Pr silicate presence only to interfacial regions between Pr_2O_3 and Si.

The application of high-K gate dielectrics will lead to extremely miniaturized MOS devices, for which also low resistance contacts to interconnects will be required. The described results demonstrate the best way to control the W/WN_x/poly-Si gate stacks. Using the sputtering ion energy as low as possible (1 keV for the given experimental set-up) and rotating the sample during AES depth profiling reveals the elemental distributions in the most faithful manner. A question arises about the applicability of rotation for profiling of actual gate stacks in sub-0.25 μm device-sized areas. Usually the rotational profiling requires an alignment of rotation axis with the

primary electron beam. However, any rotation mechanism will wobble, resulting in displacement of the targeted sample region from the analysis area. Normally these displacements are relatively small and pose no problem for profiling of blanket deposited films (as was the case in this work). However, if, for example, a gate stack of a sub-0.25 μm MOS transistor is being analyzed, then such wobbling may be detrimental. In order to avoid the shifting of the area of interest away from the primary beam, it is necessary to track and compensate the wobbling by an appropriate computer-controlled mechanical system [150]. This approach can only be realized in the combined AES/SEM set-up. It has a potential for further improvement if the sample is not mechanically repositioned, but the probing electron beam itself follows the wobble movement. In such a case the SEM will operate interchangeably with AES, periodically assessing the run-off and compensating the primary beam position. As a result an advanced characterization of patterned W/WN_x/poly-Si gate stacks will become possible.

The investigations performed on W silicides and Co silicides are important in the aspects given below. First of all, an approach is suggested which is different from what one may occasionally encounter in the literature. In the later case, a composition of silicide is obtained using sensitivity factors adjusted to obtain the "correct" metal/Si ratio (e.g. for WSi_2 [151] or $CoSi_2$ [152]). The adjustment of sensitivity factors must be done of course, using some standard sample of known composition. This scheme yields correct compositions inside the silicide film on the ADP, but does not inform about the real composition on the surfaces or interfaces. Further more, it is actually misleading about the real elemental concentrations inside the currently sputtered layer during depth profiling. The approach practiced in the current work is more "honest" in a sense that it always shows the real elemental concentrations present in the volume accessible to AES. The basis of this approach is an elemental sensitivity method, while the sensitivity factors are always derived from pure Si and pure metals (W and Co in the given case). Like with the opposite one, this approach requires first a profiling of standard silicides of well known stochiometry in order to recognize the unknown samples later. But the great advantage of the present work is measuring the correct composition on the film surface as well as the ability to detect the slightest deviation of this composition from the targeted stochiometry. This gives a wider opportunity to control the film deposition, its silicidation and other technological processes. In particular, WSi_2, $CoSi_2$, CoSi, and Co_2Si phases can be identified on the ADPs obtained with 1 keV Ar^+ ion sputtering.

This ion energy is one of the standard values for many AES spectrometers. So, the obtained results can be readily used in numerous analytical laboratories, without the need to resort to reference samples.

It is clearly demonstrated that AES is an effective tool for solving the problems of current and future microlelectronics technology. The information obtained by this technique is required to design technological processes by which the CMOS devices will be produced in the nearest years. It is noteworthy, that up to now, AES is capable of such analysis not only on blanket (laterally uniform) wafers for materials science aspects, but also on structured wafers containing real devices for process characterization and failure aspects. Due to an excellent lateral resolution of AES, this is possible at a stage when minimum feature sizes are around 100 nm. It seems plausible that even the minimum feature sizes around 50 nm will still be accessible for laterally resolved elemental mapping by AES. Further miniaturization will require other techniques which will have an adequate spatial resolution and have elemental recognition capability at the same time. The STM does not possess such capability directly, but elemental recognition is still possible by extensive theoretical simulation [153]. This is a procedure of guessing the atomic structure of the investigated sample and then checking if this structure is stable. Here guessing means setting out the types of atoms and their initial position in the surface structure. After that the structure is being shaken, or in other words the total energy of this structure is calculated when the atoms are slightly shifted from their initial positions. If the total energy becomes smaller after a certain shift, then shaking continues around this new atomic position. In this way a sequence of approximating shifts is being done until the structure finds a total energy minimum or a set of atomic positions from which any shift would only produce a deficit of energy. The thus-minimized and stable structure may just slightly vary from the guessed one or be completely different. The theoretical simulations described in this thesis are exactly of this type. They were done to clarify some very tiny differences which may exist between the actual atomic structure of the Si(100)-c(4×4) surface reconstruction and one of its widely accepted models. Such guessing process of trial and error is done until the structure is found, which would produce the STM image similar to what is experimentally observed. The obtained experimental images show the Si(100)-c(4×4) structure with the features not previously reported by other researchers. These images were intended to be reproduced by the simulations described above. Usually they require calculations which run for hours on the most powerful modern

desktop computers, just to check the validity of a single structural guess. So, the process of building the atomic model of the surface observed with STM is a tedious work for many days. It requires numerous non-trivial guesses and is thus far from being a routine analysis scheme. Nor do the results of such research seem to be in any way useful for microelectronics technology within the nearest decade. This assertion stems from the fact that the modern MOS transistors, CMOS circuits and many other devices are not at all sensitive to the sub-angstrom differences in the atomic structure of materials which these devices are made of. However, the miniaturization trends in the time domain beyond the first decade of the third millennium will definitely bring nanometer sized devices and eventually even angstrom sized single atom cells, which would store and process information simultaneously. In that situation it would matter very much to characterize these atomic structures in every tiniest detail possible. Definitely the power of the personal computers will increase immensely at this point to allow determination of every particular structure within seconds. The process will be further accelerated by artificial intelligence systems and advanced solid state theories - aiding and automating the guessing process. The STM will become an indispensable tool not only in basic research but also in the everyday design and failure mode analysis of the then nanoelectronics technology.

VII.b. Summary

In the following a summary will be given of the key scientific results obtained by the author of this thesis himself.

It was shown that Bi adsorption and desorption produces a lot of defects in the Si(100) substrate. These defects accelerate the Si(100)-2×1→Si(100)-2×n→Si(100)-c(4×4) phase transition. The STM images of the Si(100)-c(4×4) show that this structure may have a 1m symmetry instead of a 2mm symmetry as believed before.

The window of thermal stability was established for Pr_2O_3/Si(100) and Si/Pr_2O_3/Si(100) structures. The earlier one suffers from Si outdiffusion from the substrate already at 700°C both in vacuum and nitrogen environment, leading to Pr silicate formation. The latter structure is subjected to Pr silicide formation staring from 700°C in vacuum and to Pr silicate formation starting from 900°C in nitrogen.

The influence of sample rotation and different ion energies was demonstrated for AES depth profiling of $W/WN_x/Si$ and WSi_x/Si structures. Lowering of ion energy from 4 to 1 keV increases the depth resolution on ADPs of both structures, but worsens the preferential sputtering of Si in the case of WSi_x/Si. Rotating the sample during profiling does not improve the depth resolution for WSi_x/Si, but only for $W/WN_x/Si$. In the latter case also a higher sensitivity to oxygen (contaminant in this structure) is achieved, due to reduced subsurface sputtering of O atoms.

The preferential sputtering in different $CoSi_x$ phases was quantitatively investigated. The equilibrium surface concentrations during sputtering with 1 keV Ar^+ ions at 55° angle of incidence were found to be 80% Co - 20% Si for Co_2Si, 70% Co - 30% Si for CoSi, and 60% Co - 40% Si for $CoSi_2$.

References

[1] C. Y. Chang, S. M. Sze (Eds), ULSI Technology, 1996 by McGraw Hill.

[2] A. Bar-Lev, Semiconductors and Electronic Devices, 1979 by Prentice-Hall International, Inc.

[3] P. S. Peercy, Nature 406 (2000) 1023.

[4] The International Technology Roadmap for Semiconductors (ITRS) is an assessment of the semiconductor technology requirements. This assessment, called roadmapping, is a co-operative effort of the global industry manufacturers and suppliers, government organisations, consortia, and universities. The latest version of ITRS can be found in the Internet at http://public.itrs.net/Home.htm.

[5] S. P. Murarka, Silicides for VLSI Applications, 1983 by Bell Telephone Laboratories.

[6] J. Hillman et al, Solid State Technology, July (1995) 147.

[7] L. Peters, Semiconductor International, January (2000) 52.

[8] R. H. Denard et al, IEE J. Solid-State Circuits SC-9 (1974) 256.

[9] P. A. Packan, Science 285 (1999) 2079.

[10] S. Deleonibus, Solid State Technology, March (2000) S14.

[11] D. J. Frank, Y. Taur, Solid-State Electronics 46 (2002) 315.

[12] M. L. Green, E. P. Gusev, R. Degraeve, E. L. Garfunkel, J. Appl. Phys. **90** (2001) 2057.

[13] A. Inani, R. V. Rao, B. Cheng, J. Woo, Jpn. J. Appl. Phys. 38 (1999) 2266.

[14] G. D. Wilk, R. M. Wallace, J. M. Anthony, J. Appl. Phys. 89 (2001) 5243.

[15] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature **406** (2000) 1032.

[16] G. Lucovsky, J. Vac. Sci. Technol. A **19** (2001) 1553.

[17] E. P. Gusev et al, Technical Digest IEDM (2001) 451.

[18] S. Jeon, K. Im, H. Yang, H. Lee, H. Sim, S. Choi, T. Jang, H. Hwang, Technical Digest IEDM (2001) 471.

[19] P. Singer, Semiconductor International, January (2000) 38.

[20] H. J. Osten, J. P. Liu, P. Gaworzewski, E. Bugiel, P. Zaumseil, Technical Digest IEDM (2000) 653.

[21] H.-J. Müssig et al, Proceedings of the 2001 IEEE / International Integrated Reliability Workshop, Lake Tahoe, CA, USA.

[22] H. J. Osten, J. P. Liu, H. J. Müssig, Appl. Phys. Lett. 80 (2002) 297.

[23] H. J. Osten, J. P. Liu, H.-J. Müssig, P. Zaumseil, Microelectronics Reliability 41 (2001) 991.

[24] H. J. Osten, J. P. Liu, E. Bugiel, H. J. Müssig, P. Zaumseil, Mater. Sci. Eng. B87 (2001) 297.

[25] H. J. Osten, J. P. Liu, E. Bugiel, H. J. Müssig, P. Zaumseil, J. Cryst. Growth 235 (2002) 229.

[26] R. E. Schlier, H. E. Farnsworth, Semiconductor Surface Physics, 1957 by University of Pennsylvania Press.

[27] K. Müller, E. Lang, L. Hammer, W. Grimm, P. Heilman, K. Heinz, Determination of Surface Structure by LEED, ed. by P. M. Marcus and F. Jona, 1984 by Plenum.

[28] R. J. Hamers, R. M. Tromp, J. E. Demuth, Phys. Rev. B 34 (1986) 5343.

[29] J. Dabrowski, H.-J. Müssig, Silicon Surfaces and Formation of Interfaces, 2000 by World Scientific Publishing Co. Pte. Ltd., and references therein.

[30] K. C. Pandey, in Proceedings of the 17th International Conference on the Physics of Semiconductors; edited by J. D. Chadi and W. A. Harrison, Springer-Verlag, New York 1985, p.55.

[31] Y. F. Zhao, H. Q. Yang, S. J. Pang, Phys. Rev. B 62 (2000) R7715.

[32] P. W. Murray, R. Lindsay, F. M. Leibsle, P. L. Wincott, and G. Thornton, Phys. Rev B 54 (1996) 13468.

[33] A. Goryachko, P. V. Melnik, N. G. Nakhodkin, T. V. Afanasjeva, I. F. Koval, Surf. Sci. 497 (2002) 47.

[34] J. M. Walls, R. Smith (Eds), Surface Science Techniques, 1994 by Elsevier Science Ltd.

[35] K. J. Hubbard, D. G. Schlom, J. Mater. Res. **11** (1996) 2757.

[36] H. Ono, T. Katsumata, Appl. Phys. Lett. **78** (2001) 1832.

[37] C. C. Chang, J. Vac. Sci. Technol. 18 (1981) 276.

[38] A. Goryachko, J. P. Liu, D. Krüger, H. J. Osten, E. Bugiel, R. Kurps, V. Melnik, submitted to J. Vac. Sci. Technol. A.

[39] German patent # DE 101 27 234.

[40] T. Sugii, Y. Momiyama, K. Goto, Solid-State Electronics 46 (2002) 329.

[41] M. T. Takagi et al, Technical Digest IEDM (1996) 455.

[42] B. H. Lee, D. K. Sohn, J.-S. Park, C. H. Han, Y.-J. Huh, J. S. Byun, J. J. Kim, Technical Digest IEDM (1998) 385.

[43] J. E. Kelsey, C. Goldberg, G. Nuesca, G. Peterson, A. E. Kaloyeros, B. Arkles, J. Vac. Sci. Technol. B 17 (1999) 1101.

[44] C. Ryu, H. Lee, K. W. Kwon, A. L. S. Loke, and S. S. Wong, Solid State Technology, April (1999) 53.

[45] B. H. Lee, K. S. Lee, D. K. Sohn, J. S. Byun, C. H. Han, J.-S. Park, S. B. Han, and J. W. Park, Appl. Phys. Lett. 76 (2000) 2538.

[46] S. Ganguli, L. Chen, T. Levine, B. Zheng, and M. Chang, J. Vac. Sci. Technol. B 18 (2000) 237.

[47] J.-W. Jung, S.-W. Lee, Y.-G. Sung, B.-H. Lee, J.-H. Choi, B.-J. Lee, R.-H. Park, S.-B. Hang, Technical Digest IEDM (2000) 365.

[48] W.-t. Kang et al, Technical Digest IEDM (2001) 59.

[49] I. H. Cho, J.-S. Park, D. K. Sohn, J. H. Ha, Jpn. J. Appl. Phys. 40 (2001) 4854.

[50] H.-T. Chiu, S.-H. Chuang, J. Mater. Res. 8 (1993) 1353.

[51] J. W. Klaus, S. J. Ferro, S. M. George, J. Electrochem. Soc. 147 (2000) 1175.

[52] A. Goryachko, D. Krüger, R. Kurps, G. Weidner, and K. Pomplun, J. Vac. Sci. Technol. A **19** (2001) 2174.

[53] K. Maex, Materials Science & Engineering R: Reports, R11 (1993) 53.

[54] J. A. Kittl, Q. Z. Hong, Thin Solid Films 320 (1998) 110.

[55] J. A. Kittl, W.-T. Shiau, D. Miles, K. E. Violete, J. C. Hu, Q.-Z. Hong, Solid State Technology, June (1999) 81.

[56] A. Goryachko, V. Melnik, D. Krüger, D. Bolze, P. Zaumseil, R. Kurps, Proceedings of the 14th International Symposium 'Thin Films in Optics and Electronics'; Kharkov, Ukraine, April 22-27th, 2002.

[57] D. E. Aspnes, J. Vac. Sci. Technol. 18 (1981) 289.

[58] H. Lüth, Surfaces and Interfaces of Solids, 2nd edition, 1993 by Springer -Verlag.

[59] M. Grasserbauer, H. W. Werner (Eds), Analysis of Microelectronic Materials and Devices, 1991 by John Wiley & Sons Ltd.

[60] R. Weissmann, K. Müller, Auger Electron Spectroscopy - a Local Probe for Solid Surfaces, Surf. Sci. Rep. 105 (1981) 251.

[61] E. Fuchs, H. Opolzer, H. Rehme, Practical Beam Microanalysis, 1990 by VCH.

[62] L. E. Davis, N. C. MacDonald, P. W. Palmberg, G. E. Riach, R. E. Weber, Handbook of Auger Electron Spectroscopy, 2nd edition, 1976 by Physical Electronics Industries, Inc.

[63] L. C. Feldman, J. W. Mayer, Fundamentals of Surface and Thin Films Analysis, 1986 by Elsevier Science Publishing Co, Inc.

[64] M. Grasserbauer, H. J. Dudek, and M. F. Ebel, Angewandte Oberflächenanalyse mit SIMS, AES und XPS, 1986 by Springer-Verlag Berlin Heidelberg.

[65] D. Briggs, M. P. Seach (Eds), Practical Surface Analysis by Auger and X-Ray Photoelectron Spectroscopy, 1983 by John Wiley & Sons.

[66] 670 Installation, Calibration and Maintenance Manual, Version4.0, Perkin Elmer, Physical Electronics Division, Part No. 622088 Rev. B.

[67] G. Binnig, H. Rohrer, Ch. Gerber, E. Weibel, Phys. Rev. Lett. 49 (1982) 57.

[68] G. Binnig and H. Rohrer, Rev. Mod. Phys. 59 (1987) 615.

[69] D. A. Bonnell (ed.), Scanning Tunneling Microscopy and Spectroscopy: Theory, Techniques, and Applications, 1993 by VCH Publishers, Inc.

[70] C. Hamman and M. Hietschold, Raster-Tunnel-Mikroskopie, 1991 by Akademie Verlag GmbH, Berlin.

[71] I. V. Lyubinetsky, P. V. Melnik, N. G. Nakhodkin, A. E. Anisimov, Vacuum 46 (1995) 219.

[72] A. M. Goryachko, P. V. Melnik, M. G. Nakhodkin, Proceedings of the Third International Symposium on Vacuum Technology and Equipment; Kharkov, Ukraine, September 22-24th, 1999, volume 2, p. 242.

[73] A. M. Goryachko, P. V. Melnik, M. G. Nakhodkin, Visnyk Kyivskogo Universytetu, Physical-Mathematical Sciences Series, N$_{\underline{O}}$ 4, 1998, pp. 257-264.

[74] A. Goryachko, P. Melnik, M. Nakhodkin, T. Afanasjeva, I. Koval, S. Kulik, Visnyk Kyivskogo Universytetu, Physical-Mathematical Sciences Series, N$_{\underline{O}}$ 3, 2000, pp. 329-338.

[75] A. M. Goryachko, P. V. Melnik, M. G. Nakhodkin, Visnyk Radiophysica ta Electronica, N$_0$ 1, 2000, pp. 23-29.

[76] H. Wang, R. Lin, X. Wang, Phys. Rev. B 36 (1987) 7712.

[77] D.-S. Lin, P.-H. Wu, Surf. Sci. 397 (1998) L273.

[78] H. Nörenberg, G. A. D. Briggs, Surf. Sci. 430 (1999) 154.

[79] H. Nörenberg, G. A. D. Briggs, Surf. Sci. 433-435 (1999) 397.

[80] K. Miki, K. Sakamoto, T. Sakamoto, Appl. Phys. Lett. 71 (1997) 3266.

[81] T. Ide, T. Mizutani, Phys. Rev. B 45 (1992) 1447.

[82] R. I. G. Uhrberg, J. E. Northrup, D. K. Biegelsen, R. D. Bringans, L.-E. Swartz, Phys. Rev. B 46 (1992) 10251.

[83] K. Kato, T. Ide, T. Nishimori, T. Ichinokawa, Surf. Sci. 207 (1988) 177.

[84] F. K. Men, J. E. Erskine, Phys. Rev. B 50 (1994) 11200.

[85] Z. Zhang, M. A. Kulakov, B. Bullemer, Surf. Sci. 369 (1996) 69.

[86] K. Miki, J. H. G. Owen, D. R. Bowler, G. A. D. Briggs, K. Sakamoto, Surf. Sci. 421 (1999) 397.

[87] J. Wasserfall, W. Ranke, Surf. Sci. 331-333 (1995) 1099.

[88] R. Butz, H. Lüth, Surf. Sci. 411 (1998) 61.

[89] M. L. Shek, Surf. Sci. 414 (1998) 353.

[90] O. Leifeld, D. Grützmacher, B. Müller, K. Kern, E. Kaxiras, P. C. Kelires, Phys. Rev. Lett. 82 (1999) 972.

[91] O. Leifeld, A. Beyer, E. Müller, K. Kern, D. Grützmacher, Mater. Sci. Eng. B74 (2000) 222.

[92] D. Chen, M.J. Gallagher, D. Sarid, J. Vac. Sci. Technol. B 12 (1994) 1947.

[93] D.-S. Lin, Surf. Sci. 402-404 (1998) 831.

[94] R. Kosugi, S. Sumitani, T. Abukawa, Y. Takakuwa, S. Suzuki, S. Sato, S. Kono, Surf. Sci. 412/413 (1998) 125.

[95] T. Takaoka, T. Takagaki, Y. Igari, I. Kusunoki, Surf. Sci. 347 (1996) 105.

[96] M. Ikeda, T. Maruoka, N. Nagashima, Surf. Sci. 416 (1988) 240.

[97] M. Stoffel, L. Simon, D. Aubel, J. L. Bischoff, L. Kubler, Surf. Sci. 454/456 (2000) 201.

[98] L. Simon et al, Phys. Rev. B 64 (2001) 035306.

[99] Y. Wang, R. J. Hamers, E. Kaxiras, Phys. Rev. Lett. 74 (1995) 403.

[100] Y. Wang, R. J. Hamers, J. Vac. Sci. Technol. A 13 (1995) 1431.

[101] P. Moriarty, L. Koenders, G. Hughes, Phys. Rev. B 47 (1993) 15950.

[102] T. Hatayama, N. Tanaka, T. Fuyuki, H. Matsunami, Appl. Phys. Lett. 70 (1997) 1411.

[103] Ph. Sonnet, L. Stauffer, A. Selloni, A. De Vita, R. Car, L. Simon, M. Stoffel, L. Kubler, Phys. Rev. B 62 (2000) 6881.

[104] I. N. Remediakis, E. Kaxiras, P. C. Kelires, Phys. Rev. Lett. 86 (2001) 4556.

[105] A. A. Saranin et al, Jpn. J. Appl. Phys. 40 (2001) 6069.

[106] A. Sakai, Y. Torige, M. Okada, H. Ikeda, Y. Yasuda, S. Zaima, Appl. Phys. Lett. 79 (2001) 3242.

[107] A. M. Goryachko, P. V. Melnik, M. G. Nakhodkin, Visnyk Kyivskogo Universytetu, Physical-Mathematical Sciences Series, N$_{\underline{o}}$ 1, 1999, pp. 277-284.

[108] S. Tang, A. J. Freeman, Phys. Rev. B 50 (1994) 1701.

[109] H. P. Noh, C. Park, D. Jeon, K. Cho, T. Hashizume, Y. Kuk, T. Sakurai, J. Vac. Sci. Technol. B 12 (1994) 2097.

[110] Y. Qian, M. J. Bedzyk, P. F. Lyman, T.-L. Lee, S. Tang, A. J. Freeman, Phys. Rev. B 54 (1996) 4424.

[111] Franklin G. E., Tang S., Woicik J. C., Bedzyk M. J., Freeman A. J., Golovchenko J. A. Phys. Rev. B 52 (1995) R5515.

[112] Park C., Bakhtizin R. Z., Hashizume T., Sakurai T. J. Vac. Sci. Technol. B 12 (1994) 2049.

[113] Garni B., Kravchenko I. I., Salling C. T. Surf. Sci. 423 (1999) 43.

[114] Zhang Z., Kulakov M. A., Bullemer B. Surf. Sci. 369 (1996) L131.

[115] J. J. P. Stewart, J. Comp. Chem. 10 (1989) 221.

[116] J. J. P. Stewart, Journal of Computer-Aided Molecular Design, 4 (1990) 1.

[117] R. Messmer, G. D. Watkins, Phys. Rev. B 7 (1973) 2568.

[118] F.Trumbore, Bell Syst. Tech. J. 39 (1960) 205.

[119] A. Narayan, O. W. Holland, B. R. Appleton, J. Vac. Sci. Technol. B 1 (1983) 871.

[120] A. B. Bondarchuck, S. N. Goysa, I. P. Koval, P. V. Mel'nik, N. G. Nakhodkin, Surf. Sci. 336 (1995) L767.

[121] H. Ogasawara, A. Kotani, R. Potze, G. A. Sawatzky, and B. T. Thole, Phys. Rev. B 44, 5465 (1991).

[122] J. F. Moulder, W. F. Stickle, P. E. Sobol, and K. D. Bomben, ed. by J. Chastain, Handbook of X-ray Photoelectron Spectroscopy, published by Perkin-Elmer Corporation Physical Electronics Division (1992).

[123] J. Seiple, J. P. Pelz, Phys. Rev. Lett. **73** (1994) 999.

[124] S. Hofmann, Thin Solid Films 398-399 (2001) 336.

[125] S. Berg and I. V. Katardjiev, J. Vac. Sci. Technol. A 17 (1999) 1916.

[126] J. B. Malherbe and R. Q. Odendaal, Appl. Surf. Sci. 144-145 (1999) 192.

[127] S. Hofmann and J. Schubert, J. Vac. Sci. Technol. A 16 (1998) 1096.

[128] A. Zalar, Thin Solid Films 124 (1985) 223.

[129] K. Kajiwara, DE18, 1993 European Conference on Applications of Surface and Interface Analysis, October 4-8th, Catania, Italy.

[130] J. S. Byun, J.-S. Park, B. H. Lee, D.-K. Sohn, J. W. Park, J. J. Kim, J. M. Hwang, IEDM Tech. Dig. (1997) 119.

[131] C. A. Bradbury and D. K. Fillmore, J. Vac. Sci. Technol. A 16 (1998) 1103.

[132] S. F. Hung and L. J. Chen, J. Appl. Phys. 86 (1999) 4018.

[133] B. Tavel, T. Skotnicki, G. Pares, N. Carriere, M. Rivoire, F. Leverd, C. Julien, J. Torres, R. Pantel, IEDM Tech. Dig. (2001) 825.

[134] J. C. Greenwood, B. Lamb, M. Putton, Surf. Interf. Anal. 20 (1993) 524.

[135] V. I. Zaporozchenko, M. G. Stepanova, S. S. Vojtusik, Surf. Interf. Anal. 23 (1995) 185.

[136] F. Nava, et al. Mat. Sci. Rep. 9 (1993) 141.

[137] S.-J. Mu, J. T. Lue, I.-C. Wu, J. Phys. Chem. Solids 49 (1988) 1389.

[138] C. Viguier, A. Cros, A. Humbert, C. Ferrieu, O. Thomas, R. Madar, J. P. Senateur, Solid State Communications, 60 (1986) 923.

[139] M. Simard-Normandin, A. Naem, M. Saran. Mat. Res. Soc. Symp. Proc. 337 (1994) 461.

[140] Z.-C. Wu, E. T. Arakawa, J. R. Jimenez, L. J. Schowalter, Phys. Rev. B 47 (1993) 4356.

[141] Y. Hu, S. P. Tay, J. Vac. Sci. Technol. B 17 (1999) 2284.

[142] N. L. Dmitruk, et al. Solid State Phenomena, 63-64 (1998) 347.

[143] S.-H. Ko, S. P. Murarka, A. R. Sitaram, J. Appl. Phys. 71 (1992) 5892.

[144] A. A. Konova, D. A. Tonova, J. Phys. Condens. Matter 7 (1995) 6459.

[145] J. Card, A. L. Testoni, L. A. Le Tarte, Surf. Interf. Anal. 23 (1995) 495.

[146] J. C. Lascovich, Surf. Interf. Anal. 23 (1995) 636.

[147] V. Melnik, V. Popov, D. Krüger, O. Oberemok, Semiconductor Physics, Quantum Electronics & Optoelectronics 2(3) (1999) 81.

[148] C. Reale, Infrared Physics 10 (1970) 175.

[149] J. J. Xu, J. F. Tang, Applied Optics 28 (1989) 2925.

[150] P.D. Engle and J.D. Geller, J. Vac. Sci. Technol. A 12 (1994) 2373.

[151] Y. C. Jang, D. O. Shin, K. S. Kim, K.-H. Shim, N.-E. Lee, S. P. Youn, K. J. Roh, Y. H. Roh, J. Vac. Sci. Technol. A 19 (2001) 1046.

[152] G. B. Kim, J. S. Kwak, H. K. Baik, S.-M. Lee, J. Vac. Sci. Technol. B 17 (1999) 162.

[153] R. Wiesendanger, M. Bode, R. Pascal, W. Allers, and U. D. Schwarz, J. Vac. Sci. Technol. A 14 (1996) 1161.

Acknowledgments

The creation of the given thesis has become possible due to kind help, support, and contributions of the following people.

First of all I would like to thank my thesis advisors Prof. Dr. D. Schmeißer and Dr. H.-J. Müssig for the guidance received from them.

Special thanks go to project leader Dr. D. Krüger and members of his lab R. Kurps and U. Ewald for introducing me to the interface analysis lab, their enormous technical help, useful discussions, joint scientific undertakings, and a tremendous assistance with integration into life in Germany.

It is particularly important to distinguish those people who actually brought me into a fascinating field of surface science. For this I am indebted to my teachers Prof. Dr. M. G. Nakhodkin, Prof. Dr. P. V. Melnik, Prof. Dr. I. P. Koval, and Dr. I. V. Lyubinetsky.

I highly appreciate many helpful contributions and cooperation with my colleagues. It's a pleasure to express my gratitude to Prof. Dr. H.-J. Osten, Dr. J. P. Liu, and H.-J. Thieme for providing various Pr_2O_3 samples, to Dr. E. Bugiel for transmission electron microscopy investigation of Pr_2O_3 layers, to Dr. V. Melnik for secondary ion mass spectroscopy investigation of Pr_2O_3 layers, to Dr. P. Zaumseil for X-ray diffraction investigation of $CoSi_x$ layers, to Dr. O. Fursenko for spectroscopic ellipsometry investigation of $CoSi_x$ layers, to T. Afanasjeva for theoretical simulation of Si(100) surface structures, to Dr. A. Bardamid and Dr. M. Fedorchenko for very useful discussions, to O. Gulyj and M. Zosim for valuable assistance with STM electronics and software.

Last, but not least, I am very grateful to my caring and loving family - my mother and grandparents, whose support had actually made my work possible. I devote this thesis to my father, who despite his early and tragic death, had inspired my passion for science and engineering.

Abstract

The thesis discusses a fundamental question of reconstruction on the Si(100) surface as well as three material combinations, which are important for perspective microelectronics technologies: $Si/Pr_2O_3/Si(100)$, $W/WN_x/poly\text{-}Si/SiO_2/Si(100)$, and $CoSi_x/Si(100)$. A refined mixed ad-dimer model is developed for the Si(100)-c(4×4) reconstruction on the basis of scanning tunnelling microscopy investigations. A thermal stability of $Pr_2O_3/Si(100)$ and $Si/Pr_2O_3/Si(100)$ structures is studied with ion sputtering assisted Auger electron spectroscopy. The latter technique is also applied for precise determination of O and N content in the new $W/WN_x/poly\text{-}Si/SiO_2/Si(100)$ structure, and to study the preferential sputtering of Si in $CoSi_2$, CoSi, and Co_2Si phases on Si(100) surface. The $WSi_x/poly\text{-}Si/SiO_2/Si(100)$ system, which was previously used in microelectronics, is studied for comparison. The preferential sputtering of Si in WSi_x is shown to be qualitatively similar as in the $CoSi_x$ case.

Zusammenfassung

Die Arbeit beschäftigt sich mit einer grundlegenden Frage der Rekonstruktion auf der Si(100) Oberfläche sowie mit drei Materialkombinationen deren Bedeutung für perspektivische Mikroelektronik-Technologien sind: $Si/Pr_2O_3/Si(100)$, $W/WN_x/poly\text{-}Si/SiO_2/Si(100)$, und $CoSi_x/Si(100)$. Ein verbessertes gemischtes "ad-dimer" Modell war für die Si(100)-c(4×4) Rekonstruktion auf dem Grund der neuesten Raster Tunnel Mikroskopie Untersuchungen entworfen worden. Die thermische Stabilität der $Pr_2O_3/Si(100)$ und $Si/Pr_2O_3/Si(100)$ Systeme war mit der Hilfe von Auger Elektronen Spektroskopie und Ionen Bestrahlung untersucht worden. Diese Methode ist auch für die genaue Messung von O und N Inhalt in $W/WN_x/poly\text{-}Si/SiO_2/Si(100)$ Strukturen verwendet, sowie um das selektive Sputtern von Si in $CoSi_2/Si(100)$, $CoSi/Si(100)$, $Co_2Si/Si(100)$, und $WSi_x/poly\text{-}Si/SiO_2/Si(100)$ Systemen festzustellen. Es wurde gezeigt, daß das selektive Sputtern von Si in den obengenannten Systemen qualitativ ähnlich läuft.