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Influence of Gate Material and Process on Junctionless FET Subthreshold Performance

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ABSTRACT

The recent progress of dimension scaling of electronic device into nano scale has motivated the invention of alternative materials and structures. One new device that shows great potential to prolong the scaling is junctionless FET (JLFET). In contrast to conventional MOSFETs, JLFET does not require steep junction for source and drain. The device processing directly influence the performance, therefore it is crucial to understand the role of gate processing in JLFET. This paper investigates the influence of gate material and process on subthreshold performance of junctionless FET, by comparing four sets of gate properties and process techniques. The result shows that in terms of subthreshold slope, JLFET approaches near ideal value of 60 mV/decade, which is superior than the SOI FET for similar doping rate. On the other hand, the threshold value shows different tendencies between those types of device.

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1. INTRODUCTION

Ultra-sharp junctions in source and drain are extremely important in metal oxide semiconductor field effect transistor (MOSFET) especially at nanoscale dimension as it directly affect the overall performance. For example, the spread of dopant in a 90-nm technology may affect the spread of threshold voltage (V_T) up to 30 mV [1]. This deviation in turn triggers changes in current that in such circumstance may lead to catastrophic problem in the chip. Unfortunately, with the continuous scaling in the device dimension, the concentration distribution requirement of sharp junction is hard to handle further, especially when the scaling reach nanometer regime. One exciting approach to overcome this sharp junction scaling problem is by using junctionless field effect transistor (JLFET). In contrast to the conventional MOSFET, the junctionless transistor uses a structure without semiconductor junctions either in the channel-source or channel-drain regions [2]. Therefore, a homogeneous type of doping and concentration are applied throughout these regions, thus eliminating the needs of ultra-sharp source and drain junctions.

The junctionless FET offers many advantages. Firstly, its fabrication process would be easier than the conventional MOSFETs as the intricate doping process for source and drain is avoided. Secondly, the electric field in the ON-state of the device is low [3]. Thirdly, the mobility in JLFET is improved and insensitive to the interface of gate oxide to channel due to its bulk conduction, unlike surface conduction in the inversion mode device, e.g. MOSFET [4]. It also offers more robust design as it is simple to produce in thin silicon layer. Other advantage is on the possibility to reach faster switching that can be manifested in the lower subthreshold slope. For MOSFET, the ideal value is 60 mV/decade. However, in reality, many devices

cannot meet this value due to several reasons, one of which is the influence of interface trap. As the JLFET does not rely on surface/interface mechanism, it is expected that its slope could be closer to the ideal value.

A number of JLFET structures have been proposed with variations in topologies, such as single gate bulk planar JLFET[3], single gate silicon-on-insulator (SOI) JLFET [4], multi-gate nanowire junctionless transistors [5], gate-all-around nanowire junctionless transistors[6], as well as junctionless tunnel FET[7]. However, little attention is given on the gate materials in JLFET as well as the processing sequence on the gate. It is broadly accepted that the device processing influences the performance, therefore it is crucial to understand the role of gate processing in JLFET.

Our previous paper reported the subthreshold performance of junctionless transistor in comparison with SOI MOSFET FET. The performances were extracted for gate lengths of 50-200 nm to observe the short channel effects, for single thickness of oxide, t_{ox}, and with fixed channel doping N_A[8]. In this paper, we elaborate the variation of materials for gate, which is crucial in determining the threshold voltage. Furthermore, different thicknesses of oxide were also chosen in order to understand broader aspect of the device performance.

2. RESEARCH METHOD

Junctionless FET does not require any junction in the channel between source and drain. Therefore, junctionless transistor operates in accumulation mode. Figure 1 (a) illustrates an n-channel junctionless transistor which has an N+–N+–N+ doped structure for the source, channel and drain region, while Figure 1 (b) shows the conventional MOSFET which works in inversion mode. For good electrical operation, the junctionless transistor should meet specific conditions: first, very thin semiconducting layer is essential for drain, channel, and source regions to achieve full depletion in OFF-state. Later, high doping concentration (~10^{19}-10^{20} cm^{-3}) is required in the semiconducting layer to achieve sufficiently high ON-current [9, 10].

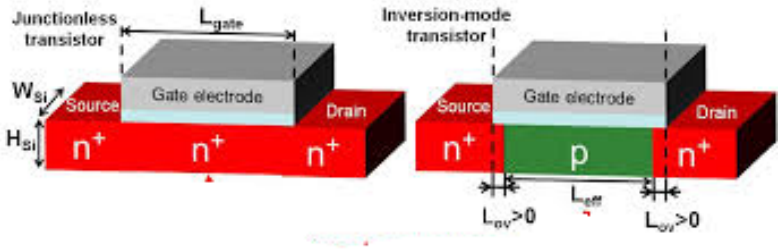

Figure 1. Cross section of FET-based devices: (a) JLFET, (b) inversion-mode FET [10]

Junctionless FET requires dielectric isolation under the semiconductor layer, similar with the SOI MOSFET. As the semiconducting layer lies on top of dielectric insulation, the channel is electrically insulated to the substrate. The thickness and doping concentration of the silicon layer determine whether the channel is in fully depleted (FD) or partially depleted (PD) operation mode. If the semiconductor layer thickness is less than the maximum depletion, x_{dmax}, it is in the FD mode, while thicker layer ensures it in PD mode. However, there are stark constrasts between SOI FET and JLFET. In addition to high source/drain doping requirement (of different type with channel), SOI FET usually employs low or even undoped channel, while JLFET requires high doping for all source-channel-drain regions. The thickness of semiconductor layer to achieve full depletion (both for FD SOI FET and JLFET) should be less than thickness of maximum depletion x_{dmax}, calculated from the following formula:

$$x_{dmax} = \sqrt{\frac{4\epsilon_{Si}\phi_F}{qN_A}} \quad (1)$$

where ϵ_{Si} is the permittivity of silicon, q is the electron charge, N_A is the impurity concentration of the semiconductor layer, and ϕ_F is the Fermi level. According to Eq. (1), the requirement of high doping in JLFET implies the silicon layer should be very thin.

The off state of JLFET is due to the mechanism of full depletion of the channel. This is in contrast with the conventional MOSFET that is based on the reverse bias of the junction. The depletion mechanism is due to the difference between the gate and the channel workfunctions. The use of different gate material can

result in different way of how the JLT works. In the case of P+ polysilicon gate electrode, the device is turned on when the gate electrode is connected to positive voltage equal or larger than the flatband voltage, and conversely for the gate electrode is of N+ polysilicon [9].

The processing sequence of JLFET was simulated by using TCAD tools (Athena) followed by electrical characterization of its subthreshold performance by using Atlas. The thin silicon epitaxial layer was grown on top of silicon oxide which serves as dielectric insulator, followed by growing gate oxide layer with dry oxidation process to create the field effect transistor mechanism. The selected transport model was drift-diffusion based on Boltzmann carrier statistics, along with the Shockley-Read-Hall Recombination with fixed carrier lifetimes models. In addition, the combination of Gummel and Newton numerical methods were used.

The gate material of JLFET is believed to be one important aspect in determining the subthreshold performances. Therefore, this research conducted the simulation on the gate material variation to find out the impact of material changing. Two different gate materials were simulated: polysilicon and aluminum. The work-function for both materials are different, thus the flat-band voltage is supposed to change depending on how much the difference is. In addition, the way the polycilicon is created may come as a source of variation in the performance. The difference between in-situ doped polysilicon and source-drain self-aligned implanted doping of polysilicon is thought as crucial in the nano regime. As a comparison, SOI FET was also simulated. Therefore, we set up four sets of gate materials to be compared. Table 4.3 shows the comparison of parameters used for each device.

Table 1. Variation of parameters in simulation of SOI and JL-FET

	SOI-*based*	JLT-*poly gate*	JLT-*in situ gate*	JLT-*metal gate*
Lg (nm)	50/100/200	50/100/200	50/100/200	50/100/200
t_{ox} (nm)	3/5/7	3/5/7	3/5/7	3/5/7
$_{tsi}$ (nm)	3,2/12,8/22,9/	3/5/10	3/5/10	3/5/10
N_A (cm^{-3})	$1,58x10^{14}$/ $1,58x10^{15}$/ $1,58x10^{16}$/	$1,99x10^{17}$/ $1,99x10^{18}$/ $1,99x10^{19}$	$1,99x10^{17}$/ $1,99x10^{18}$/ $1,99x10^{19}$	$1,99x10^{17}$/ $1,99x10^{18}$/ $1,99x10^{19}$

3. RESULTS AND ANALYSIS

The result of subthreshold simulation is shown in Figure 2 for JLFET and SOI FET with four different material processes for gate, evaluated for effective channel length L=50-200 nm and the effective channel doping $N_A = 3.98.10^{16}$ cm^{-3}. The result shows the comparison of Ig-Vds curves of all structures with the drain voltage V_D =1 V. The threshold voltage roll-off was found for all types of device, but with different tendencies, as depicted in Figure 2. The SOI FET produces lower threshold voltage. Moreover, in the reduction of channel length, its value for V_T decreases with larger step than its JLFET counterparts. On the other side, all variants of JLFET yield in higher V_T values that increase in the shorter channel length. The value of V_T is heavily related to the channel doping as well as the work function of the gate. In this case, the polysilicon gate of SOI-based and polysilicon-based JLFET structures are doped with 10^{18} cm^{-3} of As, while aluminum is subjected for metal-based JLFET.

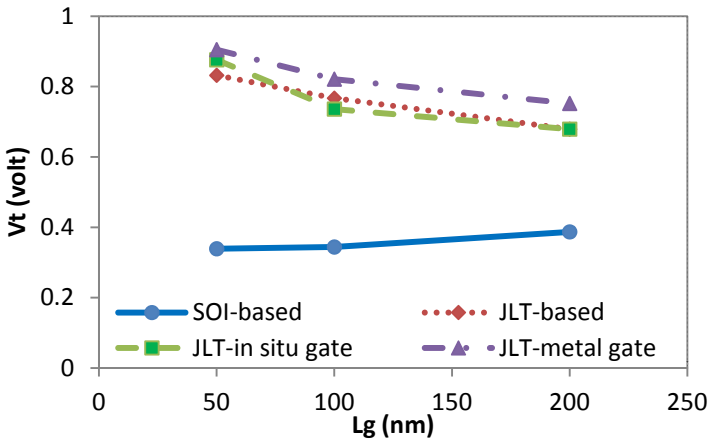

Figure 2. Comparison of threshold voltage for JLFET variants and SOI FET with t_{ox} = 3 nm

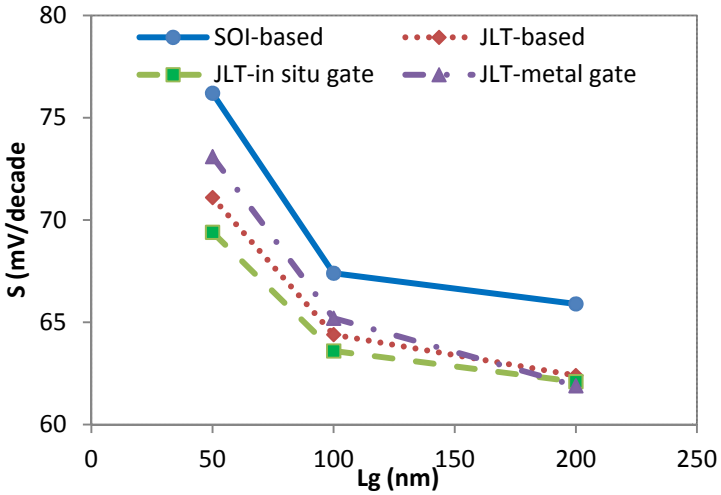

Figure 3. Comparison of subthreshold slope for JLFET variants and SOI FET at several gate lengths

When the channel length is getting smaller, the subthreshold slope value for all structures increase as revealed in Figure 3. However, the slope values for JLFET variants are generally lower than that of SOI based device, with the slope value approaching near ideal value of 60 mV/decade. In addition, the variation for both subthreshold slope and threshold voltage for JLT variants are similar or smaller than the SOI FET for similar doping rate and oxide thickness. This finding shows the real advantage of JLFET that it can turn the device on or off faster when used for switching. The faster slope is due to the bulk transport mechanism used in JLFET that the current flows in all part of the conducting channel, in contrast to the surface conduction endured in conventional MOSFET as well as SOI FET.

The influence of different oxide thickness was also investigated. The simulation shown in Figure 4 indicates that the JLFET with polysilicon gate change its threshold voltage faster than its metal gate counterpart in broad range of channel length when the oxide thickness is reduced. On the other hand, the SOI base device shows rather small variation in threshold voltage in the reduced oxide thickness. Smaller tox produces lower threshold voltage for both metal and polysilicon gates. In addition, both materials suffer from voltage roll-off in short channel. This finding underlines the importance of taking smaller oxide thickness in the reduction of channel length, as has been proposed several decades ago by Dennard for conventional MOSFET, to maintain the near constant field along the channel. In simultaneous combination of L and tox reductions for JLFET, the change of V_T can be maintained small, as the increase of V_T due to L scaling is compensated by the decrease of V_T due to t_{ox} reduction. However, for the similar scenario in SOI-based FET, the V_T roll-off is amplified.

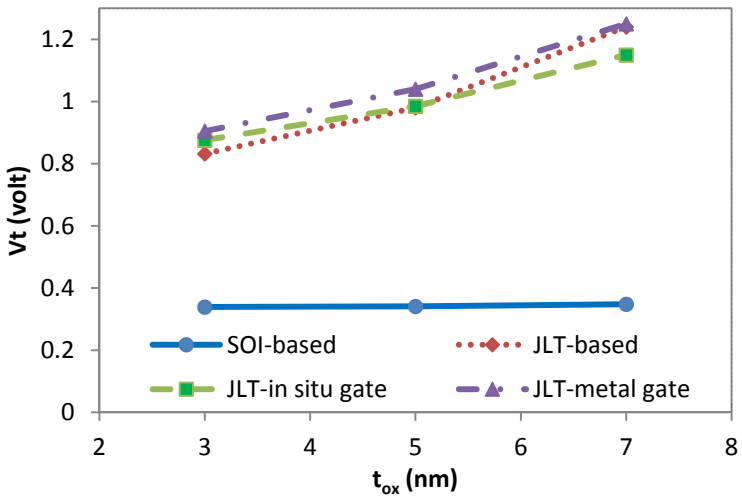

Figure 4. Threshold voltage shift due to oxide thickness variation for JLFET and SOI FET

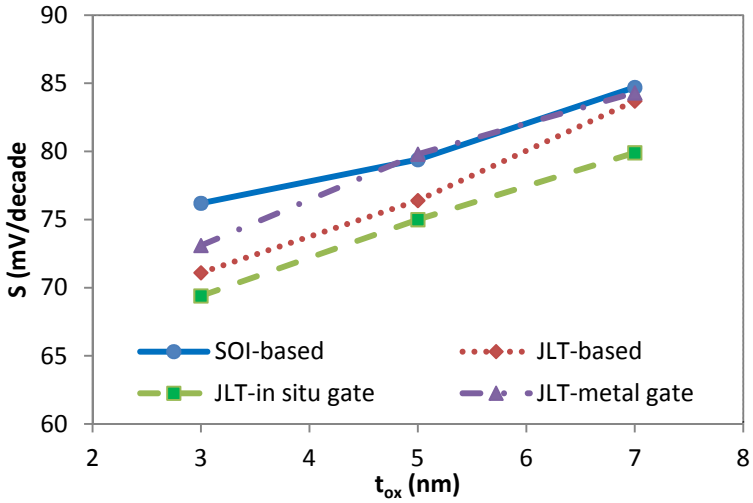

Figure 5. Subthreshold slope shift due to oxide thickness variation for JLFET and SOI FET

The simulation shown in Figure 5 reveals that both the SOI FET and variants of JLFET with polysilicon gate obtain lower subthreshold slope in thinner silicon oxide t_{ox}. This tendency is also evident for different sets of channel length. Smaller t_{ox} produces lower slope, with the tendency of reaching ideal value for tox less than 3 nm. The subthreshold slope is influenced by the channel length variation as well as the gate materials used in JLFET. The slope, S, is rising in the shorter channel length L, while the smaller oxide thickness exhibit lower slope, which is better. Smaller tox produces higher capacitance between gate and bulk silicon, therefore the charge under the oxide layer is under greater control of gate for inversion. In addition, the polysilicon-based gate shows better slope than the metal gate in short channel length. However, the metal gate based JLFET produces similar slope with SOI FET in thicker oxide. On the other hand, either the in situ or doped polysilicon gate based JLFET achieve lower slope, which is more beneficial.

Based on the trend of subthreshold variations in the change of channel length as well as oxide thinning, the short channel effect (SCE) can be evaluated further for all variants. The SCE in subthreshold performance is evident on the voltage threshold roll off and slope increase. However, the opposing tendency of V_T change between JLFETs and SOI FET leaves different scenario to resist against SCE. The manifestation of SCE in the form of V_T in all three variants of JLFET can be maintained small by simultaneous combination of L scaling and oxide thinning that result in adverse direction of threshold change. Therefore, the voltage roll-off is reduced and eventually the short channel effect (SCE) is minimized. However, the voltage roll-off in SOI is deteriorated further with the oxide thinning combined with channel scaling, therefore worsen the SCE. On the other hand, the trend of subthreshold slope increase due to channel scaling can be compensated with the decrease of oxide thickness in both SOI and JLFET, with the in-situ poly gate JLFET as the best performer between those structures under investigation.

Overall, the JLFET offers better performance than SOI especially in the SCE. Of JLFET structures, the poly-based JLFET produces slightly better promising performance than implanted poly-based JLFET, but outperform the metal based JLFET.

4. CONCLUSION

The subthreshold electrical performances of four different sets of FETs, i.e. SOI FET, metal-based JLFET, implanted poly-based FET and in-situ poly-based FET have been obtained and evaluated for L=50-200 nm using TCAD tools. Influence of different oxide thickness and the scaling effect were investigated as well. The result shows that for similar doping rate, the variants of JLFET generally produce superior subthreshold slope than the SOI FET with the slope value approaching near ideal value of 60 mV/decade. This trend is evident in both t_{ox} and L reductions that serve as an advantage. On the other hand, the threshold value shows different tendencies between those types of device. The variation of V_T in all three variants of JLFET can be maintained small by simultaneous combination of L scaling and oxide thinning, thus reducing the short channel effect (SCE) in terms of voltage roll-off. However, unlike the the scenario in JLFET, the SOI suffers from voltage roll-off when the scaling of channel is combined with oxide thinning.

The benefit of bulk transport mechanism offered by JLFET is evident in the better subthreshold slope. The investigation of the characteristic of junctionless transistor on the variation of gate material and

work function also shows that shifting of threshold voltage and subthreshold slope are evident. The polysilicon gate JLFET appears to provide better structure than metal gate JLFET for optimal output in very short channel with better performance in managing the short channel effect (SCE). This result offers better understanding on processing sequence of the devices which are very promising for the future generation devices.

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