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Design of carbon nanotube field effect transistor (CNTFET) small signal model

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ABSTRACT

The progress of Carbon Nanotube Field Effect Transistor (CNTFET) devices has facilitated the trimness of mobile phones, computers and all other electronic devices. CNTFET devices contribute to model these electronics instruments that require designing the devices. This research consists of the design and verification of the CNTFET device's small signal model. Scattering parameters (S-parameters) is extracted from the CNTFET model to construct equivalent small model circuit. Current sources, capacitors and resistors are involved to evaluate this equivalent circuit. S-parameters and small signal models are elaborated to analyze using a technique to form the small signal equivalent circuit model. In this design modeling process, at first intrinsic device's Y-parameters are determined. After that series of impedances are calculated. At last, Y-parameters model are transformed to add parasitic capacitances. The analysis result shows the acquiring high frequency performances are obtained from this equivalent circuit.

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1. INTRODUCTION

Carbon Nanotube Field Effect Transistor (CNTFET) attracted the attention of many scientists due to its excellent electrical properties. It offers a combination of high mobility, high cutoff frequency, large current density, small size, and ballistic transport. Last four decades, the electronics device industries are occupied by silicon-based devices. Silicon-based device performance and scaling are the key point to survive them in the industries [1]. But researchers are found the scaling limitation of the silicon-based devices.

Many researchers use silicon germanium (SiGe) and CMOS technologies but the production cost is high as the surface of silicon is important due to the large number of transistor used. The development of MOS transistor has always followed the Moore's law to the use of short channel. Therefore, the physical limit of this continuous scaling is achieved, and it is necessary to search for new materials that can increase the performance of the transistors. Carbon Nanotubes (CNTs) are currently considered as promising materials of a future nano-electronics technology. CNTFETs are using CNT as channel are able to overcome the silicon-base device's limitation [2]. With the various radius of CNT contains hexagonal structure of carbon mesh. Depends on the excellent electronics structure and nanometer size of CNT, it is able to become a market potential by replacing with the silicon.

Though researchers are in early stage of CNTFET development, few of them are able to model the SPICE design, Verilog circuits [3-4]. Current transforming phenomena in CNTFET's are exhibited excellent performance due to their ON-OFF ratio characteristics. It is possible to achieve higher density of current of similar dimension by performing parallel arrangement of CNTs [5, 6]. Some researchers are developed semiconducting CNTFET and metallic nanotubes as interconnects [7].

In this paper we present a simulation study of small signal model of CNTFET which act as a current amplifier that this amplifier changes an input current to a larger output current at 6.9 THz with the low input and high output impedance is generated using CNTFET technology. C language can be used for model implementation in SPICE software for the further action. For this purpose, the CNTFET model is presented first current amplifier. We adopt a CNTFET geometry using an array of parallel nanotubes as a transistor channel in order to reduce the parasitic capacitances and to improve the high frequency performance.

2. PHYSICS OF BALLISTIC CNTFETS

CNTFET's ballistic assumption can be made by considering three conditions. Firstly, scattering carrier in the channel are propagating to the drain and then back to the gate without scattering. Carrier transport becomes ballistic in this situation [8]. The drain current is proportional with CNT diameter and calculated from channel length. Secondly, four capacitors are jointly recognized as CNT. Such as, gate capacitor (C_G), source capacitor (C_S), drain capacitor (C_D) and quantum capacitor (C_Q). The highest limit would be determined by C_Q because of the higher value of C_G than the others three capacitors [4-9]. Finally, C_Q controls the CNTFET operation. If C_G greater than C_Q then V_D increases, and channel charge decreases. Similarly, if C_G less than C_Q then channel charge become independent [10].

Three different structures of CNT insulator with gate are elaborated in Figure 1 and Figure 1(c) consists of the number of CNT insulator of gate which has pitch(S) in between two of them. Gate insulator is most significant due to the Current flow was prevented by the electrostatic potential barrier in the source and drain region. According to the Figure 1 (b) and (c), Gate capacitor become,

$$C_G = \frac{2\pi\varepsilon_0\varepsilon_r L}{ln[2(t_{ins}+r)/r]} \quad (1)$$

Where, r: Nanotube radius, L: Gate length, ε_r: Dielectric constant and tins: Oxide thickness. C_G becomes in the planar gate,

$$C_G = \frac{2\pi\varepsilon_0\varepsilon_r L}{cosh^{-1}(t_{ins}/r)} \quad (2)$$

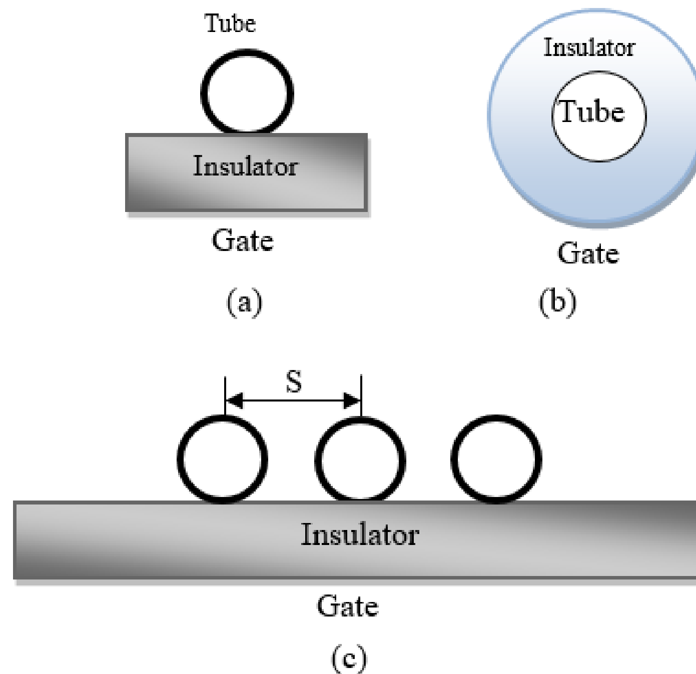

Figure 1. Different structural capacitors: (a) single CNT capacitor; (b) coaxial gated CNT capacitors; (c) array of CNT capacitors

Figure 2 shows a 3D view of CNFET device structure that is used for the modeling in SPICE CNTFET model. It contains of Gate, Drain and Source with array of CNTs capacitors. The CNTs are embedded by gate dielectric and connected to the source and drain metals is placed on the thick oxide layers similar structure to CMOS CNT as the channel. In this paper, the proposed design of the CNTFET model configurations based on single walled carbon nanotubes (SWNTs). The periodic boundary conditions impose restrictions on available states [11-18] that depending on radius in an energy discrete set from subband structure as shown in Figure 3. An analytical calculation is assumed to illustrate the the subband's energy of semiconducting CNTs [19-29].

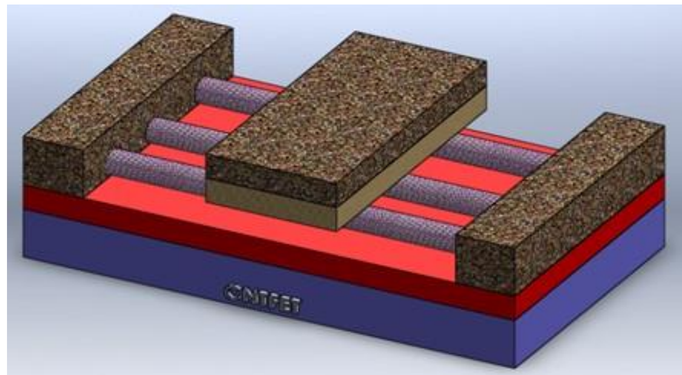

Figure 2. CNTFET 3D view of CNTFEDT model illustration

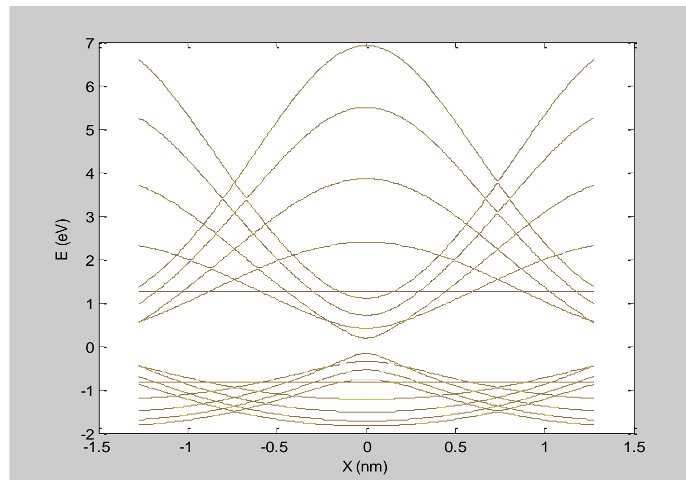

Figure 3. Single walled carbon nanotube sub-band structure

3. SMALL SIGNAL MODELS FOR CNTFETS

This section describes how the small signal model circuit is designed and analyzed as shown in Figure 4. Parasitic elements of this model CNTFET circuits are excluded. The intrinsic circuit of CNTFET includes inter electrode capacitance Cdg between the Drain and Gate, Gate-Source capacitance Cgs, inter electrode capacitance between the Drain and Source Cds, and gain parameter associated with the voltage controlled current source gm. Y-parameters is presented as the equivalent circuit elements. Figure 4 shows the Y-parameter representation with 3 terminals. Y12 and Y21 represent voltage controlled current sources and Y11 and Y22 represent shunt admittances.

Figure 4 also shows the CNTFET's interconnected small signal model. Due to short circuit of substrate to source, these are excluded in the small signal model. Therefore, substrate to source resistance is ignored. The entire component of the small signal model makes it scalable to fit in different dimensional device. The effective channel resistance is represented by gate resistance (Rg). In this model, Rsubd represents the bulk resistance and Cjd represents the bulk capacitance.

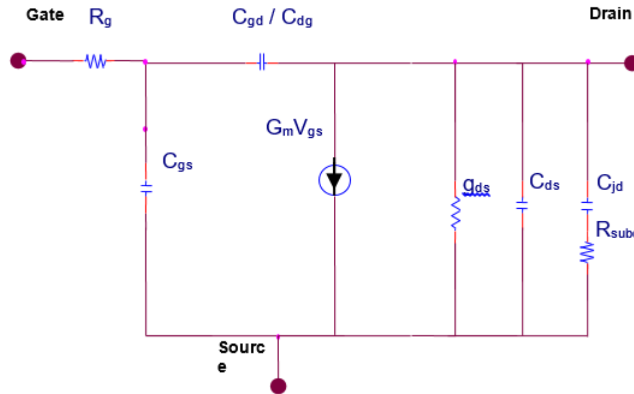

Figure 4. CNTFET small signal model

3.1. Methodology

The model consists of four capacitances Cds, Cdg, Cgd, Cgs. and three terminals source, drain and gate. Figure 3 shows the connectivity and elaboration of all the capacitors. Following analytical calculations are elucidated using drain current Id, gate current Ig and the charges,

$$C_{gs} = \frac{\Delta Q_g}{\Delta V_{gs}}, C_{gd} = \frac{\Delta Q_g}{\Delta V_{gd}} \tag{3}$$

$$C_{dg} = \frac{\Delta Q_d}{\Delta V_{dg}}, C_{ds} = \frac{\Delta Q_d}{\Delta V_{ds}} \tag{4}$$

$$i_g = \frac{dQ_g}{dt} = \frac{fQ_g}{fV_{gs}}\frac{dV_{gs}}{dt} + \frac{fQ_g}{fV_{gd}}\frac{dV_{gd}}{dt} = C_{gs}\frac{dV_{gs}}{dt} + C_{gd}\frac{dV_{gd}}{dt} \tag{5}$$

$$i_d = \frac{dQ_d}{dt} = \frac{fQ_d}{fV_{dg}}\frac{dV_{dg}}{dt} + \frac{fQ_d}{fV_{ds}}\frac{dV_{ds}}{dt} = C_{dg}\frac{dV_{dg}}{dt} + C_{ds}\frac{dV_{ds}}{dt} \tag{6}$$

In (3) and (4), due to not equal of the capacitances Cgd and Cdg, they are expressed separately. To construct small signal mode, these capacitors are required to complete the circuit. Figure 4 shows the equivalent small signal model for CNTFET that can be charged by nonreciprocal capacitances [10]. By using linear regression method Y-parameter can be solved from the S-parameter measuring value. According to the Figure 3, Y-parameter can be elaborated in the following equations,

$$Y_{11} = \frac{\omega^2(C_{gs}+C_{gd})^2R_g + j\omega(C_{gs}+C_{gd})}{1+\omega^2(C_{gs}+C_{gd})^2{R_g}^2} \tag{7}$$

$$Y_{12} = \frac{-\omega^2C_{gd}(C_{gs}+C_{gd})^2R_g - j\omega C_{gd}}{1+\omega^2(C_{gs}+C_{gd})^2{R_s}^2} \tag{8}$$

$$Y_{21} = \frac{g_m - \omega^2C_{dg}(C_{gs}+C_{dg})^2R_g - j\omega C_{dg} - j\omega g_m R_g(C_{gs}+C_{dg})}{1+\omega^2(C_{gs}+C_{dg})^2{R_g}^2} \tag{9}$$

$$Y_{22} = g_m + \frac{\omega^2C_{jd}R_{subd}+j\omega C_{jd}}{1+\omega^2{C_{jd}}^2{R_{subd}}^2} + j\omega C_{ds} + \frac{\omega^2{C_{dg}}^2R_g+j\omega C_{dg}+j\omega^2{R_g}^2C_{gs}C_{ds}(C_{gs}+C_{dg})}{1+\omega^2(C_{gs}+C_{dg})^2{R_g}^2} \tag{10}$$

$\omega^2(C_{gs}+C_{gd})^2{R_g}^2 << 1$ Provides the operation frequency up to 6.9THz. In line with this assumption, Y-parameter can be extended to the following equations,

$$Y_{11} \cup \omega^2(C_{gs}+C_{gd})^2R_g + j\omega(C_{gs}+C_{gd}) \quad (11)$$

$$Y_{12} \cup -\omega^2 C_{gd}(C_{gs}+C_{gd})R_g - j\omega C_{gd} \quad (12)$$

$$Y_{21} \cup g_m - \omega^2 C_{dg}(C_{gs}+C_{dg})^2R_g - j\omega C_{dg} - j\omega g_m R_g(C_{gs}+C_{dg}) \quad (13)$$

$$Y_{22} \cup g_{ds} + \frac{\omega^2 C_{jd}{}^2 R_{subd}}{1+\omega^2 C_{jd}{}^2 R_{subd}{}^2} + \omega^2 C_{dg}{}^2 R_g + \frac{j\omega C_{jd}}{1+\omega^2 C_{jd}{}^2 R_{subd}{}^2} + j\omega C_{ds} + j\omega C_{dg} \quad (14)$$

g_m, g_{ds}, R_g, C_{gd}, C_{dg}, C_{gs} parameters are calculated from the following equations,

$$C_{gd} = -Im[Y_{12}]/\omega \quad (15)$$

$$R_g = Re[Y_{11}]/(Im[Y_{11}])^2 \quad (16)$$

$$C_{gs} = Im[Y_{11}]/\omega - C_{gd} \quad (17)$$

$$g_m = Re[Y_{21}]|_{\omega^2=0} \quad (18)$$

$$C_{dg} = \frac{-Im[Y_{21}]/\omega - g_m R_c C_{gs}}{1+g_m R_g} \quad (19)$$

$$g_{ds} = Re[Y_{22}]|_{\omega^2=0} \quad (20)$$

$\omega^2/[Re[Y_{22}] - g_{ds} - \omega^2 C_{dg}{}^2 R_g{}^2]$ vs. ω^2use to achieve Cjd and Rsubd by the following equation.

$$\frac{\omega^2}{Re[Y_{22}] - g_{ds} - \omega^2 C_{ds}{}^2 R_g} = \omega^2 R_{subd} + \frac{1}{C_{jd}{}^2 R_{subd}} \quad (21)$$

$\omega^2/[Re[Y_{22}] - g_{ds} - \omega^2 C_{dg}{}^2 R_g{}^2]$ Helps to get Rsubd from the ω^2function.

$$C_{jd} = \frac{1}{\sqrt{\frac{\omega^2 R_{subd}}{Re[Y_{22}] - g_{ds} - \omega^2 C_{dg}{}^2 R_g} - \omega^2 R_{subd}{}^2}} \quad (22)$$

The (19) refer the calculation of C_{ds},

$$C_{ds} = Im[Y_{22}]/\omega - C_{dg} - \frac{C_{jd}}{1+\omega^2 C_{jd}{}^2 R_{subd}{}^2} \quad (23)$$

4. RESULTS

The Charge preservation parameters capacitances are examined from the (15) to (23). From the above analytical analysis, a set of simulation is done to verify the small signal model. In order to observe the performance of the CNTFET model parameters, simulation has been done for gain, gate impedance, intrinsic capacitance, transconductance, and bulk admittance with the variation of frequency. Figure 5 shows the gain versus frequency of the CNTFET small signal model. The unity gain frequency is reached at 6.9THz and the magnitude of current gain goes to 45dB. Figure 6 shows the gate impedance graph. A comparison is realized from Figure 7 in between Cgs and Cds. Finally, tranconductance and bulk admittance is plot in Figure 8.

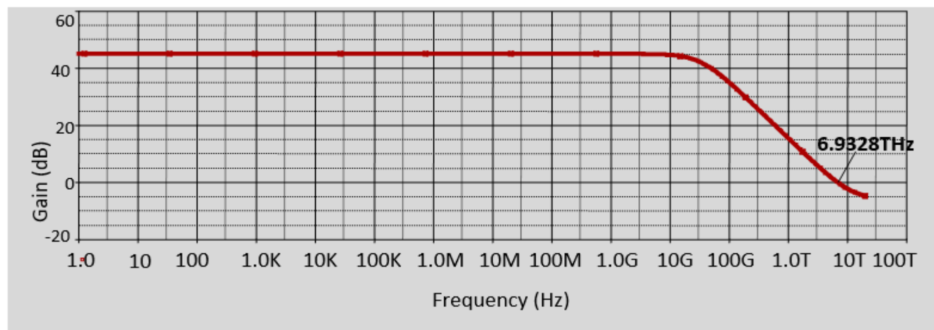

Figure 5. Output current gain of the CNTFET at 6.9 THz frequency

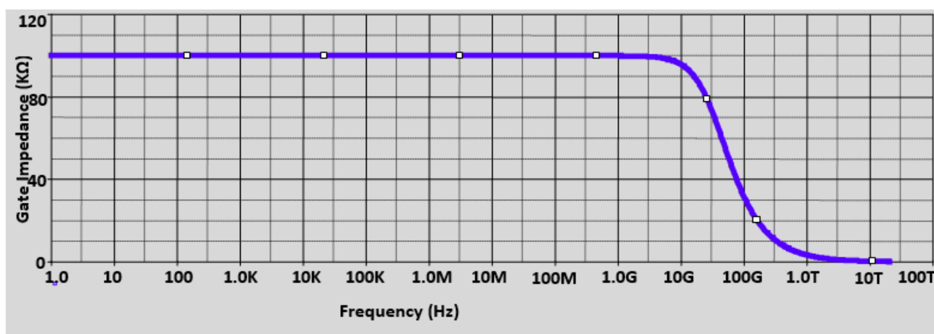

Figure 6. CNTFET Gate Impedance at high frequency

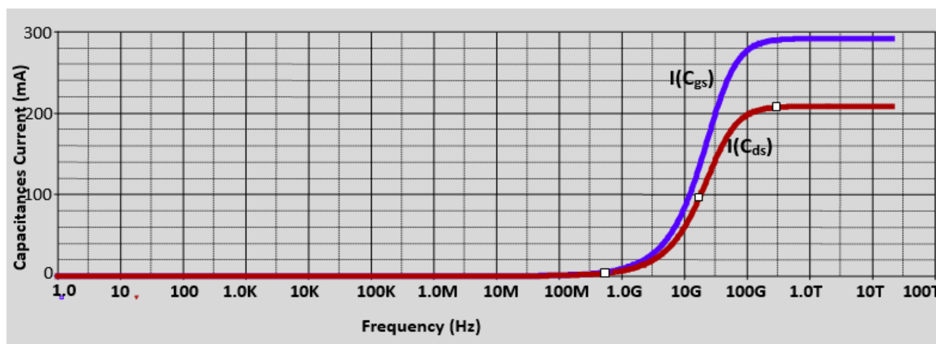

Figure 7. CNTFET's intrinsic capacitance Cgs, Cds current at 6.9 THz frequency

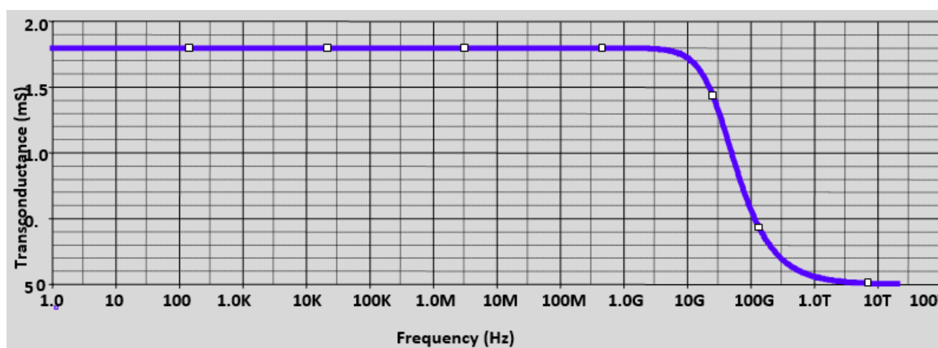

Figure 8. The transconductance (gm) of the CNTFET small signal model

5. CONCLUSION

This paper elucidated a brief analysis of the proposed design of CNTFET small signal model. The design consists of proper illustration of the small signal method and demonstrated the performances by simulating small-signal parameters for CNTFET with respect to the gain of 45dB. The intrinsic capacitance is 14aF, transconductance is 1.8mS is used in this analysis. Furthermore, this technique has introduced the capacitance to evaluate the charge preservation capacitance at the frequency of 6.9THz.

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