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Extended family of DC-DC quasi-Z-source converters

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ABSTRACT

The family of DC-DC q-ZSCs is extended from two to three classes and four to six members. All the members were analyzed based on efficient duty ratio range (R_{Deff}) and general duty ratio range (R_{Dgen}). Findings showed that similar to the traditional buck-boost converter (BBC), each of the topologies is theoretically capable of inverted buck-boost (BB) operation for the R_{Dgen} with additional advantages but differed according to class in how the gains are achieved. The new topologies have advantages of BB capability at the R_{Deff}, continuous and operable duty ratio range with unity gain at $D = 0.5$ contrary to existing topologies where undefined or zero gain is produced. Potential applications of each class were discussed with suitable topologies for applications such as fuel cells, photovoltaic, uninterruptible power supply (UPS), hybrid energy storage and load levelling systems identified.

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1. INTRODUCTION

Power converters convert electric energy from a magnitude or form to another [1, 2]. DC-DC converters convert between DC voltages, while ac-ac converters convert between ac-signals. DC-ac and ac-DC converters called inverters and rectifiers respectively convert between DC and ac signals. DC-DC converters are essential in applications involving DC signals of variable magnitudes. They generally involve using switches mostly transistors and are classified as linear or switched mode DC-DC converters depending on how the transistors are operated.

Linear mode converters involve operating the transistor at a given operating point in the linear region and regulation is achieved by varying the transistor base current (I_B) hence functions like a variable resistor [3]. In switched mode converters, transistors function as switches where they are switched ON/OFF based on their duty ratios (D). Linear mode converters are characterised by low efficiency while switched mode converters contain harmonics due to switching and require filters [4-8]. Switched mode converters were further classified into voltage source converters (VSCs) and current source converters (CSCs) until the invention of impedance source converters (ISCs/ZSCs) [9].

ISCs permits both the shoot-through (ST) limitation of VSCs without causing overcurrent for voltage boosting and open circuit (OC) limitation of CSCs without causing overvoltage for current boosting [9-13]. ST phenomenon is simultaneous switching of both switches of a common leg of an H-bridge while OC refers to turning them both OFF [14]. Dead-time and overlap-time are provided in VSCs and CSCs respectively to cater for ST and OC respectively but that causes waveform distortion and causes frequency restriction because the chances of ST or OC increases with frequency due to the possible interval becoming shorter [9, 15]. Elimination of dead and overlap-time in ISCs permits higher frequency operation leading to

reduced size, weight and cost [16]. Inductors of ISCs store energy during ST and release them during different modes while robustness of ISCs is that they can be controlled with or without ST [17-19].

A derivative of the ZSCs called quasi-ZSC (q-ZSC) shown in Figure 1 (a) was proposed by [20] to address problems including discontinuous input current during boost mode, reduced source stress and simplified control strategy. Reference [21] extended the applications of ZSCs and q-ZSCs from dc-ac [9, 18, 22-35] and ac-ac [36] to DC-DC application by proposing four topologies each for ZSC and q-ZSC topologies. The extension to DC-DC was done by taking the output across a capacitor rather than switch S_2 for both the dc-ac and ac-ac converters as shown in Figure 1 (b).

Both the DC-DC ZSC and q-ZSC families consisted of two classes each with each class comprising of two topologies. Derivation of variant topologies was possible due to the fact that the output could be taken across any capacitor and the positions of the input source and a capacitor could be swapped [21]. Other variant DC-DC converter topologies took their outputs across S_2 in what is called pulse width modulated (PWM) DC-DC ISCs [37-43] for higher voltage gain albeit with additional components. Reference [44] took the DC output parallel to the impedance network input port rather than a capacitor or switch in order to achieve common ground and high voltage gain. Detailed steady-state analysis of PWM DC-DC ISCs was presented by [38].

DC-DC ISCs are further classified according to galvanic isolation into isolated and non-isolated [12, 45]. Topologies with transformer isolation usually have safety advantages and higher voltage gain but constrained by their relatively high cost and complexity, more switches requirement and low efficiency [45, 46]. Non-isolated DC-DC ISCs have advantages of low cost, less complexities and switches and higher efficiency but are constrained by safety problem and lower voltage gain [46].

The existing family of DC-DC q-ZSCs [21] with two classes has the advantage of bidirectional operation and bipolar output operation. However, each of the classes has problems of lacking buck-boost (BB) capability at efficient duty ratio range (R_{Deff}) and either discontinuous or lower gain [47].

In this paper, a new class of DC-DC q-ZSCs is presented to extend the family of DC-DC q-ZSCs from two to three classes. Members of the new class have BB capability at the R_{Deff}, continuous or higher gain compared to existing members. A general analysis of all the classes and their topologies is presented in details by first deriving the gain of each topology. Operations of all the classes were verified by simulation and the responses of Class B and Class C conform to their theoretical gains. The responses of Class C members disagreed with their theoretical gain due to the discontinuity in their gain.

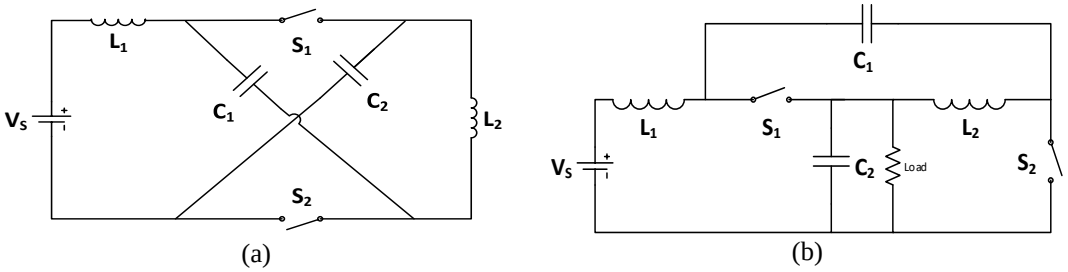


Figure 1. (a) Generic q-ZSC (b) DC-DC q-ZSC

2. OVERVIEW

a) Existing topologies

The concept q-ZSC was extended by [21] from inverter [20] to DC-DC applications. This produced four different topologies shown in Figure 2(a) to Figure 2(d) of which two of each have an identical gain curve. This lead to having two classes of DC-DC q-ZSC with each class consisting of two members [21]. Members of each class have an identical gain equation.

b) Additional topologies

Two new DC-DC converter topologies with the shared properties of q-ZSCs and traditional BBCs shown in Figure 2(e) and Figure 2(f) were recently proposed [2, 14]. Analysis of their operation shows common properties such as gain equation and output response, therefore, can be grouped as a class [47].

c) Extended family

Combining the existing four DC-DC q-ZSC topologies and the two additional topologies result in having an extended family consisting of six members as shown in Figure 2. Of these six members, three gain curves exist, of which each consists of two members. This means that the extended family consists of three classes with each having two topologies [21, 47].

3. CIRCUIT ANALYSIS

In this section, the operation of each class is analysed based on two operation modes to derive the gain equation of each topology in the class. Although ISCs can support more than two operation modes due to the permissibility of ST and OC, two operation modes were considered here because

a. Existing analyses for the existing topologies [21] are based on two switching modes.
b. Use of two switching modes enables fair comparison with other DC-DC topologies that only support two modes.

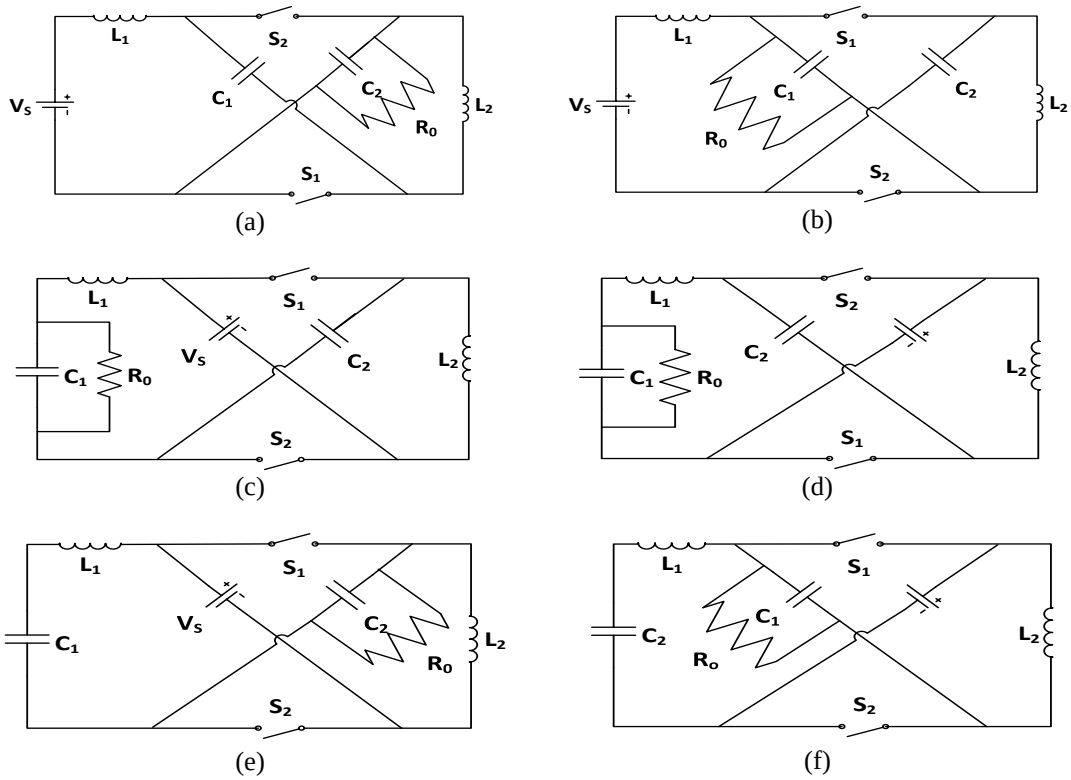


Figure 2. Extended family of DC-DC q-ZSCs

The topologies in a class are labelled as topology I and topology II. The operation of each topology is analysed based on the switching modes and the equivalent circuits for each mode are also shown. The parameters used for the circuits analyses are V_{L1} (voltage across L_1), V_{L2} (voltage across L_2), V_{C1} (voltage across C_1), V_{C2} (voltage across C_2), V_O (output voltage), V_S (input voltage) and D (duty ratio). The switches S_1 and S_2 were assumed to be ideal.

a) Class A

This class consist of the topologies of Figure 2(a) and (b) labelled as topology I and topology II and shown in Figure 3 and Figure 4 respectively.

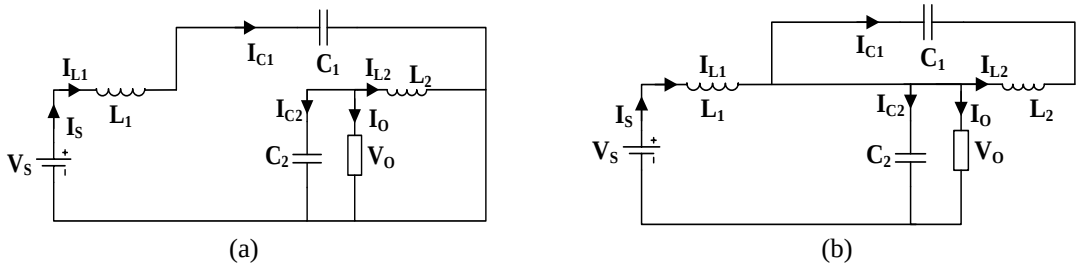


Figure 3. Class A topology I (a) mode I (b) mode II

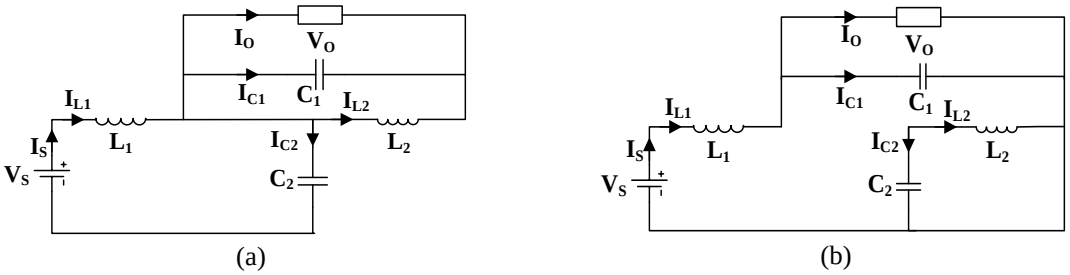


Figure 4. Class A topology II, (a) mode I (b) mode II

1. Class A topology I

Mode I: In this mode, S_1 is ON while S_2 is OFF as shown in Figure 3(a), the duty ratio is D.

$$V_{L1} = V_S - V_{C1} \quad (1)$$

$$V_{L2} = V_O \quad (2)$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 3(b), the duty ratio is $D' = 1 - D$.

$$V_{L1} = V_S - V_O \quad (3)$$

$$V_{L2} = V_{C1} \quad (4)$$

Applying Volt second balance (VSB) to get the average inductor voltages over a switching period on the inductors L_1 and L_2 yields (5) and (6).

$$\overline{V}_{L1} = -DV_{C1} + V_S - V_O + DV_O = 0 \quad (5)$$

$$\overline{V}_{L2} = DV_O + V_{C1} - DV_{C1} = 0 \quad (6)$$

From (6),

$$V_{C1} = -\frac{DV_O}{1-D} \quad (7)$$

Substituting (7) into (5) and simplifying yields

$$A_{a1} = \frac{V_O}{V_S} = \frac{1-D}{1-2D} \quad (8)$$

2. Class A topology II

Mode I: In this mode, S_1 is ON while S_2 is OFF as shown in Figure 4(a), the duty ratio is D.

$$V_{L1} = V_S - V_{C2} \quad (9)$$

$$V_{L2} = V_O \quad (10)$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 4(b) the duty ratio is $D' = 1 - D$.

$$V_{L1} = V_S - V_O \quad (11)$$

$$V_{L2} = V_{C2} \quad (12)$$

Applying VSB on L_1 and L_2 yields (13) and (14).

$$\overline{V}_{L1} = V_S - V_O + DV_O - DV_{C2} = 0 \quad (13)$$

$$\overline{V}_{L2} = DV_O + V_{C2} - DV_{C2} = 0 \quad (14)$$

From (14),

$$V_{C2} = \frac{DV_O}{D-1} \quad (15)$$

Substituting (15) into (13) yields

$$A_{a2} = \frac{V_O}{V_S} = \frac{1-D}{1-2D} \quad (16)$$

The (8) And (16) show that the ideal gains of topology I and II are identical as proposed by [21] thus they form a class with gain.

$$A_a = A_{a1} = A_{a2} = \frac{1-D}{1-2D} = \frac{D'}{D'-D} \quad (17)$$

b) Class B

The topologies in Figure 2(c) and (d) are members labelled as topology I and II and shown in Figure 5 and Figure 6 respectively.

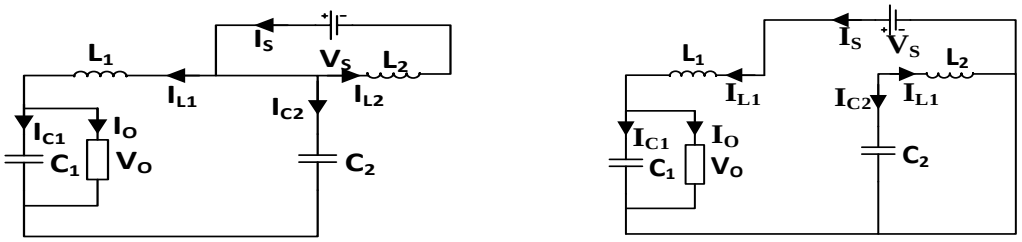


Figure 5. Class B topology I (a) mode I (b) mode II

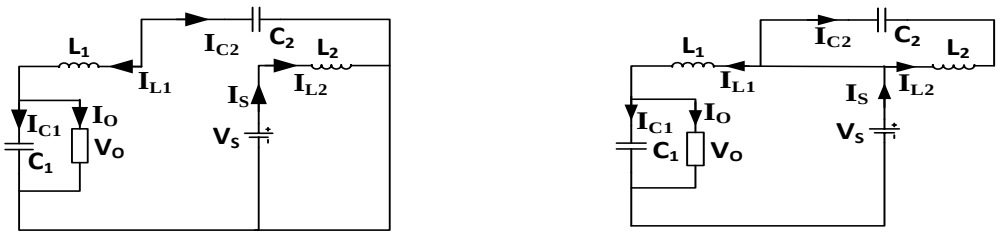


Figure 6. Class B topology II (a) mode I (b) mode II

1. Family B topology I

Mode I: In this mode, S_1 is ON while S_2 is OFF as shown in Figure 5(a), the duty ratio is D.

$$V_{L1} = V_{C2} - V_O \quad (18)$$

$$V_{L2} = V_S \quad (19)$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 5(b), the duty ratio is $D' = 1 - D$.

$$V_{L1} = V_S - V_O \quad (20)$$

$$V_{L2} = V_{C2} \quad (21)$$

Applying VSB on L_1 and L_2 yields (22) and (23).

$$\overline{V}_{L1} = DV_{C2} + V_S - V_O - DV_S = 0 \quad (22)$$

$$\overline{V}_{L2} = DV_S + V_{C2} - DV_{C2} = 0 \quad (23)$$

From (23),

$$V_{C2} = \frac{-D}{1-D} V_S \quad (24)$$

Substituting (24) into (22) and simplifying yields

$$A_{b1} = \frac{V_O}{V_S} = \frac{1-2D}{1-D} \quad (25)$$

2. Class B topology II

Mode I: In this mode, S_1 is ON while S_2 is OFF as shown in Figure 6(a), the duty ratio is D.

$$V_{L1} = V_{C2} - V_O \quad (26)$$

$$V_{L2} = V_S \quad (27)$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 6(b), the duty ratio is $D' = 1 - D$.

$$V_{L1} = V_S - V_O \quad (28)$$

$$V_{L2} = V_{C2} \quad (29)$$

Applying VSB on L_1 and L_2 yields (30) and (31).

$$\overline{V}_{L1} = DV_{C2} + V_S - V_O - DV_S = 0 \quad (30)$$

$$\overline{V}_{L2} = DV_S + V_{C2} - DV_{C2} = 0 \quad (31)$$

From (31),

$$V_{C2} = \frac{-D}{1-D} V_S \quad (32)$$

Substituting (32) into (30) and simplifying yields

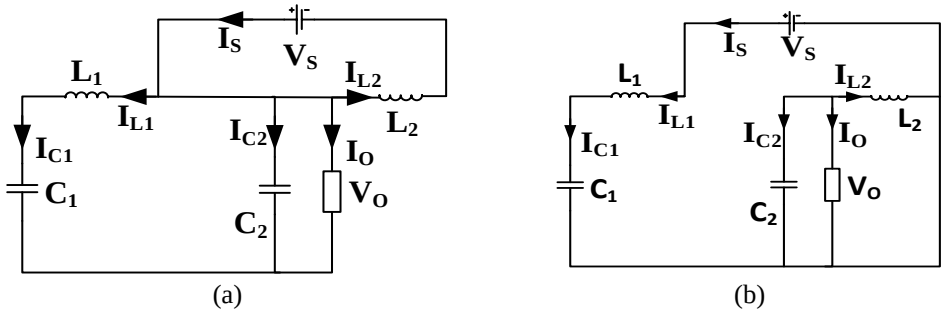
$$A_{b2} = \frac{V_O}{V_S} = \frac{1-2D}{1-D} \quad (33)$$

The (25) And (33) show that the ideal gains of topology I A_{b1} and topology II A_{b2} are identical as proposed by [21] thus they form a class with gain.

$$A_b = A_{b1} = A_{b2} = \frac{1-2D}{1-D} = \frac{D'-D}{D'} \quad (34)$$

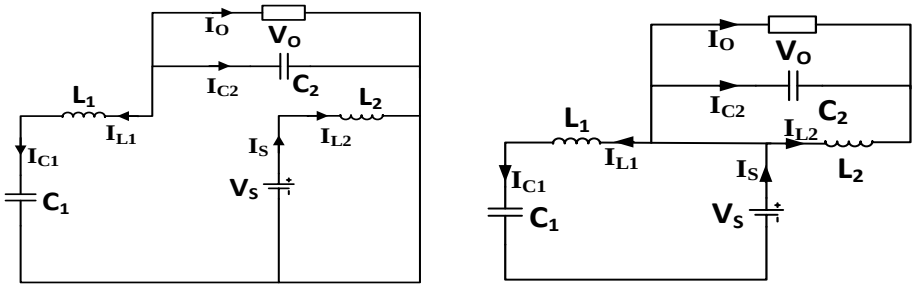
c) Class C

This class consist of the two newly proposed topologies of Figure 2(e) and (f). They are also labelled as topology I and topology II as shown in Figure 7 and Figure 8 respectively.



(a) (b)

Figure 7. Class C topology I (a) mode I (b) mode II



(a) (b)

Figure 8. Class C topology II (a) mode I (b) mode II

1. Class C topology I

Mode I: In this mode, S_1 is ON while S_2 is OFF as shown in Figure 7(a), the duty ratio is D.

$$V_{L1} = V_O - V_{C1} \quad (35)$$

$$V_{L2} = V_S \quad (36)$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 7(b), the duty ratio is $D' = 1 - D$.

$$V_{L1} = V_S - V_{C1} \quad (37)$$

$$V_{L2} = V_O \quad (38)$$

Applying VSB on L_1 and L_2 yields (39) and (40).

$$\overline{V}_{L1} = DV_O + V_S - V_{C1} - DV_S = 0 \quad (39)$$

$$\overline{V}_{L2} = DV_S - V_O(D-1) = 0 \quad (40)$$

Simplifying (40) yields

$$V_O = -\frac{D}{1-D} V_S \quad (41)$$

$$A_{c1} = \frac{V_O}{V_S} = \frac{-D}{1-D} \quad (42)$$

2. Class C topology Ii

Mode I: In this mode, S_1 is ON while S_2 is OFF as shown in Figure 7(a), the duty ratio is D.

$$V_{L1} = V_O - V_{C1} \quad (43)$$

$$V_{L2} = V_S \quad (44)$$

Mode II: In this mode, S_1 is OFF while S_2 is ON as shown in Figure 7(b), the duty ratio is $D' = 1 - D$.

$$V_{L1} = V_S - V_{C1} \quad (45)$$

$$V_{L2} = V_O \quad (46)$$

Applying VSB on L_1 and L_2 yields (47) and (48).

$$\overline{V}_{L1} = DV_O + V_S - V_{C1} - DV_S = 0 \quad (47)$$

$$\overline{V}_{L2} = DV_S + V_O(1 - D) = 0 \quad (48)$$

Simplifying (48) yields

$$V_O = -\frac{D}{1-D} V_S \quad (49)$$

$$A_{c2} = \frac{V_O}{V_S} = \frac{-D}{1-D} \quad (50)$$

The (42) And (50) show that the ideal gains of topology I A_{c1} and topology II A_{c2} are identical thus they form a class [47] with gain.

$$A_c = A_{c1} = A_{c2} = \frac{-D}{1-D} = \frac{-D}{D'} \quad (51)$$

The gain in (51) is the same as the gain of traditional BBC [2, 14].

The circuit analyses above show that the six topologies form three classes A, B and C with gains given by (17), (34) and (51) respectively for each class. Class A and class B have been previously presented [21]. The new class (class C), similar to the existing classes also consist of two topologies with identical gain equation, a quasi-impedance source network (q-ISN) comprising of two inductors, two capacitors and two switches.

The gains of the three classes are plotted against D in Figure 9. The capacitor C_1 and inductor L_1 form a series LC network with impedance Z_1 regardless of operating mode, contrary to the existing topologies where the series LC networks are formed only during given modes. This implies that the characteristics of the topologies will be altered when operated at their resonant frequencies due to resonance.

4. OPERATIONS AND APPLICABILITY

This section analyses the operations of each class as D is varied from 0 to 1. The D range (R_D) is classified into the efficient R_D (0.35 to 0.65) [12, 38, 48] and general R_D (0 to 1) thereby resulting in efficient gain range (R_{Aeff}) and general gain range (R_A). Suitable applications for each class are also discussed.

a) Efficient duty ratio range (R_{Deff})

Operations of complementarily switched converters are more efficient at R_D of 0.35 to 0.65 due to less ringing, reverse recovery problem and conduction loss [12, 38, 48, 49]. This is because when either of the switches is operated at lower D, the other is at higher D (inverse D relationship) thus increasing conduction loss, ringing and other non-idealities [38]. The boundaries and midpoint of the efficient R_D (R_{Deff}) were applied to the gain equations of these three classes to analyse their gains for the R_{Deff}. Figure 9(b) shows plots of the gains against D for R_{Deff}.

1. Class A

Applying the boundary and midpoint Ds of R_{Deff} to the gain equation of class A in (17), the resulting gains are

$$A_{a0.35} = \frac{1-0.35}{1-2(0.65)} = 2.1667 \quad (52)$$

$$A_{a0.5} = \frac{1-0.5}{1-2(0.5)} = \text{undefined} \quad (53)$$

$$A_{a0.65} = \frac{1-0.65}{1-2(0.35)} = -1.1667 \quad (54)$$

The (53) is undefined $A_{a0.5} = \frac{0.5}{0}$ because division by zero is undefined. The concept of limit is applied to have more idea on what actually occurred as $D \to 0.5$.

$$\lim_{D\to 0.5} A_a = \lim_{D\to 0.5} \frac{1-D}{1-2D} \tag{55}$$

If the limit of the function exists at 0.5, then its two one-sided limits $\lim_{D\to 0.5^+} A_a$ and $\lim_{D\to 0.5^-} A_a$ must be equal else the limit does not exist. $\lim_{D\to 0.5^+} A_a$ is the limit from the right as $D \to 0.5$ while $\lim_{D\to 0.5^-} A_a$ is the limit to the left as $D \to 0.5$.

The concept of right-sided limit (RSL) and left-sided limit (LSL) can be described using increasing and decreasing D in tuning. When a D set point is approached from a higher D such as bucking operation in traditional BBC, it is RSL ($D \gtrsim 0.5$ such that $D - 0.5 = 0^+ \Rightarrow 2D \gtrsim 1$). When D is approached from a lower D such as boosting operation in traditional BBC, it is an LSL limit ($D \lesssim 0.5$ such that $D - 0.5 = 0^- \Rightarrow 2D \lesssim 1$). Evaluating the RSL and LSL yields

$$\lim_{D\to 0.5^+} A_a = +\infty \tag{56}$$

$$\lim_{D\to 0.5^-} A_a = -\infty \tag{57}$$

$$\lim_{D\to 0.5^+} A_a \neq \lim_{D\to 0.5^-} A_a \tag{58}$$

The (58) Shows that the one-sided limits are not identical therefore the limit does not exist at $D = 0.5$, thus the converter cannot be operated at $D = 0.5$. It shows that for this R_D (0.35 to 0.65), the gain is discontinuous at $D = 0.5$ because it's limit $\lim_{D\to 0.5} A_a$ does not exist. The range of gain for class A (R_{Aa}) corresponding to R_{Deff} with the RSL and LSL incorporated to account for the discontinuity is

$$R_{Aaeff} = [2.1667, \infty)\ (-\infty, -1.1667] \tag{59}$$

This discontinuity results in having two separate gains as shown by the two dotted curves of Figure 9(b) and the two ranges of (59). They are (i) non-inverting gain (upper dotted curve of Figure 9(b)) with range (R_{Aeff}) $= [2.1667, \infty)$ and (ii) the inverting gain curve (lower dotted curve of Figure 9(b)) with range (R_{Aeff}) $[-1.1667, -\infty)$ described as non-inverting boost with gain from 2.1667 to ∞ and inverting boost with gain from $-\infty$ to -1.1667.

The theoretical gain for this class is bipolar with magnitude >1 throughout the R_{Deff} hence it functions only as boost converter but lacks buck capability at this R_D. Special precautions have to be taken to avoid operation within the neighbourhood of $D = 0.5$ because of the infinite gain.

Applicability: For the positive boost range of (59), $R_{Aa} = [2.1667, \infty)$ at $R_D = [0.35, 0.5)$. This high boost only capability makes the topologies in this class suitable for applications where voltage boosting is required like fuel cells. If the maximum input voltage magnitude is less than half the required output ($|V_S| < 0.5|V_O|$), the converter can be operated within [0.35, 0.5) with an ideal gain capability of $10V_S$ at $D = 0.4737$, else it should be operated within (0.5, 0.65] duty ratio to get an inverted boost operation. By employing active switches (MOSFET) and their anti-parallel diodes, they are capable of providing bidirectional current and bidirectional voltage [21].

Suitable applications based on its theoretical gain include hybrid energy storage system (HESS) where energy may be transferred from battery to super-capacitor (SC) and vice versa [48], uninterruptible power supply (UPS) [49] and fuel cell application [9] where high gain is needed etc. However, simulation results obtained from the verification section raises doubt over the high boost capability. See the discussion section for more details.

2. Class B

Applying the boundary and midpoint Ds of R_{Deff} to the gain equation of class A in (17), the resulting gains are

$$A_{b0.35} = \frac{1-2(0.5)}{1-(0.5)} = 0.4615 \tag{60}$$

$$A_{b0.5} = \frac{1-2(0.5)}{1-(0.5)} = 0 \tag{61}$$

$$A_{b0.65} = \frac{1-2(0.35)}{1-0.65} = -0.8571 \quad (62)$$

The gain for this class is continuous, it exists at $D = 0.5$ and is zero as shown in (61). The gain range is $R_{Abeff} = [0.4615, -0.8571]$ and is bipolar with magnitude <1 hence it functions only as bipolar buck converter and lack boost capability within this R_{Deff} of 0.35 to 0.65.

Precautions have to be taken to handle the change in polarity that occurs at the neighbourhood of $D = 0.5$ because of the effect on power flow.

Applicability: Potential application could be in a grid-connected inverter system where the ESS is charged by a higher voltage source and the ESS later powers an inverter (load) at a lower voltage. Another application is in electric vehicle (EV) where ESS packs are designed in higher voltages e.g. 48 V than auxiliary loads such as lighting and radio systems which are operated at lower voltages of 12 or 24 V [50].

3. Class C

Applying boundary and midpoint D of R_{Deff} to the gain equation of class C in (51), the resulting gains are

$$A_{c0.35} = -\frac{0.35}{1-0.35} = -0.5385 \quad (63)$$

$$A_{c0.5} = -\frac{0.5}{1-0.5} = -1 \quad (64)$$

$$A_{c0.65} = -\frac{0.65}{1-0.65} = -1.8571 \quad (65)$$

For members of this class, the gain is continuous and unity (= 1) at $D = 0.5$ as shown in (64), $R_{Aeff} = [-0.5385, -1.8571]$. Their gain is unipolar and inverting and can be $\lessgtr |1|$ thus has BB capability at this R_D. The gain is continuous and operable throughout the R_D hence requiring no precautionary measure. Contrary to class A and B, they are not capable of bidirectional operation by varying D [21, 45].

Applicability: They function as inverted BBCs by supplying an ideal output voltage that is 53.85 % of the input voltage in buck mode and up to 185.71 % of the input voltage in boost mode. A major advantage of this class is that they pose no control limitation within the duty ratio range.

Applications are similar to BBC applications with added advantages of dead and overlap-time elimination that permits higher frequency application and enables usage of smaller reactive components thus reducing size, weight and cost [16].

b) Complete duty ratio range (R_{dgen})

Operations of the three classes are analysed beyond the R_{Deff} to identify other capabilities of the converters at all permissible D at the cost of reduced efficiency. Figure 9(a) shows a plot of the gains against D for R_{Dgen}.

1. Class A

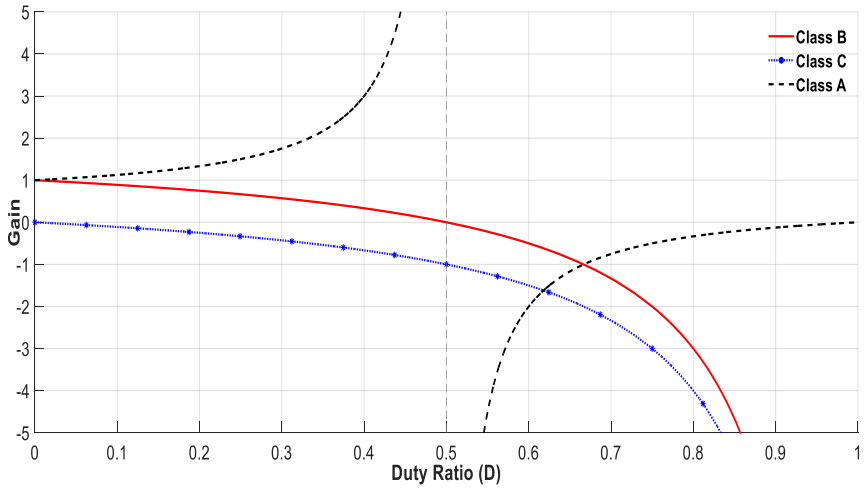
Converters in this class are better analysed by considering their discontinuous gain as two separate curves as shown in Figure 9(a). The first (upper dotted) curve covers R_D $0 \leq D < 0.5$, it's R_A is $1 \leq A_a < \infty$. The converter lacks buck capability. It functions as a non-inverting boost converter and is suitable for high boost operation. For the second curve, it covers the R_D $0.5 < D \leq 1$ and has R_A as $-\infty < A_a \leq 0$ which implies unipolar inverted BB gain. In general, this class has a bipolar boost and unipolar BB capability.

Applicability: Reference [21] found that members of class A and B are capable of bi-directional energy transfer from source to load and vice versa thus permitting four quadrant operation by using active switches (MOSFETs and their antiparallel diode) as S_1 and S_2 by only varying D without using additional components. Special control precautions should be taken to avoid operation in the discontinuous regions. Potential applications are multimode circuits involving battery, SC or/and HESS) such as [50-53] or even in simple battery-inverter, uninterruptible power supply (UPS) and other load levelling systems where the battery may be charging, discharging or on standby [21, 54-56].

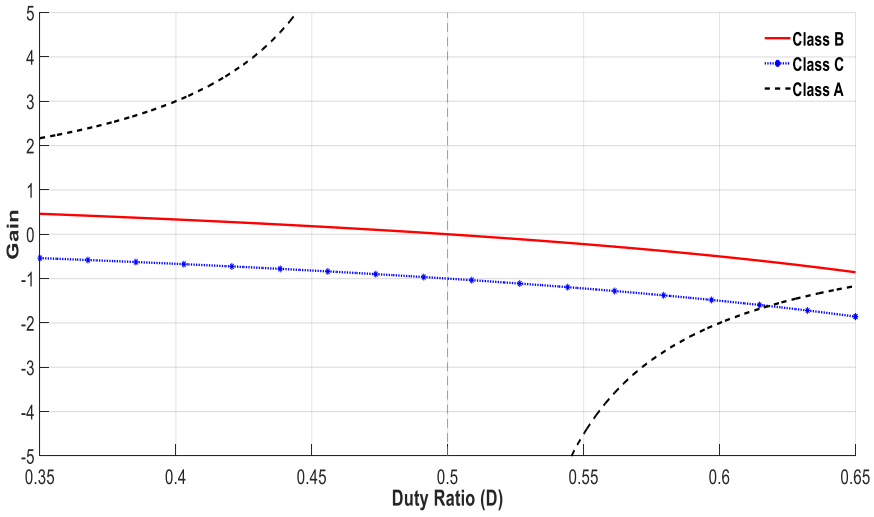
Another application is in PV distributed generation (DG) system [57] or in standalone PV system shown in Figure 10 where topology II shown in Figure 2(b) is modified by using PV output as supply with reverse blocking diode, a battery as load and replacing S_2 with an inverter bridge.

2. Class B

Topologies in this class function as non-inverting buck converter for R_D $0 \leq D < 0.5$ with R_A $1 \geq A_B > 0$ where A_B is the gain. For R_D $0.5 < D < 1$, they function as inverting BBC with $|R_A|$ as $|0 < A_B < \infty|$. This implies that this class has bipolar buck and unipolar buck-boost capability when operated over the R_D $0 \leq D < 1$ with gain $-1 \leq A_B < \infty$.



(a)



(b)

Figure 9. Plot of gain vs. duty ratio for the three classes (a) general duty ratio range (b) complete duty ratio range

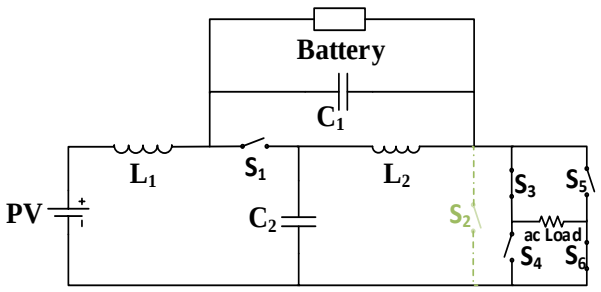


Figure 10. Class A topo. II with auxiliary H-bridge

- ***Applicability:*** They are suitable in bidirectional power transfer applications such as in HESS where ESS_1 (V_S) voltage could be above or below ESS_2 (load) voltage [58]. They are also used as inverters by varying D from $[0, 0.667]$ where the gain varies from $[1, -1]$ to give an output voltage that varies from $[V_O, -V_O]$ and the output voltage range of the inverter is the same as that of the full-bridge single-phase semi-Z-source and semi-quasi-Z-source inverters [45].

3. Class C

The gain for this class is the same as that of traditional BBC hence they have unipolar inverting BB capability when D is varied within R_D $0 < D < 1$ with gain range as $0 < A_C < \infty$. Their advantage over the two-switch and four-switch BBC is the elimination of ST and OC in the gate control signal thus permitting higher frequency operations.

- ***Applicability:*** The operation over R_{Dgen} is the general application and is similar to the efficient application because BB operation can be achieved in both applications unlike in the other classes. The major difference is that the gain is extended for the general application from $[-0.5385, -1.8571]$ to $[0, -\infty]$. Suitable application is unidirectional BB operation with wide input or output variation.

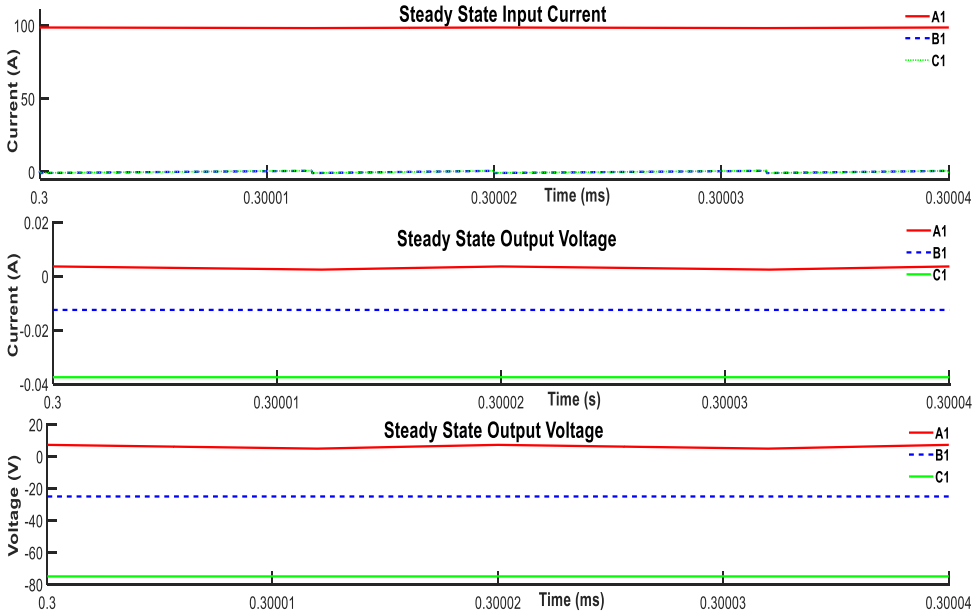
Although the number of capacitors (dual) and inductors (dual) may be thought of as disadvantage compared to traditional BBC, but BBCs with single capacitors also employ additional input capacitor [48] while the two inductors could be coupled together [11, 22, 46, 59]. Also, the capacitor and inductor requirements of ISCs are smaller due to second order filtering [9], high-frequency application permissibility also allows the use of smaller components and the non-output side components more smaller when asymmetric components are used [60].

5. VERIFICATION, RESULTS AND DISCUSSIONS

Operations of corresponding ideal symmetric converters from the three classes with parameter values given in Table 1 were simulated using MATLAB SIMULINK and compared for $D = 0.6$ and $D = 0.4$ to verify their operations. Topologies I for all the classes were used for $D = 0.6$ while topologies II were used for $D = 0.4$. Their responses are shown in Figure 11 (a) and Figure 11 (b) respectively.

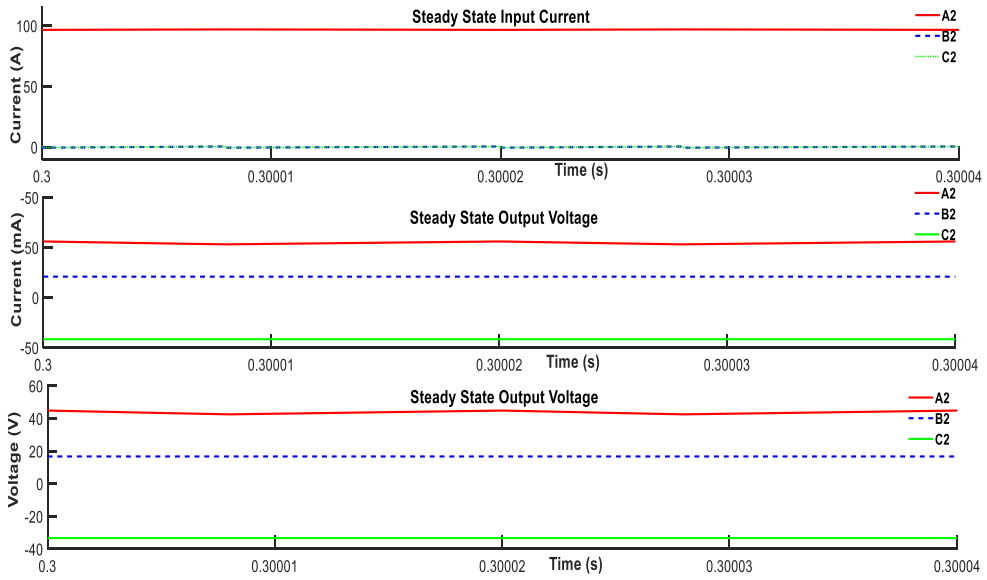
Table 1. Parameter values for the ideal symmetric q-ZSCs used

Parameter	V_g	f	R_O	C_1	C_2	L_1	L_2
Unit	V	KHz	KΩ	µF	µF	µH	µH
Value	50	50	2	500	500	400	400



(a)

Figure 11. Simulation response of the Classes at (a) D = 0.6



(b)

Figure 11. Simulation response of the Classes at (b) D = 0.4

Responses of the family shown in Figure 11 (a) and Figure 11 (b) exposes the limitations of class A caused by the discontinuity in its gain. This is because from the ideal gain (17), the output voltages of for D = 0.6 and 0.4 should be

$$V_{O(D=0.6)} = \frac{1-0.6}{1-2(0.6)} \times 50 = -100\ V \quad (66)$$

$$V_{O(D=0.4)} = \frac{1-0.4}{1-2(0.4)} \times 50 = 150\ V \quad (67)$$

These values are far away from the 7 V in the result of Figure 11 (a) and 45 V of Figure 11 (b) which are both below V_g as shown in Table 2. It signifies lack of boost capability and implies that the high boost application discussed in section IV may not be achievable.

Table 2. Comparison of ideal and simulation responses

Duty Ratio	D = 0.6			D = 0.4		
Class	A	B	C	A	B	C
Ideal	100	-25	75	150	16.7	33.3
Simulation	7	-25	75	45	16.7	33.3

Response of class B and C are in agreement with their theoretical gains as given in Table 2 thereby making them practically realizable. This also indicates that only Class C members are capable boost operation at $0.4 \leq D \leq 0.6$.

The ideal gain of each class is unique and the same for its members. Advantages and disadvantages between class members can be identified using their dynamic models [60]. Possible operating parameters should be first analysed before selecting the class to use for a given operation because each class has its pros and cons over other classes.

It is also important to note that class A and B each have one topology with common ground between input and output while the other topology has floating output. For class C, all the two topologies have floating output. Topologies with common ground have advantages over those with floating output in transformer-less applications due to leakage current [44, 45].

The higher number of capacitors and inductors shouldn't be discouraging compared to traditional DC-DC converters with single capacitor because

a. Non-impedance source DC-DC converters employ additional input capacitor [48] while the two inductors could be coupled together.
b. The capacitor and inductor requirements of ISCs are smaller due to second order filtering by the network [9].
c. High-frequency operation permissibility allows the use of smaller and asymmetric components [60].
d. Existing high gain non-impedance source DC-DC converter topologies have higher components count [46, 49].
e. Non-impedance source bidirectional DC-DC converters use additional components.
f. ISCs can also function with single capacitor [61].

6. CONCLUSION

An extended family of non-isolated DC-DC q-ZSCs with three classes has been presented. Operation of each class was analysed based on the efficient (R_{Deff}) and general duty ratio range (R_{Dgen}) to identify potential applications. Findings showed that similar to the traditional BBC, each of the topologies is capable of inverted buck-boost (BB) operation for the (R_{Dgen}).

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