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A Sub-Region Based Space Vector Modulation Scheme for Dual 2-Level Inverter System

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ABSTRACT

This paper deals the implementation of 3-level output voltage using dual 2-level inverter with control of sub-region based Space Vector Modulation (SR-SVM). Switching loss and voltage stress are the most important issues in multilevel inverters, for keep away from these problems dual inverter system executed. Using this proposed system, the conventional 3-level inverter voltage vectors and switching vectors can be located. In neutral point clamped multilevel inverter, it carries more load current fluctuations due to the DC link capacitors and it requires large capacitors. Based on the sub-region SVM used to control IGBT switches placed in the dual inverter system. The proposed system improves the output voltage with reduced harmonic content with improved dc voltage utilisation. The simulation and hardware results are verified using matlab/simulink and dsPIC microcontroller.

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1. INTRODUCTION

In recent days, multilevel inverters play an important role in industrial applications, renewable energy systems and various FACTS compensators [1]. The multilevel inverter (MLI) has many advantages like reduced harmonic level, improved output voltage, low EMI problems and output voltage nearly sinusoidal. MLI was introduced to discover the solution to improve voltage ranges of conventional semi-conductors. But the main disadvantages are capacitor balancing, CMV problem and load current fluctuations [2]. Generally for high power applications low switching frequency is prepared to avoid the switching losses in the system. The main drawback in NPCI is dc voltage fluctuations and voltage stress in each switching devices.

Many PWM methodologies are implemented to control the power switches place in the multilevel inverters [3]. Based on the PWM method the output voltage of the particular system can be increased. While using multilevel inverters, the number of switches placed in a leg increases due to increasing the level. So that switching pulse generation becomes more complicated, when number of switches increases in a leg. The system [4] used NPC multilevel inverters to reduce the harmonic level and reduce the capacitor balancing problems. The number of switches used in the both 2-level dual inverters is same as in the corresponding 3-level inverter. And the additional diodes used in the NPC inverter is not needed in the VSI inverter, so it saving the number of components used in the system [5]. Also the NPC inverter has problem of capacitor balancing, but it does not exist in the two level VSI inverter. The implementation cost of the system also reduced, when compared to other conventional multilevel inverters. The main advantage of grid connected topology is greatly enhanced fault acceptance, in case any collapse in one inverter system it can discontinue

and the operation can preserve using other inverter system. When the number of levels in the inverter increases, the dc link capacitor voltage balancing becomes extra demanding [6], [7].

Amongst various PWM methods for a multilevel inverter, SVM is suitable due to various advantages like it directly control system, identifies the voltage and switching vectors and co-ordinates transformation. The space vector diagram for any level inverter contains six sectors [8], [9]. Each sector contains number of triangles and sub regions. The reference can be placed in any of the sub-region or triangles, based on the actual and reference voltages. Based on this SVM the switching time calculation and switching vector identification can be done [10].

This proposed system explains, sub-region-based Space Vector Modulation (SR-SVM) scheme for dual 2-level inverter system. The SR-SVM is implemented to control the two-level dual inverter system based on conventional two space vector modulation. The output voltage and reduced voltage stress of the proposed system can be improved based on the reference voltage variation with sub-region concept. By using dual 2-level inverter, which minimises the load current fluctuations, switching loss and reduces the total harmonic content in the system. The simulation and hardware results are verified using matlab/simulink and dsPIC microcontroller.

2. TWO LEVEL DUAL INVERTER SYSTEM

The two-level dual inverter fed grid system shown in Figure 1. The two-level dual inverter consists of separate dc sources and each VSI inverter consists of six power switches and coupled with grid system through the coupled inductor. So, each inverter can generate its voltage vector locations and its switching time period [11]. So, each 2-level inverter can operate in 8 switching states, which consists of active and zero vectors. By using 2-level dual inverter, the voltage stress, switching losses and no need of any dc link capacitors which avoids the capacitor balancing problem [12].

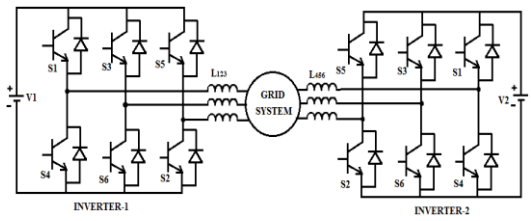


Figure 1. Two level dual inverter fed grid system

The 2-level VSI inverter can operated in 8 switching states and by connecting the two VSI inverters, which get totally 27 switching states. The minimised dc link voltage with 60% is adequate to attain the various voltage levels as that of 3-level NPC inverter, which contains 27 switching states [13]. Based on sub-region space vector concept the gate pulse generation can be achieved to control the dual two-level inverter. There is no dc link connection in 2-level VSI inverter, which won't produce load current fluctuations and capacitor balanced problem [14].

The output of two-level dual inverter is connected to grid system through coupled inductor, which avoids the usage of transformer and used to synchronise with grid system, by converting stepped wave into sinusoidal waveform [15]. The switching vectors of inverter 1 varies from a to h and the switching vectors of inverter 2 varies from A to H. During the inverter 1 and inverter 2 operations, the switches turned ON record is shown in Table 1.

Table 1. Switching vectors of individual inverter

Two level inverter-1		Two level inverter-2	
Switching Vectors	Switches Turned ON	Switching Vectors	Switches Turned ON
a (P P P)	S1, S3, S5	A' (P P P)	S1, S3, S5
b (P P N)	S1, S3, S2	B' (P P N)	S1, S3, S2
c (P N P)	S1, S6, S5	C' (P N P)	S1, S6, S5
d (P N N)	S1, S6, S2	D' (P N N)	S1, S6, S2
e (N P P)	S4, S3, S5	E' (N P P)	S4, S3, S5
f (N P N)	S4, S3, S2	F' (N P N)	S4, S3, S2
g (N N P)	S4, S6, S5	G' (N N P)	S4, S6, S5
h (N N N)	S4, S6, S2	H' (N N N)	S4, S6, S2

The value of coupled inductor can be designed based on the output voltage variation of inverters and grid voltage [16]. For example, the switching vector b (P P N) explains the switches turned ON, S1 in leg 1, S3 in leg 2 and S2 in leg 3. Based on these switching vectors the output voltage of the 2 level VSI inverter can be decided. For attainment of improved 3-level voltage output, sub-region SVM concept implemented, which consists all the 27 switching like present in the conventional 3-level NPC inverter. The three-phase output voltage received from the dual inverter Vao, Vbo & Vco represented in the following equations,

$$V_{a0} = V_{a1} - V_{a2}^{1} \quad (1)$$

$$V_{b0} = V_{b1} - V_{b2}^{1} \quad (2)$$

$$V_{c0} = V_{c1} - V_{c2}^{1} \quad (3)$$

Where Va1, Vb1, Vc1 are three phase output voltages of inverter 1 and Va2', Vb2', Vc2' are three phase output voltages of inverter 2. The total output voltage received from the dual inverter synchronised with grid system using coupled inductor.

3. MODES OF OPERATION

The modes of operation of dual inverter fed grid system can be operated as holding mode and switching mode. During the operation of dual inverter, we can get 27 possible switching operations which are controlled by generating the gating pulses for dual VSI inverter using SR-SVM method. In SR-SVM method, the required switching conditions can be obtained by varying the sub-regions from 1 to 7 based on the reference voltage value. The following selected modes explains the operation of dual inverters fed grid system,

Mode 1: to obtain the 3-level output voltage of Vdc, the inverter 1 switches S1, S3 & S5 are turned ON with voltage of Vdc/2 and the inverter 2 switches S2, S4 & S6 are turned ON with voltage of –Vdc/2, which is shown in Figure 2(a).

Output voltage in mode 1, $V_o = \frac{V_{dc}}{2} - \left(\frac{-V_{dc}}{2}\right) = V_{dc}$ (4)

Mode 2: to attain the 3-level output voltage of 0, the inverter 1 switches S1, S3 & S5 are turned ON with voltage of Vdc/2 and the inverter 2 switches S1, S3 & S5 are turned ON with voltage of Vdc/2, which is shown in Figure 2(b).

Output voltage in mode 2, $V_o = \frac{V_{dc}}{2} - \left(\frac{V_{dc}}{2}\right) = 0$ (5)

Mode 1: to acquire the 3-level output voltage of -Vdc, the inverter 1 switches S2, S4 & S6 are turned ON with voltage of -Vdc/2 and the inverter 2 switches S1, S3 & S5 are turned ON with voltage of Vdc/2, which is shown in Figure 2(c).

Output voltage in mode 3, $V_o = \frac{-V_{dc}}{2} - \left(\frac{V_{dc}}{2}\right) = -V_{dc}$ (6)

Mode 1: to achieve the 3-level output voltage of 0, the inverter 1 switches S2, S4 & S6 are turned ON with voltage of -Vdc/2 and the inverter 2 switches S2, S4 & S6 are turned ON with voltage of –Vdc/2, which is shown in Figure 2(d).

Output voltage in mode 1, $V_o = \frac{-V_{dc}}{2} - \left(\frac{-V_{dc}}{2}\right) = 0$ (7)

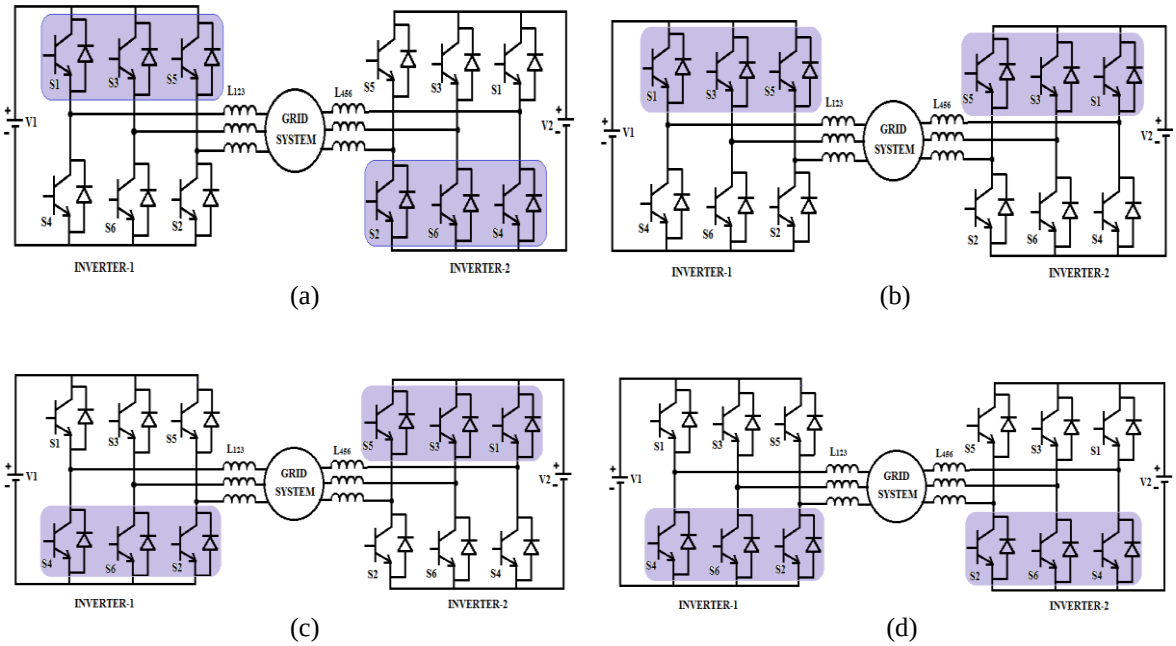


Figure 2. Various switching states of dual inverter (a) pair a-H' (b) a-A' (c) h-A' (d) h-H'

Similarly, the dual inverter can be operated in 27 switching modes to attain the three-level output voltage from the 2 level VSI system. Table 2 shows the range of dual inverter output voltages for various mode of operation.

Table 2. Range of dual inverter output voltages

Output voltage Inverter 1 (V_{01})	Output voltage Inverter 2 (V_{02})	Output voltage dual inverter (Vo)
$\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	V_{dc}
$\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	0
$-\frac{V_{dc}}{2}$	$\frac{V_{dc}}{2}$	V_{dc}
$-\frac{V_{dc}}{2}$	$-\frac{V_{dc}}{2}$	0

4. SUB-REGION SPACE VECTOR MODULATION (SR-SVM)

A sub-region based space vector modulation scheme implemented to generate switching pulses for dual two level inverter. Based on the holding and switching concept both inverters operated without any crossover distortion problem. During the reference vector tracking the inverter 1 is switched while inverter 2 is in holding condition and vice versa. The space vector hexagon model for 3-level inverter is shown in Figure 3. In that to identify the reference vector location the sub region concept implemented.

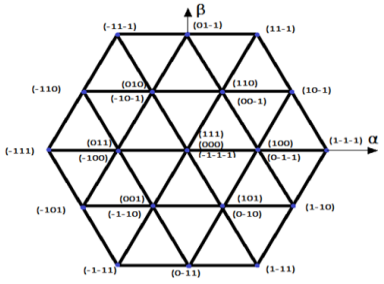


Figure 3. Space vector hexagon model for 3-level inverter

In conventional SVM method, the reference calculation and switching time calculation is done by using sector and triangle identification. But in this proposed method, first inverter operating modes and conditions (switching mode & holding mode) are decided and generation of gating pulses. The dual VSI inverter operating modes are shown in Table 3.

Table 3. Inverter operation modes to find the reference vector

Cycles	2-level inverter	Sub region-1	Sub region-2	Sub region-3	Sub region-4	Sub region-5	Sub region-6
First cycle	Inverter 1	Holding to d (P N N)	Switching pulse	Holding to f (N P N)	Switching pulse	Holding to g (N N P)	Switching pulse
	Inverter 2	Switching pulse	Holding to f (N P N)	Switching pulse	Holding to g (N N P)	Switching pulse	Holding to d (P N N)
Second cycle	Inverter 1	Switching pulse	Holding to b (P P N)	Switching pulse	Holding to c (P N P)	Switching pulse	Holding to e (N P P)
	Inverter 2	Holding to c (P N P)	Switching pulse	Holding to e (N P P)	Switching pulse	Holding to b (P P N)	Switching pulse

For example in the first cycle of SVM operation, under sub region 1 the inverter 1 is in holding mode d(P N N) (fixed switching pulse) and inverter 2 is in switching mode (which generates gate pulses for inverter 2) and the reference voltage vector point N is tracked by through sub region 1 origin, it means the point N is tracked by from OA and AN instead tracking from O to N directly, which avoids complexity in control algorithm is shown in Figure 4(a). In sub-region 1 contains the switching vector possibilities are (111), (000), (-1-1-1), (110), (00-1), (100), (0-1-1), (10-1), (11-1), (01-1), (010), among these states the exact reference point can be tracked using switching and holding condition.

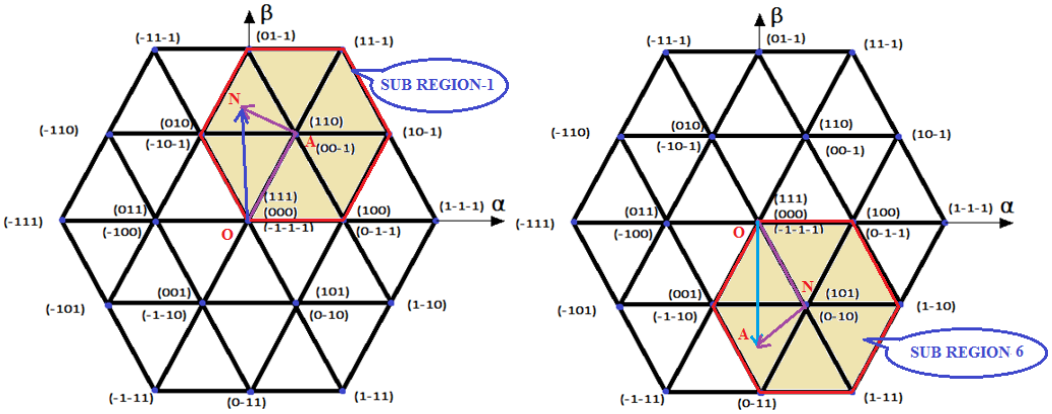


Figure 4. SR-SVM hexagon model (a) sub region 1 (b) sub region 6

Similarly in Figure 4(b) shows the sub region 6 contains the inverter 2 is in holding mode d(P N N) (fixed switching pulse applied, switches S1, S4, S6 are kept ON condition) and inverter 1 is in switching mode (which generates gate pulses for inverter 1 based on 2level inverter concept) and the reference voltage vector point N is tracked by through sub region 6 origin, it means the point N is tracked by from OA and AN instead tracking from O to N directly, which avoids complexity and switching losses in the system. However the 2 level dual inverter can operate in 6 sub regions to avoid the complexity in SVM method. In sub-region 6 contains the switching vector possibilities are (111), (000), (-1-1-1), (101), (0-10), (0-11), (001), (1-10), (100), (0-1-1). The switching losses and conduction losses in a power electronic switching devices are essentially due to switching speed and switching frequency. By using this holding and switching method to generate the pulses for the dual inverter, which avoids losses and voltage stress in the system also reduced. The power loss in the power electronic switches is identified in terms of heat indulgence. In this proposed system 2level dual inverters are applied to recognize the 3level output using SR-SVM method. In two level inverter each phase (leg) contains 2 switches, which is capable of bidirectional current flow and it avoids the dc link load current fluctuations of the proposed system.

5. SIMULATION RESULTS AND DISCUSSION

The work accessible here mainly focus on generation of 3-level output voltage with the help of 2-level dual inverter instead of using multilevel inverter, which minimises the switching loss, voltage stress and avoids capacitor balancing problem and which is simulated using matlab/simulimk 11b. The proposed system which employs the switching frequency of 10 kHz. The simulation parameters are applied dc input voltage to 2level VSI inverter is 150V on both sides, the coupled inductor value of 4mH for all three phases and grid system voltage of 300V. The switching pulse generation for the VSI inverter-2 is shown in Figure 5. And in Figure 6 and 7 shows the stepped output voltage waveform of two level VSI inverter-1 and inverter-2 with voltage of 133.5V.

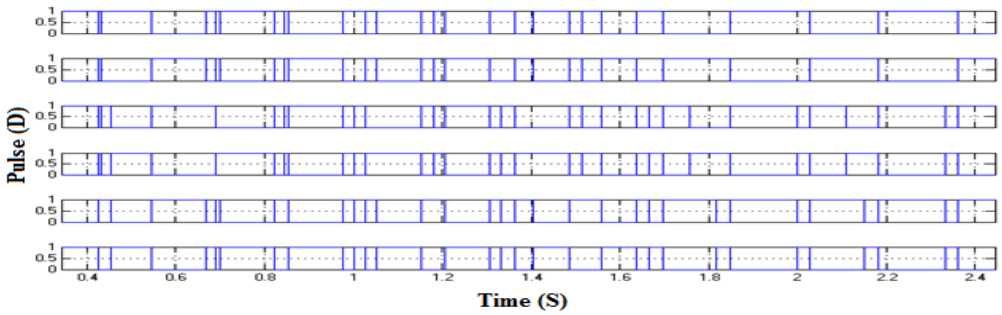


Figure 5. Switching pulse generation for inverter-2

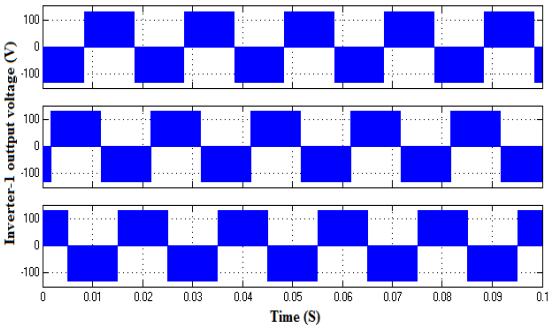


Figure 6. Output voltage of two level inverter-1

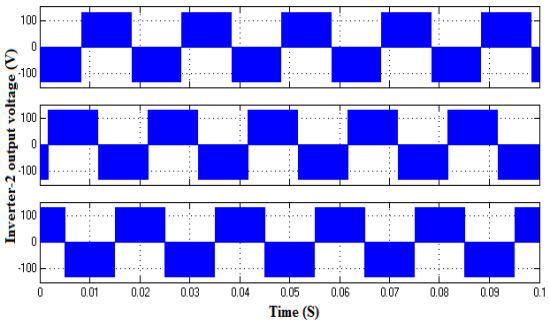


Figure 7. Output voltage of two level inverter-2

3-level steeped output voltage waveform generated using 2-level dual inverter instead of various topologies of multilevel inverter, which is shown in Figure 8 with voltage value of 267.5V. In Figure 9 shows sinusoidal output voltage of 267.5V, which is converted from inverter stepped voltage with help of coupled inductor. Here coupled inductor avoids the usage of transformer, leakage current problems and reduces the cost of the proposed system.

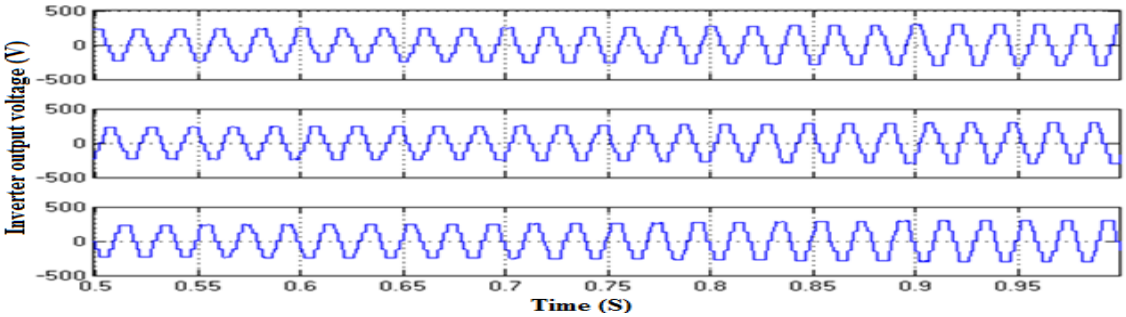


Figure 8. Three level voltage waveform using 2-level dual inverter

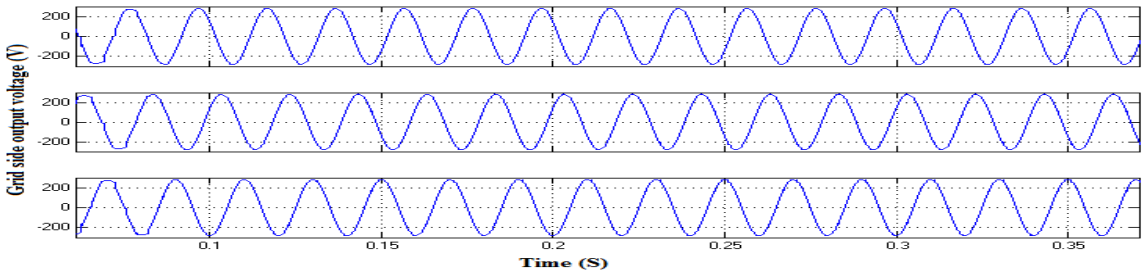


Figure 9. The output voltage waveform for grid system

In Figure 10 shows the controlled output current waveform for the proposed dual inverter system with 5.08A, which better current control compare to other conventional system. And based on SR-SVM method with holding and switching modes used to control dual inverter system, the control signal generation for SR-SVM method is shown in Figure 11and Figure 12 shows the harmonic spectrum analysis of inverter output voltage and inverter current with 1.40% & 2.89% respectively.

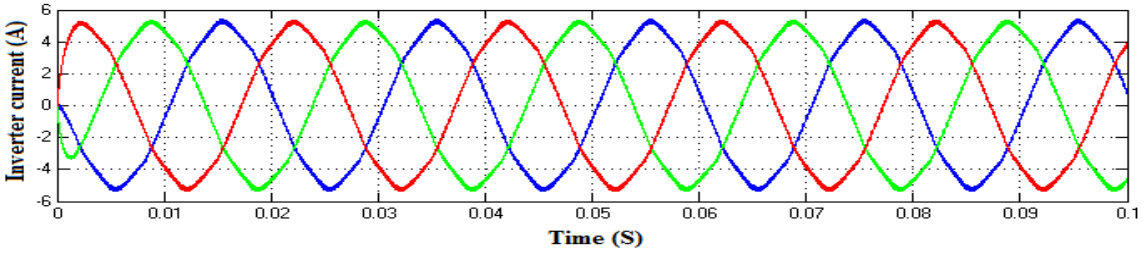


Figure 10. Controlled output current waveform of inverter

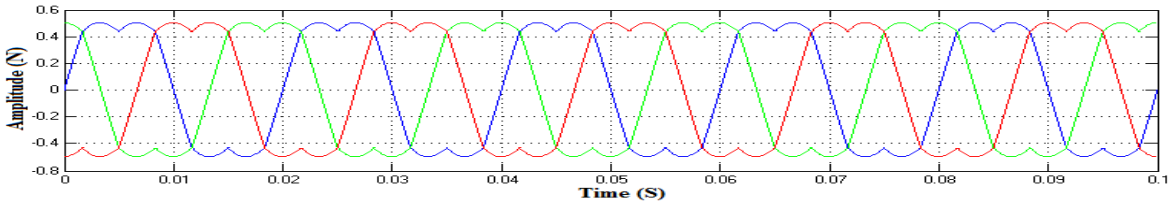
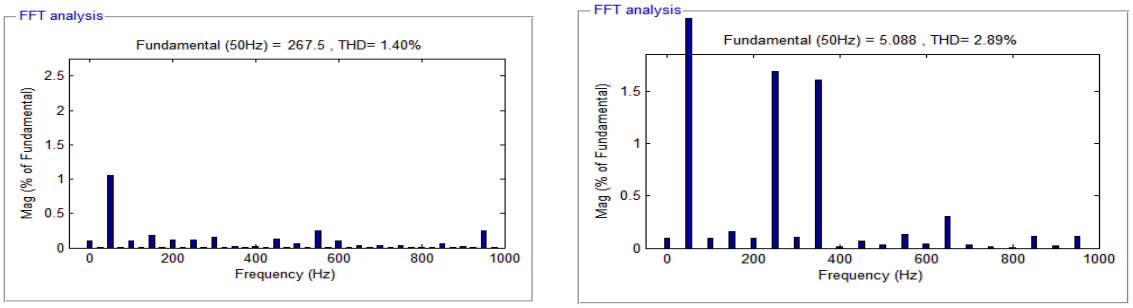


Figure 11. Control signals representation of SR-SVM



(a) (b)

Figure 12. Harmonic analysis (a) inverter voltage (b) inverter current

6. EXPERIMENTAL RESULTS AND DISCUSSION

A Sub-region based Space Vector Modulation scheme for dual 2-level inverter system was implemented using dsPIC micro controller. In this proposed system verified using 3 phase induction motor as load instead grid system. The power converter switches are premeditated for 4KVA operating drive. IGBTs used for the 2 level dual inverter power switches and coupled inductor value are 4mH. The current and voltage value are measured with help of quadrature encoder sensor. In Figure 13 shows the block diagram hardware implementation control strategy. And gating pulse generation for dual VSI inverter switch is shown in Figure 14.

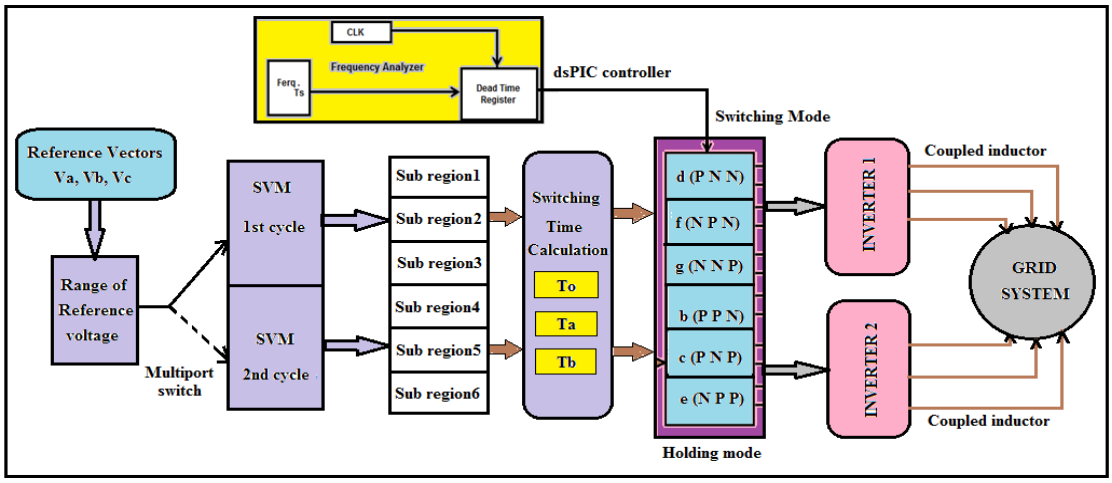


Figure 13. Hardware implementation control methodology

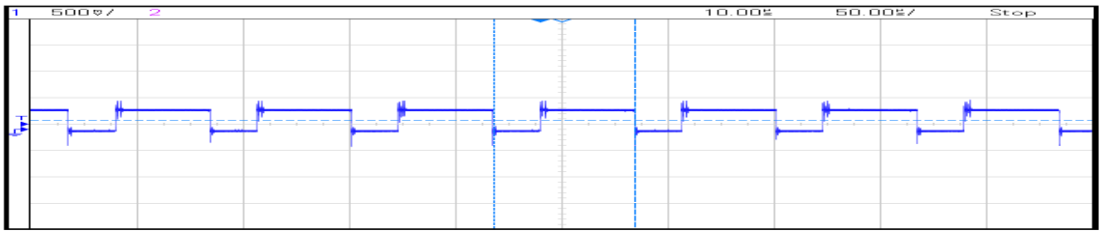


Figure 14. Firing pulse generation for inverter-1

In Figure 15 shows the output voltage waveform for inverter-1 with voltage of 120V. And Figure 16 shows coupled inductor output current for the proposed system, which used to synchronise the inverter with grid system. The three-level output voltage from the proposed system achieved by using 2-level dual inverter topology is shown in Figure 17. In Figure 18 shows the sinusoidal output voltage after the coupled inductor, which is mainly used to avoid the leakage current problem and reduces the harmonic content in the system. In Figure 19 switching frequency-inductance variation with SR-SVM and conventional SVM.

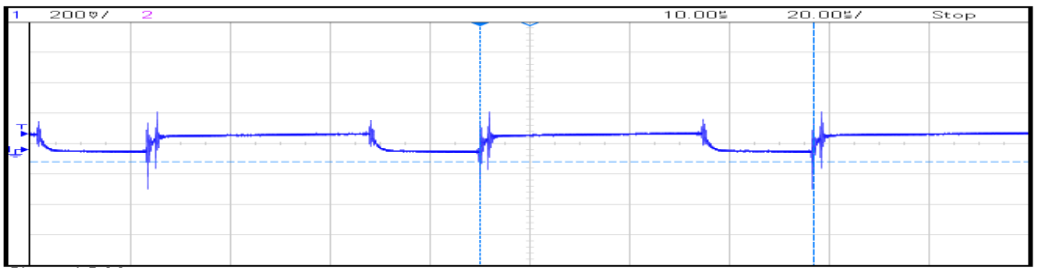


Figure 15. Output voltage waveform for inverter-1

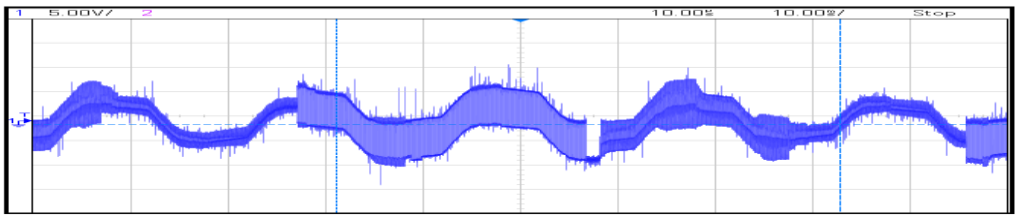


Figure 16. Coupled inductor output current

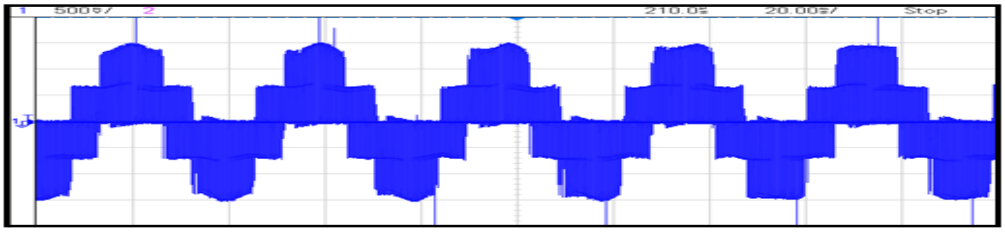


Figure 17. Three level output voltage using 2-level dual inverter

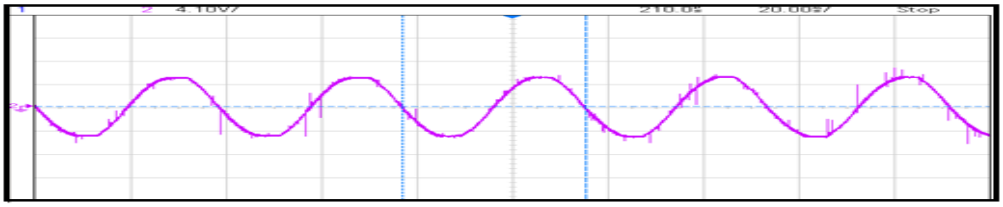


Figure 18. Sinusoidal output voltage after the coupled inductor

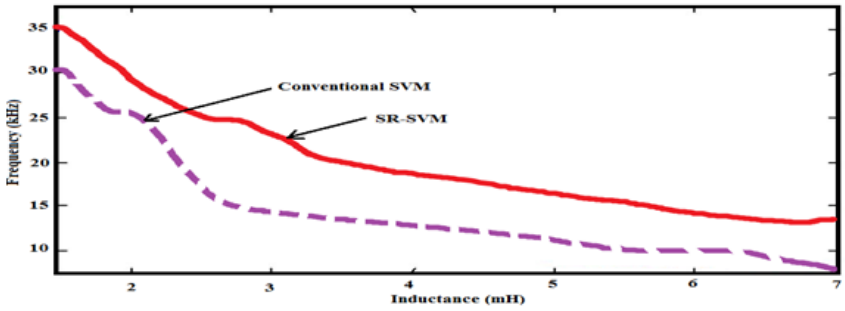


Figure 19. Switching frequency-inductance variation with SR-SVM and conventional SVM

7. CONCLUSION

This work has presented the 3-level output voltage using dual 2-level inverter with control of sub-region based Space Vector Modulation (SR-SVM). From that switching loss and voltage stress in the circuit has been avoided, the harmonic content in the system is minimised compare to conventional 3level voltage system. Dual 2level inverter system used as an alternative of multilevel inverter, where the complicity of the control algorithm minimized. SR-SVM used as a pulse generation method for the proposed circuit, which is worked based on 1st and 2nd cycle operation of SVM with help of holding and switching concept. Based on this method the tracking of reference vector become more simple and easy to design. The proposed system has the main features are 1) voltage stress and switching loss in the system minimised. The harmonic content for inverter output voltage and inverter current with 1.40% & 2.89% respectively, which is less than the IEEE standard; 2) Coupled inductor which avoids the usage of transformer and well suitable to synchronise inverter with any ac systems.

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