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Identifying worst case test vectors for FPGA exposed to total ionization dose using design for testability techniques

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IDENTIFYING WORST CASE TEST VECTORS FOR FPGA EXPOSED TO TOTAL IONIZATION DOSE USING DESIGN FOR TESTABILITY TECHNIQUES

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To my father & mother

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ABSTRACT

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TID testing

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Electronic devices often operate in harsh environments which contain a variation of radiation sources. Radiation may cause different kinds of damage to proper operation of the devices. Their sources can be found in terrestrial environments, or in extra-terrestrial environments like in space, or in man-made radiation sources like nuclear reactors, biomedical devices and high energy particles physics experiments equipment. Depending on the operation environment of the device, the radiation resultant effect manifests in several forms like total ionizing dose effect (TID), or single event effects (SEEs) such as single event upset (SEU), single event gate rupture (SEGR), and single event latch up (SEL).

TID effect causes an increase in the delay and the leakage current of CMOS circuits which may damage the proper operation of the integrated circuit. To ensure proper operation of these devices under radiation, thorough testing must be made especially in critical applications like space and military applications. Although the standard which describes the procedure for testing electronic devices under radiation emphasizes the use of worst case test vectors (WCTVs), they are never used in radiation testing due to the difficulty of generating these vectors for circuits under test.

For decades, design for testability (DFT) has been the best choice for test engineers to test digital circuits in industry. It has become a very mature technology that can be relied on. DFT is usually used with automatic test patterns generation (ATPG) software to generate test vectors to test application specific integrated circuits (ASICs), especially with sequential circuits, against faults like stuck at faults and path delay faults. Surprisingly, however, radiation testing has not yet made use of this reliable technology.

In this thesis, a novel methodology is proposed to extend the usage of DFT to generate WCTVs for delay failure in Flash based field programmable gate arrays (FPGAs) exposed to total ionizing dose (TID). The methodology is validated using MicroSemi ProASIC3 FPGA and cobalt 60 facility.

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LIST OF ABBREVATIONS

ASIC	Application Specific Integrated Circuits
ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
BIST	Built-In Self-Test
CMOS	Complementary Metal Oxide Semiconductor
CUT	Circuit Under Test
DFT	Design For Testability
EDA	Electronic Design Automation
FG	Floating Gate
FPGA	Field Programmable Gate Arrays
IC	Integrated Circuit
LFSR	Linear Feedback Shift Register
LSSD	Level Sensitive Scan Design
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Filed Effect Transistor
ORA	Output Response Analyzer
RILC	Radiation Induced Leakage Current
RTL	Register Transfer Level
SEE	Single Event Effect
SEGR	Single Event Gate Rupture
SEL	Single Event Latch up
SEU	Single Event Upset
SRAM	Static Random Access Memory
SRL	Shift Register Latch
SSI	Small Scale Integration
STA	Static Timing Analysis
STI	Shallow Trench Isolation
TID	Total Ionizing Dose
TPG	Test Pattern Generator
VLSI	Very Large Scale Integration
WCTV	Worst-Case Test Vector

Chapter 1

Summary

Electronic devices may be exposed to several sources of ionizing radiation. The radiation sources can be found in terrestrial, extra-terrestrial and man-made radiation environments. In terrestrial environment, the sources can be neutrons found in the atmosphere, or alpha particles emitted from defects inside chip's materials. In extra-terrestrial environment, such as space the sources can be trapped particles around the Earth's atmosphere, particles originating from the sun, or high energy galactic cosmic rays' particles. The man-made radiation environments include nuclear reactors, biomedical devices, and high energy particles physics experiments equipment.

The radiation sources can cause several forms of damage to the correct operation of electronic devices under radiation. Depending on the radiation source and the environment which the device operates in, several radiation resultant effects can occur. The resultant effects can cause permanent or temporary failures in the device exposed to radiation. These effects can manifest in the form of single-event effects such as single-event upset, single-event gate rupture, and single-event latch-up, or total ionizing dose effect.

For the proper design of electronic devices exposed to radiation sources, a standard test procedure must be applied to ensure proper operation of devices under radiation. MIL-STD-883, method 1019 i.e. the standard test procedure to test electronic devices under radiation emphasizes the use of worst-case test vectors (WCTVs) in the testing procedure. However, worst-case test vectors are not used in radiation testing due to the difficulty in generating such vectors for complex circuits.

Several efforts have been made to identify worst-case test vectors for ASICs [1]-[6], however, there has been no effort to identify worst-case test vectors for FPGA except [7]. This effort only works on combinational circuits or sequential circuits characterized by the presence of flip-flops at the primary inputs and outputs of the circuit. However, these conditions are very rare as most designs are composed from

complex sequential circuits. The problem of testing sequential circuits is their lack of controllability and observability in the internal registers.

Design for testability (DFT) has been proposed since decades to overcome this problem by replacing the normal registers in a design by scan cells. This will result in an increase of the controllability and observability of the internal registers. However, DFT techniques were only used for ASIC, hence FPGA macro libraries do not include scan cells as DFT was not meant for FPGA designs.

In this thesis, a novel methodology is proposed to generate WCTV for flash-based FPGA exposed to total-ionizing-dose effect. Also, two techniques are proposed to test FPGA designs using the generated WCTV. The first technique depends on altering the normal FPGA design flow to include scan cells which are not found in the FPGA macro libraries. The second technique depends on the reprogram ability of FPGA to make the off-inputs along the target path to be test have non-controlling value to propagate a transition along the path without being masked.

The methodology is validated by implementing different design using Microsemi ProASIC3 A3P125-208PQFP flash-based FPGAs and total dose using Cobalt 60 radiation facility. The experimental results show the significance of using WCTV in total-dose testing of FPGA devices.

The rest of the thesis is organized as follows. Chapter two includes a review on different radiation sources and effects. Chapter three focuses in the TID effect on CMOS circuits and floating gate MOS transistor which are the switch elements in flash-based FPGA. Chapter four introduces a review on DFT basics and path delay testing. Chapter five discusses the previously developed efforts to generate WCTV of ASICs and FPGAs. Chapter six introduces the novel proposed methodology to identify WCTV for sequential circuits in flash-based FPGA using DFT techniques. Chapter seven contains the experimental results done to validate the proposed methodology. Finally, the thesis ends by chapter eight which concludes the work done in this thesis and gives some outlines of future work that may be done.

Chapter 2

Radiation effects review

Electronic devices often operate in harsh environments which contain a variety of radiation sources. These radiation sources may cause different kinds of damage to the proper operation of the devices. Their sources can be found in terrestrial environments due to neutrons which are found in the atmosphere, or alpha particles which are emitted from defects found inside chips materials. They are also found in extra-terrestrial environments like space due to trapped particles around the Earth's atmosphere, particles which originated from the sun and high energy galactic cosmic rays' particles. Also, there are sources of radiation which originated from artificial man-made radiation found in nuclear reactors, biomedical devices and high energy particles physics experiments equipment.

The basic concept of ionizing radiation is that it transfers an amount of energy to the material exposed to its source. This deposited energy can cause a variation of effects in electronic devices such as faults in memory bits, increase in leakage current and increase in delay which can cause a total functional failure of the device.

2.1 Radiation sources

Since electronic devices are widely used in many environments including terrestrial, extra-terrestrial and man-made artificial radiation environments, an analysis of their characteristics is needed in order for these devices to operate properly in this environment.

2.1.1 Terrestrial environment

Neutrons found in Earth's atmosphere and alpha particles emitted from defects inside integrated circuit (IC) material are the most important sources of radiation in the terrestrial environment.

Atmospheric neutrons originate from the interaction between the galactic cosmic rays and the outer layers of Earth's atmosphere. Although they are not charged,

they can transmit energy to the target materials as they are able to trigger some nuclear reactions. As cosmic rays enter the Earth's atmosphere, they interact with oxygen and nitrogen and generate particles including protons, muons, neutrons and pions. The number of originated particles first increases and then decreases as the cosmic rays enter the atmosphere. This is because the atmosphere shielding dominates over the multiplication effect. As shown in Figure 1, the atmospheric neutron flux increases with altitude and reaches a peak value at approximately 15 Km. That is the altitude in which avionics operate, and this is why avionics electronic devices are most threatened by neutrons [8].

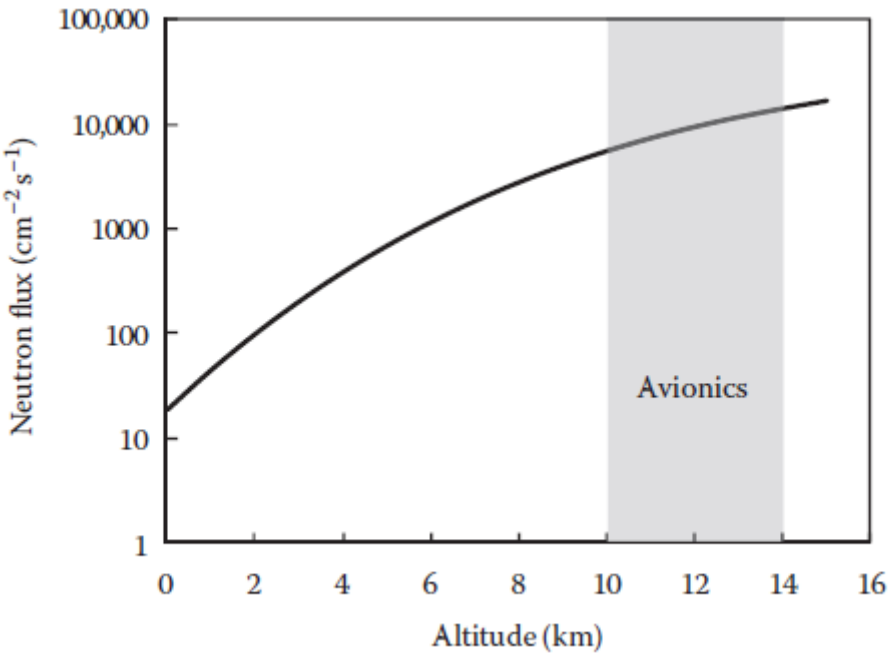

Figure 1: Flux of neutrons in the terrestrial environment as a function of altitude [8].

Another source of radiation are the alpha particles which are emitted as a result of the radioactive decay of defects inside chip material. Elements such as Uranium, Thorium, Platinum and Hafnium, which are used intentionally in the fabrication of Integrated Circuits (IC) or can be unwanted defects in the chip material, are the source of alpha particles. These elements or defects are the most responsible source for soft errors occurring in electronic devices. As the technology advances and the feature size of IC decreases, the soft errors induced by alpha particles are becoming more important than those induced by atmospheric neutrons. Also, particles like muons are gaining

more attention as they can cause threats to Complementary Metal Oxide Semiconductor (CMOS) circuits with the continuous decrease in the device dimensions [9].

2.1.2 Space

Space is one the harshest environments that electronic devices can operate in, and it is also one of the most complex environments as it contains all kinds of natural nuclei, from protons to Uranium. As shown in Figure 2, the three main sources of these particles are:

1. High energy galactic cosmic rays.
2. Solar particle events
3. Particles trapped in the magnetospheres of other planets

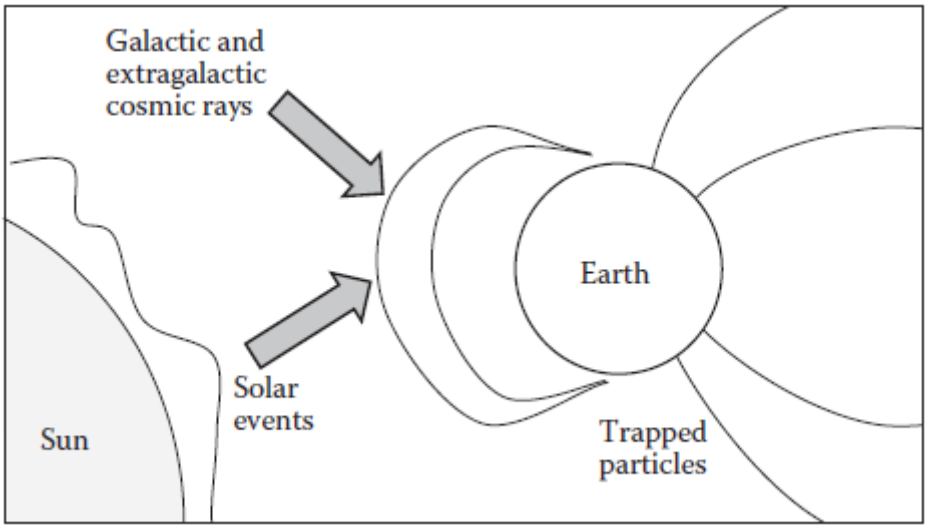

Figure 2: Schematic illustration of three main sources of radiation in space [8].

Galactic Cosmic Rays (GCRs) have a spectrum that extend to very high energies. As the name suggests, GCRs come from outside the solar system, although their source and acceleration method are not yet completely clear. They have probably been accelerated to the speed of light for millions of years and have travelled many times across the galaxy. For the most part they are made of protons, but they can include all kinds of elements. Their energy can reach a very high level, up to 10^{11} GeV, which makes them very penetrating and impossible to shield with reasonable amounts of materials. Some of the GCRs interact and emit gamma rays, and that is how we can know that they have passed through the galaxy.

The sun is the second source of space ionizing particles. Their energies can reach values greater than 10 MeV, and their fluxes depend on the solar activity cycle. Solar activity is cyclic, which changes its value from high activity every 7 years and low activity every 4 years. Two events occur in the solar activity cycle. The first is solar particle events, which consist of solar flares and coronal mass ejections, and the second one is loss of mass in the sun, which causes some protons and electrons to escape the sun's gravity and acquire high energy. These protons and electrons have a magnetic field which in turn can interact with planetary magnetic fields.

Earth's magnetospheres are objects which originated from the interaction between the magnetic field of the solar wind and the Earth's own magnetic field, which has two components, an intrinsic one and an external one from the solar wind. The Earth's magnetic field forms a natural barrier against high energy solar wind flow. With the interaction between the solar flares and the solar wind with the Earth's magnetic field, some electrons are trapped inside the Earth's magnetosphere. Due to the interaction between the galactic cosmic rays and Earth's magnetic field, some protons are trapped in the magnetosphere of Earth. These particles which have energies up to 5 MeV and 800 MeV, once trapped inside Earth's magnetosphere move in spiral lines bouncing from one pole to another. Also, these particles form a radiation belt around the Earth called the Van Allen radiation belt. It consists of two belts; the outer belt which is made for the most part of electrons which have an energy up to 10 MeV, and an inner belt which is made of both electrons and protons and has protons with energy of about 100 MeV and electrons with energy in the range of hundreds of KeV.

Due to the complexity of the space environment, it is very difficult to assess the amount of ionizing radiation hitting a system in space, and it is also dependent on the cycle of solar activity. Furthermore, the exact amount of radiation that affects a specific electronic device depends on its location inside the spacecraft or satellite that is operating in due to the shielding effect of the materials used. In a context like space, one cannot just overdesign the electronic systems because the addition of this weight when applied to spacecraft or satellites has a high cost. Furthermore, these devices lack the power to support overdesigned electronic systems. This is why complex simulation

tools and models are used to predict the dose affecting the devices and design them within the appropriate margins[8]

2.1.3 Man-made radiation

Another source of ionizing radiation can be artificially man-made, such as biomedical devices and high energy particles physics experiment equipment. In fact, doses that may exceed 100 Mrad(Si) are expected in the planned upgrade of the Large Hadron Collider (LHC) at CERN in Switzerland. To be able to compare this value, most missions in space by the National Aeronautics and Space Administration (NASA) expect a dose of less than 100 Krad(Si). That is why the design of devices in this equipment is characterized by the use of dedicated rad-hard libraries which have a layout that is made specially to avoid the problems of standard design and ultimately to withstand the high levels of radiation found in these environments.

Nuclear power plants are another source of man-made radiation. For example a fusion reactor like the one found in ITER neutral beam test facility, electronic devices are expected to be hit by large fluxes of neutrons of energies up to 14 MeV, the doses expected in the ITER environment can reach a value of 50 rad(Si) in one operating hour [10].

2.2 Radiation effects mechanisms

To analyze and design electronic devices to operate in radiation environments, one must study the radiation effect mechanism on the target material. Figure 3 shows one of these mechanisms, which occurs when a charged particle comes close to an atom. Due to the Coulomb force associated with the secondary particle, some electrons from the target atom get extracted, which in turn produces electron-hole pairs. In the case where the target material is metal, due to the high mobility of electrons and holes and because there is no band gap, the electrons and holes recombine immediately without causing any observable radiation effect. For dielectric materials like SiO_2, depending on the applied electric field, an accumulation of holes in the dielectric can occur which may result in parasitic energy levels inside or on the surface of the oxide, resulting in the Total Ionization Dose (TID) effects as shown in Figure 4 [11].

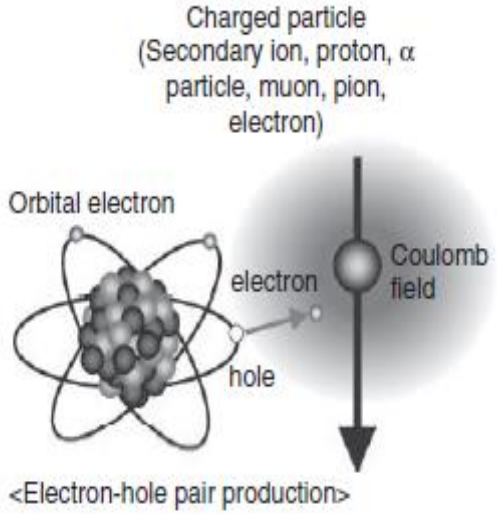

Figure 3: Coulomb interaction between charged particle and an atom [11]

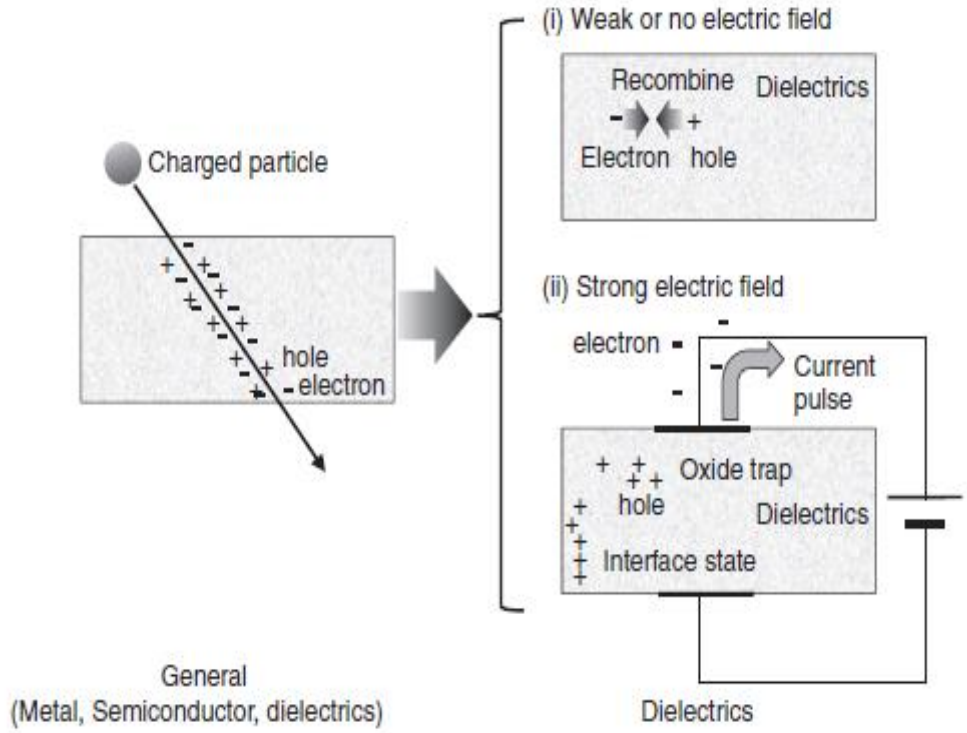

Figure 4: Physical phenomena in general solid and dielectric induced by high energy charged particle[11]

Another radiation effect mechanism is illustrated in Figure 5. The radiation effect starts with the displacement of lattice atoms in the target material due to the collision of particles including photons and neutrons. This displacement can cause dislocation loops and interstitials, which in turn results in some changes in the characteristics of the target material [11].

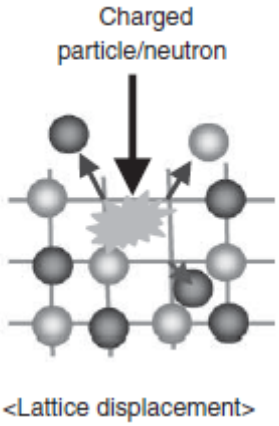

Figure 5: Lattice displacement due to radiation effect [11].

2.3 Radiation resultant effect

The resultant effect of the radiation mechanisms mentioned before depends on the type of radiation source that the target material has been exposed to, and the environment in which the device operates.

2.3.1 Total Ionization Dose effects

TID is defined as the amount of energy transferred to the target material due to ionization radiation. The unit of measurement is rad, which is an amount of energy equal to 100 ergs transferred to one gram of the target material. Due to the dependency of the amount of energy transferred onto the target material, the radiation dose is usually followed by the target material. Another unit of measurement for TID is gray (Gy), one rad is equal to 100 Gy. The main effects of TID in electronic devices are positive charge trapping (holes) in the insulation layer, and the generation of interface states in the insulation layer [8]. TID effects can be observed in electronic devices operating in space and in man-made radiation environments such as the ones in nuclear power plants or high energy particles physics experiment labs.

One of the most susceptible materials to TID is the silicon oxide (SiO_2) which is one of the most essential parts in the Metal Oxide Semiconductor (MOS) structure. The band diagram for an n-type MOS structure on a p-substrate and biased at positive voltage is illustrated in Figure 6.

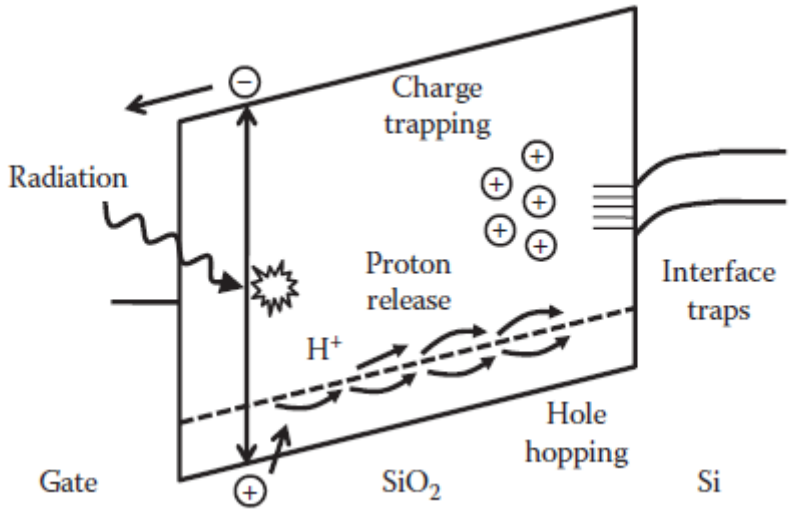

Figure 6: Band diagram of an n-type MOS biased at positive voltage [8]

Due to the transferred energy from the radiation to the silicon dioxide, some electron-holes pairs are generated inside the SiO_2. Some of these pairs are quickly recombined again in the oxide in a process called initial recombination. The amount of pairs that go through this process depends on the applied electric field, the transferred energy and the type of charged particle i.e. the source of radiation. The remaining pairs which survive the initial recombination process are called charge yield. The electrons in these pairs are attracted to the positive biased gate because of their high mobility, while the holes which are heavier and have lower mobility are attracted slowly compared to the speed of electrons to the silicon substrate. The holes remaining near their points of generation cause negative voltage shift in the characteristics of the MOS device, such as the threshold voltage [12].

As the holes which survived the initial recombination process are attracted to the silicon substrate, they move in a hopping transformation which depends on temperature and the applied electric field. This hopping process is called polaron hopping. The holes movement can take from about 10^{-17} seconds at room temperature and much longer at lower temperatures.

The holes continue their hopping movement until they reach the Silicon/Silicon Oxide (SiO_2) interface in case the gate is biased at a positive value. Some holes go to the Silicon substrate, and some others are trapped in defects sites whose density is higher near the Silicon/ Silicon Oxide (SiO_2) interface. These trapped holes can cause

permanent negative voltage shift in the characteristics of the MOS structure. This can cause a voltage shift in the threshold voltage and inversion of the channel which may cause leakage current to flow in the OFF state, leading to an increase in the static power of the integrated circuits. The number of trapped holes depends on the number of holes that survive the initial recombination process, and the quality of the oxide [8][12].

When holes are trapped near the Si/SiO_2 or during the hopping process, some hydrogen ions (protons) can be released. These hydrogen ions arrive at the interface which cause the generation of interface traps. These interface traps can exchange carriers with the channel, and their occupancy depends on the position of the Fermi level at the interface. The creation of these traps is much slower than the charge accumulation due to the trapped holes near the interface, but it also depends on the applied electric field. Interface traps can cause a positive shift in the threshold voltage of the NMOS transistor and a negative voltage shift in the threshold voltage of the PMOS transistor. It can also affect the mobility of the transistor which in turn decreases its current capability and causes timing degradation of the integrated circuits [8][12].

2.3.2 Single-Event effects

Single-Event effects (SEE) are caused by the passage of high-energy particles (heavy ion) through sensitive regions of an electronic device. They can be classified into two categories depending on their effects. Soft, in which the damage is not permanent e.g. soft errors in memory circuits, and hard in which the damage is irreversible e.g. the rupture of the dielectric in the gate. Some other SEE may or may not cause damage depending on the operation of the electronic device, such as in the case of a single-event latch-up, in which the time to cut the power supply after the occurrence of the event decides whether or not there is damage to the device [8].

Some of the main SEE are [8][13]:

1- Single-event upset (SEU):

   A soft SEE which is characterized by the flipping of the value of a single bit in a memory due to a single ionizing particle. It is also known as soft error. It is important to mention that the correct value of the memory bit can restored by rewriting the bit again i.e. the damage is not permanent.

2- Single-event gate rupture (SEGR):

   A hard SEE which is characterized by the rupture of the gate of a MOSFET, in which this rupture or damage is irreversible or permanent.

3- Single-event latch-up (SEL):

   A SEE that its damage depends on the operation of the circuit after being exposed to radiation. It is characterized by the activation of parasitic bipolar structures in CMOS circuits, which leads to a sudden increase in supply current. Depending on the time taken to cut the power source of the circuit, there may or may not be damage to the device.

Chapter 3

Total Ionizing Dose effect in CMOS circuits

Total Ionizing Dose effect "TID", which affects electronic devices operating in radiation environments like space and man-made radiation environment found in nuclear reactor, can cause several physical damages on the correct operation of CMOS circuits. These damages are due to the ionizing-radiation effect on the material used in the fabrication of CMOS circuits, specially the MOS structure. In this chapter, some of the damages caused by the "TID" effect on MOS transistors are illustrated, as well as TID testing techniques.

3.1 TID effect in MOS transistor

When MOS transistors are exposed to ionization radiation, electron-hole pairs are generated by the interaction of the high-energy particles with the atoms of the dielectric (SiO_2). The density of the generated electron-hole pairs along the track of the high-energy particles exposed to the target material, is directly proportional to the energy transferred to the target material. Linear energy transfer (LET) or stopping power which expresses the loss of energy per unit length (dE/dx), is related to the energy that enters a discrete plane of the target material (ΔE_E) and the radiation energy that leaves material plane (ΔE_L) by the following equation [14]

$$\Delta E_L(\gamma) = \Delta E_E(\gamma)\, exp\left(-\frac{\mu_{en}}{\rho}\rho\Delta x\right) \quad (1)$$

where μ_{en}/ρ is the mass attenuation coefficient of the target material, ρ is the target material density, and Δx is the thickness of the target material. The LET for protons shows a monotonic decrease with increasing energy of protons, while in the case of electrons, the LET decreases as a function of particle energy for energies below 1 Mev, while it increases for higher energies as shown in Figure 7 [15].

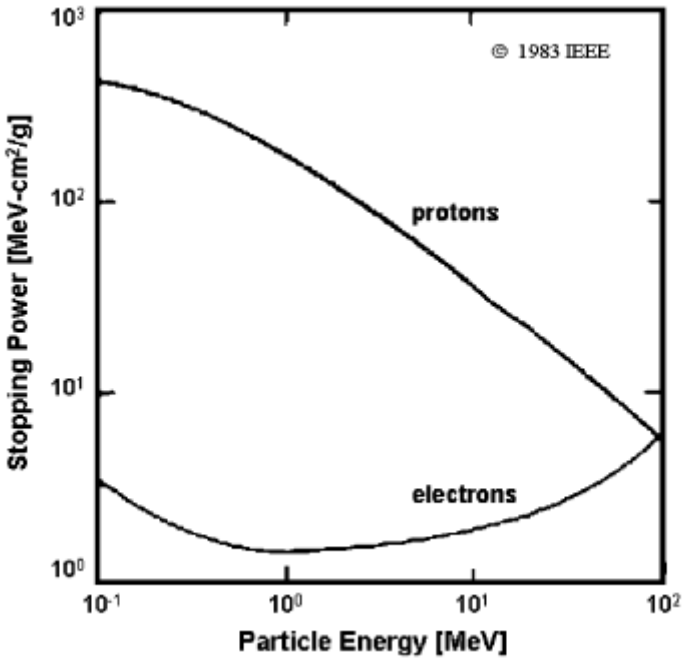

Figure 7: Linear energy transfer for protons and electrons as a function of particle energy [15]

The electrons generated along the track of the charged particles are mostly swept rapidly toward the gate (positive charge side), due to their high mobility, while the holes with lower mobility are swept in a relatively slow motion compared to the electrons, to the oxide-Silicon (SiO_2/Si) interface. A fraction of the holes moving toward SiO_2/Si interface will get trapped, which results in the formation of positive oxide-trap charges [16].

In addition to the oxide traps, interface traps can also be generated at the SiO_2/Si interface. These interface traps are a result of the interaction between the hydrogen ions that can drift to the interface. The interface traps generation process occurs in a longer time compared to the oxide charges generation process. They act as energy levels within the silicon band-gap. Interface traps can be negative or positive, depending on the location of the Fermi level at the interface, if the Fermi level at the interface is below the trap energy, it acts as a donor and the interface trap is positively charged, and if the Fermi level at the interface is above the trap energy, it acts as an acceptor and the interface trap is negatively charged. Positive interface traps causes negative threshold voltage shifts for p-channel transistors, while negative interface traps causes positive threshold voltage shifts for n-channel transistors [12].

Due to the oxide charges and interface traps, degradation of the MOS transistors characteristics occurs. Most common and critical degradations are threshold voltage shifts, mobility degradation and induced leakage current in CMOS devices.

3.1.1 Threshold voltage shifts

For MOS transistors, the total threshold voltage shifts due to TID is the sum of the threshold voltage shifts due to both oxide charge traps and interface traps which can be expressed by the following equation

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \tag{2}$$

where ΔV_{ot} is the threshold voltage shift due to oxide charge traps, and ΔV_{it} is the threshold voltage shift due to interface traps. They can be determined by the following equation:

$$\Delta V_{ot,it} = \frac{-1}{C_{ox}\, t_{ox}} \int_0^{t_{ox}} \rho_{ot,it}(x) x dx \tag{3}$$

where $\rho_{ot,it}(x)$ is the charge distribution of radiation-induced oxide charge traps or interface traps. For positive charges, the threshold voltage shift is negative, in contrast, for negative charges, the threshold voltage shift is positive [12].

The effect of oxide charge traps is illustrated in Figure 8. For n-channel MOSFET, the oxide charge traps shift the V_{gs} bias point by a negative value, which results in a reduction of the threshold voltage and in an increase of the drive current and the off-state current. For p-channel MOSFET, the oxide charge traps also shifts its bias point by a negative value, which results in an increase in the threshold voltage and a reduction of the drive and off-state currents [15].

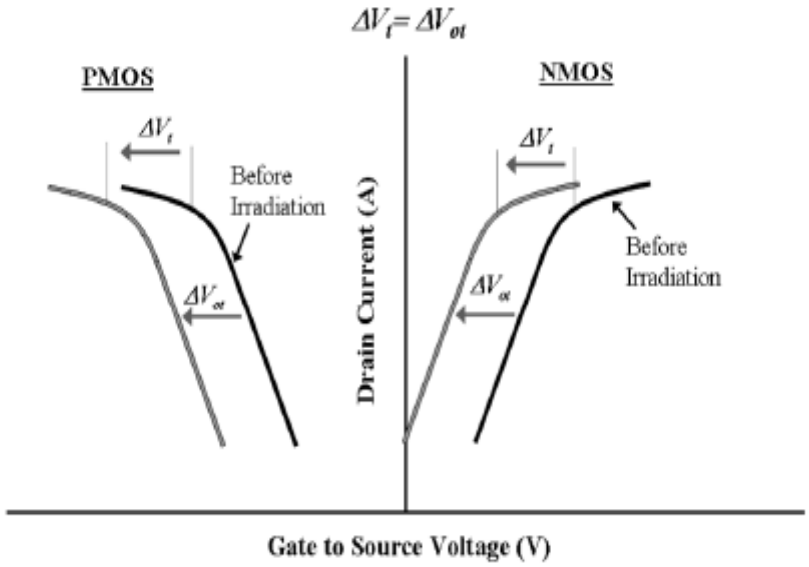

Figure 8: Illustration of the oxide charge traps on n and p channel MOSFETs [15].

The effect of interface traps is illustrated in Figure 9. Interface traps cause an increase in the subthreshold swing of both n and p channel MOSFETs. Figure 9 also shows that the threshold voltage is also impacted by the interface traps, for n channel MOSFET interface traps cause a shift in the threshold voltage by a positive value, while for a p channel MOSFET interface traps cause a shift in the threshold voltage by a negative value [15].

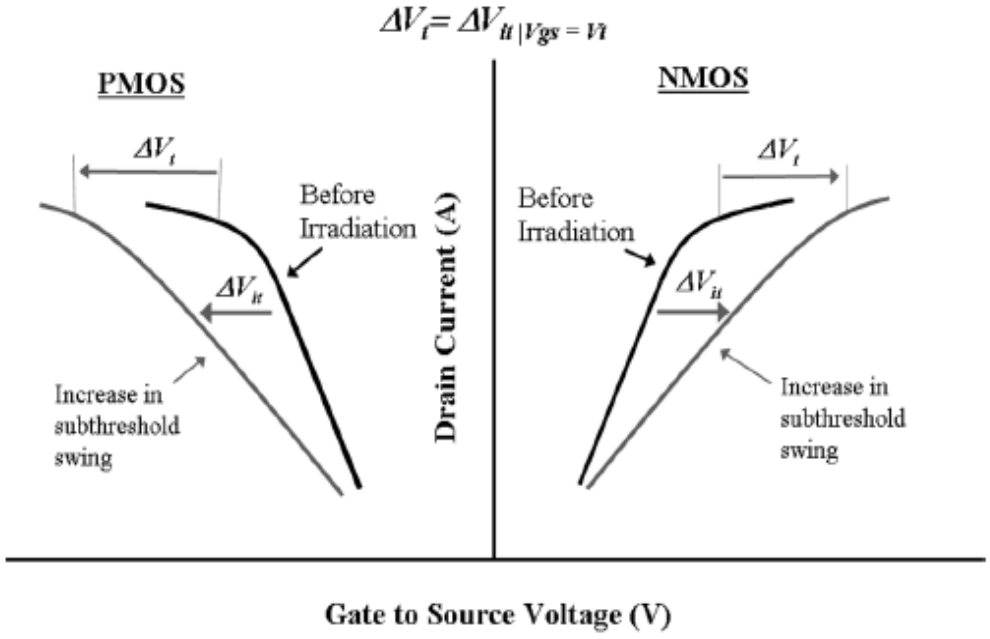

Figure 9: Illustration of the effect of the interface traps on n and p channel MOSFETs [15]

The effect of oxide charge traps on the threshold voltage shift can have a little neutralization at high dose rate and short time, while the effect of interface traps won't have enough time to build up. So, for high dose and short time, the shift in the threshold voltage can be large and negative for both n and p channel MOSFETs. For n-channel MOSFET large negative shift in the threshold voltage can lead to an increase in the leakage static power of the integrated circuit, which can lead eventually to a failure in the integrated circuit [12].

At moderate dose rates, the effect of oxide charge traps can have some neutralization, and interface traps can occur. Therefore, the threshold voltage shift due to both oxide charge traps and interface traps can be large. For n-channel MOSFET the threshold voltage shift due to oxide charge is negative, while the threshold voltage shift due to interface traps is positive, thus, they compensate each other, and even if the individual threshold voltage shift is large, the net threshold voltage shift can be small, and the failure level of the integrated circuit due to radiation can be relatively high. For p-channel MOSFET, the threshold voltage shift due to oxide charge traps and interface traps has a negative value, therefore, they add to each other unlike the n-channel MOSFET case [12].

Radiation induced charge buildup decreases rapidly with the decrease in the oxide thickness, and the threshold voltage shift is directly proportional to the oxide thickness by the following equation [15]

$$\Delta V_{ot} \propto t_{ox}^2 \tag{4}$$

This relation indicates that with the advancement in CMOS technology and the scaling down of the oxide thickness, the threshold voltage shift is reduced. Instead, charge trapping in the shallow trench isolation (STI) dielectrics, which thickness is much larger than that of the gate oxide, has become more dangerous threat in modern CMOS technologies. As a result, interface traps and oxide charge traps in the thin gate oxides are not a concern, and the total dose effects are dominated by oxide charge traps in the field oxides even at low dose of radiation [12][15].

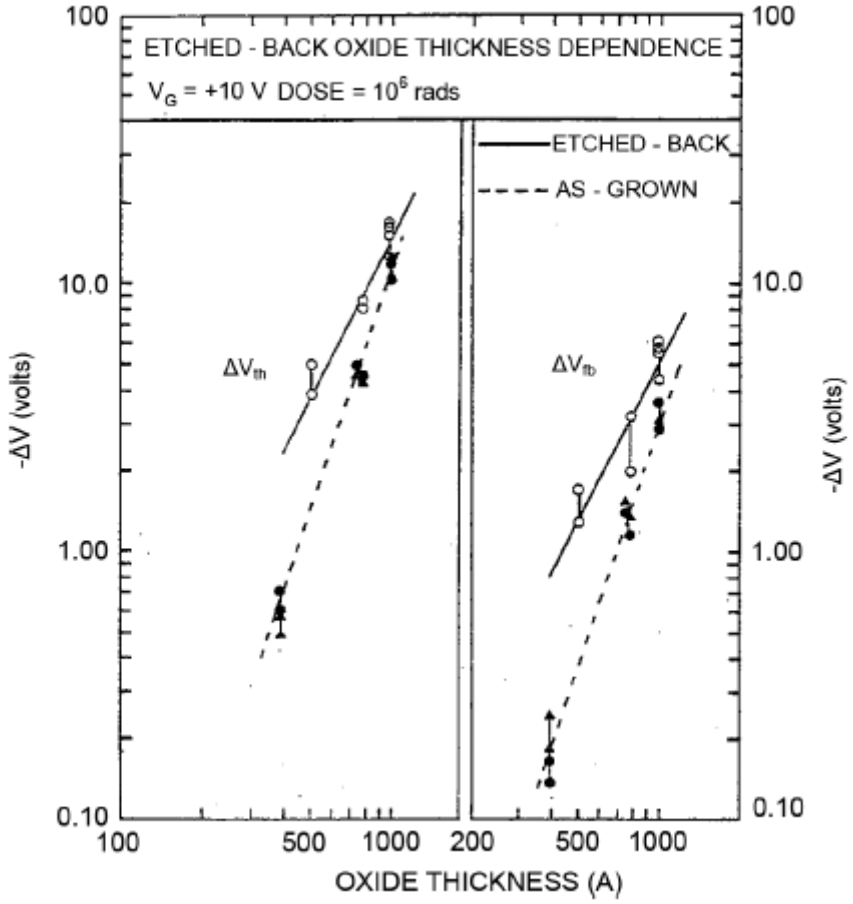

Figure 10: Illustration of the decrease in the threshold voltage shift with the scaling down of the gate oxide [17]

Other factors that can affect the value of the threshold voltage shift are the transistor dimensions (width "W" and length "L") and the device type. The narrower the width (W), the larger is the magnitude of the threshold voltage shift, this is valid for both n and p channel MOSFETs, and for width values larger than about 1 µm, the threshold voltage value should not be critical. Also, the shorter the length (L) of the transistor, the larger is the magnitude of the threshold voltage shift. For larger values of width (W) and length (L) of the transistor, the value of the threshold voltage shift is small and there is no important dependency on the transistor size [18].

3.1.2 Carriers mobility degradation

Interface traps and oxide charge traps have other effects in addition to threshold voltage shift that can affect MOS transistors. They can affect the carries mobility in the

MOS device. These effects can cause degradation in the drive capabilities of the MOS transistor, degrading the timing parameters of an integrated circuit, which may cause timing failure in the electronic circuit operation.

During the oxide charge traps formation process, holes which survived the initial recombination process are attracted to the silicon substrate. The holes transport through the Silicon Oxide (SiO_2) by a process called "Polaron hopping" which depends on the temperature and the applied electric field. Polaron causes an increase in the effective mass of the holes and a decrease in the holes mobility [12].

Like oxide charge traps, interface traps will also exchange charges with an adjacent silicon layer, but unlike oxide charge traps, interface traps are located exactly at the interface. Hence, there is no barrier to trapping and detrapping of carriers in the near surface silicon. That is why interface traps can have a significant effect on the mobility of the carries in the MOS device [15].

Both oxide charge traps and interface affects the mobility of carriers in a MOS transistor, but as illustrate in Figure 11, interface traps have a first order effect on the effective mobility of carriers of a MOS transistor, while oxide charge traps have a much weaker effect. This is due to the fact that scattering of carriers from interface traps is much more efficient than the more distant oxide charge traps in causing mobility degradation of carriers in a MOS transistor [17].

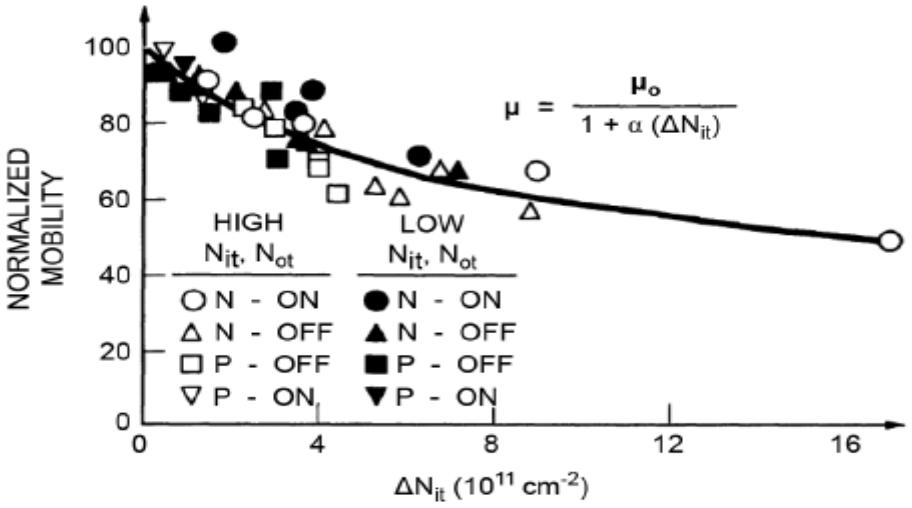

Figure 11: Mobility of carriers normalized to the pre-irradiation values as a function of interface traps density for devices with high and low interface traps and oxide charge traps densities [17]

3.1.3 Induced leakage current

In commercial CMOS technologies, another phenomenon resulting from the damage of the TID effect on the transistors, is the radiation induced leakage current (RILC). Basically, this phenomenon depends on two damaging mechanisms that happens to CMOS circuits exposed to TID effect. The first mechanism is the threshold voltage due to the silicon dioxide charge traps, and the second mechanism is the built-up charges in the filed oxide p-substrate. This phenomena is illustrated in Figure 12, which is a plot of the gate leakage current, versus gate voltage, for a non-irradiated p-substrate capacitor and a capacitor irradiated to 5.3 Mrad(Si) with Co-60 gamma rays at a gate bias of 0.3 V[12].

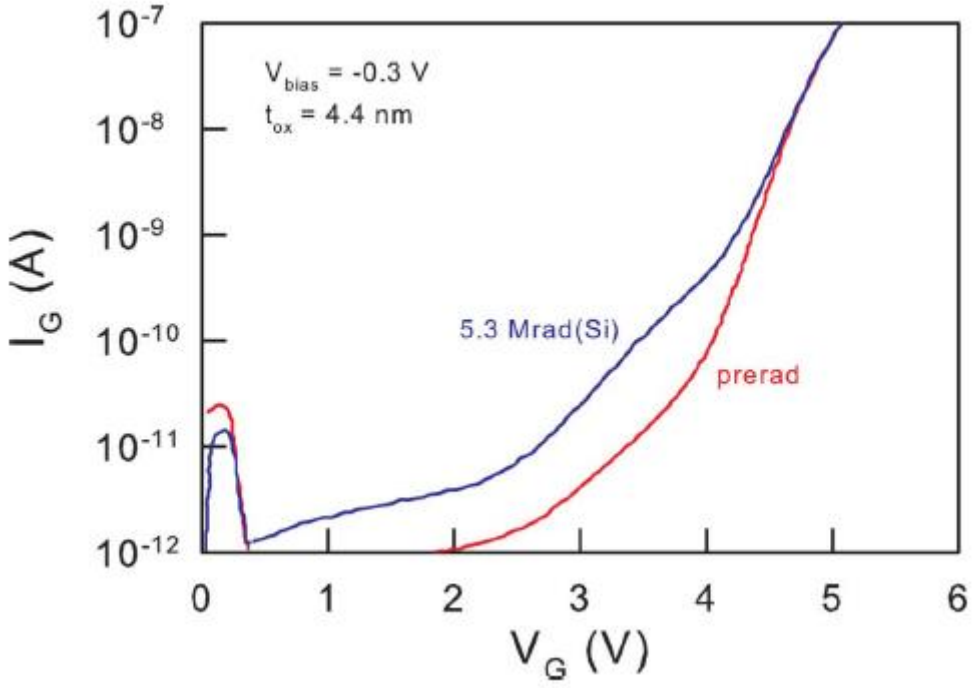

Figure 12: Gate oxide leakage current versus gate voltage for a non-irradiated capacitor and an irradiated capacitor to 5.3 Mrad(Si) [12]

With the technology scaling down, the gate oxide thickness tends to ultra-thin oxides, which makes modern IC less susceptible to radiation damage, but the filed oxides of advanced commercial technologies are still much thicker than the gate oxides and the radiation response increases proportionally with the oxide thickness. Thus, the

effect of field oxides is the most dominant effect of TID and its effect is the main concern and radiation problem of these modern technologies [12].

There are two common types of filed oxides used in the manufacturing of CMOS circuits, which are different in their formation method and their shape. The first type is local oxidation of silicon (LOCOS), which has been replaced by commercial IC manufacturers with the second type "shallow-trench isolation (STI)" for advanced submicron technologies. Figure 13(a) shows a cross section of an n-channel transistor with LOCOS isolation, showing the built-up charges in the area called "bird's beak region". Figure 13(b) shows a cross section of an n-channel transistor with STI isolation, showing the built-up charges [12].

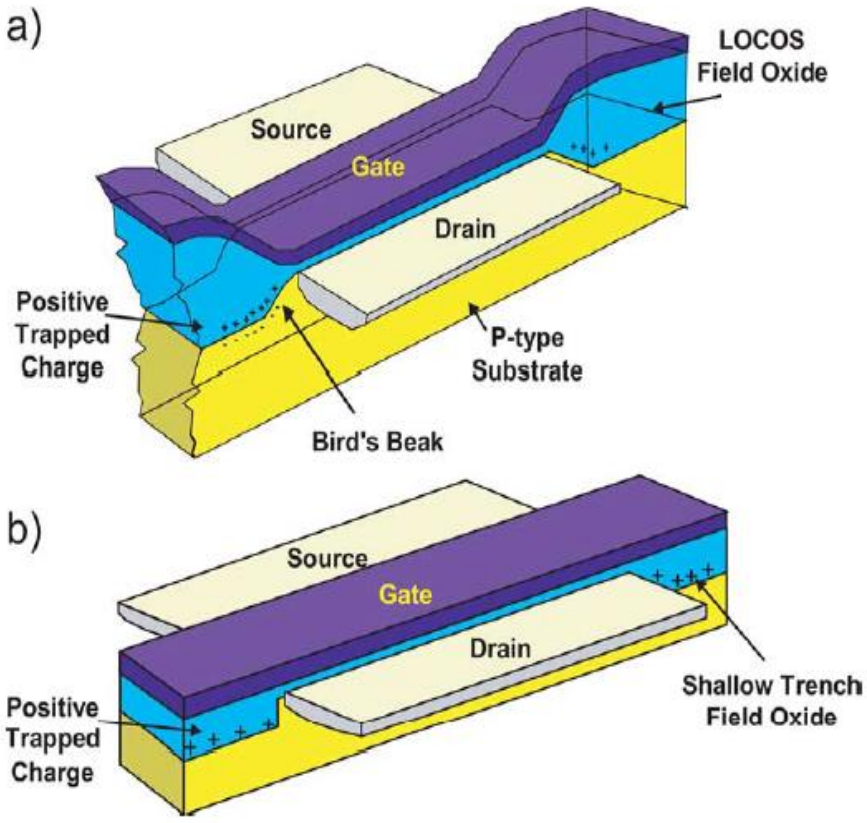

Figure 13: cross section of a) n-channel transistor with LOCOS isolation and b) n-channel transistor with STI isolation [12]

Radiation induced leakage current in shallow-trench isolation (STI) oxides is typically caused due to the exposure of high fluxes of ionizing radiation. Micro-doses of damage caused by a single ion strike have also been observed in submicron CMOS

technologies. Induced leakage current in STI can cause an increase in the standby current in modern CMOS integrated circuits. The increase of the standby current of CMOS shift registers which are manufactured in a commercial 130 nm process is illustrated in Figure 14 [15].

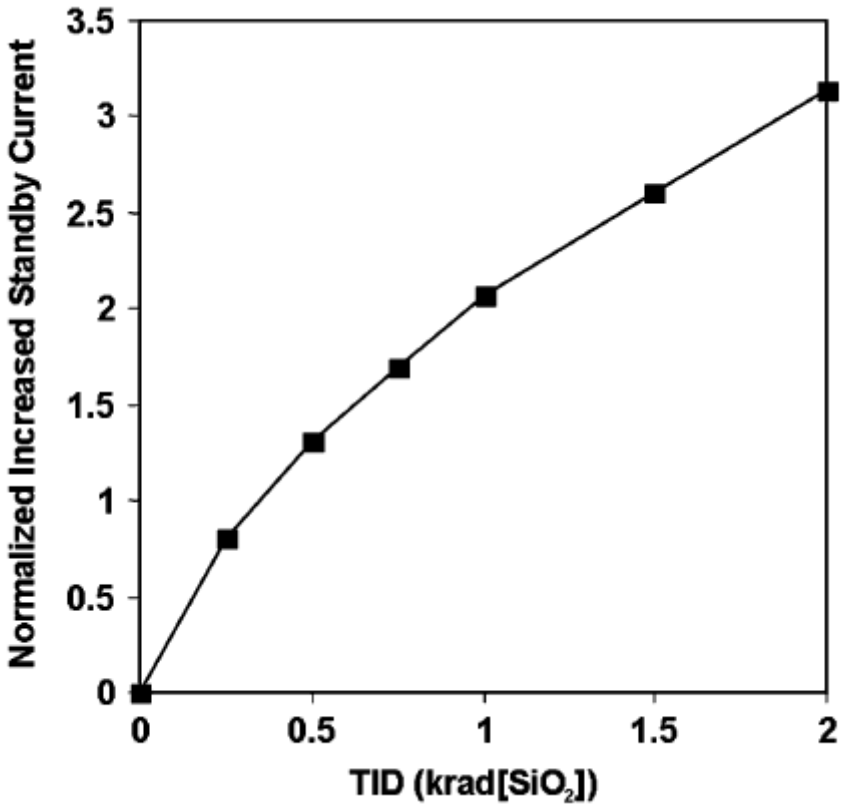

Figure 14: Normalized increased standby current in CMOS shift registers manufactured in 130 nm process as a function of the TID dose in krad [15]

The induced leakage current in the STI oxide which causes an increased in the standby current in the integrated circuits is caused by the leakage paths created because of the built-up charges by the TID effect. These leakage paths include: drain to source leakage in a single n-channel MOSFET, drain to source leakage between two n-channel transistors, and source to well leakage between different devices. The mechanism for these leakage paths are the same, it is basically because of the positively charged oxide traps invert an adjacent p-type silicon layer, which enables the flow of current from isolation region to another [15].

In the drain to source leakage path, built-up charges in the isolation dielectric at the interface along the sidewalls of the STI oxide are the cause of the creation of a

leakage path, which becomes the most significant cause to the standby current in n-channel MOSFET as illustrated in Figure 15. The impact of the STI radiation damage on the standby current for a n-channel MOSFET manufactured by a 180 nm process by the Taiwan Semiconductor Manufacturing Company (TSMC) is shown in Figure 16. The data shows a significant increase in the drain source current above 200 krad(SiO_2), and the drain source current reaches a value above 100 nA at 500 krad(SiO_2) of total dose [15].

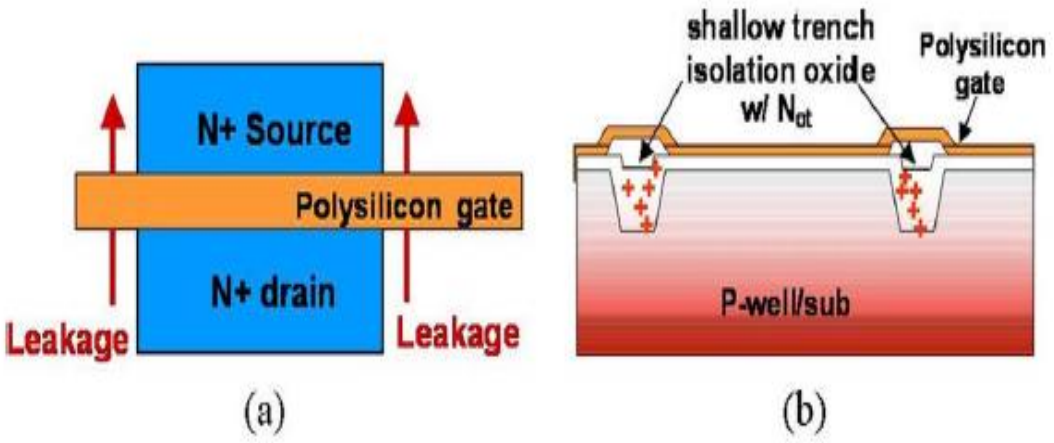

Figure 15: a) Illustration of drain source leakage path in a n-channel MOSFET and b) its cause; built-up charges in the isolation oxide [15]

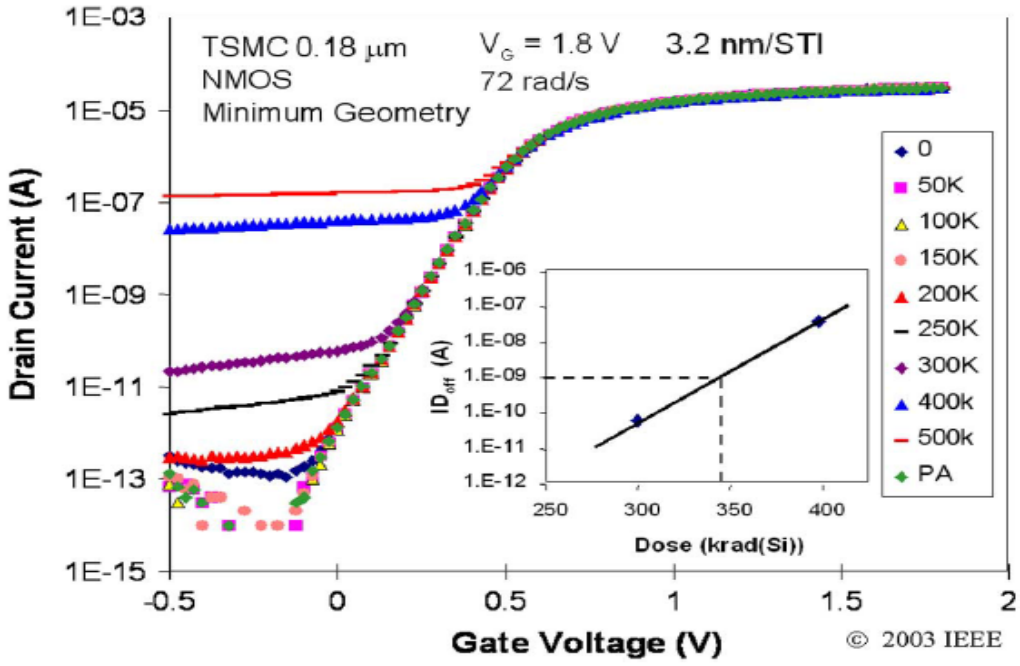

Figure 16: Impact of STI radiation damage on the current-voltage characteristics of n-channel MOSFET fabricated in TSMC 180 nm CMOS process [15]

For the drain to source leakage between two n-channel transistors, and source to well leakage between different devices, the leakage paths are interdevice paths between two adjacent n-channel transistors or between the n+ drain/source of one n-channel transistor and the n-well of an adjacent p-channel transistor, unlike the case for the drain source leakage in which the leakage path is in the same device. The leakage path between two n-channel transistors is illustrated in Figure 17, and the leakage path between an n-channel transistor and a p-channel transistor is illustrated in Figure 18 [15].

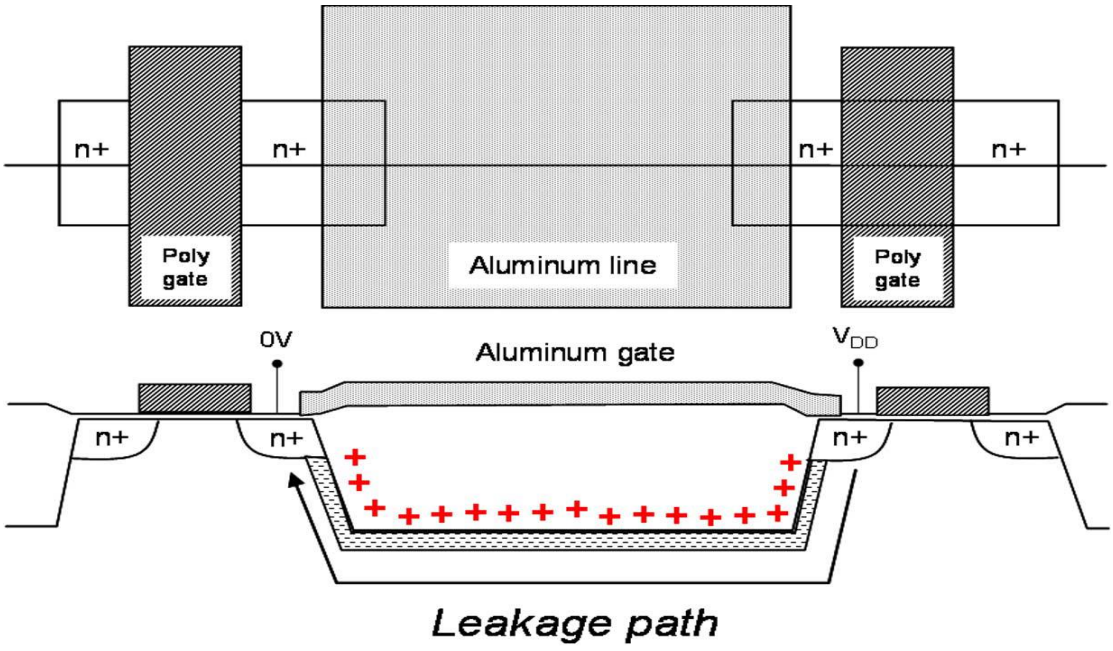

Figure 17: Leakage path between two adjacent n-channel transistors [15]

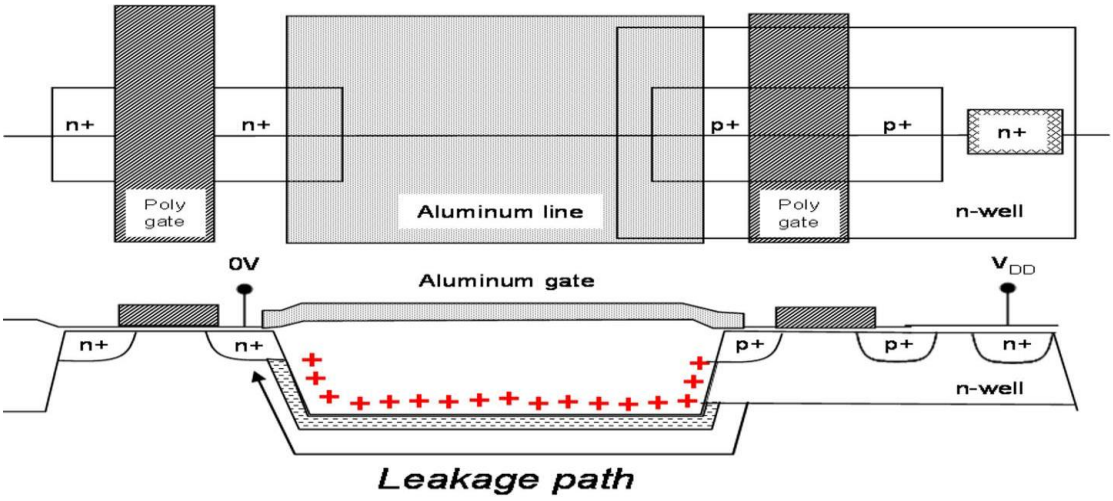

Figure 18: Leakage path between the source of n-channel MOSFET and the n-well of p-channel MOSFET [15]

The leakage paths between two different devices can be observed in the example of two inverters chain shown in Figure 19. Path (a) drains current from V_{DD} to ground because of the leakage path between the drains of two adjacent n-channel MOSFETs. This path is completed by the p-channel MOSFET in the second inverter and the n-channel MOSFET in the first inverter. Path (b) also drains current from V_{DD} to ground because of the leakage path between the drain of the n-channel MOSFET of the first inverter to the n+ well of the p-channel MOSFET of the first inverter. This path is completed by the n-channel MOSFET of the first inverter [15].

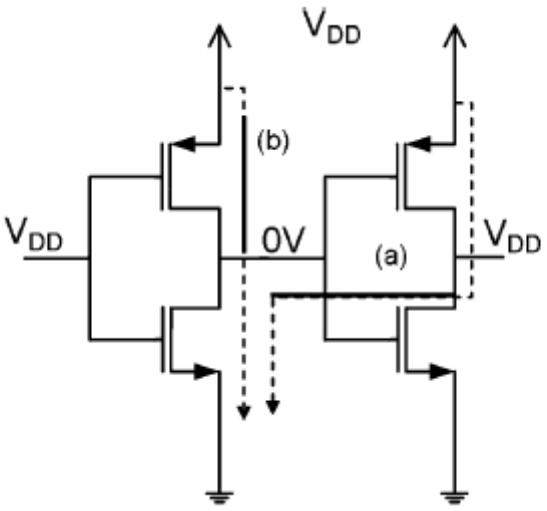

Figure 19: Example of how interdevice leakage can increase the standby current of an inverter chain. Path (a) represents the leakage path between two n-channel MOSFETs. Path (b) represents the leakage path between the drain of n-channel MOSFET and the n+ well of p-channel MOSFET [15]

The effect of the leakage current caused by the field oxides can be modeled as a parasitic field-oxide transistor which is in parallel with the gate-oxide transistor. Consider the case at the edges of the gate transistor where the gate polysilicon overlaps with the field oxide, the parasitic parallel field-oxide transistor is formed by the gate polysilicon, a portion of the field-oxide and the source and the drain of the gate transistor. As illustrated in Figure 20, during the preirradiation, the threshold voltage of the parasitic field-oxide is relatively large due to the large thickness of the field oxide, but with the radiation and the charge built-up process in the field oxide, a negative threshold voltage shift occurs in the parasitic field-oxide transistor, which shifts its drain to source leakage current versus the gate to source voltage curve to the left. If the value of this threshold voltage shift is high enough, it can cause an increase in the

"OFF" state leakage current of the gate transistor, which can prevent the gate transistor from being completely turned off. This effect can add significantly to the standby current of an integrated circuit [12].

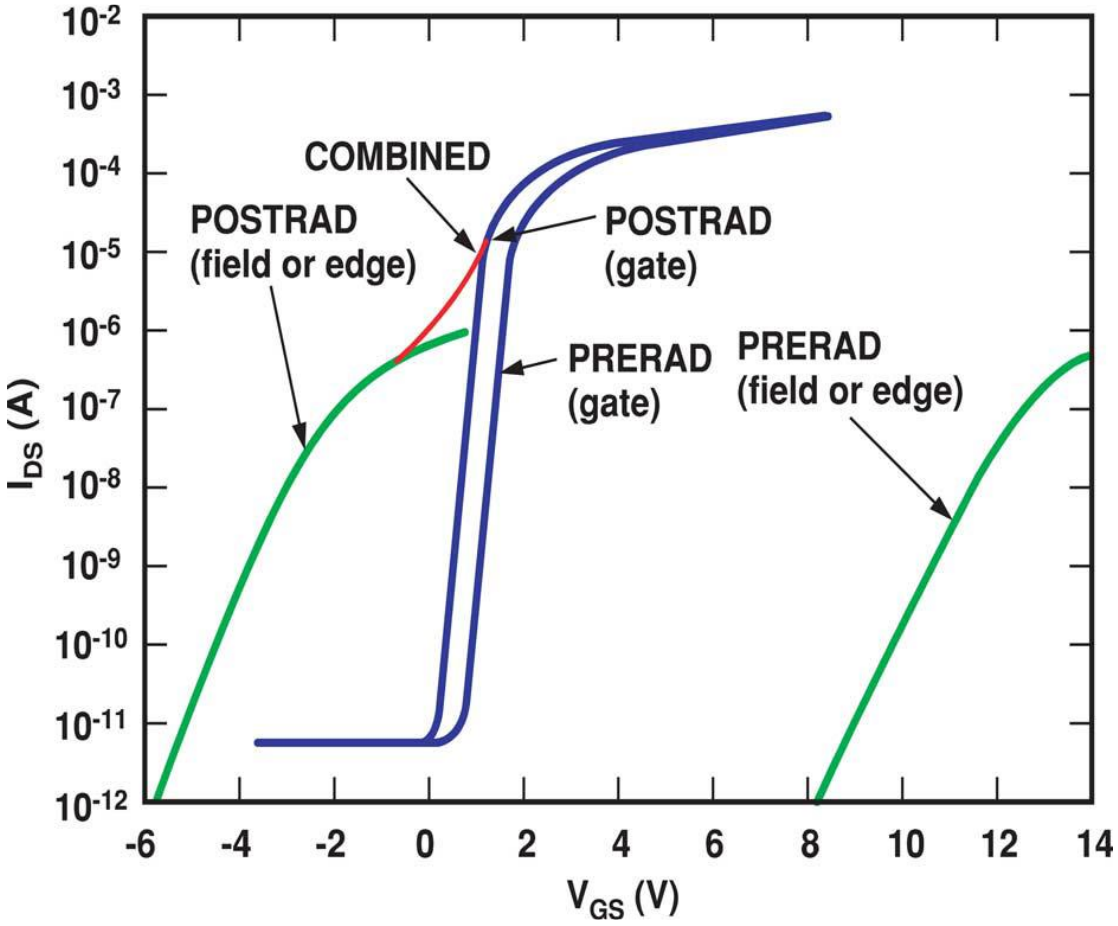

Figure 20: I-V curves for parasitic field-oxide and gate-oxide transistors showing the increase in the standby currents caused by the leakage in the field oxides [12]

3.2 TID effect in floating gate MOS

Field programmable gate arrays (FPGA) have become one of the most important devices in the electronic industry, with its high logic density, fast deployment, and reprogram ability, FPGA is the best choice for projects with limited budget and resources, and tight schedules. Flash based FPGA has advantages over other technologies like SRAM, of being re-programmable and nonvolatile. To analyze the radiation effect on flash-based FPGA, an analysis of the radiation effect in the switch

element, which consists of floating gate MOS, is required. In fact, the radiation response of the floating gate MOS is the dominant response in flash-based FPGA [19].

3.2.1 Floating gate MOS

Flash-based FPGA switch element consists of two floating gate NMOS transistors as illustrated in Figure 21. The first transistor, which is called the switch transistor, is responsible for turning on or off the data path, the other transistor, which is called the program/sense transistor, is responsible for programming the floating gate voltage and sensing the current during threshold voltage measurement. The switch and the program/sense transistors have the same control gate and the same floating gate. Depending on the threshold voltage, the switch transistor can be turned on or off. This threshold voltage is determined by the charge stored in the floating gate by a mechanism called Fowler-Nordheim tunneling through the thin gate oxide during the process of programming and erasing the FPGA. To turn the switch transistor on, a low threshold voltage must be programmed in the floating gate, and to turn the switch transistor off, a high threshold voltage must be "erased" in the floating gate [19].

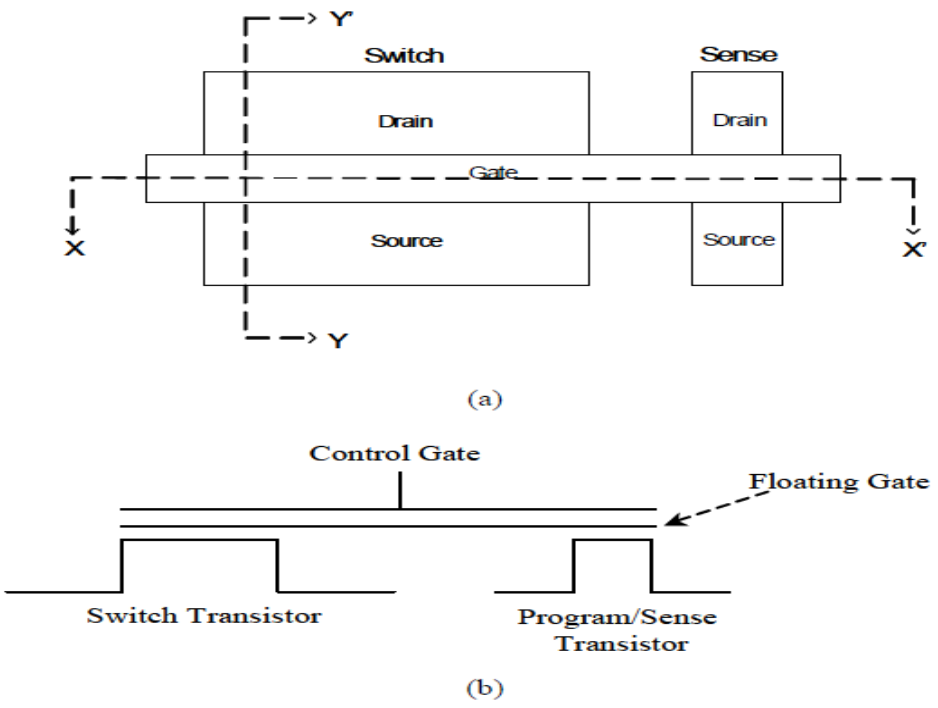

Figure 21: a) Layout of the switch element for the flash-based FPGA. b) Schematic showing the cross section X-X' [20]

Figure 22 shows the structure of the floating gate transistor. It is an NMOS transistor with a tunnel oxide, which is composed of silicon dioxide, and between the floating gate, which is composed of poly silicon, and the control gate, which is also composed of poly silicon, there exists a layer of inter-poly oxide-nitride-oxide (ONO) composite dielectric [19].

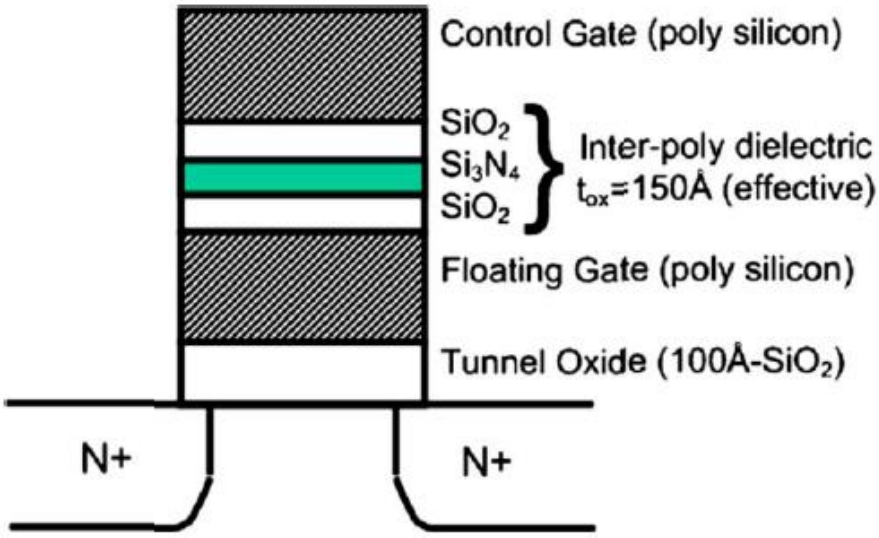

Figure 22: Schematic of the floating gate transistor in flash-based FPGA [20]

The energy band diagrams for the floating fate MOS for the high and low voltage threshold cases are illustrated in Figure 23 and 24, respectively. For the high threshold voltage or the “erased” state case, the threshold voltage of the transistor is affected by three mechanisms which are induced by the radiation: holes which are injected into the floating gate, trapped holes in the oxides, and emission of electrons over the poly-silicon/oxide barriers. When radiation hits the floating gate MOS, some electron-hole pairs are generated, which cause, depending on the applied electric field, injection and trapping of holes in the floating gate and the oxides, by increasing the electric field the number of tapped and injected holes increases. These trapped and injected holes result in a decrease in the threshold voltage. When the energy of photons caused by the radiation exceeds the potential barrier, electron emission occurs, which also cause a reduction in the threshold voltage [19].

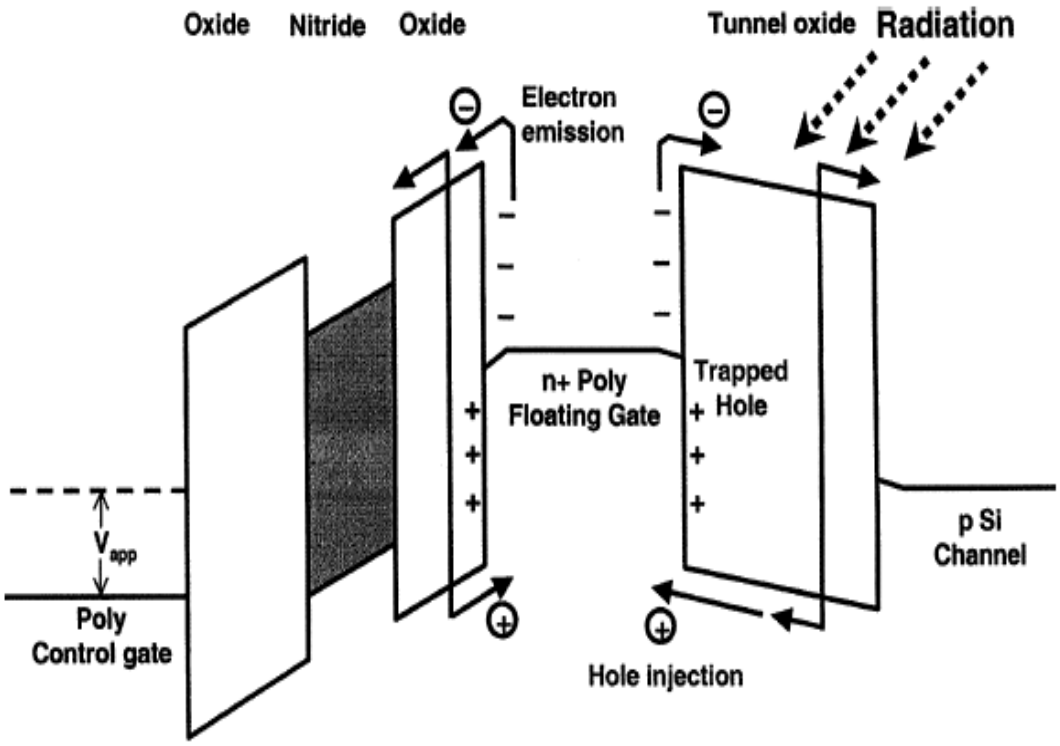

Figure 23: Energy band diagram for the floating MOS transistor for the high threshold voltage or "erased" case, showing the radiation mechanisms that affects the threshold voltage [19]

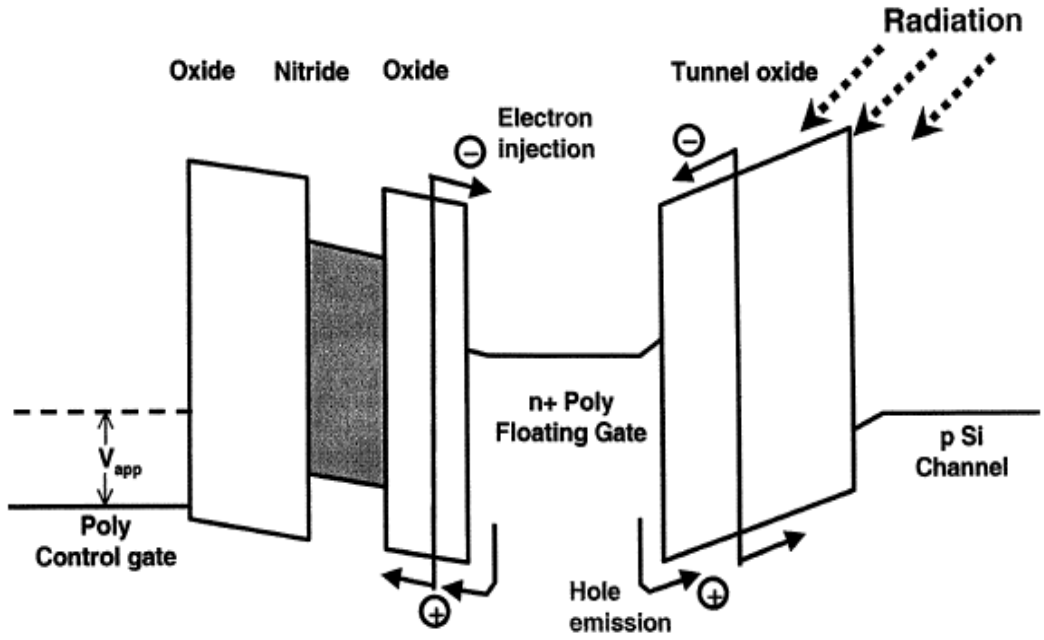

Figure 24: Energy band diagram for the floating MOS transistor for the low threshold voltage or "programmed" case, showing the radiation mechanims that affects the threhold voltage [19]

The relation between the threshold voltage of the floating gate MOS transistor and the electronic charge stored on the floating gate can be determined by the following equation:

$$V_{th} = V_{si} + \frac{Q_{fg} d_{ono}}{\epsilon_{ox}} \quad (5)$$

where V_{si} is the threshold voltage determined by processing and it is a function of many variables including the dielectric thickness; Q_{fg} is the net electronic charge per unit area stored on the floating gate; d_{ono} is the effective oxide-nitride-oxide (ONO) thickness; ϵ_{ox} is the oxide permittivity [19].

3.2.2 Threshold voltage shift

The threshold voltage shift in the floating gate MOS transistor is mainly due to three radiation induced mechanisms: injection of holes into the floating gate, trapped holes into the oxide, and electrons emission over the poly-silicon/oxide barriers. The holes injected and trapped into the floating gate and the oxide are due to the generated electron-hole pairs generated from the radiation, and the electron emission occurs if the photons induced by the radiation have more energy than the potential barrier. These three phenomena cause a reduction in the threshold voltage shift of the floating gate MOS transistor. The dependency of the threshold voltage on the radiation can be determined by the following relation:

$$V_{th}(\gamma) = C_0 + BV_{bias} + [C_1 - BV_{bias}] \exp(-A\gamma) \quad (6)$$

where γ is the total ionizing dose, V_{bias} is the control gate bias, and C_0, C_1, B and A are physical constants [20].

The I_d versus V_g curves for the high threshold or "erased" state flash cell before and after irradiation is illustrated in Figure 25, and Figure 26 shows the curves for the low threshold voltage or "programmed" state flash cell. Figure 27 shows the threshold voltage of both "erased" and "programmed" state flash cell, showing experimental data fitting to the model determined by equation (6) [20].

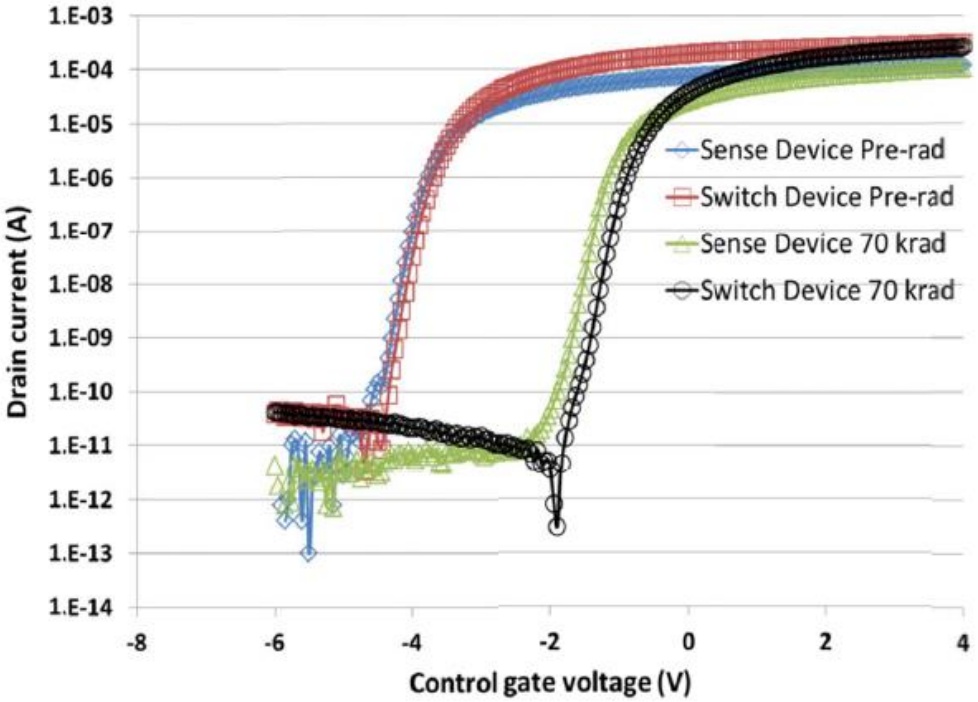

Figure 25: TID effect on the high threshold voltage flash cell [20]

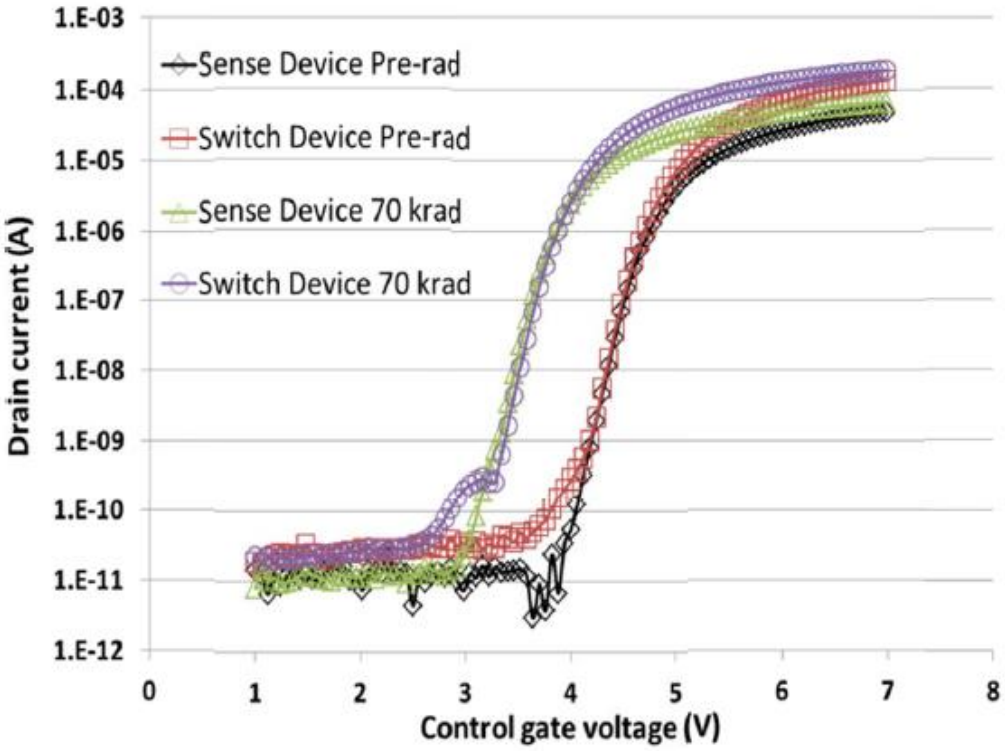

Figure 26: TID effect on the low threshold voltage flash cell [20]

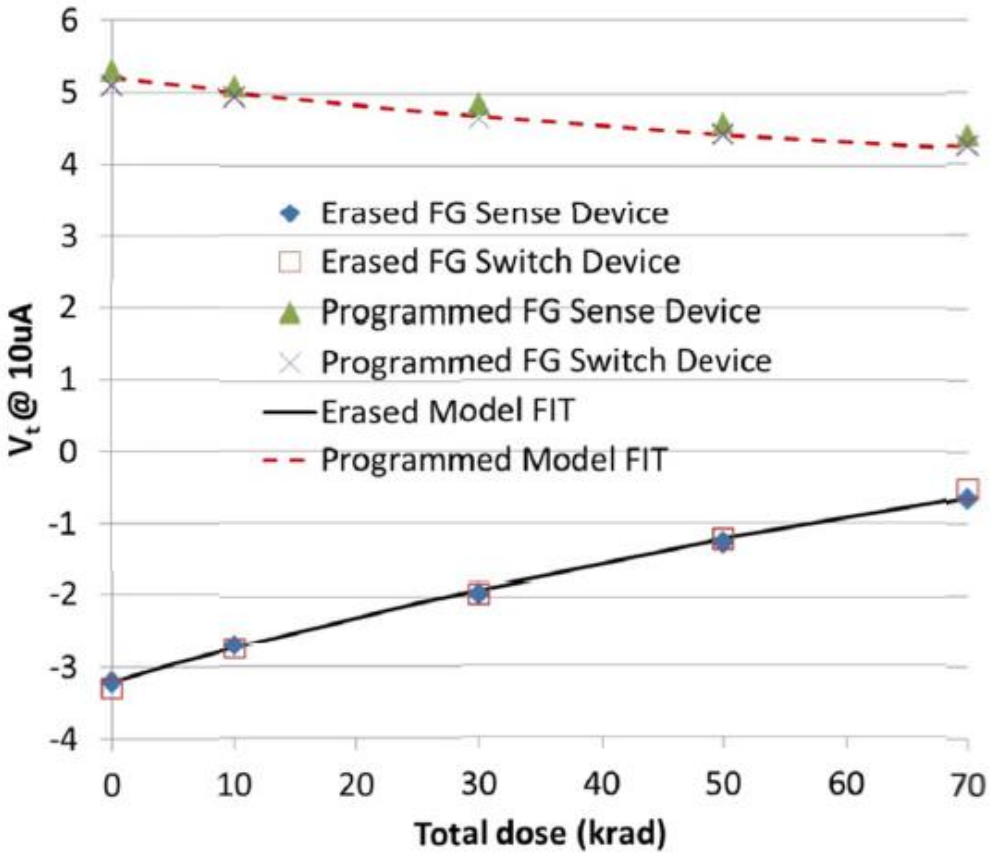

Figure 27: Experiment threhold voltage versus total dose for both low threshold and high threshold voltage flash cells and model prediction (dashed line) [20]

3.2.3 Propagation delay degradation

The threshold voltage shift in the floating gate MOS transistor of flash-based FPGA, affects the circuit parameters, one of the most important aspects of the effects of the threshold-voltage shift, is the degradation in the propagation delay. Propagation delay versus total dose experiment was conducted on a 1000-stage inverter string on a second-generation flash-based FPGA, named ProASIC^{PLUS} APA family. The experimental data for the propagation delay for both biased and unbiased cases is illustrated in Figure 28. As shown in Figure 28, the propagation delay degradation seems to have a total-dose threshold, this threshold has a higher value for the unbiased case than the biased radiation case [19].

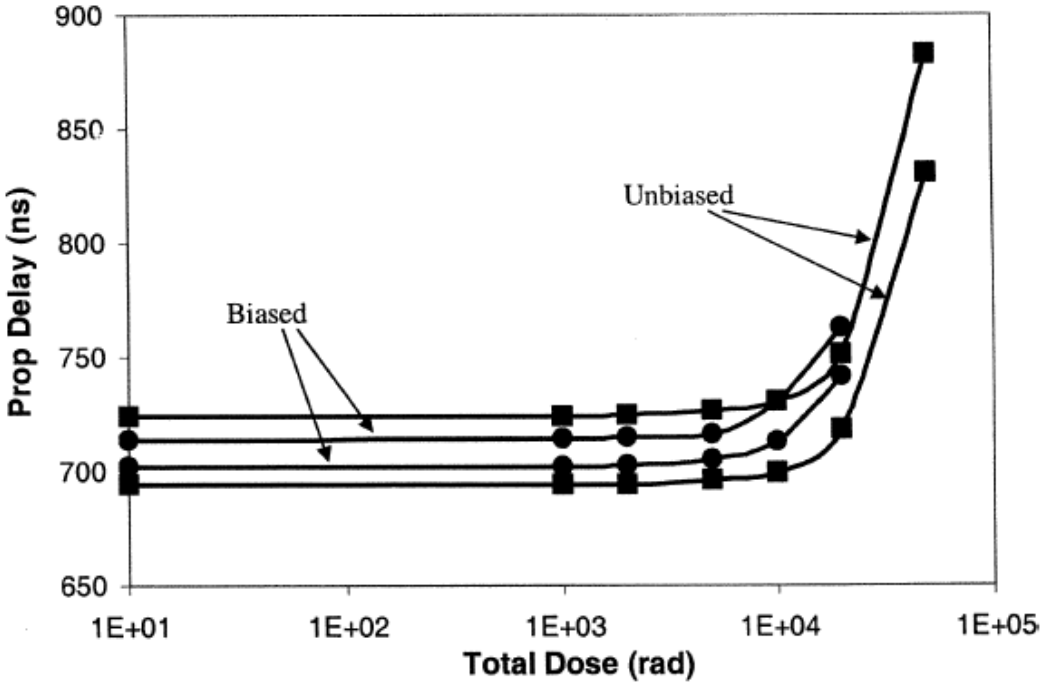

Figure 28: Experimental propagation delay versus total dose for 1000 inverter string [19]

The comparison between the SPICE simulation prediction and the actual experimental data of the propagation delay for unbiased and biased radiation conditions are shown in Figure 29 and 30, respectively. As shown in the figures, the experimental data fits the simulation prediction for the biased radiation condition, but the experimental data has less degradation than the simulation prediction for the unbiased radiation condition [19].

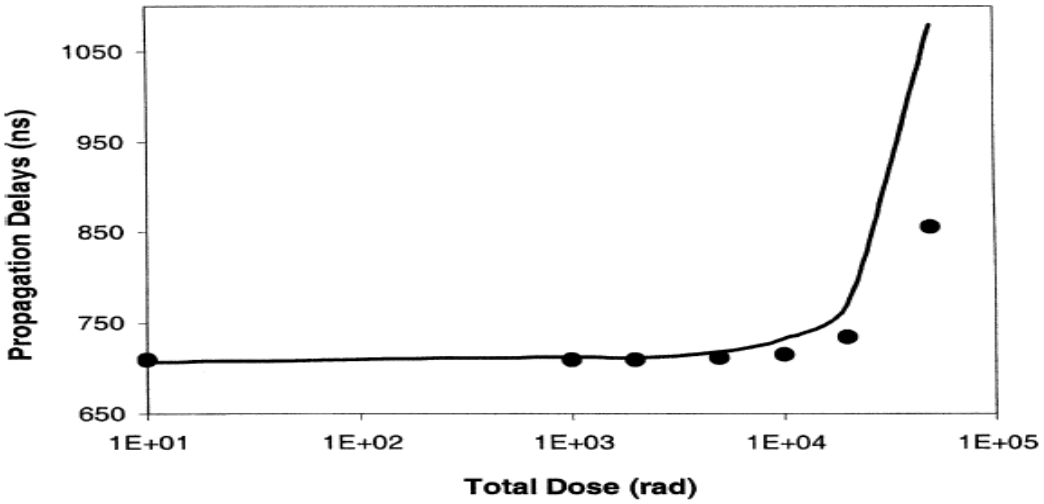

Figure 29: Propagation delay experimental data compared to SPICE simulation predictions for the unbiased case [19]

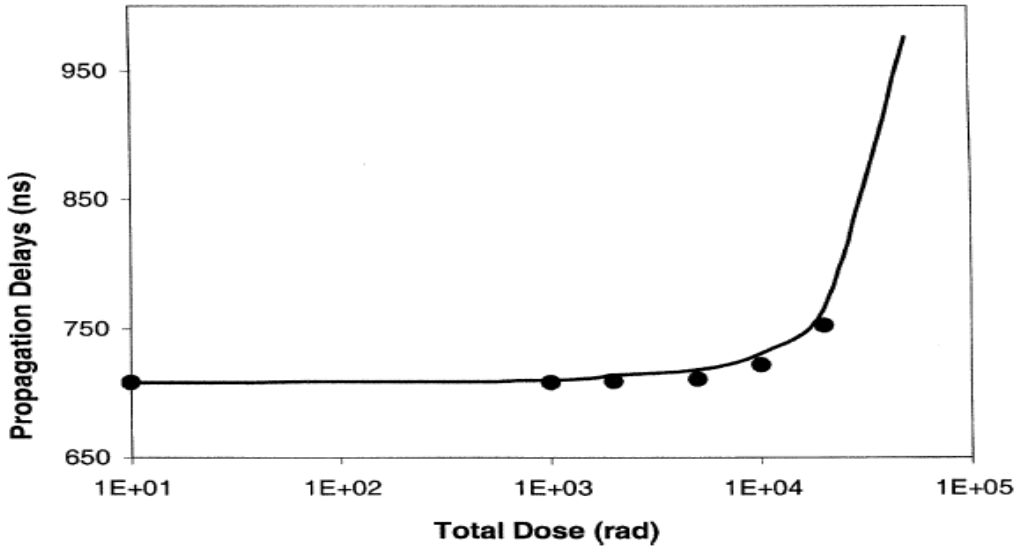

Figure 30: Propagation delay experimental data compared to SPICE simulation predictions for the biased case [19]

Also, one of the factors that affects the propagation delay degradation, is the placement and routing of the VersaTiles in the FPGA fabric. The study in [21] shows that for accumulated total ionizing dose over 20 krad(Si), the placement and routing of VersaTiles in the critical path, seems to play a significant role in determining the percentage of the propagation delay degradation.

3.3 TID testing

Understanding the nature of testing equipment and environment is crucial to successfully simulate the real radiation effect, that is why the determination of the nature and specifications of radiation sources is an important issue. Also, the testing techniques should be standardized by testing procedure to ensure the reliability of the applied test. For total ionizing dose (TID) effect testing, the MIL-STD-883, method 1019 is the standard test that should be followed in TID testing, also Gamma sources (especially cobalt-60 Co^{60}) are commonly used in TID testing.

The MIL-STD-883, method 1019, used in TID testing, emphasizes to use test vectors which should cause the worst radiation effect in the tested devices (worst case test vectors “WCTV”). However, it is very difficult to generate these worst-case test vectors due to the complexity of the designs. Actually, most TID testing don’t use WCTVs due to the difficulty of generating these vectors [7].

Chapter 4

Design for testability

With the tremendous advances in the manufacturing technology of electronic devices, integrated circuits can now have billions of transistors that operate at very high ranges of frequency that can reach the gigahertz range. These advances pose more difficulties for chips testing for several reasons. The increased clock frequency requires automatic test equipment (ATE) that can operate in the same range of circuit under test (CUT). This is because stuck-at faults tests, which are the most common model used in digital circuits, have more effectiveness when they are applied at the circuit's rated clock speed. Those ATE that can operate at these high ranges of frequency, can have a very high cost, which make the testing of such devices very expensive. Also, the increased amount of input and output ports in integrated circuits, especially microprocessors which represents the leading edge in the VLSI technology trend, increase the cost of ATE required to test such devices, and it can also cause a high increase in the testing execution time. Another factor that affects the complexity of chip testing is the increased transistor density: the higher the transistor count, the higher the complexity of testing. This is due to the increase in the internal modules inside the same chip. These internal modules become more difficult to access which in turn makes it more difficult to generate test patterns [22][23].

In the early stages of the history of manufacturing integrated circuits, the design and test phases were regarded as two separate functions, which were done by two separate groups of engineers. During the design phase, the design engineer's job was to ensure that the required functionality is implemented based on the design specifications, without any concerns about how this device will be tested after the manufacturing. While, during the test phase, the test engineer's job was to find a way to test the manufactured device in an effective way within a reasonable time. This approach worked well in the small scale integrated circuits (SSI) where the integrated circuits consisted of combinational circuits or simple finite state machines. But, with the advance in technology and the movement toward the very large scale integrated circuits

(VLSI) era, this approach could not keep up with the increased circuit complexity. Another approach was introduced in the early 1980s to test VLSI devices, which relied on fault simulation to measure the fault coverage of the supplied functional patterns. Functional patterns were developed to test design with long sequential depth, by stimulating all internal states and detecting all possible manufacturing defects. But, this approach failed to increase the fault coverage beyond 80% and the manufactured devices suffered from low quality. That is why it became clear that more attention should be paid to design devices with high fault coverage, as many devices were good from the functionality point of view, but failed in performance point of view due to the high-test cost or low quality. This has led to the introduction of the Design For Testability (DFT) engineering in the industry [24].

The first problem that DFT tried to solve was to find simpler method to stimulate and access all internal states of sequential designs and to increase the fault coverage. Many methods of testability measure and ad hoc testability enhancement were introduced for this purpose. They were mainly used to increase the circuit's controllability and observability. Controllability is defined as the difficulty in setting a certain signal to a certain value. Observability is defined as the difficulty in observing the state of a certain signal. However, these methods failed to reach high fault coverage that exceeds 90% for large designs. This was due to the fact that generating test patterns for sequential circuits is much harder than the case of combinational circuits, even with the aid of these testing methods. The problem in generating test patterns for sequential circuits is due to the existence of many internal states in the design which are difficult to set or observe from external pins. This led to the adoption of structured DFT techniques to control and observe these internal states by providing direct external access to memory elements. These reconfigured memory elements are called "scan cells". By introducing them in the design, the problem of generating test patterns for sequential circuits becomes a problem of generating test patterns for combinational circuits. Many innovative algorithms were already developed to address this problem [24].

Design with scan cells became the most popular structured DFT technique. This design called "scan design" is implemented by replacing all or selected memory

elements with scan cells, each having additional input called “scan input” and one additional output called “scan output”. By connecting the scan output of one cell to the scan input of the next cell, a “scan chain” is created. Many scan designs and scan architectures have been proposed. A design where all the memory elements are transformed into scan cells is called “full-scan design”, where a design with almost all memory elements are transformed into scan cells is called “almost full-scan design”. A design where some memory elements are selected to be transformed into scan cells is called “partial-scan design”. Although, scan designs improved quality, diagnosability, and testability of designs, it is becoming inefficient to test deep submicron on nanometer VLSI designs. because of the increased cost of traditional test schemes using automatic test patterns generation (ATPG) software, and it is becoming hard to maintain high fault coverage for these nanometer designs from chip level to the board and system level. This led to a new approach that combines the scan design with the logic built in self-test (BIST). In this architecture, the circuits that generate test patterns to test the CUT and to analyze the output responses are all embedded in the chip or on the same board where the chip resides. Logic BIST is crucial safety critical and mission critical applications which can be found in defense/aerospace, automotive, and banking industries [22][24].

4.1 Ad-hoc Design for Testability

Initially, numerous ad hoc techniques were proposed to enhance the testability of designs. These techniques involved making local adjustments to designs to improve their testability. While these techniques resulted in some improvements in the testability of designs, their main drawback was that they were local and not systematic. This means that they cannot be generalized for any design and they have to be repeated in a different manner for every design, which will produce unpredictable results [24].

Ad hoc techniques depend on good design practices learned from experience, some of which are [23]:

1- Avoid asynchronous logic feedback:

   Feedback in the combinational circuit can cause oscillation for some inputs, which makes the generation of test patterns by automatic programs difficult

for these circuits. This is because test generation algorithms are only known to work with acyclic combinational circuits.

2- Initializable flip flops:

The initialization of flip flops can be easily done by adding a clear or reset input pin in the design.

3- Avoid large number of fan-in:

Gates with large number of inputs are difficult to observe and the output of such gates are difficult to control also.

One of the most famous ad hoc DFT techniques is test point insertion (TPI). Control or observation points are inserted as test points in the internal nodes of a design. The identification of these test points is commonly done by testability analysis. Figure 31 shows an example of the insertion of an observation point for a logic circuit which has three low observability points. Point OP_2 shows the structure of an observation point which is composed of a D type flip flop and a multiplexer. A low observability point is connected to input 0 of the multiplexer, and all observation points are serially connected into a shift register using input 1 of the multiplexer. A signal which called scan enable (SE) is used as the selector of the multiplexer. When SE has a value of 0 and the clock is applied, the values of the low observability points are captured inside the D type flip flops. Then, when SE has a value of 1, the D type flip flops of OP_1, OP_2, and OP_3 act as a shift register, allowing the observability of the captured values through primary output "OP_output" as shown in the figure [24].

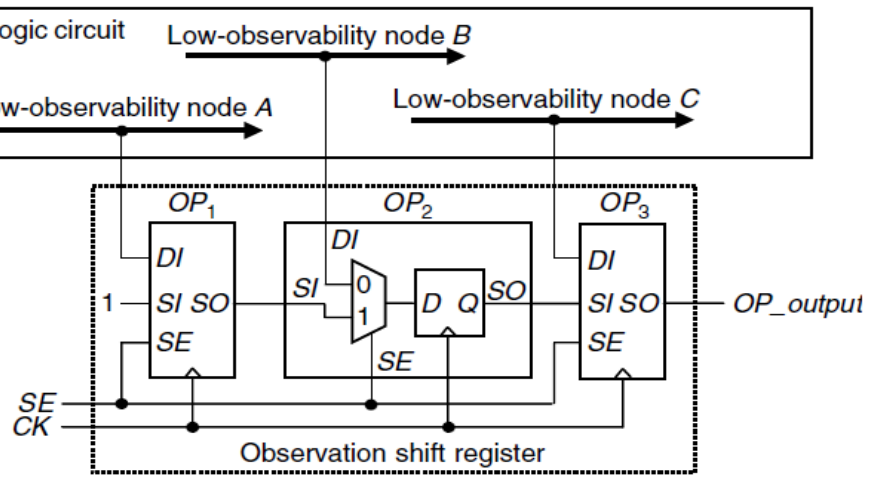

Figure 31: Example of an observation point insertion [24]

Figure 32 shows an example of the insertion of a control point for a logic circuit which has three low controllability points. Point CP_2 shows the structure of a control point which is composed of a D type flip flop and a multiplexer. The original connection between the source and destination ends in a low controllability node is cut, and instead a multiplexer is inserted. A signal which called test mode (TM) is used as the selector of the multiplexer. When TM has a value of 0 normal operation occurs and the value from the source end drives the value at the destination end through input 0 of the multiplexer. When TM has a value of 1 test mode occurs and the value of the destination end is driven from the D type flip flop of the low controllability point through input 1 of the multiplexer. The D type flip flops of CP_1, CP_2, and CP_3 in the low controllability nodes act as a shift register, so that the value required at the destination end can be shifted in the flip flops through the input called "CP_input" as shown in the figure. The drawback of this architecture is the increase in the delay of the circuit. That is why care must be taken in choosing the placement of controlling points especially in the critical path. Also, it is recommended to insert a "scan point" which is a combination of control and observation point to be able to observe the source end as well [24].

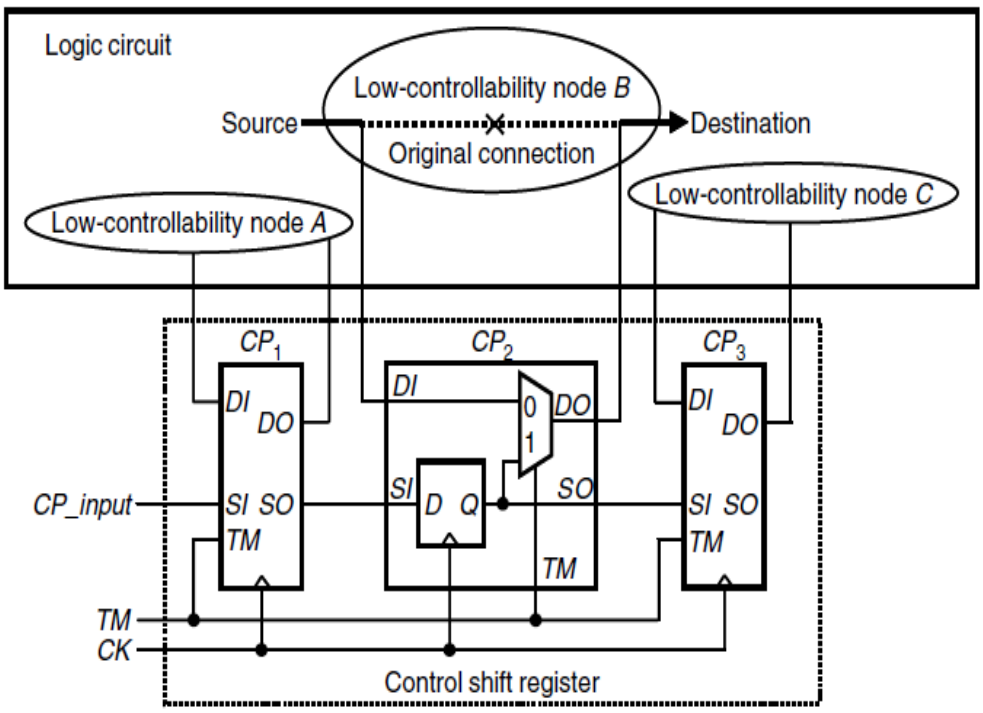

Figure 32: Example of a control point insertion [24]

4.2 Scan design

To overcome the problem of ad hoc DFT techniques being local and not systematic, structured techniques were introduced allowing DFT engineers to follow a methodical process to improve the testability of designs. With structured DFT techniques, the testing process can be easily incorporated and budgeted for as part of the design flow, yielding the desired results. Also, these techniques can be easily automated. In fact, electronic design automation (EDA) vendors provide to engineers sophisticated DFT tools which simplify and speed up DFT tasks. One of the most popular and effective structured DFT technique is the scan design, which can achieve the targeted high fault coverage [24].

Scan design the structured DFT technique that is most widely used. Its implementation includes the transformation of memory elements to “scan cells”, which have an additional input port called “scan input” (SI) and an additional output port called “scan output” (SO), and by connecting the SO of one scan cell to the SI of the next cell, one or more scan chains are created. These scan designs can operate in three modes: normal mode, shift mode, and capture mode. In normal mode all test signals are turned off and the design operates in its original functionality configuration, while in shift and capture mode, a test signal called test mode (TM) is often used to turn on all test related signals [22]. Many scan architectures have been proposed, some of which are described in the following subsections.

4.2.1 Muxed D scan design

In muxed D scan architecture, memory elements or flip flops are replaced with muxed D scan cells, which are composed as shown in Figure 33 of a multiplexer and a D type flip flop. The multiplexer uses a signal called “scan enable” SE as its selector, to select between the data input (DI) and the scan input (SI) [22].

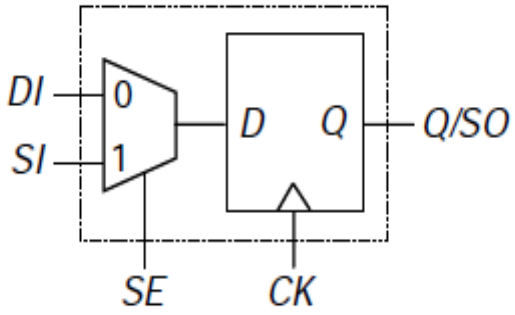

Figure 33: Illustration of a muxed D scan cell [22]

Figures 34 and 35 show an example of a sequential circuit and its corresponding muxed D full-scan scan circuit respectively. The three D type flip flops FF_1, FF_2, and FF_3 in Figure 34 are replaced with three muxed D scan cells SFF_1, SFF_2, and SFF_3 in Figure 35. The data input (DI) ports of the scan cells are connected to the combinational logic like the original circuit. The scan input (SI) ports of scan cells SFF_2 and SFF_3 are connected to the output ports of their previous scan cells SFF_1 and SFF_2, respectively, to form a scan chain. The scan input port (SI) of the first scan cell is connected to the primary input port SI, and the output port of the last scan cell is connected to the primary output port SO. When the scan enable SE has a value of 1, shift mode is on, the scan cells act as a single scan chain, allowing shifting any combination values in the scan cells. When the scan enable SE has a value of 0, capture mode is on, allowing the scan cells to capture the test response from the combinational logic when the clock is applied [22].

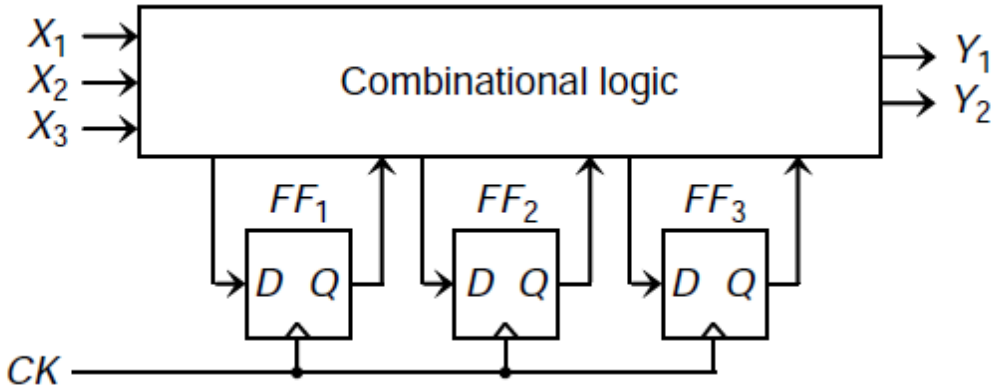

Figure 34: An example of a sequential circuit [22]

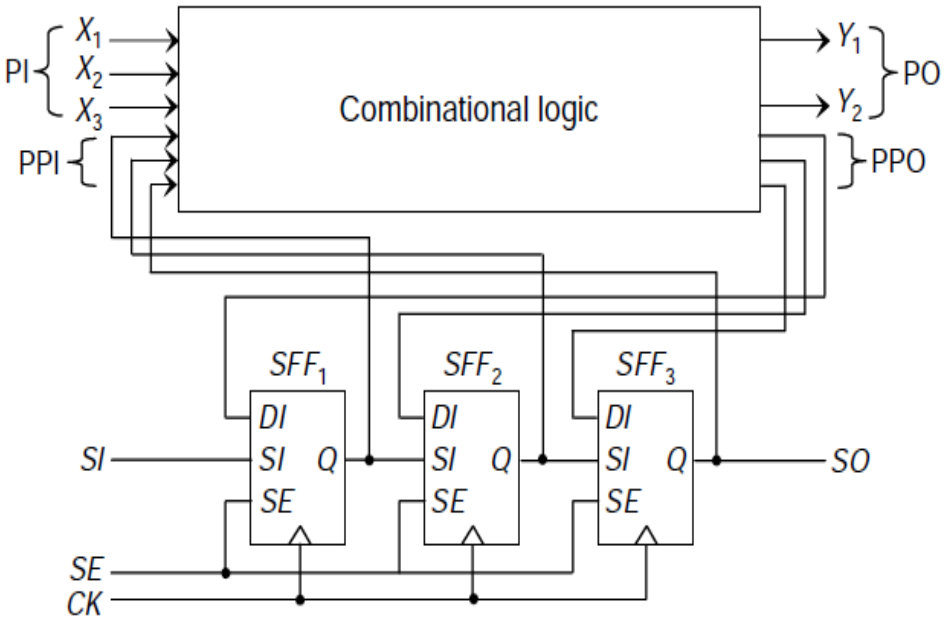

Figure 35: Corresponding muxed D full scan circuit of the sequential circuit in figure 34 [22]

As shown in Figure 35, combinational logic in the scan design has two types of inputs: pseudo primary inputs (PPIs) and primary inputs (PIs). The first type, PPIs, are the outputs of the scan cells connected to the combinational logic. The second type, PIs, are the external inputs to the circuit. Also, the combinational logic has two type of outputs: pseudo primary outputs (PPOs) and primary outputs (POs). The first type, PPOs, are the inputs of the scan cells, where the second type, POs, are the external outputs of the circuit [22].

4.2.2 Clocked scan design

In clocked scan design, memory elements, or flip flops, are replaced by clocked scan cells, which resemble the normal flip flops. The only difference is that they operate by two different clock sources as shown in Figure 36. Like the muxed scan cell, clocked scan cell has two inputs, scan input (SI) and data input (DI). However, unlike the muxed scan cell which uses a multiplexer to select between the two inputs data, the selection of these two inputs is made using two independent clock sources, shift clock (SCK) and data clock (DCK) [22].

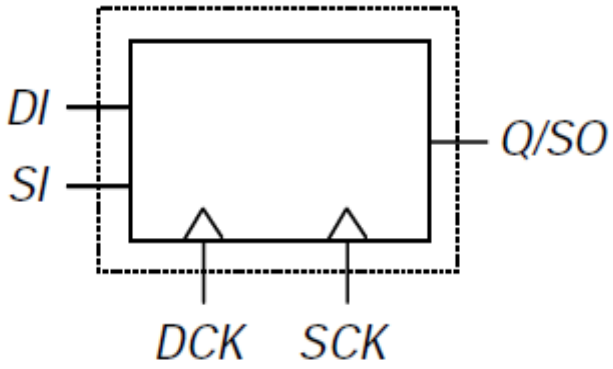

Figure 36: Illustration of clocked scan cell [22]

Figure 37 shows an example of the waveform of the operation of the clocked scan cell. The data clock (DCK) is used in normal or capture mode to capture the data value at the input port (DI), while the shift clock (SCK) is used in the shift mode to shift the data value at the input port (SI) into the cell [24].

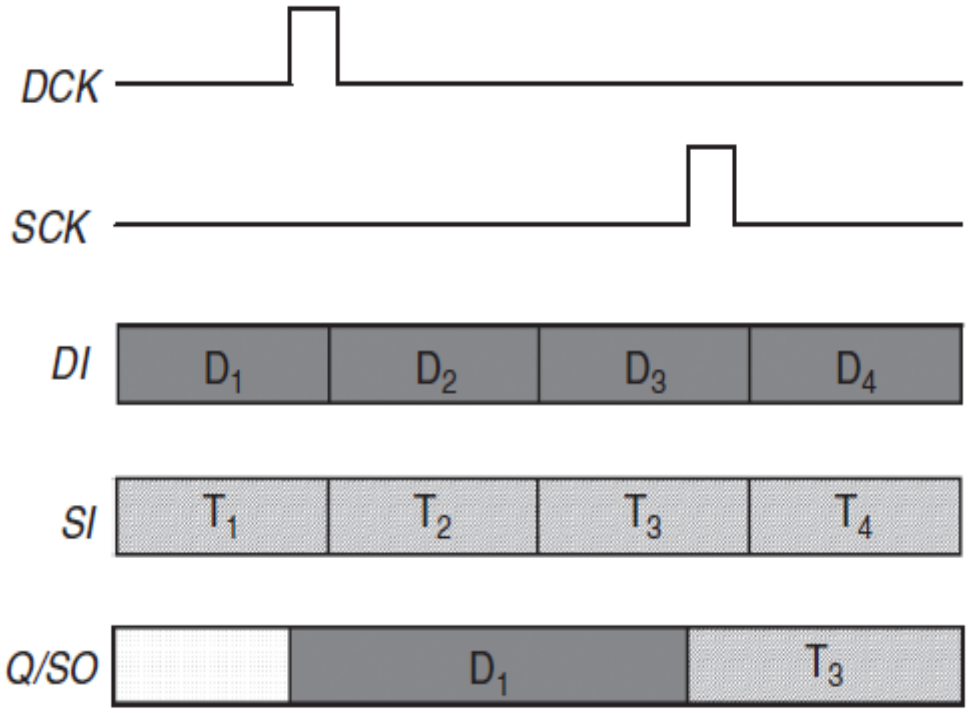

Figure 37: Example of the waveform of the operation of the clocked scan cell [24]

Figure 38 shows the corresponding clocked scan design of the sequential circuit in Figure 34. The three D type flip flops FF_1, FF_2, and FF_3 in Figure 34 are replaced with three clocked scan cells SFF_1, SFF_2, and SFF_3 in Figure 38. The difference

between the two architecture is that in muxed D scan design, a scan enable (SE) signal is used to distinguish between the test and normal operations, while in the clocked scan design, two independent clock sources, data clock (DCK) and shift clock (SCK), are used to distinguish between these two operations [22].

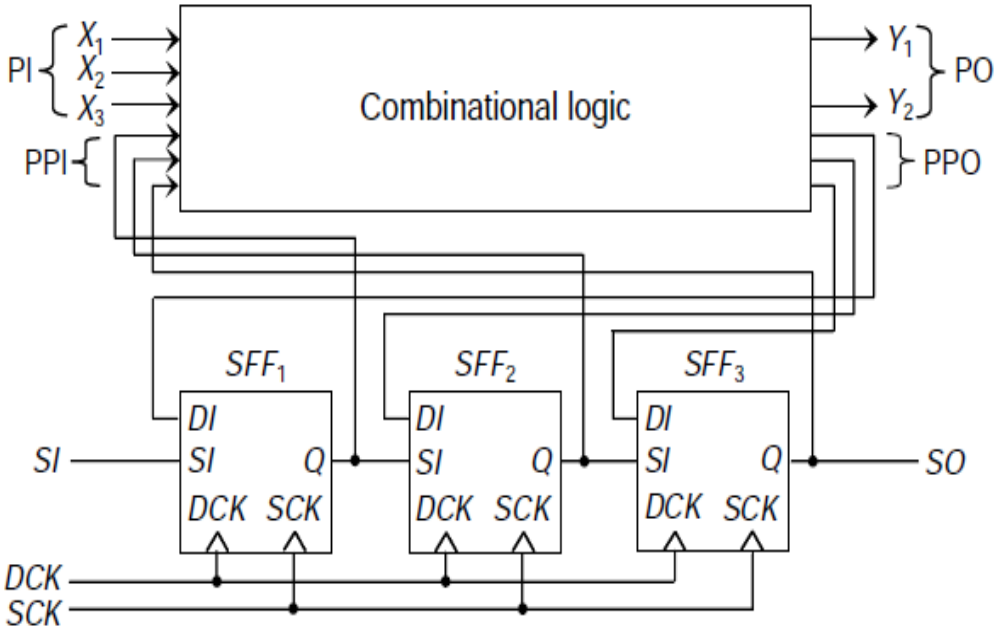

Figure 38: Clocked scan full design of the sequential circuit in figure 34 [22]

The main advantage of the clocked scan architecture is that it eliminates the performance degradation due to the increase in the delay of the data input, like the case of the muxed D scan design, in which an insertion of a multiplexer in the data input is required. However, clocked scan cell requires additional clock routing for the shift clock source [24].

4.2.3 LSSD

Level sensitive scan design (LSSD) replaces memory elements by LSSD scan cells. It is used for level sensitive latch based designs, unlike muxed D scan and clocked scan designs which are used for edge triggered flip flop based designs. Polarity-hold shift register latch (SRL) design, which can be used as an LSSD scan cell, is shown in Figure 39. It is composed of two latches, one master two ports D type latch (L_1), and one slave D type latch (L_2). Clock sources A, B, and C are used to select between the

data input port (D) and the scan input port (I), which drives the scan cell outputs (+L_1) and (+L_2). Either of these two outputs of the scan cell can drive the combinational logic in the design [24].

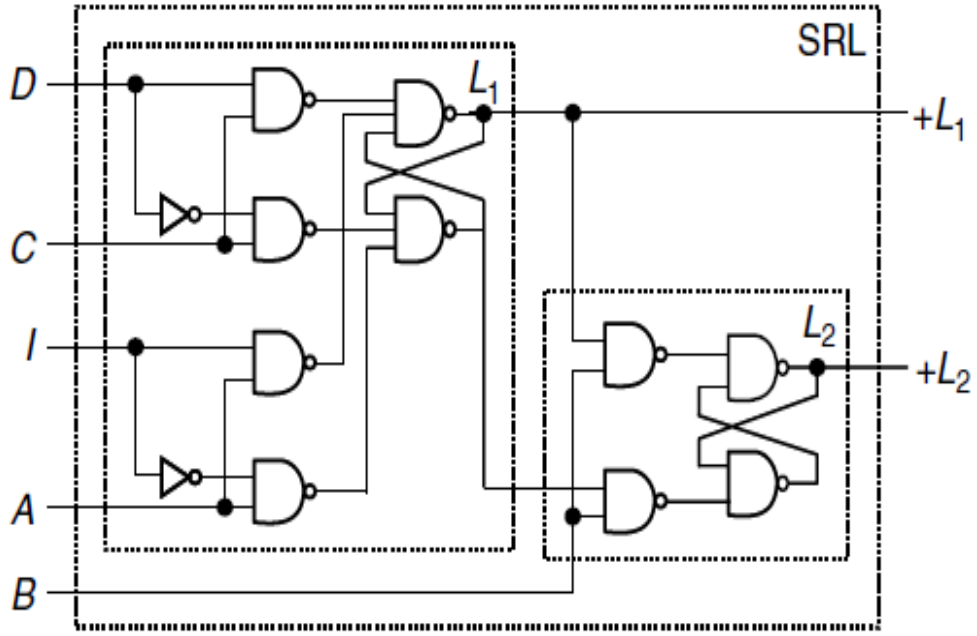

Figure 39: Illustration of the polarity-hold shift register latch (SRL) [24]

Clock sources A, B, and C are applied in a nonoverlapping manner to guarantee race-free operation of the design. If the design is using output port (+L_1) of the scan cell to drive the combinational logic, source clock (C) is used by the master latch (L_1) to latch the data value from the input port (D) and output this value to the output port (+L_1) of the scan cell. On the other hand, if the design is using output port (+L_2) of the scan cell to drive the combinational logic, source clock (B) is used after source clock (C) to latch the data value from the master latch (L_1) and output this value to the output port (+L_2) of the scan cell. An example of the waveform of the operation of the polarity-hold SRL scan cell is shown in Figure 40 [24].

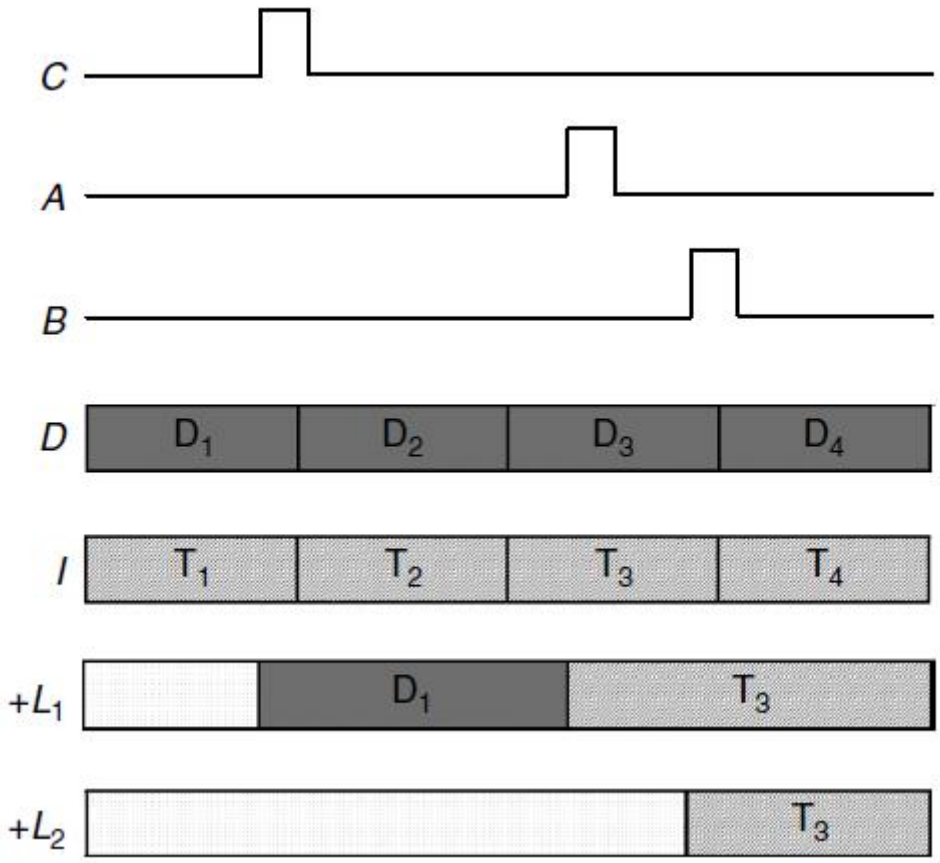

Figure 40: Example of the waveform of the operation of the polarity-hold SRL scan cell [24]

Single latch design or double latch design can be used in the level sensitive scan design. In case of the single latch design, the combinational logic is driven by the output port (+L1) of the master D type latch (L_1), while the slave D type latch (L_2) is only used for scan testing. To prevent combinational feedback loops to occur due to the usage of latches instead of flip flops, there should be at least system clock sources C_1 and C_2. These system clock sources should be applied in a nonoverlapping manner. Combinational logic which are driven by the master latches of the system clock source C_1 should drive the master latches of the second system clock source C_2, and vice versa. Figure 41 shows the corresponding LSSD using single latch design using polarity-hold SRL for the sequential circuit in Figure 34 [22].

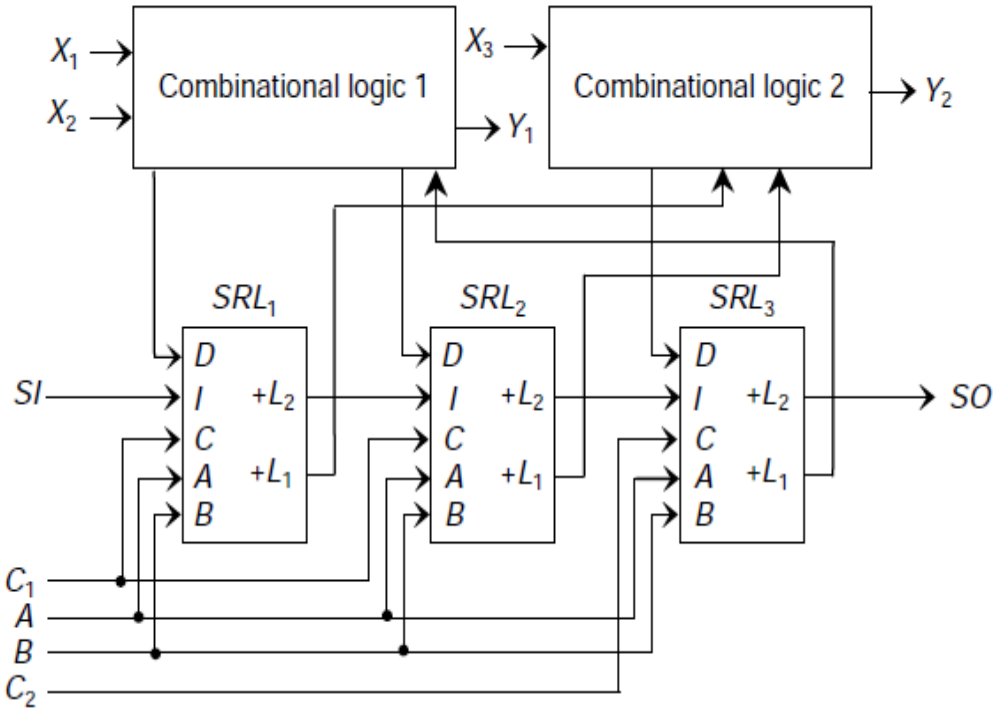

Figure 41: LSSD using single latch design for the sequential circuit in Figure 34 [22]

Figure 42 shows the corresponding LSSD double latch design using polarity-hold SRL for the sequential circuit as previously shown in Figure 34. In normal mode, clock sources C_1 and C_2 are applied in a nonoverlapping fashion, and clock source C_2 is the same as clock source B. The test mode is similar to that of the muxed D scan design. The main difference is that in muxed D scan design a scan enable (SE) signal is used to distinguish between the shift and capture operations, while in the double latch LSSD, the distinction is done by applying nonoverlapping clocks in the clock sources A, B, C_1, and C_2 [22].

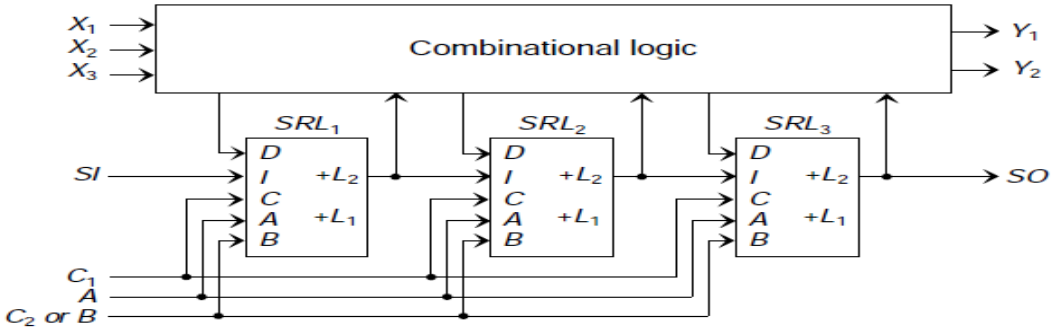

Figure 42: LSSD double latch design of the sequential circuit in Figure 34 [22]

The advantage of using LSSD is the possibility of the insertion of scan into latch based designs, while the major disadvantage is the requirement of additional clock sources routing, which increases the complexity of routing [24].

4.2.4 Enhanced scan design

Enhanced scan design allows the storing of two data bits which can be applied consecutively to the combinational logic that is being driven by the scan cells, thus increasing the capacity of typical scan cell. This feature in enhanced scan design is achieved by the addition of a D type latch to a muxed D scan or clocked scan cell. An example of an enhanced scan design is show in Figure 43 [22].

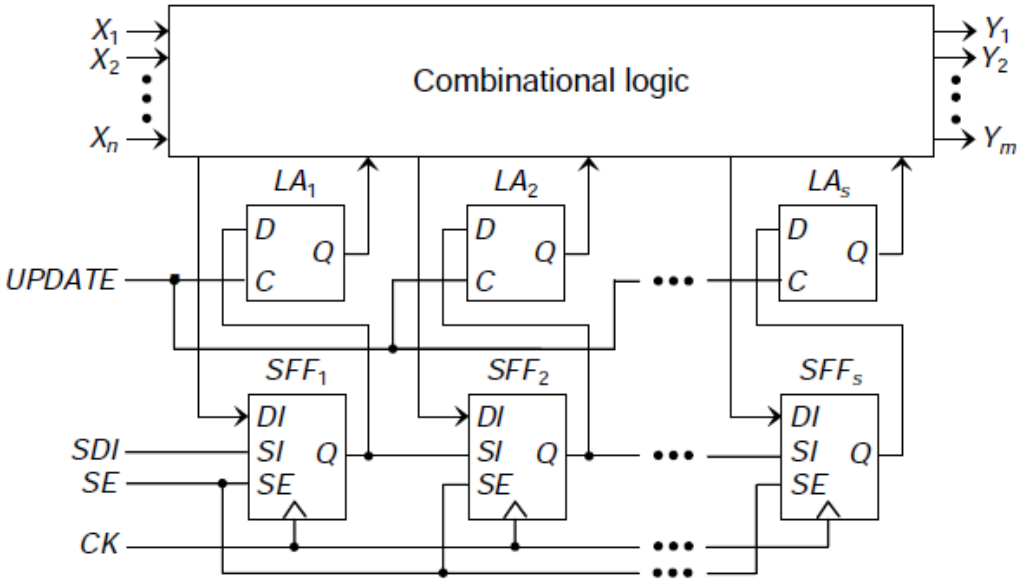

Figure 43: An example of an enahnced scan design [22]

Enhanced scan design is used especially in testing path delay fault, in which it is required to apply a pair of test vectors in an at-speed manner. With the use of enhanced scan design, applying two completely independent and arbitrary vectors to the circuit under test is possible and will increase the detection capability of the delay fault. In contrast to other scan designs that can only use two functionally dependent vectors, which are generated from the combinational logic in testing path delay fault. For the example shown in Figure 43, to apply a pair of test vectors $<V_1, V_2>$, the first

vector V_1 is shifted in the scan cells of the design. Then it is stored, by making the update signal set to a value of 1, into the D type latches. After that, the update signal is set to a value of 0 to keep the values of the first vectors in the latches. The second vector is then shifted into the scan cells of the design. Then, the update signal is set again to a value of 1 to change the stored value in the D type latches from V_1 to V_2, while applying the clock source after exactly one clock cycle to capture the output response of the test vector in an at speed manner [22].

The advantage of enhanced scan design over other architecture is that it allows to increase delay fault coverage because it makes applying two independent pair of vectors to test delay fault possible. However, in order to do that, enhanced scan design requires the implementation of an additional D type latch in the scan cell, and it may be difficult to maintain the timing between the update signal and the clock source in the testing operation. Furthermore, many false paths may be activated during the test operation, instead of functional data paths, which causes a problem of over-test. To overcome this, delay fault techniques which can be implemented with normal scan chains, like launch-on-shift (also called skewed load) and launch-on-capture (also called broad side) are used [22]. Also, it is worth mentioning that Intel Pentium 4 processor used the enhanced scan design

4.3 Logic Built-in self-test (BIST)

Logic built-in self-test (BIST) circuits incorporates all the necessary circuits to test the digital logic of the circuit inside the chip itself or elsewhere on the same board. Logic BIST system commonly composes of four modules as shown in figure 44. The test pattern generator (TPG) unit, which is responsible for automatically generating test patterns to the inputs of the circuit to be tested, the circuit under test (CUT), the output response analyzer (ORA) unit, which is responsible for compacting the output responses of the CUT into a signature, and logic BIST controller, which is responsible for generating BIST timing control signals like scan enable signals and clocks to coordinate the operation of the other units TPG, CUT, and ORA. Output response analysis commonly uses compaction, that is why all storage elements in the ORA, TPG,

and CUT are required to be initialized to a known state and it is not allowed to propagate unknown values from the CUT to the ORA [22].

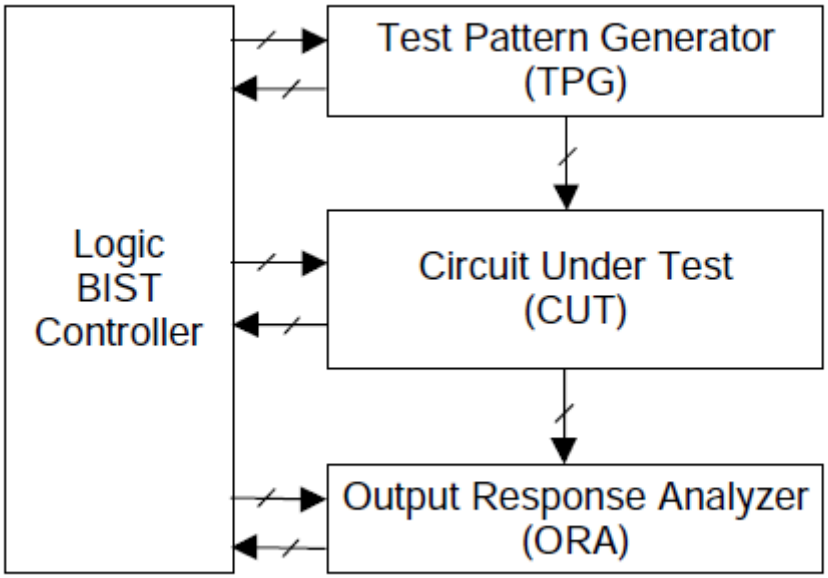

Figure 44: Common logic BIST system [22].

To generate test patterns or test sequences, TPGs commonly uses linear feedback shift registers (LFSRs), they can be used for pseudo random testing, pseudo exhaustive testing, and exhaustive testing. In Exhaustive testing, if an n-input combinational CUT is required to be tested, all possible 2^n test patterns are required to be applied, this guarantees single stuck fault coverage of 100%, however for large value of n, the test time can be huge due to the high number of test patterns to be applied. To overcome this problem, pseudo random testing can be used. In pseudo random testing, a subset of the 2n test patterns are generated and fault simulation is used to calculate the exact fault coverage. Pseudo exhaustive testing generates 2^w test patterns, where $w<k<n$ and each output of the CUT depends at most on w inputs, to eliminate the requirement of the fault simulation and maintain 100% single stuck fault coverage [22].

Multiple input signature registers (MISRs), which is basically constructed form a linear feedback shift register (LFSR) with its inputs connected to an XOR gate, are commonly used in ORAs to compact the outputs response of the CUT. Usually, to decrease the hardware overhead in the ORA, a linear phase compactor, which is composed of a network of XOR gates connected to the inputs of the MISR, is used [22].

4.4 Path delay testing

With the scaling down of dimension as the technology advances, the probability of timing related defects increases, which poses new challenges for test engineers. The stuck at faults was the most favorite fault model for test engineers, however, this fault model cannot work with new design which are characterized with nanometer scale dimension. Stuck at fault check whether the signal designated for test has been set a to a constant value of 1 or 0 and cannot be changed, or in other word it checks if the signal takes an infinite amount of time to rise from 0 to 1 or vice versa. This model fails with current design in which very small delay defects can happen due to process variation, so another fault model must be introduced to address these small defects which should be applied in at speed manner to ensure proper operation of the device under the test. Path delay fault model is used to detect accumulated delay defects in critical paths of a design, which normal static timing analysis (STA) tool fails to fully addresses as more delay variations are caused by the scaling down of dimensions, thus ensuring the proper operation of a circuit within the range of the operating frequency, which will result in the end in an increase of the quality of the manufactured devices [23][25].

4.4.1 Path delay classification

Path delay faults are different from stuck at faults in that not all test vectors applied to test for the designated fault have the same quality, or in other words the detection of the fault is not always guaranteed with all test vectors, some tests detect the fault independently of any other conditions, while some other detect the fault under some conditions. Path delay faults can be classified according to the sensitization criteria into: robust, non-robust, validatable non-robust, and functional sensitizable [26].

To begin with the classification of path delay faults, some terminologies should be introduced first. A gate's "controlling value" is the value of the input of the gate that determines the output of this gate regardless of the values of the other inputs in the gate, and "non-controlling value" is the complement of the "controlling value" for a designated gate. For example, for AND gate, if one input has a value of "0", the output

of this AND gate will be always “0”, so AND gate’s “controlling value” is “0” and its “non-controlling value” is “1”, while for example for an OR gate, this “controlling value” is “1” and the “non-controlling value” is “0”. An “on-input” signal for a path P is a signal that exists on the path P, while an “off-input” signal for a path P is a signal which resides in an input to a gate in path P but not an “on-input” signal.

4.4.1.1 Robust testable path delay faults

In robust sensitization criterion, if there is a fault on a path which can be sensitized under this condition, it is possible to observe this fault independently of other delays on the path’s “off-input” signals. To ensure robust sensitization conditions of a path tested by the sequence of vectors V_1 and V_2, the following conditions should be met. If the on-input of a gate on the path to be tested has a transition from its controlling value to its non-controlling value, the off-input can have any value while applying the first vector V_1 but it has to have a stable non-controlling value while applying the second vector V_2, or it can have a stable non-controlling value during both V1 and V2. If the on-input has a transition from its non-controlling value to its controlling value, the off-input must only have a stable non-controlling value. To illustrate this criterion more, consider the example of the AND gate shown in Figure 45, input “a” is the “on-input” of the path under test, and input “b” is the “off-input”. S1 represents a stable input value of “1” under the sequence of two test vectors V_1 and V_2 used for path delay testing, and X1 represents an unspecified value during the application of the first test vector V_1 (could be 1 or 0) and a stable 1 under the application of test vector V_2. For the first case, the on-input has a 0 to 1 transition which corresponds to a transition from the controlling value to the non-controlling value of the AND gate. To ensure robust sensitization the off-input can have any value while applying the first vector, but must have a stable 1, which is the non-controlling value of the AND gate, while applying the second vector. In case the on-input has a transition from 1 to 0 which is a transition from the non-controlling value to the controlling value of the AND gate, the off-input can only have a stable 1 which is the non-controlling value of the AND gate while applying both vectors V_1 and V_2.

Figure 45: Robust sensitization criterion for an AND gate [26]

Robust testable path delay faults are characterized by the existence of a sequence of test vectors that activates the required transition on the target path to be tested, also satisfying the early mentioned conditions for the off-inputs for every gate in the targeted path. An example of a robust testable path delay fault is shown in Figure 46. Path {a, d, e, g} is a robust testable path, and as shown off-input "a" and "f" can have any value while applying the first vector. However, they must have a value of 1, which is the non-controlling value of the AND gate, while applying the second vector. This is because the on-input has a transition from 0 to 1, which is a transition from controlling to non-controlling value of the AND gate. Off-input "c" must have a stable 0 (S0), which is the non-controlling value for the OR gate, since the on-input has a transition from 0 to 1, which is a transition from non-controlling to controlling value of the OR gate [26].

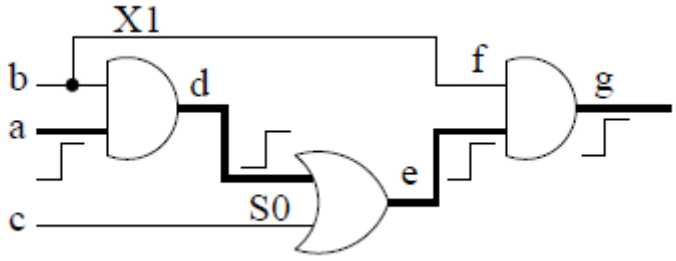

Figure 46: An example of a robust testable path delay fault [26]

4.4.1.2 Non-robust testable path delay faults

In non-robust sensitization criterion, if there is a fault on a path which can be sensitized under this condition, it is possible to observe this fault depending on the delays of other signals outside the path to be tested. The conditions for non-robust sensitization are less strict than robust sensitization. To show this consider the example

shown in Figure 47. The on-input “a” has a transition from 1 to 0, which is a transition from non-controlling to controlling value of the AND gate. However, the off-input “b” does not have a steady value of 1, which is the non-controlling value of the AND gate like the case in robust sensitization. Instead it undergoes a transition from 0 to 1, which is a transition from the controlling to non-controlling value of the AND gate. This results in an observable fault at the output of the gate depending on the arrival time of the transition of the off-input. If the transition of the off-input arrives later than the transition of the on-input, it will mask the propagation of the fault on the on-input to the output of the gate. In this case the test is called invalidated. On the other hand, if the transition of the off-input occurs before the transition of the on-input, the propagation of the fault will be observable at the output of the gate [26].

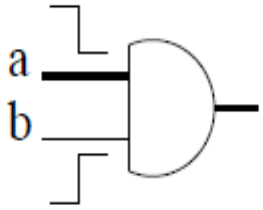

Figure 47: An example of non-robust sensitization of an AND gate [26]

Non-robust testable path delay faults are characterized by the existence of both a sequence of test vectors that activates the required transition on the target path to be tested, and at least one off-input signal satisfies the early mentioned condition in the targeted path. An example of a non-robust testable path delay fault is shown in Figure 48. If the transition in the off-input “d” arrives after the transition in the on-input “c”, the propagation of the fault at “c” will be masked and the test will be invalidated. If the transition in the off-input “d” arrives before the transition in “c”, the propagation fault will be observed at the output “e” [26].

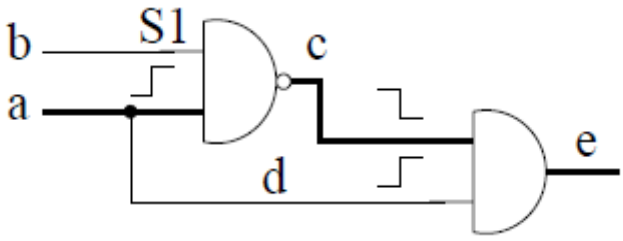

Figure 48: An example of a non-robust testable path delay fault [26]

4.4.1.3 Validatable non-robust testable path delay faults

To explain validatable non-robust testable path delay faults, consider the example shown in Figure 48. Rising transition in signal “d” is the only path that can mask the fault propagation of path {a, c, e} making its test invalidated. If the path in signal “d”, which is a robust path, is tested for delay faults and found that it is faulty, it will make the circuit faulty and the application of test of the non-robust path {a, c, e} becomes unnecessary. But if the path in signal “d” was found not faulty, which will make the transition in signal “d” arrive before the transition in “c”, making the path delay fault observable at the output “e”. The path delay fault in path {a, c, e} is then called a validatable non-robust testable path delay fault [26].

4.4.1.4 Functional sensitizable path delay faults

In functional sensitization criterion, if there is a fault on a path which can be sensitized under this condition, it is possible to observe this fault depending on the delays of other signals outside the path to be tested just like the case in non-robust sensitization criterion. To show this, consider the example shown in Figure 49. The on-input “a” has a transition from 1 to 0, which is a transition from non-controlling to controlling value of the AND gate. The off-input “b” has also a transition from 1 to 0 like the on-input “a”. This results in an observable fault at the output of the gate depending if the transitions of both the on-input and the off-input arrive late [26].

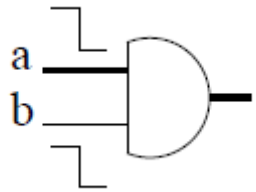

Figure 49: An example of functional sensitization of an AND gate [26].

Functional sensitizable path delay faults are characterized by the existence of a sequence of test vectors that activates the required transition on the target path to be tested, and at least one gate in the target path has a transition from non-controlling value

to controlling value in both its on-input and off-input. An example of a functional sensitizable path delay fault is shown in Figure 50. The path delay fault in path {b, c, e}, which has a rising transition, will always under any sequence of test vectors be considered a functional sensitizable path delay fault. This is because signal “d” will always have a transition from 0 to 1, which is a transition from the non-controlling to controlling value of the OR gate, and so is the transition in signal “c”, and depending on the transition arrival times of signals “c” and “d”, the fault propagation can be observed at the output of the OR gate “e” [26].

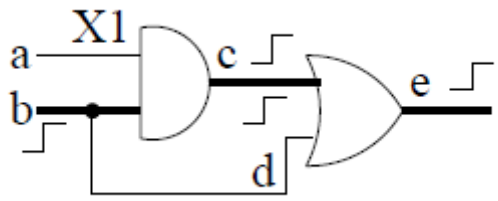

Figure 50: An example of a functional sensitizable path delay fault [26]

4.4.2 Path delay test methodologies

In path delay fault testing, the type of the circuit under test and the DFT used decides how the test is applied. In this section, several path delay test methodologies are introduced.

4.4.2.1 Slow-clock combinational test

This methodology is applicable for combinational circuits or sequential circuits, which are characterized by the presence of flip-flops at their primary inputs and primary outputs. As shown in Figure 51, an input and output latch are added to the input and output of the circuit under test respectively. In normal operation, only one clock source control the latches i.e. system clock, its period is T_c. In testing operation, there should be two independently controllable clock sources which control the input and output latches. These clock sources should have a phase delay or a skew between them. To test the delay of a certain path, a sequence of two vectors V_1 and V_2 must be applied to the circuit under test. The first vector V_1 is applied at time t_0 to the input of the circuit under test, and after a time T_s, which should be longer than the system clock period to

ensure the stabilization of all signals in the circuit due to V_1. The second vector is applied to the input of the circuit under test. The circuit under test must be allowed to run for exactly one clock period of its rated clock T_c. That is why the skew between the two clock sources in the input and output latches should be equal to the system clock period. If there is no fault in the path under test, the output of the circuit due to the second vector V_2 should be observed in the output latch. In case the delay of the path under test exceeds the rated clock period i.e. faulty path, the output of the circuit due to V1 will be observed instead at the output latch [23][26].

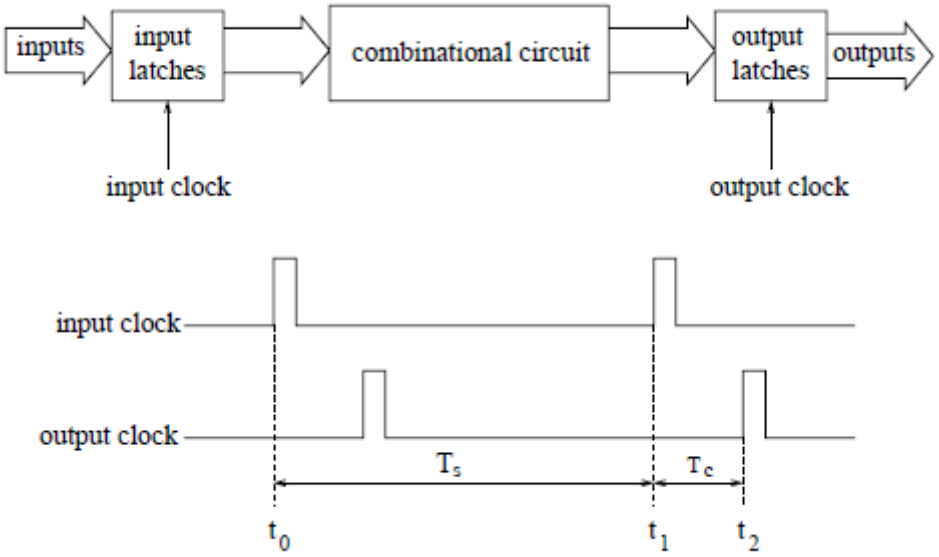

Figure 51: Slow-clock combinational test methodology [26].

4.4.2.2 Normal-scan sequential test

As mentioned before, path delay testing required the application of a sequence of two vectors. In sequential circuits with normal scan circuit i.e. with no hold latches, all primary inputs and internal states are controllable while applying the first, however, when applying the second vector, only the primary inputs are full controllable, and the internal states depends on the previous states due to the first vector. This requires that the second vector applied to the circuit under test be a function of the first applied vector. Two methods are used to generate the second vector as a function of the first vector. Scan-shift test or skewed-load test or launch-on-shift test method, generates the second vector by applying a one bit shift to the scan register, so the internal states of

the second states will be one bit shifted than the internal states of the first vector. The second method called broad-side test or launch-on-capture test, generates the second vector as a function of the first vector, and the internal states of the second vector are generated by propagating the combinational output due to the first vector into the scan registers [22][23][26]. The operation of the two methods is shown in Figure 52.

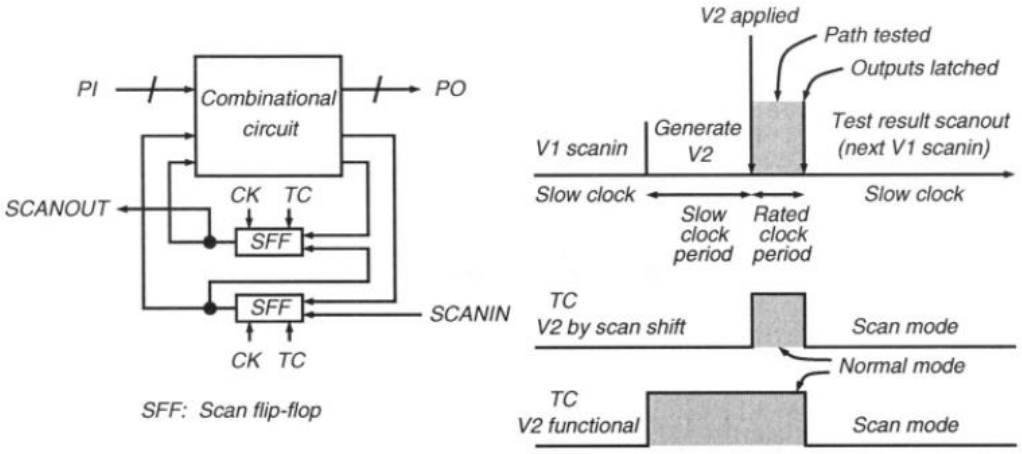

Figure 52: Normal-scan sequential test methodology [23]

In launch-on-shift test, the first vector V_1 is scanned into the scan registers using a slow clock source. After that, one more period of this slow clock is applied to shift the bits in the scan register, and the internal states of V_2 is applied to the scan register. As soon as the primary inputs of the second vector are applied to the circuit under test, the normal operation is on for exactly one rated clock period, and the outputs are latched. Primary outputs are observed and the internal bits of the scan register are scanned out to compare them with the expected outputs to check whether a fault occurred or not [23].

In launch-on-capture test, the first vector V_1 is also scanned into the scan registers using a slow clock source, and then normal mode is on by making the signal test control TC equal to 1. This operation should be also controlled by the slow clock source. As a result, the combinational output due to the first vector is latched inside the scan register which are the internal states of the second vector V_2. While the normal operation is on, one rated clock period should be applied to have the transition of $V_1 \rightarrow V_2$. At the end of this rated clock period, the outputs are latched, and the scan

registers can be scanned out and compared with the expected outputs to check whether there is a fault or not [23].

4.4.2.3 Enhanced-scan test

The normal-scan sequential test restricts the choice of the second vector applied to test a certain path in the circuit to a vector whose internal states are generated from either a shift operation of the internal states of the first vector, or as function from the combinational output due to the first vector. In enhanced-scan test, any arbitrary two vectors can be chosen to test a certain path. This is achieved by the additional latches added to normal-scan design, and the hold signal, which allows the storing of the internal states of the first vector until the application of the second vector. The operation of this methodology is shown in Figure 53 [23].

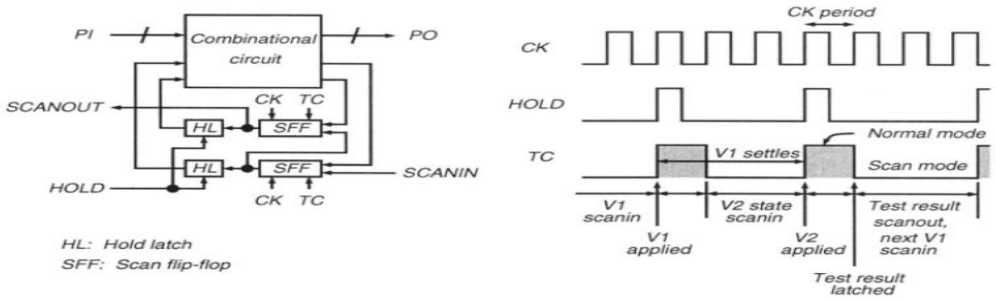

Figure 53: Enhanced-scan test methodology [23]

In this methodology, the first vector's internal states are first scanned into the scan registers via the SCANIN input while setting the test control TC signal to 0. This operation is usually done with a slow clock source to decrease power dissipation and to ensure that no delay fault in the scan paths interfere with the test process. Then, the hold signal is set to 1 to transfer these internal states to the hold latches. The internal states of the second vector are then scanned into the scan registers while the signals due to the first vector stabilizes. After that, the primary inputs of the second vector are applied while setting the hold signal to 1 and the test control to 1 to have a normal operation for exactly one rated clock period. This will result in the required transition V_1➔ V_2 in the hold latches and the inputs of the combinational circuit. At the end of this rated clock period, the outputs are latched, and the internal states are scanned out to be compared with the expected outputs to check if there is a fault or not [23].

Chapter 5

WCTV generation for ASIC and FPGA

MIL-STD-883, method 1019, is the standard that should be followed to test electronic circuit under TID effect. The standard emphasizes the use of worst case test vectors in testing electronic circuits, however, worst case test vectors are not typically used in the testing process, due to the difficulty of generating these vectors for the circuit under test. But, several methodologies have been proposed to generate worst case test vectors for electronic circuits exposed to TID effect. In this chapter, a review of some methodologies that targets both, application specific integrated circuits (ASICs), and field programmable gate arrays (FPGAs), is presented.

5.1 WCTV for ASICs

The methodology in [1] generates worst case test vectors for leakage current failure induced by TID in ASIC cells for both combinational and sequential circuits. The methodology uses normal ASIC design flow tools to generate the worst case test vectors. First, the failure in each cell in the library used is analyzed, and a fault model for every cell is developed. SPICE simulation is used to validate these fault models using the target process transistor parameters and parametric degradation from total dose experiments. Then, a package of VHDL/Verilog functions is developed implementing the fault models mentioned before. After that, two identical instances of netlist of the circuit under test, generated from normal synthesis tools, are added to the testbench, allowing simultaneous simulation of the circuit under test under both irradiation input vectors (I), and post irradiation input vectors (P). Finally, by using normal simulation tools, all possible combinations of irradiation input vectors and post irradiation input vectors are applied to the circuit under test, to find the vectors that will make the circuit exhibits maximum leakage current (max_IL). The testbench setup for this methodology is shown in Figure 54.

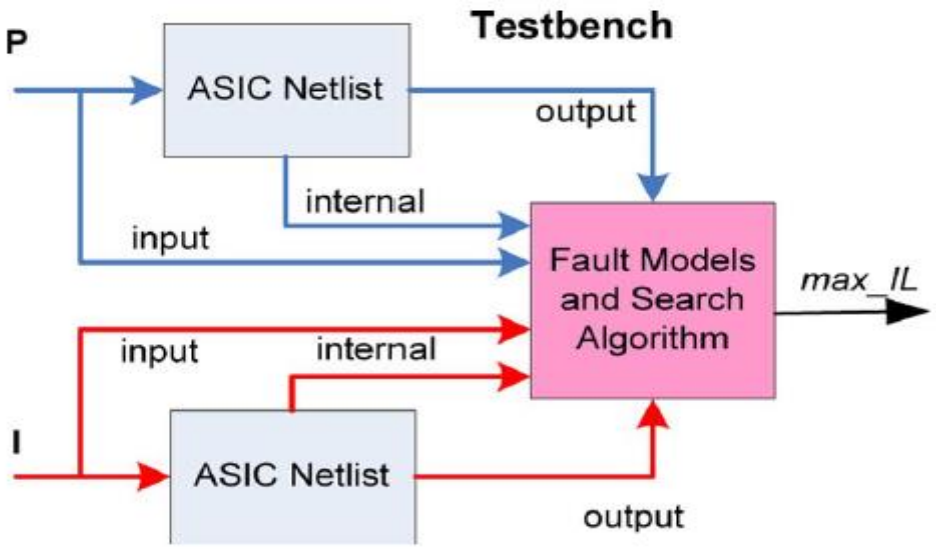

Figure 54: Testbench setup to identify worst case test vectors for leakage current failure in ASICs [1].

Another methodology is proposed in [2] to generate worst cast test vectors for logic failure in combinational circuits of ASIC exposed to TID effect. The methodology starts with the register transfer level (RTL) VHDL or Verilog of the design, then by using synthesis tool, a netlist composed of the standard cells found in the library used is generated, which can be expressed in VHDL or Verilog. Each cell in the generated netlist is then analyzed and a fault model is developed based on the logic failure analysis of the cell, and this model is validated using SPICE simulation with the transistor parameters extracted from the technology used in the synthesis and the transistor parametric degradation from total dose experiments. Depending on the cell, the fault model can be stuck at 0 or stuck at 1. A ranking system is then developed to order the cells per their sensitivity to TID effect induced by radiation. The methodology then targets the cells with the highest sensitivity, and automatic test pattern generation (ATPG) tools like Mentor Graphics FastScan is used to insert a stuck at 0 or stuck at 1, depending on the targeted cell and its fault model, at the output of the cell. The ATPG tool will generate input test patterns, which will be the WCTV of the design under test, and the fault will manifest at the primary output of the circuit.

The advantage of this methodology, is that it decreases significantly the time needed if exhaustive search is used for the identification of WCTVs, especially large design with high number of inputs and large number of transistor count, for example the exhaustive search for WCTV of 64x64 multiplier requires 2^{256} combinations of

irradiation and post irradiation input test vectors to be simulated, which is impossible to do. However, the disadvantage of this methodology, is that it only applies to combinational circuits of ASIC, but most ASIC design are composed of sequential circuits.

A new methodology is proposed in [3] that makes use of genetic algorithm in the identification of WCTV for leakage current failure in ASICs exposed to TID effect. This methodology also develops a fault model for each cell in the library used, but in this time the fault model includes the effect of the leakage current induced in the field oxide, and these fault models were implemented using VHDL functions. The design is first synthesized using normal synthesis tools, and a netlist written in Verilog is generated. The synthesized netlist in Verilog along with the fault models of each cell mentioned before written as VHDL functions are simulated in Mentor Graphics Questa simulation tool. A smart search algorithm based on genetic algorithm principles is then used instead of the exhaustive search method which can take very long time in designs with large number of inputs for the identification of the WCTV. This search algorithm is written in System Verilog simulating the design under test using normal simulation tools. The authors compare between the exhaustive search algorithm and the search algorithm based on genetic algorithms for an example design of an 8x8 multiplier. The search algorithm based on genetic algorithm significantly reduced the time for the identification of WCTV to an order of a few seconds compared to a whole two days that the exhaustive search require to generate WCTV for a simple design like an 8x8 multiplier.

This methodology significantly reduced the time needed for the identification of WCTV of designs, compared to the time needed by the exhaustive search algorithm which can be impossible in some cases where the design is characterized by a large number of inputs and a high number of transistor count. And although, the fault model includes the effect of local oxidation for silicon (LOCOS) which is not used in modern technologies, the authors mention that the fault model is still applicable for a more used technology like shallow trench isolation (STI).

In [4] another methodology is proposed for the identification of WCTV for logic faults in ASIC exposed to TID effect. This methodology begins also with the

development of fault models for logic failure for each cell in the library used, but this methodology includes process technologies that exhibit field oxide (FOX) edge leakage which wasn't discussed in the other methodologies. Including the FOX leakage in the fault model of the cells will increase the accuracy of the failure analysis of cells, because as the technology advances, the FOX leakage becomes the dominate contributor to the device failure. These new fault models are then implemented using VHDL or Verilog, and a logic simulator like Mentor Graphics ModelSim is used for the identification input vectors combination satisfying the excitation and manifestation conditions. A ranking system is then developed to order each cell according to their sensitivity to logic failure due to TID effect, and by targeting the cells with the highest sensitivity by inserting a stuck at 0 or stuck at 1, depending on the fault model of the designated cell, ATPG software tool like Mentor Graphics FastScan can be used for the identification of inputs vectors that manifest these stuck at faults at the primary outputs of the design under test, and these vectors will be the WCTV for this design if it is guaranteed that no logical masking happens between the vectors. The flow diagram of the mentioned methodology is shown in Figure 55.

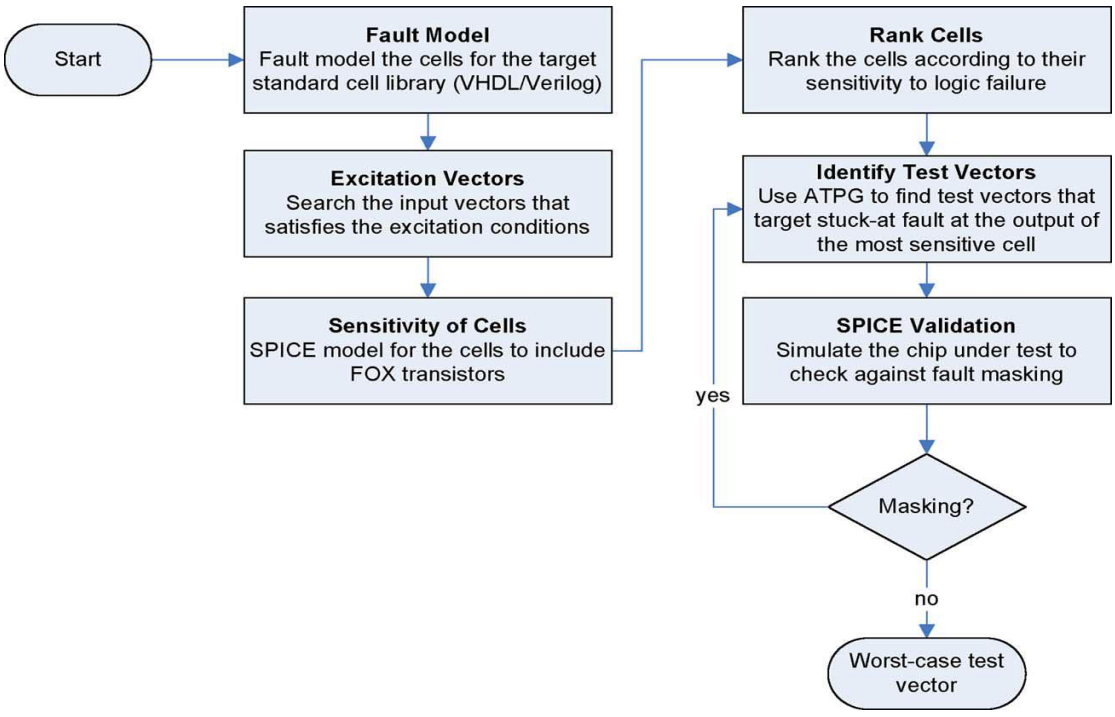

Figure 55: Flow diagram to identify worst case test vector for ASICs [4]

A new methodology designed especially for ASIC composed of sequential circuits is proposed in [5]. The methodology is used for the identification of WCTV for leakage, logic, and delay failure of sequential circuits in ASIC exposed to TID effect. The difference between combinational circuits and sequential circuits, is that the later are characterized by the presence of memory elements. So, in order to test sequential circuits for a single fault, a sequence of test vectors is required to be applied to the circuit to initialize the memory elements to a known state, as opposed to the case of combinational circuits where a single test vector can be applied to the circuit to test it for a single fault. The authors classify sequential circuits into two broad categories: cycle-free circuits, which are characterized by the absence of feedbacks between the flip-flops making the length of test vectors sequence bounded by its sequential depth which is determined by the number of flip-flops in the circuit, like pipelined sequential circuits, and cyclic circuits, which are characterized by an undefined sequential depth which make the upper limit of test vectors sequence also undefined, like finite state machines circuits.

For cycle-free sequential circuits, the authors report that flip-flops are not the dominant contributor to the circuit failure due to TID effect, instead the combinational logic existing between flip-flops are the dominant contributors. In the methodology, an equivalent combinational circuit is constructed from the original sequential circuit by removing its memory elements, and then fault model of each cell is developed to rank the cells in order of their sensitivity to failure induced by TID effect. Then, ATPG tool is used to generate input test vectors to exhibit stuck at 0 or stuck at 1 fault at the outputs of the most sensitive cells in the design depending on the developed fault models. These input test vectors are the WCTV for the designated failure of the original sequential circuit. These vectors must be applied for a number of clock cycles equal to the number of the flip-flops in the design under test to fill the memory elements with the required states. For cyclic sequential circuits, the equivalent combinational circuit is also constructed, but this time its inputs are the primary inputs of the original circuit and the registers of the previous state. ATPG tool is also used to generate test vector sequence that will induce a stuck at 0 or stuck at 1 faults at the outputs of the most sensitive cells

in the design, and the fault will be exhibited in the primary outputs of the original circuit.

Although this methodology was the first to address generation of WCTV especially for sequential circuits, as the generation of these vectors is very hard due to difficulty in controlling the internal states of the memory elements in sequential circuits, however, this methodology cannot be applied to large designs with large number of memory elements, because it will be more harder and even impossible to generate input vectors sequence that will initialize memory elements to known states.

Another effort is presented in [6] to generate WCTV for delay failure in ASIC exposed to TID effect. The methodology starts first with introducing a novel fault model for delay failure in sequential circuits. The methodology explains that the maximum frequency that a sequential circuit can operate depends on the maximum delay in the combinational logic between any two flip-flops or what is called critical path. In order to have a delay failure induced by TID effect, the delay in the combinational logic in a chosen critical path must exceed the slack made by the operating frequency. The methodology generates WCTV using two steps. The first step is to identify number of critical paths that can be candidates for the testing, these paths should have the longest delay between primary inputs and primary outputs, and by using directed graph and the developed fault models, the candidates critical paths for testing can be identified. The second step is to identify a set of irradiation and post irradiation input vectors that will exhibit maximum delay in the paths generated from the first step. For this step, an algorithm based on genetic algorithm is developed to identify the test vectors maximizing the delay of the candidates critical paths generated from the first step using the developed fault model.

The advantage of this methodology is that it didn't rely on exhaustive search for the generation of WCTV, which in large design with high number of inputs and sequential circuits with large number of states can take very long time to implement or it can be even impossible to simulate such huge number of possibilities. Instead, the methodology used genetic algorithm basics to develop a search algorithm to generate WCTV, which in this case will take much less time to complete compared to the

exhaustive search method. Giving this, the methodology can be applied to large designs which are characterized by large number of inputs and internal states.

5.2 WCTV for FPGA

All the mentioned methodologies above depended on the transistor level circuit information, which can be easily extracted in case of a design using standard cell based ASIC, however, this information are proprietary and cannot be shared with normal users in case of FPGAs. That is why, it has been hard to identify WCTV for FPGA exposed to TID effect.

There has not been any effort to identify WCTV for FPGA exposed to TID effect except in [7], which proposes a methodology to identify WCTV for delay failure in flash-based FPGA. The authors built their methodology on the fact that floating gate transistor, which is the switch element in flash-based FPGA, is the dominant factor in the degradation of flash-based FPGA induced by TID effect. Since the transistor level circuit of each cell in the FPGA cannot be shared with normal user, the state of each floating gate transistor (whether it is used or not) in each cell cannot be known, that is why the methodology depends on probability analysis to estimate the number of floating gate transistors used in every cell in the FPGA. The authors then explain that in order for a delay failure to manifest in the operation of the FPGA, the delay of the combinational logic between two flip-flops must exceed the slack value for the operating frequency of the FPGA. The identification of WCTV is done through three steps. First, by using the static timing analysis (STA) tool of the FPGA vendor, some candidates critical paths with the highest delay are identified. Second, from these critical paths, the path with the highest estimated number of floating gate transistors and the highest estimated probability to occur is chosen. Third, ATPG tool like Mentor Graphics FastScan is used to identify input test vectors that will allow a signal to toggle its value from 0 to 1 without being masked by other signals in the chosen path. The toggling must manifest its value at the primary output of the circuit under test to be able to observe the fault. These input test vectors are the WCTV for the design implemented in the FPGA.

Although this methodology was one of its kind, because it was the first effort to identify WCTV for FPGA design, and it only depends on the information that the FPGA vendor give to normal users, however, this methodology only applies to combinational circuit of sequential circuits characterized by a flip-flop at the input and a flip-flop at the output of the circuit, and that is very rare to find in today's design, as most of the designs consists of complex sequential circuits with many flip-flops and internal states.

Chapter 6

Methodology

A novel methodology is proposed to generate WCTV for flash-based FPGA exposed to TID effect. The methodology is based on the delay failure analysis and fault model developed in this effort [7]. The authors have developed methodology to generate WCTV, but only for combinational circuit or sequential circuits characterized by the presence of flip-flops at the primary inputs and outputs of the circuit under test. However, this is a very rare case as most designs contain complex sequential circuits. In this thesis, a novel methodology is proposed to target complex sequential circuits by adopting DFT techniques which originally used for testing complex ASIC designs. The methodology is verified experimentally by implementing different designs on MicroSemi ProASIC3 and exposing them to total ionizing dose using Cobalt 60 facility.

6.1 Failure analysis

For a synchronous circuit, the maximum operating frequency is determined by modeling the design into a combinational circuit between the source and destination registers as shown in Figure 56. The clock period must satisfy the following equation:

$$T_{clk} \geq t_d + t_{cq} + t_{su} \quad (1)$$

where $t_d$is the propagation delay of the combinational circuit between the source and destination registers, $t_{cq}$is the clock to output delay of the source register, and t_{su} is the setup time of the destination register [7].

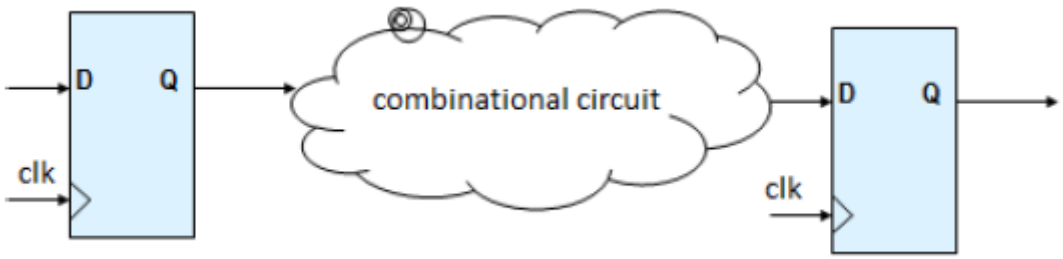

Figure 56: Synchronous circuit's model [7].

Depending on the value of the setup slack, delay failure can occur in the target design. If the setup slack is positive, then the circuit will operate normally under the specified clock period. However, if the setup slack is negative a delay failure will occur in the circuit operating with the specified clock period. The decrease in the setup slack can be expressed as:

$$\Delta S_{su} = -\left(\Delta t_d + \Delta t_{cq} + \Delta t_{su}\right) \quad (2)$$

as seen from the above equation, the decrease of the setup slack depends on the increase in the propagation delay of the combinational circuit, the clock to output delay of the source register, and the setup time of the destination register.

To identify the different factors contributing to the increase of the delays of the parameters mentioned in (2), an analysis of the cells composing the FPGA under test must be done. In this thesis MicroSemi ProASIC3 flash FPGA is the chosen FPGA for the analysis. This FPGA consists of a sea of logic cells called VersaTiles. Each VersaTile can be configured as either a three-input lookup table (LUT), or as a D-type flip-flop/latch (with or without enable) as shown in Figure 57 [27].

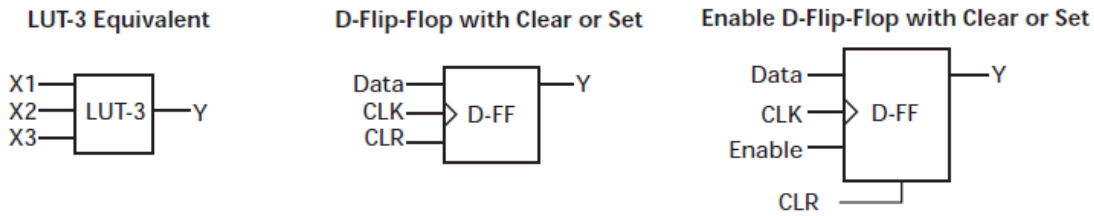

Figure 57: Various configurations of VersaTile [27]

The configuration of Versatiles is done by programming the 31 FG switches in each VersaTile as shown in Figure 58. The transistor level schematic of these FG switches is shown in Figure 59 [7].

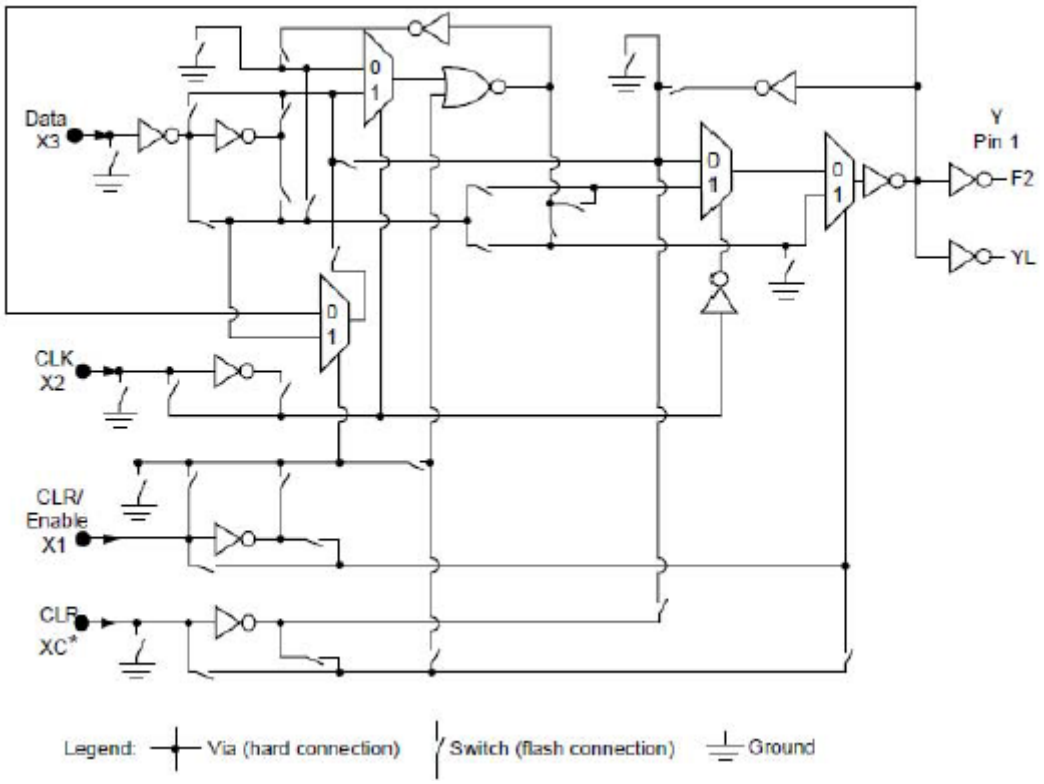

Figure 58: Schematic diagram of a VersaTile [7]

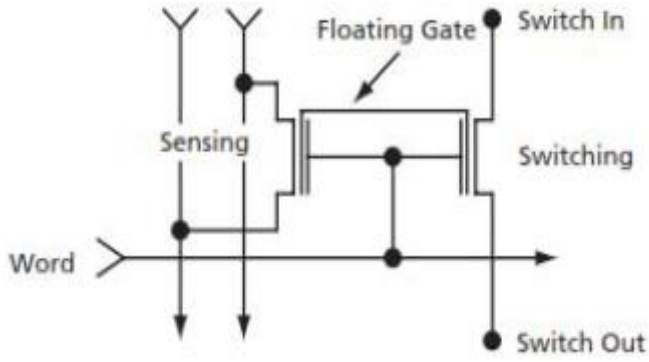

Figure 59: Transistor level of a FG switch [7]

The exact configuration of each FG switch in a VersaTile is proprietary and cannot be shared with normal user. However, the analysis in [7] indicates that there may be one, two, or three FG switch in the path from the input of the VersaTile to the output. The rest of the FG switches are used for the connection of other nodes to the ground. Furthermore, in the delay failure analysis in [7], FG switches are assumed to be the dominant factor in the increase of the delay parameters mentioned before in equation (2) due to TID effect.

In addition to the FG switches found in each Versatile, which can include one, two, or three FG switches in the path from the input to the output, FG switches can also be found in the interconnection between different VersaTiles. These switches are used to connect VersaTiles and larger functions with any of the four-level routing hierarchy. Therefore, the decrease in the setup slack due to TID effect is dominant by the degradation of the FG switches found in the paths of setup time of the destination register, clock to output delay of the source register, combinational circuit between the source and the destination register, and the interconnection between the VersaTiles. It has been found that the clock to output path contains one FG switch, and the setup time path contains two FG switches. Each cell in the combinational circuit can have from one to three FG switches depending on its configuration based on the required functionality of the cell. The interconnection between the cells can have any number of FG switches. Therefore, the total decrease of the setup slack due to TID effect taking only in consideration the increase in the delay of FG switches can be expressed by the following equation:

$$\Delta S_{su} = -(\Delta t_{sw} \times N + 3) \tag{3}$$

where Δt_{sw} is the increase of the delay in the FG switch due to TID effect, and N is the estimated number of FG switches in the combinational circuit between the source and destination registers and the interconnections between the cells. There is an addition of three FG switches to the estimated number of FG switches to account for the switches in the clock to output and setup time paths [7].

6.2 Fault model

To identify WCTV for a design, a fault model must be developed, which abstracts the targeted failure at a certain level of circuit representation. In this thesis, the fault model developed in [7] is used to identify WCTV for sequential circuits in flash-based FPGA.

As it has been established before, the increase in the delay of the FG switches is the dominant factor in the decrease in the setup slack due to TID effect. However, the exact number of the FG switches in the combinational circuit between the source and the destination registers, and the FG switches in the interconnections between the

cells in a certain path i.e. N cannot be exactly determined as they are proprietary to the FPGA vendor. This is because the number of FG switches in a VersaTile depends on the required functionality to be implemented in this VersaTile. Several configurations of the switches in a certain VersaTile can result in the same functionality. Furthermore, the four-level hierarchical routing makes it impossible for the normal user to deterministically estimate the exact number of FG switches in the routing nets. Thus, the authors in [7] followed an approach based on probability to find the total estimated number of FG switches in a certain path i.e. $\widehat{N}$.

To determine an estimated number of FG switches for a given cell i.e. $\hat{k}$, every configuration of the switches in the VersaTile that results in the same functionality must be analyzed. The probability that the cell has a particular number of FG switches is the number of configurations that results in this number of switches divided by the number of the total possible number of configurations that results in the same functionality of the cell. For example, NOR3 cell has three inputs X1, X2, and X3. There could be 28 different configurations of FG switches inside the VersaTile that will result in a functionality of a three input NOR gate. The estimated number of FG switches from every input to the output of the cell is shown in Table I. For the path from input X1 to output Y, the most probable number of FG switches i.e. $\hat{k}$ is equal to 1 with a probability of 15/28. The most probable number of FG switches from input X2 to output Y equal to 2 with a probability of 27/28. For input X3 to output Y path the most probable number of FG switches is 3 with a probability of 20/28. Thus, the most probable estimated number of FG switches for NOR3 $\hat{k}$ is equal to 2 and it is along the path from input X2 to output Y [7].

Table I

Estimated number of FG switches along the paths from every input to the output of a NOR3 cell [7]

Input	Output	Estimated number of FG switches ($\hat{k}$)	Probability
X1	Y	3	13/28
X1	Y	1	15/28
X2	Y	1	1/28
X2	Y	2	27/28
X3	Y	2	8/28
X3	Y	3	20/28

On the other hand, for an OR3 cell, there is only one configuration of the FG switches in the VersaTile to have a functionality of a three input OR gate. That is why in this case the exact number of FG switches along the paths from its input to the output of the cell can be determined. The number of FG switches along the paths of every input to the output of the cell is shown in Table II [7].

Table II

Estimated number of FG switches along the paths from every input to the output of an OR3 cell [7]

Input	Output	Estimated number of FG switches ($\hat{k}$)	Probability
X1	Y	1	1
X2	Y	2	1
X3	Y	2	1

This uncertainty in determining the exact number of FG switches along the path of the combinational circuit between the source and destination registers, and the routing nets between the VersaTiles, results in an estimated increase in the delay along a chain of VersaTiles, which can be given by the following equation [7]:

$$\Delta t_d = \Delta t_{sw} \times \widehat{N} \tag{4}$$

The experiments conducted in [7] reveals that there is an increase in the delay along a chain of VersaTiles with the increase of $\widehat{N}$ at different total dose level below 65 krad(Si). The experiments also show that the relationship between the increase in the

delay and the increase of the estimated number of switches is nonlinear for almost all cases. Hence, in this methodology, critical paths with the highest number of estimated FG switches along the path are targeted for delay testing to identify WCTV for sequential circuits of flash-based FPGA exposed to TID effect.

6.3 WCTV generation for sequential circuits

In the previous effort [7] a methodology has been proposed to generate WCTV of flash-based FPGA exposed to TID effect. However, this methodology is only limited to combinational circuits or sequential circuits characterized by the presence of flip-flops at the primary inputs and outputs of the circuit under test. These cases are very rare to find as most designs consist of complex sequential circuits. In this thesis, a new methodology is proposed to generate WCTV for sequential circuits in flash-based FPGA using DFT techniques which are usually used for testing manufacturing defects in ASIC chips.

Generating test patterns for sequential circuits is harder than generating test patterns for combinational circuits. This is because in sequential circuits, in order to test a certain fault e.g. path delay fault, not only a pair of vectors must be applied to the primary inputs of the circuit under test, but also the internal states of registers in the sequential circuit must be controlled and initialized to a determinant value. Controlling these internal registers is difficult and maybe impossible for complex designs with high number of registers [24]. To overcome this issue, test engineers often rely on structured DFT techniques to increase the controllability and observability of these internal registers. The increase in the controllability and observability is done by replacing normal registers with scan cells. Despite the fact that DFT techniques were widely used for decades in testing complex sequential circuits, they were never used in radiation testing to generate WCTV for designs under test. Furthermore, DFT techniques were usually used in testing ASIC devices, however, DFT is never meant for FPGA designs that is why scan cells are not included in the FPGA macro libraries.

To generate WCTV for delay failure of sequential circuits in flash-based FPGA, path delay fault is used. Path delay fault is used to detect accumulated delay defects in critical paths of a certain design. So, in this methodology a number of critical paths of

the design under test is chosen based on the maximum estimated number of FG switches along the path.

There exist several types of path delay faults some of which are mentioned in section 4.4.1. In this methodology, robust testable path delay fault is chosen. This is because WCTV will be the input test patterns that will stimulate delay fault in the critical path with the highest estimated number of FG switches along the path and manifest this fault in the primary output of the circuit, and there must be no other delay faults which can interfere with the transition in the targeted path. This will ensure an observation of the delay fault for only the targeted path in the primary output of the circuit. Furthermore, to ensure correct observability, this methodology even put more restrictions on the conditions for robust testable path delay mentioned in section 4.4.1.1 by making the off-inputs of gates along the path have only a steady non-controllable value. To illustrate the difference between the two conditions consider the example shown in Figure 60. In a), normal robust sensitization conditions are shown for an AND gate. If the on-input has a transition from the controlling value to the non-controlling value, the off-input can have any value during the application of the first vector and a non-controlling value during the second vector. On the other hand, if the transition of the on-input is from the non-controlling value to the controlling value, off-input must have a steady non-controlling value during the application of the two vectors. However, in b) whether the on-input has a transition from the controlling value to the non-controlling value or vice versa, off-input must have a steady non-controlling value during the application of the two vectors.

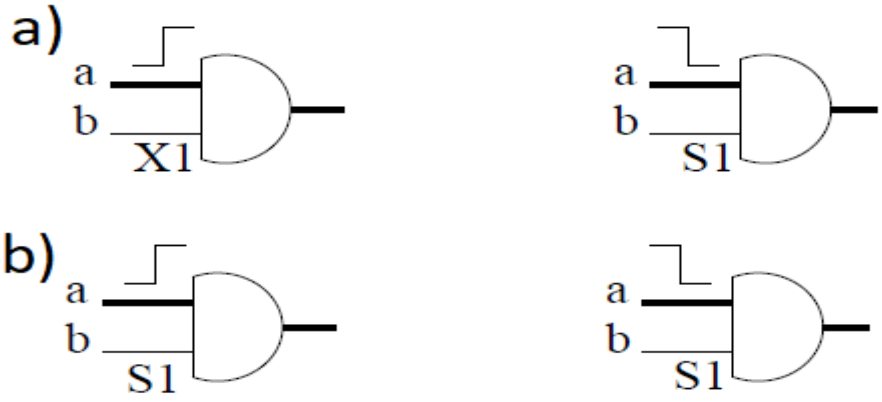

Figure 60: Conditions of an AND gate for: a) normal robust sensitization and b) modified robust sensitization for WCTV generation

To generate test patterns that will stimulate path delay fault on a target path based on the early mentioned conditions, ATPG tools such as Mentor Graphics FastScan are used. However, for sequential circuits these ATPG tools, even state of art of these tools fail to generate test patterns for sequential circuits due to the lack of controllability and observability for the internal registers in the circuit. This is why test engineers modify their designs and replace normal registers with scan cells. This is a normal design step in the ASIC flow and standard cells library provide the designer with scan cells. However, scan cells are not included in the FPGA macro libraries.

To overcome this issue in FPGA design flow, the netlist generated from the RTL code by the FPGA vendor synthesis tool is used with DFT tools such as Mentor Graphics DFTAdvisor. FPGA vendors like Microsemi provides the user with EDA tools to program their design in the target FPGA. A simple configuration can be made to make the synthesis tool of the FPGA vendor such as Synplify Pro, which is used by Mircrosemi EDA tool Liber SOC, generate a netlist from the RTL code. The netlist can be written in Verilog or VHDL. This netlist can be used by DFT tools to replace every normal flip-flop in the design with a scan cell to increase the controllability and observability of the internal registers.

The DFT tool connects the scan cells to each in a scan chain. In the scan chain, every output of the scan cell is connected to the “scan-in” input of the next scan cell. A primary input is added to the design which is the “scan-in” input of the first scan cell in the scan chain. Also, a primary output is added to the design which is the output of the last scan in the scan chain. A control signal i.e. scan enable SE is also added to the design to distinguish between the normal operation and the testing operation where the scan chain acts as a shift register. An example of a sequential circuit and its corresponding scan design is shown in Figure 61. In this methodology, muxed D scan architecture, discussed in section 4.2.1, is chosen.

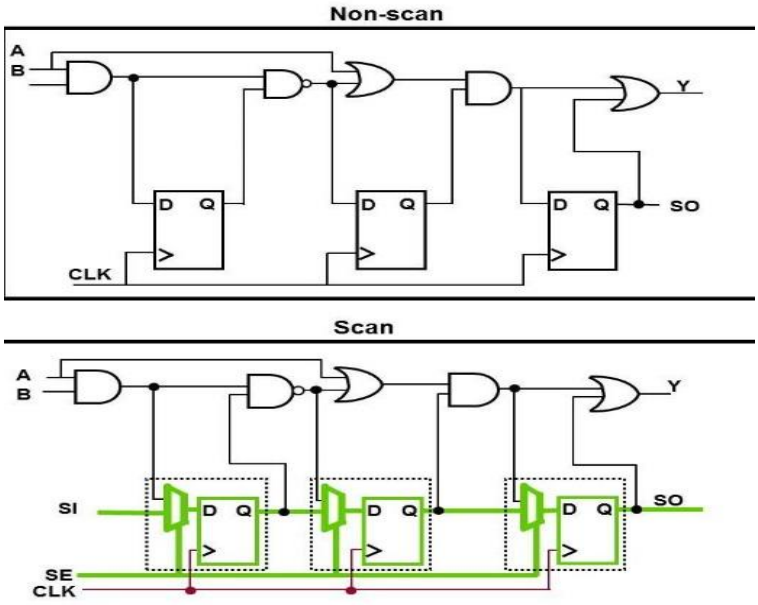

Figure 61: An example of a sequential circuit and its corresponding muxed D scan design

The new netlist generated from the DFT tool containing scan cells can now be delivered to ATPG tool such as Mentor Graphics FastScan to generate test patterns for path delay fault of the target path. In FastScan, path delay fault must be chosen as the fault type. This can be done by setting the fault type to path delay fault in a ".do" file that runs when the tool starts. An example of such script is shown in Figure 62.

```
1  set system mode atpg
2  set fault type path_delay
3  load path worst_path.asci
4  add fault -all
5  create patterns
```

Figure 62: An example of a script to set the fault type to path delay fault

The target path must be described in a ". asci" file where every cell in the path between the source register and the destination register is listed in order. The path should start and ends with a register which can controlled i.e. scan cell. An example of such description of a path is shown in Figure 63.

```
PATH "worst_path" =
PIN u1/DFF_1/DFF_1/Q +;
PIN u1/NOT_11/A +;
PIN u1/NOT_11/Y -;
PIN u1/DFF_0/DFF_1_RNI73OQ/B -;
PIN u1/DFF_0/DFF_1_RNI73OQ/Y -;
PIN u1/NOT_40/A -;
PIN u1/NOT_40/Y +;
PIN u1/DFF_2/DFF_1_RNIBIMJ/A +;
PIN u1/DFF_2/DFF_1_RNIBIMJ/Y +;
PIN u1/NOT_85_RNO_14/C +;
PIN u1/NOT_85_RNO_14/Y +;
PIN u1/NOT_85_RNO_7/A +;
PIN u1/NOT_85_RNO_7/Y +;
PIN u1/NOT_85_RNO_2/A +;
PIN u1/NOT_85_RNO_2/Y +;
PIN u1/NOT_85_RNO/C +;
PIN u1/NOT_85_RNO/Y +;
PIN u1/NOT_85/A +;
PIN u1/NOT_85/Y -;
PIN u1/NOT_94/A -;
PIN u1/NOT_94/Y +;
PIN u1/NOT_94_RNI64FV/A +;
PIN u1/NOT_94_RNI64FV/Y +;
PIN u1/DFF_4/DFF_1_0/D +;
END;
```

Figure 63: An example of a ".asci" file describing a path in a design

Launch-on-capture path delay test methodology, discussed previously in section 4.4.2.2, was chosen to generate test patterns to test a certain path. This is because launch-on-capture methodology is the best methodology that can describe the normal operation of the design under test. Launch-on-capture begins with an initialization of the internal states of a sequential circuit to some values due to the application of the first vector. The second vector is generated from the output of the combinational logic between the registers. This can easily occur in the normal operation of the design test if the internal states of the design reach values equal to the internal states due to the application of the first vector, and then the primary inputs have values equal to the second vector of the test patterns. In contrast to enhanced scan test for example, which generates any two independent test patterns that can never occur within the normal operation of the design under test.

After determining the path to be tested and the test methodology, in our case launch-on-capture, FastScan generates a file with the test patterns that can test delay fault in the target path. This file describes the procedure required for testing the required

path using the generated test patterns. The test patterns consist of a sequence of two test vectors and a scan chain vector. Each test vector consists of values to be applied in the primary input of the design under test. The scan chain consists of a set of values that the internal registers should be initialized to. An example of the procedure to be applied and the test patterns is shown in Figure 64. These primary inputs and the scan chain vector are the WCTV for delay failure for a certain sequential design.

```
SCAN_TEST =

    pattern = 0  clock_sequential ;
//      Path delay pattern: path = WP_chosen1, edge = rise, detection = robust
//      Launch_time   = 2 at /A_Z_1.D_F_F_Z (MASTER, chain1-3)
//      Capture_time  = 5 at /C_Z_1.D_F_F_Z (MASTER, chain1-19)
//      Observe_point = /C_Z_1.D_F_F_Z (MASTER, chain1-19)
    apply "grp1_load" 0 =
        chain "chain1" = "00000110100100110100000010010110";
    end;
    force   "PI" "0000100010111101111O" 1;
    pulse "/Clk" 2;
    force   "PI" "0010000100010000000" 3;
    measure "PO" "00111101001100000010001011110111001000001100l110" 4;
    pulse "/Clk" 5;
    apply "grp1_unload" 6 =
        chain "chain1" = "00001000010000001001110011000001";
    end;
```

Figure 64: Part of an example of the generated file by FastScan describing the procedure and test patterns for testing a path delay fault

To test a certain design in a flash-based FPGA with the generated WCTV resulted from the above methodology, two techniques were developed to apply the test patterns to the target path with the highest estimated number of FG switches. The first technique depends on altering FPGA design flow to include the scan cells in the design. The second technique depends on the programmability characteristic of FPGA to test a particular path with the developed WCTV.

In normal FPGA design flow, the design begins with writing RTL code in Verilog or VHDL. Then, the synthesis tool translates this code into gates in the form of netlist which can be written in Verilog or VHDL. This netlist is then placed and routed by the vendor EDA tool. The tool then generates programming data describing the design to be downloaded in the FPGA. In order to include scan cells in the mentioned flow, the netlist generated from the synthesis tool is delivered to a DFT tool such as Mentor Graphics DFTAdvisor to replace normal registers with scan cells and connect

them in a scan chain, and to add input and output to control the testing operation. The DFT tool generates a modified netlist of the original netlist generated from the FPGA vendor's synthesis tool which is also written in Verilog or VHDL. The modified netlist is then exported to the FPGA vendor's EDA tool. However, a new RTL design describing the scan cell must be included first to the project. An example of such Verilog code describing the scan cell is shown in Figure 65. To minimize the differences between the original design and the modified design with scan cells, the new design must be confined in the exact same area as the original one. This is done by defining a particular region for the place and route tool to place the macros of design inside it, and also constraining all the routing inside this region.

```
1  module dfscr ( D, CLK, CLR, Q, SCAN, D1)/*synthesis
2  syn_netlist_hierarchy=0 syn_preserve=1*/;
3  input   SCAN , D , D1 , CLK, CLR;
4  output  Q ;
5  wire X;
6
7    MX2 mux_1( .S( SCAN ),
8               .A ( D ),
9               .B ( D1 ),
10              .Y ( X )
11   );
12
13
14   DFN1C1 D_F_F  (
15     .Q(Q),
16     .CLK(CLK),
17     .CLR(CLR),
18     .D(X)
19 );
20 endmodule
```

Figure 65: An example of a Verilog code describing a scan cell

Hence, the modified netlist can then be placed and routed by the EDA tool to generate programming data to download the desired design in the FPGA. The modified design can now be downloaded to the target FPGA, and the test procedure described by FastScan can be applied to test the design using the generated test patterns.

A logic BIST is implemented with the modified design in the FPGA to generate the scan chain vector and the required primary inputs specified by the ATPG tool. The logic BIST is also used to check the output of the circuit against the expected output to

check whether there is a delay failure in the target path or not. The transition between the two vectors and the checking of the output must be made in an at-speed manner with the target operating frequency.

The disadvantage of this technique is the modification of the original design by adding a multiplexer, input pins, and output pins to the original design. This causes an increase in the delay of the circuit under test. However, the increase is minimum due to the confinement of the modified design in the exact same area of the original one.

Another technique was introduced to overcome the disadvantage of the early mentioned technique which uses the reprogram ability characteristic of the FPGA. Since only one path is required to be tested by propagating a transition along the path without being masked by other signals, no need to replace all the registers in the design with scan cells. This is done by transforming the cells along the path to act as a buffer or as an inverter to the transition on the target path in a similar technique to the one mentioned in [28] as shown in Figure 66. This will result in no modification and no increase in the delay of the path to be tested. In order to do that, every off-input of every cell along the path to be tested should always have a steady non-controlling value. The transition is done by applying a transition from high to low or vice versa to the input of the source register in the target path. The transition will go from the source register to the destination register without being masked by other signals since all the off-inputs have non-controlling value during the transition. The output of the transition can be latched by the destination register. The output of the destination register can then be compared with the expected output and observed at the primary output to know whether there is a fault or not in the target path.

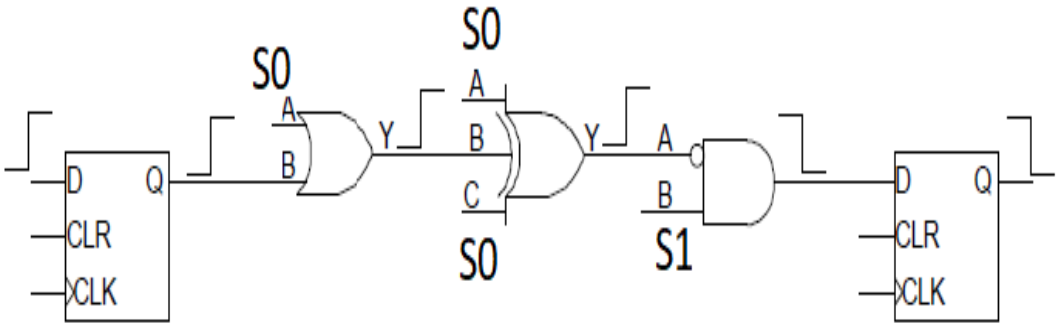

Figure 66: Proposed technique to test a path by modifying off-inputs of cells along the path

XOR gates can act as a buffer or as an inverter of the propagating transition along the path depending on the off-inputs. If the off-inputs of the XOR gate have a 0 value, the gate will act as a buffer, and if the off-inputs have a value of 1, the gate will act as an inverter. That is why the values of the off-inputs for every cell along the path to be tested should be equal to the value that the generated test patterns will force on these inputs if they are applied based on the procedure described by the ATPG tool. This will ensure that this technique have the exact transition that will happen in the normal operation of the circuit under test.

A logic BIST is implemented with the design in the FPGA to propagate the transition in the input of the source register. This transition must be made in an at-speed manner to test if the target path has a delay more than the rated clock period of the design under test. Also, the output must be checked with the expected output during exactly one rated clock period that the design is intended to operate at.

The advantage of this technique over the other technique is that no extra cells and thus no extra delay is added in the target path to be tested. Thus, giving similar behavior of the target path in the design to be tested.

Chapter 7

Experimental results

The methodology mentioned in chapter 5 was validated using two designs: an 8x8 multiplier and S1423, a benchmark circuit from ISCAS'89 benchmark circuits [29]. Both designs were implemented using Microsemi ProASIC3 A3P125-208PQFP flash-based FPGAs. The FPGAs were exposed to total dose using Cobalt 60 radiation facility at a dose rate of 100 rad/s. In this chapter the experimental results of both designs are presented.

7.1 8x8 multiplier

In order to validate the proposed methodology in identifying WCTV, a design which does not need to be modified to identify WCTV is chosen. Then, a comparison between the results before and after the modification is made. For this purpose, an 8x8 multiplier which is a combinational circuit with flip-flops at the primary inputs and the primary outputs. The worst-case path i.e. the path with the highest estimated number of FG switches in the multiplier is shown in Figure 67.

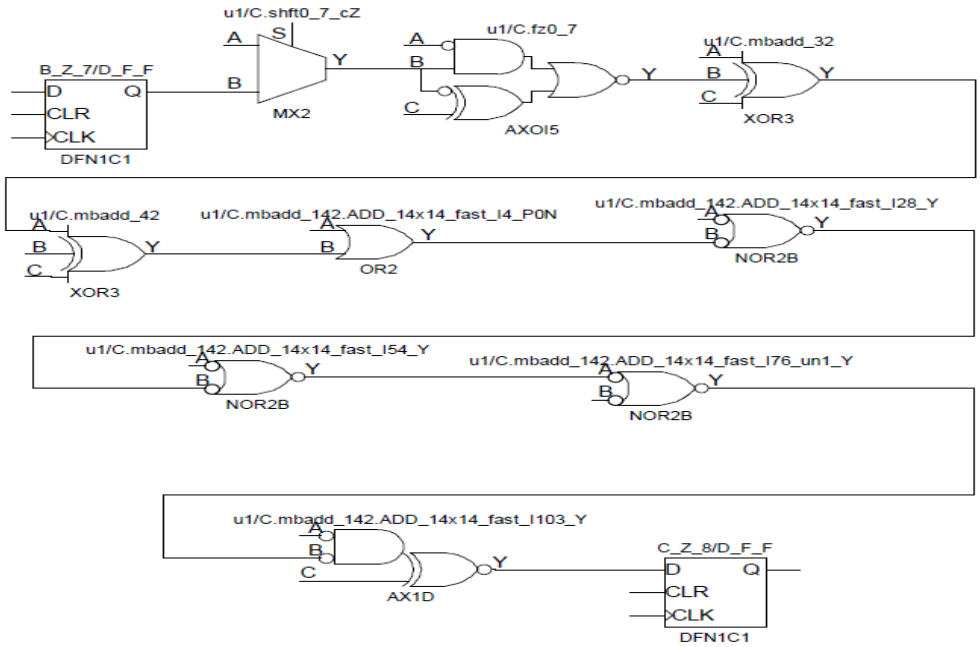

Figure 67: Worst-case path for the 8x8 multiplier

Identification of WCTV for this worst-case path is made by using Mentor Graphics FastScan ATPG tool. The tool indicates the first vector in the sequence of test patterns to be (A=01011101 and B=01001001), and the second vector to be (A=01011101 and B=11001001). Microsemi static timing analysis tools, SmartTime, identifies the pre-rad maximum frequency of operation for the worst-case path to be 134 MHz. So, an arbitrarily operating frequency is chosen to be 130 MHz to leave a reasonable margin for positive slacks in the critical paths. The FPGAs were exposed to total dose using Cobalt 60 radiation facility at a dose rate of 100 rad/s. Using the above conditions, the multiplier failed at 10 krad(Si).

The circuit is then modified using the first technique mentioned in section 6.3 to test the same worst-case path shown in Figure 67. This technique replaces all the registers in the original circuit by scan cells by using the netlist generated by DFT tool Mentor Graphics DFTAdvisor. ATPG tool Mentor Graphics FastScan identify the test patterns and the scan chain vector to test the target path. The tool indicates the first vector in the sequence of test patterns to be (A=01011101 and B=11001001), the second vector to be (A=10000100 and B=01000000), and the scan chain vector to be 00101110101001001000000010010110. The circuit with the scan insertion also failed at 10 krad(Si) when running at a frequency of 123 MHz. This reduction in the operating frequency between the original design and the modified design is due to the addition of multiplexers to transform normal registers to scan cells. However, the reduction is very low indicating a comparable total dose failure between the original design and the modified design.

The circuit is also modified using the second technique mentioned in section 6.3 to test the worst-case path shown in Figure 67. The technique depends on altering off-inputs of every cell along the path to have a steady non-controlling value to prevent any masking in the transition along the target path. A logic BIST circuit is embedded with the design to start a transition at the input of the source register and compare the output in an at-speed manner. The modified circuit also failed at 10 krad(Si) when running at a frequency of 130 MHz.

To show the significance of the WCTV, test patterns were generated to test best-case path i.e. the path with minimum estimated number of FG switches. The best-case

path is shown in Figure 68. For the original multiplier, Mentor Graphics FastScan ATPG tool indicates that the first vector in the sequence of test patterns to be (A=10111111 and B=10010010), and the second vector to be (A=10111100 and B=00011011). The operating frequency was also chosen to be 130 MHz. The FPGAs were exposed to total dose using Cobalt 60 radiation facility at a dose rate of 100 rad/s. Using the above conditions, the multiplier failed at total dose above 65 krad(Si), where ProASIC3 are reported to be failing functionally after that level [7].

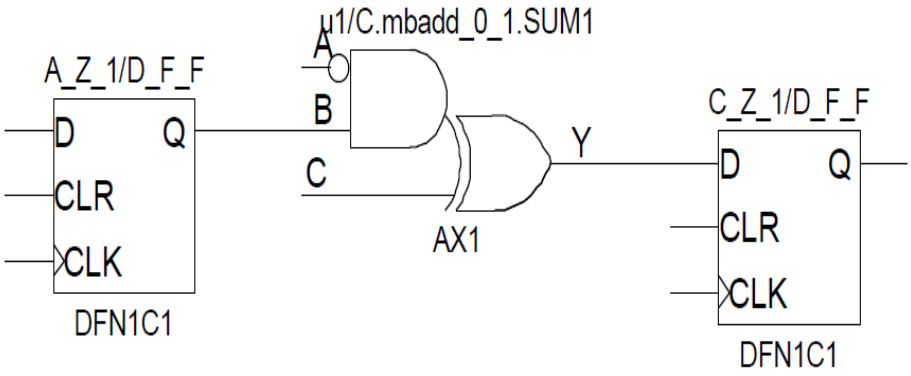

Figure 68: Best-case path for the 8x8 multiplier

Again, the original circuit is modified based on the second technique mentioned in section 6.3 to test the best-case path shown in Figure 68. A logic BIST circuit was also embedded with the design to start a transition at the input of the source register and compare the output in an at-speed manner. The modified circuit also failed at total dose above 65 krad(Si) when running at a frequency of 130 MHz.

Experimental results for the original multiplier, the modified design based on the first technique, and the modified design based on the second technique are summarized in Table III. As shown in Table III, the test vectors for worst-case paths using the first technique are the same as the test vectors using the second technique. This is because the difference in the two techniques is how the test is applied to the circuit under test. However, for the circuit under test the WCTV will be the test vectors including the first and second vector which will be applied to the primary inputs of the design, and the chain vector which the internal registers should be initialized at during the application of the primary inputs vectors.

Table III

Summary of the total dose experimental results of the 8x8 multiplier

Test case	Test vectors	Failure level krad(Si)
Worst-case (original design)	A=01011101, B=01001001 A=01011101, B=11001001	10
Worst-case (1st technique modification)	A=01011101, B=11001001 A=10000100, B=01000000 Chain=00101110101001001000000010010110	10
Worst-case (2nd technique modification)	A=01011101, B=11001001 A=10000100, B=01000000 Chain=00101110101001001000000010010110	10
Best-case (original design)	A=10111111, B=10010010 A=10111100, B=00011011	>65
Best-case (2nd technique modification)	A=01000100, B=11101111 A=00001000, B=10000000 Chain=01111101000101101000000100101101	>65

The comparison of the failure levels of the original circuit with the modified circuits implemented are similar which proves that the proposed techniques reflect the actual failure level of the original circuit. Furthermore, the comparison between the worst and best-case failure levels indicates the significance of using worst-case test vectors in total dose testing of FPGA devices.

7.2 S1423

Another sequential circuit was examined to validate the proposed methodology. S1423 which is a more complex sequential circuit from ISCAS'89 sequential benchmark circuits [29], was used. In contrast to the multiplier circuit mentioned before, ATPG tool Mentor Graphics FastScan cannot generate test patterns for the design due to the lack of controllability and observability of the internal registers. That is why the circuit must first be modified to increase the controllability and observability

of the internal registers by replacing them with scan cells. The replacement process is done using DFT tool Mentor Graphics DFTAdvisor. The generated netlist from the DFT tool is then delivered to the ATPG tool to generate test patterns, to test the worst-case path of the design i.e. the path with highest estimated number of FG switches, shown in Figure 69.

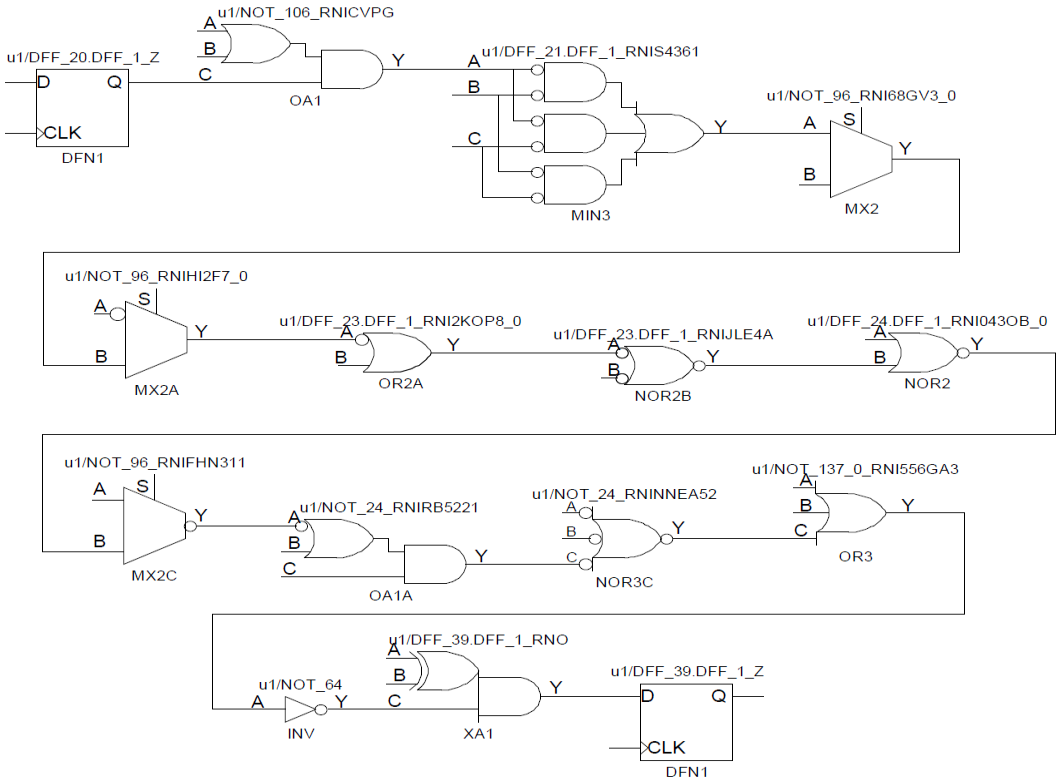

Figure 69: Worst-case path for S1423 circuit

The tool indicates the first vector in the sequence of test patterns to be 01101111011100101, the second vector to be 00000110101101010, and the scan chain vector to be 000110101111000110011000011011111000110111111000100000 10011011101010111001. Where the test vector must be applied to the following primary inputs of the design respectively {G0, G1, G10, G11, G12, G13, G14, G15, G16, G2, G3, G4, G5, G6, G7, G8, G9}.

The circuit was also modified using the second technique mentioned in section 6.3 to test the worst-case path shown in Figure 69. A logic BIST circuit was also embedded with the design to start a transition at the input of the source register and compare the output in an at-speed manner. The modified circuit based on the second technique was again implemented using Microsemi ProASIC3 A3P125-208PQFP

flash-based FPGAs. The FPGAs were exposed to total dose using Cobalt 60 radiation facility at a dose rate of 100 rad/s. The modified circuit failed at 9 krad(Si) running at a frequency of 110 MHz

To show the significance of the WCTV for this circuit, test patterns were generated to test best-case path i.e. the path with minimum estimated number of FG switches. The best-case path is shown in Figure 70. DFT tool Mentor Graphics DFTAdvisor was also used to generate a netlist where the normal registers are replaced with scan cells. The netlist is used by ATPG tool Mentor Graphics FastScan to generate test patterns for best-case path testing. The tool indicates the first vector in the sequence of test patterns to be 01001111111100101, the second vector to be 00000110111101010, and the scan chain vector to be 000110101111001000101010 001011111010110010111000100000000110111010101010 01.

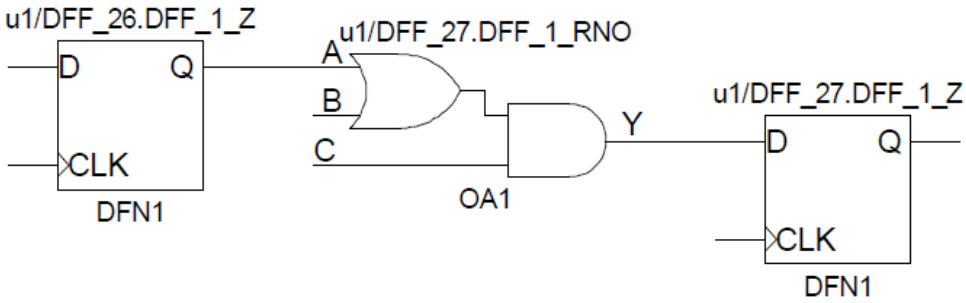

Figure 70: Best-case path for S1423 circuit

Similar to the multiplier experiment, the original circuit is modified based on the second technique mentioned in section 6.3 to test the best-case path shown in Figure 70. A logic BIST circuit was also embedded with the design to start a transition at the input of the source register and compare the output in an at-speed manner. The modified circuit also failed at total dose above 65 krad(Si) when running at a frequency of 110 MHz. This again indicates the significance of using WCTV in total dose testing of FPGA devices.

Experimental results of S1423 modified circuit based on the second technique to test worst-case and best-case paths are shown in Table IV. The test vectors are to be applied to the primary input vector {G0, G1, G10, G11, G12, G13, G14, G15, G16, G2, G3, G4, G5, G6, G7, G8, G9} of the benchmark circuit.

Table IV

Summary of the total dose experimental results of the S1423 circuit

Test case	Test vectors	Failure level krad(Si)
Worst-case (2nd technique modification)	01101111011100101 00000110101101010 Chain=000110101111000110011000011011111000 110111111000100000100110111010101110 01	9
Best-case (2nd technique modification)	01001111111100101 00000110111101010 Chain=000110101111001000101010001011111010 110010111000100000000110111010101010 01	>65

Chapter 8

Conclusion and future work

8.1 Conclusion

In this thesis, a novel methodology was introduced to identify worst-case test vectors for delay failures induced by TID effect in sequential circuits implemented in flash-based FPGA. The methodology uses a previously developed fault model that indicates that the degradation of floating gate switches i.e. the switch element in flash-based FPGA is the dominant factor causing delay failure in flash-based FPGAs induced by TID effect.

The methodology generates test vectors for sequential circuits using DFT techniques. DFT techniques were used as even state of art ATPG tool fails to generate test vectors for sequential circuits due to their lack of controllability and observability of their internal registers. DFT tool such as Mentor Graphics DFTAdvisor was used to increase the controllability and observability of the internal registers by replacing them with scan cells. ATPG tool such as Mentor Graphics FastScan can then be used with the modified design with scan cells to generate worst-case test vectors by targeting the path with highest number of estimated floating gate switches.

Two techniques were developed to test sequential circuits with the generated worst-case test vectors. The first technique relies on altering the normal design flow of FPGA to include scan cells in the design. This is because normal FPGA macro libraries does not include scan cells as DFT is not meant for FPGA design. Modified design with scan cells generated from DFT tool is placed and routed in the exact same area of the original design to minimize the differences. The second technique relies on the reprogram ability of FPGA. The off-inputs along the target path are modified to have non-controlling values, which will propagate a transition along the target path without being masked by other signals. Thus, maintaining the path under test without any extra delay.

The methodology was experimentally validated by implementing different sequential circuits designs using Microsemi ProASIC3 A3P125-208PQFP flash-based FPGAs and total dose using Cobalt 60 radiation facility.

This work was submitted to the IEEE conference on Radiation Effects on Components and Systems (RADECS) to be published in its proceedings.

8.2 Future work

More complex sequential circuits are needed to validate the proposed methodology in generating worst-case test vectors. The methodology should be modified to generate worst-case test vectors for leakage current failure in flash-based FPGA. The methodology should also be applied to ASIC where DFT techniques were used for decades to detect manufacturing defects.

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