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THE AMERICAN UNIVERSITY IN CAIRO
NANOTECHNOLOGY GRADUATE PROGRAM

Accurate Multiple Input Switching
solution for Static Timing Analysis

Khaled El-Kinawi

May 2013

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I would like to thank my supervisor Dr.Yehea Ismail for his efforts and his guidance during my work on this dissertation. I would like to express my gratitude for Dr.Hanadi Salem for her efforts in the continuous development and improvement of the nanotechnology. I would like to also thank my colleagues and friends Mohamed Abdelsalam and Tamer Abdul Aziz for their enlightening discussion that contributed to my understanding of the behavior of CMOS gates. Their help can't be overlooked. I would like also to express my sincere appreciation to my parents and family for their support.

Finally, I would like to thank God for his help and inspiration.

Abstract

Multiple Input switching is a problem in Static Timing Analysis of nanoscale electronics, which is ignored in the industry. The methods and techniques of Static Timing analysis are discussed. Effective capacitance technique is presented. The composite current model is described and examined. The Multiple Input switching problem is explored and analyzed. The history effect in Multiple Input switching is explained. The miller capacitance effect is illustrated. A number of solutions, present in the literature, are discussed. A simple and innovative solution for the Multiple Input switching problem is presented. The solution is verified using Spice and matlab. Experimental evidence is presented to show the effectiveness of the solution. Matlab is used to simulate the solution. An Algorithm for minimum and maximum delay analysis is elaborated.

1 Introduction

The Integrated Circuit (IC) industry continues to serve the needs of our society for faster and cheaper products. IC industry is reducing the feature size of ICs every two years. Today, ICs are produced with 20 nanometer feature size. This allows the industry to produce ICs with larger number of transistors. The current progress of the industry follows Moore's law. In accordance with Moore's law, it is expected for the number of transistors to continue to increase over the coming years. There are many new challenges in the design and manufacturing aspects in this new era of nano-electronics. The need for smaller feature sizes that passed the lithography limit is one of these challenges for the electronics manufacturing process. This challenge promoted the development of new techniques for resolution enhancement. The new nano-electronics era didn't change only the manufacturing process, but it also affects the design process. It is becoming more difficult to design and verify such complex electronic ICs. The large number of transistor in an IC requires more powerful and efficient tools. The digital design process is becoming more automated in IC industry. The need for automation is stressed due to the importance of earlier market entry and to keep up with Moore's law. The complexity of design is complicated by the increase of transistor count, the need for higher frequency of operation and shorter gate delay. The automated design process requires extensive verification.

The verification process can be divided into physical, logical and timing verification. The physical verification ensures the manufacturability of the design. It

ensures that the produced design follows the lithographical rules. The logical verification, also known as Layout Versus Schematic, compares a logical view of the design to the physical view. It ensures the adherence of the layout to the logical view of the design. Timing verification analyzes the timing behavior of the design. It calculates the maximum operating frequency of the design. There are two type of timing verification: Dynamic Timing Analysis and Static Timing Analysis. This Thesis will focus on an accurate solution for the Multiple Input Switching problem in Static Timing Analysis.

The rest of the thesis dissertation is organized as follows. The second section will discuss the background of Timing verification and Static Timing Analysis (STA). The basics of STA will be explained in the second section. The second section will elaborate about the effective capacitance STA technique and discuss composite current models. These models are the state-of-art models used in the industry. An understanding of these models is essential for understanding the basic ideas of this dissertation. The second section will discuss the Multiple Input switching problem and the solutions in the literature. The Multiple Input switching is dissected and explained in the second section. The third section introduces the ideas of the proposed solution. . A number of Spice simulation and matlab trials are shown in this section. The fourth section explains the algorithm for the solution in max-delay and min-delay analysis scenarios. Conclusion is given in the fifth section. The sixth section will include a proposal for future work. The final section include publication

2 Background

2.1 Timing Verification

Timing Verification ensures the adherence of the design to design timing requirements. It ensures that the design's data will be correctly handled and will stay uncorrupted. In order to elaborate about timing verification, it is important at this stage to discuss the details of the typical design structure. A typical design uses parallel processing to improve throughput. This is implemented using a series of memory elements, such as a flip-flop, connected with combinational logic that processes the data. There is a global triggering signal that prompts the flip-flop to store information. This signal is known as the clock signal. The maximum frequency for the clock signal is the operating frequency. Figure 2.1 shows a typical stage inside a digital design. This stage is preceded and followed with similar stages. The operating frequency depends on the stage with the longest path. The longest path is called the critical path. The critical path is usually optimized extensively to improve the design's overall performance. However, all flip-flops are subject to two inherit timing constraints to correctly store data. The Flip-flops require that the information to be stored remain unchanged before and after clock signal. The time required for the data to remain constant before the clock signal is called setup-time. The time required for the data to remain constant after the clock signal is called hold-time. It is part of the timing verification to ensure that these constraints are honored. The setup-time is also incorporated in the calculations of the operating frequency and clock period. There are two ways to do timing verifications.

The first way is Dynamic timing analysis.

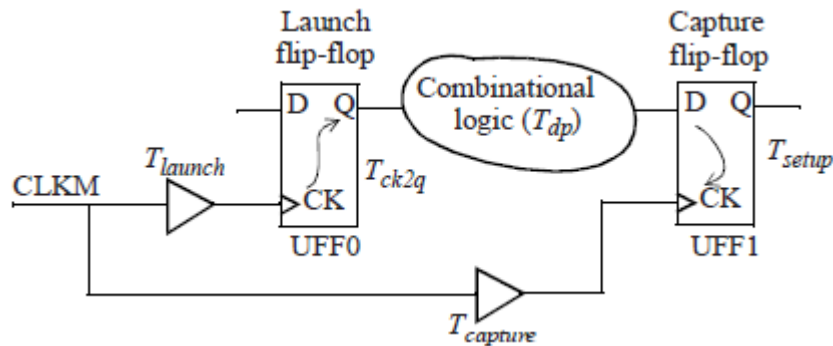


Figure 2.1 : Flip Flop to Flip Flop path[1]

Dynamic timing analysis is a circuit simulation that uses the complicated physical equations of transistors to calculate delay. Test vectors are need to be specified for dynamic analysis. It is very difficult to cover all possible cases for a chip since Dynamic timing analysis takes a lot of time. There is a need for a fast, exhaustive method to ensure timing integrity. Static timing analysis (STA) uses simplified timing models to analysis the chips. It ignores functionality and concentrates on the timing aspect of the implementation.

2.2 Static timing analysis

Static Timing Analysis (STA) is the main method of timing verification in digital IC design. It ensures the performance of an integrated circuit. Static Timing Analysis (STA) offers a compromise between accuracy and run-time. STA uses stripped-down models to estimate delay with a high degree of accuracy without requiring a long run time.

The models are generated using Spice through a characterization process. Although the characterization process would depend on the slow Spice simulation, they are done once. The models are stored as simple look-up tables. The look-up table

relates the output transition and delay time of gate to the input transition and output capacitance. These models are re-used by the different designers. The STA models relate all inputs to all outputs. However, they relate unrelated signals such as relating a functional mode signal to test mode signal. Therefore, the designer needs to specify for the tool these false paths. The false paths are usually specified by the digital design team. Although these models relate all inputs to all outputs, it assumes that only one input changes at a single moment. The input-output relationship is called a timing arc. The timing arc assumption ignores the possibility of Multiple Input switching at a single moment. The most accurate STA timing model is the recently industrially adopted model, which is the composite current source model. STA also includes a number of techniques to compensate for accuracy while maintaining simplicity. These techniques, such as the effective capacitance technique address changes in the industry without complicating the timing model. In this thesis, a simple technique will be presented to eliminate errors in STA caused by multiple input switching. In the following subsection, the effective capacitance technique and the composite current model will be discussed in more detail.

2.3 Effective capacitance

The STA models use look-up tables to relate the voltage transition time of a single input and the output load capacitance to calculate the delay of a gate. These look-up tables are collectively regarded as Non-Linear Delay Models (NLDM). The output load is assumed to be a pure capacitor. This model worked well in large feature size, where the interconnects' resistance were very small. As the feature size decreased,

interconnects' resistance increased. The original model, which depends solely on the capacitance, was ineffective. Since interconnects are a continuous array of resistance and capacitors, they are best estimated through a π -model. The π -model is made of a resistor with two capacitors on each end of the resistance. The other terminal of the capacitors is connected to the ground as shown on the left side of the figure. It is very difficult to relate the input transition and the output load represented by the π -model using a look-up table.

It was proposed to substitute the π -model with an effective capacitance as shown in Figure 2.2[2]:

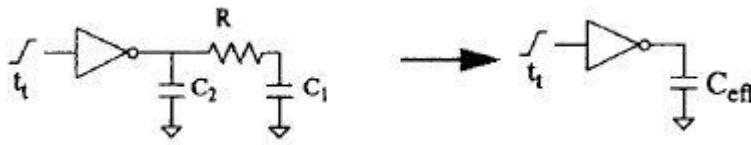


Figure 2.2: Effective capacitance replaces π -model [1]

This effective capacitor produces the same delay as the π -model. The following equation is used to determine the effective capacitance [2]. The t_D is the 50% delay point time. The t_x is the 20% point time.

$$C_{eff} = C_2 + C_1 \left[1 - \frac{RC_1}{t_D - \frac{t_x}{2}} + \frac{(RC_1)^2}{t_x \left(t_D - \frac{t_x}{2} \right)} e^{\frac{-(t_D - t_x)}{RC_1}} \left(1 - r^{\frac{-t_x}{RC_1}} \right) \right]$$

Equation 2.1 : effective capacitance and π -model [2]

This substitution ensures that the correct delay is reported. However, the output transition time is incorrect using this approach. The waveform of the output voltage

curve is incorrect after the 50% delay point. In order to correct this issue, the model is substituted by the figure below. The driving resistance of the gate is calculated and the waveform is corrected

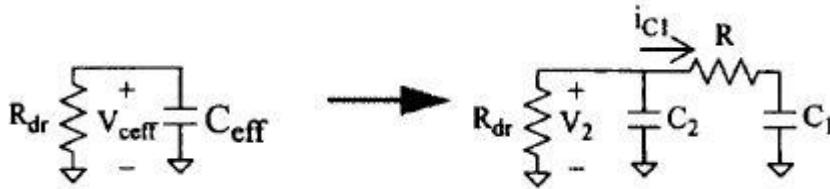


Figure 2.3 : Driving resistance model replace effective capacitance [1]

There are several methods to calculate the driving resistance such as using the thevenin equivalent or the simple equation shown below. t_{80} represents the 80% point delay. t_s shows the time, which the effective capacitance model is still valid before switching to the driving resistance model.

$$R_{dr} = \frac{(t_{80} - t_s)}{\ln\left[\frac{V(t_s)}{V(t_{80})}\right]} C_{eff}$$

Equation 2.2 : Driving resistance equation [1]

This technique is used with NLDM. This approximation is acceptable because the driving resistance is comparable to the interconnect resistance [3]. In order to deal with highly resistive interconnects, Composite current source models must be used [3]. A technique similar to effective capacitance is used with Composite current source models

2.4 Composite Current Source model

As the feature size is reduced, the top-level interconnect is becoming more resistive with narrower metal widths [3]. The industry decided to use the Composite Current Source (CSS) to replace older models such as NLDM because the current-based models improve accuracy since the driver resistance becomes infinite. This model can be divided into a driver and receiver component as shown in Figure 2.4[4]. The receiver components may be composed of two different capacitors. The first capacitor is used before the 50% delay point. The second capacitor is used after the 50% delay point. This arrangement mimics the transistor capacitance combination better. The values of the capacitors are pre-characterized using Spice.

The driver model is a voltage-dependent, time-varying current source with infinite resistance. This driver model simulates the transistor better in the nanoscale. The current source is characterized using a number of different input voltage transitions and different load capacitances.

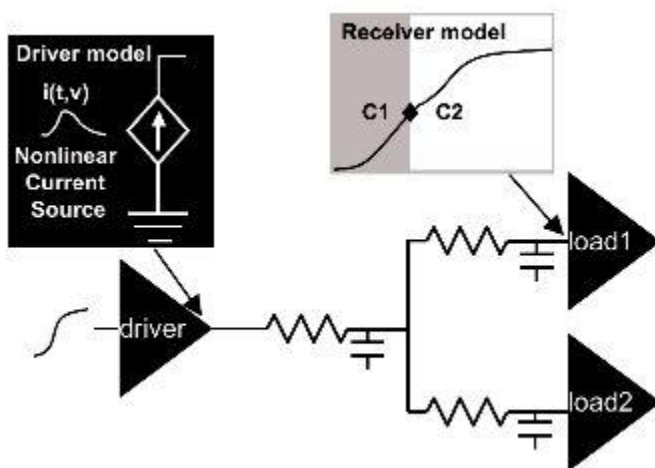


Figure 2.4 : Receiver and driver model in CCS [4]

The current waveforms for each gate are extracted as individual points using a golden simulator such as Spice. These current waveforms are used similarly to NLDM. The STA engine deduces an effective capacitance, whose current match the current for a lumped network. “There will be a unique current that will elicit the same voltage on both a lumped capacitance and the network at the given timestep.”[3] Unlike NLDM, the matching factor for the effective capacitance is the voltage. The effective capacitance matching occurs during every time step. “This current is the chosen value for the given timestep, and we reapply this procedure at every subsequent timestep” [3]. This recreates a current waveform. The current waveform is then integrated to extract the gate delay, output transition of this gate and input transition of the subsequent stage. The input transition of the subsequent gates is used to repeat the process.

2.5 Multiple Input switching (MIS)

Multiple Input switching is the case, where several input change their values at the same time. The difference between single input switching case and Multiple Input switching case in cell delay and output voltage transition time delay will henceforth be called delay error and transition error respectively. This research focuses mainly on when the change of the inputs occurs simultaneously because the delay error is of maximum value in that case.[5] Simultaneous Multiple Input Switching (MIS) in the worst delay analysis increases the delay. MIS in the minimum delay analysis decreases the delay. As far as we know, there is no proposed solution for minimum delay and transition error in both academia and the industry. We can conclude that best case as

the ground and the output of transistor. The value of this capacitance is double the gate-drain capacitance. This capacitance is called the miller capacitance.

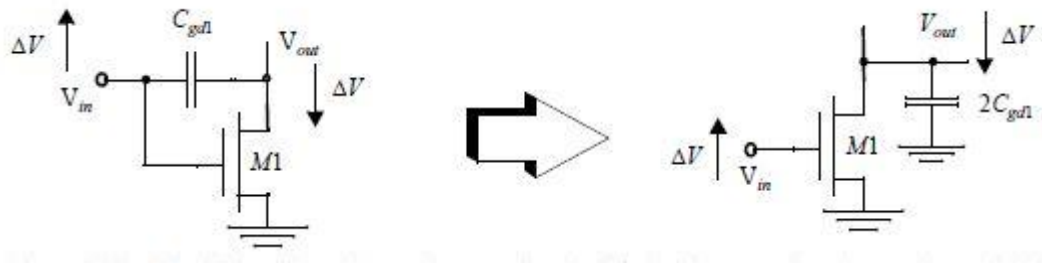


Figure 2.6 : explanation of the miller capacitance [6]

If the input A is switching individually, the miller capacitance is smaller in that case than the MIS case. When input B is switching, the miller capacitance is smaller than MIS case and the intermediate node (the node between transistor A & B) capacitance is discharged before B switches. It is theoretically expected to the delay to be larger in the SIS case, when the input A switches individually, than in the SIS case, where the input B switches individually.

According to [7] and [8], the delay error between MIS and SIS may reach up to 100%. The worst delay of the multiple switching scenarios occurs when the multiple switching signals have the same input transition and occur simultaneously [5]. The worst case MIS also depends on the input values before the MIS event. The pre-MIS event input values must induce the storage of charge in the intermediate node capacitance to increase the delay error. In order to induce this scenario, the A NMOS transistor must be turned off first. The B NMOS transistor is then turned off after transistor A. Thus, the worst case MIS will have AB input vector start as '01' then change to '00' and then

'11'[8]. This will ensure that intermediate node will maintain a voltage value of threshold voltage subtracted from the supply voltage before becoming a floating node. The intermediate node capacitor will be fully charged. This will delay the change in the output and increase the MIS error. This scenario is used in all of the simulations. This phenomenon is called the history effect.

In the industry, the simultaneous multiple input switching (MIS) is largely ignored. The probability for MIS was relatively low in the past. This probability has increased as the operating frequency increased. There are a number of solutions proposed for MIS problem. The complexity of these solutions reduces their applicability and practicality.

2.5.1 MIS existing solutions

There are a number of existing solutions in academia for MIS. However, Academia hasn't provided a satisfactory solution to MIS. This sub-section is dedicated to explain two famous MIS solutions in academia. The current source based solution and the inverter substitution solution will be presented.

2.5.1.1 Current based solutions

The most famous solution is the use of the current-based models. In [7] and [8], we find two distinct current-models models to solve the MIS. [7] Presented a model called multi-port current source model. The multi-port current source model is shown in Figure 2.7. It models the gates using a voltage-dependent current source and a voltage-dependent charge source. The current and charge source are dependent on the voltage

of all the ports. In Figure 2.7, 'p' symbol represents ports. This makes characterization more complicated and increases the run-time of static timing analysis. It would be also very difficult to build a library based on this model. This model "can result in 20% or higher delay estimation error in some cases" [8]. This large error is unacceptable in STA.

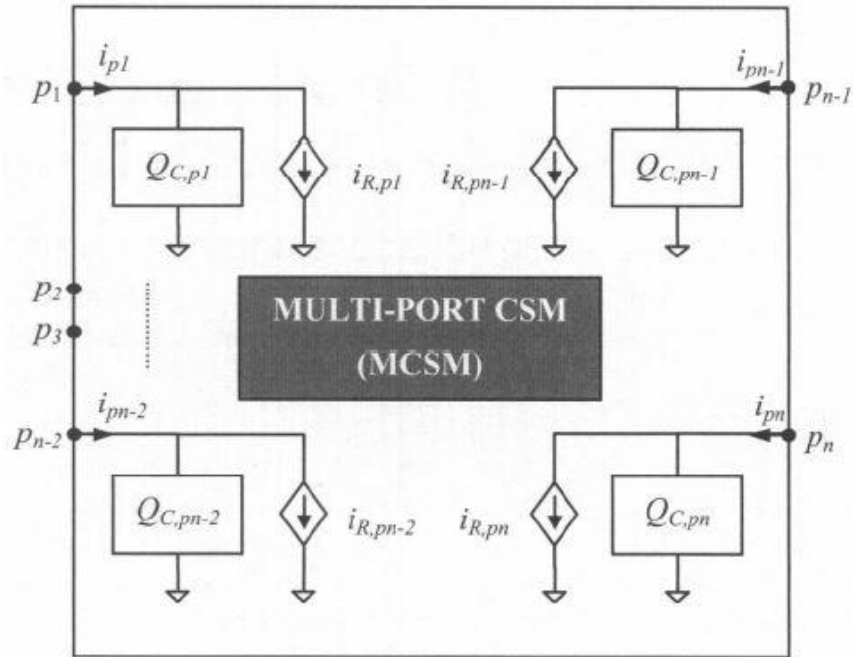


Figure 2.7 : Multi-port CSM [7]

In [8], a two-current source model is used. The second current source is used to determine the value of the intermediate node voltage. As shown in Figure 2.8, the current sources are a function of the voltage at all terminals [7]. V_a & V_b represent the voltages of terminal A & B respectively. V_N represents the voltage of the intermediate node. V_o represents the voltage of the output. The characterization and the library of this model are very complicated. It would increase the run-time and reduce the advantage of STA.

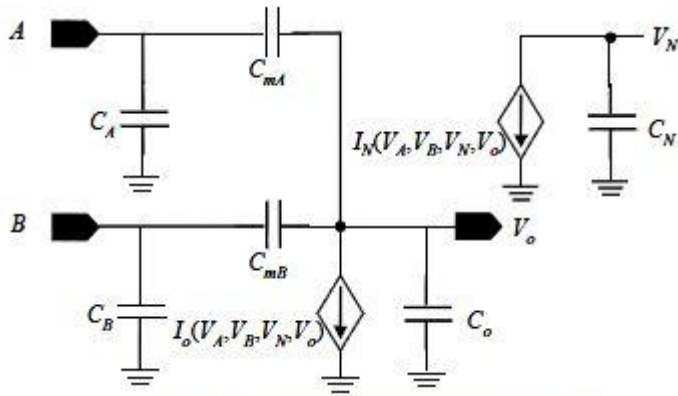


Figure 2.8 : Complete MIS CSM of a NOR2 gate [8]

These models are very complicated, when compared to CCS. The complexity of the solutions coupled with the low statistical probability of the occurrence of SMIS in older technologies discouraged the industry from including these error correction solutions in the industrial process.

2.5.1.2 Inverter solution

The inverter solution transforms the input waveform into an equivalent form. It also replaces the complicated gates into a collection of inverters. In [9], “the waveforms of the switching inputs are replaced by an equivalent waveform and the multi-input gate is collapsed into an inverter by series-parallel reduction of the transistors” [5]. The error presented in [9] is 5%. This percentage is very high for STA. In [10], the author attempts to modify the Inverter solution to improve accuracy. However, the authors focus on calculating the maximum current. “Both these techniques give significant errors when we measure delay and output transition time” [5]. These techniques are very difficult to implement in STA. They would require significant run-time and it would reduce the advantage of STA. Although this method reduces the error of the Multiple Input

switching, it still has a significant overall error. In the next section, a novel solution is presented that overcomes these limitations.

3 MIS Novel Solution

In order for the industry to accept a proposed solution of MIS problem, it must have the following properties:

- It must have low overhead during the transition and delay calculation process.
- The accuracy of the solution must be within 1-2% of the Spice results.
- It would be optimum if it builds on models that the industry uses such as NLDM or CCS.
- It should have a low number of new timing arcs. The lower number of timing arcs would reduce the complexity of the overall timing analysis.
- The solution should eliminate the error in delay and output transition of the gate. This would ensure the completion of the solution.

3.1 Current shift

The MIS delay error could reach up to 100% [7]. The current shift theory is aimed at reducing this error to an acceptable value. The proposed idea is to shift the output current values in time for one of the SIS case. This would allow the delay of this SIS case to increase. The value of shift should make the delay of the modified SIS current equal to MIS case. This shift is a side effect of the increase of the miller capacitance. The

current shift would maintain the benefit of the current source and would be easily implemented in STA.

3.1.1 Current shift experimental observation

The simulation explores a NAND gate. It uses the configuration shown Figure 2.5. The NAND starts with an output of '0' and switch its output to '1' and back to '0'. This is done to initiate the NAND in a condition similar to its regular operation conditions. The intermediate capacitor is also allowed to store charge when the output is switched to '1'. This will cause the maximum MIS error and account for the history effect. The simulation uses tsmc 65nm technology Spice models. The simulation is repeated for different input transitions, load capacitors and transistor widths.

Five hundred and ten simulations were performed using Spice iterating over different variation for the configuration of a tsmc 65nm NAND gate, input transitions and load capacitances. Each simulation test case includes two SIS cases and the MIS case that has the same load capacitor, transistor sizing and input transition on its inputs. The simulations ensured that the worst case MIS is compared the SIS cases. The current and voltage waveform is produced. The delay, input and output transitions are calculated. The maximum output current is also calculated.

The options "runlvl=6 post=2 brief" were used during Spice simulation to ensure higher accuracy during simulation. The timestep was 1f. The following figures show the input and output of the simulation for SIS & MIS cases. All current images, delay and transition calculation are done on the second rising edge. Figure 3.1 shows the inputs

for SIS case. The black line represents the voltage for input A. The blue line (grey) represents input B. Figure 3.2 shows the output for the SIS case. In this case, input A is switching.

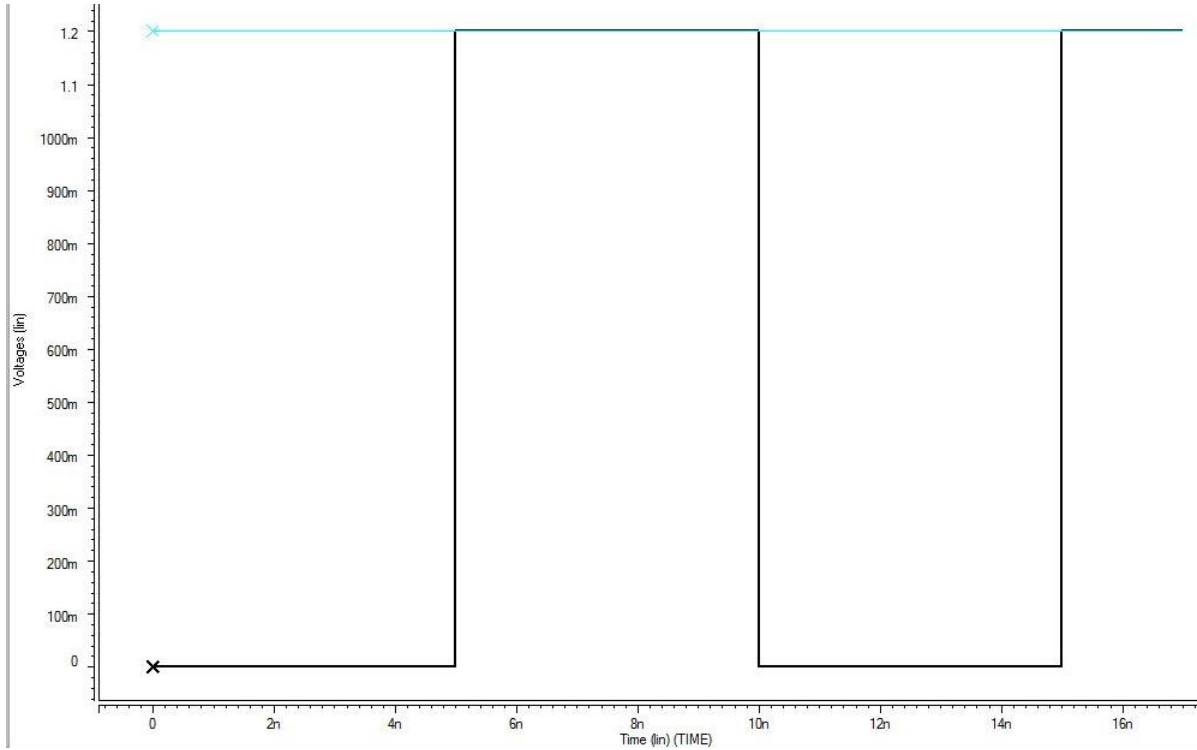


Figure 3.1 : SIS case inputs

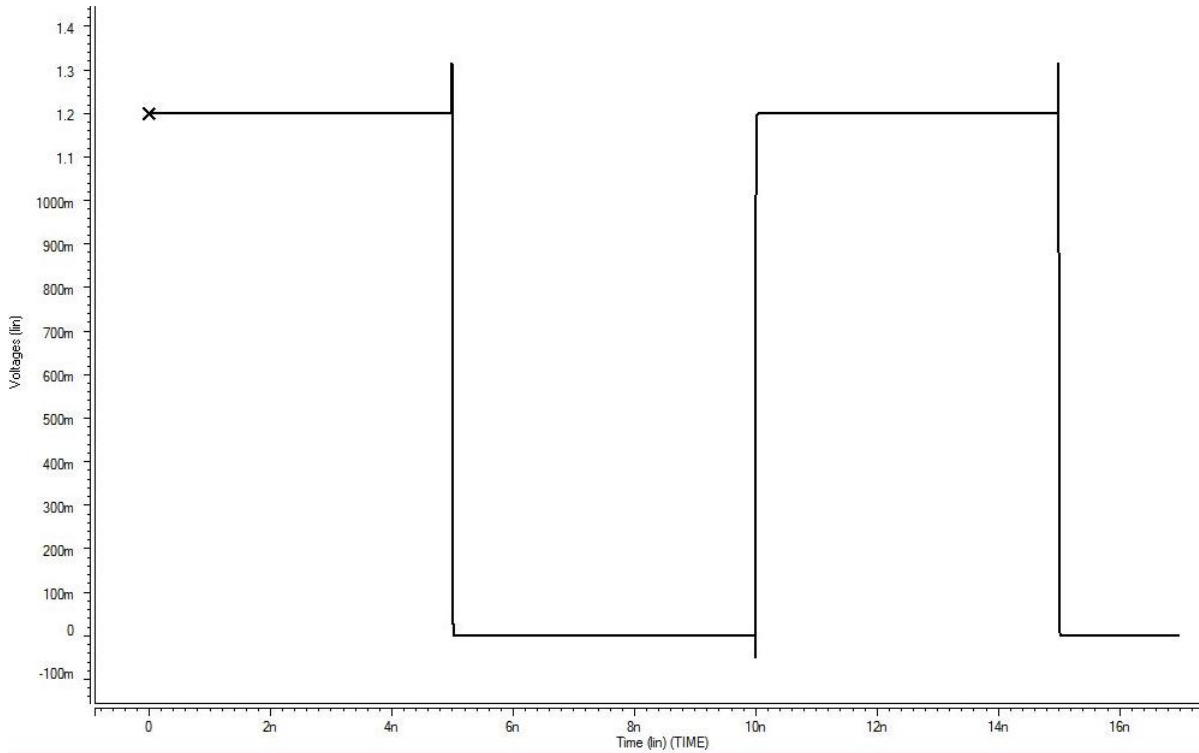


Figure 3.2 : SIS output

In Figure 3.3, the inputs for MIS case are shown. The black line represents the voltage for input A. The blue line (grey) represents input B. The input A falls before the input B to prevent the discharge of the intermediate capacitance. This ensures maximum delay error. The time period of the input is large to ensure stabilization of the output. The Spice simulation of SIS case is meant to mimic the characterization process of CCS model. Figure 3.4 shows the MIS case output.

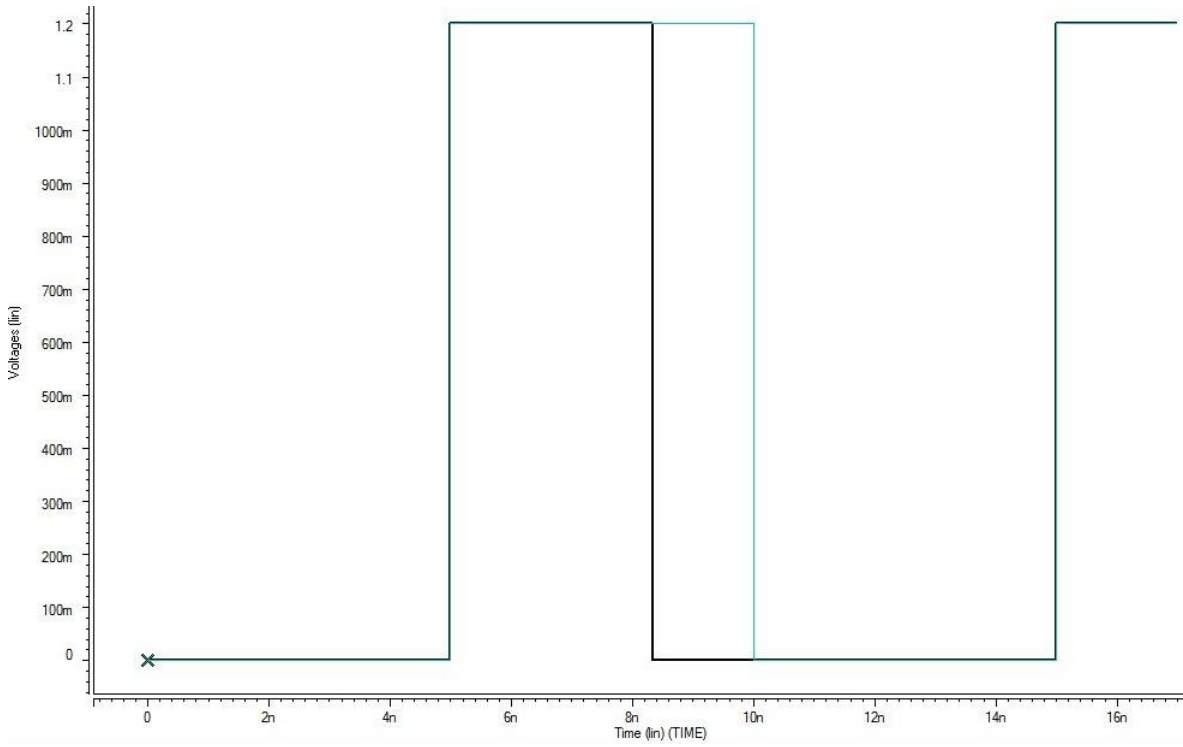


Figure 3.3 : MIS Inputs

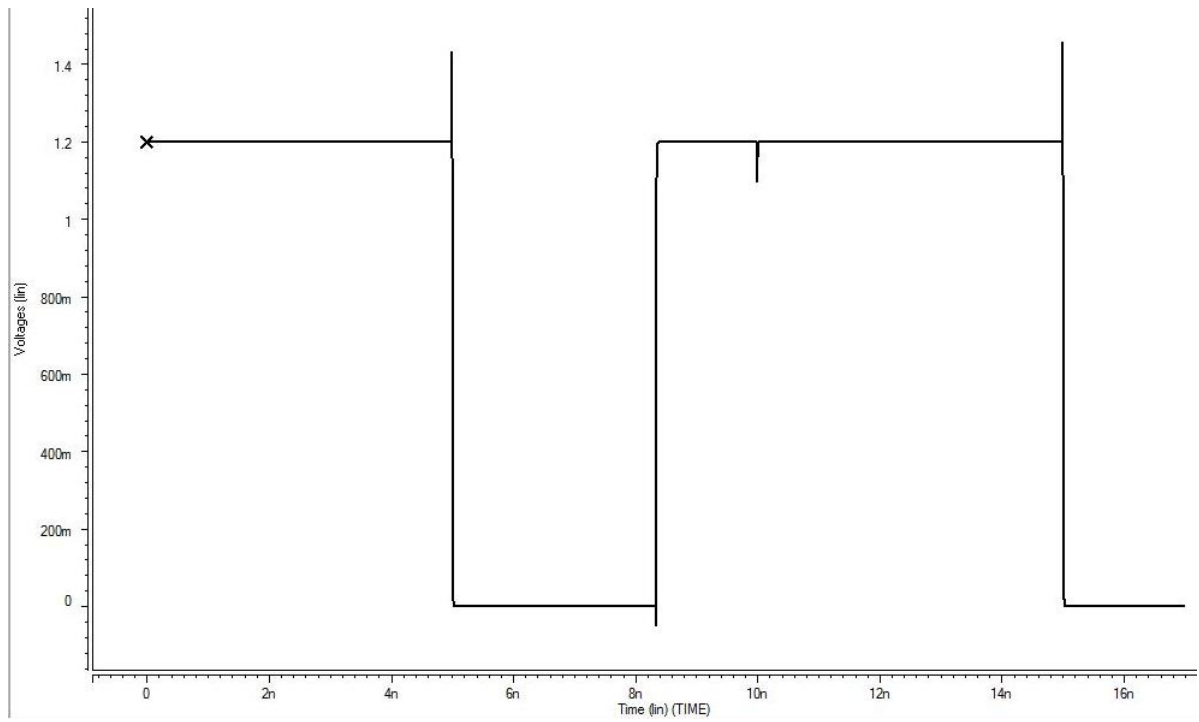


Figure 3.4 : MIS output

The shape of the current in the MIS case is shown in the following figures. Please note that the MIS current (in black) and Input A SIS case current (in blue). The MIS current appears to be a delayed version of the input A SIS case.

These figures show that if the current of the grounded NMOS SIS case is shifted in time. We can reproduce an approximate waveform of MIS. This shift maintains the basic benefits of CCS models. This shift can be added as a variable in the model. The static timing analysis tool can use this variable and re-generate MIS current waveform. Figure 3.5 through Figure 3.10 show a sample of the Spice simulation test cases. These figures illustrate the difference between the SIS and MIS currents. Through observation, a hypothesis can be formed about the relation SIS between MIS. The hypothesis states that MIS current a shift version of the SIS current.

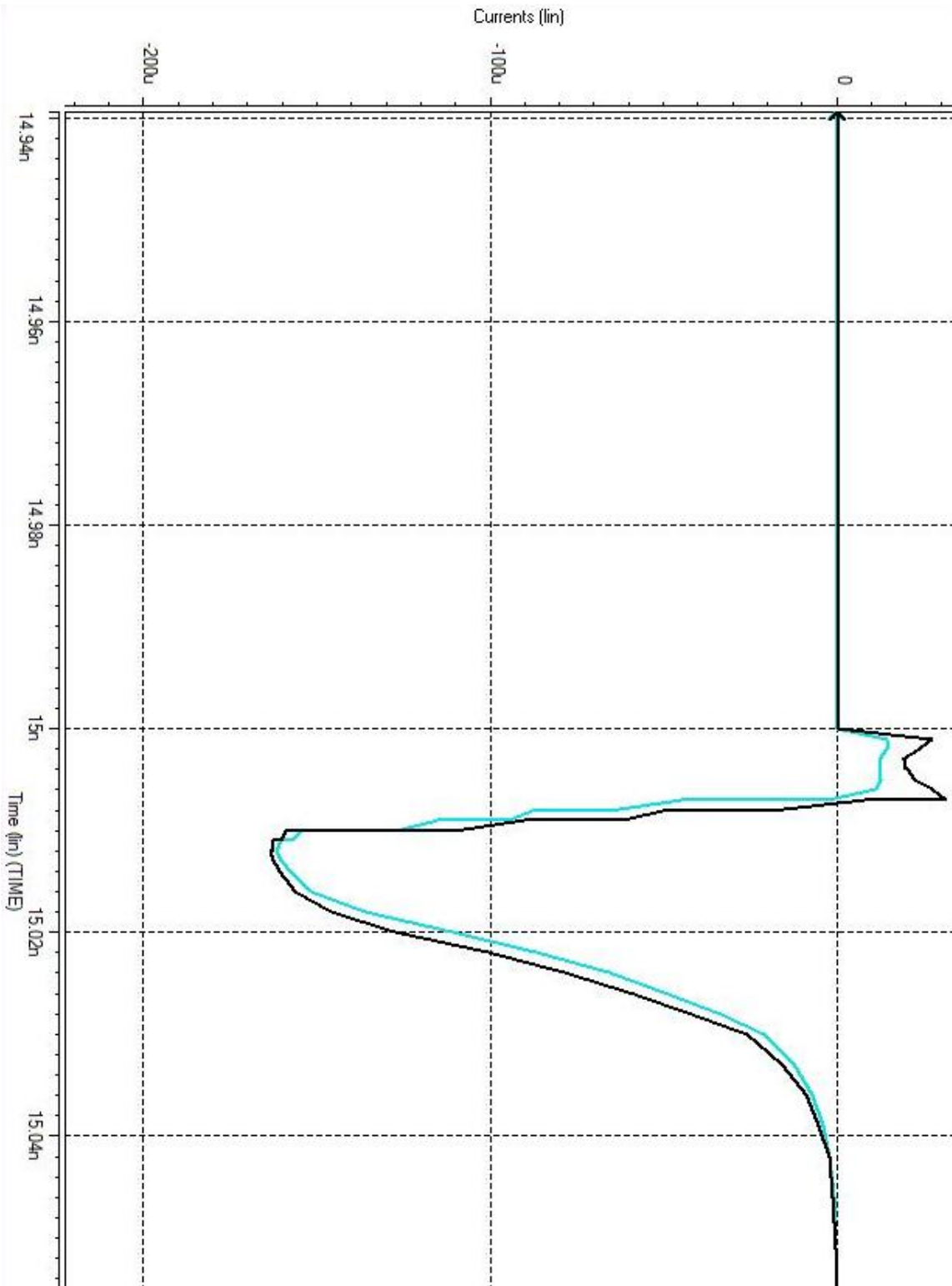


Figure 3.5 : MIS (black) & SIS currents (light blue) for input transition 10ps, the NMOS transistor width is 390nm, and the load capacitance is 2f farad

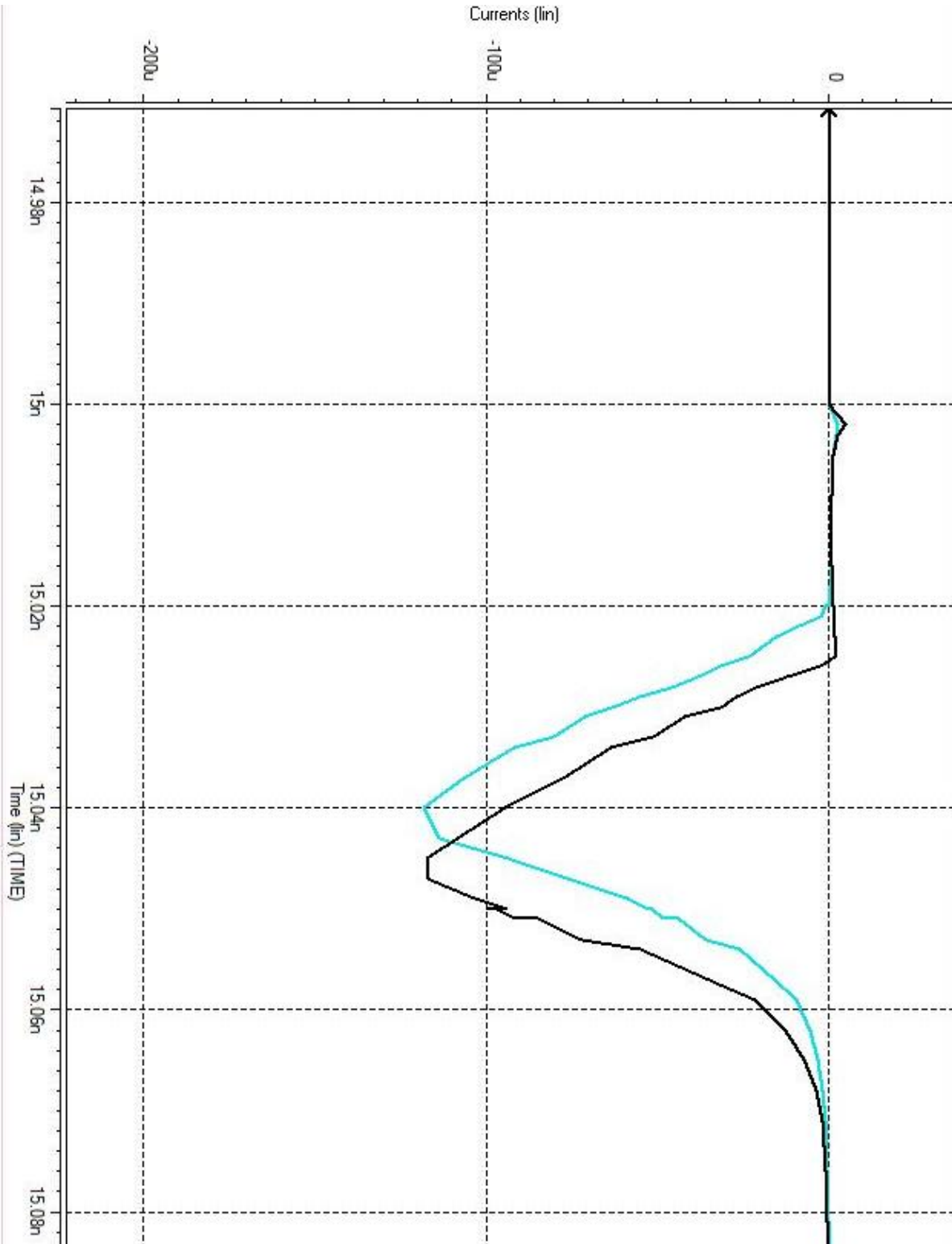


Figure 3.6 : MIS (black) & SIS (light blue) currents for input transition 50ps, the NMOS transistor width is 390nm, and the load capacitance is 2f farad

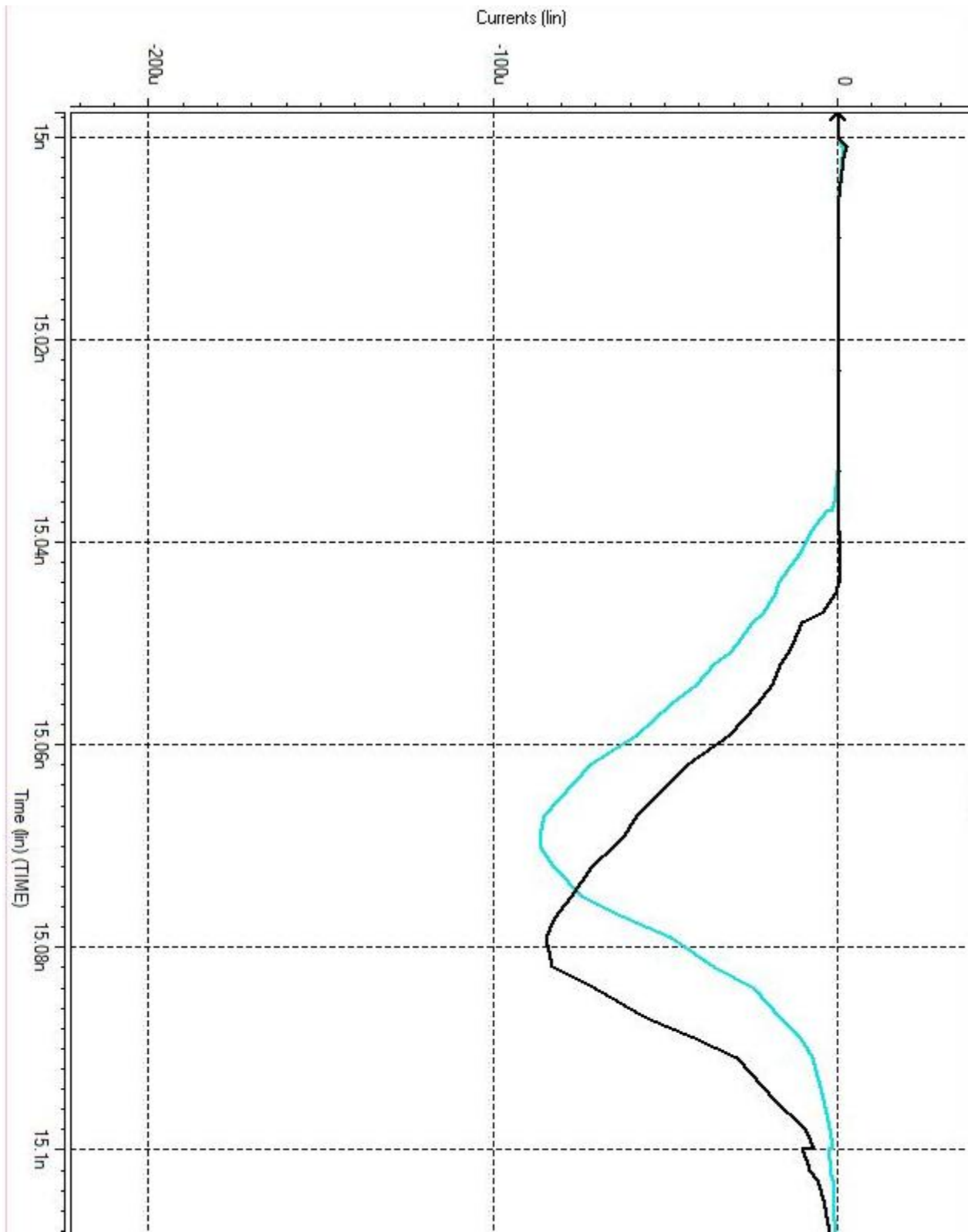


Figure 3.7 : MIS (black) & SIS currents (light blue) for input transition 100ps, the NMOS transistor width is 390nm and the load capacitance is 2f farad

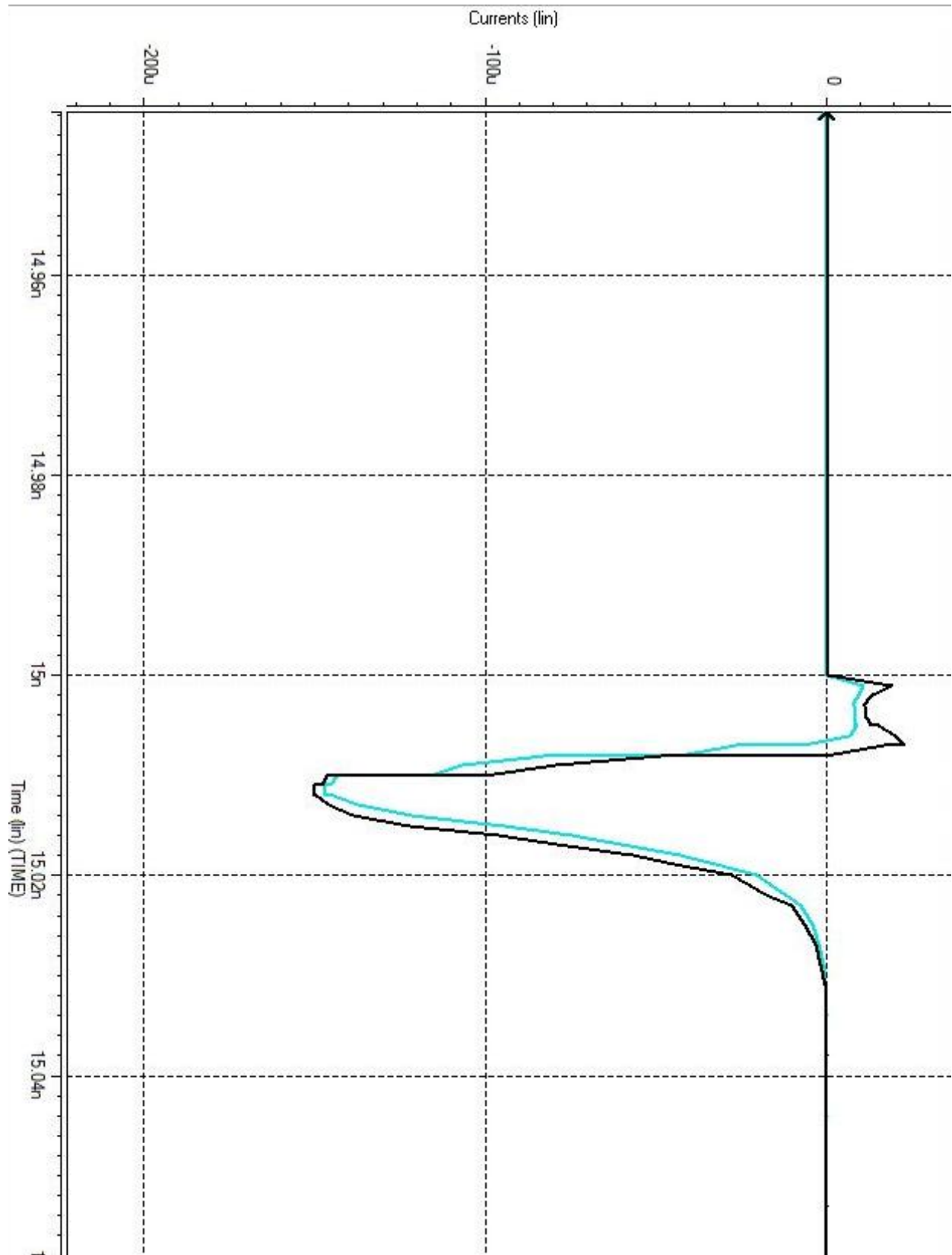


Figure 3.8 : MIS (black) & SIS currents (light blue) for input transition 10ps, the NMOS transistor width is 585nm and the load capacitance is 1 f farad

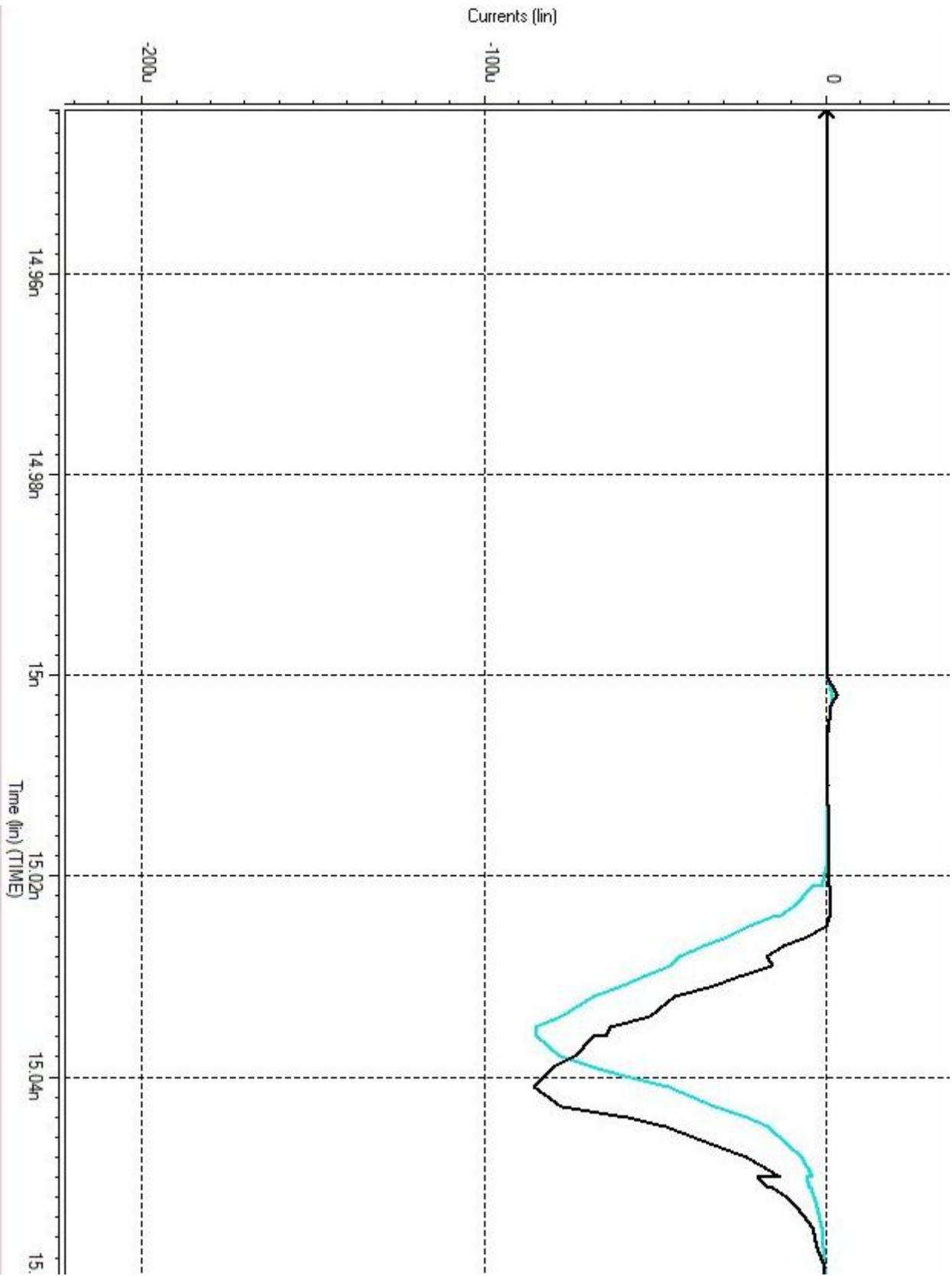


Figure 3.9 : MIS (black) & SIS currents (light blue) for input transition 50ps, the NMOS transistor width is 585nm and the load capacitance is 1 f farad

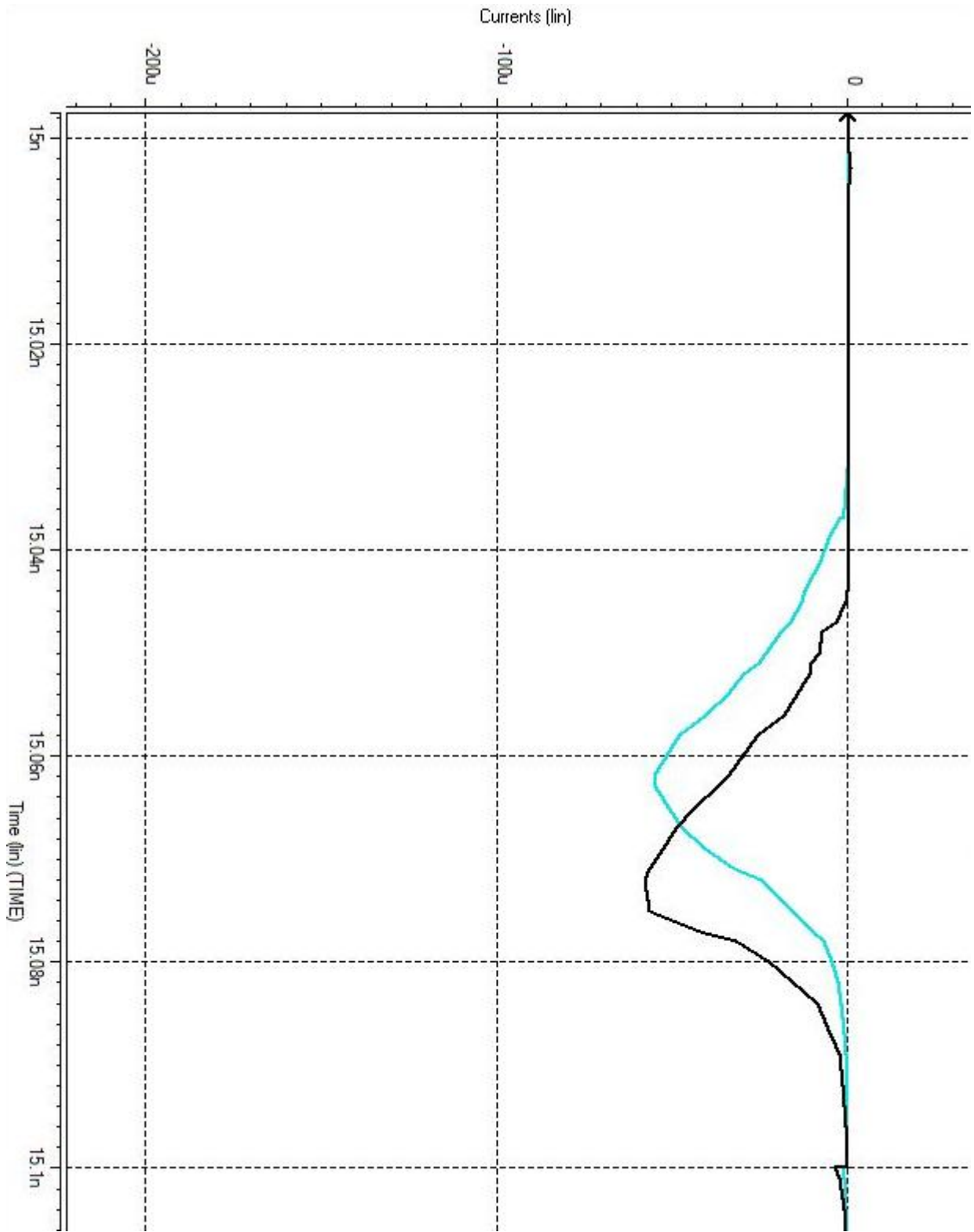


Figure 3.10 : MIS (black) & SIS currents (light blue) for input transition 100ps, the NMOS transistor width is 585nm and load capacitance is 1 f far

3.2 Multiplication factor

The transition time error can't be reduced using only the current shift. The current shift would eliminate the delay error. However, the voltage transition time of the shifted current will be the same as the transition time of the original unshifted SIS case. The absolute transition time error is less than 2% in 44% of the tested cases. In 79% of simulation, the MIS case's output voltage has smaller or equal output transition time to its respective SIS case. MIS cases, which have smaller transition time, are less pessimistic. Another solution for the transition time error would be preferred.

The solution is using a multiplication factor. The multiplication factor is multiplied by the current values. After shifting the current, you can easily deduce the mid-point voltage delay using integration. We can then multiply the current values that occur after the delay point to modify the transition time. Since we are multiplying the current values after the delay point, the delay calculations are unaffected. This method is similar to the effective capacitance method, where you use the effective capacitance to find the delay then calculate the transition time using the driving resistance. We use the current shift method to calculate the delay then use the multiple the current values occurring after the voltage mid-point to calculate the transition time. The multiplication factor can reduce or increase the transition time of the altered current waveform. This is essential to correct for decrease or increase of output voltage transition time.

3.2.1 Matlab verification

In order to verify these concepts, two cases of the Spice simulations were processed using matlab. The current waveforms of the SIS & MIS cases were imported in matlab. The current was then integrated to produce the output voltage waveform for both the MIS & SIS case. The current shift is then performed on the SIS current waveform. The shifted current is then integrated to produce a new voltage waveform. This waveform is compared with the MIS voltage waveform. The shifted SIS current is then manipulated using the multiplication factor. The multiplied shifted current waveform is integrated again. The voltage waveform of that current is compared to the MIS voltage waveform. The delay and transition error of final waveform and MIS error is mentioned. The matlab verification was done on two cases. These cases exemplify the most difficult situation for the implementation of this method. The first test case was chosen because the maximum value of the SIS & MIS cases has the largest difference. This illustrates that the current manipulation method can overcome large differences in the maximum value of current. The second case has the largest absolute error in transition time in the Spice simulations. The current and voltage waveform are represented graphically and several calculation are made to assess the success of the current manipulation method.

3.2.1.1 The first case

This case followed the procedure outlined above. Figure 3.11 shows the original SIS current is in light blue. The MIS is in Black.

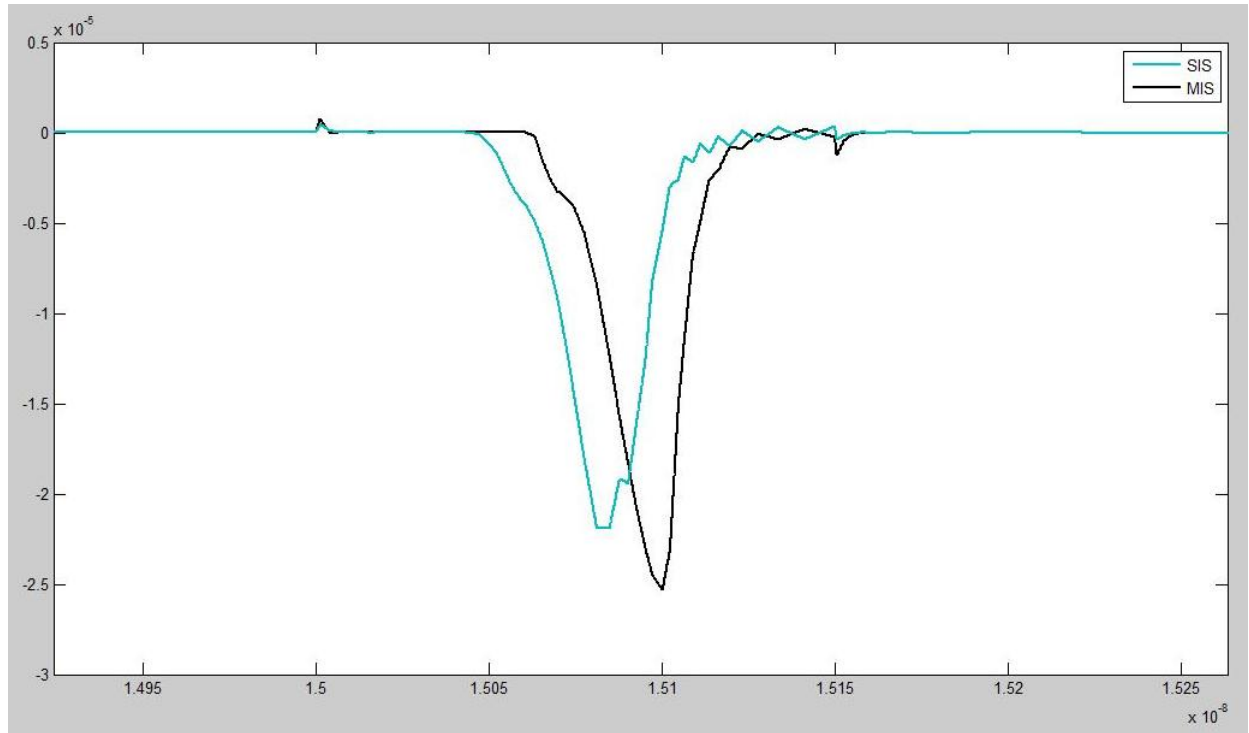


Figure 3.11 : Initial MIS (black) & SIS currents (light blue) in the first case

The second figure shows after shifting the current. The value of the shift is determined through a number of iterations. An estimated initial value is used to shift the current. The current is integrated. The delay of resultant voltage of the shifted current is compared to the MIS delay. If the error is unacceptable, the delta value is changed and the comparison is repeated. This delta value is essential for applying this solution. Figure 3.12 shows the shifted current and the MIS current.

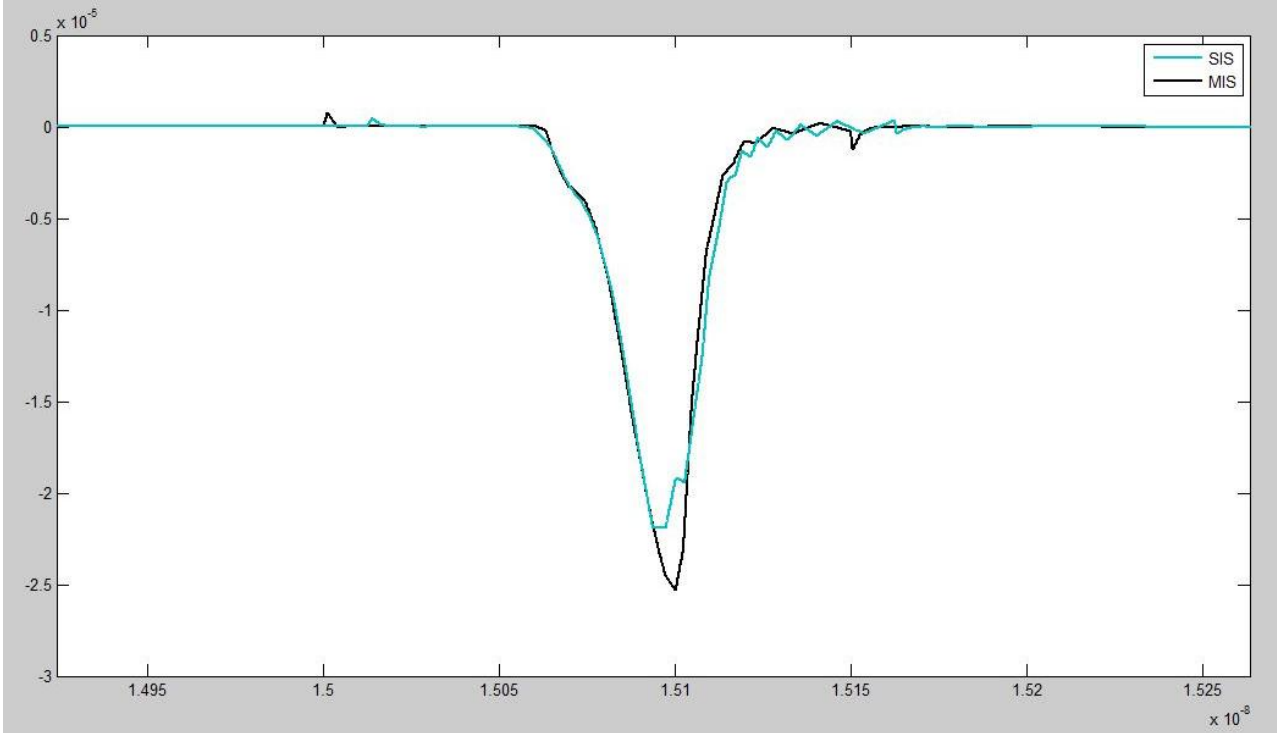


Figure 3.12 : Shifted SIS (light blue) and MIS (black) in the first case

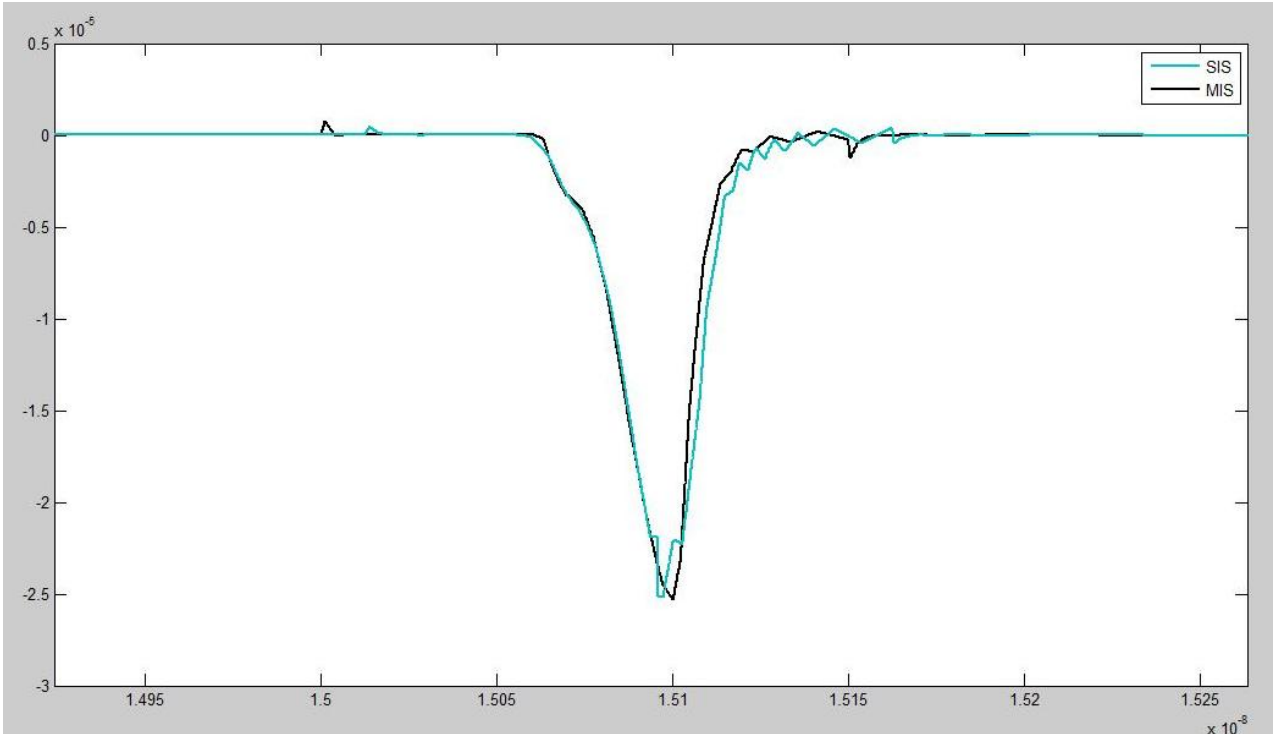


Figure 3.13 : Modified SIS (light blue) and MIS (black) in the first case

After calculating the delay, we then experimentally determine the multiplication factor.

The multiplication factor is chosen through an iterative process similar to the shift factor, where we compare the transition time error. Figure 3.13 shows the modified current after shifting and multiplication and the MIS current.

Figure 3.14 shows the voltage waveform of the SIS and MIS cases before modification.

Figure 3.16 shows the close correlation between the voltage waveform after current modifications and MIS voltage. The percentage delay error was reduced from 60% in the original case to 0.34% in the modified case. The percentage transition error was reduced from 9.19% in the original case to 0.19% in the modified case. The degree of error correction is dependent on the iterative process. The error could have been reduced further but these error values are acceptable for STA.

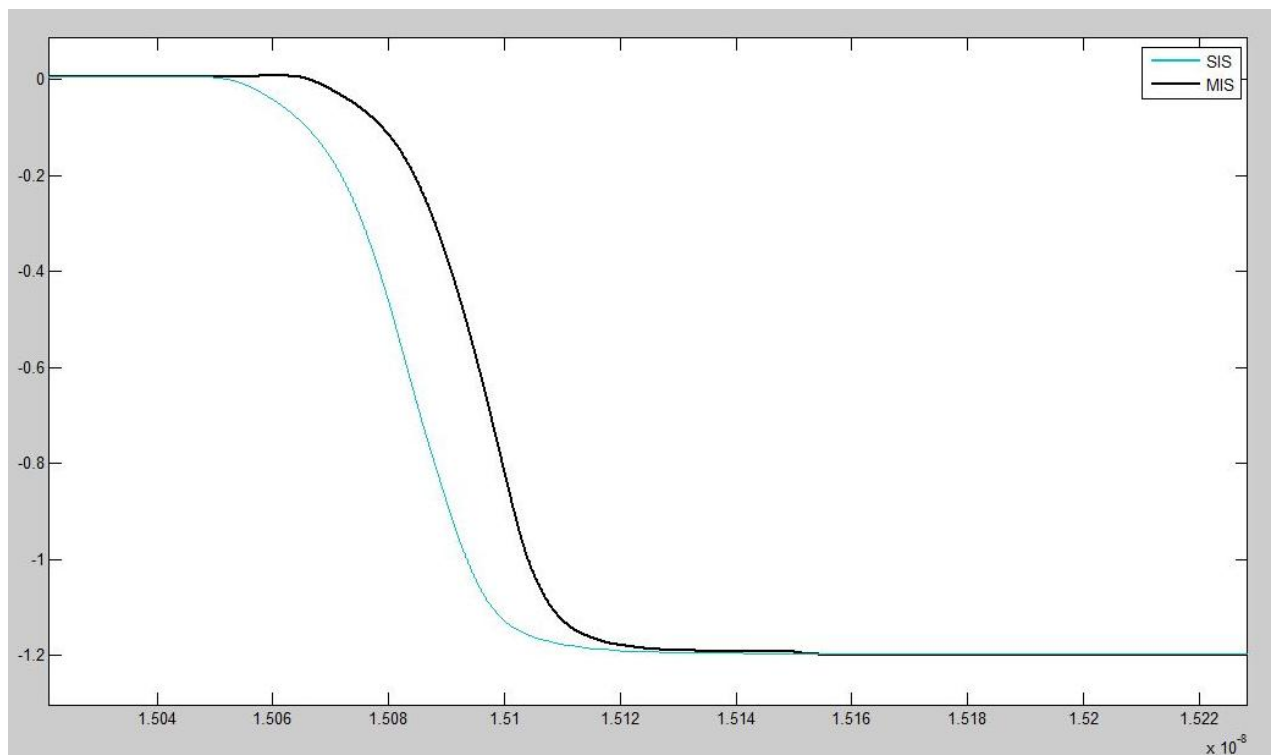


Figure 3.14 : Original SIS voltage (light blue) and MIS voltage (Black) in the first case

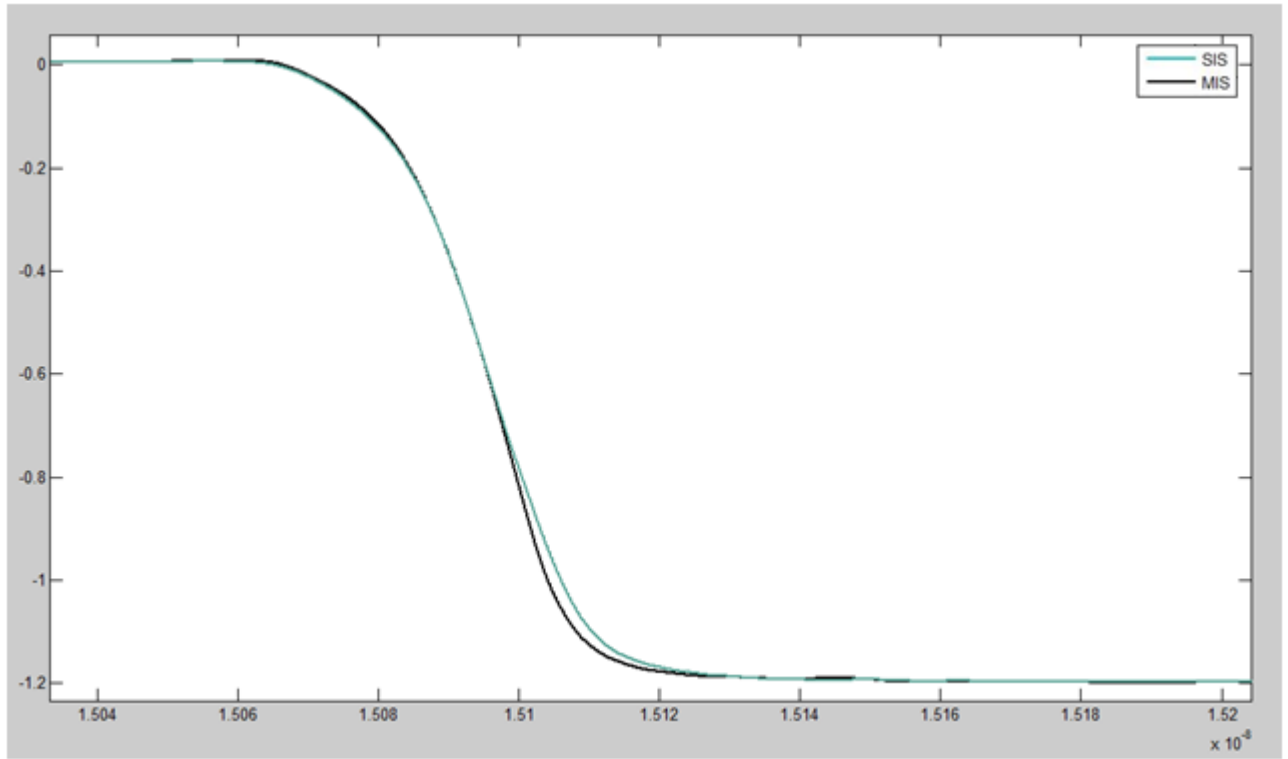


Figure 3.15 : Shifted SIS voltage (light blue) and MIS voltage (Black) in the first case

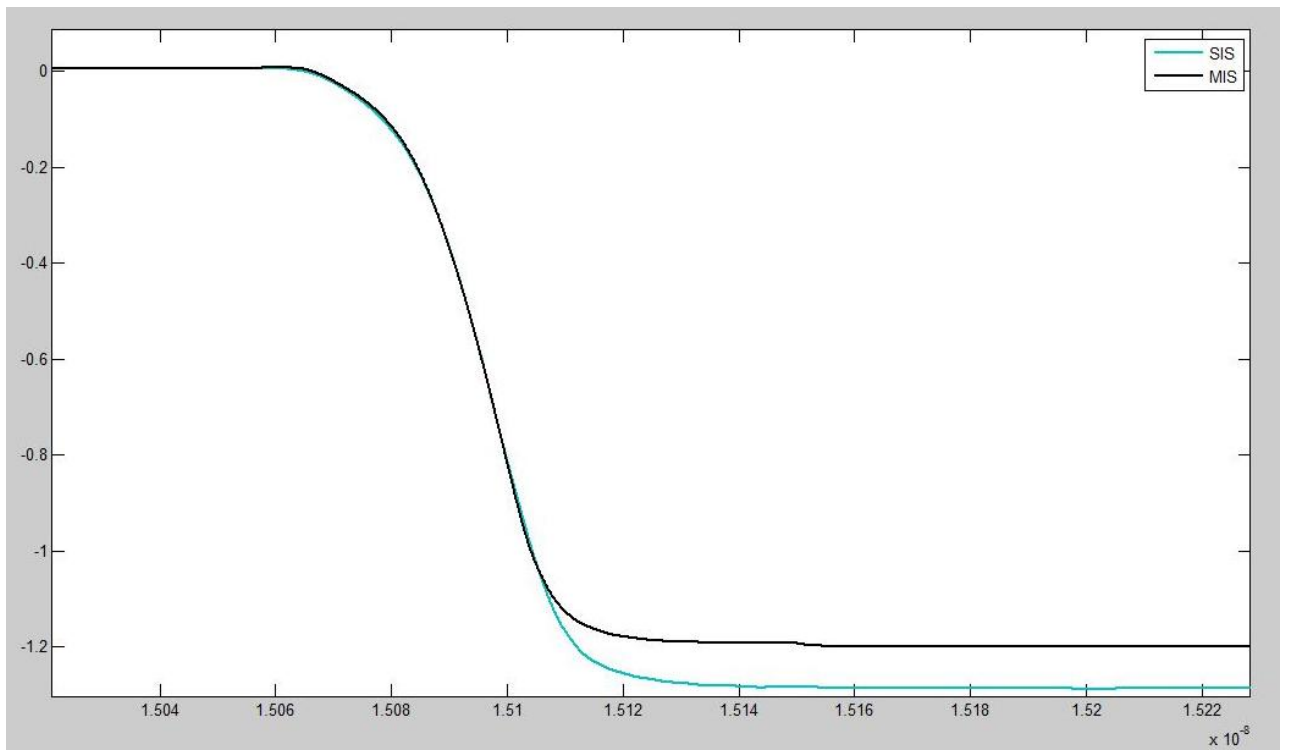


Figure 3.16 : Modified SIS voltage (light blue) and MIS voltage (Black) in the first case

3.2.1.2 The Second Case

We applied the previously described process on another case. This case has the largest transition time error. Figure 3.17 shows the unmodified current and MIS current. Figure 3.18 shows the SIS current shifted in comparison to the MIS current. Figure 3.19 shows the SIS current after modification in its final form compared to MIS currents. As we can see the voltage waveforms show a huge reduction in transition as well as delay percentage error. The delay percentage error in delay reduced from 82.69% to 0.31%. The transition percentage error reduced from -10.73% to 0.43%.

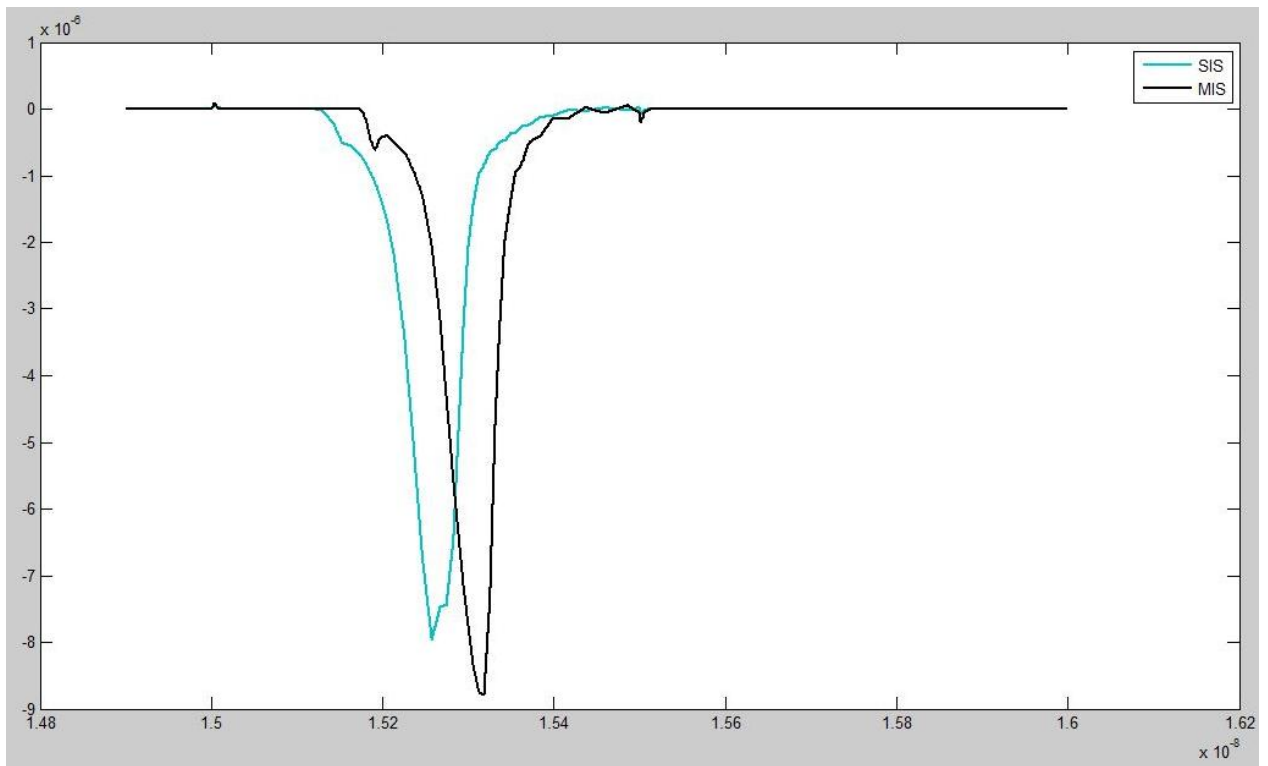


Figure 3.17 : Initial MIS (black) & SIS currents (light blue) in the second case

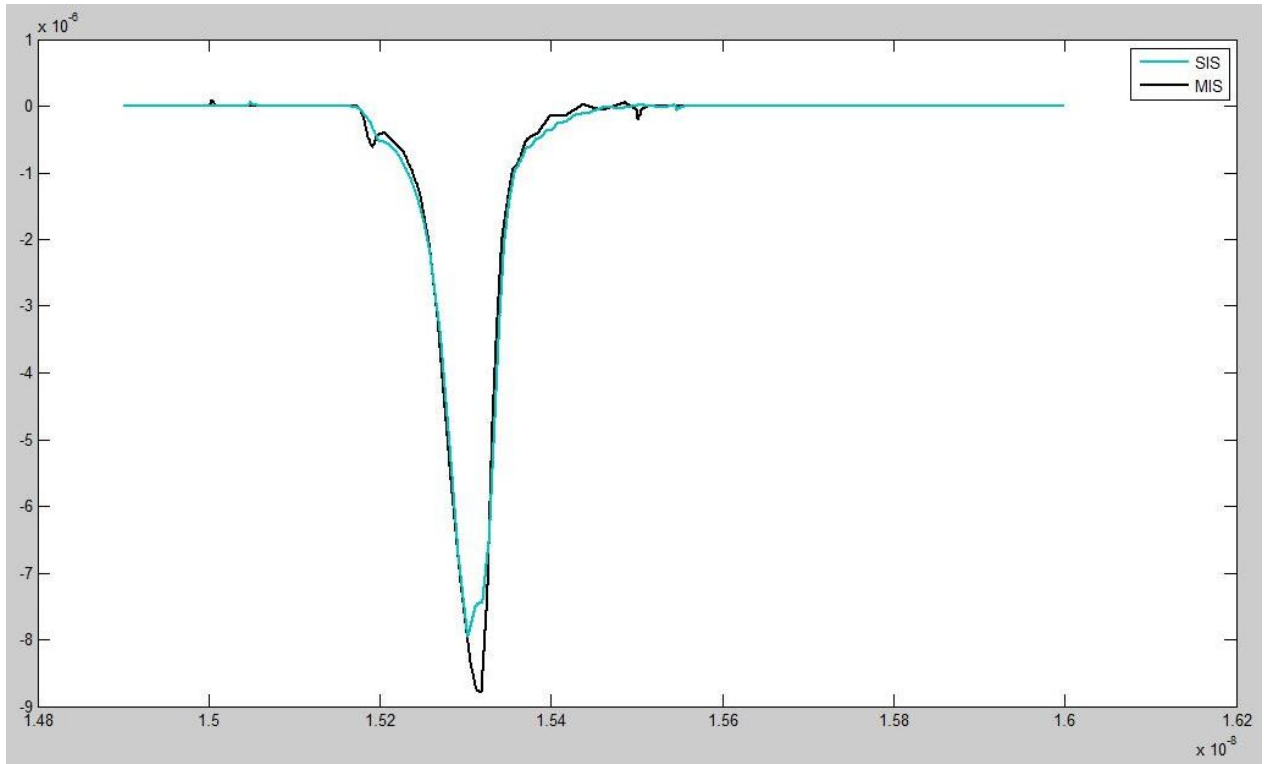


Figure 3.18 : Shifted SIS (light blue) and MIS (black) in the second case

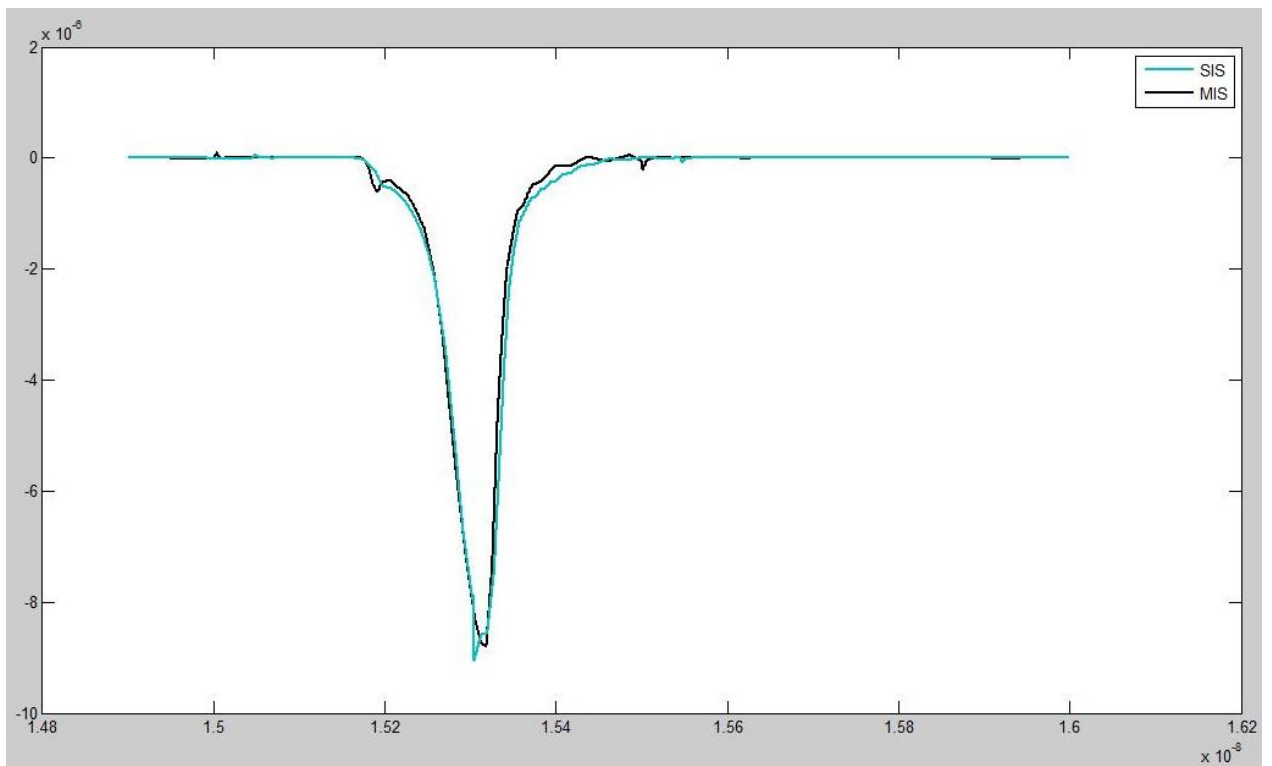


Figure 3.19 : Modified SIS (light blue) and MIS (black) in the second case

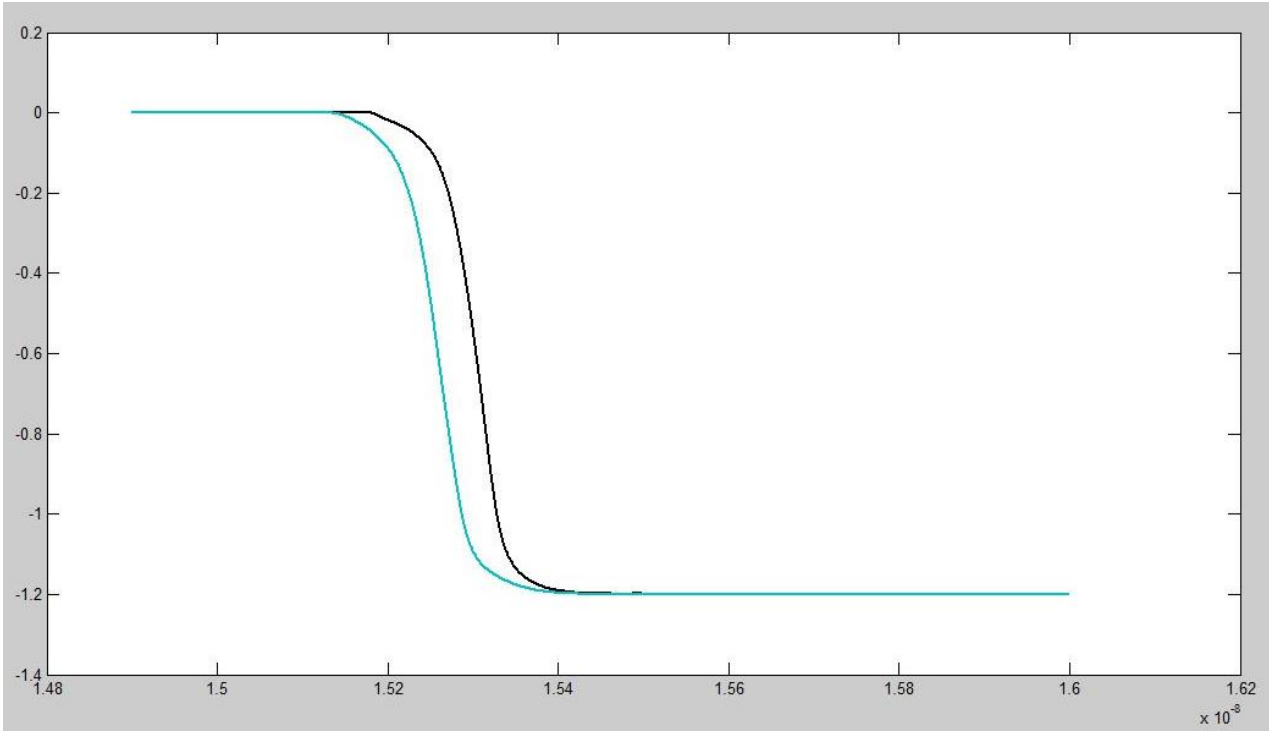


Figure 3.20 : Original SIS voltage (light blue) and MIS voltage (Black) in the second case

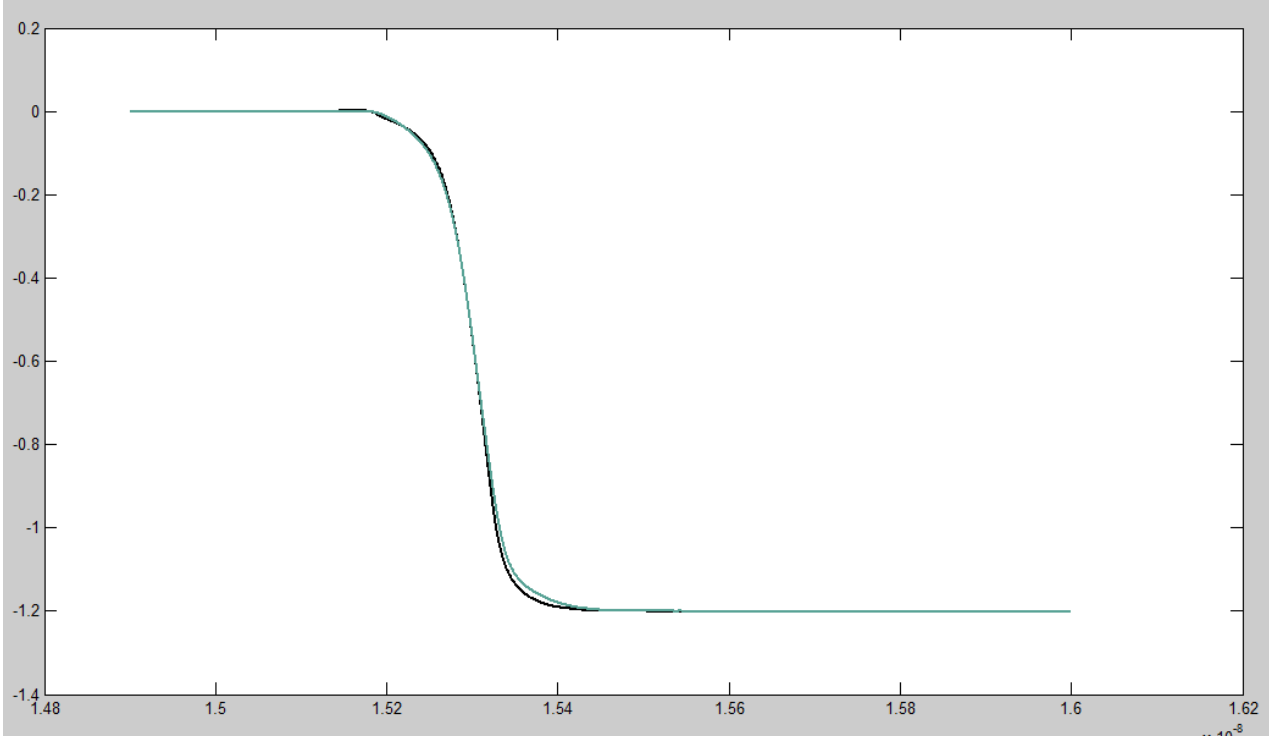


Figure 3.21 : Shifted SIS voltage (light blue) and MIS voltage (Black) in the second case

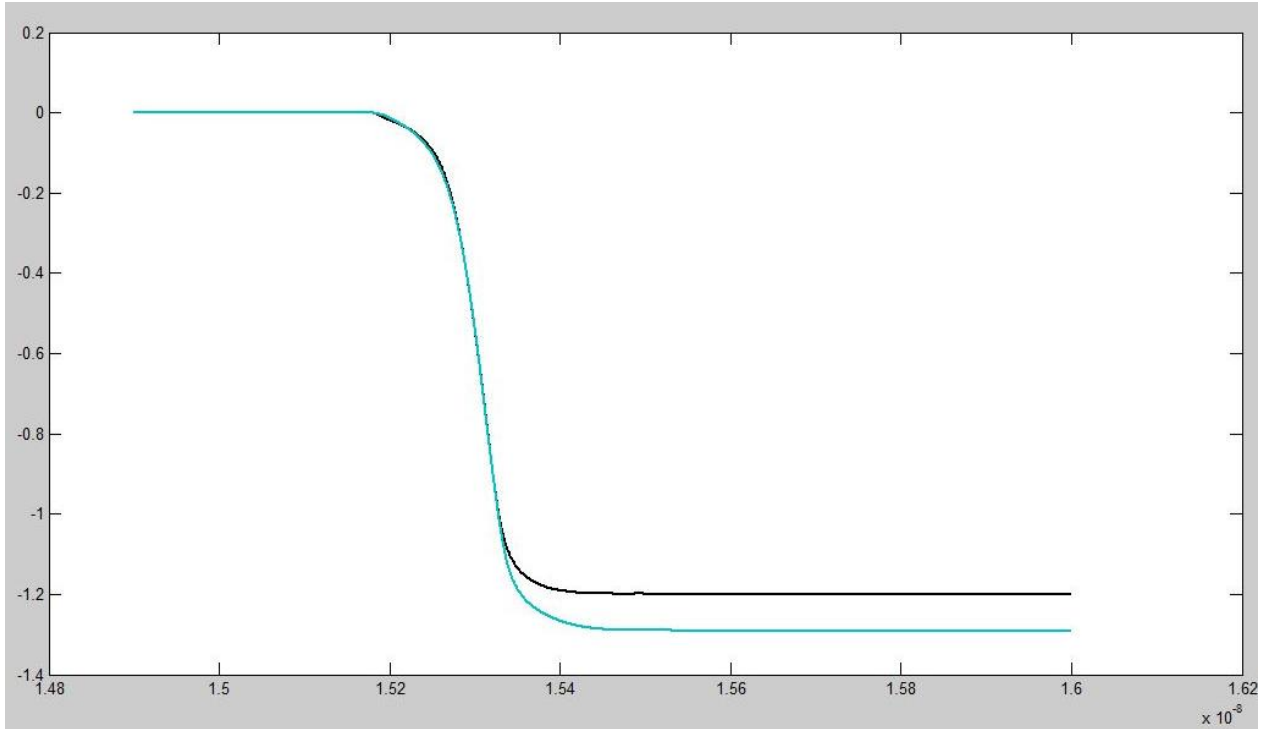


Figure 3.22 : Modified SIS voltage (light blue) and MIS voltage (Black) in the second case

4 Complete current manipulation solution

In the previous section, we proved the basic concepts of the current shifting and scaling method. In this section, the algorithm, that comprises these basic concepts, will be detailed. The algorithm can be divided into two major scenarios. The scenarios represent the type of analysis. There is a max-delay and min-delay scenario.

4.1 Max delay scenario

4.1.1 Characterization Procedure

The procedure for the characterization of the max delay scenario requires, in addition to the simulation of the two SIS cases, the simulation of the MIS case. The MIS case will have its inputs switch simultaneously. The input transition time of both inputs

in the MIS case must be equal. The delay and transition time error is recorded. The current shift value and multiplication factor are calculated. These values are recorded in the library.

Figure 4.1 illustrated the exact procedure for the characterization step after alteration. The addition step is an overhead on the characterization process. The overhead is significant. The addition MIS case for a 2-input gate will represent a new arc in addition to the original two arcs. This is a 33% increase to processing time. In 3-inputs gate, there would be 4 MIS cases. There is one MIS case that account for switching of the three inputs simultaneously. The other three MIS cases occur when you iterate the stabilization of one of the input on a specific value. The 4 MIS cases are added to the 3 SIS cases. This would lead to a total of 7 cases. This would account for an increase of 133%. If we apply the same concept to a 4-input gate, the MIS cases would be 11 cases. The number of SIS cases for a 4-input gate is 4 cases. The increase in the number of cases is 275%. Although the increase of cases in the characterization process is significant, the characterization process occurs once. The correction possible by this method would justify the increase in the processing time in characterization time. The number of case increase is inherent in the Multiple Input problem.

Figure 4.2 shows an example of CCS model library. The figure illustrates how the current table is stored in index_3. Index_1 and index_2 store the input voltage transition time and out capacitance respectively for this specific current table. The value for the current shift value and multiplication factor will be added as index_3 and index_4

respectively. The current table will have index_5 as an identifier. The model will not suffer major increase in the data. This would maintain the model size.

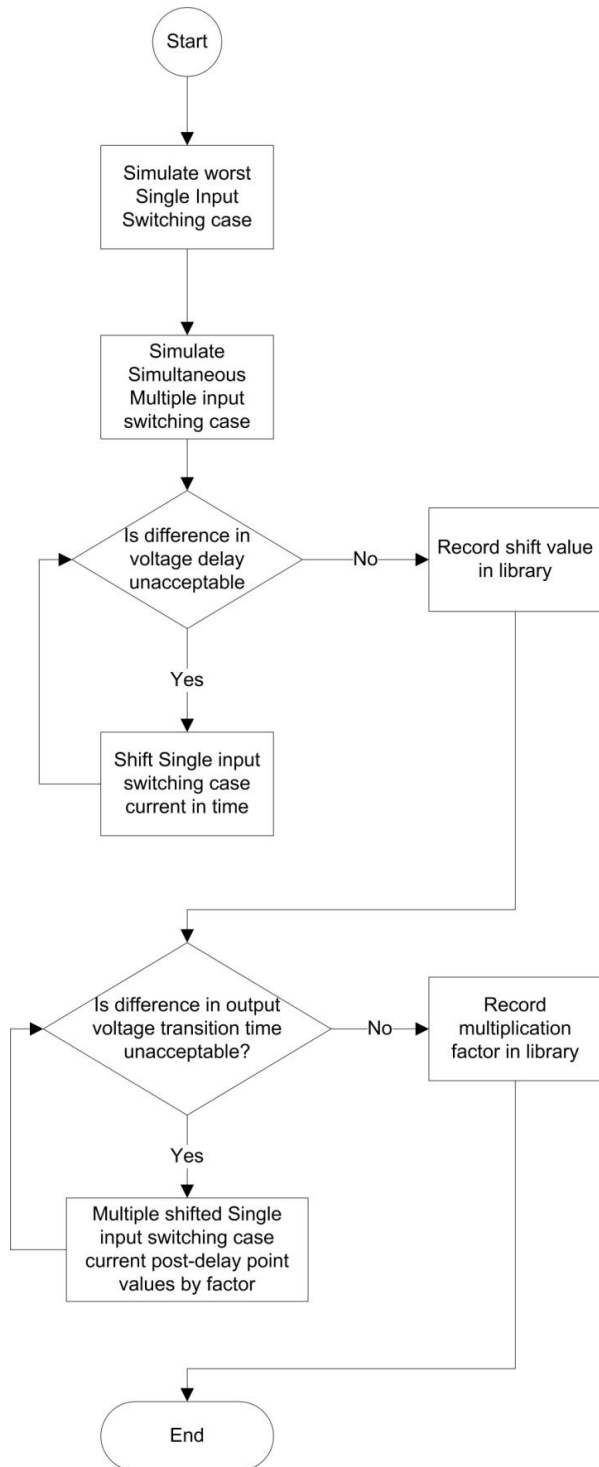


Figure 4.1 : Max delay scenario characterization procedure

```

pin (OUT) {
  . . .
  timing () {
    related_pin : "IN"-;
    . . .
    output_current_fall () {
      vector ("LOOKUP_TABLE_1x1x5") {
        reference_time : 5.06; /* Time of input crossing
          threshold */
        index_1("0.040"); /* Input transition */
        index_2("0.900"); /* Output capacitance */
        index_3("5.079e+00, 5.093e+00, 5.152e+00,
          5.170e+00, 5.352e+00"); /* Time values */
        /* Output charging current: */
        values("-5.784e-02, -5.980e-02, -5.417e-02,
          -4.257e-02, -2.184e-03");
      }
      . . .
    }
    . . .
  }
  . . .
}

```

Figure 4.2 : CCS model library [1]

4.1.2 Run-time procedure

The run-time procedure for max-delay analysis after characterization is very simple. The STA engine would initiate the error correction, if the following conditions are satisfied:

- The two inputs switching windows coincide.
- If the transition times of the inputs are within a pre-set tolerance of each other.

The second condition concerning the tolerance is meant to safe guard against variation.

It would ensure the detection of any possible MIS event. If these conditions are

satisfied, the STA engine would use the current shift value and multiplication factor and apply it on the SIS current values as stated in the matlab verification section.

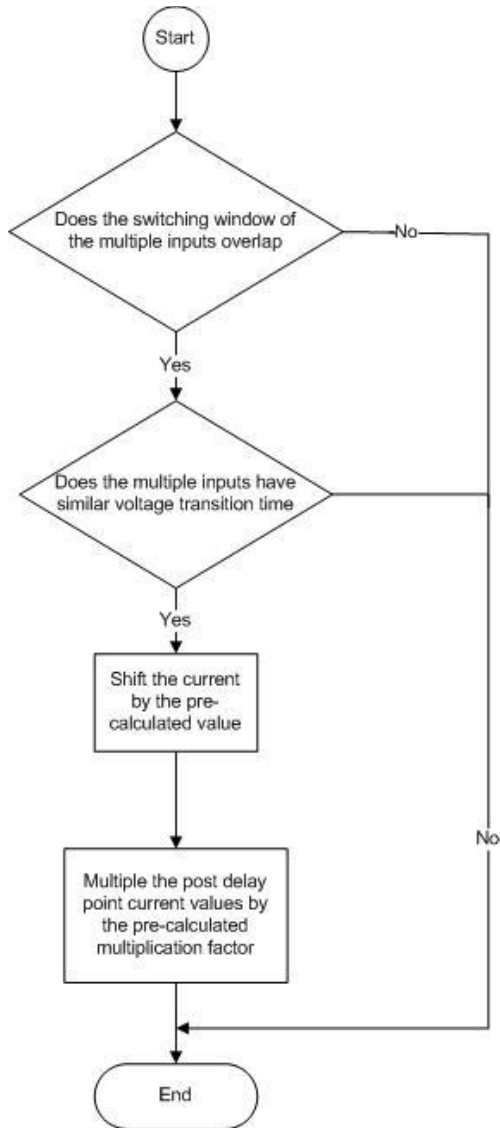


Figure 4.3 : Max-delay scenario run-time procedure

4.2 Min-delay scenario

The minimum delay scenario requires a correction in the run-time only. This alleviates the overhead in the characterization time. The run-time procedure is very simple. The STA engine checks that the inputs have the same switching windows. When this condition is satisfied, the current values are added together incorporating any delay between the inputs. This means that the current would be delayed depending on the occurrence of the input edge. This method is accurate, flexible and simple

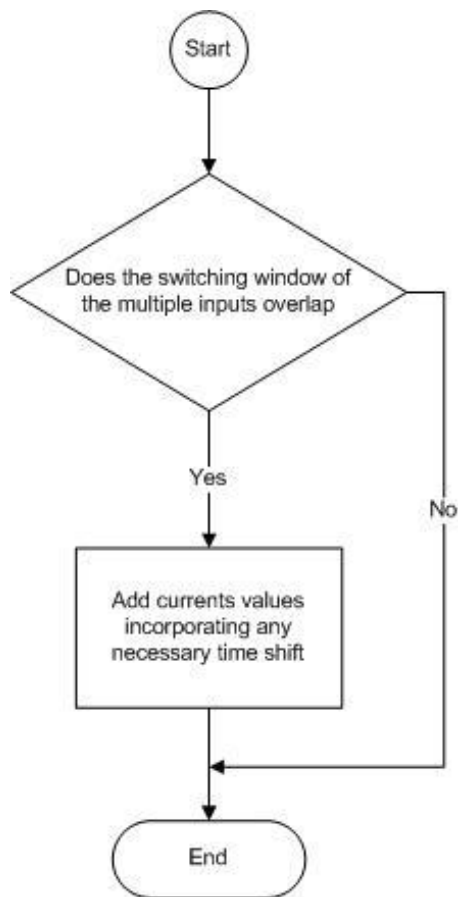


Figure 4.4 : Min-delay scenario run-time procedure

5 Conclusion

This dissertation presented a simple, flexible and diverse solution for the MIS problem in STA. The solution changes in the characterization process for STA models. The current shift value and multiplication factor are calculated during the modified characterization process. They are then used during the run-time processing. This thesis also present the only solution for the minimum delay analysis MIS prolem. The solution takes advantage of the CCS model and maintains its accuracy. The study included a practical and realistic algorithm that can guide the reader through implementation of this solution. The implementation of this solution would improve ASIC designed chips by increasing their yield. The idea should spark interest of the industry in this problem and motivate the implementation of this solution.

6 Future works

The next phase should include relating the current shift value to the time separation between the edges during MIS. The characterization tools and flows should be modified to calculate the shift value and multiplication factor. The introduction of more efficient and accurate method for calculating the current shift value and multiplication factor should be explored. An accuracy study using modified CCS model, which would require syntax modification and modified STA engine is needed. This study is needed to assure the feasibility and applicability of this.

7 Publication

Khaled El-Kinawi, Yehea Ismail “Current manipulation technique for multiple input switching problem in Static Timing Analysis” (in preparation)

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Appendix

Spice code

```
1 $NAND
2
3 .param LL =0.06um WW=0.195um TWW='4*WW/3' TT=100p vdd=1.2V period=10n
4
5 vdc d 0 dc vdd
6
7 $Lower input switching structure
8 va a 0 PULSE(0 vdd delay TT TT 'period/2' period)
9 vb b 0 dc vdd
10 mn1 net1 a 0 0 nch L=LL W=WW
11 mn2 out1 b net1 0 nch L=LL W=WW
12 mp1 d a out1 d pch L=LL W=TWW
13 mp2 d b out1 d pch L=LL W=TWW
14 C1 out2 0 cc
15 vtest out1 out2 dc 0V
16
17 $Upper input switching
18 vau au 0 dc vdd
19 vbu bu 0 PULSE(0 vdd delay 'nn*TT' TT 'period/2' period)
20 mnul netu1 au 0 0 nch L=LL W=WW
21 mnu2 outu1 bu netu1 0 nch L=LL W=WW
22 mpul d au outu1 d pch L=LL W=TWW
23 mpu2 d bu outu1 d pch L=LL W=TWW
24 Cul outu2 0 cc
25 vutest outu1 outu2 dc 0V
26
27 $Simultaneous structure
28 valpha alpha 0 PULSE(0 vdd 'delay' TT TT 'period/3' period)
29 vbeta beta 0 PULSE(0 vdd 'delay+shift' 'nn*TT' TT 'period/2' period)
30 mns1 nets1 alpha 0 0 nch L=LL W=WW
31 mns2 outs1 beta nets1 0 nch L=LL W=WW
32 mps1 d alpha outs1 d pch L=LL W=TWW
33 mps2 d beta outs1 d pch L=LL W=TWW
34 Csl outs2 0 cc
```

```

35 vstest outs1 outs2 dc 0V
36 .op
37 .option runlvl=6 post=2 brief dccap
38
39 .TRAN 1f 17n sweep DATA=DATAN
40 $.TRAN 1f 17n sweep DATA=DATAR
41 $.TRAN 1f 17n sweep DATA=DATAM
42 $.TRAN 1f 16n sweep DATA=DATAO
43
44
45 .MEAS TPHLLS TRIG PAR('V(a) -0.5*VDD') VAL=0 RISE=2
46 + TARG PAR('V(out1) -0.5*VDD') VAL=0 FALL=2
47
48 .MEAS TPHLUS TRIG PAR('V(bu) -0.5*VDD') VAL=0 RISE=2
49 + TARG PAR('V(outu1) -0.5*VDD') VAL=0 FALL=2
50
51 .MEAS TPHLSS TRIG PAR('min(V(alpha),V(beta)) -0.5*VDD') VAL=0 RISE=2
52 + TARG PAR('V(outs1) -0.5*VDD') VAL=0 FALL=2
53 .MEAS FALLTIMEL TRIG PAR('V(out1)-0.9*VDD') VAL=0 FALL=2
54 + TARG PAR('V(out1)-0.1*VDD') VAL=0 FALL=2
55 .MEAS FALLTIMEU TRIG PAR('V(outu1)-0.9*VDD') VAL=0 FALL=2
56 + TARG PAR('V(outu1)-0.1*VDD') VAL=0 FALL=2
57 .MEAS FALLTIMES TRIG PAR('V(outs1)-0.9*VDD') VAL=0 FALL=2
58 + TARG PAR('V(outs1)-0.1*VDD') VAL=0 FALL=2
59
60
61 .MEAS TRAN ivtestz when I(vtest)=0 FROM=15ns TO=16ns FALL=2
62 .MEAS TRAN ivstestz when I(vstest)=0 FROM=15ns TO=16ns FALL=2
63
64 .MEAS idelay PARAM='ivstestz-ivtestz'
65
66 .MEAS TRAN IMINL MIN I(vtest) FROM=14ns TO=16ns
67 .MEAS TRAN IMINU MIN I(vutest) FROM=14ns TO=16ns
68 .MEAS TRAN IMINS MIN I(vstest) FROM=14ns TO=16ns

```



```

69
70 $.print I(vtest) I(vstest)
71
72 $ to check worst current error
73 .DATA DATAO
74 TT WW shift cc nn
75 150p 0.975um 0 0.5ff 1
76 .ENDDATA
77 $to check worst transtion error
78 .DATA DATAM
79 TT WW shift cc nn
80 5.00E-10 1.95E-07 0 5.00E-16 1
81 .ENDDATA
82 $to repair data
83 .DATA DATAR
84 TT WW shift cc nn
85 1.00E-12 3.90E-07 0 5.00E-16 1
86 1.00E-12 5.85E-07 0 5.00E-16 1
87 1.00E-12 5.85E-07 0 1.00E-15 1
88 1.00E-12 7.80E-07 0 5.00E-16 1
89 1.00E-12 7.80E-07 0 1.00E-15 1
90 1.00E-12 9.75E-07 0 5.00E-16 1
91 1.00E-12 9.75E-07 0 1.00E-15 1
92 .ENDDATA
93 $ to sample data
94 .DATA DATAN
95 TT WW shift cc nn
96 1p 0.195um 0.00E+00 0.5ff 1
97 1p 0.195um 0.00E+00 1ff 1
98 1p 0.195um 0.00E+00 2ff 1
99 1p 0.195um 0.00E+00 3ff 1
100 1p 0.195um 0.00E+00 4ff 1
101 1p 0.195um 0.00E+00 5ff 1

```

102	2p	0.195um	0.00E+00	0.5ff	1
103	2p	0.195um	0.00E+00	1ff	1
104	2p	0.195um	0.00E+00	2ff	1
105	2p	0.195um	0.00E+00	3ff	1
106	2p	0.195um	0.00E+00	4ff	1
107	2p	0.195um	0.00E+00	5ff	1
108	5p	0.195um	0.00E+00	0.5ff	1
109	5p	0.195um	0.00E+00	1ff	1
110	5p	0.195um	0.00E+00	2ff	1
111	5p	0.195um	0.00E+00	3ff	1
112	5p	0.195um	0.00E+00	4ff	1
113	5p	0.195um	0.00E+00	5ff	1
114	10p	0.195um	0.00E+00	0.5ff	1
115	10p	0.195um	0.00E+00	1ff	1
116	10p	0.195um	0.00E+00	2ff	1
117	10p	0.195um	0.00E+00	3ff	1
118	10p	0.195um	0.00E+00	4ff	1
119	10p	0.195um	0.00E+00	5ff	1
120	20p	0.195um	0.00E+00	0.5ff	1
121	20p	0.195um	0.00E+00	1ff	1
122	20p	0.195um	0.00E+00	2ff	1
123	20p	0.195um	0.00E+00	3ff	1
124	20p	0.195um	0.00E+00	4ff	1
125	20p	0.195um	0.00E+00	5ff	1
126	50p	0.195um	0.00E+00	0.5ff	1
127	50p	0.195um	0.00E+00	1ff	1
128	50p	0.195um	0.00E+00	2ff	1
129	50p	0.195um	0.00E+00	3ff	1
130	50p	0.195um	0.00E+00	4ff	1
131	50p	0.195um	0.00E+00	5ff	1
132	75p	0.195um	0.00E+00	0.5ff	1
133	75p	0.195um	0.00E+00	1ff	1
134	75p	0.195um	0.00E+00	2ff	1
135	75p	0.195um	0.00E+00	3ff	1

136	75p	0.195um	0.00E+00	4ff	1
137	75p	0.195um	0.00E+00	5ff	1
138	100p	0.195um	0.00E+00	0.5ff	1
139	100p	0.195um	0.00E+00	1ff	1
140	100p	0.195um	0.00E+00	2ff	1
141	100p	0.195um	0.00E+00	3ff	1
142	100p	0.195um	0.00E+00	4ff	1
143	100p	0.195um	0.00E+00	5ff	1
144	150p	0.195um	0.00E+00	0.5ff	1
145	150p	0.195um	0.00E+00	1ff	1
146	150p	0.195um	0.00E+00	2ff	1
147	150p	0.195um	0.00E+00	3ff	1
148	150p	0.195um	0.00E+00	4ff	1
149	150p	0.195um	0.00E+00	5ff	1
150	200p	0.195um	0.00E+00	0.5ff	1
151	200p	0.195um	0.00E+00	1ff	1
152	200p	0.195um	0.00E+00	2ff	1
153	200p	0.195um	0.00E+00	3ff	1
154	200p	0.195um	0.00E+00	4ff	1
155	200p	0.195um	0.00E+00	5ff	1
156	250p	0.195um	0.00E+00	0.5ff	1
157	250p	0.195um	0.00E+00	1ff	1
158	250p	0.195um	0.00E+00	2ff	1
159	250p	0.195um	0.00E+00	3ff	1
160	250p	0.195um	0.00E+00	4ff	1
161	250p	0.195um	0.00E+00	5ff	1
162	300p	0.195um	0.00E+00	0.5ff	1
163	300p	0.195um	0.00E+00	1ff	1
164	300p	0.195um	0.00E+00	2ff	1
165	300p	0.195um	0.00E+00	3ff	1
166	300p	0.195um	0.00E+00	4ff	1
167	300p	0.195um	0.00E+00	5ff	1
168	350p	0.195um	0.00E+00	0.5ff	1
169	350p	0.195um	0.00E+00	1ff	1

170	350p	0.195um	0.00E+00	2ff	1
171	350p	0.195um	0.00E+00	3ff	1
172	350p	0.195um	0.00E+00	4ff	1
173	350p	0.195um	0.00E+00	5ff	1
174	400p	0.195um	0.00E+00	0.5ff	1
175	400p	0.195um	0.00E+00	1ff	1
176	400p	0.195um	0.00E+00	2ff	1
177	400p	0.195um	0.00E+00	3ff	1
178	400p	0.195um	0.00E+00	4ff	1
179	400p	0.195um	0.00E+00	5ff	1
180	450p	0.195um	0.00E+00	0.5ff	1
181	450p	0.195um	0.00E+00	1ff	1
182	450p	0.195um	0.00E+00	2ff	1
183	450p	0.195um	0.00E+00	3ff	1
184	450p	0.195um	0.00E+00	4ff	1
185	450p	0.195um	0.00E+00	5ff	1
186	500p	0.195um	0.00E+00	0.5ff	1
187	500p	0.195um	0.00E+00	1ff	1
188	500p	0.195um	0.00E+00	2ff	1
189	500p	0.195um	0.00E+00	3ff	1
190	500p	0.195um	0.00E+00	4ff	1
191	500p	0.195um	0.00E+00	5ff	1
192	750p	0.195um	0.00E+00	0.5ff	1
193	750p	0.195um	0.00E+00	1ff	1
194	750p	0.195um	0.00E+00	2ff	1
195	750p	0.195um	0.00E+00	3ff	1
196	750p	0.195um	0.00E+00	4ff	1
197	750p	0.195um	0.00E+00	5ff	1
198	1p	0.39um	0.00E+00	0.5ff	1
199	1p	0.39um	0.00E+00	1ff	1
200	1p	0.39um	0.00E+00	2ff	1
201	1p	0.39um	0.00E+00	3ff	1
202	1p	0.39um	0.00E+00	4ff	1
203	1p	0.39um	0.00E+00	5ff	1

204	2p	0.39um	0.00E+00	0.5ff	1
205	2p	0.39um	0.00E+00	1ff	1
206	2p	0.39um	0.00E+00	2ff	1
207	2p	0.39um	0.00E+00	3ff	1
208	2p	0.39um	0.00E+00	4ff	1
209	2p	0.39um	0.00E+00	5ff	1
210	5p	0.39um	0.00E+00	0.5ff	1
211	5p	0.39um	0.00E+00	1ff	1
212	5p	0.39um	0.00E+00	2ff	1
213	5p	0.39um	0.00E+00	3ff	1
214	5p	0.39um	0.00E+00	4ff	1
215	5p	0.39um	0.00E+00	5ff	1
216	10p	0.39um	0.00E+00	0.5ff	1
217	10p	0.39um	0.00E+00	1ff	1
218	10p	0.39um	0.00E+00	2ff	1
219	10p	0.39um	0.00E+00	3ff	1
220	10p	0.39um	0.00E+00	4ff	1
221	10p	0.39um	0.00E+00	5ff	1
222	20p	0.39um	0.00E+00	0.5ff	1
223	20p	0.39um	0.00E+00	1ff	1
224	20p	0.39um	0.00E+00	2ff	1
225	20p	0.39um	0.00E+00	3ff	1
226	20p	0.39um	0.00E+00	4ff	1
227	20p	0.39um	0.00E+00	5ff	1
228	50p	0.39um	0.00E+00	0.5ff	1
229	50p	0.39um	0.00E+00	1ff	1
230	50p	0.39um	0.00E+00	2ff	1
231	50p	0.39um	0.00E+00	3ff	1
232	50p	0.39um	0.00E+00	4ff	1
233	50p	0.39um	0.00E+00	5ff	1
234	75p	0.39um	0.00E+00	0.5ff	1
235	75p	0.39um	0.00E+00	1ff	1
236	75p	0.39um	0.00E+00	2ff	1
237	75p	0.39um	0.00E+00	3ff	1

238	75p	0.39um	0.00E+00	4ff	1
239	75p	0.39um	0.00E+00	5ff	1
240	100p	0.39um	0.00E+00	0.5ff	1
241	100p	0.39um	0.00E+00	1ff	1
242	100p	0.39um	0.00E+00	2ff	1
243	100p	0.39um	0.00E+00	3ff	1
244	100p	0.39um	0.00E+00	4ff	1
245	100p	0.39um	0.00E+00	5ff	1
246	150p	0.39um	0.00E+00	0.5ff	1
247	150p	0.39um	0.00E+00	1ff	1
248	150p	0.39um	0.00E+00	2ff	1
249	150p	0.39um	0.00E+00	3ff	1
250	150p	0.39um	0.00E+00	4ff	1
251	150p	0.39um	0.00E+00	5ff	1
252	200p	0.39um	0.00E+00	0.5ff	1
253	200p	0.39um	0.00E+00	1ff	1
254	200p	0.39um	0.00E+00	2ff	1
255	200p	0.39um	0.00E+00	3ff	1
256	200p	0.39um	0.00E+00	4ff	1
257	200p	0.39um	0.00E+00	5ff	1
258	250p	0.39um	0.00E+00	0.5ff	1
259	250p	0.39um	0.00E+00	1ff	1
260	250p	0.39um	0.00E+00	2ff	1
261	250p	0.39um	0.00E+00	3ff	1
262	250p	0.39um	0.00E+00	4ff	1
263	250p	0.39um	0.00E+00	5ff	1
264	300p	0.39um	0.00E+00	0.5ff	1
265	300p	0.39um	0.00E+00	1ff	1
266	300p	0.39um	0.00E+00	2ff	1
267	300p	0.39um	0.00E+00	3ff	1
268	300p	0.39um	0.00E+00	4ff	1
269	300p	0.39um	0.00E+00	5ff	1
270	350p	0.39um	0.00E+00	0.5ff	1
271	350p	0.39um	0.00E+00	1ff	1

272	350p	0.39um	0.00E+00	2ff	1
273	350p	0.39um	0.00E+00	3ff	1
274	350p	0.39um	0.00E+00	4ff	1
275	350p	0.39um	0.00E+00	5ff	1
276	400p	0.39um	0.00E+00	0.5ff	1
277	400p	0.39um	0.00E+00	1ff	1
278	400p	0.39um	0.00E+00	2ff	1
279	400p	0.39um	0.00E+00	3ff	1
280	400p	0.39um	0.00E+00	4ff	1
281	400p	0.39um	0.00E+00	5ff	1
282	450p	0.39um	0.00E+00	0.5ff	1
283	450p	0.39um	0.00E+00	1ff	1
284	450p	0.39um	0.00E+00	2ff	1
285	450p	0.39um	0.00E+00	3ff	1
286	450p	0.39um	0.00E+00	4ff	1
287	450p	0.39um	0.00E+00	5ff	1
288	500p	0.39um	0.00E+00	0.5ff	1
289	500p	0.39um	0.00E+00	1ff	1
290	500p	0.39um	0.00E+00	2ff	1
291	500p	0.39um	0.00E+00	3ff	1
292	500p	0.39um	0.00E+00	4ff	1
293	500p	0.39um	0.00E+00	5ff	1
294	750p	0.39um	0.00E+00	0.5ff	1
295	750p	0.39um	0.00E+00	1ff	1
296	750p	0.39um	0.00E+00	2ff	1
297	750p	0.39um	0.00E+00	3ff	1
298	750p	0.39um	0.00E+00	4ff	1
299	750p	0.39um	0.00E+00	5ff	1
300	1p	0.585um	0.00E+00	0.5ff	1
301	1p	0.585um	0.00E+00	1ff	1
302	1p	0.585um	0.00E+00	2ff	1
303	1p	0.585um	0.00E+00	3ff	1
304	1p	0.585um	0.00E+00	4ff	1
305	1p	0.585um	0.00E+00	5ff	1

306	2p	0.585um	0.00E+00	0.5ff	1
307	2p	0.585um	0.00E+00	1ff	1
308	2p	0.585um	0.00E+00	2ff	1
309	2p	0.585um	0.00E+00	3ff	1
310	2p	0.585um	0.00E+00	4ff	1
311	2p	0.585um	0.00E+00	5ff	1
312	5p	0.585um	0.00E+00	0.5ff	1
313	5p	0.585um	0.00E+00	1ff	1
314	5p	0.585um	0.00E+00	2ff	1
315	5p	0.585um	0.00E+00	3ff	1
316	5p	0.585um	0.00E+00	4ff	1
317	5p	0.585um	0.00E+00	5ff	1
318	10p	0.585um	0.00E+00	0.5ff	1
319	10p	0.585um	0.00E+00	1ff	1
320	10p	0.585um	0.00E+00	2ff	1
321	10p	0.585um	0.00E+00	3ff	1
322	10p	0.585um	0.00E+00	4ff	1
323	10p	0.585um	0.00E+00	5ff	1
324	20p	0.585um	0.00E+00	0.5ff	1
325	20p	0.585um	0.00E+00	1ff	1
326	20p	0.585um	0.00E+00	2ff	1
327	20p	0.585um	0.00E+00	3ff	1
328	20p	0.585um	0.00E+00	4ff	1
329	20p	0.585um	0.00E+00	5ff	1
330	50p	0.585um	0.00E+00	0.5ff	1
331	50p	0.585um	0.00E+00	1ff	1
332	50p	0.585um	0.00E+00	2ff	1
333	50p	0.585um	0.00E+00	3ff	1
334	50p	0.585um	0.00E+00	4ff	1
335	50p	0.585um	0.00E+00	5ff	1
336	75p	0.585um	0.00E+00	0.5ff	1
337	75p	0.585um	0.00E+00	1ff	1
338	75p	0.585um	0.00E+00	2ff	1
339	75p	0.585um	0.00E+00	3ff	1

340	75p	0.585um	0.00E+00	4ff	1
341	75p	0.585um	0.00E+00	5ff	1
342	100p	0.585um	0.00E+00	0.5ff	1
343	100p	0.585um	0.00E+00	1ff	1
344	100p	0.585um	0.00E+00	2ff	1
345	100p	0.585um	0.00E+00	3ff	1
346	100p	0.585um	0.00E+00	4ff	1
347	100p	0.585um	0.00E+00	5ff	1
348	150p	0.585um	0.00E+00	0.5ff	1
349	150p	0.585um	0.00E+00	1ff	1
350	150p	0.585um	0.00E+00	2ff	1
351	150p	0.585um	0.00E+00	3ff	1
352	150p	0.585um	0.00E+00	4ff	1
353	150p	0.585um	0.00E+00	5ff	1
354	200p	0.585um	0.00E+00	0.5ff	1
355	200p	0.585um	0.00E+00	1ff	1
356	200p	0.585um	0.00E+00	2ff	1
357	200p	0.585um	0.00E+00	3ff	1
358	200p	0.585um	0.00E+00	4ff	1
359	200p	0.585um	0.00E+00	5ff	1
360	250p	0.585um	0.00E+00	0.5ff	1
361	250p	0.585um	0.00E+00	1ff	1
362	250p	0.585um	0.00E+00	2ff	1
363	250p	0.585um	0.00E+00	3ff	1
364	250p	0.585um	0.00E+00	4ff	1
365	250p	0.585um	0.00E+00	5ff	1
366	300p	0.585um	0.00E+00	0.5ff	1
367	300p	0.585um	0.00E+00	1ff	1
368	300p	0.585um	0.00E+00	2ff	1
369	300p	0.585um	0.00E+00	3ff	1
370	300p	0.585um	0.00E+00	4ff	1
371	300p	0.585um	0.00E+00	5ff	1
372	350p	0.585um	0.00E+00	0.5ff	1
373	350p	0.585um	0.00E+00	1ff	1

374	350p	0.585um	0.00E+00	2ff	1
375	350p	0.585um	0.00E+00	3ff	1
376	350p	0.585um	0.00E+00	4ff	1
377	350p	0.585um	0.00E+00	5ff	1
378	400p	0.585um	0.00E+00	0.5ff	1
379	400p	0.585um	0.00E+00	1ff	1
380	400p	0.585um	0.00E+00	2ff	1
381	400p	0.585um	0.00E+00	3ff	1
382	400p	0.585um	0.00E+00	4ff	1
383	400p	0.585um	0.00E+00	5ff	1
384	450p	0.585um	0.00E+00	0.5ff	1
385	450p	0.585um	0.00E+00	1ff	1
386	450p	0.585um	0.00E+00	2ff	1
387	450p	0.585um	0.00E+00	3ff	1
388	450p	0.585um	0.00E+00	4ff	1
389	450p	0.585um	0.00E+00	5ff	1
390	500p	0.585um	0.00E+00	0.5ff	1
391	500p	0.585um	0.00E+00	1ff	1
392	500p	0.585um	0.00E+00	2ff	1
393	500p	0.585um	0.00E+00	3ff	1
394	500p	0.585um	0.00E+00	4ff	1
395	500p	0.585um	0.00E+00	5ff	1
396	750p	0.585um	0.00E+00	0.5ff	1
397	750p	0.585um	0.00E+00	1ff	1
398	750p	0.585um	0.00E+00	2ff	1
399	750p	0.585um	0.00E+00	3ff	1
400	750p	0.585um	0.00E+00	4ff	1
401	750p	0.585um	0.00E+00	5ff	1
402	1p	0.78um	0.00E+00	0.5ff	1
403	1p	0.78um	0.00E+00	1ff	1
404	1p	0.78um	0.00E+00	2ff	1
405	1p	0.78um	0.00E+00	3ff	1
406	1p	0.78um	0.00E+00	4ff	1
407	1p	0.78um	0.00E+00	5ff	1

408	2p	0.78um	0.00E+00	0.5ff	1
409	2p	0.78um	0.00E+00	1ff	1
410	2p	0.78um	0.00E+00	2ff	1
411	2p	0.78um	0.00E+00	3ff	1
412	2p	0.78um	0.00E+00	4ff	1
413	2p	0.78um	0.00E+00	5ff	1
414	5p	0.78um	0.00E+00	0.5ff	1
415	5p	0.78um	0.00E+00	1ff	1
416	5p	0.78um	0.00E+00	2ff	1
417	5p	0.78um	0.00E+00	3ff	1
418	5p	0.78um	0.00E+00	4ff	1
419	5p	0.78um	0.00E+00	5ff	1
420	10p	0.78um	0.00E+00	0.5ff	1
421	10p	0.78um	0.00E+00	1ff	1
422	10p	0.78um	0.00E+00	2ff	1
423	10p	0.78um	0.00E+00	3ff	1
424	10p	0.78um	0.00E+00	4ff	1
425	10p	0.78um	0.00E+00	5ff	1
426	20p	0.78um	0.00E+00	0.5ff	1
427	20p	0.78um	0.00E+00	1ff	1
428	20p	0.78um	0.00E+00	2ff	1
429	20p	0.78um	0.00E+00	3ff	1
430	20p	0.78um	0.00E+00	4ff	1
431	20p	0.78um	0.00E+00	5ff	1
432	50p	0.78um	0.00E+00	0.5ff	1
433	50p	0.78um	0.00E+00	1ff	1
434	50p	0.78um	0.00E+00	2ff	1
435	50p	0.78um	0.00E+00	3ff	1
436	50p	0.78um	0.00E+00	4ff	1
437	50p	0.78um	0.00E+00	5ff	1
438	75p	0.78um	0.00E+00	0.5ff	1
439	75p	0.78um	0.00E+00	1ff	1
440	75p	0.78um	0.00E+00	2ff	1
441	75p	0.78um	0.00E+00	3ff	1

442	75p	0.78um	0.00E+00	4ff	1
443	75p	0.78um	0.00E+00	5ff	1
444	100p	0.78um	0.00E+00	0.5ff	1
445	100p	0.78um	0.00E+00	1ff	1
446	100p	0.78um	0.00E+00	2ff	1
447	100p	0.78um	0.00E+00	3ff	1
448	100p	0.78um	0.00E+00	4ff	1
449	100p	0.78um	0.00E+00	5ff	1
450	150p	0.78um	0.00E+00	0.5ff	1
451	150p	0.78um	0.00E+00	1ff	1
452	150p	0.78um	0.00E+00	2ff	1
453	150p	0.78um	0.00E+00	3ff	1
454	150p	0.78um	0.00E+00	4ff	1
455	150p	0.78um	0.00E+00	5ff	1
456	200p	0.78um	0.00E+00	0.5ff	1
457	200p	0.78um	0.00E+00	1ff	1
458	200p	0.78um	0.00E+00	2ff	1
459	200p	0.78um	0.00E+00	3ff	1
460	200p	0.78um	0.00E+00	4ff	1
461	200p	0.78um	0.00E+00	5ff	1
462	250p	0.78um	0.00E+00	0.5ff	1
463	250p	0.78um	0.00E+00	1ff	1
464	250p	0.78um	0.00E+00	2ff	1
465	250p	0.78um	0.00E+00	3ff	1
466	250p	0.78um	0.00E+00	4ff	1
467	250p	0.78um	0.00E+00	5ff	1
468	300p	0.78um	0.00E+00	0.5ff	1
469	300p	0.78um	0.00E+00	1ff	1
470	300p	0.78um	0.00E+00	2ff	1
471	300p	0.78um	0.00E+00	3ff	1
472	300p	0.78um	0.00E+00	4ff	1
473	300p	0.78um	0.00E+00	5ff	1
474	350p	0.78um	0.00E+00	0.5ff	1
475	350p	0.78um	0.00E+00	1ff	1

476	350p	0.78um	0.00E+00	2ff	1
477	350p	0.78um	0.00E+00	3ff	1
478	350p	0.78um	0.00E+00	4ff	1
479	350p	0.78um	0.00E+00	5ff	1
480	400p	0.78um	0.00E+00	0.5ff	1
481	400p	0.78um	0.00E+00	1ff	1
482	400p	0.78um	0.00E+00	2ff	1
483	400p	0.78um	0.00E+00	3ff	1
484	400p	0.78um	0.00E+00	4ff	1
485	400p	0.78um	0.00E+00	5ff	1
486	450p	0.78um	0.00E+00	0.5ff	1
487	450p	0.78um	0.00E+00	1ff	1
488	450p	0.78um	0.00E+00	2ff	1
489	450p	0.78um	0.00E+00	3ff	1
490	450p	0.78um	0.00E+00	4ff	1
491	450p	0.78um	0.00E+00	5ff	1
492	500p	0.78um	0.00E+00	0.5ff	1
493	500p	0.78um	0.00E+00	1ff	1
494	500p	0.78um	0.00E+00	2ff	1
495	500p	0.78um	0.00E+00	3ff	1
496	500p	0.78um	0.00E+00	4ff	1
497	500p	0.78um	0.00E+00	5ff	1
498	750p	0.78um	0.00E+00	0.5ff	1
499	750p	0.78um	0.00E+00	1ff	1
500	750p	0.78um	0.00E+00	2ff	1
501	750p	0.78um	0.00E+00	3ff	1
502	750p	0.78um	0.00E+00	4ff	1
503	750p	0.78um	0.00E+00	5ff	1
504	1p	0.975um	0.00E+00	0.5ff	1
505	1p	0.975um	0.00E+00	1ff	1
506	1p	0.975um	0.00E+00	2ff	1
507	1p	0.975um	0.00E+00	3ff	1
508	1p	0.975um	0.00E+00	4ff	1
509	1p	0.975um	0.00E+00	5ff	1

510	2p	0.975um	0.00E+00	0.5ff	1
511	2p	0.975um	0.00E+00	1ff	1
512	2p	0.975um	0.00E+00	2ff	1
513	2p	0.975um	0.00E+00	3ff	1
514	2p	0.975um	0.00E+00	4ff	1
515	2p	0.975um	0.00E+00	5ff	1
516	5p	0.975um	0.00E+00	0.5ff	1
517	5p	0.975um	0.00E+00	1ff	1
518	5p	0.975um	0.00E+00	2ff	1
519	5p	0.975um	0.00E+00	3ff	1
520	5p	0.975um	0.00E+00	4ff	1
521	5p	0.975um	0.00E+00	5ff	1
522	10p	0.975um	0.00E+00	0.5ff	1
523	10p	0.975um	0.00E+00	1ff	1
524	10p	0.975um	0.00E+00	2ff	1
525	10p	0.975um	0.00E+00	3ff	1
526	10p	0.975um	0.00E+00	4ff	1
527	10p	0.975um	0.00E+00	5ff	1
528	20p	0.975um	0.00E+00	0.5ff	1
529	20p	0.975um	0.00E+00	1ff	1
530	20p	0.975um	0.00E+00	2ff	1
531	20p	0.975um	0.00E+00	3ff	1
532	20p	0.975um	0.00E+00	4ff	1
533	20p	0.975um	0.00E+00	5ff	1
534	50p	0.975um	0.00E+00	0.5ff	1
535	50p	0.975um	0.00E+00	1ff	1
536	50p	0.975um	0.00E+00	2ff	1
537	50p	0.975um	0.00E+00	3ff	1
538	50p	0.975um	0.00E+00	4ff	1
539	50p	0.975um	0.00E+00	5ff	1
540	75p	0.975um	0.00E+00	0.5ff	1
541	75p	0.975um	0.00E+00	1ff	1
542	75p	0.975um	0.00E+00	2ff	1
543	75p	0.975um	0.00E+00	3ff	1

544	75p	0.975um	0.00E+00	4ff	1
545	75p	0.975um	0.00E+00	5ff	1
546	100p	0.975um	0.00E+00	0.5ff	1
547	100p	0.975um	0.00E+00	1ff	1
548	100p	0.975um	0.00E+00	2ff	1
549	100p	0.975um	0.00E+00	3ff	1
550	100p	0.975um	0.00E+00	4ff	1
551	100p	0.975um	0.00E+00	5ff	1
552	150p	0.975um	0.00E+00	0.5ff	1
553	150p	0.975um	0.00E+00	1ff	1
554	150p	0.975um	0.00E+00	2ff	1
555	150p	0.975um	0.00E+00	3ff	1
556	150p	0.975um	0.00E+00	4ff	1
557	150p	0.975um	0.00E+00	5ff	1
558	200p	0.975um	0.00E+00	0.5ff	1
559	200p	0.975um	0.00E+00	1ff	1
560	200p	0.975um	0.00E+00	2ff	1
561	200p	0.975um	0.00E+00	3ff	1
562	200p	0.975um	0.00E+00	4ff	1
563	200p	0.975um	0.00E+00	5ff	1
564	250p	0.975um	0.00E+00	0.5ff	1
565	250p	0.975um	0.00E+00	1ff	1
566	250p	0.975um	0.00E+00	2ff	1
567	250p	0.975um	0.00E+00	3ff	1
568	250p	0.975um	0.00E+00	4ff	1
569	250p	0.975um	0.00E+00	5ff	1
570	300p	0.975um	0.00E+00	0.5ff	1
571	300p	0.975um	0.00E+00	1ff	1
572	300p	0.975um	0.00E+00	2ff	1
573	300p	0.975um	0.00E+00	3ff	1
574	300p	0.975um	0.00E+00	4ff	1
575	300p	0.975um	0.00E+00	5ff	1
576	350p	0.975um	0.00E+00	0.5ff	1
577	350p	0.975um	0.00E+00	1ff	1

```

578 350p 0.975um 0.00E+00 2ff 1
579 350p 0.975um 0.00E+00 3ff 1
580 350p 0.975um 0.00E+00 4ff 1
581 350p 0.975um 0.00E+00 5ff 1
582 400p 0.975um 0.00E+00 0.5ff 1
583 400p 0.975um 0.00E+00 1ff 1
584 400p 0.975um 0.00E+00 2ff 1
585 400p 0.975um 0.00E+00 3ff 1
586 400p 0.975um 0.00E+00 4ff 1
587 400p 0.975um 0.00E+00 5ff 1
588 450p 0.975um 0.00E+00 0.5ff 1
589 450p 0.975um 0.00E+00 1ff 1
590 450p 0.975um 0.00E+00 2ff 1
591 450p 0.975um 0.00E+00 3ff 1
592 450p 0.975um 0.00E+00 4ff 1
593 450p 0.975um 0.00E+00 5ff 1
594 500p 0.975um 0.00E+00 0.5ff 1
595 500p 0.975um 0.00E+00 1ff 1
596 500p 0.975um 0.00E+00 2ff 1
597 500p 0.975um 0.00E+00 3ff 1
598 500p 0.975um 0.00E+00 4ff 1
599 500p 0.975um 0.00E+00 5ff 1
600 750p 0.975um 0.00E+00 0.5ff 1
601 750p 0.975um 0.00E+00 1ff 1
602 750p 0.975um 0.00E+00 2ff 1
603 750p 0.975um 0.00E+00 3ff 1
604 750p 0.975um 0.00E+00 4ff 1
605 750p 0.975um 0.00E+00 5ff 1
606 .ENDDATA
607
608 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_bip_npn
609 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfres_sa
610 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmvar
611 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_esd

```



```

612 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rtmom
613 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmvar_25
614 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_disres
615 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_na
616 .lib "./crn65gplus_2d5_1k_v1d0.1" tt
617 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_mim
618 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfrtmom
619 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_na25od33
620 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfres_rpo
621 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_hvt
622 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_na25od33
623 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmmim
624 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_25od33
625 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_res
626 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_lvt
627 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_25ud18
628 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_bip
629 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_mos_cap
630 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_na33
631 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_25ud18
632 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_na33
633 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_18
634 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_na
635 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio
636 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_25od33
637 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_hvt
638 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfind
639 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmos_33
640 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_lvt
641 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_na25
642 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmos_25
643 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_dnw
644 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfjvar
645 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmos
646 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_na25
647 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_rfmos_18
648 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_mos_cap_25
649 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_33
650 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_25
651 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_33
652 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_25
653 .lib "./crn65gplus_2d5_1k_v1d0.1" tt_dio_18
654 .end

```

Matlab code for first case

```
1 Time = [ 1.490000E-08 1.490001E-08 1.490002E-08 1.490003E-08 1.490004E-08]
2 Itest = [ 8.66E-09 8.66E-09 8.66E-09 8.66E-09 8.67E-09]
3 Istest = [ 5.46E-09 5.46E-09 5.46E-09 5.46E-09 5.46E-09]
4 deltao =1533
5 delta =1250
6 mult = 1.15
7 Itest2 = [zeros(1,delta) Itest]
8 Itest3 = Itest2(1:110001)
9 Itest3(19573:110001) = Itest2(19573:110001).*mult
10 Itestsum = cumtrapz(Itest).*20
11 Istestsum = cumtrapz(Istest).*20
12 Itest3sum = cumtrapz(Itest3).*20
13 [c] = find(Istestsum<=-0.6 & Istestsum>-0.61)
14 tsmid = Time(c(1))
15 [c] = find(Itest3sum<=-0.6 & Itest3sum>-0.61)
16 tmmid = Time(c(1))
17 [c] = find(Itestsum<=-0.6 & Itestsum>-0.61)
18 tomid = Time(c(1))
19
20 delerr = tsmid - tmmid
21
22 [c] = find(Istestsum<=-0.12 & Istestsum>-0.15)
23 tsup = Time(c(1))
24 [c] = find(Itest3sum<=-0.12 & Itest3sum>-0.15)
25 tmup = Time(c(1))
26 [c] = find(Itestsum<=-0.12 & Itestsum>-0.15)
27 toup = Time(c(1))
28 [c] = find(Istestsum<=-1.08 & Istestsum>-1.1)
29 tslow = Time(c(1))
30 [c] = find(Itest3sum<=-1.08 & Itest3sum>-1.1)
31 tmlow = Time(c(1))
32 [c] = find(Itestsum<=-1.08 & Itestsum>-1.1)
33 tolow = Time(c(1))
34 trano = tolow -toup
35 trans = tslow - tsup
36 tranm = tmlow - tmup
37 tranerror = trans - tranm
38 pererr = delerr/2.06E-11
39 pertran = tranerror/trans
40
```

Matlab code for second case

```
1 Time = [ 14.90000e-09 14.90001e-09 14.90002e-09 14.90003e-09]
2 Itest = [ -1.3042e-09 -1.3047e-09 -1.3051e-09 -1.3056e-09]
3 Istest = [ -1.2836e-09 -1.2840e-09 -1.2845e-09 -1.2850e-09]
4 deltao =1533
5 delta =4500
6 Itest2 = [zeros(1,delta) Itest]
7 Itest3 = Itest2(1:110001)
8 Itestsum = cumtrapz(Itest).*20
9 Istestsum = cumtrapz(Istest).*20
10 mult = 1.15
11 Itest3(40427:110001) = Itest2(40427:110001).*mult
12 Itest3sum = cumtrapz(Itest3).*20
13 [c] = find(Istestsum<=-0.6 & Istestsum>-0.61)
14 tsmid = Time(c(1))
15 [c] = find(Itest3sum<=-0.6 & Itest3sum>-0.61)
16 trnmid = Time(c(1))
17 [c] = find(Itestsum<=-0.6 & Itestsum>-0.61)
18 tomid = Time(c(1))
19
20 delerr = tsmid - trnmid
21
22 [c] = find(Istestsum<=-0.12 & Istestsum>-0.15)
23 tsup = Time(c(1))
24 [c] = find(Itest3sum<=-0.12 & Itest3sum>-0.15)
25 tmup = Time(c(1))
26 [c] = find(Itestsum<=-0.12 & Itestsum>-0.15)
27 toup = Time(c(1))
28 [c] = find(Istestsum<=-1.08 & Istestsum>-1.1)
29 tslow = Time(c(1))
30 [c] = find(Itest3sum<=-1.08 & Itest3sum>-1.1)
31 tmlow = Time(c(1))
32 [c] = find(Itestsum<=-1.08 & Itestsum>-1.1)
33 tolow = Time(c(1))
34 trano = tolow -toup
35 trans = tslow - tsup
36 tranm = tmlow - tmup
37 tranerror = trans - tranm
38 pertran = tranerror/trans
39 pererr = delerr/5.41E-11
```