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The American University in Cairo

School of Science and Engineering

MACRO-MODEL OF THROUGH SILICON VIAs (TSVs) Arrays

A Thesis Submitted to

Electronics Engineering Department

in partial fulfillment of the requirements for

the degree of Master of Arts/Science

By Kareem Ali Ahmed

Under the supervision of:

Prof.Yehea Ismail

Dr.Eslam Yahya

Dr.Alaa El Rouby

August/2012

Cairo, Egypt

`

The American University in Cairo

School of Science and Engineering (SSE)

MACRO-MODEL OF THROUGH SILICON VIAs (TSVs) ARRAYS

A Thesis Submitted by

Kareem Ali Ahmed

Submitted to Department of Electronics

August/2012

In partial fulfillment of the requirements for

The degree of Master of Science

has been approved by

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Date _____________________

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Thesis first Reader

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Date _____________________

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Thesis Second Reader

Affiliation:

Date _____________________

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Department Chair

Date _____________________

____

Dean of SSE

Date _____________________

DEDICATION

From Deep of My heart

To: My Father, My Mother, My Sister and My Grandmother

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First of all, I have to thank god for giving me the strength and guiding me in the right way to finish my master thesis, also I have to thank many people that always supported me in my life and during my master.

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ABSTRACT

OF THE THESIS OF

Kareem Ali Abd El-Twab Ahmed for Master of Science

Major: Electronics Engineering

The American University in Cairo

Title: Macro-Model of Through Silicon Vias (TSVs) Arrays

Supervisor: Prof. Yehea Ismail Co-Supervisor: Dr. Eslam Yahya, Dr.Alaa El Rouby

As continued scaling down of transistors becomes increasingly difficult due to physical and technical issues like the increase of leakage power and total power consumption, overall, 3D integration is now considered a viable solution to get a higher bandwidth and power efficiency. Use of Through-silicon-vias (TSVs), which connects stacked structures die-to-die, is expected to be one of the most important techniques enabling 3D integration.

As the number of through silicon Vias (TSVs) exists in the same chip is increasing, an algorithm to build a macro-model is needed to find inter-relationship between TSVs. There are different coupling parameters that exist between TSVs like: capacitive, inductive and resistive coupling. This work provides an algorithm to build a macro-model of an array of TSVs where only capacitive coupling is considered, as it is expected to be the dominating parameter.Using a simulation based technique, where characterization for bundles of TSVs were done and a scaling equation that can give the variationsoccur to capacitance value with scaling the physical dimensions of the TSV (pitch, radius, length and dielectric thickness (t_{ox})) is proposed. The considered ranges for the physical parameters are: radius (from 1um to 10um), t_{ox} (from 0.1um to 0.5 um), length (from 10um to 100um) and pitch (from 10um to 95um). Using theproposed algorithm, a macro model can be built in a negligible time, which provides lots of time saving compared to hours required by other tools such as EM simulators or device simulators. The average error range 3% to 6%and a maximum cumulative error of algorithm and usage of scaling equation is 18.2% that occurs at very few dimensions and in very few capacitances from the extracted capacitance values, for both self and coupling capacitance.

Table of Contents

Chapter 1: Introduction 10
1.1 Motivation 10
1.1.1 System on Board (SOB): 11
1.1.2 Multi-Chip Module (MCM): 11
1.1.3 System on Chip (SOC): 12
1.1.4 3D integration or System in Package (SIP): 12
1.2 Problem Definition 14
1.3 Problem Solution 16
1.4 Contribution 17
1.5 Thesis Organization 17
Chapter 2: Background and Literature Review 19
2.1 TSV Technologies 19
2.2 Single TSV Models: 20
2.2.1 Model of G.Katti et al [14] 20
2.2.2 Model of T.Bandyopapdhyay et al [13] 21
2.2.3 Joohee Kim et al. [15] 22
2.2.4 Khaled Salah et al. 24
2.3 Coupling between Two TSVs 25
2.3.1 Kihyun Yoon et al [21] 25
2.3.2 Ioannis Savidis et al. [22], [23] 25
2.4 Coupling between Bundle of TSVs 27
2.4.1 Dae Hyun Kim et al. [24] 27
2.4.2 Roshan Weeraskera. [26] 28
2.4.3 Biancun Xie et al. [29] 30
Chapter3: Algorithm 32
3.1 TSV distribution in a chip 32
3.2 Algorithm. 34
3.3 Window Structure 35

3.3.1 Window Size 37
3.3.2 Structures Count Reduction 38
3.3.3 Different 3x3 Structures 45
3.4 Double Counting 50
3.5 Macro-Modeling Techniques 52
Chapter 4: Dimension Scaling 60
4.1 Scaling equation 60
4.2 Characterization Scenarios 64
4.3 Equation Coefficients 68
4.3.1 Coefficients Usage 69
4.3.2 Coefficients Calculation 72
4.4 Characterization Results 73
4.4.1 3x3 Window Results 73
4.4.2 9x9 Structure Results 80
Chapter 5: Results and Algorithm Enhancements 87
5.1 Verification Tools and Techniques 87
5.2 Results 88
5.2.1 Simulation at Reference Dimensions 90
5.2.2 Algorithm Enhancement for Self-capacitance Error 92
5.2.3 Maximum Error Reduction 94
5.2.4 Simulation at Different Dimensions 95
5.3 Hybrid Algorithm 97
Chapter 6: Conclusion, Recommendations and Future Work 105
6.1 Conclusion and Recommendations 105
6.2 Future Work 107
6.2.1 Algorithm Enhancements 107
6.2.2 Other Perspective 108
Bibliography 110

Table of Figures

Figure 1- 1 1Moore's Law and More. [2] 10
Figure 1- 2 Historical evolution of the five system technologies over the past 50 years. [3] 11
Figure 1- 3 (a) System on Board, (b) Multi-Chip Module. [3] 11
Figure 1- 4 System on Chip. [4] 12
Figure 1- 5 3-D stacked chip package annual growth. [9] 13
Figure 1- 6 3D stacking of ICs with different technologies. [3] 14
Figure 1- 7 3D chip stacking categories. [3] 14
Figure 1- 8 1D Distribution of busses. Dotted lines mean that this capacitance can be neglected. 15
Figure 1- 9 Different TSV arrays structures. (a) Two unshielded TSVs, (b) Add two surrounding TSVs, (c) Add four surrounding TSVs. Capacitance calculated between blue TSVs. 16

Figure 2- 1 The typical TSV (a) 3D view (b) Top view (c) Side view. [33] 20
Figure 2- 2 (a) RLC TSV model. (b) RC TSV model. (c) C TSV model. [12] 21
Figure 2- 3 Equivalent circuit model. [13] 21
Figure 2- 4 a) Structure of a signal TSV and a ground TSV with bumps with the via-last process and their structural parameters, and (b) the proposed scalable scalable electrical model with labeled RLGC components. [14] 23
Figure 2- 5 The proposed lumped model for a TSV based on a single π structure. The model is composed of Ro, Lo, R1, L1, Cox, Cox, Csi, Cdep, Rsi and Rdep. [15] 24
Figure 2- 6 Equivalent circuit model of a coupled TSV. [17] 25
Figure 2- 7 Capacitance of two TSVs when (a) using a ground plane and (b) using a ground tap. [18] 26
Figure 2- 8 Self (a) and total (b) Capacitance of centric TSV in 3 × 3 bundle. [21] 29
Figure 2- 9 TSV bundle nearest neighbor coupling capacitances. [21] 29
Figure 2- 10 Coupling S-parameters between different TSV pairs. [22] 30
Figure 2- 11 The coupling (a) capacitance, (b) inductance and (c) resistance change with respect to distance for different TSV arrangements. [18] 31

Figure 3- 1 Array of TSVs (a) regular, (b) irregular. 33
Figure 3- 2 TSV structure density: a) dense (70TSVs), b) middle dense (53 TSVs), c) middle sparse (33TSVs), d) sparse (18 TSVs). 33
Figure 3-3 Algorithm Flow Chart. 36
Figure 3- 4 Sliding window of window size 3x3 applied on 4x4 structure, a) window on first TSV, b) window on second TSV, c) window on last TSV in the array. 37
Figure 3- 5 Sum of Structures Count for Different Array Sizes. 39
Figure 3- 6 Structures Count for Different Array Sizes and Selected Number of Empty TSVs. 39

Figure 3- 7 Structures Count Where a Centric TSV can not Exist and Structures Count Where Centric TSV Should Exist. 40
Figure 3- 8 TSV Sub-structure (a)4empty places in a 3x3 sub-structure.(b) Rotation of a to left by 90. (c) Rotation of b to left by 90. 41
Figure 3- 9 a) Capacitance values of centric TSV for Figure3-8a, b) Capacitance values of centric TSV for Figure3-8b, c) Capacitance values of centric TSV for Figure3-8c. Capacitance values obtained from Q3D extractor-quasi static EM simulator. 42
Figure 3- 10 a) Original Sub-structure, b) Mirror of a around x-axis, c) Rotation of mirrored sub-structure to left by 90°, d) Rotation of mirrored sub-structure to right by 90°. 42
Figure 3- 11a) Capacitance values of centric TSV for Figure3-10a, b) Capacitance values of centric TSV for Figure3-10b, c) Capacitance values of centric TSV for Figure3-810, d) Capacitance values of centric TSV for Figure3-10d. Capacitance values obtained from Q3D extractor-quasi static EM simulator...43
Figure 3- 12 (a) Flowchart of generating non-redundant window structures. (b) Flowchart of redundant structure extraction. 44
Figure 3- 13 Different Capacitance types: a) 1st inline, b) 2nd inline middle, c) 2nd inline peripheral, d) diagonal, e) 2nd diagonal, f) Asymmetric. 46
Figure 3- 14 Coupling capacitance value between TSV5 and TSV6 for inline coupling capacitance and between TSV5 and TSV3 for diagonal coupling capacitance. 50
Figure 3- 15 Two direct coupled TSVs showed in (a) with different surroundings as in (b), (c). ...51
Figure 3- 16 Chart gives different possibilities to build simulation based macro-model.............54
Figure 3- 17 Flowchart of implemented algorithm. 55
Figure 3- 18 Flowchart of creating the library. 56
Figure 3- 19 Flowchart of calculating capacitance in simulation based technique. 56

Figure4- 1a) Geometry of two wire transmission line, b) Geometry of two coupled TSVs. 62
Figure4- 2 Coupling capacitance variation with changing pitch. 62
Figure4- 3 Coupling capacitance variation with changing radius. 63
Figure4- 4 Coupling capacitance variation with changing tox. 63
Figure4- 5 Coupling capacitance variation with changing length. 63
Figure4- 6 Flowchart of building coefficients library. 71
Figure4- 7 Direct coupling capacitance between (TSV5 and TSV2) in a 3x3 full matrix window structure with varying length using Q3D and relation equation. 74
Figure4- 8Total capacitance of centric TSV in a 3x3 full matrix window structure with varying pitch using Q3D and relation equation. 75
Figure4- 9 Direct coupling capacitance between (TSV5 and TSV2) in a 3x3 full matrix window structure with varying radius using Q3D and relation equation...76
Figure4- 10 Direct coupling capacitance between (TSV5 and TSV2) in a 3x3 full matrix window structure with varying tox using Q3D and relation equation. 76

Figure4- 11 Total capacitance of centric TSV in a 3x3 full matrix window structure with varying both stsv and tox using Q3D and relation equation. 77
Figure4- 12 Diagonal coupling capacitance between (TSV5 and TSV1) in a 3x3 full matrix window structure with varying both stsv and rtsv using Q3D and relation equation...............................78
Figure4- 13 Total capacitance of centric TSV in a 3x3 full matrix window structure with varying both rtsv and tox using Q3D and relation equation..79
Figure4- 14 Total capacitance of centric TSV in a 3x3 full matrix window structure with varying stsv, rtsv and tox using Q3D and relation equation. 80
Figure4- 15 Test structure of size 9x9 contains 71 TSVs. 83
Figure4- 16 Compare of total capacitance of TSV 71 with varying pitch only obtained from both algorithm and Q3D simulations. 84
Figure4- 17 Compare of total capacitance of TSV 71 with varying both pitch and tox only obtained from both algorithm and Q3D simulations...84
Figure4- 18 Compare of total capacitance of TSV 71 with varying pitch, radius and tox only obtained from both algorithm and Q3D simulations...85

Figure5- 1 Histogram of all capacitance error in 9x9 test case structure at ref dimensions.........91
Figure5- 2 Histogram of total capacitances error of all TSVs in 9x9 test case structure..............93
Figure5- 3 Histogram of all capacitance error in 9x9 test case structure at reference dimensions, using enhanced self-capacitance calculation in the algorithm..94
Figure5- 4 Histogram of all capacitance error in 9x9 test case structure at reference dimensions using average double counting...96
Figure5- 5 Histogram of total capacitances error of all TSVs in 9x9 test case structure using average double counting...96
Figure5- 6 Histogram of all capacitance error in 9x9 test case structure at stsv=85um, rtsv=8.5um, tox= 0.3um, ltsv=50um using minimum double counting. 98
Figure5- 7 Histogram of all capacitance error in 9x9 test case structure at stsv=85um, rtsv=8.5um, tox= 0.3um, ltsv=50um using average double counting...98
Figure5- 8 Histogram of all capacitance error in 9x9 test case structure at stsv=25um, rtsv=6.5um, tox= 0.5um, ltsv=50um using average double counting...99
Figure5- 9 (a) Scanning line algorithm, (b) Scanning line at eight angles.................................101
Figure5- 10 Histogram of all capacitance error in 9x9 test case structure at reference dimensions using hybrid algorithm with average double counting technique and enhancements in calculating self-capacitance value...102
Figure5- 11 Histogram of total capacitance error in 9x9 test case structure at reference dimensions using hybrid algorithm with average double counting technique and enhancements in calculating self-capacitance value...103

Figure6- 1 Dielectric constant relaxation versus frequency. [32] 109
Figure6- 2 Coupling capacitance variation with frequency. 109

Chapter 1

Introduction

1.1 Motivation

Gordon Moore proposed in 1965 that; number of transistors on a single chip doubles every 18 to 24 months; this became known as Moore's Law. Moore's law is working in the right way with scaling down transistor sizes. It results in an increase in functionality and computational capability of electronic devices with the evolution of technology. However recently, lots of bottlenecks have appeared while continuing scaling down the transistor size to sub microns technologies. One of those bottlenecks is the difficulty and costly way in continuing lithographic scaling. Lithographic scaling at certain points will be impractical from the economic point of view as it is going to be so expensive and will result in very expensive ICs. Another bottleneck is the massive increase in the power dissipation which in return results in stopping the scaling of clock frequency. There is also a massive increase in dynamic power dissipation due to the fact that interconnects increases exponentially with scaling[1]. As a result, there is a new trend nowadays, known as "More than Moore" [2] depicted in Figure1-1. The approach of "More than Moore" focuses on system integration rather than transistor density; While Moore's law focuses on miniaturizing the transistor which can be just 10% of the system and leaving the other 90% which are bulky discrete passive components such as resistors, capacitors, inductors, antennas, filters, switches and interconnects. So system level integration requires the miniaturization at package level as well as chip level. According to that, new system level integration techniques appeared with time as depicted in Figure1-2 and is discussed in the following:

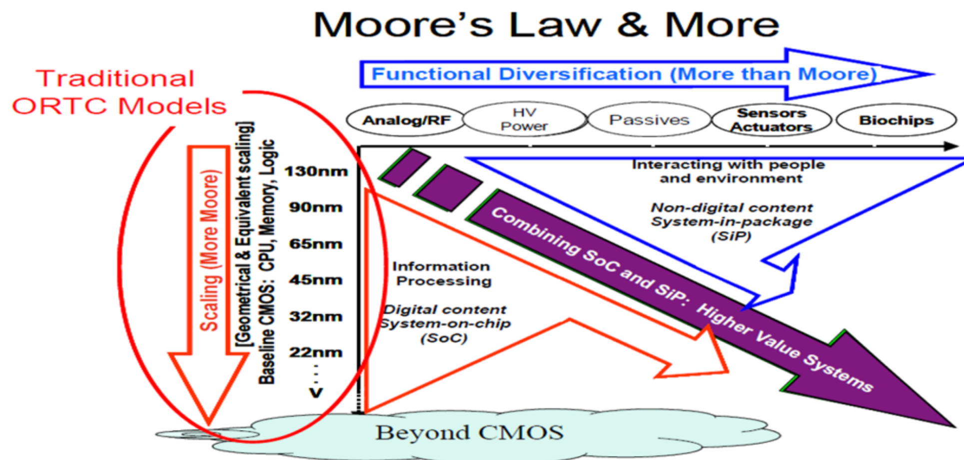


Figure 1- 11Moore's Law and More. [2]

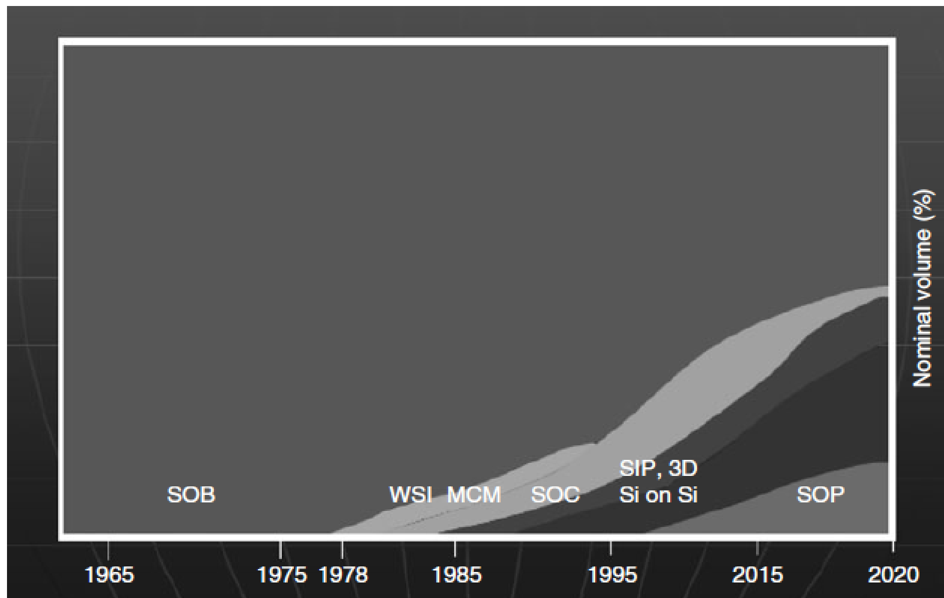


Figure 1-2Historical evolution of the five system technologies over the past 50 years. [3]

1.1.1 System on Board (SOB):

SOB[3] is the assembly of bulky IC packages, discrete components, connectors, cables, batteries, I/Os, massive thermal structures, and printed wiring boards all within the same board and it is shown in Figure1-3a.

1.1.2 Multi-Chip Module (MCM):

In MCM [3] different ICs are integrated in the same package in a 2D manner and inter-connection are done between them using long wire and routing channels. Long wires are considered as the main source of performance degradation in that system level integration technique.An example of MCM is shown in Figure1-3b.

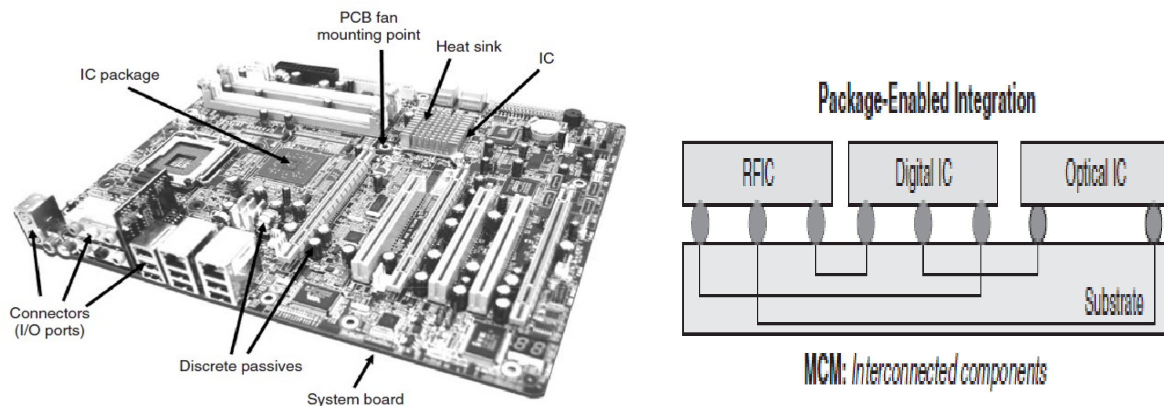


Figure 1-3(a) System on Board, (b) Multi-Chip Module. [3]

1.1.3 System on Chip (SOC):

In SoC [4] all of the functions are implemented on a single die as illustrated in Figure1-4. Different people have different definitions for what SoC comprises. A digital logic designer might say that a SoC contains one or more processor cores, memory blocks, peripheral functions, and hardware accelerators, all created on the same piece of silicon. By comparison, someone like a system architect looking at things from a slightly higher vantage point might say that SoC is a single device that combines digital logic, memory, and analog/RF functions all on the same die.

1.1.4 3D integration or System in Package (SIP):

3D integration [5] or as some calls it System-in-Package (SiP) [3] started to gain traction around the year 2000. 3D Integration may be considered to be the modern shape of a multi-chip module (MCM). The idea behind a SiP is that multiple bare dice and/or chip-scale package (CSP) devices are mounted on a common substrate. Substrate is used to connect all chips together and that is mainly done in a 3D manner. The substrate and its components are then placed in (or built into) a single package. This approach has several advantages over a System-on-Chip (SoC); including the fact that one can include analog, digital, and radio frequency (RF) dice in the same package. Each die can be implemented usingmost appropriate technology process. Also, designers can employ a number of off-the-shelf dice coupled, perhaps, with a limited number of relatively small, internally-developed components. Furthermore, when it comes to re-spinning the device in the future to evolve existing functionality or add new features, it is the case that you need to modify only a subset of the dice.

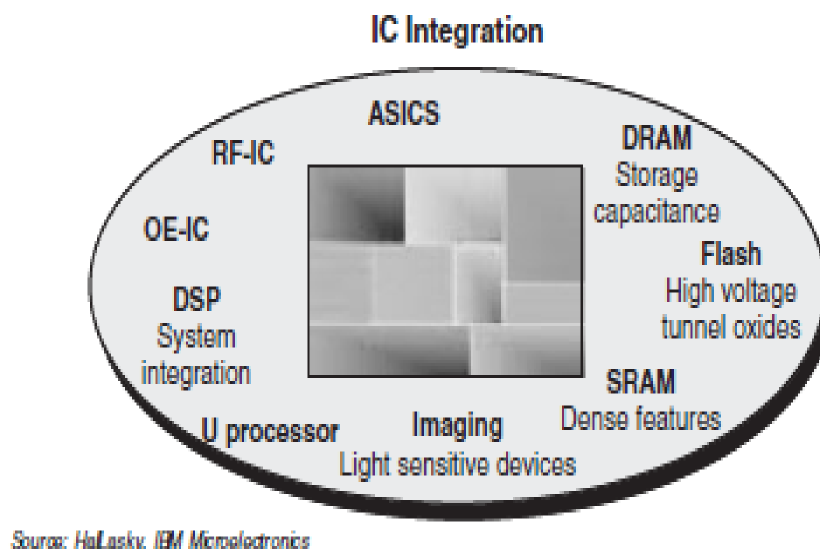


Figure 1-4System on Chip. [4]

3D integration technology provides a better performance in many design criteria. As3D integration is compared with the conventional 2D approaches, it can be noticed that 3D-ICs target interconnect delay problems, have less interconnect length, and enable integration of heterogeneous technologies (analog ICs, digital ICs, MEMS, etc). Because of the higher performance that can be obtained from shorter interconnect length using 3D technologies its world-wide market doubled from 2065 million units in 2007 to be 5227 million units in 2011 as shown in Figure 1-5. Several 3D interconnection techniques [6] are already well known in the industry nowadays like wire bonding, metal bumps, flip chip [7] and TSV [8] shown in Figure1-6. 3D interconnection techniques can be in general classified into two categories: Non-TSV chip stacking and TSV chip stacking as shown in the chart in Figure1-7.

TSV is expected to have a higher performance due to the reduction in wire interconnection required especially when compared with the conventional wire bonding technique. TSVs also have lower cost especially when compared with the expensive flip chip technique. Also, it results in less I/O power consumption which in return makes it an excellent choice to replace the conventional I/O structures, such as flip chip, metal bumps and wire bonding especially for low power applications.

However, TSV technology needs lots of studies and research in order to be ready to have the lead in all of the industrial 3D integration. An accurate modeling for a single TSV and for structures of multiple of TSVs is required in order to have a fully automated process to design a 3D IC. Also other issues have to be studied for the TSV like thermal management and the heat effect of the whole 3D structure, so the required model should take the temperature effect into consideration as well.

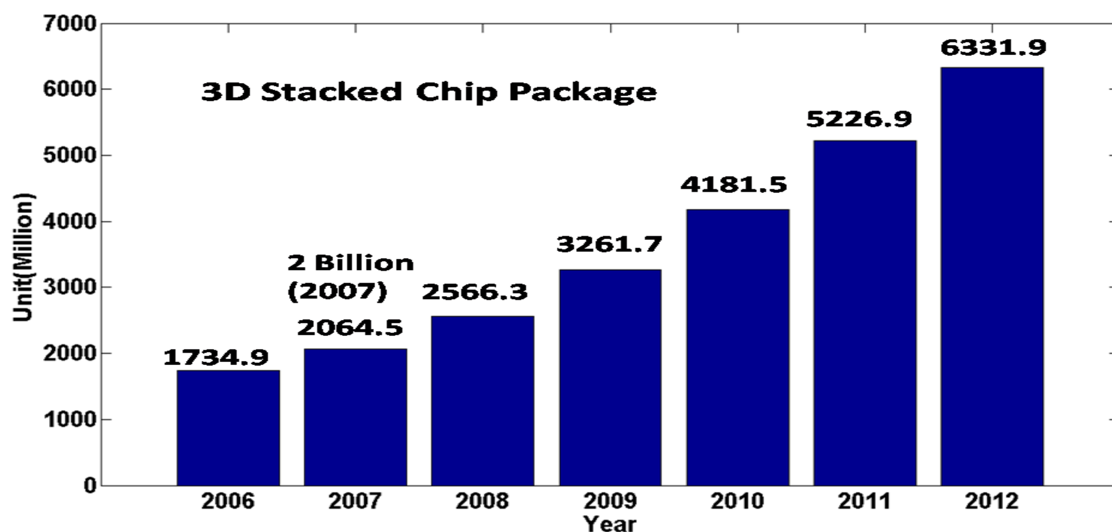


Figure 1-5 3D stacked chip package annual growth. [9]

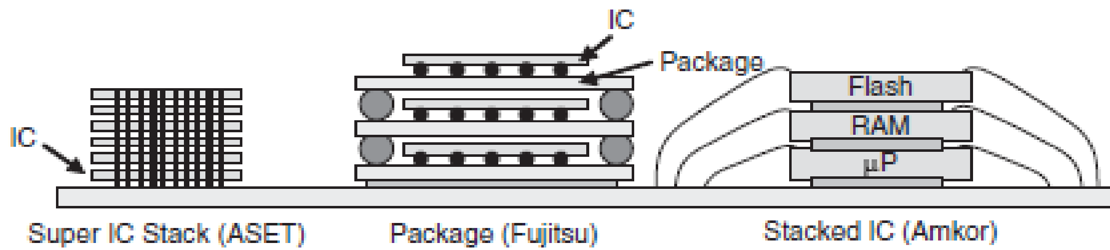


Figure 1-63D stacking of ICs with different technologies. [3]

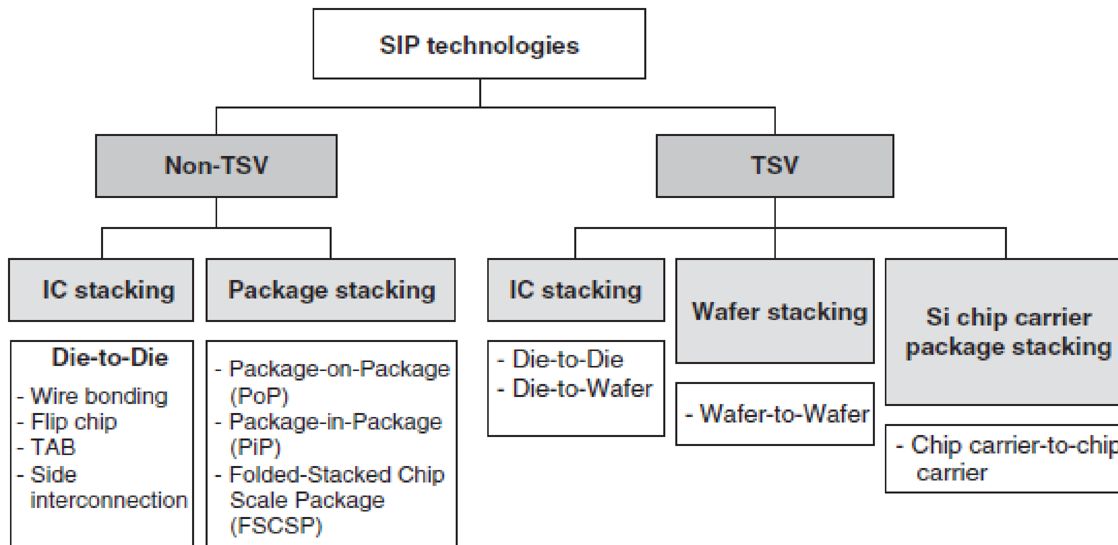


Figure 1-73D chip stacking categories. [3]

1.2 Problem Definition

With the evolution of technology, more devices can be integrated in the same area (IC), which means more interconnects are needed. Using TSVs as the interconnect technique means that more TSVs are required in the same chip. A $100x100$ array size of TSVs can be reached in today's technology. These TSVs affect each other as well as the surrounding devices. There are different coupling parameters that exist between different components in the system like: capacitive, inductive and resistive coupling. In order to have a fully automated design process and a CAD tool that can help the designer in the design flow of a 3D IC, those parameters are needed. Those parameters can be obtained by electromagnetic wave simulators like Ansoft-Q3d extractor [10] (Quasi static wave simulator) or device simulators like Synopsys-Sentaurus [11]. Using those tools can take hours, and sometimes days, to get coupling and self-parameters of the TSVs, especially for large structures of TSV bundles. There is coupling between all the TSVs in the array, which means large number of components is needed to build an equivalent model. Due to different physical phenomenon, some values of those coupling parameters are very small

and can be neglected. There are different works in the literature which model single TSV[12], [13], [14], [15], [16] or, at most, the mutual effect of few TSVs on each other[17], [18], [19], [20], [21],[22]. Practically, TSVs are found in large arrays and these models cannot solve the interrelationship between them.

Solving TSV arrays is much more complex than Solving traditional busses. Busses are considered as a 1-D distribution where one bus can totally shield capacitive coupling between two other TSVs as shown in Figure1-8, as they are distributed in the same row or column. Also in busses it is a matter of peer-to-peer capacitance the surrounding busses wouldn't affect on coupling capacitance values. While TSV arrays are considered as 2-D distribution as shown in Figure1-9 and may be a 3-D distribution in case of stacking of more than two chips. As TSVs exist in a 2D distribution, so there would be coupling with different surrounding TSVs located in all direction. Therefore, a larger capacitance matrix is expected in case of TSVs and more parameters should be considered like number of surrounding TSVs and position of those surroundings. It is no more a peer-to-peer capacitance as more parameters should be considered. The effect of existence of surrounding TSVs can be shown by noticing different structures exist in Figure1-9, where Figure 1-9a is a structure that contains only two TSVs, then in Figure1-9b, c increasing number of surrounding TSVs to 2 and 4 respectively. As can be noticed in Table.I, capacitance between the blue TSVs decreases with the increase of the surrounding TSVs and that decrease in capacitance value occurs with varying the structure can't be neglected as it results in a relatively large error.

As shown in Figure 1-9, the TSVs can be distributed in a random spatial distribution. The distribution, array size, and the TSVs physical dimensions are defined by the chip designers. The objective is to build an algorithm which is able to solve *NxM* TSV array in-which the TSVs are randomly distributed.

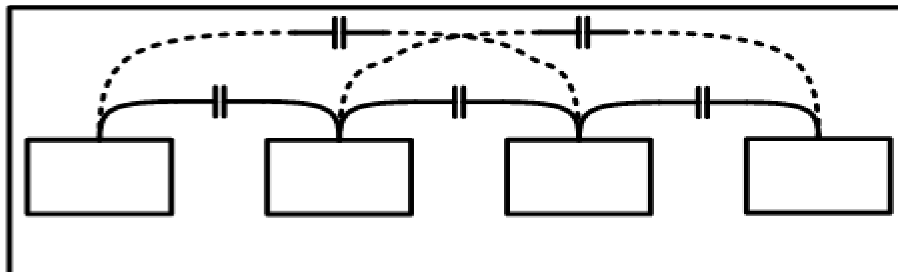


Figure 1-8 1D distribution of busses. Dotted lines mean that this capacitance can be neglected.

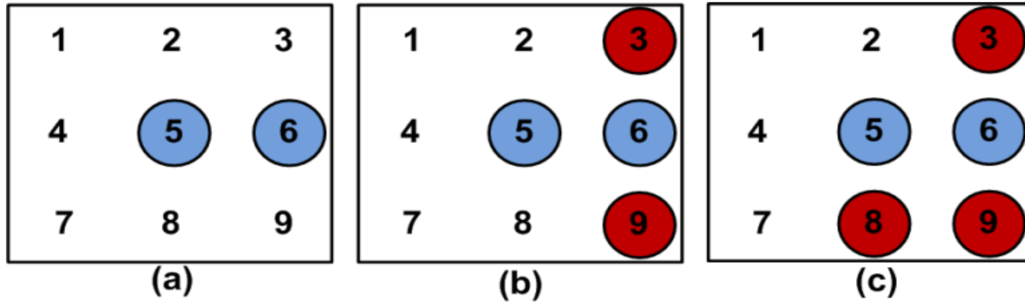


Figure 1- 9 Different TSV arrays structures. (a) Two unshielded TSVs, (b) Add two surrounding TSVs, (c) Add four surrounding TSVs. Capacitance calculated between blue TSVs.

Table 1 Capacitance value between blue TSVs in different structures in Figure1-9.

Structure	**Figure1-9a**	**Figure1-9b**	**Figure1-9c**
Coupling capacitance value(fF)	6.6284	3.9238	2.9928

1.3 Proposed Solution

To solve the previously stated problems, an algorithm is needed to build a macro-model that represents the coupling effects between different TSVs, and self-parameters of each TSV in the chip. The model can be obtained from a model based technique or a simulation based technique, more details about those different techniques are given in Chapter 3. A "**Macro model**" is a macro as it focuses on larger scale, not on a single TSV or single device but it consider the whole components in the system and find the interrelationship between them. Also it is a macro as it executes certain instructions in order to solve the given array of TSVs and it is a model as these instructions are fixed for any given distribution or dimensions of TSV arrays.

The proposed algorithm is a simulation based algorithm which is able to solve *NxM* TSV arrays in-which the TSVs are randomly distributed. The algorithm is based on Divide and Conquer technique which is dividing the main problem (the *NxM* TSV array) into smaller sub-problems (we call it "substructures"). The sub-problem is *3x*3 substructures which are simulated by using EM simulators and all the required capacitances are extracted and stored in a library. Since the 3x3 structure can have many shapes, depending on which TSV is exist and which one is absent, all the possible structures are simulated and their results are stored in the library. The proposed algorithm then composes the solutions of the different sub-problems (3*x*3 substructures) to obtain the solution of the main problem (*NxM* TSV array). This gives an algorithm which is able to solve any NxM TSV array in-which the TSVs are randomly placed. However, the library valuesare simulated at specific physical dimensions (TSV length, diameter, oxide thickness, etc) we call them reference dimensions. "**Reference Dimensions**" are TSV physical dimensions at which different structures are simulated to get coupling and self-parameters to be used inside the library of the TSVs. In case the input structure is

designed on different physical dimensions, scaling equations are developed which are able to calculate the new capacitances at the new dimensions.

1.4 Contribution

Coupling effects between TSVs and self-parameters of a TSV are the focus of this work. So inter-relationship between devices and TSVs is out of scope of the thesis. There are different coupling parameters between TSVs like: capacitive, inductive and resistive coupling. Only capacitive coupling is considered in this work as it is expected to be the most effective in the performance, that approximation is accepted in lower frequency but for high frequencies inductance is expected to have large effect and should be conisdered. Both simulation based and model based methodologies that can be used to build the macro-model were discussed; only the simulation based technique was implemented in this work. There are different characterization techniques which can be used in the simulation based methodology, these techniques are defined and discussed. Due to time and man power limits, only the most conservative and accurate characterization technique is implemented, details are discussed in Chapter 4.

Regarding the TSV structures, there are different types where the TSVs can be distributed in a dense way (i.e. dense class), in a sparse way (i.e. sparse class), or in the middle between sparse and dense (i.e. middle dense or middle sparse class). This work focuses on dealing with dense class, as it is expected to have lots of dense clusters of TSVs in nowadays technology. The proposed algorithm gives an average error in the range of 3% to 6% in a negligible time. The algorithm is built using c-programming language. Optimization to get coefficients for the characterization is done using Mat-lab [23]. The golden reference for this work is the capacitance values obtained from quasi static EM wave solver Q3D Extractor [10].

1.5 Thesis Organization

Chapter 2: illustrates different TSV technologies and presents the considered technology during this work. Then model of single TSV as it can be used in the simulation based approach is presented. After that, the chapter shows previous work that consider coupling between just two TSVs and works that consider coupling in case of bundle of TSVs. Finally, an algorithm that is used to build a macro-model using model based technique is shown.

Chapter 3: illustrates the algorithm of the scanning window. Then discusses appropriate window size choice, the double counting issue and how it can be solved. After that, the chapter shows how to extract redundant structures, which makes large reduction in number of possible structures of the chosen window. Finally, different techniques that can be used to build a macro-model are discussed.

Chapter 4: presents the proposed scaling equations. Scaling equations are used to capture variations occur in coupling and self-capacitances when the dimensions changes from the reference dimensions in the simulation based technique. Also, different characterization techniques are presented and the results of the implemented technique in this work are discussed.

Chapter 5: illustrates different verification flows and tools that can be used to verify the results. Then shows the results obtained from the proposed algorithm for a dense test structure. Finally, it discusses further enhancements for the algorithm depending on the obtained results to get better accuracy.

Chapter6: illustrates conclusion obtained from the results and some recommendations/guidelines are given. Finally this chapter presents our view for the future work to improve the algorithm

.

Chapter 2

Background and Literature Review

In literature, there is very little work that provides a complete algorithm to build a macro-model for an array of TSVs. Previous work focuses on building a lumped model of a single TSV or proposing coupling models between two TSVs. Few works proposed models that consider the existence of more than two TSVs and the shielding effects resulted between each other, which in return affects the coupling parameters between those TSVs as discussed in Chapter 3.

In this chapter, different models of a single TSV that exist in literature are reviewed. Some works in literature that discuss the coupling between TSVs are reviewed. Reason for reviewing models of single TSV and coupling model between TSVs is that it can help in building a model based macro-model as explained in later chapters. Then some works in literature that focus on coupling in bundle of TSVs are discussed. Immaturity of those models led us to focus on the other trend which is simulation based; the difference between model based and simulation based techniques are discussed in chapter 4.

2.1 TSV Technologies

There are different technologies for the TSV which have been compared in many publications as in [13]; the TSV shape can be cylindrical or square. Metal used to build the TSV can be copper or tungsten or other metal types as presented in [3]. Three famous structures are:

1- Through silicon via with thin (≤ 1um) inorganic dielectric liner.
2- Through silicon via with thick (≥ 2um) organic liner.
3- Through package via in glass substrate.

During this work, the most well-known technology of the TSV is considered. This TSV technology is a uniform circular cylinder of a conducting material (copper) surrounded by an insulator (silicon dioxide) which is intended to prevent leakage and resistive coupling through the substrate (silicon). The substrate has its body contacts connected to a DC voltage. This structure is shown in Figure 2-1. The characteristics of a TSV are dependent on its geometrical parameters such as TSV diameter, height, oxide layer thickness, and electrical parameters such as metal conductivity, oxide permittivity, and silicon substrate resistivity.

2.2 Single TSV Models:

Due to the critical role that 3D integration ICs are playing nowadays, it is required to have a fully automated process to design a 3D IC. In order to achieve that, an electrical model representing the behavior of the TSV is required. This model should take into consideration the semiconductor MOS effects. An accurate model for the TSV is requiredwith suitable closed form equations representing the electrical components inthe model (resistance, capacitance and inductance). This model can help in building up a Macro Model for TSVs using the model based technique as discussed in chapter 3. Also, it helps in predicting the suitable dimensions for the TSV with the rapid scaling down in CMOS technology.

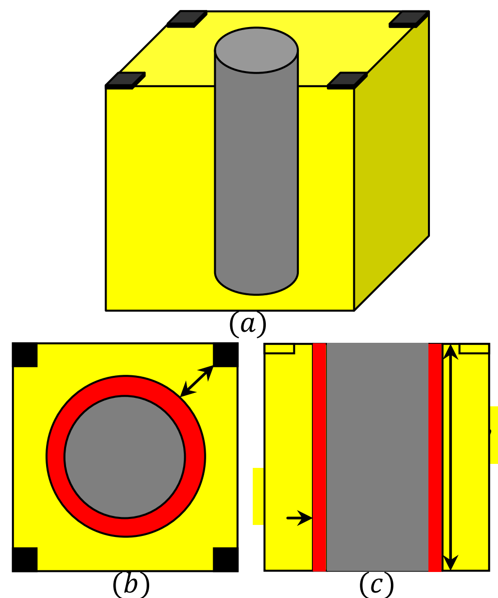


Figure 2-1The typical TSV (a) 3D view (b) Top view (c) Side view. [33]

In this section different electrical models for a single TSV exist in literature are discussed giving up some of their closed form equations.

2.2.1 Model of G.Katti et al [12]

G.Katti et al at IMEC, Leuven [12]proposed a model for RLC parameters of the TSV. In that model, TSV resistance, inductance and capacitance are given as a function of physical parameters and material characteristics. The model is validated using numerical simulators like Raphael and Sdevice. Raphael and Sdevice are considered as device simulators. In addition, their results are compared with actual experimental measurements of a fabricated TSV which in return added a lot to their work.

A lumped RLC model that is proposed by IMEC is shown in Figure2-2a.Rtsv and Ltsv cause the voltage drop between the two metals at the top and the bottom. Ctsv is connected between the TSV and ground (which is bulk of the silicon substrate). It is deduced that L_{tsv} is predominant only for clock frequencies with rise and fall time above 3GHZ. This happens when $wL_{tsv} \geq R_{tsv}$, so the model is approximated to be as in Figure2-

2b. The model is analyzed in a circuit composed of two inverters at the input and output of the TSV, afterwards Elmore delay is calculated. Using 0.25μm technology, it is found that Rtsv has minimal impact on delay as it is always added to the driving resistance of inverter and the BEOL resistances so it can be neglected and removed from the model. As a result, the model was reduced to be as shown in Figure 2-2c.

2.2.2 Model of T.Bandyopapdhyay et al [13]

T.Bandyopadhyayet al at Georgia Institute of technology [13] proposed an analytical model shown in Figure2-3. TheMetal oxide semi-conductor (MOS) effect of the TSV is considered in the model. C_{ox} represents oxidecapacitance; voltage dependent depletion capacitance is represented by C_{dep}. R_{via} and L_{via} are the resistance andthe inductance of the TSV respectively. 3D full-wave electromagnetic (EM) simulator (CST Microwave studio) is used to compare between different technologies of TSV using the S-parameter which represents the electrical signal loss. Two TSVs were compared one with thin liner oxide and another one with a thick liner oxide. Results of comparison show thatthe thick liner oxide has lower loss as Si has small resistivity. So in thin structure more electric field moves in Si while in thick structure less electric field moves in it. That explains why the structure with thicker oxide has lower loss.

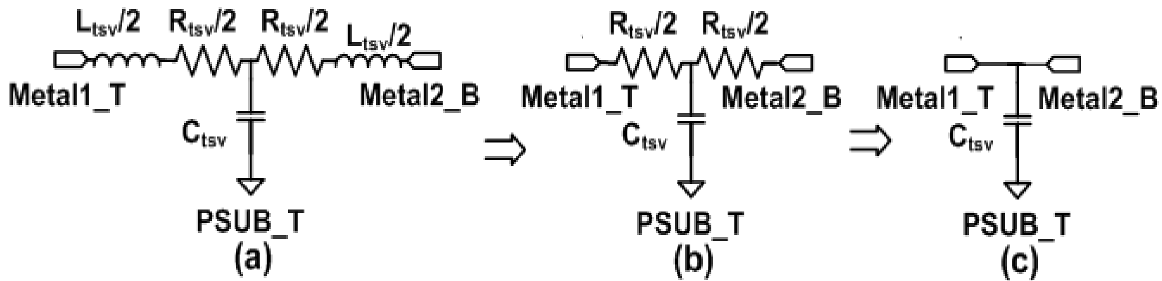


Figure 2- 2(a) RLC TSV model. (b) RC TSV model. (c) C TSV model. [12]

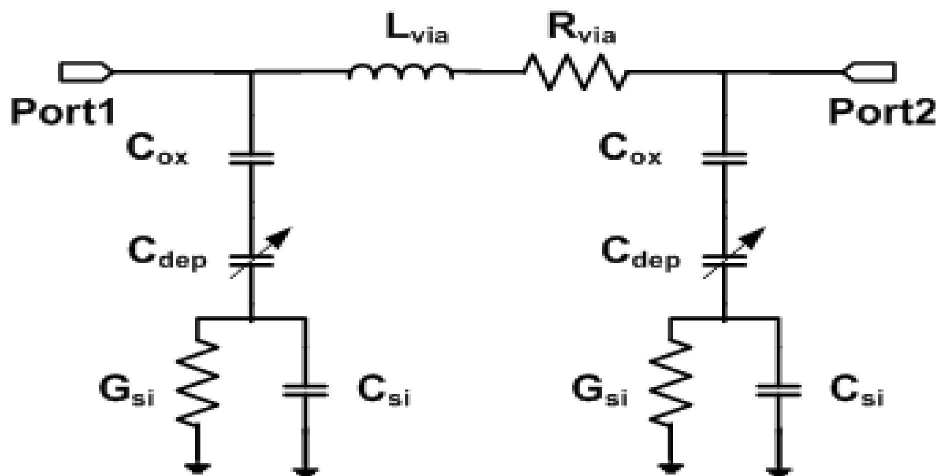


Figure 2- 3Equivalent circuit model. [13]

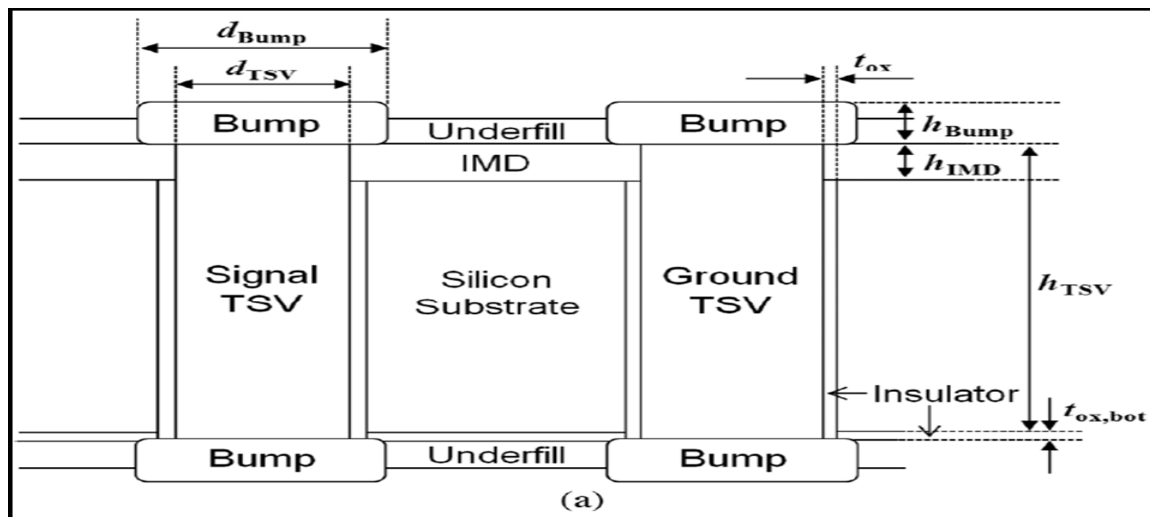
In this work lots of parametric studies on TSV parameters are done to find their effects on TSV capacitance.This is because the capacitance is the key in the TSV total delay.The considered parameters are: TSV diameter, Dielectric liner thickness, Dielectric liner material, Si resistivity, Bias voltage and TSV filling material. Then that study is used to give design advices for both a signal and power TSV. A signal TSV requires small capacitance while a power TSV requires large capacitance. So it is deduced that the required structure for the signal TSV is with smaller TSV diameter, thicker liner thickness to reduce oxide capacitance, a low dielectric constant and a high resistivity silicon substrate in order to reduce the depletion capacitance. On the contrary, the opposite of all the previous can be used for a power TSV as a larger capacitance is required.

2.2.3 Joohee Kim et al. [14]

Their considered technology for modeling the TSV is shown in Figure 2-4a. Both bump and redistribution layer (RDL) is considered in their model. Bump provides a joint between stacked chips. RDL provides a horizontal interconnection to redistribute signals between heterogeneous dies. When designing I/O channel with TSVs in 3-D IC, bump and RDL are essential components that should be considered with the TSV. Therefore, modeling and analysis of a TSV with the bump and RDL is important for advanced 3-D IC design. A figure of the proposed model is shown in Figure2-4b.

Some perspectives that are considered in their model are: Insulator capacitance, which results because of the existence of dielectric between conductors (metal TSV) and the semiconductor (silicon). Insulator capacitance is modeled using cylindrical formula of capacitances. Capacitance between bump and silicon (C_{Bump}), results from the excessive part of the bump that comes over the silicon. C_{Bump} is between bump and silicon where both bump and TSV have the same potential. So both the insulator capacitance (between TSV and silicon) and bump capacitance are added. Capacitance can be calculated using general capacitance law ($C= \varepsilon.A /d$). Capacitance of under-fill ($C_{underfill}$) formed between the two bumps is also considered in the model. Under-fill is a material used to separate between the stacked chips. Capacitance of inter-metal dielectric (IMD- silicon dioxide) formed between the TSVs. As bump and TSV have same potential, so both IMD capacitance and under-fill capacitance are parallel and added together. Both $C_{Underfill}$ and C_{IMD} close form equations obtained from the model of parallel wires capacitances [24]. Since silicon is a semiconductor, there is capacitance (C_{si-sub}) and conductance (G_{si-sub}) between the signal and ground TSVs. Capacitance of silicon substrate C_{si-sub} is modeled by applying the parallel-wires capacitance model[24]. In most circuit designs, dielectric losses can be ignored since the conductor losses are dominating. However, as frequencies increase, it is important to consider the dielectric losses which vary with frequency. So the loss effect of semiconductor can be represented by conductance G_{sub} which is

obtained from the capacitance using the equation that relates both capacitance and conductance [25]. Both the resistance of Bump and TSV are considered and modeled with structural parameters. Both skin effect and proximity effect are considered in the equations. For higher frequencies, the inductances of both bump and TSV become dominant over resistance, so it is also considered. Closed form equations of inductances are obtained from the loop inductance model between two parallel conducting wires. One weakness in that model is that it didn't consider the semiconductor MOS effect. Therefore, the depletion region created with voltage variation is not considered in that model.



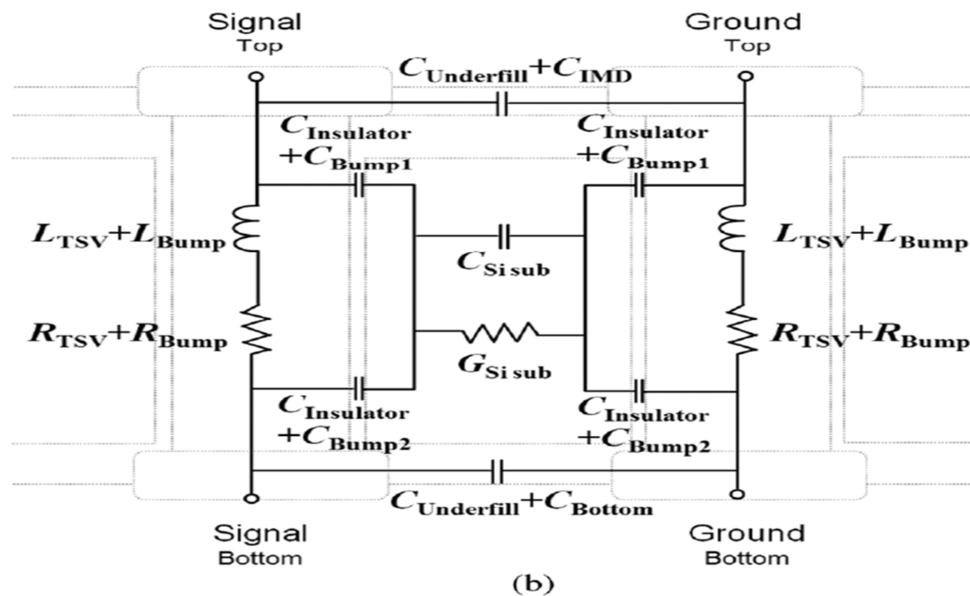


Figure 2-4a) Structure of a signal TSV and a ground TSV with bumps with the via-last process and their structural parameters, and (b) the proposed scalable electrical model with labeled RLGC components. [14]

2.2.4 Khaled Salah et al.

The objective of K. Salah et al [15], [16]was to develop a complete model that captures the nonlinear capacitance effects that results from the depletion region (MOS effect) beside the ohmic loss of the TSV conductor and oxide capacitance. This work also includes the body contact effect on the TSV behavior. The proposed lumped element model for the TSV is based on underlying physics. Their proposed model is fit to complete frequency dependent empirical data. These data obtained from an electro-magnetic wave (EM) solver over a wide range of TSV physical and technological parameters using dimensional analysis method [26].

The lumped RLC model for the TSV represents the TSV's electrical performance in standard simulators; the model target capturing the following TSV behavior/physics:

1. Conductor ohmic losses.
2. Capacitance across the oxide.
3. Capacitance and resistance across the substrate.

The model was derived based on the well-known single π structure and it is shown in Figure 2-5.

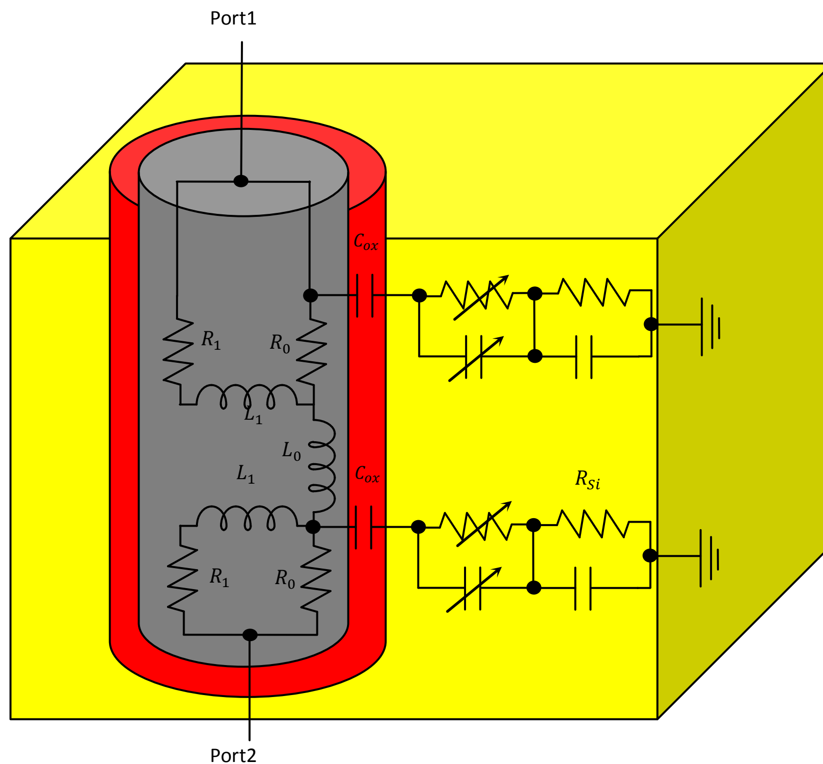


Figure 2-5Proposed lumped model for a TSV based on a single π structure. The model is composed of Ro, Lo, R1, L1, Cox, Cox, Csi, Cdep, Rsi and Rdep. [15]

2.3 Coupling between Two TSVs

In this section different models in literature which consider coupling between two TSVs are discussed. These models don't considerthe existence of other surroundings, neither TSVs nor device or even body contacts which affect on the coupling parameters values.

2.3.1 Kihyun Yoon et al [17]

This work presents a lumped element model for coupled TSVs, metal interconnects, redistribution layer (RDL) and the combination of the 3 kinds of interconnects in silicon interposer with a closed form expressions for the model parameters. The proposed lumped model is verified with s-parameters measurements results, which showthe strength of the proposed model. However, this work didn't consider the shielding effect of TSVs on each other. The lumped model for two coupled TSVs is shown in Figure2-6.

It is mentioned in that work that mutual inductance has very small effect on coupling as mainly the TSV interconnects are short so has small inductive coupling values. Capacitive coupling is the dominant parameter between coupled TSVs that clarifies the reason of neglecting inductance coupling in our work and just consider capacitive coupling.

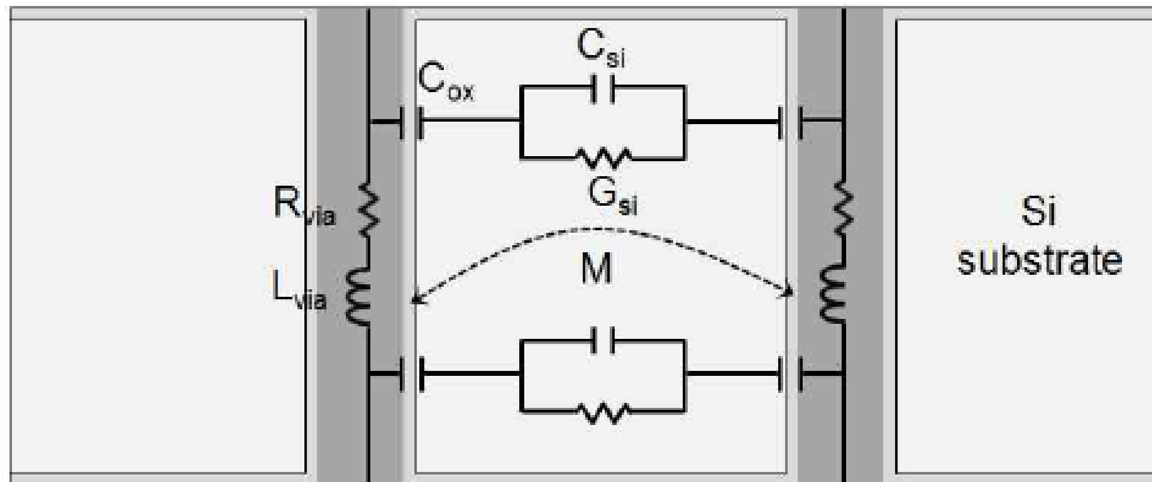


Figure 2- 6Equivalent circuit model of a coupled TSV. [17]

2.3.2 IoannisSavidis et al.[18], [19]

In[18]characterization of a single TSV is presented where the variation of self-capacitance, inductance and resistance values of the TSV with varying its physical parameters (size, length and dielectric thickness) is presented. It is shown that the electrical characteristics for TSV depend on the ground type, whether it is a ground plane in the back of the substrate or a ground tap. The work shows that capacitance to ground tap is much lower than the capacitance to ground plane. As illustrated in this work, it can be concluded that the electrical field lines generated from a TSV can't be neglected.

TSV to TSV interaction is also illustrated in this work, but no closed form expressions for coupling parameters are given. Only variation of the coupling capacitance with spacing between the two TSVs is discussed. The effect of using a ground plane or ground tap on the capacitance values (both self and total) is presented. As shown in Figure2-7, total capacitance value resulted from placing a ground plane is double total capacitance in case of using a ground tap. That is because of the larger capacitance to ground value in case of ground plane that add a lot to the total capacitance. While the ground plane halves the coupling capacitance between two TSVs as compared to ground tap, because the ground plane absorb more field lines than ground tap do. That result in less electric field reach the other TSV which means lower coupling capacitance in case of ground plane.

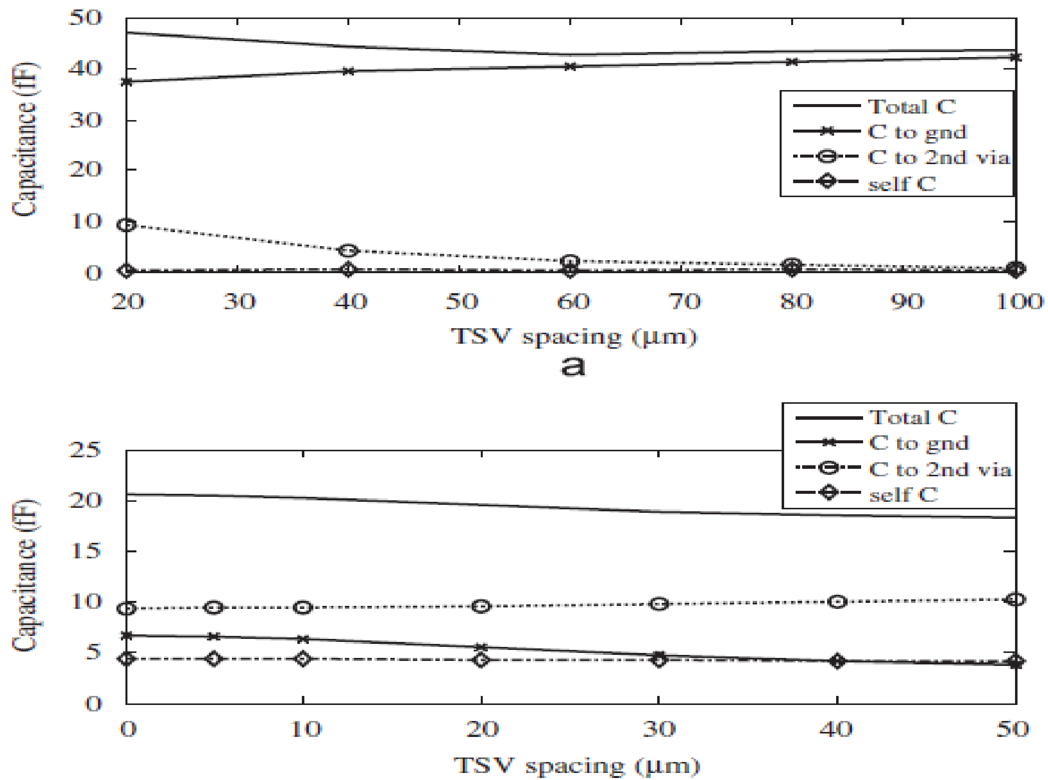


Figure 2- 7Capacitance of two TSVs when (a) using a ground plane and (b) using a ground tap. [18]

Savidis and G. Friedman in [19] proposed a closed form expressions for capacitance, resistance and inductance of single TSV over a ground plane, and capacitance coupling in equation (1). Inductive coupling between two TSVs over a ground plane is proposed. Resistive coupling which represents real part of coupling impedance is not mentioned in this work. In self-capacitance equation, formation of depletion region in bulk substrate surrounding the TSV is considered. The main idea of the built closed form expressions is to add a fitting parameter to adjust the coupling

capacitance for a specific physical factor. Where there is a term ($\boldsymbol{\alpha}$) that considers the non-linearity of the coupling capacitance with the aspect ratio (length/diameter (L/D)). Another term ($\boldsymbol{\beta}$) captures effect of distance between TSV and ground plane (S_{gnd}). Another term ($\boldsymbol{\gamma}$) consider non-linearity of coupling capacitance with the distance between two TSVs (S).

$$\boldsymbol{Cc = 0.4\alpha\beta\gamma * \frac{\varepsilon_{si}}{S}\pi DL} \tag{1}$$

2.4 Coupling between Bundle of TSVs

In this section, different models in literature that consider coupling between bundles of TSVs in an array are discussed. An algorithm to calculate coupling capacitance between certain TSV and surrounding TSVs that exists in literature is presented, discussing its points of weaknesses and strengths.

2.4.1 Dae Hyun Kim et al.[20]

In [20] an algorithm which is used to calculate coupling capacitance between certain TSV and surrounding TSVs is presented. The algorithm proposed in this work considers only coupling capacitance between TSVs similar to the focus of our work.But it neglects all the self-parameters of TSVs even self-capacitance; however it considers the coupling not only between TSVs and each other but also between TSVs and wires used in interconnection in the same chip.

Their proposed algorithmis a model based algorithm, where a set of equations are used to represent different parameters in the model. Usage of equations make it more flexible and with less overhead. The algorithm main idea is like a scanning line that finds all the surrounding TSVs with a certain angle, then starts to exclude the TSVs that are totally shielded or at a distance exceeds certain predetermined limit (DMAX). TSVs at distance (DMAX) are considered very far and results in a very small coupling capacitance that can be neglected. That distance depends on the used technology, so the algorithm requires a calculation of an empirical value called DMAX which vary with the used technology. Due to the dependence on empirical calculated parameters DMAX that vary with different technologies, the flexibility of the model is reduced. The equations proposed in their work don't consider the shielding effect that results from more than one TSV in the neighborhood of the TSV of interest. Neglecting shielding effect of surroundings may result in a large error in case of dense structure. This point isn't covered in their work, since only sparse structure of TSVs is considered and their test cases contained only 8 or 9 TSVs. That means their work suites more sparse structures. While in our work the focus is on dense structures that contain lots of TSVs close to each other, also taking into consideration the shielding effect results from surrounding TSVs on coupling capacitance values. Their model is verified against a device simulator

(Synopsys Raphael [27]) resulted in 6.03% error for regular structure, which is a 3x3 array of TSVs, and the capacitance is calculated for the centric TSV at different dimensions. While an average error varies between 5.06%-8.24% for random TSV structures with maximum error of 18.91% after trying 20 random generated TSV arrays.

A square shaped TSV technology is used in their work, which made the modeling of the electrical circuit parameters easier; while in our work a cylindrical shaped TSV technology is used, which is more complex in modeling. Cylindrical shaped TSV technology is more realistic from industry point of view, as it is hard to form sharp edges of square shaped TSVs due to variations, so it is going to end up with cylindrical TSVs that is more realistic and easier for fabrication. It is mentioned in this work that "it is almost impossible to use look up table to compute TSV capacitance because too many variables exist" [20]. Where in our work a simulation based technique is used to build the macro-model which uses a look up table to calculate the capacitance value and that shows the strength of our work.

2.4.2 RoshanWeeraskera. [21]

This PhD thesis presents some work on characterization of isolated TSV, coupling parameters between just two TSVs and coupling parameters between bundles of TSV. Variation of capacitance, inductance and resistance of a single TSV with different dimensions of TSV physical parameters (radius, length and dielectric thickness) are presented. While only variations of coupling capacitance and inductance between two TSVs and bundles of TSVs with different dimensions of TSV physical parameters (including pitch) are considered,neglecting the resistive coupling. For bundles of TSVs only the full matrix 3x3 array of TSVs structure is considered, but all coupling capacitances between the TSVs in that array are considered, not just coupling between middle and surrounding. While in our work larger structures of TSV arrays are considered which is expected to be the case in nowadays technologies.

Figure2-8 shows variation of both self and total capacitance with pitch.Self-capacitance results from electric field lines that don't terminate on other surrounding TSVs. So it is intuitive that as the pitch increases the TSVs becomes far from each other so less amount of electric field lines can reach other TSVs and get terminated on there surfaces. That means more electric field lines stay with the current TSV, results in larger self-capacitance value. While lower electric filed lines reach other TSVs means that coupling capacitance values are reduced by increasing pitch. Coupling capacitance is more effective in total capacitance value, as there is a coupling capacitance with all the surrounding. So coupling capacitance is the larger portion of total capacitance. Total capacitance is summation of all coupling and self-capacitances of a TSV. So as the coupling capacitance decrease the total capacitance decreases.

Also this work presents models for isolated TSV, two parallel coupled TSVs and bundle of TSVs with a closed form expression for each model parameters. Two methods are used to obtain those closed form expressions which are: response surface method [28] and dimensional analysis [29]. The model of a 3*x*3 bundle of TSVs is shown in Figure2-9. A cylindrical shaped TSV technology is used in this work which is similar to the technology used in our work.

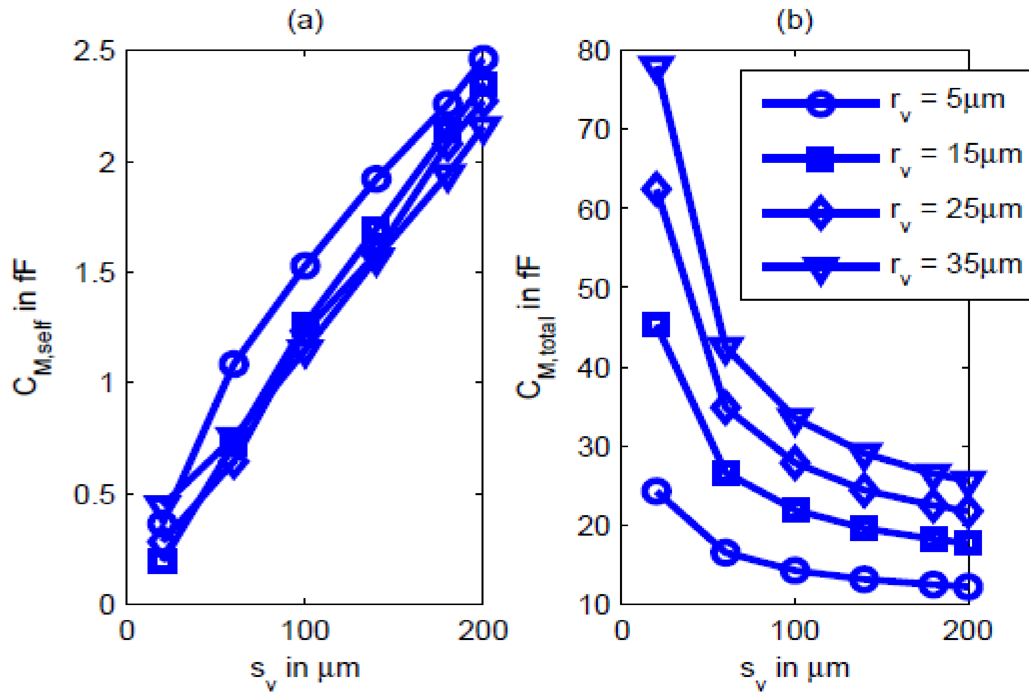


Figure 2- 8Self (a) and total (b) Capacitance of centric TSV in 3 × 3 bundle. [21]

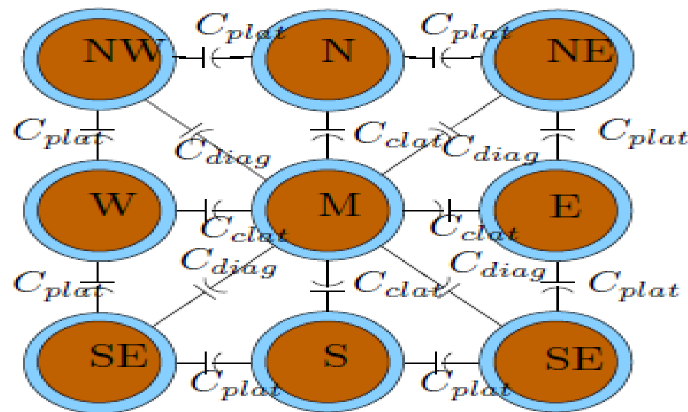


Figure 2- 9TSV bundle nearest neighbor coupling capacitances. [21]

2.4.3 BiancunXieet al. [22]

In [22]coupling between TSVs in a bundle is illustrated, where a coupling analysis method for large size TSV array is proposed. The lumped element modeling technique is replaced by full wave analysis method which is scalable to multiple TSVs.An efficient numerical method is used to model the TSV based on cylindrical modal basis functions[30]. No closed form expressions for coupling parameters are proposed. But s-parameters and noticing of coupled waveform is used to present the coupling effects between TSVs in bundles. Figure 2-10 shows s-parameters for a 5*x*5 array of TSVs, it can be noticed that coupling effect is larger at higher frequencies.

In conclusion, this chapter presents different models for isolated TSV, two parallel coupled TSVs and bundle of TSVs are presented. An algorithm that is used to calculate coupling capacitance for bundle of TSVs, which uses model based technique to build the model, is presented. Some works in literature that present electrical characterization for models parameters with variation in TSV physical dimensions (radius, length, dielectric thickness and pitch) are also presented.It is shown in previous work [14] that capacitive and resistive coupling is important and should be considered while building the macro-model. Inductive coupling can be neglected, as its value is not affected by the surrounding environment as shown in Figure 2-11b. While capacitive and resistive coupling are affected by the surrounding environment as shown in Figure2-11a and Figure 2-11c, where a, b, c, d, e are TSV arrays differ in number of TSVs exist in each array. Only Capacitive coupling is considered in this work, while resistive coupling is left for future work.

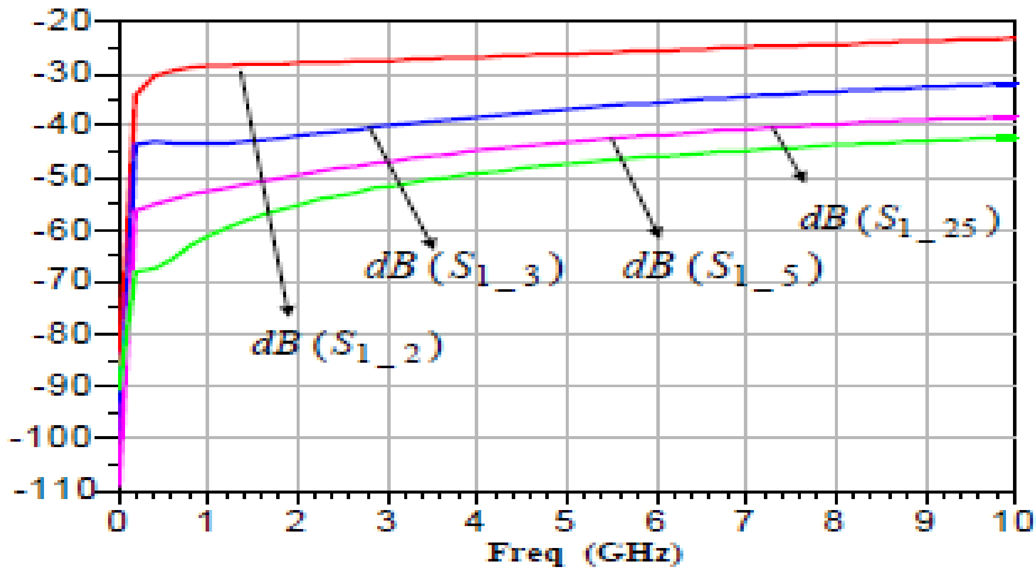
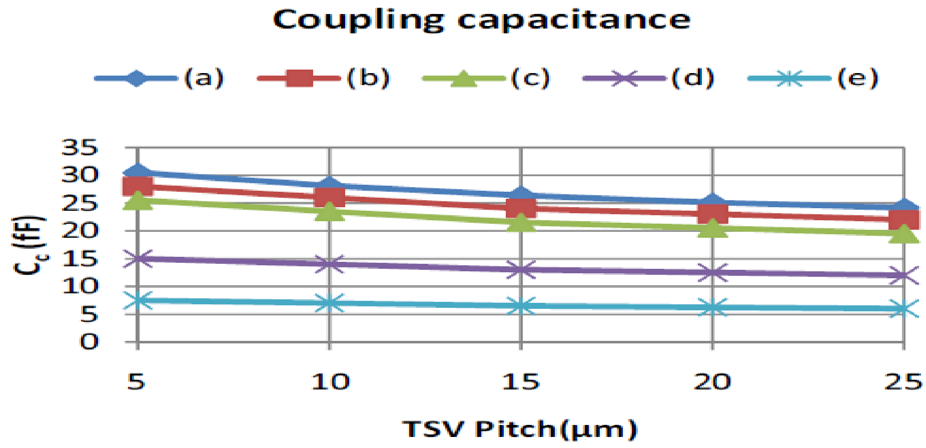
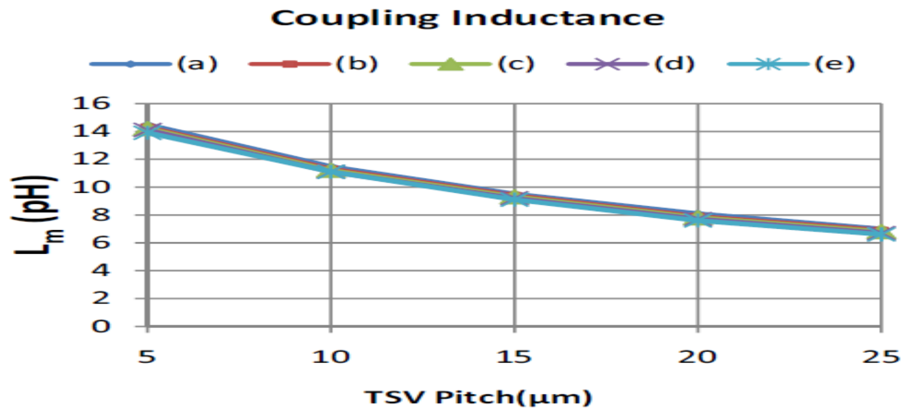


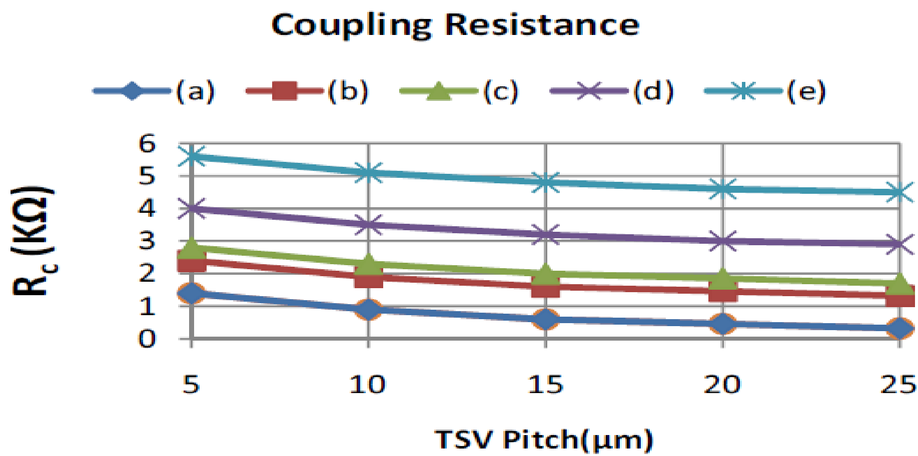
Figure 2- 10Coupling S-parameters between different TSV pairs. [22]



(a)



(b)



(c)

Figure 2- 11The coupling (a) capacitance, (b) inductance and (c) resistance change with respect to distance for different TSV arrangements. [18]

Chapter3

Algorithm

In this chapter the assumptions that are taken in the structure of the TSVs bundle are presented. Then the proposed algorithm is illustrated. After that, window size effect and appropriate window size choice for the algorithm are discussed. Subsequently, different structures of the window are presented and discussed to show how surrounding TSVs effect on each other. Thereafter, it is shown that total number of structures that have to be considered for the chosen window size can be reduced. Then solution for double counting issue resulted from using sliding window technique is discussed. Finally, Different techniques to build a macro-model and different techniques for characterizing bundles of TSVs are defined.

3.1 TSV distribution in a chip

During our work it's assumed that any given distribution of TSVs can be converted to be a grid matrix where the step between TSVs is the minimum distance between anytwo neighbor TSVs in that distribution.TSV structures can be classified into regular and irregular arrays. "**Regular Structures**" are TSV structures in which TSVs exist in all possible places in the grid as in Figure.3.1a. "**Irregular Structures**" are TSV structures in which there are possible places don't contain a TSV, as in Figure.3.1b. Having a grid doesn't mean that the distribution is always regular, as the absence of TSVs from its position in that gird results in irregular distribution of TSVs or what is called in our work irregular structure of TSVs.A 7x7 full grid is shown in Figure.3.1a; it looks regular but as shown in Figure.3-1b the absence of some TSVs from the grid results in an irregular distribution of TSVs.

It is recommended to have TSVs in cluster in order not to have coupling between TSVs and devices. Also, in that case it is easier to build an algorithm that can cover different perspectives and different coupling parameters.

Structures of TSV bundles can be classified into four categories depending on the number of existing TSVs in the array: Dense, Middle Dense, Middle Sparse and Sparse, where:

- **Dense:** for an array of TSVs of size *nxn* a full matrix contains n^2 TSVs, so dense structures contain from 75% to 100% of possible number of TSVs. An example of dense structures is shown in Figure3-2a.

- **Middle Dense:** for an array of TSVs of size *nxn* a full matrix contains n^2 TSVs, so middle dense structures contain from 50% to 75% of possible number of TSVs. An example of middle dense structures is shown in Figure3-2b.

- **Middle Sparse:** for an array of TSVs of size *nxn* a full matrix contains n^2 TSVs, so middle sparse structures contain from 35% to 50% of possible number of TSVs. An example of middle sparse structures is shown in Figure3-2c.

-**Sparse**: for an array of TSVs of size *nxn* a full matrix contains n^2 TSVs, so sparse structures contain less than 35% of possible number of TSVs. An example of sparse structures is shown in Figure 3-2d.

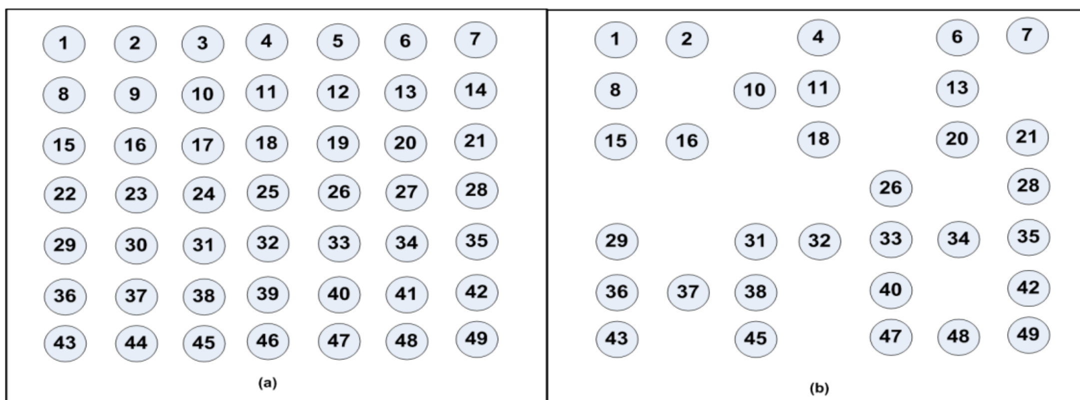


Figure 3- 1 Array of TSVs (a) regular, (b) irregular.

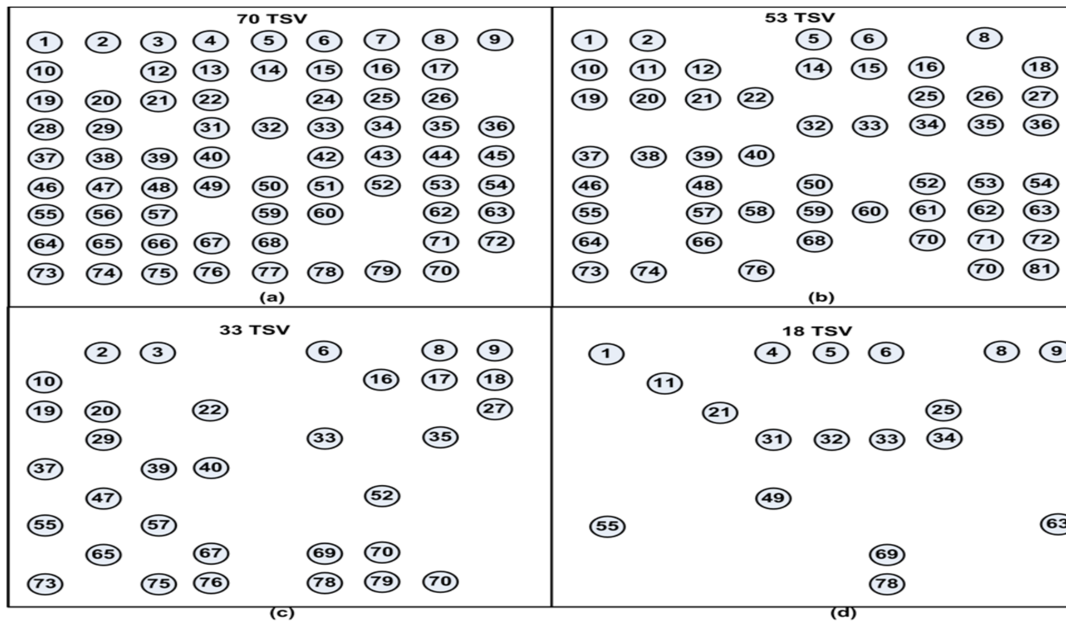


Figure 3- 2TSV structure density: a) dense (70TSVs), b) middle dense (53 TSVs), c) middle sparse (33TSVs), d) sparse (18 TSVs).

It is expected that middle sparse and middle dense have approximately the same shielding effects. As a result, it is expected to have same technique in building the macro-model and same behavior. As a result, both of these types can be considered as one type (middle dense or middle sparse) where the number of TSVs exist in the structure is from 35% to 75% of total possible number of TSVs in that array size.

3.2 Algorithm.

It is required to build a Macro-model for a bundle of TSVs distributed in a certain structure in a chip. A Macro-model means: building a model that focus on larger scalenot on a single TSV or single device but it consider the whole components in the system and find the interrelationship between them. Also it is a macro as it executes certain instructions in order to solve the given array of TSVs and it is a model as these instructions are fixed for any given distribution or dimensions of TSV arrays. The model is required to get all coupling parameters between allcomponents of the system and self-parameters of all components of the system. A reduced form of the macro-model is to consider coupling between certain components of the system like coupling between TSVs and each other and coupling between TSVs and wires. Another reduced form of the macro-model is just to consider the capacitive effect while neglecting inductive and resistive effects. The macro-model proposed in this work considers both coupling capacitance between TSVs and self-capacitance of each TSV, neglecting coupling inductance as illustrated in chapter 2, and leaving coupling resistance for future work.

It is required to solve large array structures of TSVs that contain large number of TSVs. But trying to solve the whole structure at one step would be very complex as a result of existence of many aspects that affect parameters needed to be extracted (i.e. capacitance, inductive and resistive coupling). Therefore, it is recommended to divide the large structure into smaller structures (i.e. sub-structures) these can be solved easily then combine the solution of the small structures to obtain the solution of the original large structure. The previous idea is similar to a divide and conquer algorithm [30]. Divide and conquer paradigm consists of the following major phases:

1- Divide the problem into smaller sub-problems that are similar to original problem but smaller in size and can be solved easily.
2- Solve sub-problems recursively.
3- Combine solution of sub-problems in order to create a solution to the original problem.

One of the main conditions in order to apply a divide and conquer algorithm is that the solutions of the sub-problems can be integrated to form the final solution of the original problem. That can be satisfied in large TSV structures and is shown in our proposed algorithm. The proposed algorithm is a sliding window algorithm, where instead of

solving the whole structure; a window is used to choose a smaller group of TSVs that can be solved easily. Then the window slide to solve other group of TSVs till it finishes the whole group of TSVs present in the original TSV array.

Figure3-3 shows flow chart of the proposed algorithm.The algorithm is considered as a sliding window algorithm. . First, the structure to be solved is read from the user. Thereafter, first TSV (i.e. TSV 1) becomes the centric TSV of the formulated window, as shown in Figure3-4a. The window defines a sub-structure inside the original structure. "**Sub-structure**" is a group of TSVs defined by the formulated window and it is inside the original structure that is read from the user. For a window size of 3x3 the formed sub-structure when the window is centered over TSV 1 contains TSVs 1, 2 and 5. These TSVs are the only considered TSVs when solving that sub-structure and all other surrounding TSVs are neglected. Then the window slides to the next TSV in order (i.e. TSV 2), as depicted in Figure3-4b. The window defines the new sub-structure that is going to be solved which in that case contains TSVs 1, 2, 3, 5, 7. Each time the window slides it makes the next TSV in order as the centric TSV and defines the new sub-structure that is going to be solved. As depicted in the flow chart in Figure3-3, the window keeps sliding till it reaches the last TSV in the given structure as shown in Figure3-4c. For two consecutive TSVs in the array where there are no empty TSVs in-between, it is noticeable that coupling capacitance exists between these two TSVs is calculated twice, once at each window. This double counting issue needs to be solved. Therefore, capacitance matrix should be updated to have just one capacitance value between two TSVs. More details about solving the double counting issue are mentioned in section 3.4. After updating the capacitance matrix, solution is generated with these capacitance values obtained in the capacitance matrix.

It is easy to combine solutions obtained at different windows using the proposed algorithm as every TSV can exists in more than one window. That is the sort of connection between the sub-problems (i.e. different windows) that result in a combined solution of the given structure after applying the algorithm and recursively repeat the capacitance calculation process at each window.

3.3 Window Structure

In this section more details about choosing appropriate window size are given. Then discussing how number of available structures or combination for the chosen window size can be reduced tremendously just by excluding the redundant structures. Finally, chosen structures for the chosen window size are discussed to show how the number of surrounding TSVs affects on the value of capacitances.

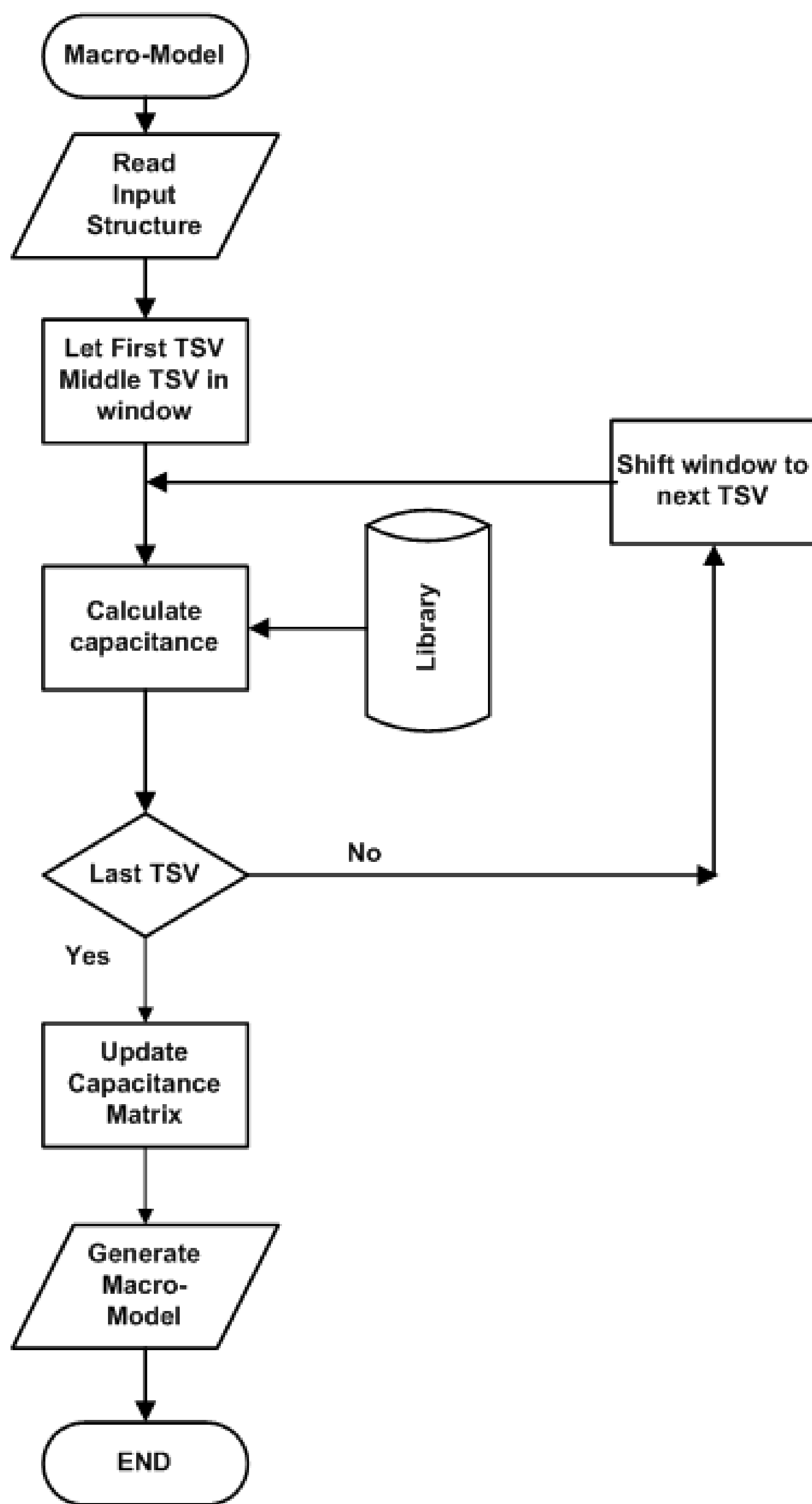


Figure 3-3Algorithm Flow Chart.

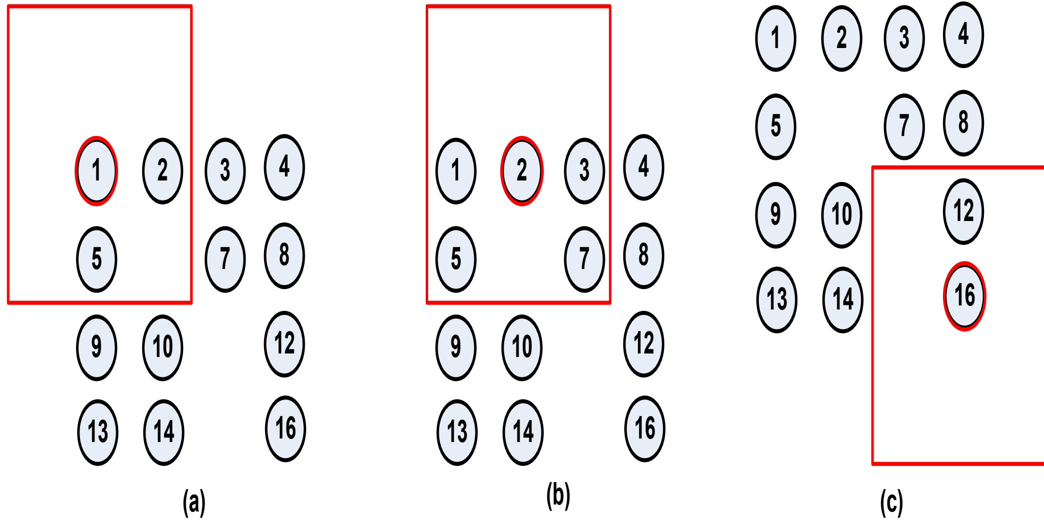


Figure 3- 4Sliding window of window size 3x3 applied on 4x4 structure, a) window on first TSV, b) window on second TSV, c) window on last TSV in the array.

3.3.1 Window Size

Our algorithm depends on having centric TSV, and then its self-capacitance and coupling capacitances with the surrounding TSVs are calculated. The dependence on a centric TSV existence means that window size should be an odd number in order to havecentric TSV. For the aid of symmetry and simplicity it is chosen that the window is square shaped. Main parameter that determines the chosen window size is the number of possible structures that can be obtained at that size. This number affects on the number of possible windows that can beformulated while building the macro-model and that is important in some cases especially while calculating capacitance values. As in case capacitance calculation depends on each window structure. In other words, each sub-structure has different equations, or may be different coefficients. Another case where window size is very important, as it determines the number of possible structures for the window, is when using a look-up table instead of equations to find the capacitance values. That means there would be an entry for each sub-structure in the library. So the number shouldn't be very large in order to be realistic to build that library, even if it is going to be builtonce and for all. In our work library based technique (simulation based model) is our target, thus number of possible substructures that are determined by window size is an important parameter. Equation (2) can be used to calculate the total number of possible structures for certain window size:

$$\text{Substructures Count} = \sum_{r=0}^{n} {}^{\mathrm{n}}\mathrm{C}_{\mathrm{r}} \qquad (2)$$

Where n represents square root of total number of available TSVs in full array of TSVs of size nxn, r is number of empty positions exist in the window.In case of a $3x3$ window size, n=3 means a full array contains 9 TSVsand in that case r=0, where r varies from 0 to 9. For r=4, means matrix contains 5 TSVs and there are 4 empty positions in a 3x3 window size.For r=9, means matrix is empty.

Figure3-5 shows plot of equation (2) for different array sizes.It clearly appears that number of possible structures (structures count) increases exponentially with array size.For 3x3 window size structures count is 512 and it increases to be 33.6 million when just increase the window size to $5x5$.Figure 3-6 gives the structures count for different array sizes at each possible number of empty TSVs in the array. Figure 3-6 shows that always the dominating number of structures count occurs when half of the array is empty and the other half contains TSVs.

Larger window size is expected to give better accuracy for the resulted macro-model as it considers larger number of capacitancesin the same window and considers coupling between more TSVs. The larger the window size the more shielding effect is considered in the same window because while calculating the capacitances the only seen TSVs are the TSVs inside the window. The smaller the window size the smaller the number of TSVs seen inside the window and then the smaller the shielding effect caused by surrounding TSVs is discovered. From that discussion it is clearly expected that $5x5$ window-size would give better accuracy than $3x3$ window size. However number of possible structures in case of $5x5$-size can't be handled and would be very difficult to build a library contains all these 33.6 million possible sub-structure. That's why a $3x3$ window size is chosen in our work. As our case of interest is dense type structuresand as the electric field lines are terminated on conductors surface, so a TSV exists in the same line between two TSVs would shield the electric field lines to move in-between.That means the coupling capacitance between these TSVs would be very small, only a small fringe capacitance would exist. Therefore, as the structure is dense a $3x3$ window size would be enough to capture the most important capacitances that have large values. While the remaining capacitances would be very small thus it is acceptable to be neglected.

3.3.2 Structures Count Reduction

Total number of possible window structures can be reduced by two means:

1- Centric TSV Existence
2- Redundant Structures Removal

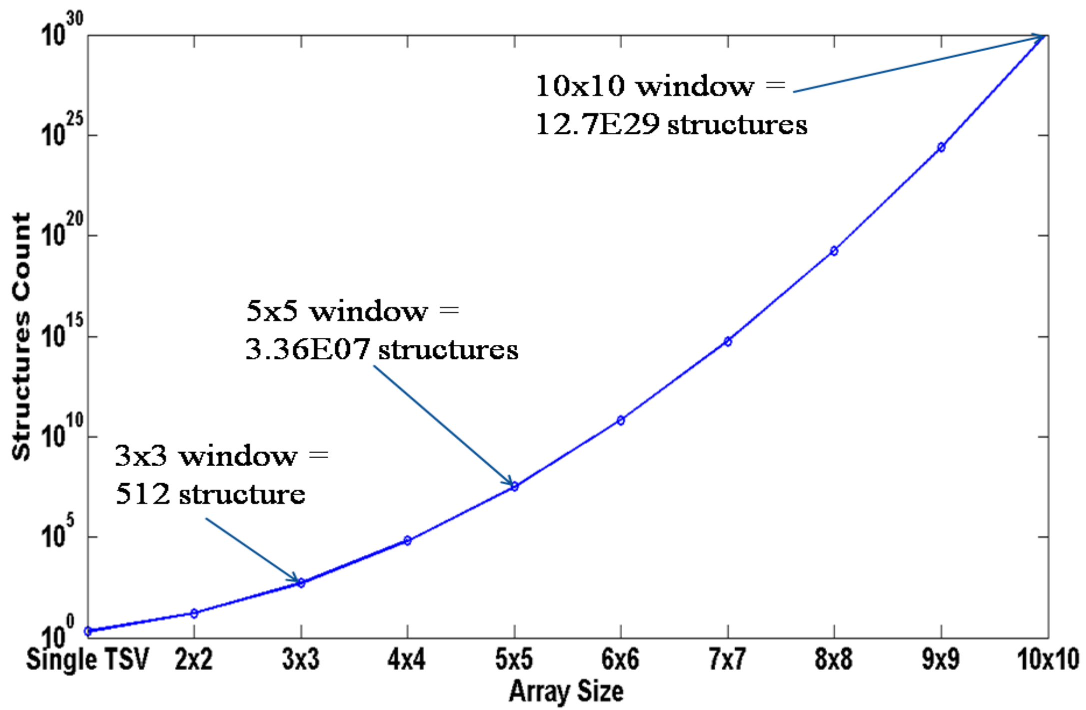


Figure 3- 5Sum of Structures Count for Different Array Sizes.

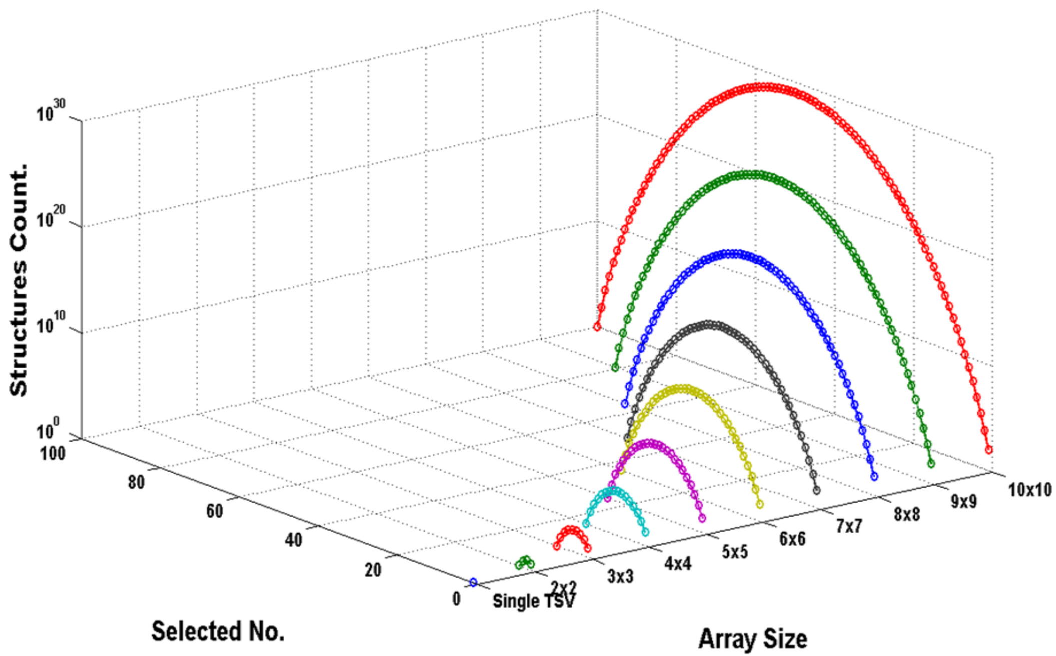


Figure 3- 6Structures Count for Different Array Sizes and Selected Number of Empty TSVs.

3.3.2.1 Centric TSV Existence

In our algorithm a window should include centric TSV, where window moves on each TSV and place it in the center. Structures with no centric TSV exists can be excluded and no need for it in the library, as it wouldn't ever occurs while building the macro-model. In that case Equation (3) can be used to calculate total number of possible structures (Sub-structure count):

$$\text{Substructures Count} = \sum_{r=0}^{n-1} {}^{\mathrm{n-1}}\mathrm{C_r} \tag{3}$$

Figure3-7 shows plot of equation (3) for different array sizes compared to plot of equation (2).As shown in Figure3-7 and as can be proved by dividing both the equations, structures count according to equation (3) is half structures count according to equation (2). Consequently, for a 3x3 window size structures count after removal of structures with no centric TSVs is going to be 256 structures. While for a 5x5 window size the number is 16.8 million which is still very large number.

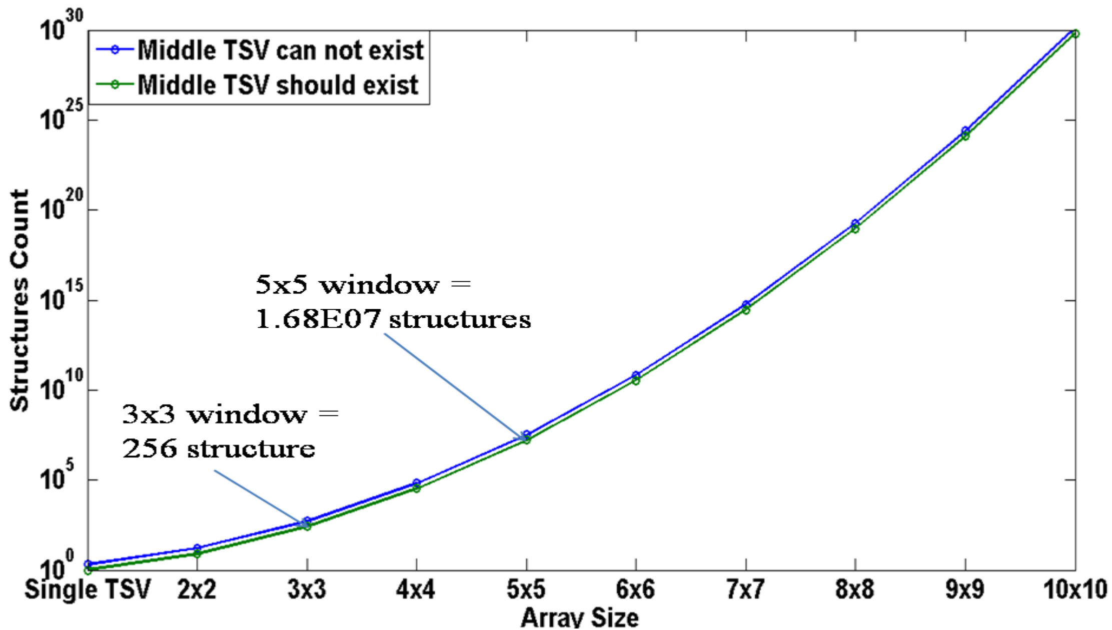


Figure 3-7Structures Count Where a Centric TSVcannot exist and Structures Count Where Centric TSV Should Exist.

3.3.2.2 Redundant Structures Removal

It is noted that some of the possible structures of the window is just a mirror or one of the three rotated versions of the same sub-structure or one of the three rotated versions of the mirrored version. In that case it is expected that the capacitance matrix is going to be just the mirror or rotation of the original capacitance matrix. Capacitance matrix of the mirrored sub-structure is going to be mirror of the original capacitance matrix wither it is

mirrored around x-axis or y-axis, thus the equivalent capacitance matrix is also mirrored around x-axis or y-axis respectively. Similarly, for the case of rotation, the number of rotations occurs to the original sub-structure is going to be the number of rotations occurs to capacitance matrix to get the equivalent capacitance matrix of that rotated structures and in the same direction of rotation.

Figure3-8a shows a window sub-structure, Figure 3-8b is the result of rotating Figure3-8a to left and Figure3-8c is rotation of Figure3-8b to left which is the result of rotating Figure3-8a twice. Note that numbering on the TSVs is fixed and doesn't rotate with rotating the sub-structure as the number is given according to the position of the TSV in the array. However each TSV is given a color to clarify the change of position of each TSV with rotation. Figure3-9a is the capacitance matrix of the centric TSV (TSV5) which contains total capacitance of TSV 5 at the middle of the matrix and coupling capacitance between TSV 5 and the surrounding TSVs in rest of the cells. Figure3-9b is the capacitance matrix of Figure 3-8b and it is clear that it is just the rotation to left for capacitance matrix shown in Figure 3-9a. While Figure3-9c is the capacitance matrix of Figure 3-8c and it is clear too that it is just the rotation of capacitance matrix in Figure3-9b or two time rotation to left for capacitance matrix shown in Figure3-9a. Therefore, all of these structures can be replaced by just one non-redundant sub-structure and if any of these rotated versions appeared the capacitance matrix can be obtained from the non-redundant entry exist in the library.

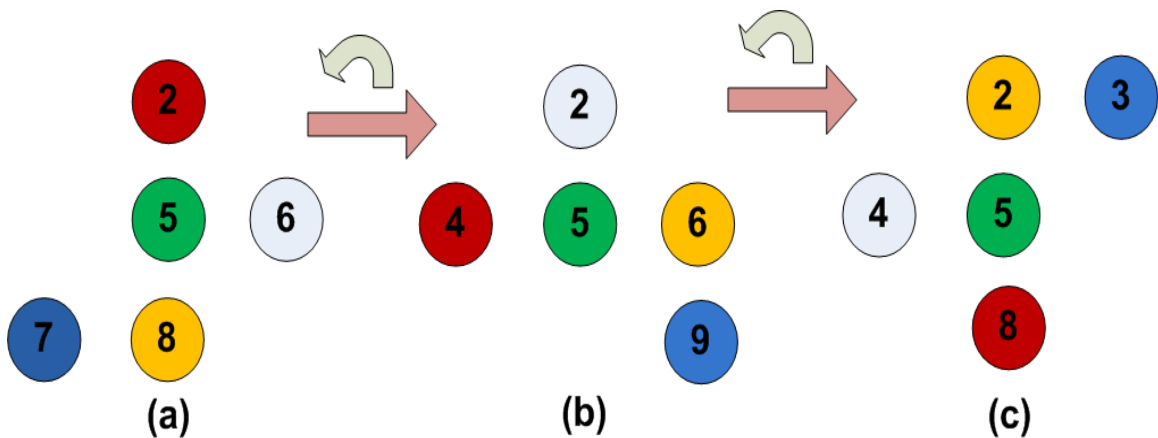


Figure 3- 8TSV Sub-structure (a)4empty places in a 3x3 sub-structure.(b) Rotation of a to left by 90. (c) Rotation of b to left by 90.

0	4.2	0
0	14.6	3.7
2.23	3.6	0

(a)

0	3.7	0
4.19	14.5	3.6
0	0	2.22

(b)

0	3.6	2.22
3.7	14.5	0
0	4.19	0

(c)

Figure 3- 9 a) Capacitance values of centric TSV for Figure3-8a, b) Capacitance values of centric TSV for Figure3-8b, c) Capacitance values of centric TSV for Figure3-8c. Capacitance values obtained from Q3D extractor-quasi static EM simulator.

Figure 3-10a is the same sub-structure in Figure3-8a and if that sub-structure is mirrored around x-axis Figure3-10b is resulted. Figure 3-11b is the capacitance matrix of the mirrored sub-structure shown in Figure3-10b. It is clear that this capacitance matrix is just the mirror of the capacitance matrix shown in Figure 3-11a where Figure 3-11a is the capacitance matrix of original sub-structure shown in Figure 3-10a. In case of rotating Figure 3-10b to left Figure 3-10c is resulted, or to right Figure 3-10d is resulted which are structures different from these obtained by rotating the original sub-structure shown in Figure 3-8a. Moreover, capacitance matrices of these structures can be obtained from original capacitance matrix just be mirroring and rotating the original capacitance matrix. So, it means that these are redundant structures too and can be removed.

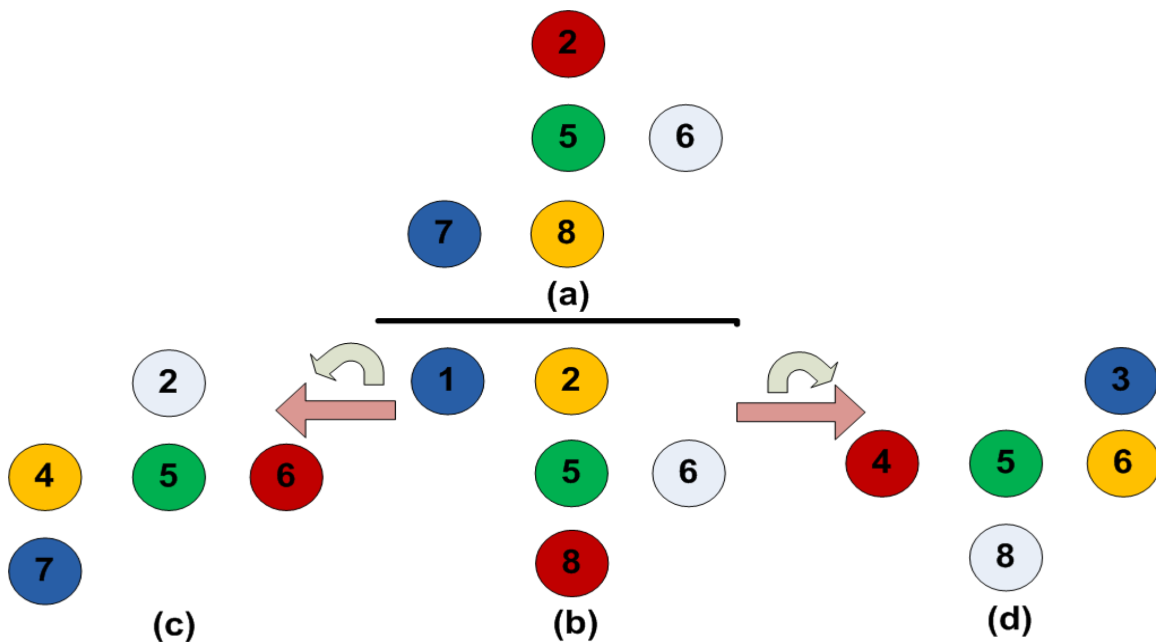


Figure 3- 10 a) Original Sub-structure, b) Mirror of a around x-axis, c) Rotation of mirrored sub-structure to left by 90°, d) Rotation of mirrored sub-structure to right by 90 °.

0	4.2	0
0	14.6	3.7
2.23	3.6	0

(a)

0	3.7	0
3.6	14.6	4.2
2.23	0	0

(c)

2.22	3.6	0
0	14.6	3.7
0	4.2	0

(b)

0	0	2.23
4.2	14.6	3.6
0	3.7	0

(d)

Figure 3- 11a) Capacitance values of centric TSV for Figure3-10a, b) Capacitance values of centric TSV for Figure3-10b, c) Capacitance values of centric TSV for Figure3-810, d) Capacitance values of centric TSV for Figure3-10d. Capacitance values obtained from Q3D extractor-quasi static EM simulator.

It can be concluded that redundantsub-structure can be resulted from:

i- Rotation of a non-redundant sub-structure. That means 3 structurescan be removed, as the 3 rotated versions of a sub-structure would have the same capacitance matrices.

ii- Mirror sub-structure which adds one extra sub-structure to be removed and 3 rotations for the mirrored sub-structure means another 3 structures can be excluded.

So for one sub-structure maximum number of equivalent redundant structures that can be found and excluded in all possible structures would be 7 structures. Some cases rotation of mirrored structures is similar to one of the rotations of the original sub-structure. In that case maximum number of equivalent redundant structures for these structures is only 3. There arealso some structures that haveonly one similar sub-structure and some structures that have no redundant structures at all.

A C-module is implemented to generate all different structures of a window size 3x3 under condition that each sub-structure should include a centric TSV as illustrated in flowchart in Figure 3-12a. Subsequently, the resulted total number of possible structures

as illustrated before is 256. A redundant extraction module is implemented using C-programming language as illustrated in the flowchart in Figure3-12b. After extracting all the redundant structures the rest of non-redundant structures (unique structures) are found to be 51 structures. The number of non-redundant structures is the number of structures that should be simulated and included in the library. Therefore, with these reduction methods for the possible structures count an order of magnitude reduction obtained, where structures count is reduced from 512 to be 51 unique structures.

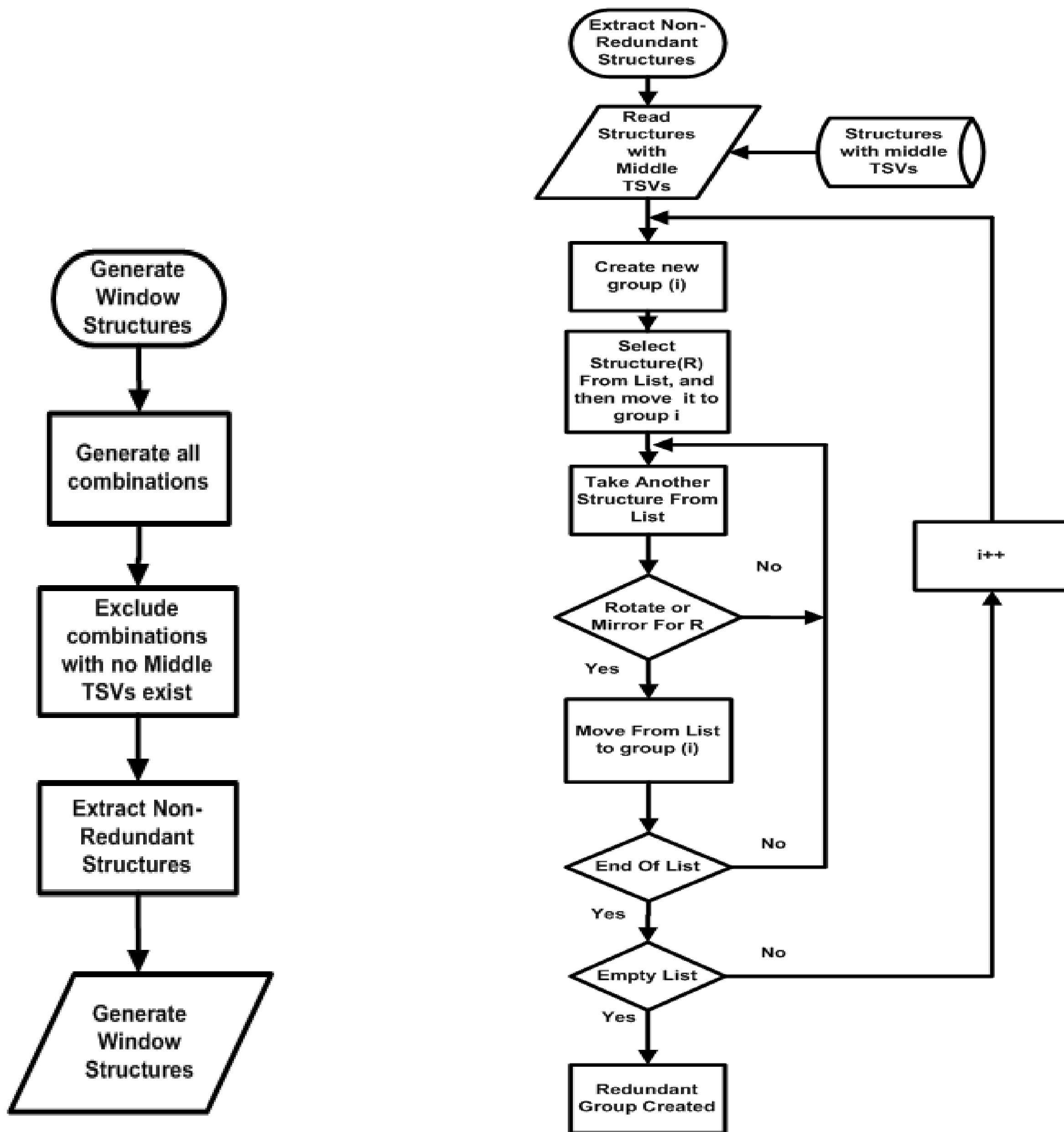


Figure 3-12(a) Flowchart of generating non-redundant window structures. (b) Flowchart of redundant structure extraction.

3.3.3 Different 3x3 Structures

In this section different sub-structure for a window of size 3x3 is discussed.It is illustrated that the capacitance value varies tremendously with count of surrounding TSVs for the TSV of interest. Surrounding TSVs result in shielding effects, where each of the TSVs in the neighborhood absorbs electric field lines so the amount of electric field lines moves from the TSV of interest to another TSV is reduced. As amount of electric field lines moves from a TSV to another is reduced also the coupling capacitance value between these two TSVs is reduced. The position of the surrounding TSVs to TSV of interest effects on amount of shielding occurs and hence reduction occurs to coupling capacitance. Perpendicular TSVs absorb more electric field than diagonal TSVs, supposing the case of a grid matrix, as the distance of perpendicular TSVs is shorter than distance between a TSV and another on its diagonal. Therefore, coupling capacitance between perpendicular TSVs (i.e. 1st inline coupling capacitance) is larger than coupling capacitance between diagonal TSVs (i.e. diagonal coupling capacitance). Number of surrounding perpendicular TSVs and number of surrounding diagonal TSVs affectsthe amount of reduction occurs to coupling capacitance and even for self-capacitance. Self-capacitance also got affected by amount of shielding because it is resulted from amount of electric field line that isn't absorbed by any of the surrounding TSVs or devices. Thus, as shielding increases that means more TSVs exist and more electric field is absorbed results in lower self-capacitance value.

There are different capacitances types that can exist in a window shown in the following:

1st neighbor coupling cap (1st inline): it exists between any two direct neighbor TSVs and can't be neglected for different structure as it has the largest value among different capacitance types. Example of it is shown in Figure3-13a.

2nd neighbor middle cap (2nd inline middle cap): exists between a TSV and its second neighbor on the same straight line (row or column) where the row or column that contains these TSVs exists in the middle of the matrix with the existence or absence of a TSV in-between. Example of it is shown in Figure 3-13b.First and second types can be included in a more generic name which is "*m* inline middle cap", where *m* can be any number between 1 to *n* (*n* is size of the given array).

2nd neighbor peripheral cap (2nd inline peripheral cap): exists between a TSV and its second neighbor on the same straight line (row or column) where that row or column exists at the peripheral (edge) of the matrix with the existence or absence of a TSV in the middle between them. The difference between the middle 2nd neighbor cap and the peripheral 2nd neighbor cap comes from the shielding for the TSVs at the middle ismore than the TSVs at the edges (peripheral). Example of that capacitance type is shown in Figure 3-13c.

Diagonal cap (diagonal cap): it is the direct coupling capacitance between a TSV and its direct neighbor where its place exists on the diagonal to that TSV. The formed triangle have two equal sides equal to the pitch and the diagonal is the third side that connects the coupling capacitance between the two TSVs and equal to (√2 *x* pitch). Example of that capacitance type is shown in Figure3-13d.

2nd diagonal Cap: it is the coupling capacitance between a TSV and its 2nd neighbor where its place exists on the diagonal to that TSV with the existence or absence of a TSV in the middle. The formed triangle have two equal sides equal to twice the pitch and the diagonal is the third side that connects the coupling capacitance between the two TSVs and equal to (2√2 *x* pitch). Example of that capacitance type is shown in Figure 3-13e. Both fourth and fifth types can be included in a more generic name which is"*m* diagonal cap" where m can be any number between 1 to *n* (*n* is size of the given array).

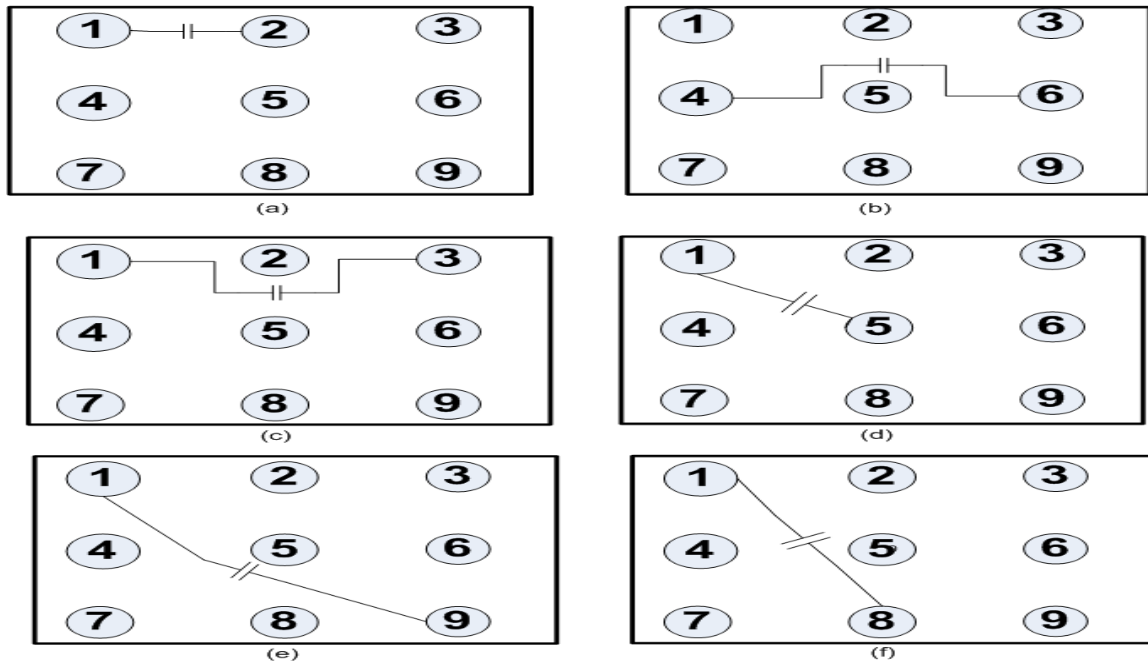


Figure 3- 13 Different Capacitance types: a) 1st inline, b) 2nd inline middle, c) 2nd inline peripheral, d) diagonal, e) 2nd diagonal, f) Asymmetric.

Unequal diagonal cap (Asymmetric 2*x*1 Cap): is the coupling capacitance between a TSV and its far neighbor where its place exists on a diagonal to that TSV with the existence or absence of TSVs between them. The formed triangle have unequal sides,first side is equal to pitch and the second side is equal to twice pitch and the diagonal is the third side that connects the coupling capacitance between the two TSVs and equal to (√5 *x* pitch). Example of that capacitance type is shown in Figure 3-13f. More generic name to be asymmetric *mxr* capacitance, where *m*, *r* can be any number between 1 to *n* (*n* is size of the given array), but should be unequal.

In our algorithm mainly centric TSV of the window is the TSV of interest where its self and coupling capacitances are calculated. Capacitance types that exist in that case in a 3x3 window size are 1st inline coupling capacitance and diagonal capacitance. To show how the count of the surrounding TSVs affect on coupling capacitance value, coupling capacitance of unshielded sub-structure containing only two TSVs is compared to different structures contain more than two TSVs. That is done to notice the effect of increasing number of surrounding TSVs on coupling capacitance between the same TSVs. This procedure is done for both 1st in line coupling capacitance shown in Table.2 and diagonal coupling capacitance shown in Table.3.The sub-structure is represented in the form of zeros and ones. Zero means that this position is empty. One means that this position contains a TSV. Error represents the difference percentage of capacitance value between the unshielded sub-structure (i.e. neglecting the surrounding TSVs) and the shielded sub-structure (i.e. considering the surrounding TSVs) is calculated according to equation (4).

$$\boldsymbol{Error} = \frac{\boldsymbol{C_{unsh}} - \boldsymbol{C_{sh}}}{\boldsymbol{C_{unsh}}} * \mathbf{100} \quad (\%) \tag{4}$$

Table.2 and Table.3 shows how coupling capacitance value decreases with each time increasing number of surrounding TSVs. However as noticed in the tables and as shown by Figure3-14 that effect of shielding resulted by surrounding TSVs started to reduce when the array became middle dense (i.e. had more than 5 TSVs which is more than 50% of available places in the array). That means amount of reduction in coupling capacitance started to decrease when the TSVs of interest became totally shielded, so addition of more surrounding TSVs wouldn't affect the coupling capacitance value. It can be noticed from first three entries in the two tables that in middle sparse structures the effect of shielding or the amount of reduction that happen to the coupling capacitance depends on the position of the surrounding TSVs. That can be noticed from the lowering in the coupling capacitance when the surrounding TSV is in direction of electric field, for example when it goes from TSV5 to TSV6 or TSV3 as in entries 3 and 4 in both tables, than the case the surrounding TSV is far away from the two coupled TSVs as in entries 1 and 2 in the two tables. However existence of a TSV even if it is in the other direction of the two coupled TSV results in lowering coupling capacitance value from unshielded case. Furthermore, it can be noticed from entries 1 and 2 that the presence of a perpendicular TSV in the other direction of the coupled TSVs made more shielding than the case of existence of a diagonal TSV in other direction of coupled TSV. These results can give guidelines for the shielding effects caused by TSVs on each other. Coupling capacitance values are obtained from Q3D extractor simulations at certain dimensions (pitch, radius, dielectric thickness and height), so for different dimensions the effect may vary a little bit. As for a larger pitch, effect of having more surrounding TSVs which are

far from the coupled TSVs wouldn't affect much on the coupling capacitance value. So a further study is needed for shielding effect in case of different dimensions. This study would be very helpful in creating model based macro-model which depends on building a set of equations as going to be discussed in section 3.5. Thus, as far these shielding effects are noticed, then it should be included in the model to capture correctly variations in the coupling capacitance value with increasing the surrounding TSVs neighbors considering position of those TSVs.

Table 21st inline Coupling Capacitance for Centric TSV for different sub-structure and finding error result from shielding effect compared to unshielded sub-structure. @ Ptsv=15.6um, htsv=50um, rtsv=2.5um and tox=0.3um.

Entry	Unshielded Structure	Coupling Cap value (C_{unsh}) (fF)	Other Structure	Coupling TSVs	Coupling Cap Value (C_{sh}) (fF)	Error %
1	0 0 0 0 1 1 0 0 0	6.6284	0 0 0 0 1 1 1 0 0	TSV5 & TSV6	5.5997	15.52
2			0 0 0 1 1 1 0 0 0		5.4724	17.44
3			0 0 0 0 1 1 0 1 0		5.0843	23.30
4			0 0 0 0 1 1 0 0 1		5.0781	23.39
5			0 0 1 0 1 1 0 0 1		3.9238	40.80
6			0 1 1 0 1 1 0 0 1		3.4355	48.17
7			0 1 1 0 1 1 0 1 1		2.9928	54.85
8			1 1 1 0 1 1 0 1 1		2.9224	55.91
9			1 1 1 1 1 1 0 1 1		2.833	57.26
10			1 1 1 1 1 1 1 1 1		2.8103	57.60

Table 3 1st Diagonal Coupling Capacitance for Centric TSV for different structure and finding error result from shielding effect compared to unshielded structure. @ Ptsv=15.6um, htsv=50um, rtsv=2.5um and tox=0.3um.

Entry	Unshielded Structure	Coupling Cap value (C_{unsh}) (fF)	Other Structure	Coupling TSVs	Coupling Cap Value (C_{sh}) (fF)	Error %
1	0 0 1 0 1 0 0 0 0	5.3886	0 0 1 0 1 0 1 0 0	TSV5 & TSV3	4.4366	17.6669
2			0 0 1 0 1 0 0 1 0		4.1786	22.4548
3			0 0 1 0 1 0 0 0 1		4.1576	22.8445
4			0 0 1 0 1 1 0 0 0		3.3173	38.4386
5			0 0 1 0 1 1 0 0 1		2.9476	45.2993
6			0 1 1 0 1 1 0 0 1		1.5178	71.8331
7			0 1 1 0 1 1 0 1 1		1.3345	75.2348
8			1 1 1 0 1 1 0 1 1		1.1499	78.6605
9			1 1 1 1 1 1 0 1 1		1.1028	79.5346
10			1 1 1 1 1 1 1 1 1		1.0325	80.8392

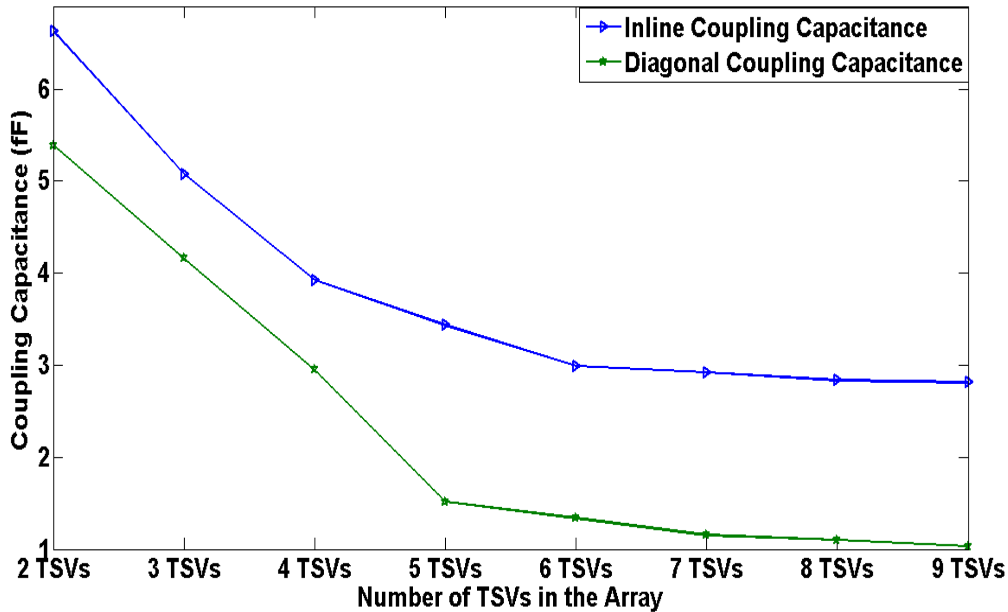


Figure 3- 14Coupling capacitance value between TSV5 and TSV6 for inline coupling capacitance and between TSV5 and TSV3 for diagonal coupling capacitance.

3.4 Double Counting

The algorithm for building the macro-model depends on a sliding window technique, and is described in section 3.2. For any two direct neighbor TSVs where there are no TSVs or empty positions in between, wither they are inline or diagonal, the capacitance between these two TSVs is calculated twice at two different windows. The final generated macro-model should contain only one capacitance value from these two values. Consequently, a function called "update capacitance matrix" is needed in order to solve that double counting issue and just get one value from those two calculated values.

Double counting can be solved using different options like:

i- Minimum double counting technique: take minimum value from the two capacitances.
ii- Maximum double counting technique: take maximum of either capacitance.
iii- Average double counting technique: take the average of both the capacitance values.

One of these options would give better accuracy, so more investigations are needed to choose the suitable technique to give better accuracy for the built macro-model.

The value of both calculated capacitances in two different windows would be equal in case that the two windows have same structure. Otherwise both values of calculated capacitances would be different. The main reason for different capacitance values calculated at the two windows is the different count of surrounding TSVs captured by each window. The window that gives a more accurate value is the window that

captures more surroundings. If more surroundings are captured that would be the actual case, as it means that these surroundings actually exist in the given sub-structure as it is captured by one of the windows. More surroundings means more shielding exists. More shielding means more electric field lines are shielded and less electric field lines moves between the two coupled TSVs. Lower electric field lines moves between two coupled TSVs results in a lower coupling capacitance value.

Lemma 1: "Taking minimum coupling capacitance value (i.e. minimum double counting solution) between two coupled TSV would give more accurate coupling capacitance estimation".

Supposing that first window captured the sub-structure in Figure3-15a when it stands on TSV2 and then after the window moves to TSV5 it captures the sub-structure shown in Figure 3-15b. In Figure 3-15b more shielding is discovered when the window slides to the other TSV. The coupling capacitance between TSV5 and TSV2 is given in Table.4 for different structures shown in Figure3-15. It is clear that the capacitance value decreased with more shielding exist. Q3D extractor can be used to measure the amount of electric flux density (D) that reaches TSV2 from TSV5 and from which electric field line that reaches TSV2 from TSV5 can be calculated using equation (5). Table.5 shows the calculated electric flux density that reaches TSV2 from TSV5 for different structures in Figure3-15. It is clear that the existence of more TSVs makes more shielding and results in lower electric flux density that reaches TSV2 from TSV5.

$$\boldsymbol{D} = \boldsymbol{\varepsilon_r \varepsilon_o E} \tag{5}$$

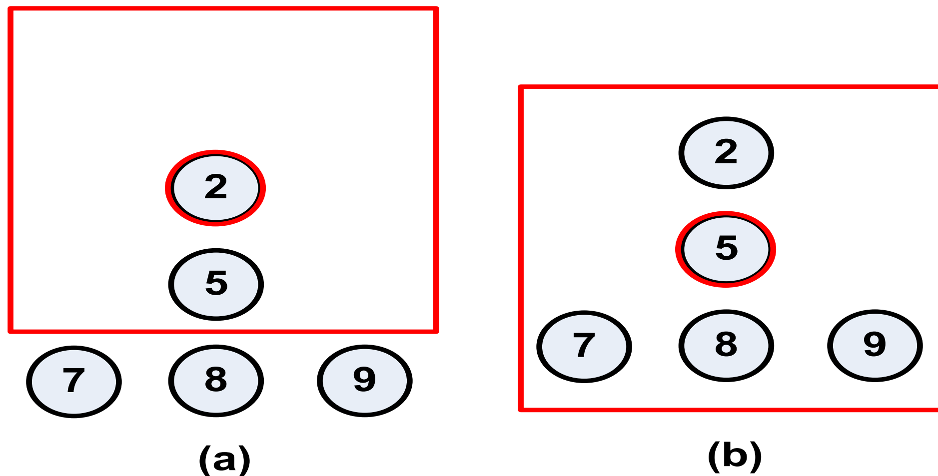


Figure 3- 15Two direct coupled TSVs showed in (a) with different surroundings as in (b), (c).

Table 4Coupling capacitance value between TSV5 and TSV2 for different sub-structure given in Figure3-15

	Figure3-15a	Figure3-15b
Coupling between TSV5 and TSV2 (fF)	6.6284	4.77

Table 5 Electric flux density that reaches TSV2from TSV5 for different sub-structure given in Figure3-15.

	Figure3-15a	Figure3-15b
Electric flux density that reaches TSV2 from TSV5 (C/m2)	4.87e4	3.97e4

From previous discussion it can be concluded thatthe more shielding exists the lower the amount of electric field lines move between two coupled TSVs. Lower electric field lines moves between two coupled TSVs mean lower coupling capacitance value between these two TSVs. Therefore, when one of the two windows gives a lower coupling capacitance between two TSVs that means it captured more shielding which actually exists in the given structure. Thus, taking minimum value among calculated capacitances from the two windows would give better accuracy and solves the double counting issue. However it doesn't give 100% accuracy because of the existence of more shielding that a 3x3 window couldn't capture. But it gives better accuracy in calculating coupling capacitance value than other options (i.e. averaging or taking maximum).

Having better accuracy from minimum double counting technique in finding each coupling capacitance value doesn't mean it would give better accuracy in all capacitance types. Subsequently, more investigation for different double counting techniques is required for the whole model, where all model capacitances are considered including total capacitance of each TSV. Further study for other double counting techniques is given in chapter 5 after presenting the whole model accuracy.

3.5 Macro-Modeling Techniques

As presented in section 3.2 our proposed algorithm is a sliding window. A window of size 3*x*3 moves on each TSV in the given array of TSVs making each of them its central TSV. Thereafter, self-capacitance of centric TSV and coupling capacitances between the centric TSV and surrounding neighbors inside the same window are calculated. As shown in Figure 3-16, there are two techniques that can be used to calculate macro-model parameters (which are capacitances in our work) and build that macro-model:

a- Model Based.
b- Simulation Based.

a- Model Based:

In this technique a set of equations are used to find both self-parameters of the TSV and the coupling parameters between different TSVs in the given array of TSVs. It is expected to have different sets of equations for each sub-structure of TSVs (each possible window). Equations may differ in different sub-structure types of TSV arrays (dense, middle dense and sparse).

b- Simulation Based:

In this technique self-parameters of a single TSV and coupling parameters between different TSVs in the given structure are obtained using a look up table (LUT). The library can be built using any of the following methods:

i- Electromagnetic wave simulator: ex: Q3D Extractor, Quasi static EM wave simulator.
ii- Device simulator: ex: Synopsys-Raphael or Sentarus.
iii- Obtained from measurements of fabricated arrays of TSVs.

The library is built at certain dimension for the TSV array structure (pitch, radius, dielectric thickness and length). It is certain that these parameters changes from a given structure to another. Therefore, characterization for bundles of TSVs is needed in order to help in finding a relation that can capture the variations of both self and coupling capacitances of TSVs with different dimensions.

In this work simulation based technique is used to build the macro-model.LUT that contains the capacitances values both self and coupling for all possible structures of a 3x3 window (i.e. 51 possible structures) is used and built as shown in flowchart Figure3-16.The LUT contains capacitances values obtained from Q3D Extractor (quasi-static EM wave simulator) simulations for all possible structures. A scaling equation proposed in chapter 4 is used to capture the variations in capacitance values with dimension scaling. After adding the scaling equation part, the algorithm flowchart can be illustrated as shown in Figure3-18. Capacitance calculation with dimension scaling is done as shown in Figure3-19. As shown in Figure3-16, there are different ways to do characterization for bundles of TSVs, which helps in finding suitable coefficients for the relation proposed in chapter 4. Characterization can be classified into two methods:

a- Characterization per structure.
b- Characterization for all structures.

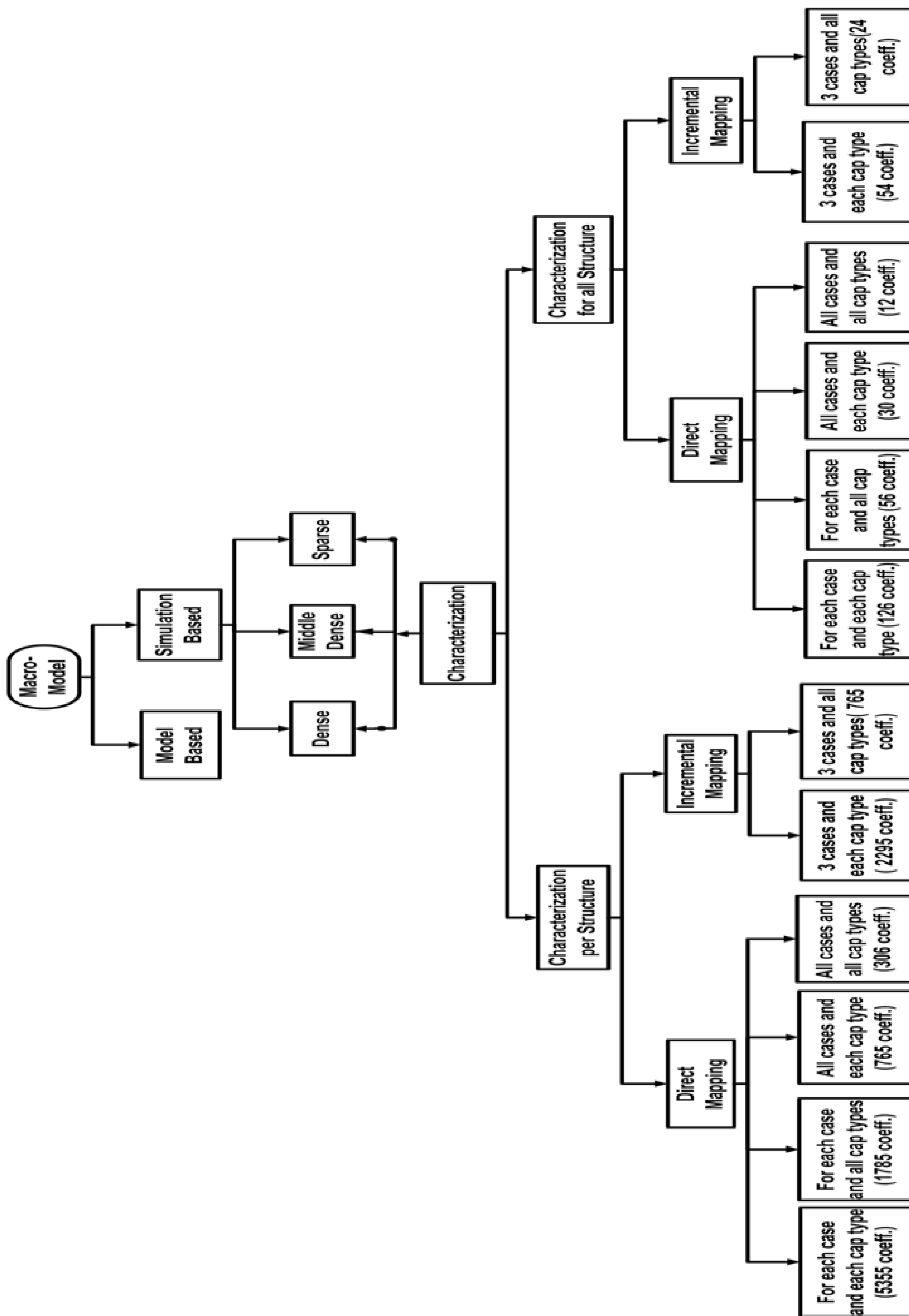


Figure 3- 16Chart gives different possibilities to build simulation based macro-model.

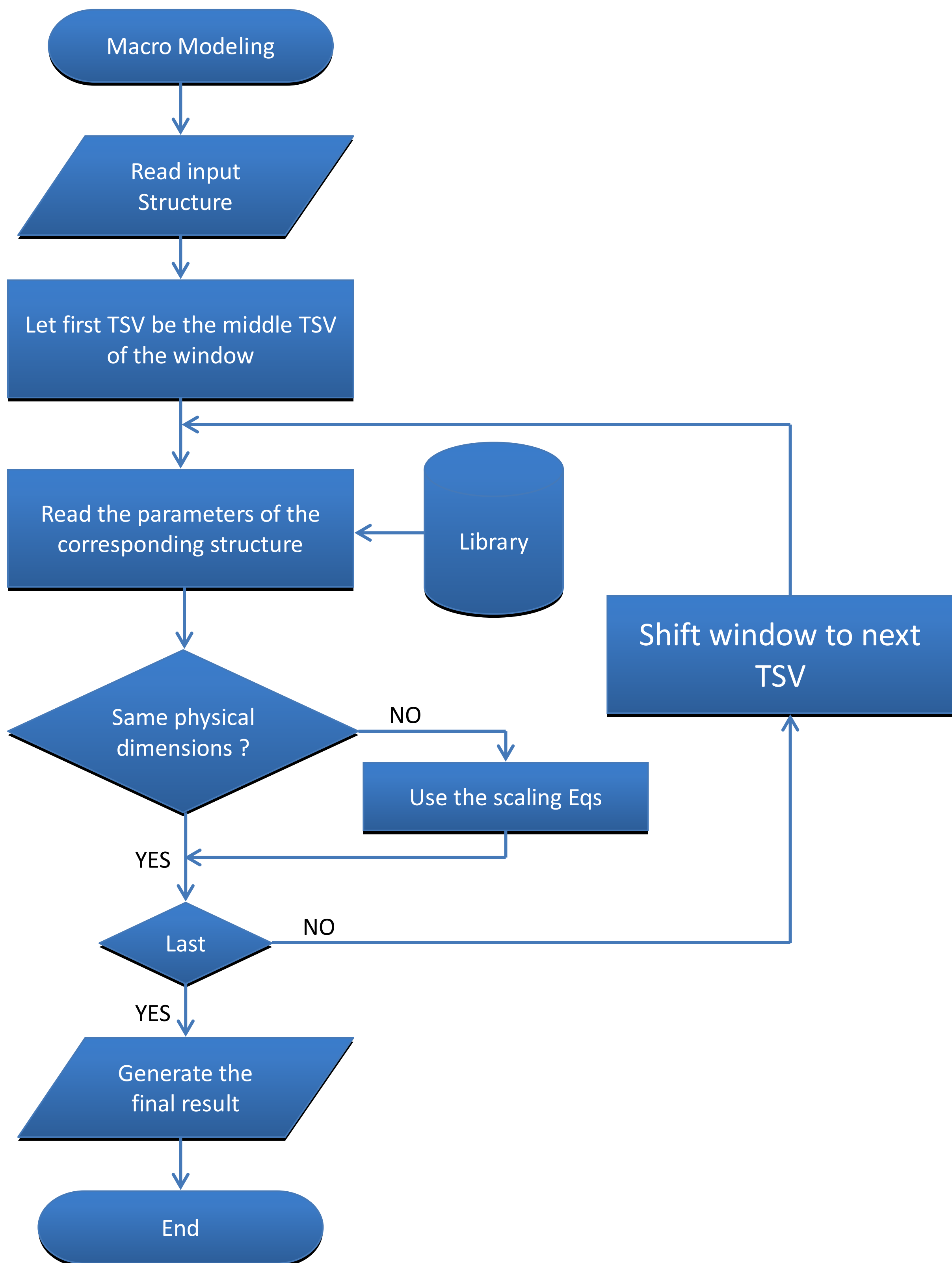


Figure 3- 17 Flowchart of implemented algorithm.

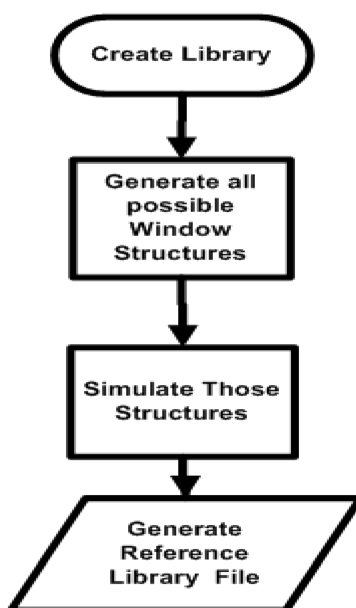


Figure 3- 18 Flowchart of creating the library.

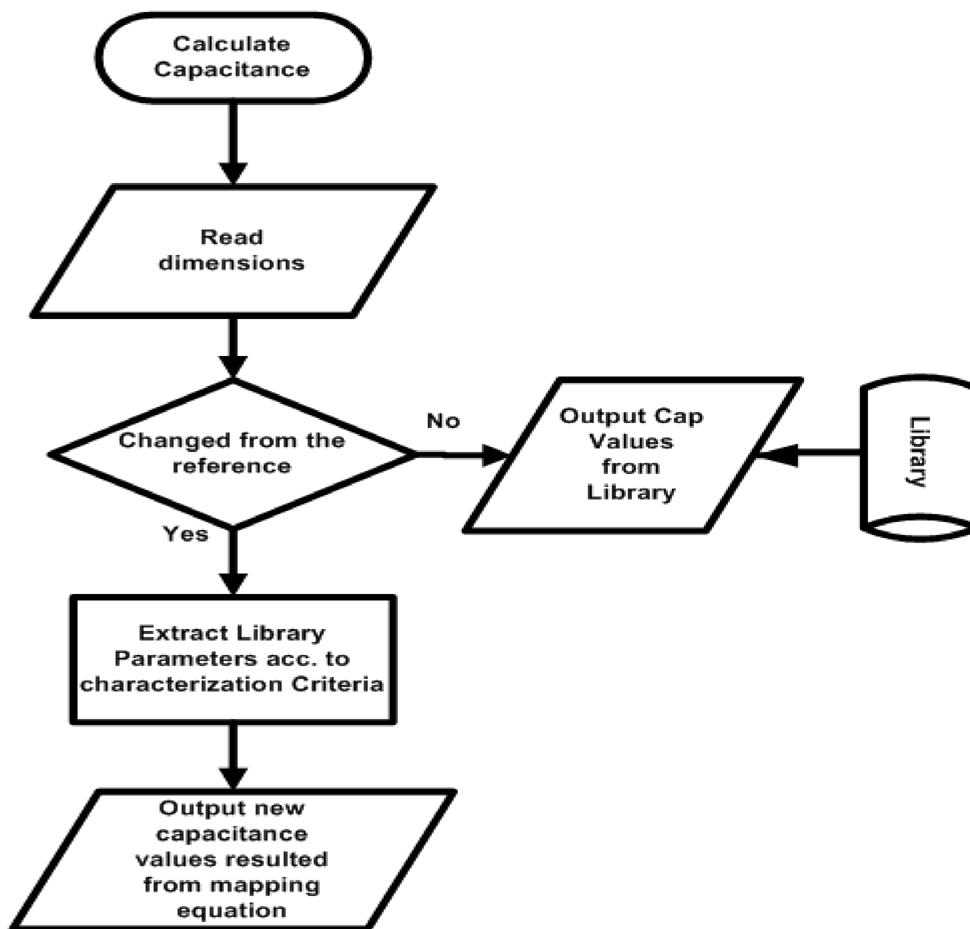


Figure 3- 19Flowchart of calculating capacitance in simulation based technique.

a- Characterization per structure:
In this method characterization is done on each structure separately of all possible structures (51 structures) to find its own set of coefficients that helps to capture variations occur to capacitances value with dimensional scaling.
b- Characterization for all structures:
In this method characterization is done to just one sub-structure and use optimization algorithm to find the coefficients suits that sub-structure. As capacitance value changes from window structure to another window structure, thus same coefficients obtained from one structure are expected to work with other structures. However more error is expected using that method. The aim of the characterization for just one sub-structure is to reduce total number of coefficients saved in coefficients library. However a higher number of coefficients for that sub-structure is used but would be applicable for all other sub-structure so the total number of required coefficients is lower compared for finding coefficients for each sub-structure. Another option for characterization for all structures is to do optimization to find the coefficients for some or all possible structures at the same time. Extra programming work is needed but can provide better accuracy than just doing the optimization for one sub-structure.

There are three capacitance types exist in each sub-structure for our proposed algorithm which are:

i- 1st inline coupling capacitance.
ii- Diagonal coupling capacitance.
iii- Total capacitance of the centric TSV.

Total capacitance is used to find self-capacitance more details about that is in chapter4. Different scaling scenarios considered depending on which of physical parameters changes from reference dimensions:

i- Pitch only.
ii- radius only,
iii- dielectric thickness only,
iv-pitch & dielectric thickness together,
v- pitch & radius together,
vi-radius & dielectric thickness together,
vii- Pitch, radius & dielectric thickness all together.

Length variations isn't considered in thatscaling scenarios, because the relation between variation of capacitance value with length of TSV is linear as proved in chapter 4 Figure 4-5. Subsequently, variation in capacitance due to changing the length can be calculated before doing further mapping due to variations of other dimensions.

Each of the previous methods can be done using two ways:

a- Direct Mapping.
b- Incremental Mapping.

a- Direct Mapping:

. Means to find the new capacitance value from the reference capacitance value at one step where no intermediate calculations are required.

b- Incremental Mapping:

In incremental mapping only 3 scaling scenarios of the seven scaling scenarios are considered which are: changing pitch only, changing radius only and changing dielectric thickness only. It is called incremental mapping as when more than one parameter changes more than one step is required to get the new capacitance value. For example, if pitch, radius and dielectric thickness changes, first an intermediate capacitance is calculated to capture variation occurs according to changing the pitch. Then another intermediate capacitance is calculated depending on the previous intermediate capacitance to capture the variation occurs in capacitance value due to variations in radius. In that step both of radius and pitch variations are captured. To obtain the new capacitance value a final step is done where the capacitance value is calculated depending on the last intermediate capacitance value that considered both pitch and radius variations to capture the variation occurs with changing dielectric thickness. At the end, all of the variations in dimensions occurred are considered but more than one step is required and that is the reason for the name incremental, as each step add to the previous step. More details about characterization and obtaining the suitable coefficients are discussed in chapter 4.

In conclusion, it is assumed that the given structure of TSVs is represented as a grid distribution. Grid distribution doesn't mean it is totally regular distribution but the absence of TSVs from their positions results in an irregular distribution. The proposed algorithm is a sliding window technique. A window moves on each TSV and places it in its center. Then calculate the self-capacitance of the centric TSV and the coupling capacitance that exists between centric TSV and other surrounding TSVs exist in the same window. Thereafter, a discussion is made about which window size is appropriate to be used in the proposed algorithm and how the number of possible structures grows up exponentially with size. Therefore, a 3x3 window size is chosen in our work so all possible structures can be handled. Subsequently, proposing how the number of possible structures can be reduced by two techniques: first, just having structures that havecentric TSV while excluding structures with no centric TSV. Second, removing the redundant structures and just leaving the unique structures that are not the rotation or mirror of each other. After that, different structures are presented to notice the shielding effect on the coupling capacitance and how shielding caused by surrounding TSVs results in reducing

the coupling capacitance tremendously. Then solution for the double counting issue is proposed showing that taking the minimum value gives better accuracy. Thereafter, different techniques that can be used to build the macro-model are defined. Finally different methods that can be used to characterize TSVs structures in order to capture the variation occur to coupling and self-capacitances with dimension scaling are presented.

Chapter 4

Dimension Scaling

As presented in previous chapter, a simulation based technique is used in this work to build the macro-model. A LUT is built that contains self and coupling parameters (i.e. capacitance in this work) of all possible structures for a window of size 3*x*3.These parameters obtained using Q3D extractor simulations for all possible unique sub-structure of the window at certain dimensions. Therefore, at different dimensions a relation is needed to capture the variation in capacitance values. In this chapter the proposed relation that can capture the capacitance variation with dimensions scaling is presented showing how it is implemented. In addition, different techniques that can be used to do characterization for bundles of TSVs (refer to Figure 3-16) are discussed, showing the number of coefficients needed in each flow. Thereafter, discussing why these coefficients are added and what is the responsibility of each coefficient. After that, a comparison between results obtain from Q3D and corresponding results obtained using scaling equation for a 3*x*3 window is shown. Subsequently, applying the algorithm for a test case of 71 TSVs in a 9*x*9 array and compare its capacitance value obtained from Q3D with the corresponding capacitance values obtained using scaling equation. That is done to show that this equation helps the algorithm to capture the effects of dimension scaling with larger TSV arrays in high accuracy.

4.1 Scaling equation

As discussed previously, a scaling equation or relation is needed to capture the variation in the capacitances values with different dimensions. In order to find the equation that relates thecoupling capacitance with physical parameters of the TSV a closer look to the physical structure is done. A TSV is composed of a conductor surrounded by dielectric and it is coupled with another TSV which is another conductor surrounded by dielectric both dipped in a semiconductor material (silicon). As TSV plays the role of an interconnect and its technology is very close to wires, then it is expected to have an equation or relation that is very close to the equation of coupling capacitance exists between two wires (two conductors). Therefore, the equation mentioned in [31], that gives the coupling capacitance between two wires, can give the indication of how the relation looks like. For two wires that is shown in Figure 4-1a with radius (a) and separated by distance (d) the coupling capacitance per unit length is given in equation (6). From equation (6) it can be found that Cc is inversely proportional with logarithmic of pitch (d) and directly proportional with logarithmic of radius (a). That also is noticed by using Q3D Extractor to find the coupling capacitance with varying dimensions of TSV bundle (pitch (p_{tsv}), radius (r_{tsv}), dielectric thickness (t_{ox}) and length (l_{tsv})) shown in Figure 4-2, Figure 4-3, Figure 4-4 and Figure 4-5 respectively. From the previously

mentioned figures it isclearthat coupling capacitance is inversely proportional with logarithmic of dielectric thickness (t_{ox}) and linearly directly proportional with length of TSV. What is shown by the simulations of Q3D go with the understanding of the physical phenomena. As pitch (S_{tsv}) increases, Cc decreases. That result because electric field lines moves from one of the conductors to the other becomes weaker with increasing the pitch and that results in lower coupling capacitance for a certain extent. Thereafter, as the pitch keep increasing similar electric field intensity is obtained, so Cc starts to saturate in a logarithmic manner. Increasing the radius means that the effective area increases so more field reaches the other conductor which mean higher capacitance. Increasing dielectric thickness means that the distance between the two conductors' increases to keep constant S_{tsv}, consequently a lower coupling capacitance is obtained. That agrees with what is known that by increasing tox, leakages to substrate is reduced which means lower coupling effects exist and higher coupling impedance.

$$C = \frac{\pi\varepsilon}{\cosh^{-1}(\frac{d}{2a})}$$

Or (6)

$$C = \frac{\pi\varepsilon}{ln(\frac{d}{a})}, \ for\ a \ll d$$

From previous discussion, it can be concluded that the relation between coupling capacitance and physical parameters of the TSV is: linear direct proportionality with length, logarithmic direct proportionality with radius of TSV, and logarithmic inverse proportionality with both t_{ox} and s_{tsv}. Relation between coupling capacitance and different physical parameters:

$$Cc\ \alpha\ \frac{L}{\cosh^{-1}\left(\frac{p_{tsv}}{2r_{tsv}}\right)}$$

For $$ptsv = s_{tsv} + 2r_{tsv} + 2t_{ox}$$

Then $$Cc\ \alpha\ \frac{L}{\cosh^{-1}\left(1+\left(\frac{s_{tsv}+2t_{ox}}{2r_{tsv}}\right)\right)} \quad (7)$$

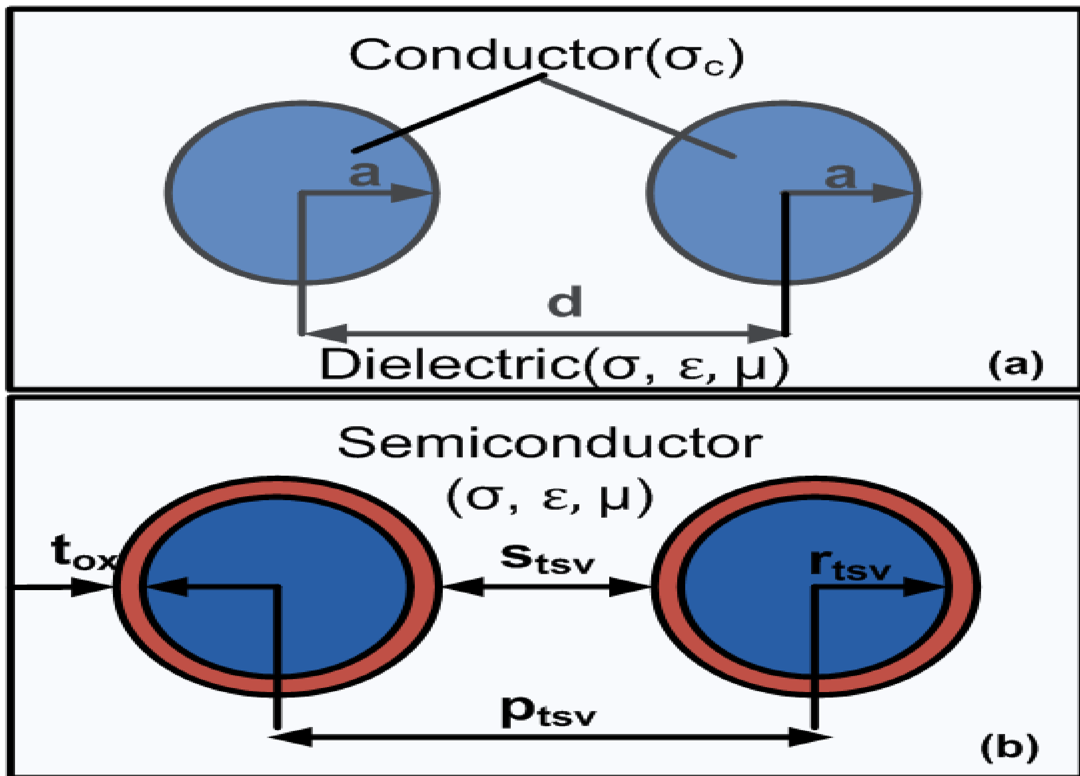


Figure4- 1a) Geometry of two wire transmission line, b) Geometry of two coupled TSVs.

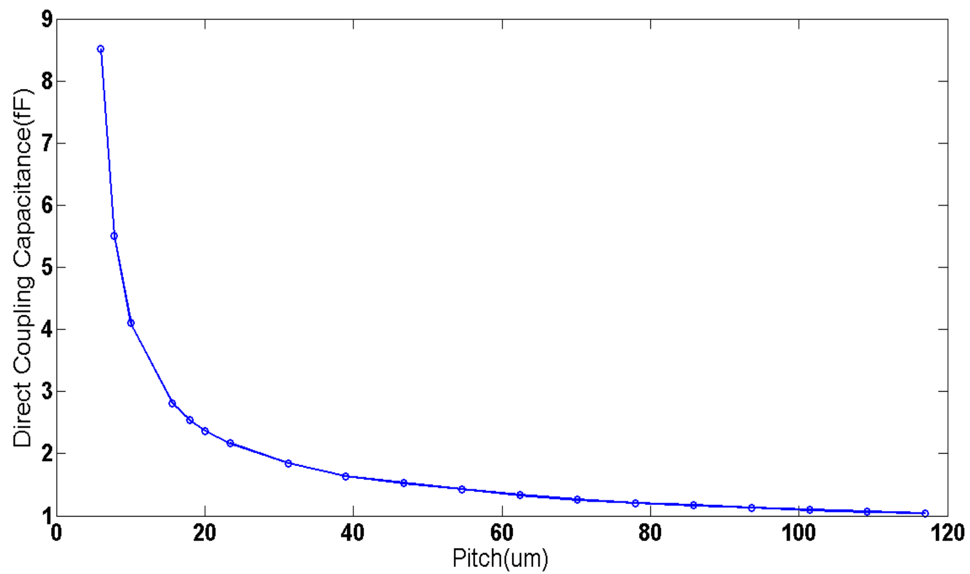


Figure4- 2 coupling capacitance variation with changing pitch.

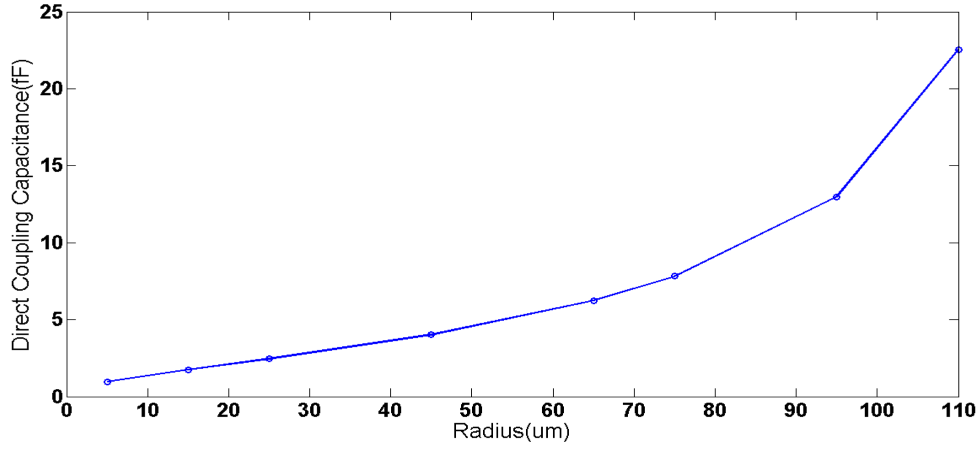


Figure4- 3 coupling capacitance variation with changing radius.

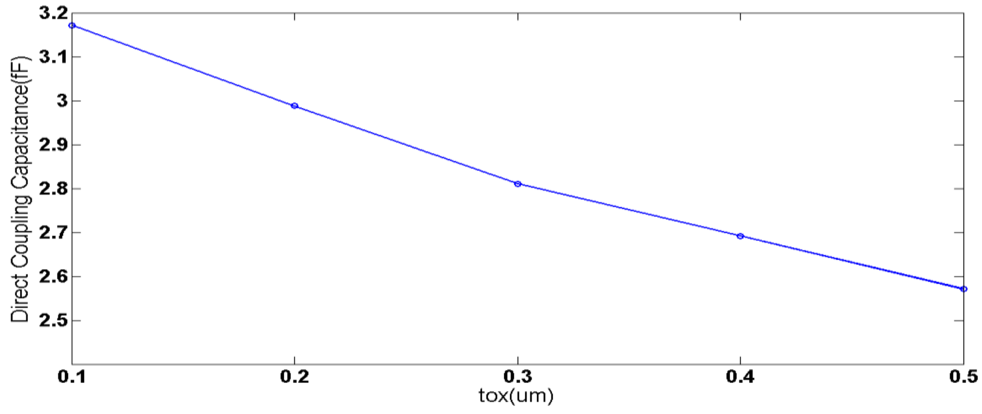


Figure4- 4 Coupling capacitance variation with changing tox.

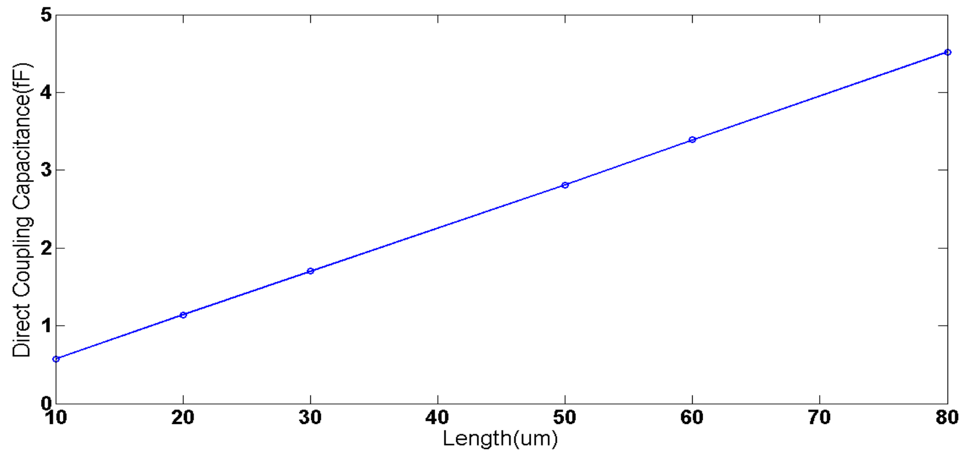


Figure4- 5Coupling capacitance variation with changing length.

For self-capacitance as it is explained in chapter 2, it has a different behavior than the case of coupling capacitance. For example, increasing pitch between TSVs means that TSVs becoming far from each other so less amount of field lines terminate from a TSV on other TSVs. That means more field lines are left free so that lead to the increase of self-capacitance with pitch and these results are proved and shown in Figure 2-8.That different behavior in self-capacitance results in a need for a new relation that catches the behavior of variation of self-capacitance with dimension scaling. But looking for the behavior of total capacitance found that it is similar to behavior of coupling capacitance. Total capacitance is sum of all coupling capacitances and self-capacitance. Therefore, value of coupling capacitances dominates over self-capacitance and that makes total capacitance has same behavior of coupling capacitance with different dimensions. That's why in this work, instead of having two relations, one for coupling capacitance and another one for self-capacitance, just (7) is used to capture variation occurs to both coupling and total capacitances as both of them have same behavior. Then self-capacitance can be calculated from total capacitance. Self-capacitance is the subtraction of all coupling capacitances between current TSV and surrounding TSVs from the total capacitance of the current TSV. More accurate results can be obtained by driving two relations, one for coupling capacitance and the other for self-capacitance.

$$C_{i,i} = C_{i,tot} - \sum_{i \neq j} C_{i,j} \tag{8}$$

Where:

$C_{i,i}$ is self-capacitance of TSV i,

$C_{i,tot}$ is total capacitance of TSV i,

$C_{i,j}$ is coupling capacitance between TSV i and TSV j.

4.2 Characterization Scenarios.

The relation proposed in equation (7) needs some coefficients in order to be capable of capturing variations in capacitances values with dimensions scaling at high accuracy. The number of used coefficients and what each of them represents depend on the used characterization criteria. Different characterization criteria are presented in Figure 3-15. Different characterization criteria are explained in the following, giving expectations for the number of coefficients needed in each technique. Thereafter, in next section characterization criteria used in this work is explained, showing the need of each added coefficients and comparing the equation results with Q3D Extractor simulations.

Characterization or scaling relation should be capable of capturing variation occurs in different capacitance types and different scaling scenarios. Capacitance types that exist in our simulation based algorithm are:

i- 1st inline coupling capacitance.
ii- Diagonal coupling capacitance.
iii- Total capacitance of the centric TSV.

Also different scaling scenarios that should be considered depending on which of the physical parameters changes from reference dimensions, changing:

i- Pitch only.
ii- radius only,
iii- dielectric thickness only,
iv-pitch & dielectric thickness together,
v- pitch & radius together,
vi-radius & dielectric thickness together,
vii- Pitch, radius & dielectric thickness all together.

Characterization criteria can be divided into two categories, characterization per structure or characterization for all structures.

a- Characterization per structure:

In this technique, characterization is done for each possible structure of the window. The number of needed coefficients depends on which option is chosen from the available options listed in Figure 3-15 and discussed below. Can be done using two methods:

i- Direct Mapping:

Finding the new capacitance value from the reference capacitance value at one step without the need to calculated any intermediate values or capacitances. Direct mapping can be applied at different scenarios:

- Direct mapping characterization for each capacitance type in each case.An optimization algorithm is applied to find suitablecoefficients that give good accuracyfor each of capacitances type variations that happen in each case. That technique is the applied technique in our work, as it is kind of exhaustive search and is expected to give better accuracy compared to other techniques. It is found that each capacitance type needs five coefficients to have a good accuracy. Consequently, total number of coefficients needed for each structure is:

$$Coeff.\,count\ per\ structure = 5(coeff.) * 3(cap.\,types) * 7(cases) = 105 Coeff.$$

$$Coeff. count\ for\ all\ struct. = 105(coeff.) * 51(possible\ struct.) = 5355Coeff.$$

- Direct mapping characterization for all capacitance types in each case.Same coefficients are used for all capacitance types but these coefficients are different in each case. Total number of coefficients needed assuming that five coefficients are enough for all capacitance types in each case:

$$Coeff. count\ per\ structure = 5(coeff.) * 1(cap. types) * 7(cases) = 35Coeff.$$

$$Coeff. count\ for\ all\ struct. = 35(coeff.) * 51(possible\ struct.) = 1785Coeff.$$

- Direct mapping characterization for each capacitance type in all scaling scenarios. There are set of coefficients for each capacitance type but these set of coefficients is applicable for all case. Optimization is done for each capacitance type separately but in all scaling scenarios the same time. Total number of coefficients needed assuming five coefficients is enough for each capacitance type in all scaling scenarios:

$$Coeff. count\ per\ structure = 5(coeff.) * 3(cap. types) * 1(cases) = 15Coeff.$$

$$Coeff. count\ for\ all\ struct. = 15(coeff.) * 51(possible\ struct.) = 765Coeff.$$

- Direct mapping characterization for all capacitance types in all scaling scenarios. Same coefficients are used for all capacitance types and these set of coefficients is applicable for all case. Optimization is done for all capacitance types in the same time and including all the scaling scenariosthe same time. Total number of coefficients needed in that case assuming number of coefficients increases to be six coefficients as there is lots of parameters that should be satisfied:

$$Coeff. count\ per\ structure = 6(coeff.) * 1(cap. types) * 1(cases) = 6Coeff.$$

$$Coeff. count\ for\ all\ struct. = 6(coeff.) * 51(possible\ struct.) = 306Coeff.$$

ii- Incremental Mapping:

As discussed in chapter 3, incremental means that new capacitance value due to dimension scaling isn't obtained at one step, but an intermediate capacitance value or more could be needed in order to get the new capacitance value. The main aim of incremental mapping is to reduce the number of scaling scenarios. Only 3 scaling scenarios are considered in incremental mapping and all other scaling scenarios can be obtained from those 3 basic scaling scenarios. These considered three scaling scenarios are: changing pitch only, changing dielectric thickness only or changing radius only. Incremental mapping can be done in different scenarios:

- Incremental mapping characterization for each capacitance type in three scaling scenarios. There are set of coefficients for each capacitance type in each of the three

scaling scenarios. Total number of coefficients needed assuming five coefficients is enough for each capacitance type in three scaling scenarios:

$$Coeff.count\ per\ structure = 5(coeff.) * 3(cap.types) * 3(cases) = 45Coeff.$$

$$Coeff.count\ for\ all\ struct. = 45(coeff.) * 51(possible\ struct.) = 2295Coeff.$$

- Incremental mapping characterization for all capacitance types in the three scaling scenarios. Same coefficients are used for all capacitance types but these coefficients are different in each of three scaling scenarios. Total number of coefficients needed assuming that five coefficients is enough for all capacitance types in each case:

$$Coeff.count\ per\ structure = 5(coeff.) * 1(cap.types) * 3(cases) = 15Coeff.$$

$$Coeff.count\ for\ all\ struct. = 15(coeff.) * 51(possible\ struct.) = 765Coeff.$$

b- Characterization for all structures

In this technique characterization is done to just one sub-structure and use optimization algorithm to find the coefficients suits that sub-structure. As capacitance value changes from window structure to another window structure, the same coefficients obtained from one sub-structure are expected to work with others. However, more error is expected using that method. Another option for characterization for all structures is to do optimization to find the coefficients for some or all possible structures at the same time. Extra programming work is needed in case of optimizing all possible structures at the same time. But it can provide better accuracy than just doing the optimization for one sub-structure. It can be done using same methods in per structure characterization: Direct mapping and incremental mapping, with the same scenarios but with much lower number of coefficients. As number of coefficients is obtained for one sub-structure and wouldn't be multiplied by number of possible structures. However number of coefficients for one sub-structure can be larger, but total number of coefficients for this kind of characterization would be much lower as shown in the following:

i- Direct Mapping:

- Direct mapping characterization for each capacitance type in each case, assuming six coefficients is enough for each capacitance type in each scaling scenarios:

$$Coeff.count\ = 6(coeff.) * 3(cap.types) * 7(cases) = 126Coeff.$$

- Direct mapping characterization for all capacitance types in each case, assuming that seven coefficients is enough for all capacitance types in each case:

$$Coeff.count\ = 8(coeff.) * 1(cap.types) * 7(cases) = 56Coeff.$$

- Direct mapping characterization for each capacitance type in all scaling scenarios, assuming ten coefficients is enough for each capacitance type in all scaling scenarios:

$$Coeff.count \ = 10(coeff.) * 3(cap.types) * 1(cases) = 30Coeff.$$

- Direct mapping characterization for all capacitance types in all scaling scenarios, assuming number of coefficients increases to be 12 coefficients as there are lots of parameters that should be satisfied:

$$Coeff.count \ = 12(coeff.) * 1(cap.types) * 1(cases) = 12Coeff.$$

ii- Incremental Mapping:

- Incremental mapping characterization for each capacitance type in three scaling scenarios, assuming six coefficients is enough for each capacitance type in three scaling scenarios:

$$Coeff.count \ = 6(coeff.) * 3(cap.types) * 3(cases) = 54Coeff.$$

- Incremental mapping characterization for all capacitance types in the three scaling scenarios, assuming that eight coefficients is enough for all capacitance types in each case:

$$Coeff.count \ = 8(coeff.) * 1(cap.types) * 3(cases) = 24Coeff.$$

In conclusion, it is expected that characterization per structure would give better accuracy than characterization for all structures. But on the other hand, characterization for all structures has much lower number of coefficients for all the scenarios. If more sophisticated optimization code is used to find the suitable coefficients, characterization for all structures at the same time can give an acceptable accuracy. More investigation and exploration for these different scenarios and options should be applied on the algorithm to compare the results obtained from these different scenarios and notice which is better scenario. That is left for future work. As mentioned in this work, the applied characterization technique is characterization per structure using direct mapping technique where coefficients were found for each capacitance type and each case. This approach is expected to give the highest accuracy among other scenarios. But still all other options should be implemented and then comparison would be fair enough.

4.3 Equation Coefficients

This section describes the use of each of coefficient in the equation, and show why the equation ended up with five coefficients to capture the variation in the coupling

capacitance accurately. The optimization algorithm used to get the coefficients is presented.

4.3.1 Coefficients Usage

In order to make equation (7) captures the variations occur to capacitance value with varying dimensions, some coefficients is needed and multiplied by parameters inside the equation, in order to help increasing the accuracy of scaling equation. In the following the task of each coefficient is described giving reasons of adding each of the coefficients shown inequation (10).

$$\mathbf{Cc}\ \alpha\ \frac{\mathbf{L}}{\cosh^{-1}\left(\alpha_1+\left(\frac{\alpha_2 \mathbf{stsv}+\alpha_3 \mathbf{tox}}{\alpha_4 \mathbf{rtsv}}\right)\right)} \tag{9}$$

The relation given in equation (9) can be used to find new capacitance value resulted from varying the dimensions with the aid of equation (10).

$$\mathbf{Cc_{new}} = \alpha_5 * \mathbf{Cc_{old}} * \frac{\cosh^{-1}\left(\alpha_1+\left(\frac{\alpha_2 \mathbf{Stsv_{old}}+\alpha_3 \mathbf{tox_{old}}}{\alpha_4 \mathbf{rtsv_{old}}}\right)\right)}{\cosh^{-1}\left(\alpha_1+\left(\frac{\alpha_2 \mathbf{Stsv_{new}}+\alpha_3 \mathbf{tox_{new}}}{\alpha_4 \mathbf{rtsv_{new}}}\right)\right)} \tag{10}$$

Where,

$Stsv_{old}$, tox_{old}, $rtsv_{old}$: are pitch, dielectric thickness and radius reference dimensions where library is built at.

$Stsv_{new}$, tox_{new}, $rtsv_{new}$: are pitch, dielectric thickness and radius actual dimensions of the given structure.

Ccold: capacitance value obtained at reference dimensions and saved in library.

Ccnew: new captured capacitance value that results due to changing the dimensions of the given structure from reference dimensions.

The relation can be rewritten to be as in equation (12) by using equation (11), where instead of having the dependency on stsv (distance between edges of dielectric of surrounding one TSV to the edge of the dielectric surrounding the next TSV). It is going to depend on p_{tsv} (distance between centers of TSV to center of the other TSV). The relations between different coefficients alphas (α) and betas (β) are given in equation (13).

$$\boldsymbol{ptsv = stsv + 2rtsv + 2tox} \tag{11}$$

$$\mathbf{Cc}\ \alpha\ \frac{\mathbf{L}}{\cosh^{-1}\left(\beta 1+\left(\frac{\beta 2*ptsv+\beta 3*tox}{\beta 4*rtsv}\right)\right)} \tag{12}$$

$$\beta 1=\alpha 1-\frac{2*\alpha 2}{\alpha 4}$$

$$\beta 2=\alpha 2,\qquad \beta 3=\alpha 3-2*\alpha 2 \tag{13}$$

$$\beta 4=\alpha 4,\qquad \beta 5=\alpha 5$$

The main purpose of multiplying a coefficient by anequation variable (dimension) is to make that variable behavior dominating in the equation, therefore capacitance value changes according to the variations in that variable. The considered range for each of these variables while doing characterization is an important aspect and the resulted coefficients value depends on that range.In our work the considered ranges are: for stsv (15 um to 95um), for rtsv (2um to 10um) and for tox (0.1um to 0.5um). As noticed that stsv values are mostly an order of magnitude larger than radius and nearly two orders of magnitude larger than tox values. Therefore, without any coefficients the value of stsv is dominating in the equation. As a result, the two coefficients α_3 and α_4 are multiplied by t_{ox} and r_{tsv} respectively in order to capture variations occurs due to varying any of these parameters by enlarging both of these parameters using the multiplied coefficients. That meansvalues of α_3 and α_4 are mostly large, especially in case of varying any of t_{ox} or rtsv. That's why at the reference value it is important to reduce the effect of s_{tsv} on the equation so that effect of varying both of toxand rtsv dominates the equation. Moreover, when only radius is changing reduction of stsv would give better accuracy. Consequently, another extra coefficient is needed in that case which is α_2. As the added 1 in argument of $\cosh^{-1}$ shown in equation (7) is from $(2r_{tsv}/2r_{tsv})$, consequently when varying radius, or radius and t_{ox} keeping pitch constant it's important to have another coefficient α_1 that helps in making rtsv in the denominator of $\cosh^{-1}$ dominates in the equation and effective. Therefore, values of both coefficients α_1 andα_2 are always ≤ 1, as α_2 reduces the dominating effect of s_{tsv} and α_1 enlarge the effect of rtsv in the denominator of $\cosh^{-1}$. In case of changing only one parameter the variations that happen to capacitance from reference isn't very large, consequently the error would be small. While in case of varying two or more parameters at the same time, the division of old to new parameters as shown in equation (10) results in a fixed error over all dimensions. As a result, coefficient α_5 can be used in order to shift all the values to overcome that fixed error and increase the accuracy. That's why α_5 ranges from (0.97 to 1.05) where 0.97 means that results obtained from relation is always larger than these obtained from Q3D simulation

by 3% so when multiplied by 0.97 these 3% is reduced and that add up to the accuracy of the equation.

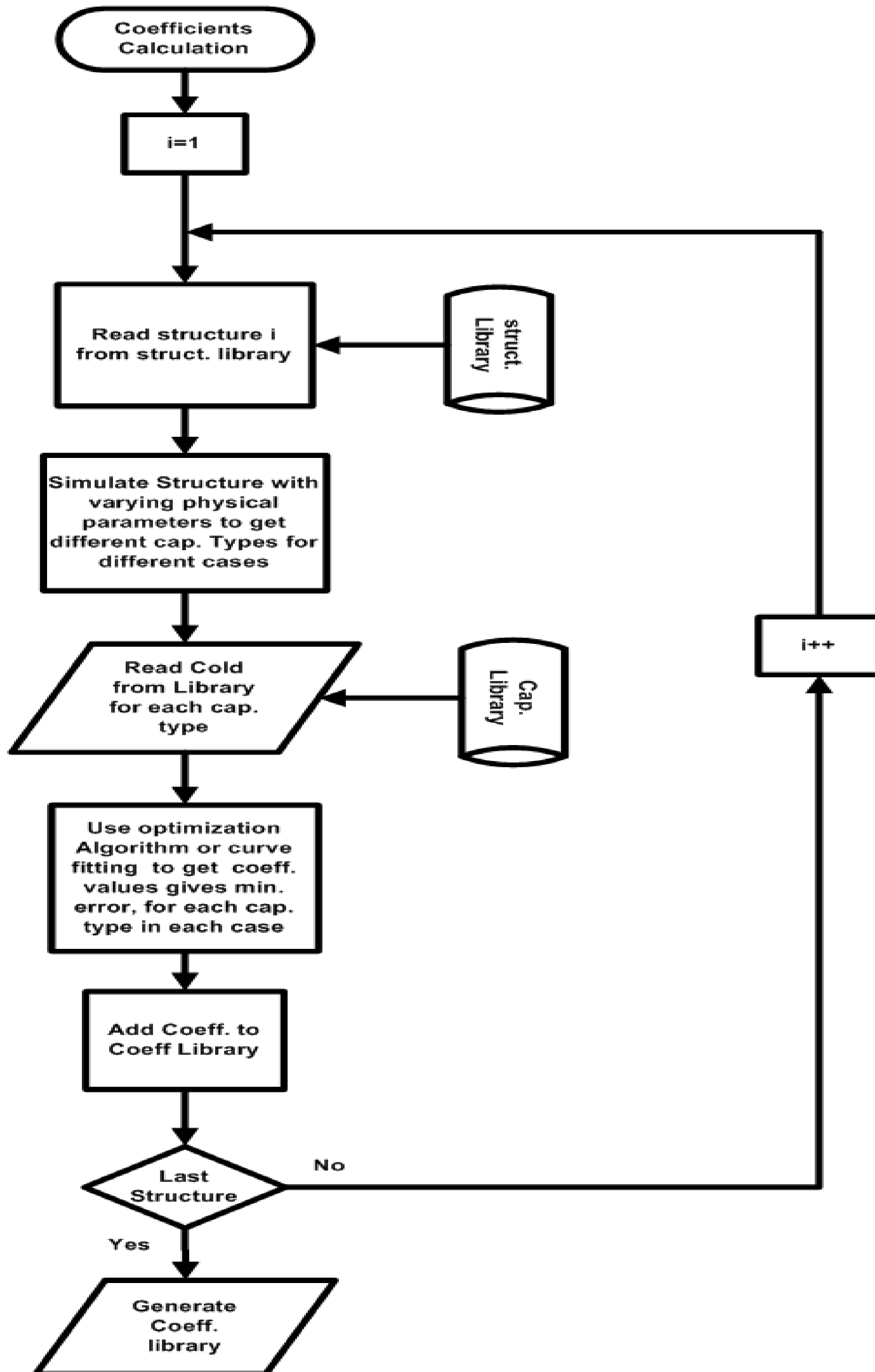


Figure4- 6 Flowchart of building coefficients library.

4.3.2 Coefficients Calculation

As mentioned above that there are 5 coefficients that needs to be obtained for each capacitance type in each of the seven scaling scenarios and that is required for each sub-structure. Figure4-6 shows a flowchart of the steps that is done to obtain the coefficients for each capacitance type in each case. First, the first sub-structure in all possible structures library is read. Using Q3D extractor, parametric sweep simulations are done to that sub-structure for the seven scaling scenarios. The range of varying the structure dimension in each case is as mentioned in section4.3.1. Each simulation run gives all capacitance types, so there is no simulation for each capacitance type. But there is a parametric sweep simulation for each case. Thereafter, reference capacitance value for each capacitance type is obtained from capacitance library in order to be used in the scaling equation. Subsequently, a corresponding value for the capacitance values obtained from Q3D for each capacitance type in each case is obtained using the scaling equation. At that point two matrices are available one contains capacitance values from Q3D and the other contains capacitance values from scaling equation. Therefore, an error percentage can be calculated between Q3D values and the corresponding equation values and just by tuning the coefficients using any technique or algorithm, the equation values changes and so the percentage error. Finally, the optimization algorithm gives out the coefficient that returned the minimum error. Then these coefficients are added to coefficients library. Thereafter, check if last sub-structure is reached or not. If not, then it takes next sub-structure in order from structures library and does same process to obtain its coefficients. If yes, that means all the coefficients is obtained and coefficients library is build and is generated to be used in algorithm to build the macro-model.

In our work a simple optimization technique is used to find the coefficients that give minimum error. The implemented algorithm is an algorithm that tries different values for each coefficient in a range determined for each of these coefficients. That range is determined by our knowledge of the use of each coefficient. Subsequently, algorithm save values of coefficients together that gives minimum error. The optimization goal is an important parameter to be determined. There are different options for the optimization goal:

i- Adding all the errors and find the coefficients that gives the minimum sum of errors.
ii- Find the maximum error (max_error) occurs in all iterations and find the coefficients values that give the minimum (max_error) among all the iterations.That gives better accuracy as the optimization is done to reduce the (max_error) occurs. That method is the implemented one in our work as it is expected to give better accuracy.

Also a more sophisticated algorithm can be used and other search techniques that can give better accuracy like the non-deterministic heuristic “genetic algorithm” which is a powerful non deterministic heuristic, but that is left for the future work.

4.4 Characterization Results

In this section result of characterizing one chosen sub-structure of a $3x3$ window sub-structure is presented. Results are presented to show how equation (10) captures the capacitance variations with changing dimensions at high accuracy for different capacitance types in different scaling scenarios using direct mapping technique. Moreover, results for using equation (10) in a larger structure $9x9$ array of TSVs contains 71 TSVs are presented. These results are presented to show that equation (10) can be used in the algorithm to build the macro-model as the window isn't the main purpose. On the other hand, having a larger structure and calculating its capacitance value with different dimensions is one of the main goals of having equation (10). The reference dimensions considered in this work are: p_{tsv}=30.6um, s_{tsv}=25um, r_{tsv}=2.5um, t_{ox}=0.3um and l_{tsv}=50um.

4.4.1 3x3 Window Results

In this work characterization for different structures of a $3x3$ window is done to find the suitable coefficients for each capacitance type in each case. But results of just one sub-structure are shown here because of the space limit. The chosen sub-structure is a full matrix of a $3x3$ window as it is expected to be the most repeated window in dense structures.

4.4.1.1 Changing Length

As discussed before and shown in equation (9), the capacitance value is linearly directly proportional with length of TSV. After varying the length of TSVs in the full matrix 3x3 window structure and comparing the different capacitance types obtained using equation (14) with the corresponding capacitance obtained using Q3D simulations as shown in Figure4-7.The results shows that the error results from capacitance mapping due to changing the length is negligible and that is the main reason for just considering variations of just three parameters (pitch, radius and tox) considering different combinations between them. When length vary, a pre-step for calculating the capacitance according to dimension scaling, is to calculate the capacitance due to variation in length of TSV using equation (14) with negligible error (about 0.6%). Then consider variations occur to other dimensions.

$$\mathbf{Cc_{new}} = \mathbf{Cc_{old}} * \frac{\mathbf{L_{new}}}{\mathbf{L_{old}}} \tag{14}$$

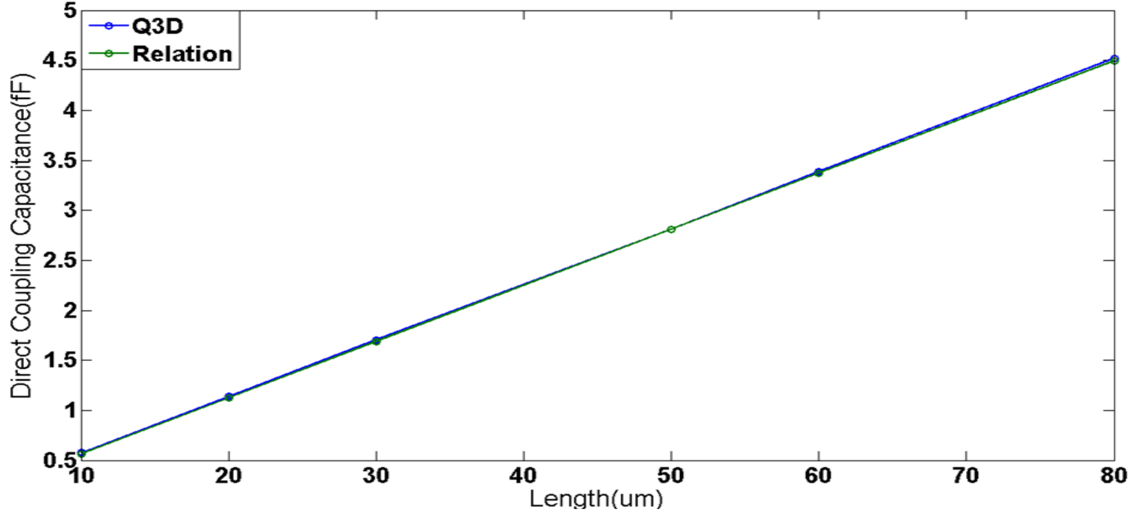


Figure4- 7 Direct coupling capacitance between (TSV5 and TSV2) in a 3x3 full matrix window structure with varying length using Q3D and relation equation.

4.4.1.2 Changing pitch only

The 3*x*3 full matrix sub-structure is simulated different times at different pitch (s_{tsv}) for the range mentioned in section 4.3 while all other parameters are kept constant at reference dimensions. Optimization algorithm is used to find coefficients for different capacitance types, where algorithm optimizes for percentage error that occurs between Q3D simulations and equation (15). A maximum percentage error of 1% occurs with varying pitch only and results in direct coupling capacitance at certain dimensions.While for other dimensions and other capacitance types error is less than 0.1% as shown in Figure4-8 which compares Q3D results of total capacitance value of TSV5 with equation (15).

$$\mathbf{Cc_{new} = \alpha_5 Cc_{old} * \frac{\cosh^{-1}\left(\alpha_1 + \left(\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}\right)\right)}{\cosh^{-1}\left(\alpha_1 + \left(\frac{\alpha_2 Stsv_{new} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}\right)\right)}} \quad (15)$$

4.4.1.3 Changing Radius Only

Similarly, simulations for 3*x*3 full matrix sub-structure is done for different radius values in the range mentioned in section 4.3, while keeping other dimensions at the reference values. Thereafter, optimization algorithm is used to find suitable coefficient for all capacitance types in that case. The algorithm optimize for the percentage error that occurs between Q3D simulations and equation (16). A maximum error of 4% is obtained at certain dimensions, while an average error of 1.5% occurs in most of dimensions. Comparison of direct coupling capacitance values (between TSV5 and TSV2) obtained from both Q3D simulations and equation (16) is shown in Figure 4-9.

$$Cc_{new} = \alpha_5 Cc_{old} * \frac{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}))}{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{new}}))} \quad (16)$$

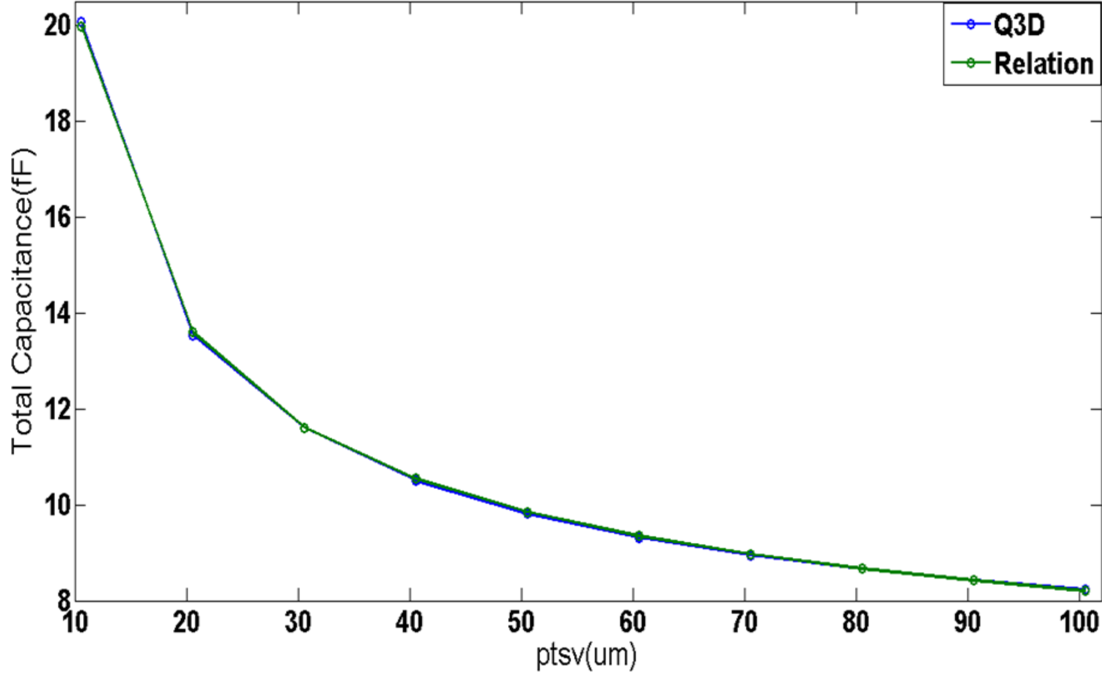


Figure4- 8Total capacitance of centric TSV in a 3x3 full matrix window structure with varying pitch using Q3D and relation equation.

4.4.1.4 Changing Dielectric Thickness Only

Similarly, simulations for 3*x*3 full matrix sub-structure is done for different dielectric thickness values in the range mentioned in section 4.3, while keeping other dimensions at the reference values. Then optimization algorithm is used to find suitable coefficient for all capacitance types in that case. Also the algorithm optimizes for the percentage error that occurs between Q3D simulations and equation (17), a negligible error (0.004%) is obtained at all toxdimension for all t_{ox} range. Comparison of direct coupling capacitance values (between TSV5 and TSV2) obtained from both Q3D simulations and equation (17) is shown in Figure 4-10.

$$Cc_{new} = \alpha_5 Cc_{old} * \frac{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}))}{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{new}}{\alpha_4 rtsv_{old}}))} \quad (17)$$

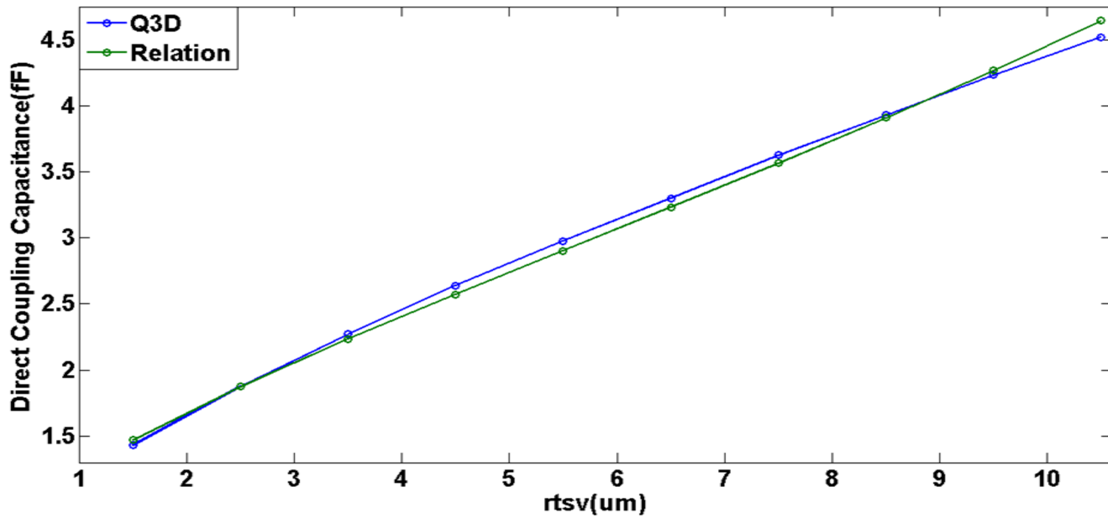


Figure4- 9Direct coupling capacitance between (TSV5 and TSV2) in a 3x3 full matrix window structure with varying radius using Q3D and relation equation.

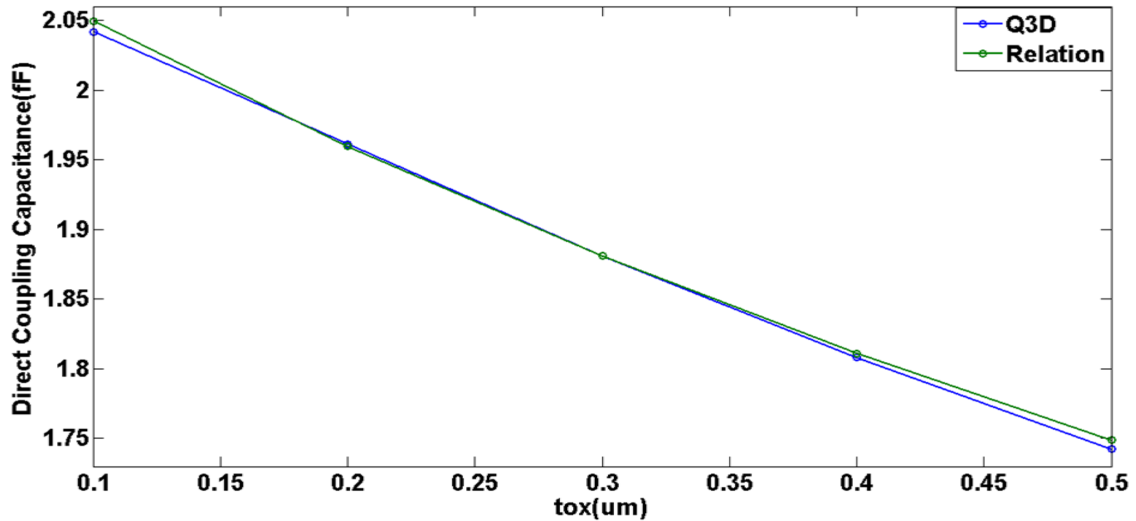


Figure4- 10Direct coupling capacitance between (TSV5 and TSV2) in a 3x3 full matrix window structure with varying tox using Q3D and relation equation.

4.4.1.5 Changing Both Pitch and Dielectric Thickness Only

Two parameters changes at the same time which are s_{tsv} and t_{ox} while keeping both ltsv and r_{tsv} at the reference dimensions. In case of two parameters changes there is more simulation cases and more capacitance values obtained from Q3D. Subsequently, optimization algorithm is used to find suitable coefficient for all capacitance types in that case. The algorithm optimize for the percentage error that occurs between Q3D

simulations and equation (18). A maximum error of 4% resulted at certain dimensions, while an average error of 2% occurs in most of dimensions. Comparison of total capacitance value of TSV 5 obtained from both Q3D simulations and equation (18) is shown in Figure 4-11.

$$\mathbf{Cc_{new}} = \alpha_5 \mathbf{Cc_{old}} * \frac{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}))}{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{new} + \alpha_3 tox_{new}}{\alpha_4 rtsv_{old}}))} \quad (18)$$

4.4.1.6 Changing Both Pitch and Radius Only

Two parameters changes at the same time which are stsv and rtsv while keeping both ltsv and tox at the reference dimensions. Then optimization algorithm is used to find suitable coefficient for all capacitance types in that case. The algorithm optimize for the percentage error that occurs between Q3D simulations and equation (19). A maximum error of 6% resulted at certain dimensions, while an average error of 3.5% occurs in most of dimensions. Comparison of diagonal coupling capacitance (between TSV5 and TSV1) values obtained from both Q3D simulations and equation (19) is shown in Figure 4-12.

$$\mathbf{Cc_{new}} = \alpha_5 \mathbf{Cc_{old}} * \frac{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}))}{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{new} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{new}}))} \quad (19)$$

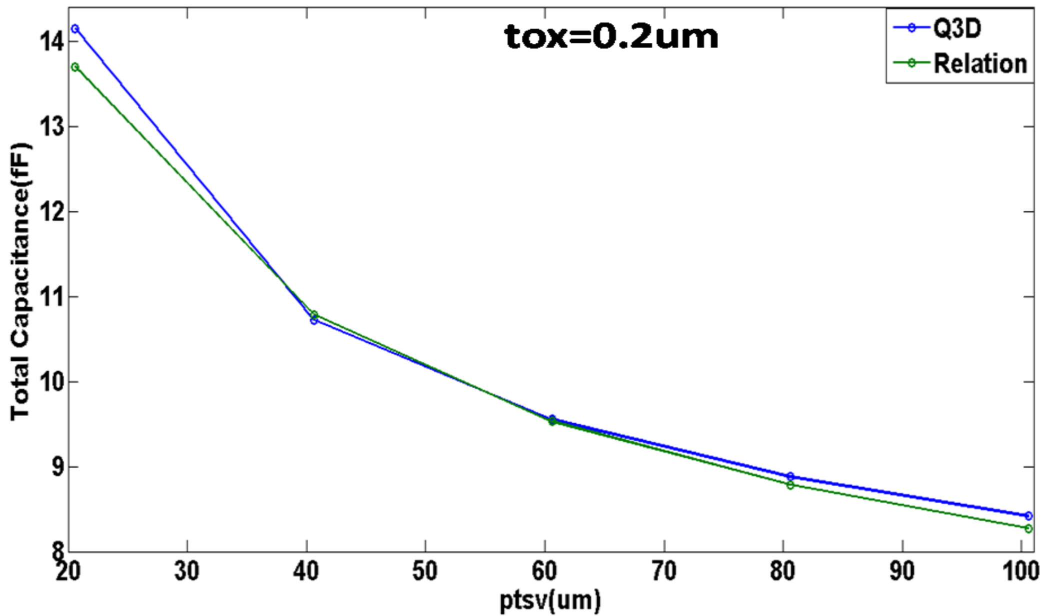


Figure4-11Total capacitance of centric TSV in a 3x3 full matrix window structure with varying both stsv and tox using Q3D and relation equation.

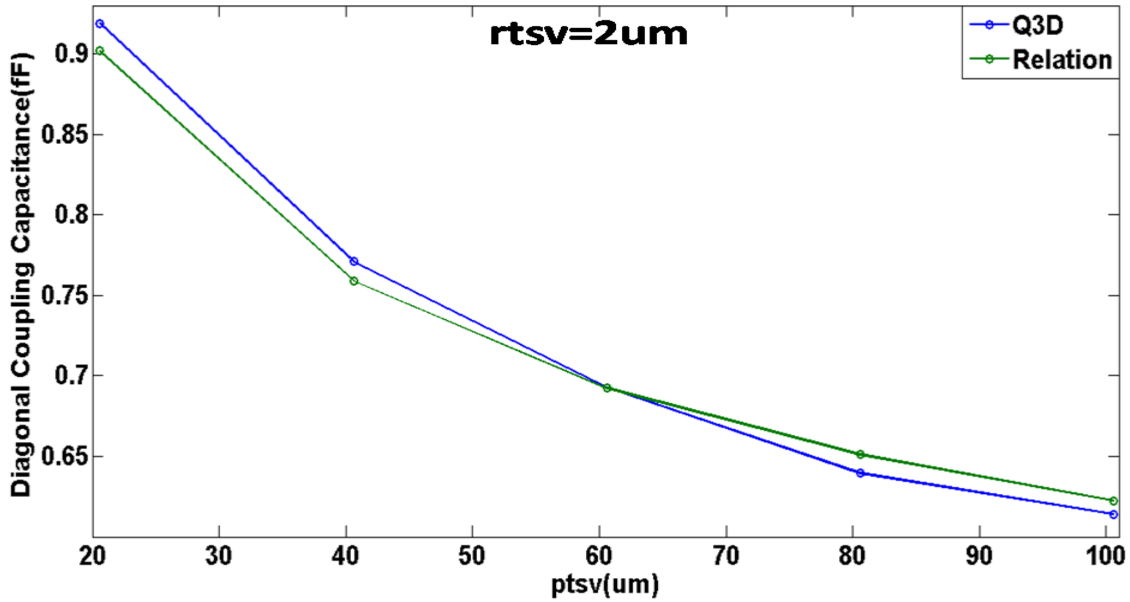


Figure 4-12 Diagonal coupling capacitances between (TSV5 and TSV1) in a 3x3 full matrix window structure with varying both stsv and rtsv using Q3D and relation equation.

4.4.1.7 Changing Both Dielectric Thickness and Radius Only

Two parameters changes at the same time which are t_{ox} and r_{tsv} while keeping both ltsv and s_{tsv} at the reference dimensions. Thereafter, optimization algorithm is used to find suitable coefficient for all capacitance types in that case. The algorithm optimize for the percentage error that occurs between Q3D simulations and equation (20). A maximum error of 5.5% resulted at certain dimensions; while an average error of 2.5% occurs in most of dimensions. Comparison of total capacitance values of TSV5 obtained from both Q3D simulations and equation (20) is shown in Figure 4-13.

$$Cc_{new} = \alpha_5 Cc_{old} * \frac{\cosh^{-1}\left(\alpha_1 + \left(\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}\right)\right)}{\cosh^{-1}\left(\alpha_1 + \left(\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{new}}{\alpha_4 rtsv_{new}}\right)\right)} \quad (20)$$

4.4.1.8 Changing pitch, Dielectric Thickness and Radius

Three parameters changes at the same time which are s_{tsv}, t_{ox} and r_{tsv}. Subsequently, optimization algorithm is used to find suitable coefficient for all capacitance types in that case. The algorithm optimize for the percentage error that occurs between Q3D simulations and equation (20). A maximum error of 9.5% resulted at certain dimensions; while an average error of 4% occurs in most of dimensions. Comparison of total capacitance values of TSV5 obtained from both Q3D simulations and equation (21) is shown in Figure 4-14.

$$Cc_{new} = \alpha_5 Cc_{old} * \frac{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{old} + \alpha_3 tox_{old}}{\alpha_4 rtsv_{old}}))}{\cosh^{-1}(\alpha_1 + (\frac{\alpha_2 Stsv_{new} + \alpha_3 tox_{new}}{\alpha_4 rtsv_{new}}))} \quad (21)$$

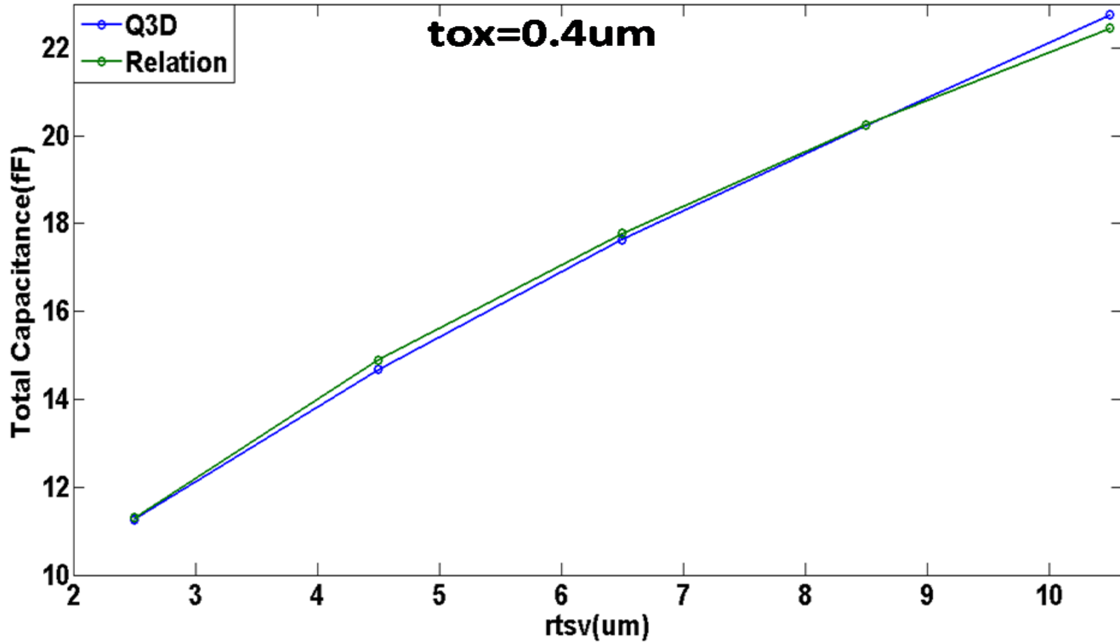


Figure 4-13 Total capacitance of centric TSV in a 3x3 full matrix window structure with varying both rtsv and tox using Q3D and relation equation.

In conclusion, all the previous simulations and optimizations to get the coefficients for each of capacitance types in each case are done to all the possible structures of a 3x3 window size. A maximum error of 10% occurs at few dimensions for all possible structures and all capacitance types in all scaling scenarios. This 10% error mostly happens when all of the parameters (pitch, radius and tox) changes at the same time.The total average error of all possible structures and all capacitance types in all scaling scenarios are 3.5 %. It is also important to note that not all the calculated error is positive error (where estimated capacitance is larger than actual capacitance) but in some cases the resulted error is negative error (where estimated capacitance is smaller than actual capacitance). Therefore, the error occurs by mapping of capacitance due to dimension scaling wouldn't always add to the algorithm estimation error, but it can increase the accuracy of the estimated results. When a negative error exists that means the estimated capacitance by the algorithm is lower than the capacitance value of a 3x3 sub-structure at these dimensions. That would be closer to the actual value of that capacitance in a larger structure (more shielded) in case that algorithm over estimated capacitance value causing a positive error. Consequently, positive error of algorithm would be canceled by negative error resulted from using scaling equation.

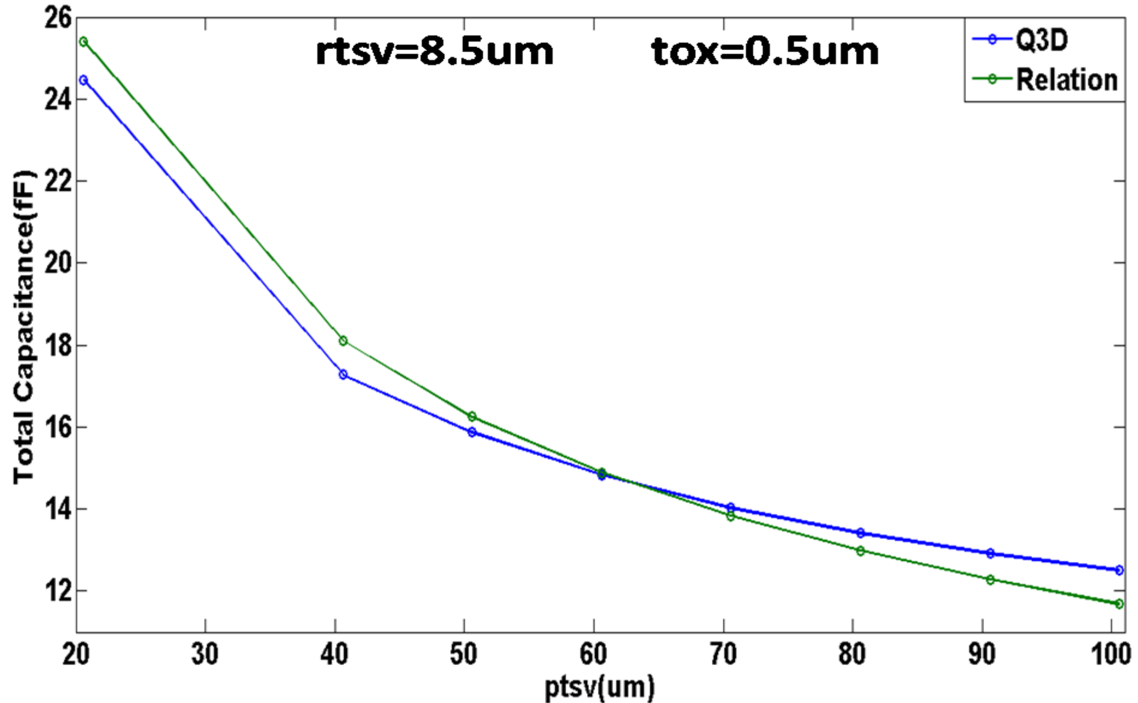


Figure 4-14Total capacitance of centric TSV in a 3x3 full matrix window structure with varying stsv,rtsv and tox using Q3D and relation equation.

In general, there are two sources of error in the final generated solution: algorithm error and scaling equation usage error. Each of them can be positive or negative error as explained in the following:

a- Algorithm error:

Occurs due to using the algorithm, where in the proposed algorithm a window of size 3x3 is used and from that window capacitance is calculated. That window is with limited size which is much smaller than the given array. Therefore, extra surrounding TSVs that make shielding for electric field lines between TSVs could exist and couldn't be captured inside the window. That results in error in the calculated capacitance value. This kind of error can be found by applying the algorithm at reference dimensions, where scaling equation isn't needed so the resulted error is only an algorithm error. It can be classified into:

i- Negative error:

Value estimated from algorithm at reference dimensions is less than value resulted from Q3D simulation. It only occurs in total capacitance values as a result of neglecting lots of capacitances in the algorithm, some of these capacitances have relatively large values. It occurs in TSVs exist in sparse substructures.

ii- Positive error:

Value estimated from algorithm at reference dimensions is larger than value obtained from Q3D simulation. It occurs in all capacitance types, where all estimated coupling capacitances from the algorithm is going to be larger than or equal to actual capacitance value. In addition, it occurs in total capacitance values where over estimation in capacitance value from window results in larger total capacitance value than the actual value. For total capacitance, it occurs in TSVs exist in dense substructures.

b- Scaling error:

Occurs due to using the scaling equation, where dimensions of the given TSV array structure vary from reference dimensions. This kind of error can be negative error or positive error:

iii- Negative error:

Value resulted from scaling equation is less than value resulted from Q3D simulation. That kind of error can improve accuracy of calculated capacitance using algorithm. The improvement can be obtained in dense substructures, as negative error reducesthe over estimation occurs by the algorithm for capacitance values. That reduces total accumulative error resulted from both algorithm and then usage of scaling equation.

iv-Positive error:

Value resulted from scaling equation is larger than value resulted from Q3D simulation.In case of positive algorithm error occurs in dense substructures, that kind of error is added to algorithm error results in larger error in the final calculated capacitance. But positive error can increase accuracy in sparse substructures. Where over estimation of capacitance value compensate the neglected capacitances by the algorithm and that cancels negative error occurs in total capacitances of TSVs in sparse substructures result in reducing total accumulative error.

4.4.2 9x9 Structure Results

The previous presented results are for 3x3 structures where it is the window used in the algorithm. But to be sure that the technique can give good results for larger structures, a test case of a dense structure contains 71 TSVs shown in Figure 4-15 is considered. That test structureis simulated using Q3D for different scaling scenarios at different dimension then the algorithm is used to find the capacitance matrix using the scaling equation at same dimensions used in Q3D simulations. A TSV which is totally shielded (TSV 71), and when the window reaches it, the resulted window is full matrix window structure, is chosen to get its total capacitance obtained from both Q3D simulation and also from

algorithm. Subsequently, calculate the resulted error. A fully shielding TSV is chosen because the results presented in the previous section are for the full matrix window. The reason to just compare the total capacitance is that it is the summation of all coupling and self-capacitance of the TSV of interest so it considered as the cumulative error of both coupling and self-capacitances. Total capacitance can give a good intuition for error resulted from using the scaling equation. Total capacitance error of the chosen TSV (TSV 71) resulted from using the algorithm at reference dimension without including thescaling equation error is 0.9%. As noticed this error is a positive algorithm error as that TSV falls inside a dense substructure where capacitance values is slightly over estimated by the algorithm resulted in small positive error.

First, changing one dimension only (s_{tsv}), and comparing the results obtained from scaling equation in equation (15) with the results obtained from Q3D as presented in Figure 4-16. As presented in the previous section error that occurs from mapping in a $3x3$ sub-structure when pitch only varies, can reach 1%.In addition, another 1% error already exists due to the algorithm used. That means it is expected to have a maximum of total capacitance error from just varying pitch to be 2% or around this value. The results shown in Figure 4-16 give a maximum error of 2% which goes with the intuitively expected value for maximum error. As discussed before the effect of existence of negative error appears in the dimensions with reduced error. For example at s_{tsv}=70um, error reduced from 0.9% to 0.1% which mean a negative error of 1% occurs.That result in a final error of 0.1%, which is lower than the error obtained at reference dimensions.Therefore, using that scaling equation can improve the accuracy of the final model at certain dimensions. As the algorithm error of that TSV is a positive error, so negative error resulted from scaling equation would improve the accuracy while positive error would worsen the accuracy of the estimated capacitance. However, very large negative error would worsen the accuracy but with an opposite sign. It can be concluded that for a positive algorithm error, it is preferred to get a negative error results from scaling equation than getting a positive error in case both of those errors have the same magnitude.

Second, changing two dimensions only (s_{tsv} and t_{ox}), and comparing the results obtained from the scaling equation in equation (18) with the results obtained from Q3D as presented in Figure 4-17. It is shown in the previous section that maximum error occurs while mapping of capacitance value due to changing both s_{tsv} and t_{ox} is 4%. Consequently, a maximum of 5% error can be obtained that result from both algorithm error (1%) and scaling equation (4%). Moreover, the existence of negative error improves the accuracy of the calculated total capacitance at some dimensions as shown in Figure 4-17. It is clear that mostly the maximum error obtained from usage of scaling equation (4%) error is a negative error. That is the reason that the highest error exist in the

simulated dimensions is 3% only. In addition, that can be noticed from the value obtained from the relation (scaling equation) which is lower than the value obtained from Q3D, and that is the case of negative error occurrence.

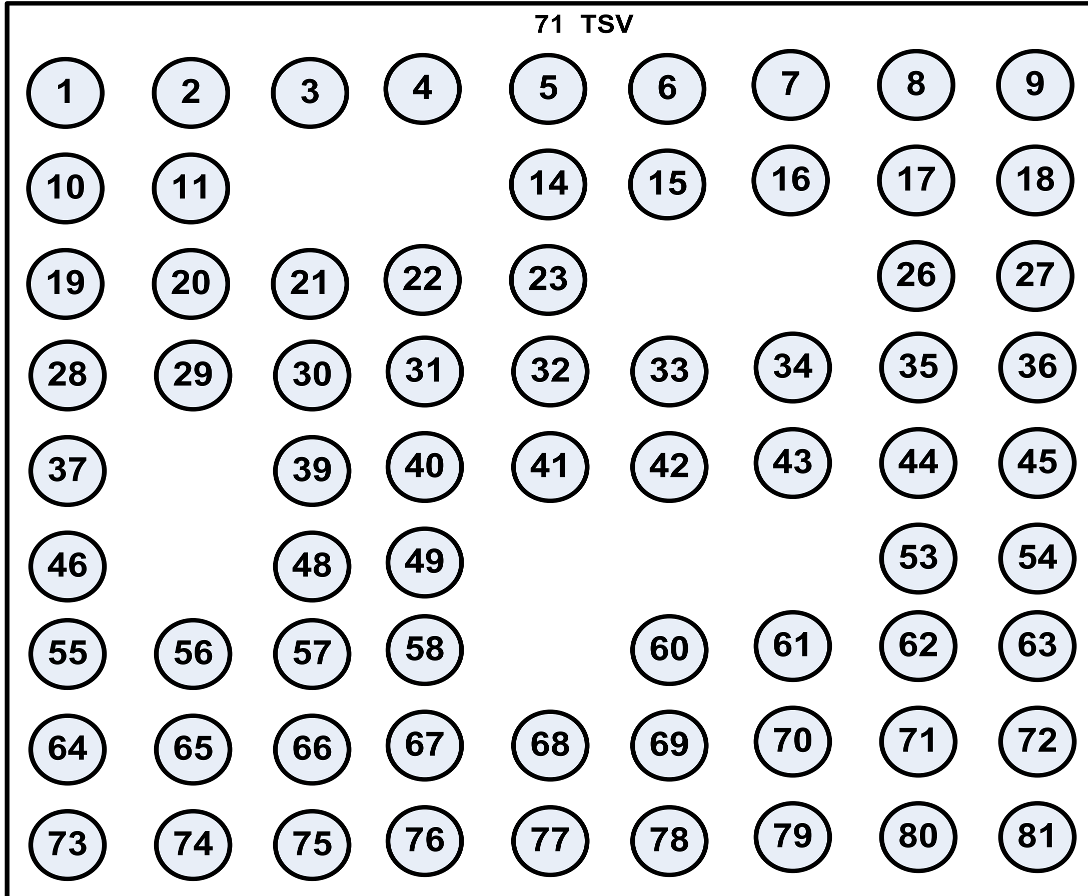


Figure4- 15 Test structure of size 9x9 contains 71 TSVs.

Third, changing three parameters at the same time (stsv, tox and rtsv), similarly, comparing the results obtained from the scaling equation in equation (21) with the results obtained from Q3D as shown in Figure 4-18. The maximum error occurs in the full matrix of size 3x3 due to using the scaling equation is found to be 10 %. As 10% is negative error, the error resulted at these dimensions in larger structure size is 9% (@ stsv=60um, tox=0.2um, rtsv=3um) and that is the maximum expected occurring error. While maximum positive error is about 7.7% which results in an error of 8.6% (@ stsv=15um, tox=0.1um, rtsv=4.5um), It is shown in Figure 4-18 that at certain dimensions the existence of negative error results in reducing the error from 0.9% to 0.5% and 0.6%.Negative error existence appears in these dimensions where the calculated capacitance value from scaling equation is lower than value extracted from Q3D simulation (ex: @ s_{tsv}=75um, t_{ox}=0.1um, r_{tsv}=6.5um).

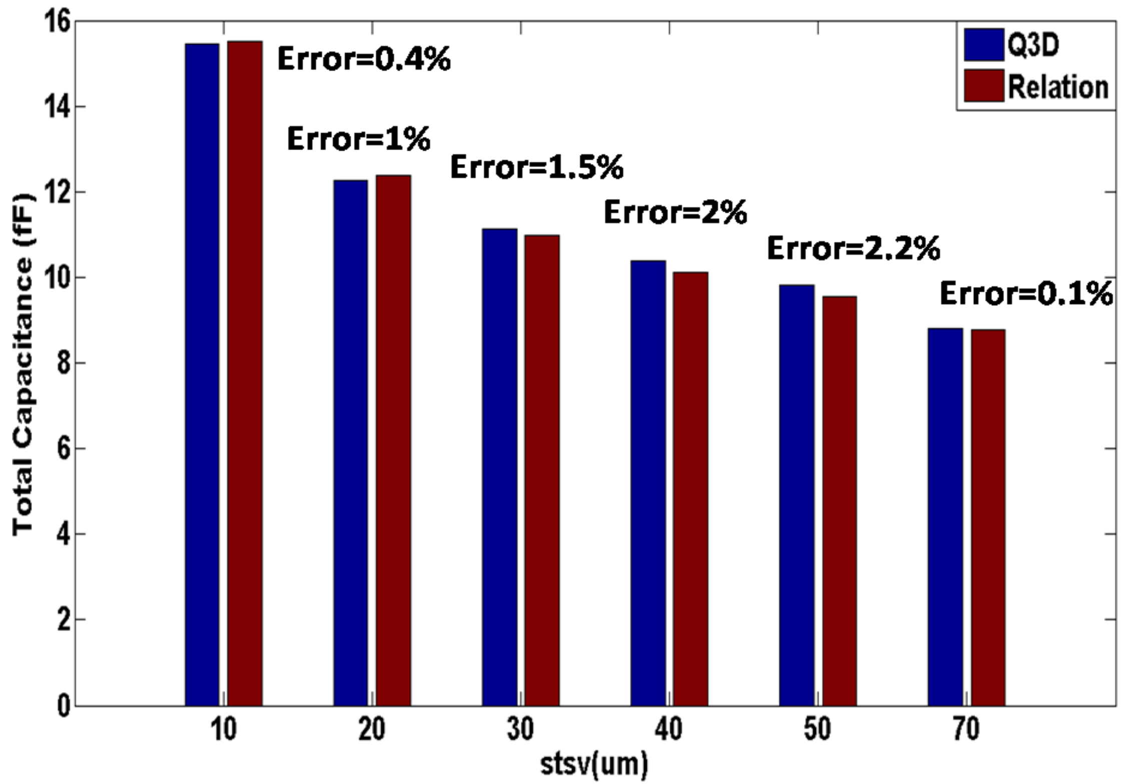


Figure4- 16 Compare of total capacitance of TSV 71 with varying pitch only obtained from both algorithm and Q3D simulations.

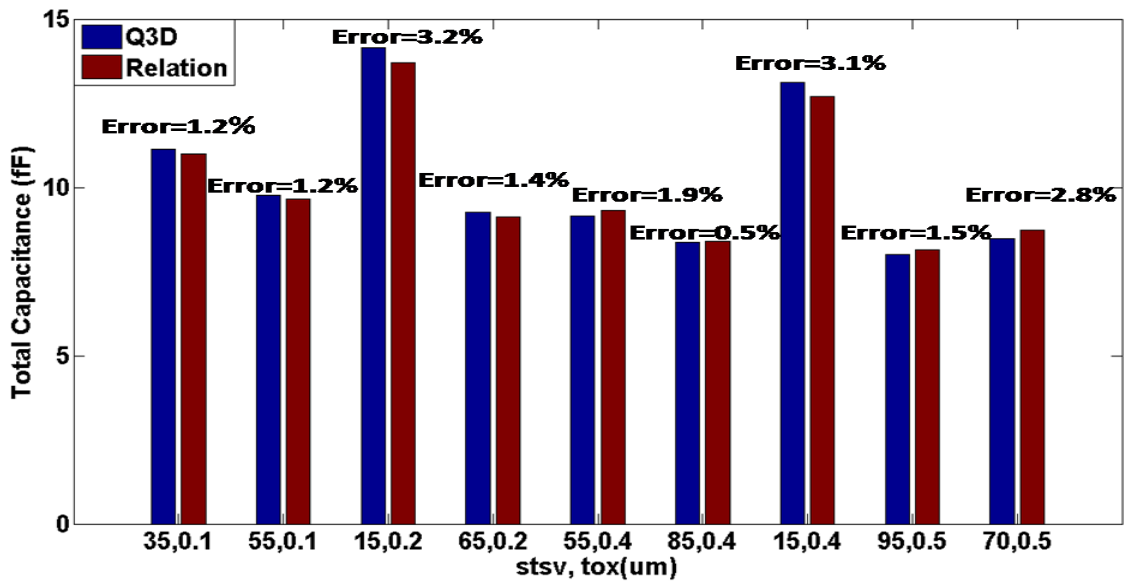


Figure4- 17Compare of total capacitance of TSV 71 with varying both pitch and tox only obtained from both algorithm and Q3D simulations.

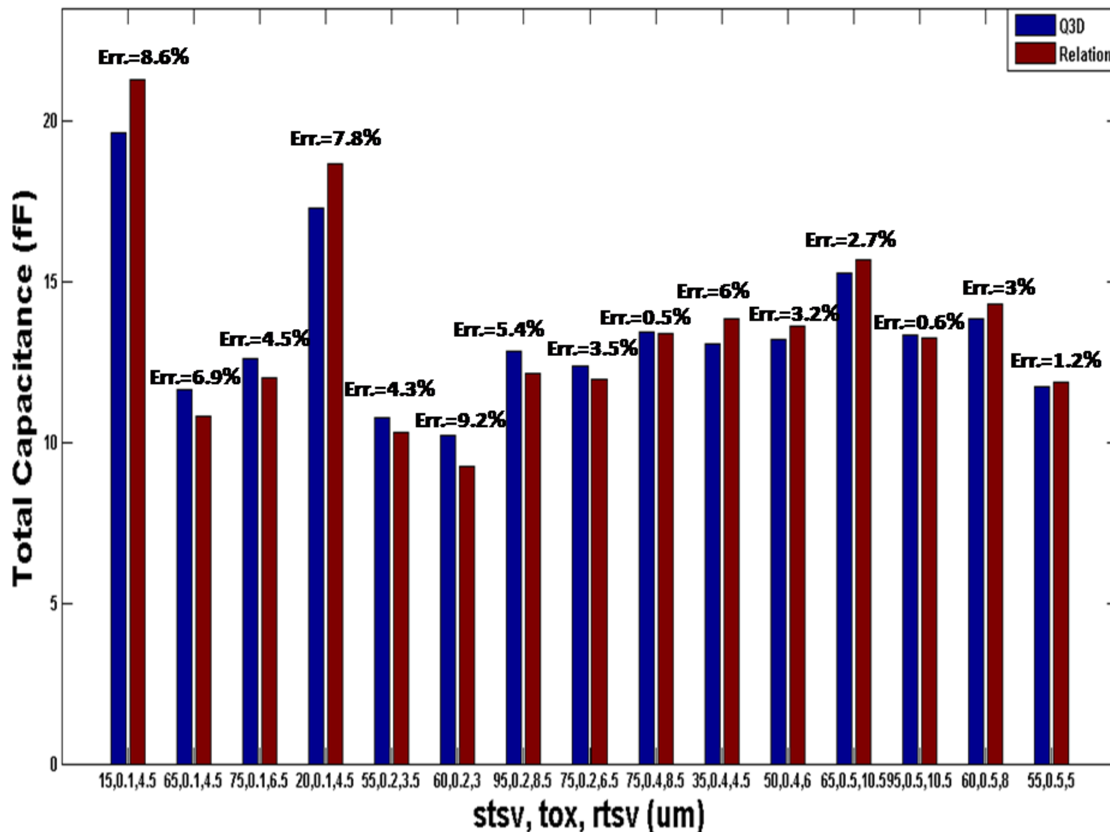


Figure4- 18Compare of total capacitance of TSV 71 with varying pitch, radius and tox only obtained from both algorithm and Q3D simulations.

From the previous discussion, it can be concluded that it is better to represent the error occurs due to mapping in the form of negative error and positive error, not the absolute of each of them. Both of these error types can add to accuracy of created macro-model in different scaling scenarios. Negative error resulted from scaling equationcan add to accuracy of the macro-model when algorithm error is positive. Total error in that case is (error from algorithm- negative error from mapping). In case of positive algorithm error, positive error results from usage of scaling equation would worsen the accuracy of the calculated capacitance. While Positive error resulted from scaling equation can add to accuracy of the macro-model when algorithm error is negative. Total error inthat case is (positive error from mapping - error from algorithm). In case of negative algorithm error, negative error results from usage of scaling equation would worsen the accuracy of the calculated capacitance.

In conclusion, the proposed scaling equation used to calculate capacitance values due to dimensional scaling is proposed in this chapter, giving the steps of implementing this scaling equation. Thereafter, different scenarios to do characterization for bundles of TSVs are proposed and the differences between each of these scenarios are discussed.

Characterization can be done per structure or for all structures at the same time and each of these categories can be done using direct mapping or incremental mapping. The main difference in each of these scenarios is the number of needed coefficients and how to obtain these coefficients. Subsequently, discussing the needed number of coefficients in the scenario of characterization used in this work and how it ended up with five coefficients for each capacitance type in each case for each structure. After that, discussing how to obtain the suitable values for each coefficient, using a suitable optimization algorithm or curve fitting. Thereafter, discussing how important to determine the optimization goal as it effects on the resulted coefficients values and the maximum error occurs from using the scaling equation. After showing results of characterization of $3x3$ window structures, and results of applying the algorithm on larger TSV array (ex: $9x9$ array size) and comparing it with results obtained from Q3D simulations. It can be concluded that it is better to do optimization while considering positive and negative error not the absolute of each of them. It is expected that in dense window structures it is better to guide the optimization algorithm to give coefficients that give maximum error to be a negative error and try to reduce the maximum positive error. Moreover, it is expected that in sparse window structures it is better to guide the optimization algorithm to give coefficients that give maximum error to be positive error and try to reduce maximum negative error. The reason is that dense window structure mostly results in positive algorithm error, while sparse window structures mostly results in negative algorithm error.

Chapter 5

Results and Algorithm Enhancements

In this chapter, different tools and techniques that can be used to verify the proposed model is discussed. In addition, detailed discussion for the metric that can be used to quantize the error produced by the macro-model is presented. Thereafter, error of each capacitance is calculated using the defined metric and discussion for results is provided. Finally some improvements for the algorithm is added in order to modify accuracy of calculating self-capacitance value of each TSV and to decrease maximum error resulted in the macro-model.

5.1 Verification Tools and Techniques

In order to have a golden reference where it can be used to build the LUT and comparing the final results obtained by the algorithm, different tools types like: device simulator or quasi-static electromagnetic wave simulator or full wave electromagnetic wave simulator, can be used as a golden reference.

A device simulator like Silvaco or Synopsys (Sdeviceor Raphael) can be used to verify the model. Mainly the device simulator can be used to extract the equivalent resistance, capacitance and inductance of a single TSV structure and coupling parameters of an array of TSVs. The extracted values of R, L and C are compared with the corresponding values calculated from the algorithm and hence accuracy of the model can be calculated using a defined metric.

Generally, device simulators can give good results with very small tool error as it works on the physical properties of materials and motion of the carriers. It focuses on the physics of devices; however, it does not consider field effects. Moreover, device simulator can be used to extract s-parameters for TSV structure and then compare it with corresponding s-parameters extracted from the model. S-parameters mainly give the attenuation effect that occurs to the signal as it moves from a TSV to another.

Regarding the electromagnetic (EM) simulators, two types of (EM) wave simulators exist which are: full wave simulator (Ansoft, HFSS) and quasi-static simulator (Ansoft, Q3D Extractor). Both can be used, but there is difference in accuracy between them. Table 6 shows a comparison between full wave and quasi static simulators; wave simulator generally produces its results by solving Maxwell’s equations. The difference between full wave and quasi-static simulators lies in conditions considered in Maxwell’s equation. For quasi-static simulator, it assumes that everything is static and then puts the velocity of the wave into consideration as it is moving, by using the equation given in equation (22). That leads to more accurate results that can be obtained from the full wave

simulators (e.g. HFSS), but it takes a much longer time than what a quasi-static simulator takes. For a design composed of a large number of TSVs it can take days to be simulated. Many works use the quasi-static simulators as it is faster depending on the small error exist atlow frequencies. However at the higher frequencies (≥ 60GHZ), full wave simulator has to be used as quasi-static wave simulator wouldn't be accurate. In our work frequency dependency of coupling parameters isn't considered and left for future work, so quasi-static EM simulator (e.g.: Q3D Extractor) can be used.

$$\boldsymbol{v} = \frac{\boldsymbol{c}}{\sqrt{\boldsymbol{\varepsilon_r}}} \tag{22}$$

When using the (EM) wave simulator, the model verifications can be done by comparing the S-parameters obtained from the wave simulator with the S-parameters obtained from the model which can be obtained using a tool like AWR-Microwave office. Since Microwave office is a quasi-static simulator, it is preferable to compare its results using a quasi-static EM wave simulator. Coupling and self-parameters of structures of TSVs can be extracted using quasi-static wave simulator and compared with the corresponding values obtained from the algorithm using the defined metric to calculate error between both values.

Table 6 COMPARISON BETWEEN DIFFERENT TYPES OF ELECTROMAGNETIC SIMULATORS. [16]

Item	Static	Quasi-Static	Full-Wave
Equations	$\nabla \times \vec{E} = 0$ $\nabla \times \vec{H} = \sigma\vec{E}$ $\nabla \cdot \varepsilon\vec{E} = \rho$ $\nabla \cdot \mu\vec{H} = 0$	$\nabla \times \vec{E} = 0$ $\nabla \times \vec{H} = \sigma\vec{E}$ $\nabla \cdot \varepsilon\vec{E} = \rho$ $\nabla \cdot \mu\vec{H} = 0$	$\nabla \times \vec{E} = -\mu\frac{\partial\vec{H}}{\partial t}$ $\nabla \times \vec{H} = -\varepsilon\frac{\partial\vec{E}}{\partial t} + \sigma \times \vec{E}$ $\nabla \cdot \varepsilon\vec{E} = \rho$ $\nabla \cdot \mu\vec{H} = 0$
Skin effects	No	Yes	Yes
Displacement current	No	No	Yes

5.2 Results

In thiswork a quasi-static electromagnetic wave simulator (i.e. Ansoft, Q3D Extractor) is used to get both coupling and self-capacitances of TSVs structures. Results from EM wave simulator can be compared to corresponding capacitance values calculated using the algorithm, then error resulted from using the algorithm can be calculated. Error is calculated between each capacitance extracted from Q3D and corresponding capacitance value obtained from the algorithm. Thereafter, a histogram can be plotted for all error values, and their number of occurrence would give a full picture of the total macro-model accuracy. Calculating error for all capacitances can help in determining the average error

and maximum error that result in the macro-model from using the algorithm. Direct calculation of error between each two corresponding capacitances resulted from both Q3D and algorithm may result in a 100%. That 100% error would occurs for capacitances neglected in the macro-model which means it has a zero value in the macro-model. However some of these neglected capacitance values are very small compared to other coupling capacitance values and total capacitance of its TSV. It still leads to 100% error using error calculation according to each capacitance value. In that case the error is meaningless as this capacitance value is very small and can be neglected without causing any troubles in the accuracy of the macro-model. Therefore, a new metric has to be defined to calculate the error between each two corresponding capacitances resulted from both Q3D and algorithm.

The proposed metric depends on how effective is each capacitance value compared to the total capacitance of the TSV. The larger the capacitance value, the more it is effective and has larger percentage in total capacitance. The proposed metric given in equation (23) calculates the error by comparing each capacitance (calculated from the model) by its Q3D counterpart (the exact value) and relate that to the total capacitance. In case the capacitance is neglected in the macro-model (has a zero value in the model) then the error would be determined according to the ratio of that capacitance from the total capacitance value. Using the proposed metric that error would be very small, in case of very small and non-effective capacitance values. Consequently, the resulted error in that case is more realistic.

$$\boldsymbol{Error} = \frac{\left(\boldsymbol{Cc_{i,jmodel}} - \boldsymbol{Cc_{i,jQ3d}}\right)}{\boldsymbol{C_i tot_{Q3D}}} \tag{23}$$

Where,
$Cc_{i,jmod}$: the coupling capacitance between TSVi and TSVj calculated from the Macro-model
$Cc_{i,jQ3D}$: the coupling capacitance between TSVi and TSVj extracted from Q3D simulation.
$C_{i\text{-}tot\text{-}Q3D}$: the total capacitance of TSVi extracted from Q3D simulation.

Total capacitance value seen at each TSV is considered as the summation of all coupling capacitances and self-capacitances of that TSV. In that case the TSV of interest (i.e. calculating total capacitance for it) is considered as signal TSVs while all other TSVs are considered to be grounded. In case of the error in calculated capacitance is in one direction (i.e. always positive or always negative) it’s acceptable to have total capacitance as summation of all coupling and self-capacitance as it is the worst case, when one TSV is signal TSV while other TSVs are grounded. Error is in one direction in case of calculating capacitance at reference dimensions, the capacitance obtained in that case is

always larger than actual capacitance value or equal to zero (always has positive error). After using scaling equation, some of the calculated capacitances values become lower than the actual value of that capacitance. That result from the existence of both positive and negative error. Therefore in that case, it is better to have two limits for the error, one for the summation of the capacitances results from negative error and the other for the summation of capacitances results from positive error.

5.2.1 Simulation at Reference Dimensions

The algorithm is used to build the macro-model and get capacitance matrix for all TSVs in the chosen test case of the 9*x*9 array structure that contains 71 TSVs shown in Figure 4-15 at reference dimensions. In that casescaling equation wouldn't be used as dimensions don't changes from reference dimensions. Q3D is used to simulate same structure in Figure 4-15 and get its capacitance matrix. Thereafter, the metric defined in (23) is used to calculate the error between each capacitance exists in capacitance matrix of Q3D and its corresponding capacitance obtained from the algorithm. A histogram for the error occurs in all capacitances is presented in Figure 5-1. As shown in Figure 5-1, most of error occurs in calculated capacitances is within the range of 0.1% to 1.9%. That is mainly because of lots of capacitance values that can be neglected as it has very small value compared to total capacitance as the test structure is dense. For rest of capacitances, mainly error occurs in range of 3% to 5.5% and very few capacitances have an error greater than 6%. Error greater than 15% occurs only 4 times for the TSV at the edges of the given structure. A maximum error of 20.9% occurs only 1 time, which occurs at the total capacitance of TSVs in sparse substructures exist in the given structure. As expected large error values occurs at total capacitance. As error occurs in total capacitance is cumulative error of all coupling capacitances and self-capacitance of that TSV where total capacitance is summation of all coupling capacitances and self-capacitance. Table.7 shows value of maximum error and average error happen among all the errors in all the capacitances (71(TSV) *x* 72(capacitances) =5112 capacitance).

Table 7 Maximum and average error in all capacitance at reference dimensions of test case structure.

Avg. error (%)	Max. error (%)
0.6751	20.91344

Table.8 shows the maximum error that occurs at all capacitances of each TSV. Table.8 can show the effect of position of TSV on maximum error occurs at all of its capacitances. The number in each cell is the maximum error occurs at each TSV in that position. For example, the number in the cell in top left corner of Table.8 represents the maximum error occurs at all the capacitances of TSV1. Each cell represents position of that TSV in the test structure shown in Figure 4-15. Cell with zero values means that there are no TSVs in that position in the test structure. As expected the maximum error

mostly occurs in total capacitance of each TSV as it contains the cumulative error of all capacitances of that TSV. Moreover, it is noted that larger error occurs at TSVs where it exist in a sparse substructures, in other words, in sparse windows created. The reason of large error in sparse substructures is that window size is small that couldn't capture 2nd inline neighbor capacitance that exists in sparse substructure, with no centric TSV in between the two coupled TSV. In that case the value of 2nd inline capacitance would be relatively large and neglecting it causes relatively large error as the case for TSV60. TSV60 has the largest error as it exists in a very sparse window (substructure) and large coupling capacitance values are neglected, as coupled TSVs with TSV60 that have relatively large coupling capacitance values doesn't appear in the same window.

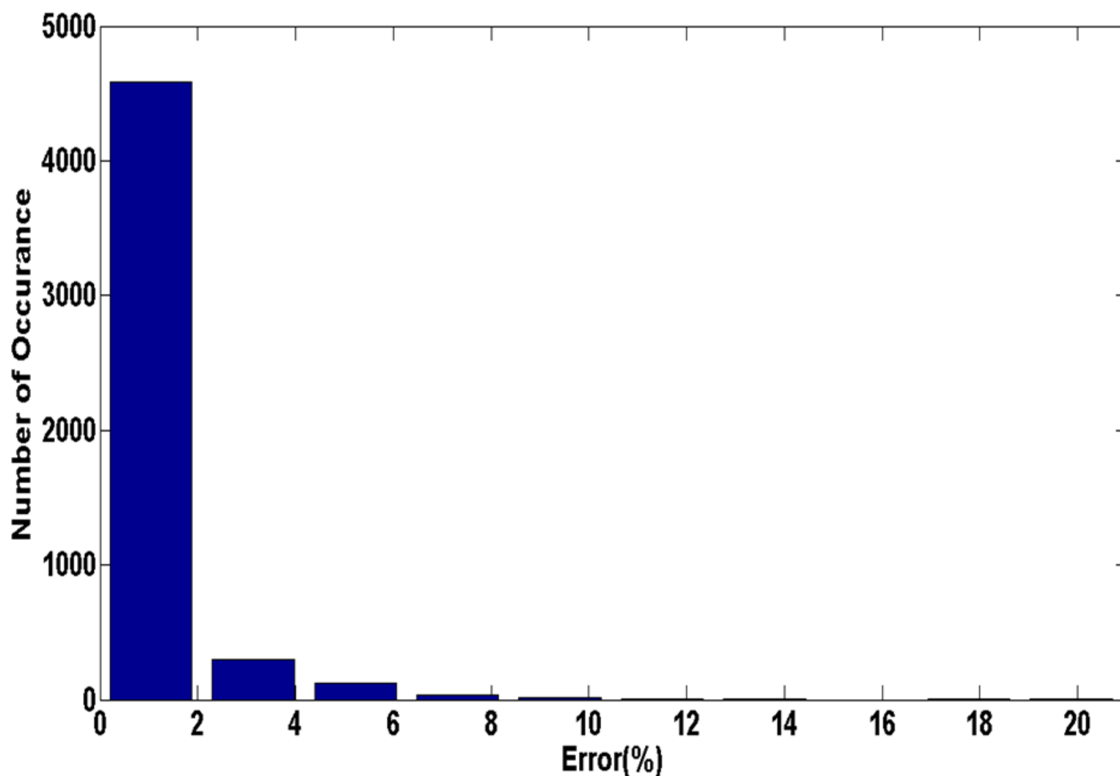


Figure5- 1 Histogram of all capacitance error in 9x9 test case structure at reference dimensions.

A larger error can occur because of neglecting the shielding effect of the TSVs that doesn't appear in the window which results in calculating larger capacitance value than the real value. But solving double counting issue by taking the minimum value could reduce error resulted at those situations. Large error occurs at peripheral TSVs; especially corner TSVs, as they have relatively large 2nd inline capacitances (i.e. fringe capacitance) that are neglected by the algorithm causing a relatively large error. The reason that these capacitances aren't included in the model is that capacitances only calculated between

centric TSV of the window and the other TSVs, so no 2nd inline capacitance type can exist in the final macro-model.

Table 8Maximum error among all capacitances errors for each TSV.

17.873	6.94759	11.2325	11.6570	8.45728	5.82121	6.36742	4.74339	19.017
4.8155	3.89024	0	0	5.82631	6.60088	6.59355	3.71644	4.8547
6.6119	4.03411	6.96985	6.94137	6.08888	0	0	4.41789	6.1248
9.2214	4.35602	4.47566	3.83977	4.58355	6.67967	6.93874	4.12778	7.0689
12.117	0	6.96158	4.53809	7.34916	9.91011	6.99711	4.35324	6.6723
11.823	0	6.83705	6.73851	0	0	0	4.42042	6.8022
8.8306	4.24512	4.52175	6.98299	0	20.9134	7.00458	4.15785	7.0646
5.1476	3.37167	3.75125	4.13681	4.66952	4.05820	3.67873	3.29538	5.1018
19.688	5.6053	8.12102	7.98777	6.73267	7.37016	7.71517	5.50497	19.274

It is shown in Table.7 that average error of all capacitance is 0.68%. Average error is very small because of the large number of capacitances exist and most of them are very small capacitances that can be neglected. Consequently, error caused because of neglecting them is very small. 0.68% average error can't be consider as a realistic average error occurs by the algorithm. It can be noticed from Figure 5-1 that an average error of 4% or 5% would be a more realistic average error caused by using the proposed algorithm, as most of calculated capacitances (not neglected ones) error fill within that range of error. However, error occurs at total capacitance can give a good sign for error caused by using the algorithm as total capacitance represents the cumulative error of all coupling and self-capacitances. A histogram of error occurs at the total capacitance of all TSVs is shown in Figure5-2. It is shown that about 26 TSVs have a total capacitance error less than 2% and most of error occurs at total capacitance of all TSVs is less than 10%. Very few capacitances havelarge error, which occurs at TSVs in sparse windows (substructures) or corner TSVs. An average error of 4.9% occurs for total capacitances of all TSVs.

5.2.2 Algorithm Enhancement for Self-capacitance Error

In previous section, it is found that the error of self-capacitance is relatively larger than error obtained for other coupling capacitances. The main reason is that self-capacitance of each TSV is calculated only once, when it is centered in the sliding window. The number of surrounding TSVs effects on the resulted value of self-capacitance of TSV. Therefore, if the window where self-capacitance of the TSV is calculated inside don't show enough shielding caused by surrounding TSVs so the resulted self-capacitance would have large error. To improve the accuracy of self-capacitance calculation, it shouldn't be calculated only once. Self-capacitance of each TSV can be calculated at

each window that TSV appear inside, not only when it is the centric TSV of that window. In that case more shielding that actually surrounding that TSV can be considered and a more accurate capacitance value for self-capacitance is obtained. Minimum capacitance value is chosen among the list of all calculated self-capacitances values of the same TSV. Table.9 shows self-capacitance error with no enhancement added in the algorithm and with the enhancement. It is clear in that table that error of calculating self-capacitance decreased by adding that enhancement.

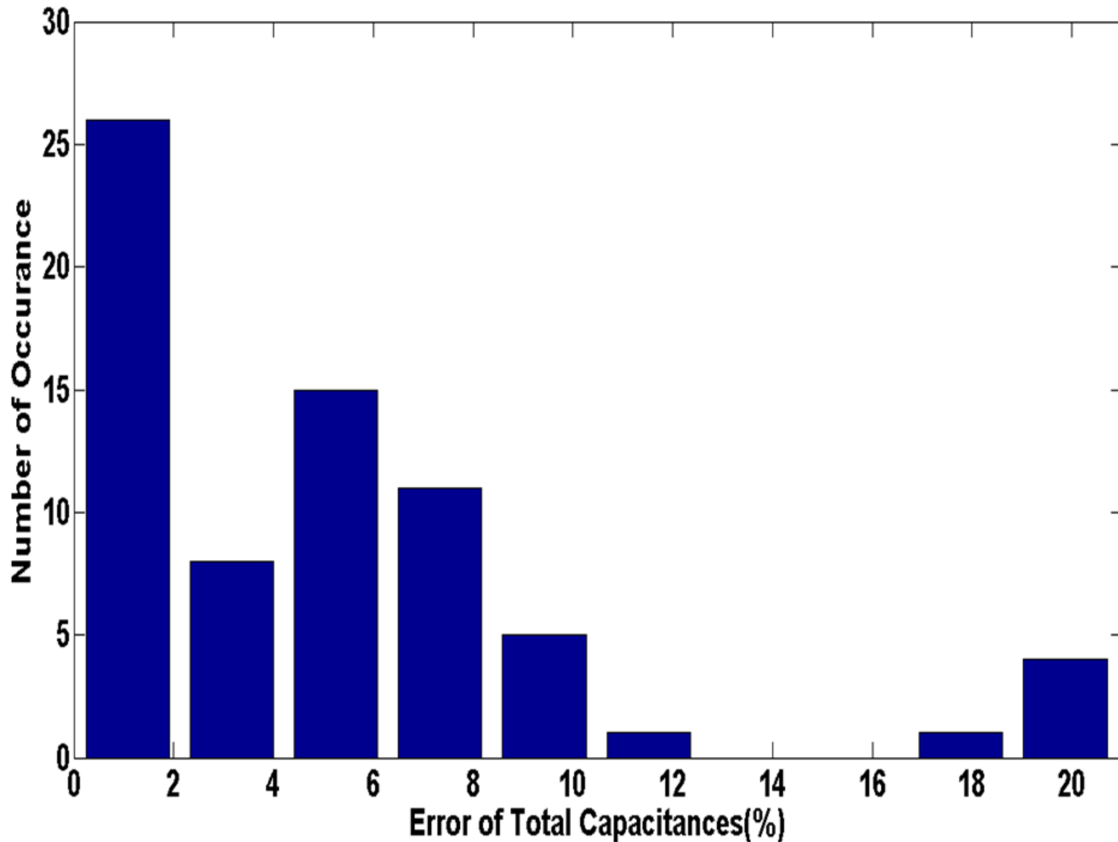


Figure5- 2 Histogram of total capacitances error of all TSVs in 9x9 test case structure.

However, the error in the self-capacitance decreases but the error in the total capacitance increases in return. As there are lots of capacitances are neglected using the algorithm, consequently total capacitance of certain TSV (i.e. in sparse substructures) in Q3D simulation is larger than the corresponding value obtained in the macro-model. The larger value of self-capacitance that causes larger error in the self-capacitance, but on the other hand, it compensates lower total capacitance value obtained by the algorithm. After applying the enhancement on calculating self-capacitance value, lower value for self-capacitance is obtained. Total capacitance value is reduced in the model results in larger error in that total capacitance value. The decreased error in self-capacitance is faced by

an increase in error of total capacitance with the same behavior. Therefore, same average error is obtained for all capacitances (0.6751%) using both enhanced and non-enhanced algorithm. Adding self-capacitance calculation enhancement to the algorithm resulted in increasing maximum error from 20.9% to 25.4% as shown in Figure 5-3.

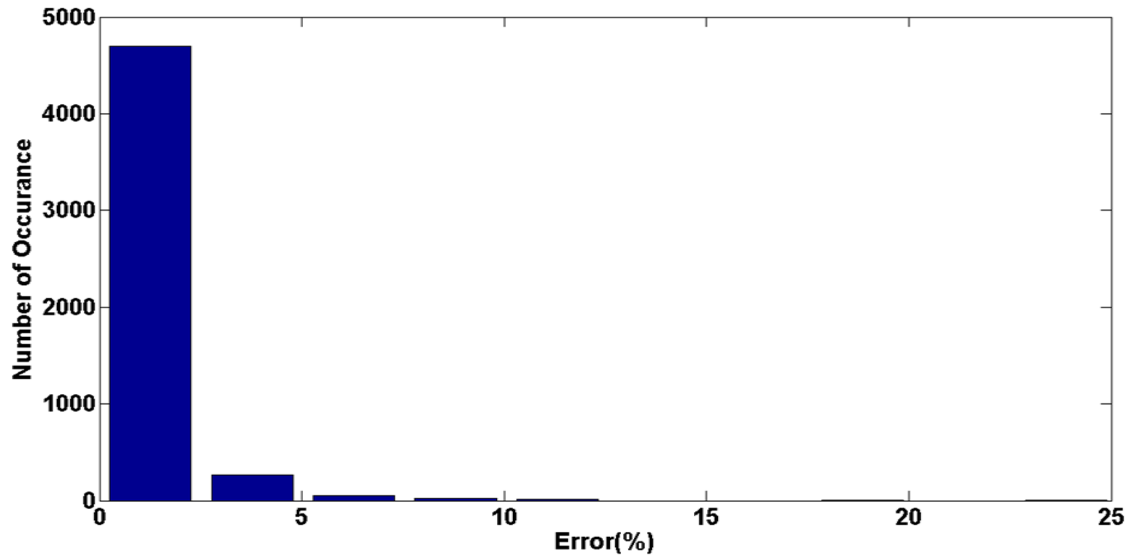


Figure5- 3Histogram of all capacitance error in 9x9 test case structure at reference dimensions, using enhanced self-capacitance calculation in the algorithm.

Table 9 Error in self-capacitance value of some TSVs with and without using method of enhancing self-capacitance calculation.

TSV number	Self Cap. Error (Nominal Alg.)(%)	Self Cap. Error (Enhanced Alg.)(%)
1	9.659416	3.425605
19	6.023167	4.610063
73	9.054871	5.552095

5.2.3 Maximum Error Reduction

As noticed in the previous sections, the value of maximum error occurs due to the algorithm is large. It mainly occurs in total capacitance, and the main reason for that is the large amount of capacitances neglected through using the algorithm in very dense structure like our test case. Mostly the calculated total capacitance value from the algorithm is lower than the actual total capacitance value obtained using Q3D. Main reason of having lower total capacitance calculated from the algorithm is using minimum double counting technique to solve double counting issue, which results in better

accuracy for the calculated coupling capacitance. But on the other hand, if average double counting technique is used instead of minimum double counting technique, the error in estimating the coupling capacitance value increases relatively. However error in calculated total capacitance of each TSV is reduced, as average double counting technique over estimate the value of coupling capacitance. That larger value of coupling capacitance compensates the value of capacitances neglected due to using the algorithm and results in more accurate total capacitance value at most of TSVs. That can be shown in histogram in Figure 5-4, where maximum error occurs improved to be 14.5% using average double counting technique, instead of 20.9% using minimum double counting technique. In addition, there is unmentionable increase in the average error of all capacitance values from 0.68% to 0.72%. The increase in average error is due to the increase in error of coupling capacitances where number of coupling capacitances exist in the resulted macro-model is larger than number of total capacitances. To have better figure of average error occurs due to using the algorithm, its better to notice the average error occurs in total capacitance value and the distribution of that error as presented in Figure 5-5. However some of total capacitance error increased slightly, but lots of total capacitance error decreased and also maximum error occur to total capacitance decreased. As noticed the average error of total capacitance values reduced from 4.9% to 4.25% due to using average double counting technique instead of minimum double counting technique. Consequently, using average double counting technique improved accuracy of both maximum error and average error as it improved accuracy of total capacitance calculation where maximum error occurs.

5.2.4 Simulation at Different Dimensions

In previous section, simulations are done at the reference dimensions so the resulted error is an algorithm error. The final error of the macro-model wouldn't only be algorithm error, but it is the cumulative error results from both algorithm and the use of scaling equation when dimensions change from reference dimensions. In this section different structure with different dimensions are simulated using algorithm and Q3D to notice the change in maximum error and average error due to adding effect of scaling equation. From previous chapter, dimensions that caused largest error because of using scaling equation are obtained. These dimensions are simulated in the test case structure using both algorithm and Q3D extractor in order to get a figure of maximum cumulative error occurs from both algorithm and usage of scaling equation. That can give maximum error that can occur in the macro-model, and the corresponding average error.

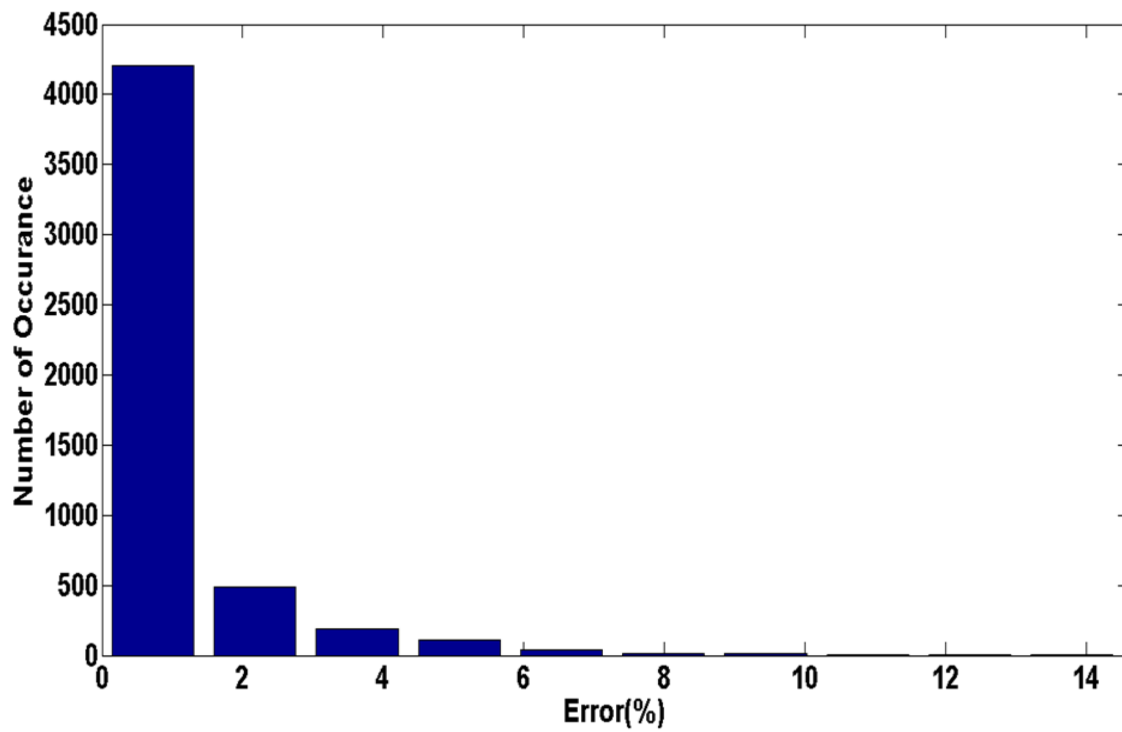


Figure5- 4Histogram of all capacitance error in 9x9 test case structure at reference dimensions using average double counting.

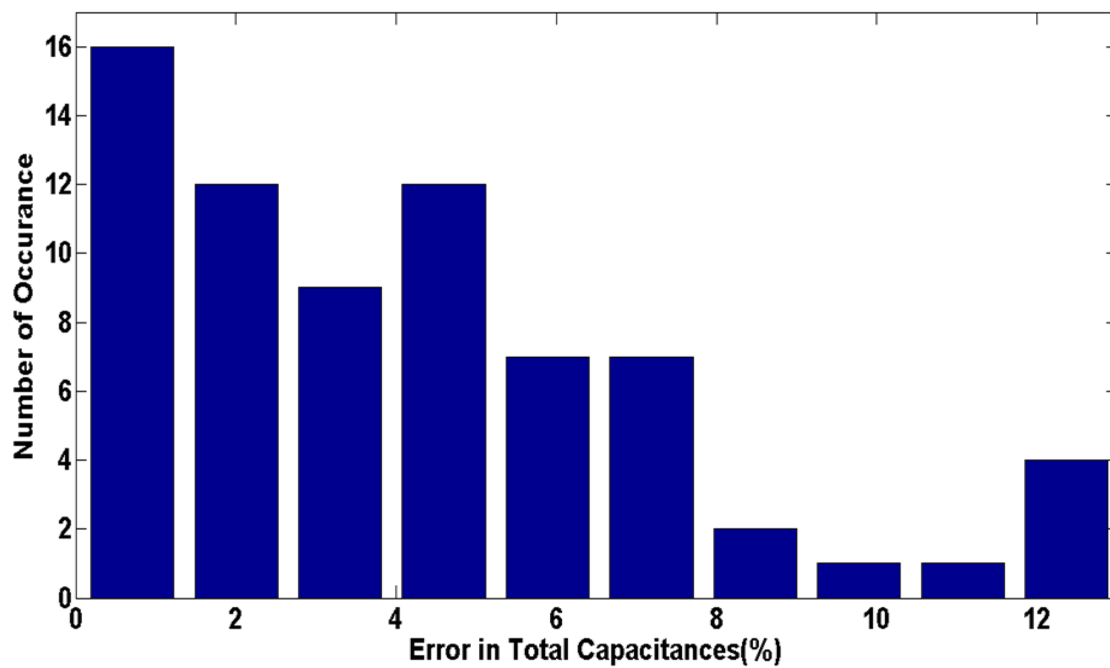


Figure5- 5Histogram of total capacitances error of all TSVs in 9x9 test case structure using average double counting.

Histograms shown in Figures 5-6 is for number of occurrence of errors of all capacitances at s_{tsv}=85um, r_{tsv}=8.5um, t_{ox}= 0.3um, l_{tsv}=50um. s_{tsv} and r_{tsv} changed from reference dimensions, while t_{ox} and l_{tsv} are kept at reference dimensions. As noticed in Figure5-6, due to dimension scaling and the use of scaling equation maximum error increased by 5.5% (from 20.9% to 26.4%), with slight increase in average error from 0.675% to 0.678%. Which mean that error in most of capacitances values doesn't increase, but large increase in maximum error with nearly same average error means that error decreased in some of capacitances while an error increases occurred to few capacitances. Using average double counting technique instead of minimum double counting technique resulted in lower maximum error of 19.9% as shown in Figure 5-7. The increase of error in average double counting technique due to usage of scaling equation is the same as in minimum double counting technique (increased by 5.5% from the maximum error occurred at reference dimensions). Also average double counting technique resulted in same average error as in case of minimum double counting technique.

Usage of scaling equation doesn't mean that maximum error and average error always increases. For certain dimensions, the use of scaling equation would results in improving the accuracy of the macro-model, resulting in lower maximum error and lower average error. As in the case shown in Figure 5-8 (@ s_{tsv}=25um, r_{tsv}=6.5um, t_{ox}=0.5um) where maximum error decreased to be 14.2% and average error decreased to be 0.49%. Table.10 shows maximum error and average error for all capacitances and for total capacitance for test case structure at different dimensions. Simulations for dimensions that caused maximum error in characterization are done, in order to know range of maximum error that can occur from both algorithm and usage of scaling equation. It turned out that maximum error is about 19.9%, maximum average error for all capacitances is 0.78% and maximum average error for total capacitances is 8.2%.

5.3 Hybrid Algorithm

In previous sections, further enhancements for the algorithm in order to reduce maximum error occur by the algorithm and to reduce error occurs while calculating self-capacitance of each TSV are done. To reduce self-capacitance error, self-capacitance of each TSV is calculated at different windows in order to capture more shielding effect. Thereafter, minimum value among all calculated self-capacitances of same TSV is chosen, where it would be the more accurate one as it resulted from capturing more shielding effect which it actually exist. Maximum error occurs at certain positions in the given structure which are:

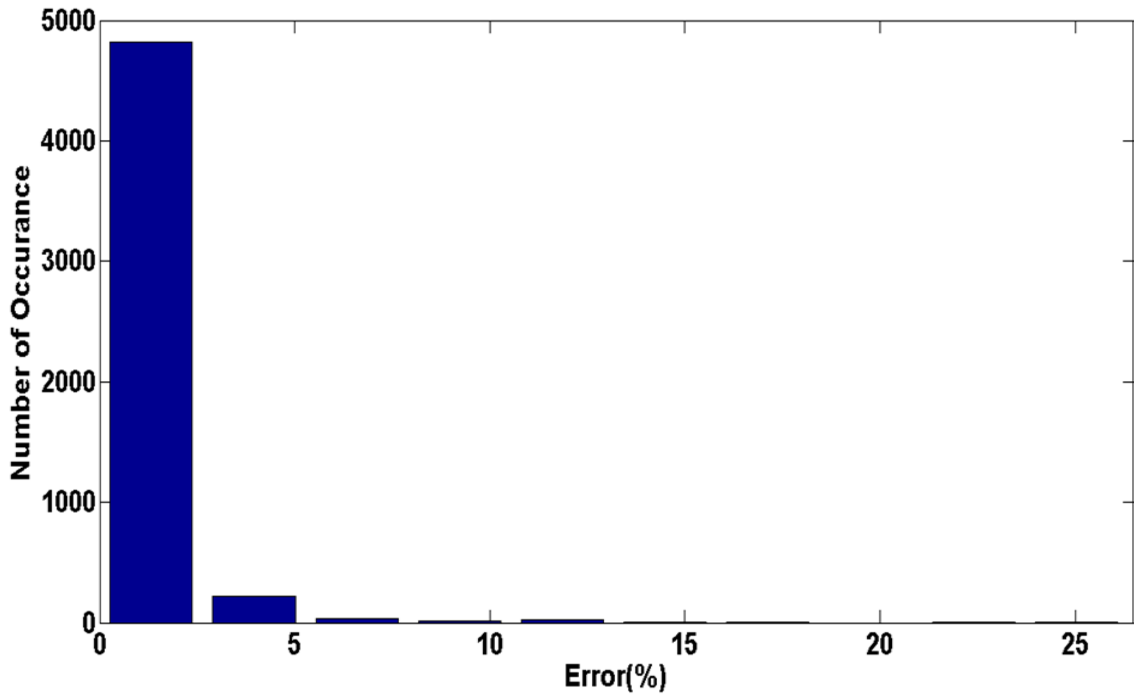


Figure5- 6Histogram of all capacitance error in 9x9 test case structure at stsv=85um, rtsv=8.5um, tox= 0.3um, ltsv=50um using minimum double counting.

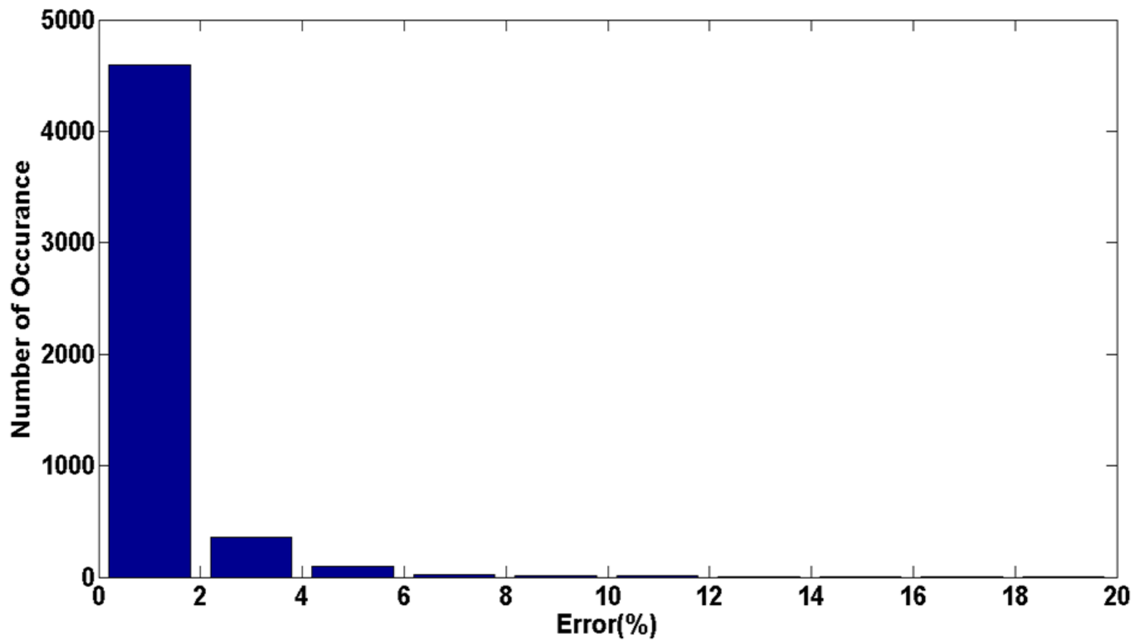


Figure5- 7Histogram of all capacitance error in 9x9 test case structure at stsv=85um, rtsv=8.5um, tox= 0.3um, ltsv=50um using average double counting.

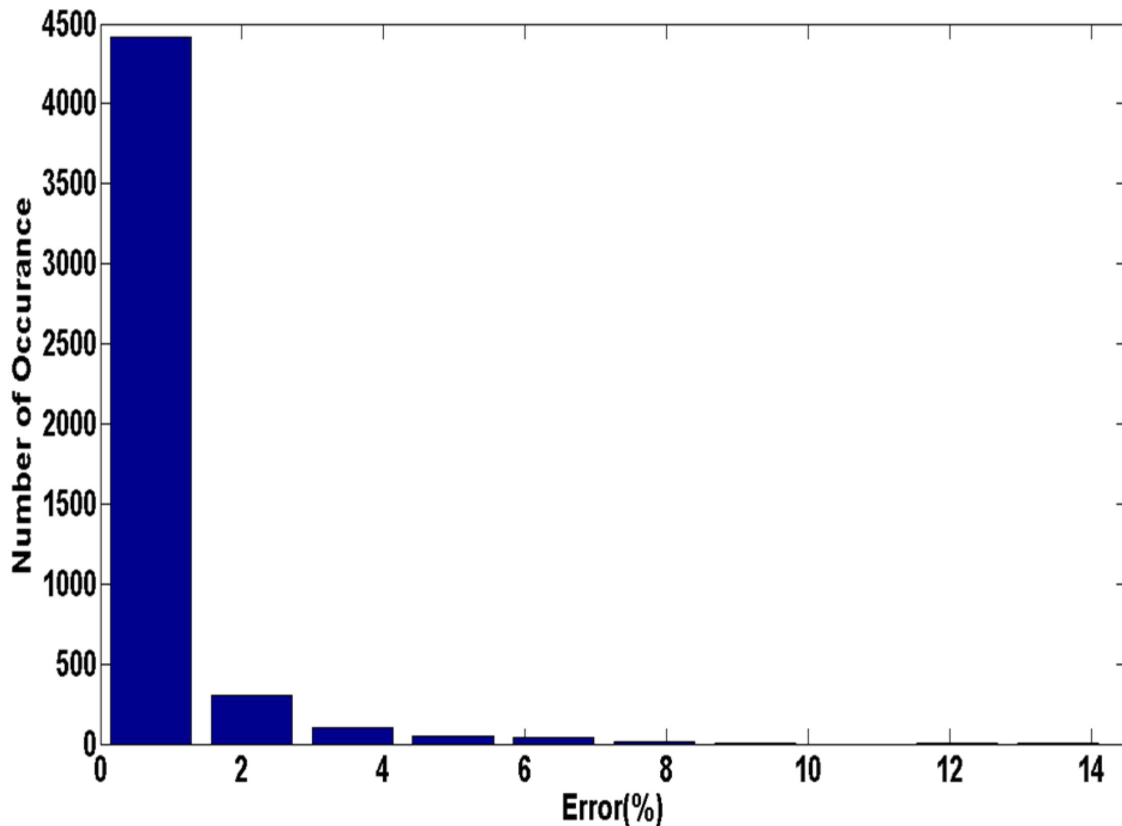


Figure5- 8Histogram of all capacitance error in 9x9 test case structure at stsv=25um, rtsv=6.5um, tox= 0.5um, ltsv=50um using average double counting.

Table 10 Maximum error and average error for test case structure with different dimensions using average double counting technique.

Dimensions (um)			Maximum Error	Average Error (all capacitances)	Average Error (total capacitances)
tox	rtsv	stsv			
0.2	2.5(r)	45	18.5447	0.7812	7.29
	4.5	35	14.0702	0.6297	3.0035
0.3(r)	8.5	85	19.9517	0.6789	8.2
0.5	6.5	25(r)	14.2324	0.4893	2.6354
	10.5	85	19.6215	0.6370	6.9103

1- Corner TSVs: in that case there would be two 2nd inline capacitances (i.e. fringe capacitance) on the two sides of the array, and there values are relatively large. Neglecting these capacitances causes large error in total capacitance of those TSVs, as the estimated total capacitance value would be smaller than the actual total capacitance value. To reduce error in these position, average double counting technique is used, where the value of coupling capacitance between those TSVs and there surrounding is overestimated. The resulted total capacitance would be close from the real value of total capacitance value.

2- TSVs in sub-sparse structures (sparse windows): these TSVs have empty positions around them, that made window created on them don't capture coupling effect caused by their second neighbor TSVs that don't appear in the same window due to the small window size used in the algorithm. These second neighbor TSVs are considered as direct neighbor for these TSVs as there is no shielding TSVs exist in-between. For example, in test structure in Figure 4-15, TSV60 fill inside a sparse sub-structure, where the window created on TSV 60 doesn't contain surrounding TSVs like TSVs (41, 42, and 43). Therefore, coupling capacitance between TSV60 and these TSVs wouldn't be included in the resulted macro-model, however, a relatively large coupling capacitance between TSV60 and these TSVs exist. Neglecting these capacitances causes a relatively large error in total capacitance of TSV60. Using average double counting technique, reduces maximum error in TSVs in these positions, but still other modifications for the algorithm can be done in order to reduce maximum error occurs in these TSVs. These modifications are presented in next part.

There are different algorithms that can be used to build the macro-model, but the main limitation is the need for accurate equations that can calculate different capacitances types and consider different effects. Especially it is needed that these equations include shielding effect results due to existence of other surrounding TSVs. Another algorithm is to use a scanning line or scanning cone as shown in Figure5-9a. The line or cone moves on each TSV in the array and while it is sit on the TSV it starts to rotate by 360° to capture all surrounding TSVs and calculate coupling capacitances between current TSV and the surrounding ones. The angle by which that line is moving is an important parameter, whereas this angle decreases more surrounding TSVs are captured. In addition, as this angle is larger, fewer surrounding TSVs are captured. Using that algorithm a library based technique wouldn't bepossible, as there are very large numbers of cases that has to be handled. The suitable technique for that algorithm would be model based technique, with a set of equations that can cover these different cases.

In our work as it is simulation based technique, so the scanning line algorithm can be used to enhance the resulted capacitance matrix from our proposed algorithm. After the sliding window finishes its work and build the macro-model, another run can be done using the scanning line that moves on each TSV try to capture more capacitances that sliding window didn't succeed in capturing, as in the case described before for TSV60. The scanning line sit on each TSV in the given structure and start to rotate till it make a full round with 360°. The angle of rotation is chosen to be 45°, as our window size is $3x3$ so there is a total of 8 possible surrounding TSVs for the centric TSV in a $3x3$ window size.That means there is a 45° angle difference between each two consecutive TSVs of those 8 TSVs. Choosing the angle step to be 45 means the line search in the same positions of the surrounding TSVs exists in the same window. The line moves in eight directions as shown in Figure 5-9b. In case a window isn't full of TSVs which means

there are empty positions, this line can get other TSVs in the same direction of empty positions that couldn't be captured by the window. Some of these TSVs aren't expected to be so far as dense structures are the considered structures in this work. Consequently, when the line hit a TSV, if that TSV is 1st inline or 1st diagonal, then its capacitance is already calculated using the sliding window and no need to be calculated again as the capacitance already calculated by sliding window would be more accurate. While incase it's not a 1st neighbor then no capacitance is already calculated between these two TSVs, and an equation is needed to calculate this capacitance. As shown in Figure 5-9b red line is for coupling capacitances that are added by scanning line and blue line are for capacitances that already calculated using sliding window and wouldn't be calculated using scanning line. Equation of calculating coupling capacitance between two unshielded TSVs proposed in equation (24) can be used to calculate the capacitance discovered by scanning line. A coefficient γ is added to capture the shielding effect caused by surrounding TSVs, where its value varies with the number of surrounding TSVs to the TSV of interest (i.e. scanning line is sit on it).

$$\mathbf{Cc} = \gamma \frac{\mathbf{0.9\ \pi\varepsilon L}}{\mathbf{cosh^{-1}}\left(\mathbf{1}+\left(\frac{\mathbf{stsv+\ tox}}{\mathbf{rtsv}}\right)\right)} \tag{24}$$

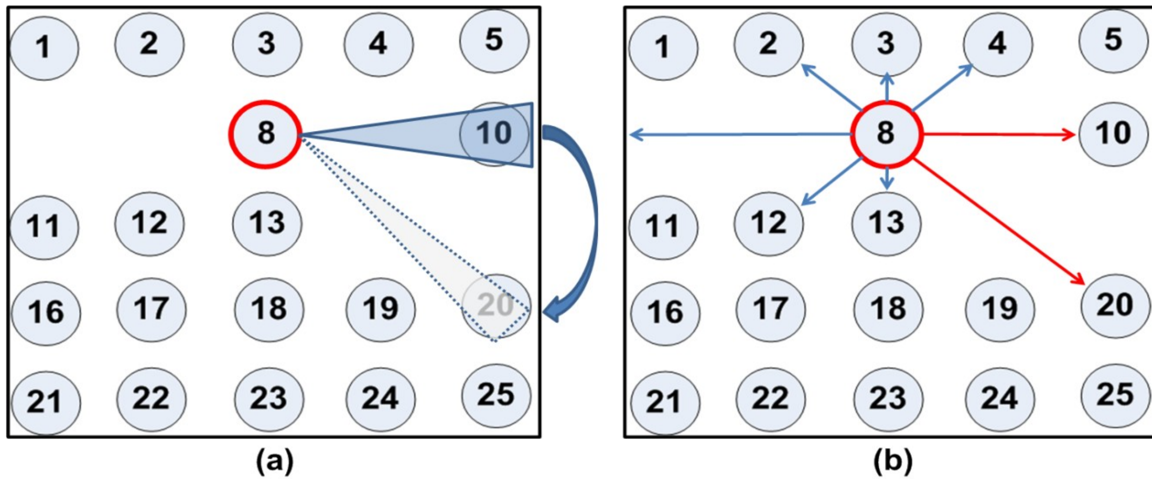


Figure5- 9 (a) Scanning line algorithm, (b) Scanning line at eight angles.

The hybrid algorithm is applied on the test structure shown in Figure 4-15, an improvement of the maximum error is resulted. Maximum error reduced from 20.9% to 19%, with using minimum double counting technique and no enhancements for calculating self-capacitance is added. That maximum error occurs at corner TSVs, which can be solved using average double counting technique, and also enhancements in calculating self-capacitance values are added. Results of adding all enhancements to the algorithm are shown in histogram in Figure 5-10. As it is shown in Figure 5-10,

maximum error caused by the algorithm is improved from 14.5% to be 12.5%, and the average error cause in all total capacitance slightly increased to be 5.5%. That increase is due to using enhancements in self-capacitance calculation which led to increase in error in some total capacitances led to the slight increase in total capacitances average error as shown in Figure 5-11. Moreover hybrid algorithm is applied to the test structure at different dimensions to find maximum error resulted from accumulation of both algorithm and usage of scaling equation. As shown in Table.11, at dimensions that caused maximum error in the characterization of 3*x*3 windows, maximum accumulative error occurred as a result of using hybrid algorithm reduced from 20% to be 18.2%, with an average error in total capacitance values within range 3.3% to 6.6%.

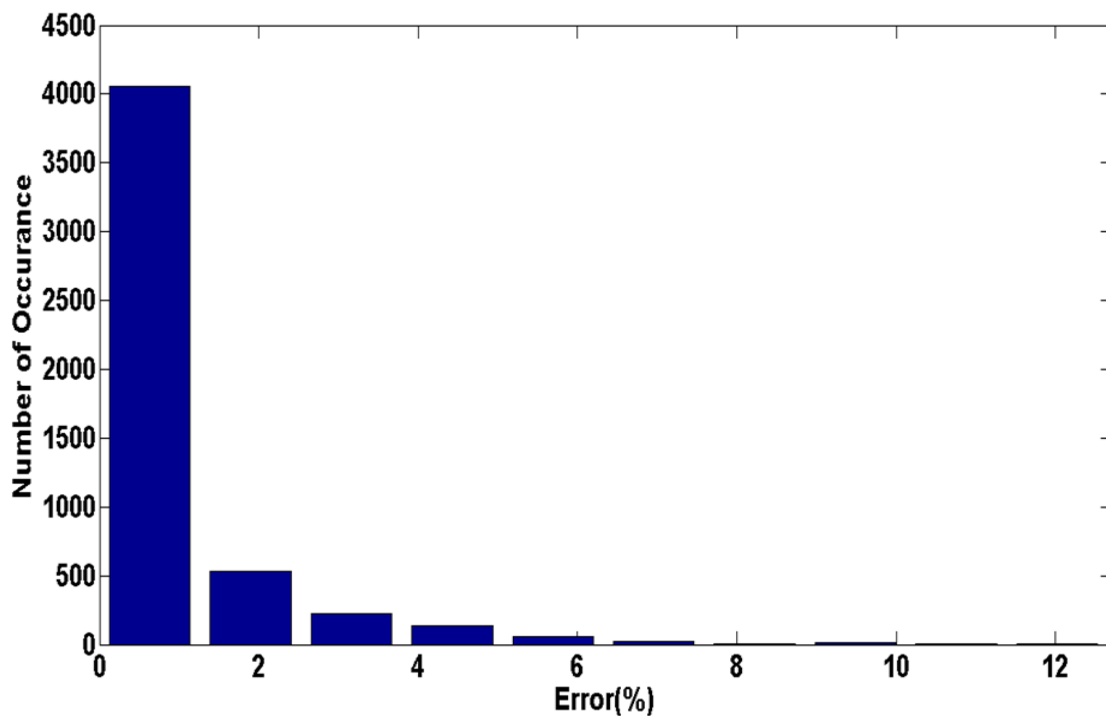


Figure5- 10Histogram of all capacitance error in 9x9 test case structure at reference dimensions using hybrid algorithm with average double counting technique and enhancements in calculating self-capacitance value.

In conclusion, in this chapter different tools and technique that can be used to get accuracy of algorithm in building the macro-model are illustrated. In this work Q3D extractor is used as a golden reference and capacitance error calculation for all capacitances is used to get the accuracy of algorithm in building the macro-model. Thereafter, the metric used to calculate the error in each capacitance in the capacitance matrix of the macro-model is defined. That metric measures the error in the capacitance with respect to its effect on the total capacitance (i.e. its ratio from total capacitance).

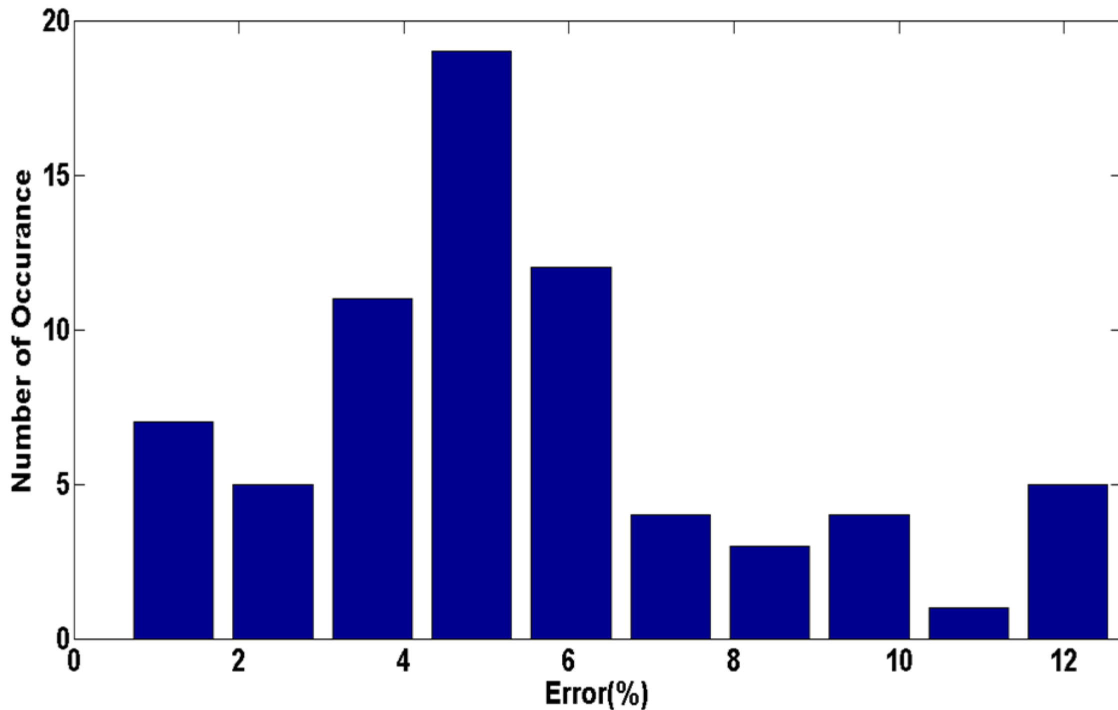


Figure5- 11Histogram of total capacitance error in 9x9 test case structure at reference dimensions using hybrid algorithm with average double counting technique and enhancements in calculating self-capacitance value.

Table 11Maximum error and average error for test case structure with different dimensions using hybrid algorithm with average double counting technique and adding self-capacitance calculation enhancements.

Dimensions (um)			Maximum Error	Average Error (all capacitances)	Average Error (total capacitances)
tox	rtsv	stsv			
0.2	2.5(r)	45	18.2	0.7468	5.7
	4.5	35	11.13	0.6299	4.17
0.3(r)	8.5	85	18.2	0.6425	6.6
0.5	6.5	25(r)	12.2	0.4841	3.4
	10.5	85	15.8	0.6031	5.6

Total error has two sources: algorithm error and usage of scaling equation error. Maximum algorithm error of 20.9% and average algorithm error of 0.67%are calculated for the chosen test structure (@ reference dimensions). After that, it is found that average error of total capacitance would give a better estimate of average error resulted by the algorithm, as total capacitance error is the cumulative error of all coupling and self-capacitance of a TSV. An algorithm average error of 4.9% is found that is the average error of total capacitances of all TSVs. Then some enhancements in the algorithm are done to get better accuracy for calculating self-capacitance value, by getting a value of self-capacitance of each TSV from different windows. Using self-capacitance calculation enhancement lead to decrease in error of self-capacitance but resulted in increase in maximum error occurs from the algorithm. Thereafter, it is discovered that average

double counting technique would give better accuracy than minimum double counting technique. Maximum error using average double counting reduced to be 14.5% with reduction in average error of total capacitance to be 4.25%. Subsequently, simulations for the test structure at different dimensions are done in order to get the cumulative error resulted from both algorithm and scaling equation usage. It turned out that maximum error is in the range of 14% to 19.9%, and average error of total capacitance is in the range of 2.6% to 8.2% for different dimensions. Moreover, it is found that using of scaling equation doesn't always mean adding more error for the macro-model but at some dimensions it do improves the macro-model accuracy. That is mainly due to existence of two types of errors (positive and negative error) resulted from usage of scaling equation. Therefore, scaling equation error can cancel the effects of algorithm error which results in some cases in a better accuracy. After that scanning line technique is added to sliding window technique to formulate the hybrid algorithm. With the aid of average double counting technique and adding enhancements of calculating self-capacitance values resulted in improvements of maximum cumulative error to 18.2% with an average error range from 3.3% to 6.6%. The maximum error range is obtained by simulating dimensions that resulted in maximum error while doing characterization shown in chapter 4.

Chapter 6

Conclusion, Recommendations and Future Work

In this chapter, conclusions from the results obtained in previous chapters are presented, giving some recommendation of how to do modifications for the algorithm to get better results. In addition, recommendations for getting better results from characterization are presented. Thereafter, pointing out to some plans for future work in order to improve the accuracy of the model.

6.1 Conclusion and Recommendations

This work proposes an algorithm for building a macro-model for TSV array. The proposed algorithm is a simulation based algorithm which is using a LUT that contains capacitance values at reference dimensions. With the aid of a scaling equation, capacitance values can be calculated at different physical dimensions.

It can be concluded that coupling capacitance between any two TSVs, vary with count of surrounding TSVs, due to shielding effect caused by existence of other surrounding TSVs. Therefore, as count of surrounding TSVs increases the coupling capacitance decreases. Moreover, it is shown that the main reason for choosing a window size of 3x3 in the implemented window scanning technique is that number of possible structures increases exponentially with the increase of the window size. Also, it is shown that number of possible structures can be decreased by excluding redundant structures. Redundant structures have the same capacitance matrix but they are just rotated or mirrored versions of each other. Excluding redundant structures and only considering structures that contain centric TSVs resulted in an order of magnitude reduction of possible sub-structure count of window size $3x3$ from 512 to 51 unique structures. Even with excluding redundant structures, number of possible structures for larger window size is still unmanageable. Consequently in this work, we do not use larger window sizes for simulation based technique. However in model based technique, set of equation can describe model parameters and it is expected to work with different sub-structure. May be in that case, it would be easier to use larger window sizes, as a LUT wouldn't be required and also no characterization is needed for all structures to get variations in model parameters values with dimension scaling.

There are different scenarios in order to do characterization for different TSVs structures. Characterization is required to get coefficients which suit the scaling equations in order to capture variations occur to capacitance values with dimension scaling. This step is discussed for different capacitance types (inline, diagonal and total capacitance) and in different scaling scenarios (changing pitch only, radius only, tox only, both pitch

and radius only, both pitch and tox only, both radius and tox or the three parameters). The scenario that is expected to give most accurate results is to do characterization per structure (for each structure) and for each capacitance type in that structure. We consider this scenario while conducting the characterization process. However, this technique is very complex and takes lots of time but it is expected to give better accuracy. Other scenarios which produce lower number of coefficients can be tested in order to compare it with the exhaustive scenario.

Optimization goal affects the resulted accuracy of scaling equation usage, where it affects the final value of the coefficients to be used in scaling equation. It is recommended to consider both positive and negative errors while doing optimization to get coefficients value, and not the absolute of each of them. It is also recommended to guide the optimization algorithm to give the coefficients that give the maximum error to be a negative error and try to reduce the maximum positive error in dense window structures. As dense window results in a positive algorithm error, so when the scaling equation error is negative, both negative and positive errors cancel each other. In addition, guide the optimization algorithm to give coefficients that give maximum error to be positive error and try to reduce maximum negative error in sparse window structures. As sparse window results in a negative algorithm error (especially in total capacitance), so when the scaling equation error is positive, both negative and positive errors cancel each other.

Several enhancements are added to the algorithm in order to get better accuracy of the resulted model. Comparison between maximum error occurs at each of these enhancements is shown in Table.12. First enhancements are done in the way of calculating self-capacitance value to reduce error occurs in the calculated value. Then, discovered that usage of average double counting technique instead of minimum double counting technique improved maximum error occurs by algorithm from 20.9% to 14.5% with decrease in average error occurs in total capacitances from 4.9% to 4.2%. Finally, using hybrid algorithm of sliding window followed by scanning line, in addition to enhancements in calculating self-capacitance value and usage of average double counting technique, resulted in improving accuracy of maximum error to be 12.5%.

Our proposed algorithm is compared with an algorithm proposed in [20] and comparison is shown in Table.13. Their algorithm is model based that uses scanning line technique. A set of equations are used to calculate different capacitances exist between TSVs. But as shielding effect of surrounding TSVs isn't considered in their model, and then it is suitable for sparse structures. That can be shown from their test cases that only contain 9 TSVs as a maximum, while our algorithm targets dense structures. Also, their TSV technology is square shaped, which is different than our TSV technology,

cylindrical shape. Cylindrical shape is more common due to technology issues. Our algorithm was tested in different structures and a maximum error for different dimensions of 18.2% is obtained with an average error range 3.3 to 6.6%. While their algorithm has a maximum error of 19% and average error range 8.18-11.86%.

Table XII Comparison between maximum errors obtained in different techniques.

Maximum Error (%)	Basic Alg.	Self Cap. Enhancement	Total Cap. Enhancement	Hybrid Alg.
Without scaling	20.9%	25%	14.5%	12.5%
With scaling	26.4%	29%	19.95%	18.2%

Table 13 Comparison between algorithm in [20] with our proposed algorithm.

Comparison	Our Algorithm	Georgia Tech. Algorithm
Macro-model Technique	Simulation Based (LUT)	Model Based
TSV technology	Cylindrical shape	Square shape
Structure Type	Dense	Sparse
Golden Reference	Q3D Extractor	Raphael
Algorithm technique	Sliding window	Scanning line
Time Elapsed	Negligible time	Negligible time
Maximum Error	Hybrid algorithm (18.2%)	19%
Average Error	Hybrid algorithm (3.3-6.6%)	8.18- 11.86%

6.2 Future Work

In this section, further improvements for the proposedalgorithm which can be done as a future work are discussed. Also, other perspectives that aren't considered during the scope of this work and left for future work are highlighted.

6.2.1 Algorithm Enhancements

As discussed in previous chapters, that the proposed algorithm is a sliding window technique where the window stand on only positions that contain TSVs while the window bypass empty positions in the given array. That is the reason of reducing number of possible sub-structure for a window size of 3*x*3 from 512 to 256 sub-structures. After removing redundant sub-structures, number of possible sub-structures reached 51 unique sub-structures. However accuracy of the resulted macro-model can be improved by adding two enhancements to the algorithm:

1- Instead of just calculating capacitances between centric TSV and other surrounding TSV in the window, also capacitances can be calculated between all TSVs in the window. That is expected to enhance the accuracy of the model, especially for TSVs on edges. As discussed in previous chapters, there is large error occurs in edges TSVs as

fringe capacitance in these cases have relatively large values and neglecting them add relatively larger error for the model. Therefore, calculating capacitance between all TSVs in the window is going to capture those fringe capacitances (i.e. 2nd inline or 2nd diagonal capacitances) which are going to add for accuracy of the model. Moreover, it is expected that average double counting technique wouldn't be required after adding this enhancement and instead we can use minimum double counting technique. As by adding these fringe capacitance to the resulted model, no need for over estimating capacitance values in order to reduce total capacitance error. But adding that enhancementadds extra complexity to the algorithm and a larger library is needed. Where the library size is going to increase by 8 times the current size. That is needed to be experimented and notice if the improvements in accuracy deserve the added complexity or not.

2- Window wouldn't only stop by positions that have TSVs, but it stops in empty positions too. That it is like creating fake TSVs in these empty positions. By adding this enhancement to the algorithm, important 2nd inline capacitances can be captured. As for the case where there are two neighbor TSVs with an empty position in between, using old algorithm, coupling capacitance between both of them couldn't be found. While using the enhanced technique, it can capture this kind of coupling capacitances. But adding this enhancement, adds an extra complexities to the algorithm in return. The added complexities are:

a- Instead of just calculating capacitance between centric TSV and the surrounding in the window, the previously mentioned enhancement in 1 has to be included. As there are some cases with no centric TSVs, so capacitance needs to be calculated between all TSVs exist in the window. That means larger library is needed, and more complexity is added.

b- Number of possible sub-structure is going to increase, as reduction that is caused by just having sub-structures with centric TSVs, is removed. After removing redundant sub-structures total number of possible unique sub-structures in that case is found to be 92 unique sub-structures. This enhancement increases number of possible sub-structures from 51 to 92 sub-structures. That means larger library, more coefficients and characterization are needed for more sub-structures in case of using per structure technique in characterization. That should be experimented in future work to see if the added accuracy in the model deserves these added complexities or not.

6.2.2 Other Perspective

In this part other perspectives that aren't considered in our algorithm and can be considered in future work are discussed in the following points:

1- Resistive coupling that exists between TSVs can be included in the model and study its effect on performance of TSVs to see if it is important to be considered in the

model or not. In case it is important, another scaling equation is needed for resistive coupling to capture variations in coupling resistance with dimension scaling.

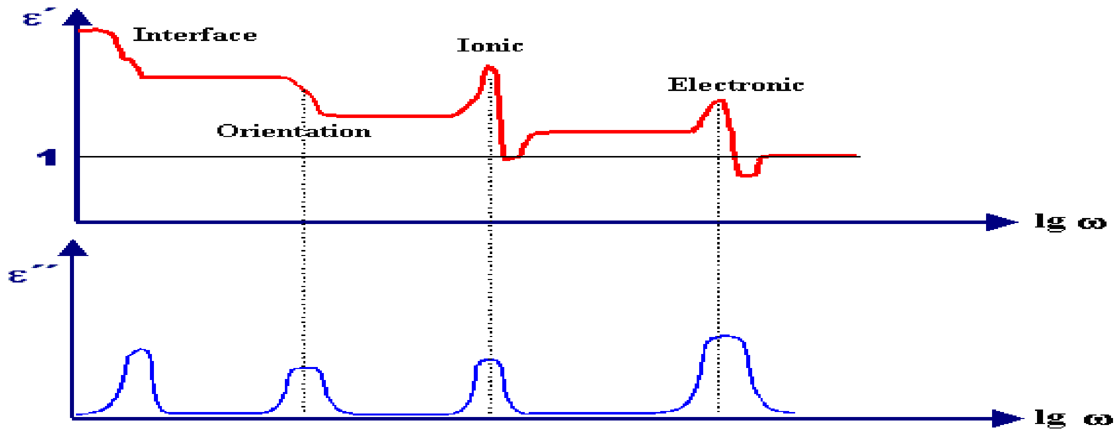


Figure 6-1Dielectric constant relaxation versus frequency. [32]

2- Finding another scaling equation for self-capacitance. As it has different behavior from coupling capacitance and that is expected to add more accuracy in calculation of self-capacitance value.
3- Add frequency dependency to the algorithm and hence to the macro-model.As the operating frequency affects a lot the value of capacitances, mainly due to variation of dielectric constant with frequency as shown in Figure 6-1. Figure 6-2 shows that variation of coupling capacitance value with frequency. Frequency dependency can be considered in the algorithm by adding extra components in coupling branch between two TSVs in the macro-model just to capture the frequency dependency of capacitance values or other coupling parameters.

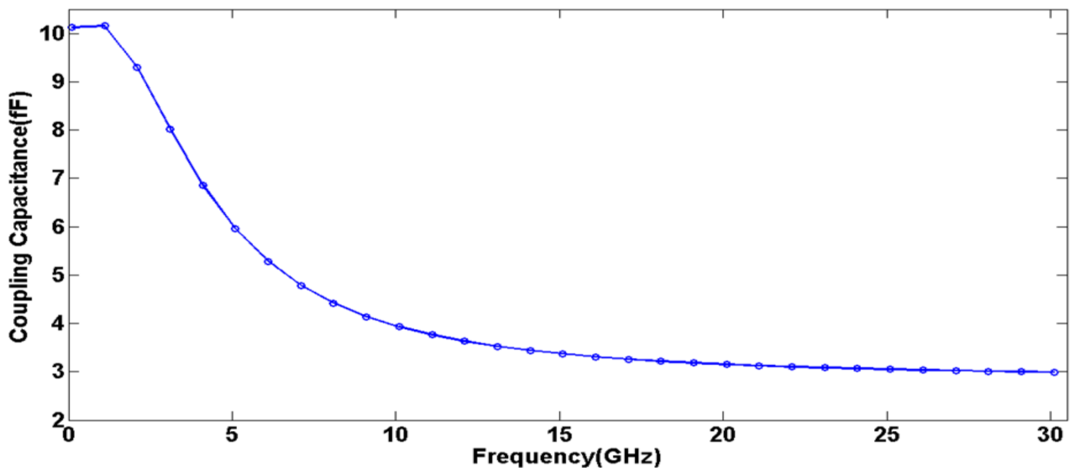


Figure 6-2 Coupling capacitance variation with frequency.

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